Physics-based Scalable Compact Model for Terminal Charge, Intrinsic Capacitance and Drain Current in Nanosheet FETs

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Abstract

This work presents a physics-based SPICE compatible model for Nanosheet FETs, which provides explicit expressions for the drain current, terminal charges and intrinsic capacitances. The drain current model is based on the drift-diffusion formalism for carrier transport. The terminal charge and intrinsic capacitance models are calculated by adopting the Ward–Dutton linear charge partition scheme that guarantees charge conservation. The model uses the novel bottom-up approach to calculate the terminal charges, uses very few empirical parameters and is accurate across device dimensions and bias conditions.

Keywords: terminal charges, nanosheet FET, Ward-Dutton, quantum confinement, bottom-up scalable compact model

Introduction

The Nanosheet FET (NsFET) is the leading architecture for extending CMOS technology scaling beyond the 5 nm node. It offers superior gate electrostatics with negligible short-channel effects [1]-[2]. Fig. 1 shows the schematic diagram of a NsFET with extremely thin body (H) and width (W). For such a system, the Quantum Mechanical Confinement (QMC) induced effects significantly impact device performance [3], results in the formation of sub-bands, thereby affecting the density of states (DOS). This phenomenon also affects the inversion charge density and is more pronounced in thin and narrow NsFETs. Therefore, to accurately reproduce NsFET Current-Voltage (I-V) and Capacitance-Voltage (C-V) characteristics, it is essential to calculate and incorporate accurate sub-band energy levels within the compact model. Recently, a few compact models addressing electrostatics and transport in NsFETs have been proposed [4]-[6]. For instance, a recent extension of Berkeley Short-channel IGFET Model (BSIM) introduced a model that incorporated sub-band information using empirical equations with several fitting parameters, which makes the model prone to convergence issues and also loses its physical insight [4]. The authors in [5] had proposed a Lambert function-based electron density model with additional sets of empirical equations and also assumed an effective 3D DOS, thereby neglecting the effect of QMC. The authors in [6] introduced a surface potential model with some correction factors, which may increase the complexity of the model. Note that, the models proposed in [4]-[5] were orientation independent, however due to the non-planar nature of NsFET channel, the different crystallographic orientation of NsFET sidewalls leads to varying impact on device performance [7]. Recently, a bottom-up compact model was developed, which modified the sub-band energy calculation of an infinite potential well to capture the wave-function penetration in an explicit manner [8]. This allowed accurate calculation of any number of sub-bands without use of fitting parameters for the entire range of narrow/thin to wide/thick geometry in a computationally efficient manner. The model also accounts for surface orientation, width scaling and thickness scaling by using effective mass as a function of channel orientation and transport direction [7]. A terminal charge model is also required for dynamic behavior calculations, enabling AC and transient circuit simulations for NsFET. In this work, the bottom-up core compact model [8] is extended to compute the terminal charges and intrinsic capacitances analytically using the Ward-Dutton scheme without using any additional fitting parameters or approximations. The proposed large signal model is verified using the experimentally calibrated TCAD simulations and is shown to be valid for a wide range of H and W, accurately capturing the QMC induced effects within the NsFET.

Simulation Set-up

The simulation setup in Global TCAD Solutions (GTS) framework [9], well calibrated with experimental data as shown in Fig.2, is used for validation of developed compact model. The effective oxide thickness (EOT), width (W) and substrate doping (N_A) of the calibrated device are 1 nm, 20 nm and 10^{16} cm^{-3} respectively. The calibrated TCAD deck is then used to simulate the NsFETs with gate length (L) of 500 nm and different H, W.

Model

A. Drain Current

The carrier transport in the NsFET is modeled using drift-diffusion (DD) formalism which offers several advantages including accuracy for short length (L) devices [10]. The drain current is expressed as follows,

$$I_{DS} = -\mu \mathrm{Q}_{inv} \frac{d\phi_c}{dz} + \mu \phi_t \frac{dQ_{inv}}{dz} \quad (1)$$

Here, μ is the transverse field dependent mobility, Q_{inv} is the inversion charge density, ϕ_c is the center potential as described in [8] and ϕ_t is the thermal potential. The Q_{inv} in above equation can be written as [8],

$$Q_{inv} = -2C_{inseff}\left(V_G - \phi'_{ms} - \phi_c\right) + qN_AWH \quad (2)$$

In (2), C_{inseff} is the effective insulator capacitance, V_G is the applied gate voltage. Since the drain current is continuous along the z direction, integrating (1) along z from source to drain, the final expression for $\mathrm{I_{DS}}$ can be expressed as,

$$I_{DS} = \frac{2\mu_{eff}C_{inseff}}{L}\left[\left(V_G - \phi'_{ms}\right)\left(\phi_c(V_D) - \phi_c(V_S)\right) - \left(\frac{\phi_c^2(V_D) - \phi_c^2(V_S)}{2}\right)\right] - \frac{\mu_{eff}}{L} qN_AWH\left(\phi_c(V_D) - \phi_c(V_S)\right) + \frac{\mu_{eff}\phi_t}{L}\left(Q_{inv}(V_D) - Q_{inv}(V_S)\right) \quad (3)$$

Here, μ_{eff} is the effective electron mobility which is derived by utilizing the method in [11]. It can be expressed as,

$$\mu_{eff} = \frac{\mu_o}{1 - \left(\frac{\alpha}{2\epsilon_S (W+H)}\right)\left(\overline{Q_B} + \eta\overline{Q_{inv}}\right)} \quad (4)$$

Here, μ_o is the low transverse field mobility, α is an empirical parameter, $\in_S$ is the permittivity of the semiconductor, $\overline{Q_B}$ and $\overline{Q_{inv}}$ is the average body and inversion charges respectively. In (3), I_{DS} is single unified equation which is expressed as an explicit function of the source terminal voltage (V_S) and drain terminal voltage (V_D) without using any additional approximations.

B. Terminal Charges

For NsFETs, there are three terminal charges associated with gate (Q_G), source (Q_S) and drain (Q_D). The Q_G can be evaluated as an integral of the total semiconductor charge density (Q_s),

$$Q_G = -\int_0^L Q_s\, dz \tag{5}$$

Using dz from I_{DS}, the final expression for Q_G can be calculated as

$$Q_G = \frac{\mu_{eff}}{I_{DS}}[Q_{G1}(V) - Q_{G2}(V) - Q_{G3}(V)]_{V_S}^{V_D} \tag{6}$$

Where,

$$Q_{G1} = \frac{Q_{inv}^3}{6C_{inseff}},\ Q_{G2} = \frac{qN_AWHQ_{inv}^2}{4C_{inseff}} \text{ and } Q_{G3} = \frac{\phi_t Q_s^2}{2I_{DS}}$$

To determine Q_D and Q_S, the widely accepted WD linear charge partition is used which guarantees charge conservation. The Q_D therefore can be evaluated as,

$$Q_D = \int_0^L \frac{z}{L} Q_{inv}\, dz \tag{7}$$

Using z and dz from (1), the final expression for Q_D can be written as,

$$Q_D = \frac{\mu_{eff}^2}{LI_{DS}^2}[Q_{D1}(V) + Q_{D2}(V) + Q_{D3}(V)]_{V_S}^{V_D} \tag{8}$$

Where,

$$Q_{D1} = \frac{1}{8C_{inseff}^2}\left[\frac{Q_{inv}^5}{5} - \frac{Q_{inv}^2(V_s)Q_{inv}^3}{3}\right]$$

$$Q_{D2} = \frac{-\phi_t}{4C_{inseff}}\left[\frac{3Q_{inv}^4}{4} - \frac{Q_{inv}^2(V_s)Q_{inv}^2}{2} - \frac{2Q_{inv}^3 Qinv(V_s)}{3}\right]$$

$$Q_{D3} = \phi_t^2\left[\frac{Q_{inv}^3}{3} - \frac{Q_{inv}(V_s)Q_{inv}^2}{2}\right]$$

The Q_S can be obtained by charge conservation and is calculated as,

$$Q_S = -(Q_G + Q_D + Q_B) \tag{9}$$

Note that, the developed intrinsic device charge model is analytical, free from any additional empirical parameters and possess scalability without compromising its computational efficiency. The intrinsic capacitance in NsFET are modeled as,

$$C_{i,j} = \delta_{i,j}\frac{\partial Q_i}{\partial V_j},\ \ \delta_{i,j} = \begin{cases} -1 & i \neq j \\ 1 & i = j \end{cases} \quad i,j = g,d,s \tag{10}$$

Here, $C_{i,j}$ represents the change in charges at terminal i in response to the varying voltage applied at terminal j, while keeping the voltage at other terminals constant. The intrinsic device capacitances are evaluated analytically, by utilizing the derived terminal charge expressions.

Results

Fig. 3a shows the model and simulated transfer characteristics for V_{DS} of 50 mV and 700 mV. As shown, the model agrees very well with the simulation data. Fig. 3b shows the output characteristics of the device for different V_{GS}. As shown, the model accurately captures the device output characteristics for a wide range of V_{GS}. To further demonstrate the model capability, Fig. 4 shows the transfer and the output characteristics of NsFETs with W = 20 nm but varying H. The good agreement of the model with the simulation data in Fig. 4 clearly shows that the proposed model can be seamlessly scaled from thick to thin NsFETs using purely physical and analytical expressions. Fig. 5 shows the gate (C_{gg}), source-gate (C_{sg}), and drain-gate (C_{dg}) terminal capacitances for V_{DS} of 10 mV. For this particular bias condition, the NsFET is always in the linear region, such that both C_{sg} and C_{dg} are equal to one half of C_{gg}, which is reflected in the model and simulation data. Fig. 6 plots the C_{gg}, C_{sg} and C_{dg} for two different V_{DS} (350 mV and 700 mV). These plots validates the model accuracy across different bias conditions (linear to the saturation region of operation). Fig. 7 shows the gate-drain (C_{gd}), drain (C_{dd}) and source-drain (C_{sd}) capacitances as a function of V_{DS} for different V_{GS}. As shown, the model is in excellent agreement with the simulation data. The model captures the behaviour of all the terminal capacitances of NsFET without using any additional fitting parameters. Fig. 8a shows the modeled and the simulated C_{gg} for NsFETs with W = 20 nm and varying H. The model accurately captures the shift in threshold voltage as well as the variation of C_{gg} with H. Fig. 8b plots the C_{gg} as a function of H for W = 20 nm at a fixed gate to source overdrive voltage (V_{OV}) of 400 mV. The plot shows that Cgg improves with reduction in the sheet thickness due to improved gate electrostatics. Fig. 9 plots C_{gd} as a function of V_{DS} for 20 nm wide NsFET with different H, at V_{GS} of 500 mV. As shown the model accurately captures the variation of Q_G with V_{DS} for different device dimensions. The figures 8 and 9 also show that the proposed equations efficiently model the NsFET behaviour across different device dimensions and bias conditions.

Conclusion

The focus of this work is to develop a core terminal charges and drain current model for NsFETs, with highest accuracy, at the same time capturing inherent physics with minimum empirical parameters. Following that, a physics-based scalable model was presented. The drain current model includes transverse electric field-dependent mobility and derived using drift-diffusion formalism. While the terminal charges model were derived using the WD charge partition scheme without using any additional empirical parameters. The developed model results were validated with calibrated TCAD simulation data and shown to be accurate across various bias conditions and device dimensions, thus ensuring scalability.

References

[1] M. A. Breton et al., JM^3, 21(2), pp. 021206, 2022. [2] N. Loubet et al., VLSI, pp. T230–1, 2017. [3] K.Uchida et al., IEDM, pp.29.4.1-29.4.4, 2001. [4] A. Dasgupta et al., IEEE TED, pp. 730-737, 2020. [5] G.I. Zebrev et al., IEEE TED, pp. 1574-1579, 2023. [6] O.Rozeau et al., IEDM, pp. 7.5.1-7.5.4, 2016. [7] A.Singh et al.,IEEE ICEE, pp. 1-5, 2022. [8] M. D. Ganeriwala et al., IEEE TED, pp. 380-387,20221–9, 2023. [9] "Global TCAD Solutions," https://www.globaltcad.com [10] A.S.Roy et al., IEEE TED, pp. 308-313, 2014. [11] Y. Tsividis and C. McAndrew, The MOS transistor. Oxford University Press, 2013.

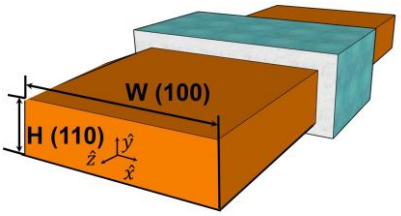


Fig. 1: Cross-sectional view of a NsFET confined in the x-y direction (z is the transport direction). W and H are width and thickness of the NsFET respectively. The vertical and horizontal sidewalls of channel has different crystallographic orientations.

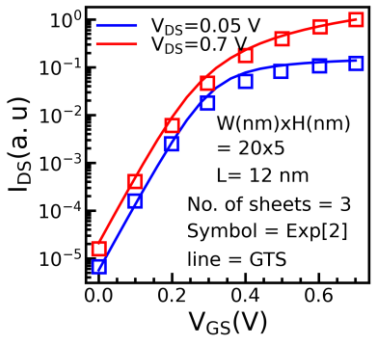


Fig. 2: Transfer characteristics of the NsFET with three sheets and W (nm) × H (nm) = 20 × 5, gate length = 12 nm for V_{DS} = 50 and 700 mV. Symbols represent the experimental data [2] and solid lines represent the TCAD data. The TCAD deck is well-calibrated against the experimental data.

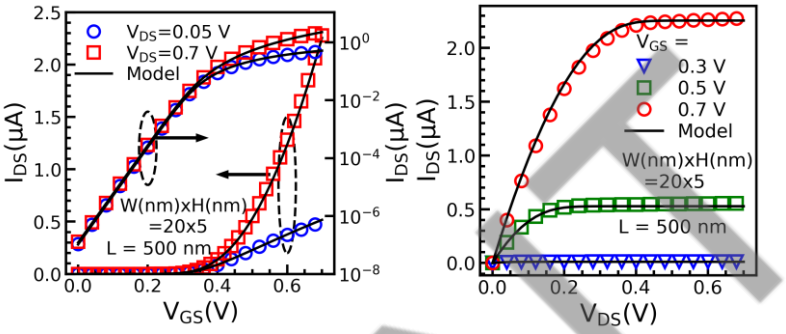


Fig. 3: Drain current (I_{DS}) for NsFETs with W (nm) × H (nm) = 20 × 5 and L = 500 nm as a function of, (a) V_{GS} for various values of V_{DS} and (b) V_{DS} for various values of V_{GS}. The model agrees very well with the simulation data.

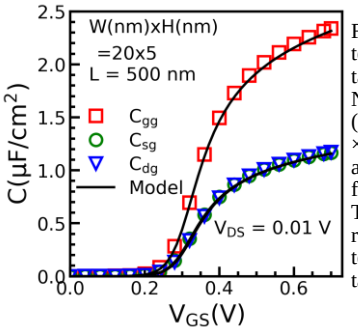


Fig. 5: Different terminal capacitances of the NsFET with W (nm) × H (nm) = 20 × 5 and L = 500 nm as a function of V_{GS} for V_{DS} = 10 mV. The model accurately predicts the terminal capacitances.

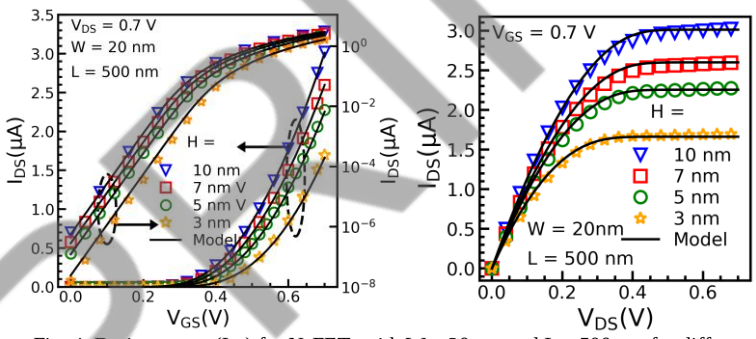


Fig. 4: Drain current (I_{DS}) for NsFETs with W = 20 nm and L = 500 nm for different H as a function of (a) V_{GS} for a fixed V_{DS} = 700 mV and (b) V_{DS} for a fixed V_{GS} = 700 mV. The model agrees very well with the simulation data.

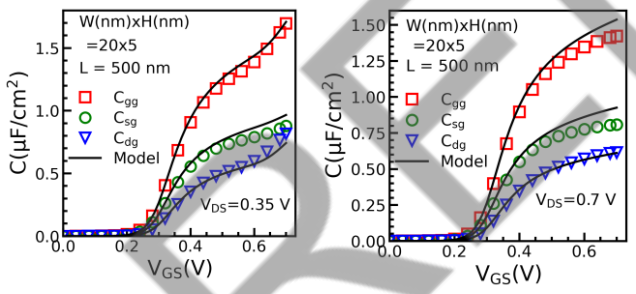


Fig. 6: Different terminal capacitances of the NsFET with W (nm) × H (nm) = 20 × 5 and L = 500 nm as a function of V_{GS} for, (a) V_{DS} = 350 mV and (b) V_{DS} = 700 mV. The model predicts the simulation data during transition from linear to saturation region.

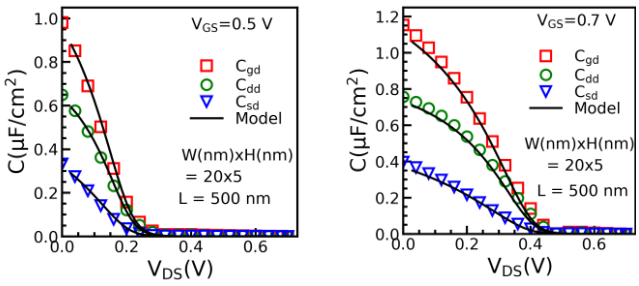
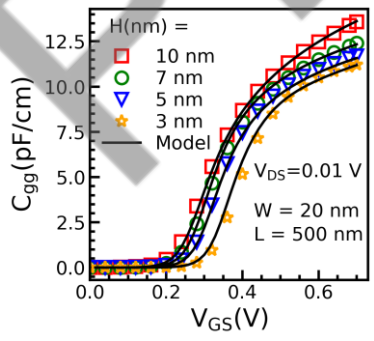


Fig. 7: Different terminal capacitances of the NsFET with W (nm) × H (nm) = 20 × 5 and L = 500 nm as a function of V_{DS} for, (a) V_{GS} = 500 mV (b) V_{GS} = 700 mV. The model agrees well with the simulation data.



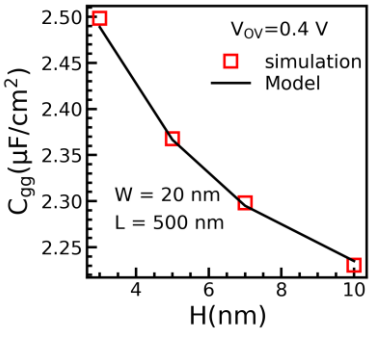


Fig. 8: C_{gg} for NsFETs with W = 20 nm and L = 500 nm (a) for different H as a function of V_{GS} and (b) as a function of H at V_{OV} = 400 mV. The model is able to capture the threshold voltage shift and the gate electrostatics change with reducing H.

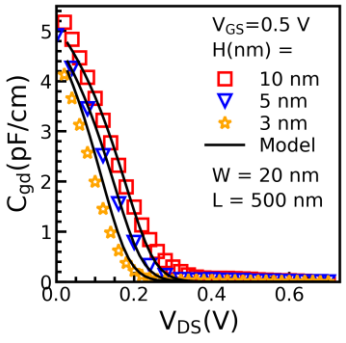


Fig. 9: C_{gd} for NsFETs with W = 20 nm and L = 500 nm as a function of V_{DS} for varying H at V_{GS} = 500 mV. The model captures the thickness variation very well.