UNIVERSIDAD
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OPTIMUM DESIGN AND NOVEL CONTROL TECHNIQUES FOR ISOLATED, RESONANT AND QUASI-RESONANT, DCDC CONVERTERS

DISEÑO OPTIMIZADO Y TÉCNICAS DE CONTROL PARA CONVERTIDORES DCDC RESONANTES Y CUASI-RESONANTES CON AISLAMIENTO

A thesis submitted to the University of Granada in partial
fulfillment of the requirements for the degree of

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in
Information and Communication Technologies

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Programa de Doctorado en Tecnologías de la Información y las Comunicaciones

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Thesis Acceptance

This student's Thesis, entitled "Optimum design and novel control techniques for isolated, resonant and quasi-resonant, DCDC converters" has been examined by the undersigned committee of examiners and has received full Approval for acceptance in partial fulfillment of the requirements for the degree of Doctor of Philosophy.

APPROVAL: _____ Chief Examiner

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Declaración / *Declaration*

El doctorando / *The doctoral candidate* [Manuel Escudero Rodríguez] y los directores de la tesis / *and the thesis supervisor/s*: [Diego Pedro Morales Santos, y Noel Rodríguez Santiago]

Garantizamos, al firmar esta tesis doctoral, que el trabajo ha sido realizado por el doctorando bajo la dirección de los directores de la tesis y hasta donde nuestro conocimiento alcanza, en la realización del trabajo, se han respetado los derechos de otros autores a ser citados, cuando se han utilizado sus resultados o publicaciones.

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SUMMARY

MOTIVATION AND OBJECTIVES

The power supplies or power converters are required in many applications to convert between the AC of the distribution grid to AC or DC at different voltage and current levels required by the electric loads. Each application may include different conversion steps and at different voltage levels. In every conversion step part of the energy is lost and dissipated in the form of unwanted heat. The conversion efficiency in every step is the result of dividing the utilized output power by the total input power in the converter. The total efficiency of the system is the result of multiplying the individual efficiencies of the stages, and will always be necessarily lower than the minimum of the individual efficiencies in the conversion chain.

Traditional linear power supplies have been extensively replaced by the more efficient and smaller Switched Mode Power Supplies (SMPS). SMPS makes use of semiconductor switches commutating at a relatively high frequency and reactive circuit elements (inductors and capacitors) to perform the power conversion. The semiconductor switches in SMPS alternate between their on state, where their voltage drop is minimal, and their off state, where they don't conduct current. However, during the switches turn-on transition and turn-off transition, there is certain overlap of voltage and current which causes switching losses.

For the currently available semiconductor power switching devices the resonant and quasi-resonant converters are the most attractive options for achieving high efficiency, high power density or a combination of both at a reasonable cost. The key advantage of the resonant and quasi-resonant converters is the reduction of the switching losses. The switching losses can be reduced achieving Zero Voltage Switching (ZVS) for the turn-on transition and Zero Current Switching (ZCS) for the turn-off transition.

Among the isolated, resonant and quasi-resonant DCDC converter topologies, the most common ones in medium-high power and high-voltage applications are the series-parallel resonant converter (LLC), the Phase Shifted Full Bridge (PSFB) and the Dual Active Bridge (DAB) due to their simplicity and high efficiencies. Among those topologies each one has its own advantages and disadvantages, which makes each of them best suited for different applications, power and voltage ranges.

This thesis is focused in the study of the LLC and the PSFB. Both of this topologies are very promising and well suited for any of the available power switch semiconductor technologies in the market, and more specifically for Si Super Junction (SJ) MOSFETs, which are the most mature devices and the most competitive in cost currently and in the foreseeable future. The general objective of this thesis is the optimization, improved reliability and functionality of the LLC and the PSFB converters maintaining as much as possible the simplicity of the standard circuit configuration.

Therefore, this thesis comprises the design and construction of several DCDC converters with similar specifications and similar magnetic structures to study the achievable performance of the two main topologies objective of this work: LLC and PSFB. More specifically, the fundamental research objectives of this thesis include:

- The development of very high-efficiency DCDC converters for server applications, including the design optimization of quasi-resonant converters experimentally demonstrated with a 1.4 kW PSFB converter from 400 V to 12 V.
- The development of very high-efficiency DCDC converters for telecommunitation applications, including the design optimization of quasi-resonant converters, experimentally demonstrated with a 3.3 kW PSFB converter from 380 V to 54.5 V, and the design optimization of resonant converters, experimentally demostrated with a 3.3 kW half-bridge LLC converter from 400 V to 52 V.
- The development of bidirectional DCDC converters for Electrical Energy Storage (EES) applications, including the bidirectional operation of traditionally considered non-bidirectional PSFB converters, experimentally demonstrated with a 3.3 kW bidirectional PSFB from 380 V to 54 V and from 50 V to 400 V.
- The integration of a very high-efficiency DCDC converter in a complete two-stage off-line Power Supply Unit (PSU) for server applications, experimentally demonstrated with a 3 kW totem-pole ACDC converter followed by a 3 kW half-bridge LLC DCDC converter from 400 V to 50 V.

Once the objectives have been outlined and after the previous brief theoretical background, in the following we summarize the several contributions of this thesis together with the most relevant results obtained and the conclusions that could be derived from them.

RESULTS AND CONCLUSIONS

It has been found that, although PSFB can achieve higher efficiencies than what is commonly expected thanks to the newest devices and the newly proposed control techniques, the LLC is still potentially superior and capable

of higher efficiencies with less components at a lesser cost. However, in bidirectional applications the large signal gain range of the PSFB makes it arguably superior to the LLC.

A 3300 W bidirectional PSFB DCDC converter from 380 V to 54 V has been designed and built achieving 98 % efficiency in forward or buck mode and 97% in reverse or boost mode. The achieved power density is in the range of 4.34 W/cm³ (71.19 W/in³), which is enabled by the use of Surface Mount Device (SMD) packages, the innovative stacked magnetic construction and the innovative cooling solution. This DCDC converter proves the feasibility of PSFB topology as a high efficiency topology at the level of fully resonant topologies when combined with the latest SJ MOSFET technologies. This DCDC converter proves as well that the PSFB topology can be used as a bidirectional DCDC stage without changes in the standard design or construction of a traditional and well known topology, but only through innovations in control techniques powered by digital control.

A 3300 W LLC DCDC converter from 400 V to 51.5 V has been designed and built achieving 98.1 % peak of efficiency. The achieved power density is in the range of 4 W/cm³ (66 W/in³). The optimized layout and an optimized driving circuitry achieves benchmark performance with minimum stress on the devices, enabled also by the innovative cooling concepts presented in this converter. This DCDC converter proves the feasibility of the half-bridge LLC as a high-efficiency topology for a 3300 W converter, at the level of full-bridge LLC or a dual stage LLC. This DCDC converter also proves that digital control is not only capable of controlling the LLC topology but the most effective way to overcome its difficulties and pitfalls. Moreover, the included protections mechanisms and control schemes further boost the reliability and performance of the converter achieving the best possible efficiency.

A 1400 W PSFB DCDC converter from 400 V to 12 V has been designed and built achieving 97 % peak efficiency. The achieved power density is in the range of 3.70 W/cm³ (60.78 W/in³) thanks to the full SMD solution. This DCDC converter proves that an analytical optimum design procedure can further boost the performance of the PSFB near fully resonant topologies for low voltage outputs.

Finally, a complete 3 kW two stage off-line PSU for server applications has been designed and built achieving 97.5 % peak efficiency. The overall outer dimensions of the PSU are 73.5 mm x 520 mm x 40 mm, which yields a power density in the range of 32 W/inch³ (1.95 W/cm³). Due to the outer dimension limits, a planar transformer with reduced height and volume was preferred for this design.

In the next paragraphs the described contributions correspond to the published works that constitute this thesis by compendium of publications.

In the first contribution, a novel modulation scheme is proposed for the bidirectional operation of the PSFB DCDC converter reducing the secondary side rectifiers overshoot without requiring additional circuitry or lossy snubbering techniques. The novel modulation scheme is experimentally demonstrated in a 3.3 kW PSFB DCDC converter with nominal 380 V input and nominal 54.5 V output.

M. Escudero, D. Meneses, N. Rodriguez and D. P. Morales, "Modulation Scheme for the Bidirectional Operation of the Phase-Shift Full-Bridge Power Converter," in *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 1377-1391, Feb. 2020.

In the second contribution, a novel modulation scheme is proposed for the reduction of the overshoot in the secondary side rectifiers in PSFB DCDC converters operating in Discontinuous Conduction Mode (DCM). Furthermore, other secondary side rectifiers overshoot causes are analyzed and solutions proposed for each of the scenarios. The novel modulation scheme and the design principles are experimentally demonstrated in a 3.3 kW PSFB DCDC converter with nominal 380 V input and nominal 54.5 V output.

M. Escudero, M. Kutschak, D. Meneses, D. P. Morales and N. Rodriguez, "Synchronous Rectifiers Drain Voltage Overshoot Reduction in PSFB Converters," in *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 7419-7433, July 2020.

In the third contribution, a detailed set of design criteria for PSFB DCDC converters is proposed. The design optimization procedure is experimentally demonstrated with the design of a new 1.4 kW PSFB DCDC converter further exceeding the efficiency and power density of a previous 1.4 kW PSFB DCDC converter with similar specifications, input voltage (400 V) and output voltage (12 V).

Escudero, M.; Kutschak, M.-A.; Meneses, D.; Rodriguez, N.; Morales, D.P. A Practical Approach to the Design of a Highly Efficient PSFB DC-DC Converter for Server Applications. *Energies* 2019, *12*, 3723.

In the fourth contribution the impact in the performance and the design of resonant ZVS converters of the nonlinear distribution of charge in the capacitances of semiconductor devices is analyzed. A Si SJ device is compared to a SiC device of equivalent $C_{oss(tr)}$, and to a GaN device of equivalent $C_{oss(er)}$, in single device topologies and half-bridge based topologies, in full ZVS and in partial or full hard-switching. A prototype of 3300 W resonant LLC DCDC converter, with nominal 400 V input to 52 V output, was designed and built to demonstrate the validity of the analysis.

M. Escudero, M. Kutschak, N. Fontana, N. Rodriguez and D. P. Morales, "Non-Linear Capacitance of Si SJ MOSFETs in Resonant Zero Voltage Switching Applications," in *IEEE Access*, vol. 8, pp. 116117-116131, 2020.

In the fifth contribution the design of a new complete power supply for server applications is discussed. The main constraints of the new solution are the very high peak efficiency, the long hold-up time and the maximum outer dimension. The PSU is comprised of a front-end ACDC bridgeless totem-pole PFC and a back-end DCDC half-bridge LLC. Due to the extended hold-up time, the PSU requires large intermediate energy storage and an extended gain range for the LLC. Due to the outer dimension limits, a planar transformer with reduced height and volume is preferred. Finally, the very high efficiency target requires a careful design based on the accurate modeling of the overall losses of the converter. The analysis is demonstrated experimentally with a 3 kW PSU achieving 97.47 % of efficiency at 230 VAC.

M. Escudero, M. -A. Kutschak, D. Meneses, N. Rodriguez and D. P. Morales, "High Efficiency, Narrow Output Range and Extended Hold-Up Time Power Supply with Planar and Integrated Magnetics for Server Applications," PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2021, pp. 1-8.

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LIST OF SYMBOLS

AC	Alternate Current
ACDC	Alternate Current to Direct Current
CCM	Continuous Conduction Mode
CLLC	Capacitor Inductor Inductor Capacitor
CrCM	Critical Conduction Mode
DAB	Dual Active Bridge
DC	Direct Current
DCDC	Direct Current to Direct Current
DCM	Discontinuous Conduction Mode
DPS	Double Phase Shift
EES	Electrical Energy Storage
EPS	Extended Phase Shift
EMI	Electromagnetic Interference
FHA	First Harmonic Approximation
FoM	Figure of Merit
Fres	Resonant Frequency
Fsw	Switching Frequency
GUI	Graphical User Interface
HB	Half Bridge
HEMT	High Electron Mobility Transistor
HS	High Side
HV	High Voltage
IGBT	Isolated Gate Bipolar Transistor
LCC	Inductor Capacitor Capacitor
LLC	Inductor Inductor Capacitor
LS	Low Side
LV	Low Voltage
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
OCP	Over Current Protection
OVP	Over Voltage Protection
PFC	Power Factor Correction
PRC	Parallel Resonant Converter
PSFB	Phase Shift Full Bridge
PWM	Pulse Width Modulated
Qoss	Charge stored in the output capacitance
Qrr	Reverse recovery charges
RCD	Resistor Capacitor Diode
Rds,on	On state Drain to Source Resistance
Si	Silicon
SiC	Silicon Carbide
SJ	Super Junction
SMD	Surface Mount Devices
SMPS	Switched Mode Power Supply
SPS	Single Phase Shift
SR	Synchronous Rectifier
SRC	Series Resonant Converter
THD	Total Harmonic Distortion
Tj	Junction Temperature
TPS	Triple Phase Shift
UART	Universal Asynchronous Receiver Transmitter
UPS	Uninterruptible Power Supply
USB	Universal Serial Bus
UVP	Under Voltage Protection
UVLO	Under Voltage Lockout
WBG	Wide Band Gap
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

CHAPTER 1. INTRODUCTION

1. BACKGROUND

Electric energy is commonly distributed through a high voltage Alternating Current (AC) grid, which diminishes the conduction losses caused by the long transmission lines from the energy sources to the local area step down transformers. The step down transformers convert the high voltage AC into medium voltage AC. The specifications of the medium voltage AC depends on the region, ranging from single phase with nominal 110 V_{AC} up to 240 V_{AC}, or three phase with nominal 110 V_{AC} up to 480 V_{AC} (line to line), at 50 Hz or 60 Hz. These values are subjected to certain tolerances and may transitorily deviate from its nominal values. Moreover, surge events caused by other equipment, lighting discharge or temporarily loss of the power should be considered in the design of the downstream power conversion stages.

Some electric loads can be supplied directly from the medium voltage V_{AC}, such is the case of light bulbs or some motors. Other loads require Direct Current (DC) at lower voltages. The power supplies or power converters are required in those applications to convert between the AC of the distribution grid and the DC at the different voltage and current levels required by the loads. Moreover, they can provide additional features like isolation, voltage regulation, current regulation, power factor correction, short-circuit protection… required for reliability and safety of the user, the equipment itself and other surrounding systems, and the distribution network.

Traditional linear power supplies have been extensively replaced by the more efficient and smaller Switched Mode Power Supplies (SMPS). Pioneer Magnetics started building SMPS in 1958. And General Electric published an early design for a switching power supply in 1959. Through the 1960s the aerospace industry provided the main driving force behind the development of SMPS. As the cost came down SMPS were designed into public commercial products.

Figure 1 shows a simplified structure of a common power distribution in a computing center. Other applications may include different conversion steps and at different voltage levels. In every step part of the energy is lost and dissipated in the form of unwanted heat. The efficiency of a conversion step is the result of dividing the usable output power by the input power in the converter. The total efficiency of the system is the result of multiplying the individual efficiencies of the stages, and will always be necessarily lower than the minimum of the individual efficiencies in the conversion chain.

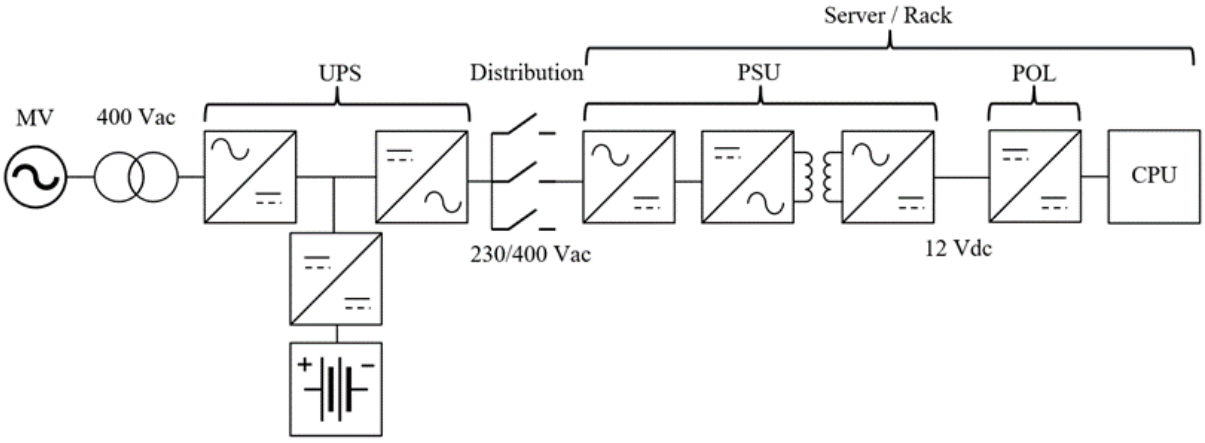

Figure 1. Example of the power distribution architecture in a common computing center.

The growing power consumption has become a cause for environmental concern, resulting in initiatives and regulations to make power supplies more efficient. The government's Energy Star [1] and the industry-led 80 Plus certifications [2] pushed manufacturers to produce less wasteful power supplies. On the other hand, the efficiency of the converters has a direct impact on the cost of maintenance of the systems, due to the cost of the supplementay supplied electrical power and the additionally required cooling facilities.

There are two possible approaches or solutions towards the decrease of the overall conversion losses:

- Increasing the efficiency of the individual conversion stages, thanks to the improvements in semiconductor technologies, in magnetics, the introduction of new converter topologies or control techniques [3]. But also including changes in the architecture of the power distribution, e.g. increasing the bus voltage in server applications from 12 V_{DC} to 50 V_{DC} (Figure 1 and Figure 2), which reduces the conduction losses for the increasingly high currents at a rack level [4].
- Reducing the number of conversion stages, e.g. in Figure 2 the intermediate steps between the Uninterruptible Power Supply (UPS) battery and the DCDC stage of the Power Supply Unit (PSU) has been eliminated replacing the local V_{AC} distribution by a 400 V V_{DC}. Although this example may bring efficiency benefits, it is still not a common solution due to the safety and reliability concerns. Other architectures simply relocate the

UPS stage further downstream, at the PSU level, or include a battery backup connected to the Low Voltage (LV) DC bus within the rack (12 V V_{DC} or most commonly 50 V V_{DC}) .

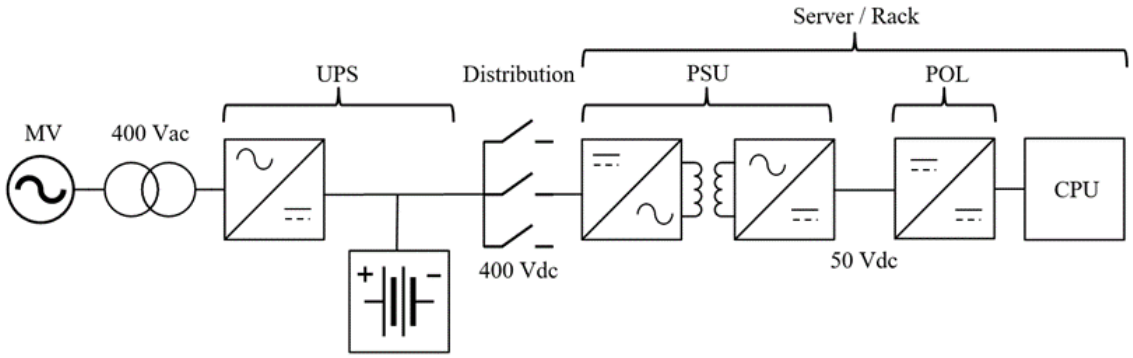

Figure 2. Example of current trends in the computing center power distribution architecture.

The PSU in Figure 1 can be connected to the AC distribution network and provides a tightly regulated DC output. Power supplies connected to the AC distribution network are commonly known as off-line power supplies. In low power applications, under 75W, there are no requirements in terms of power factor and Total Harmonic Distortion (THD) for off-line power supplies. In those applications are common single stage converters. However, in medium and high power applications a power supply generally comprises at least two stages: a first stage providing Power Factor Correction (PFC) and THD and a second stage providing isolation and a tightly regulated voltage or current output (Figure 3).

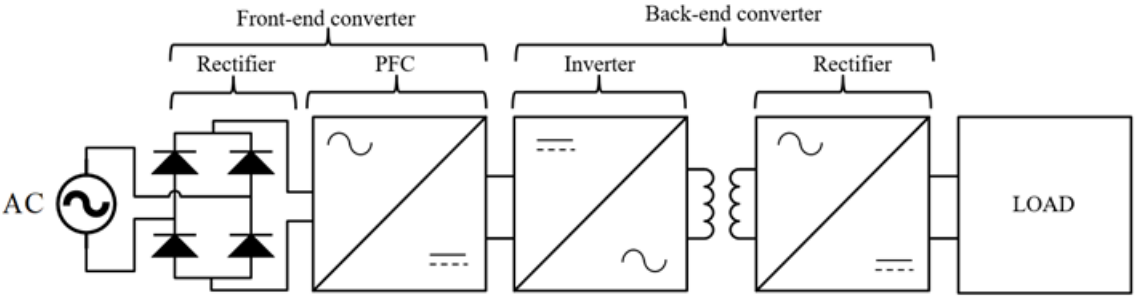

Figure 3. Main blocks of a high power off-line PSU.

1.1. SWITCHED MODE POWER SUPPLIES (SMPS)

SMPS makes use of semiconductor switches commutating at a relatively high frequency and reactive circuit elements (inductors and capacitors) to perform the power conversion. The semiconductor switches alternate between their on state, where their voltage drop is minimal, and their off state, where they don't conduct current. During the transition from on to off (Figure 4 and Figure 6) and from off to on (Figure 5 and Figure 5), the semiconductor switch enters its linear mode where voltage and current overlap and cause additional losses [5]-[8].

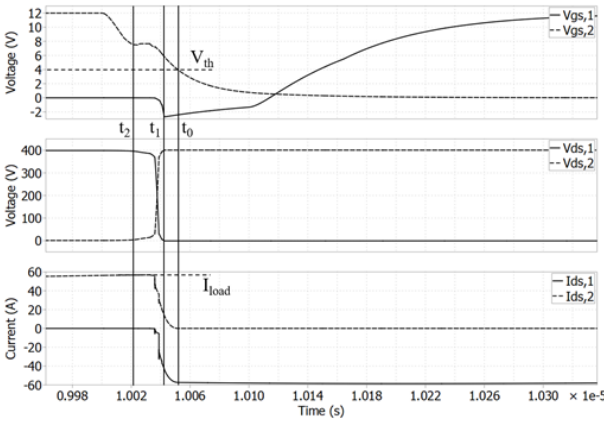

Figure 4. Power MOSFET hard-switched turn-off transition and Zero Voltage Switched (ZVS) turn-on transition.

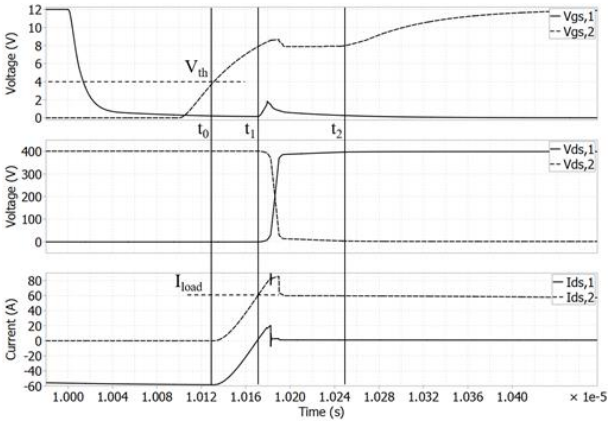

Figure 5. Power MOSFET hard-switched turn-on transition and Zero Voltage Switched (ZVS) turn-off transition.

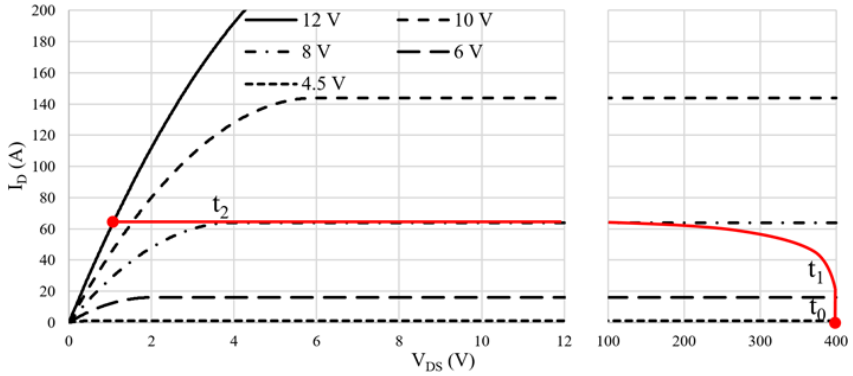

Figure 6. Example trajectory of the voltage and current in a power MOSFET during a hard-switched turn-off transition.

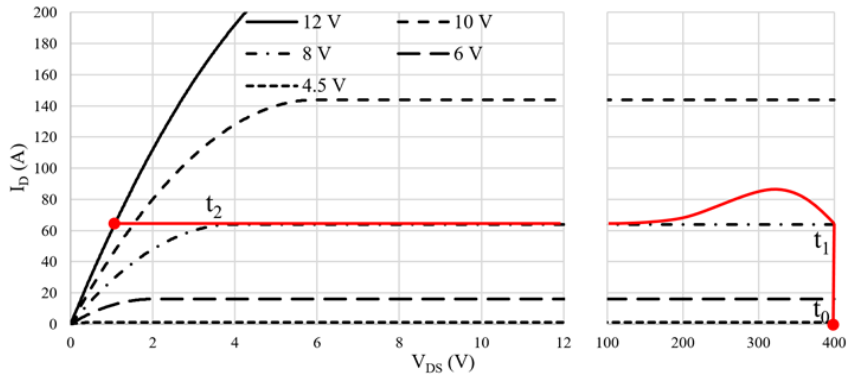

Figure 5. Example trajectory of the voltage and current in a power MOSFET during a hard-switched turn-on transition

In order to further reduce losses in SMPS it is possible to make use of reactive circuit elements (inductors and capacitors) together with the parasitic resonant elements of the semiconductor switch itself to achieve lossless transitions between the on and off states [9]. This operation paradigm includes what are commonly known as resonant and quasi-resonant converters. There are two main alternatives for achieving lossless transitions, switching at a Zero Voltage (ZVS) or at a Zero Current (ZCS), being the most convenient ZVS turn-on and ZCS turn-off (Figure 6).

Nevertheless, it has been reported recently that even when there is no overlap of current and voltages in a power switching device during the turn-on and turn-off transitions there could be still losses related to a hysteresis in the charge and discharge of the parasitic output capacitance. The phenomena can be interpreted as a transitory increase of an equivalent resistance in series with the output capacitance of the device during its charge and discharge. The phenomena is mostly present in Super-Junction (SJ) MOSFETs and GaN High Electron Mobility Transistors (HEMTs). However, the root cause of the loss is different among the technologies and difficult to predict. Many recent works in the literature have proposed techniques for the accurate measurement and estimation of the related soft-switching hysteretic loss [10]-[11].

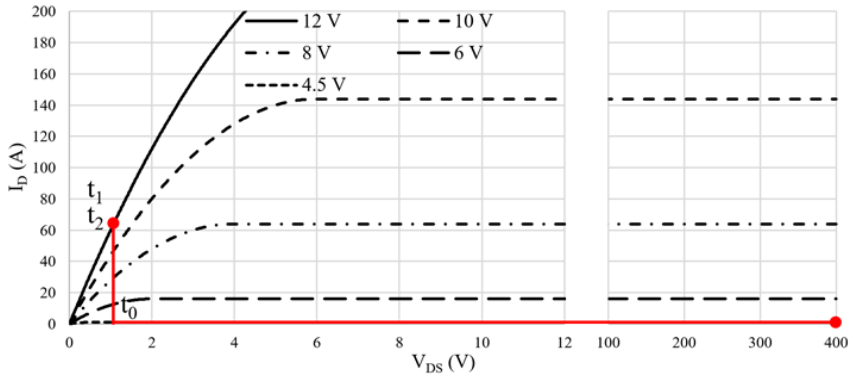

Figure 6. Example trajectory of the voltage and current in a power MOSFET during a ZVS turn-on or a ZCS turn-off transition.

1.2. POWER SEMICONDUCTOR SWITCHES

The switching power supply has been known to electrical engineers since the 1930s, but the technique was of limited use in the vacuum-tube era. It took about 30 years for semiconductor devices to become robust enough to handle direct switching of mains voltages at useful power levels. In low and medium power applications the most common power semiconductor switches nowadays are Silicon (Si) MOSFETs and IGBTs. The main advantages

of these two technologies are their high performance and low cost. IGBTs are better tailored for relatively low switching frequencies because of their comparatively high switching losses. Moreover, the IGBT is a bipolar type structure and cannot conduct bidirectional current, requiring of an additional anti-parallel diode in many converter topologies.

The Si power MOSFETs technology had reached near the theoretical limits of the material itself near the end of the 1990s. Other alternative semiconductor materials have been under study due to their promising intrinsic properties which may allow to manufacture devices with a Figure of Merit (FoM) several orders of magnitude better than Si devices. In [12]-[14] Baliga has shown that the specific on-state resistance of the power MOSFET ($R_{sp,standard}$) increases with the square of the breakdown voltage (V_B), and is inversely proportional to the cube of the critical field. The specific on-state resistance can be expressed as (1) where μ_n, ε_S, and E_C are the electron mobility, the permittivity of a semiconductor material, and the critical electrical field, respectively. However, Si devices continue to be attractive today due to its cost, availability of the raw material and maturity of the technology. Figure 7 represents the theoretical specific on-state resistance for Si, 4H-SiC and GaN calculated with (1).

$$R_{sp,standard} = \frac{4V_B^2}{\mu_n \varepsilon_S E_C^3} (\Omega \cdot cm^2) \quad (1)$$

At the end of the 1990s a new concept of construction for the Si MOSFETs, the SJ MOSFET, pushed the boundaries of Si beyond its theoretical limits. In this new construction the doping levels in the channel can be increased (effectively lower $R_{ds,on}$) without compromising the blocking voltage capability with the principle of charge compensation. This technology is still developing today, although already near its limits. An early theoretical study of the SJ concept, widely adopted today, was introduced by Fujihira [15] with the specific on-state resistance given by (2) where d is the cell pitch of a SJ device. However, the cell pitch is not only a technology limitation, other parasitic effects not considered in this simplified model limit the achievable minimum $R_{ds,on}$ [13]. Figure 8 represents the theoretical specific on-state resistance for Si SJ and 4H-SiC SJ calculated with (2), including contemporary examples of commercially available devices.

$$R_{sp,SJ} = \frac{4V_B}{\mu_n \varepsilon_S E_C^2} d(\Omega \cdot cm^2) \quad (2)$$

Many power device FoMs have been reported in the literature characterizing different aspects such as conduction loss, switching loss, and thermal and semiconductor materials [16]. The Baliga's FoM ($R_{sp,standard}$) [17] is well suited for low-frequency systems. The most widespread high-frequency FoM considers the specific on-resistance and the input capacitance (by Baliga [12]) and the specific on-resistance and the output capacitance (proposed by Kim [18]). The high-frequency FoM is better suited to assess the balance between conduction and switching losses of the different semiconductor technologies in modern power converters.

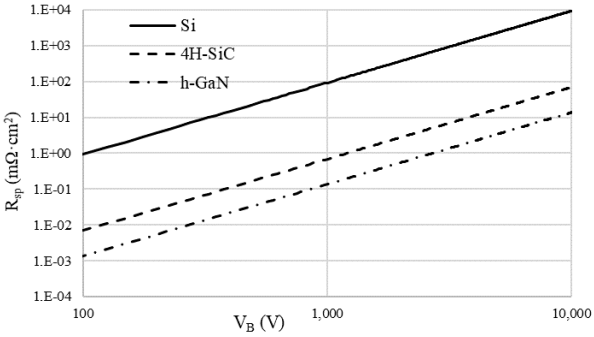

Figure 7. Theoretical specific on-state resistance limit for different semiconductor materials.

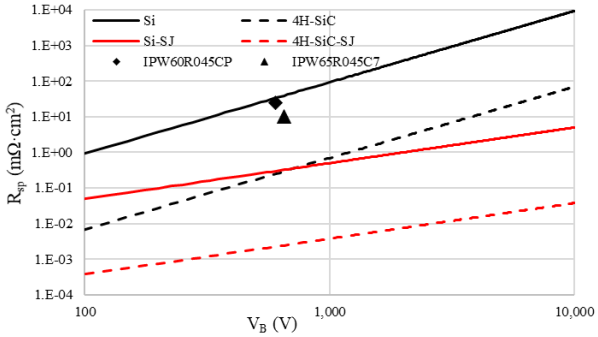

Figure 8. Theoretical specific on-state resistance limit for SJ MOSFETs of different semiconductor materials, including two examples of commercially available Si SJ MOSFETs.

2. OBJECTIVES

The most commonly used resonant and quasi-resonant converter topologies have been introduced in the early years of the SMPS development. Some of their working principles have taken years to be fully understood, and still today new publications can be frequently found describing new inventions, discoveries or aspects previously unnoticed. On the other hand, the characteristics of the most modern device technologies heavily influences the optimum design methodology for these converters, the performances that can be achieved, and new possible configurations of the circuits. Commonly known converter topologies should be continuously revisited and their capabilities re-evaluated on behalf of those advances. Moreover, upcoming new application requirements like bidirectionality may make traditional topologies, with the appropriate control schemes, advantageous against currently widespread alternatives.

The core of this thesis is the study of resonant and quasi-resonant converters with the aim of increasing their efficiency, reliability and functionality taking advantage of the new developments in semiconductor technologies, novel magnetics construction and novel control techniques. The fundamental research objectives of this thesis are:

- The development of very high-efficiency DCDC converters for server and telecommunication applications, including the design optimization of resonant and quasi-resonant converters.
- The development of bidirectional DCDC converters for Electrical Energy Storage (EES) applications, including the bidirectional operation of traditionally considered non-bidirectional converters.

The following section outlines the overall thesis structure, as well as present a list of the significant contributions and a list of publications made during the course of the project.

3. STRUCTURE OF THE THESIS

It must be pointed out that this is a thesis by compendium of publications, which comprises published papers resulting from the research done during the doctoral period.

This thesis is organized as follows:

- Chapter 1 (this chapter) introduces the research context of this thesis, and the fundamental research questions that this work addresses. It also provides an outline of the thesis structure.
- Chapter 2 presents a review of the current state of the art in the area of resonant and quasi-resonant, isolated, uni-directional and bidirectional DCDC converters, in terms of their topology, modulation schemes and design.
- **Section I** comprises Chapter 3 to Chapter 6, and provides a description of the DCDC converter systems that have been simulated, designed and built to explore and verify the concepts presented in this thesis. Chapter 3 introduces a 1400 W PSFB for server applications. Chapter 4 introduces a bidirectional 3300 W PSFB for telecom or EES applications. Chapter 5 presents a 3300 W half-bridge LLC for telecom applications. Chapter 6 presents a 3000 W half-bridge LLC integrated in a complete two-stage off-line PSU for server applications.
- **Section II** comprises Chapter 7 to Chapter 11, and provides the five published papers presented to constitute the thesis by compendium of publications.
- **Section III** comprises Chapter 12 to chapter 16, and encompasses the research outcomes that are not part of the compendium or have not yet been published. Chapter 12 introduces a frequency modulation scheme for the input voltage range extension in PSFB converters. Chapter 13 introduces a modulation scheme for the resetting of the circulating currents in PSFB. Chapter 14 introduces a switched capacitor circuit for the driving of power semiconductors. Chapter 15 presents a modulation scheme for the cold start-up of the isolated boost converter (bidirectional PSFB). Chapter 16 presents a modulation scheme for the gain range extension and bidirectional operation of LLC converters.
- Finally, **Section IV**, comprising Chapter 17, collects the final conclusions drawn from the obtained results, as well as guidance and possible lines of work for future research.

4. IDENTIFICATION OF ORIGINAL CONTRIBUTIONS

This thesis presents several key contributions to the field of power electronic converters, which are listed in this section.

The first contribution is presented in Chapter 7. In this published paper a novel modulation scheme is proposed for the bidirectional operation of the PSFB DCDC converter reducing the secondary side rectifiers overshoot without requiring additional circuitry or lossy snubbering techniques. The novel modulation scheme is experimentally demonstrated in a 3.3 kW PSFB DCDC converter with nominal 380 V input and nominal 54.5 V output. Moreover, the proposed modulation scheme in this first contribution is pending patent, which application has also been published [19].

M. Escudero, D. Meneses, N. Rodriguez and D. P. Morales, "Modulation Scheme for the Bidirectional Operation of the Phase-Shift Full-Bridge Power Converter," in *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 1377-1391, Feb. 2020.

The second contribution is presented in Chapter 8. In this published paper a novel modulation scheme is proposed for the reduction of the overshoot in the secondary side rectifiers in PSFB DCDC converters operating in DCM. Furthermore, other secondary side rectifiers overshoot causes are analyzed and solutions proposed for each of the scenarios. The novel modulation scheme and the design principles are experimentally demonstrated in a 3.3 kW PSFB DCDC converter with nominal 380 V input and nominal 54.5 V output. Moreover, the proposed modulation scheme in the second contribution has been registered and granted a patent, which has also been published [20].

M. Escudero, M. Kutschak, D. Meneses, D. P. Morales and N. Rodriguez, "Synchronous Rectifiers Drain Voltage Overshoot Reduction in PSFB Converters," in *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 7419-7433, July 2020.

The third contribution is presented in Chapter 9. In this published paper a detailed set of design criteria for PSFB DCDC converters is proposed. The design optimization procedure is experimentally demonstrated with the design of a new 1.4 kW PSFB DCDC converter further exceeding the efficiency and power density of a previous 1.4 kW PSFB DCDC converter with similar specifications, input voltage (400 V) and output voltage (12 V).

Escudero, M.; Kutschak, M.-A.; Meneses, D.; Rodriguez, N.; Morales, D.P. A Practical Approach to the Design of a Highly Efficient PSFB DC-DC Converter for Server Applications. *Energies* 2019, *12*, 3723.

The fourth contribution is presented in Chapter 10. In this published paper, the impact in the performance and the design of resonant ZVS converters of the non-linear distribution of charge in the output capacitance of semiconductor devices is analyzed. A Si SJ device is compared to a SiC device of equivalent $C_{oss(tr)}$, and to a GaN device of equivalent $C_{oss(er)}$, in single device topologies and half-bridge based topologies, in full ZVS and in partial or full hard-switching. A prototype of 3300 W resonant LLC DCDC converter, with nominal 400 V input to 52 V output, was designed and built to demonstrate the validity of the analysis.

M. Escudero, M. Kutschak, N. Fontana, N. Rodriguez and D. P. Morales, "Non-Linear Capacitance of Si SJ MOSFETs in Resonant Zero Voltage Switching Applications," in *IEEE Access*, vol. 8, pp. 116117-116131, 2020.

The fifth contribution is presented in Chapter 11. In this published paper the design of a new complete power supply for server applications is discussed. The main constraints of the new solution are the very high peak efficiency, the long hold-up time and the maximum outer dimension. The PSU is comprised of a front-end ACDC bridgeless totem-pole PFC and a back-end DCDC half-bridge LLC. Due to the extended hold-up time, the PSU requires large intermediate energy storage and an extended gain range for the LLC. Due to the outer dimension limits, a planar transformer with reduced height and volume is preferred. Finally, the very high efficiency target requires a careful design based on the accurate modeling of the overall losses of the converter. The analysis is demonstrated experimentally with a 3 kW PSU achieving 97.47 % of efficiency at 230 VAC.

M. Escudero, M. -A. Kutschak, D. Meneses, N. Rodriguez and D. P. Morales, "High Efficiency, Narrow Output Range and Extended Hold-Up Time Power Supply with Planar and Integrated Magnetics for Server Applications," *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2021, pp. 1-8.

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CHAPTER 2. STATE OF THE ART

1. INTRODUCTION

The back-end isolated DCDC converter in off-line power supplies, introduced in Chapter 1, generally comprises a High Voltage (HV) primary side inverter feeding the primary side of the main transformer, a secondary side LV rectification stage connected to the secondary side of the main transformer and a smoothing filter at the output of the rectification stage providing low ripple DC voltage.

Isolation is a safety requirement in off-line power supplies. The safety isolation between the HV input and the LV output ensures that the user will not be exposed to dangerous currents or voltages touching any unprotected conductive part of the converter or the equipment in general. The most common technique for achieving safety isolation between the input and the output of the converter is through transformers, which transfer power through the magnetic field. Moreover, the transformer provides an efficient way of stepping up or down the voltages in relatively large ratios. Although other alternative methods for the transmission of power through the isolation barrier uses capacitors, they are mainly used in very low power applications.

The primary side HV inverter comprises one switch or several of them stacked in pairs conforming a building block so-called half-bridge. Single device converters are common in low power applications (up to 100 W), half-bridge converters are commonly used in medium power (up to 1kW) whereas full-bridge converters can reach efficiently much higher powers (6-7 kW).

The secondary side rectification stage comprises passive diodes or active semiconductor switches, commonly known as synchronous rectifiers (SRs) because they emulate ideal diodes. The secondary side rectification stage can adopt several configurations depending on the converter's output voltage and current (Figure 1): center tapped is well suited for LV and high-current outputs, full bridge is the most effective for HV and low-current outputs, current doubler is the most convenient for very high output currents, whereas voltage doubler is a good alternative for high output voltages [1]-[2]. However, the configuration of the rectification stage does not influence significantly the working principles of the converters.

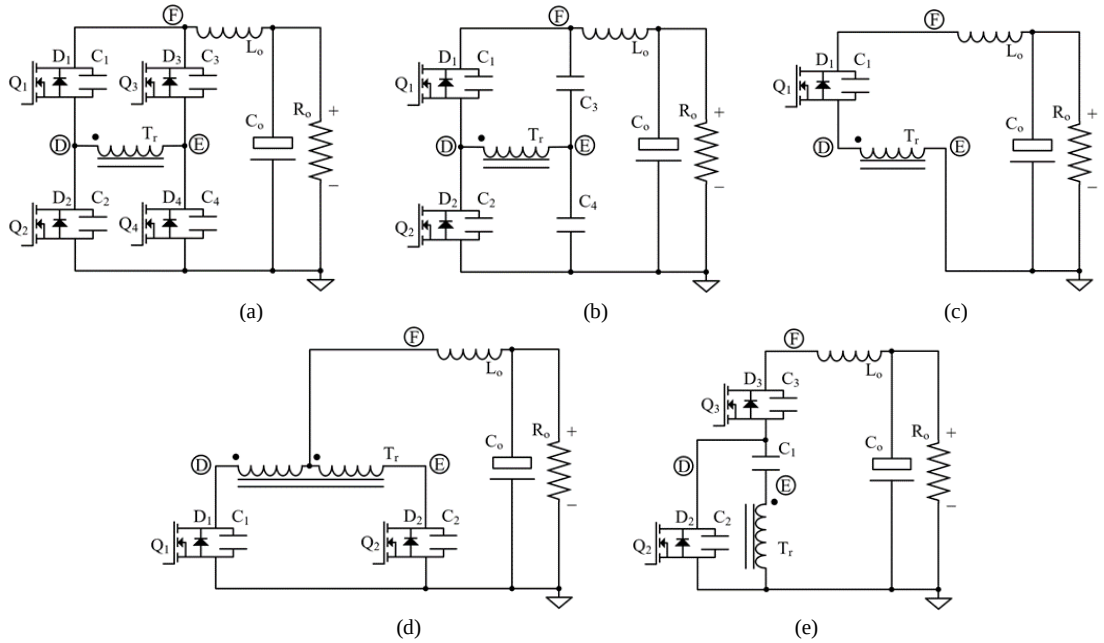

Figure 1. Various possible rectifier configurations. (a) Full-bridge rectifier. (b) Bridge voltage doubler. (c) Half-wave rectifier. (d) Center-tapped rectifier. (e) Trapezoid voltage-doubler.

The output filter comprises a set of capacitors and, in most cases, one or more inductors. The main objective of the output filter is reducing de voltage and current ripple at the output of the converter. However, in some converter topologies it is taken advantage of for achieving ZVS in the primary side devices or clamping the secondary side rectifiers drain voltage overshoot. There is as well, generally, an input filter to the converter, which provides most of the energy during the hold-up time, while simultaneously serving as the output filter of the front-end PFC stage of the complete PSU.

Figure 2 makes a summary of one possible classification of isolated two-port DCDC converters based on the number of devices and the configuration of their output and input filters. Notice that the classification is not necessarily exhaustive nor complete, but includes the most commonly used converters objective of this thesis.

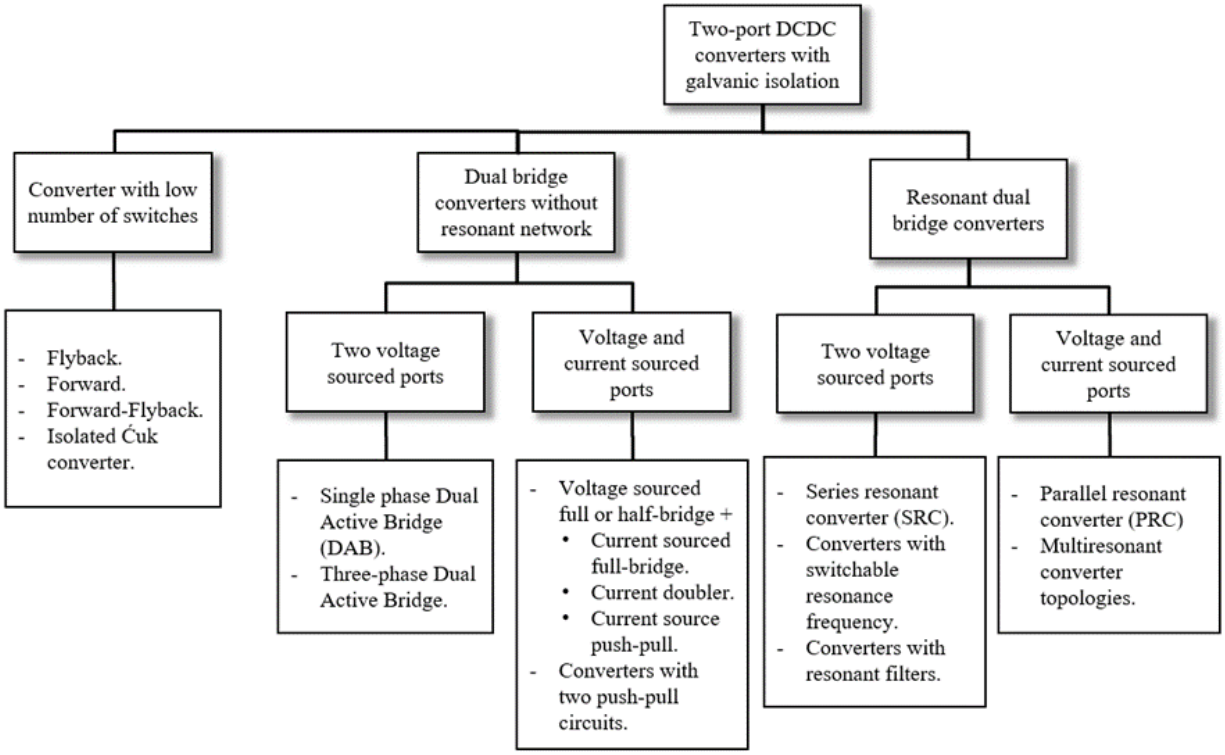

Figure 2. A possible classification of DCDC converters with galvanic isolation. Adapted from [3].

1.1. RESONANT CONVERTERS

The commonly known as resonant converters take advantage of the natural resonance between inductors and capacitors to achieve ZVS, ZCS or a combination of both. The resonant circuit or resonant tank can be comprised of two or more elements in series or in parallel (Figure 3 and Figure 4) [4]. Resonant converters large signal gain depends on the configuration of the resonant tank and can be adjusted varying the switching frequency of the primary switches. The exact analysis of resonant converters leads to complex models that cannot be easily used in the converter design procedures. In [5], R. Steigerwald has described a simplified method applicable to any resonant topology, based on the assumption that input to output power transfer is essentially due to the fundamental harmonic components of currents and voltages [6].

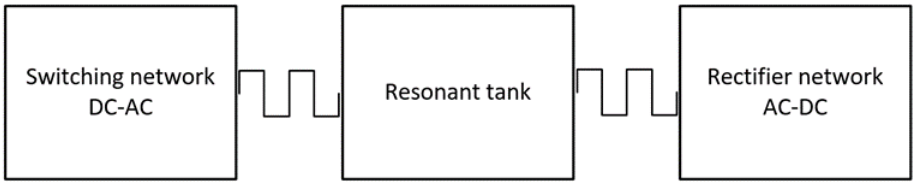

Figure 3. Conventional resonant converter structure. Adapted from [4].

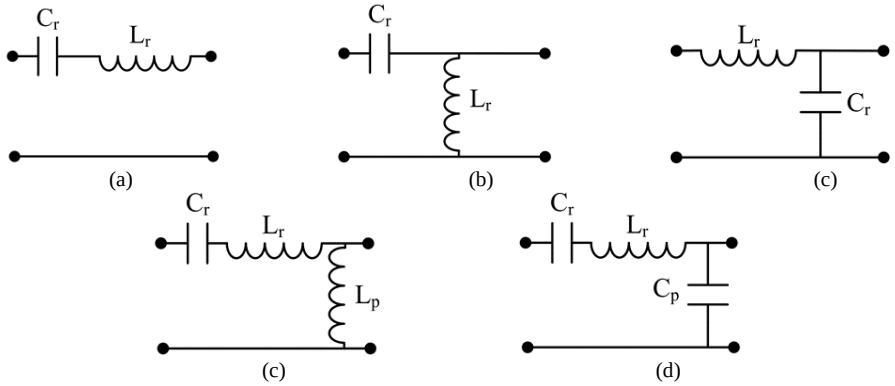

Figure 4. Basic two and three element resonant topologies. (a) Series Resonant Converter (SRC). (b) Parallel Resonant Converter (PRC). (c) LLC. (d) LCC. Adapted from [4].

The LLC is a resonant converter in which the resonant tank is comprised of a series inductor, a series capacitor and another inductor in parallel to the load, therefore its name, LLC (Figure 5). This converter has been extensively studied in the literature [7]-[16]. Although its design and control is complex, thanks to its merits and the widespread availability of commercial off-the-self controllers, this topology has become very popular. LLC converters can be very efficient and relatively cheap due to their low component count. Moreover, the two inductors part of the resonant tank can be realized as a part of the main transformer: the series inductor realized by the leakage and the parallel inductor realized by the magnetizing inductance.

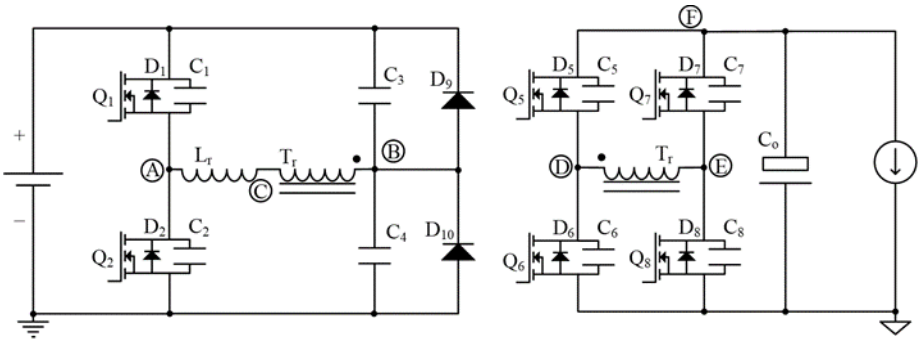

Figure 5. LLC converter simplified circuit.

One of the most attractive features of the LLC is that it can operate as a step-up or as a step-down converter. The normalized unity gain is achieved switching at the frequency of the resonance between the series inductor and the series capacitor (e.g. 75 kHz in Figure 6). In this operation point the gain of the converter is nearly independent of the load. Moreover, the maximum efficiency of the converter is usually achieved near this operation point. Therefore, an LLC can be designed to operate at its optimum point in nominal conditions and still be capable of maintaining regulation during hold-up time.

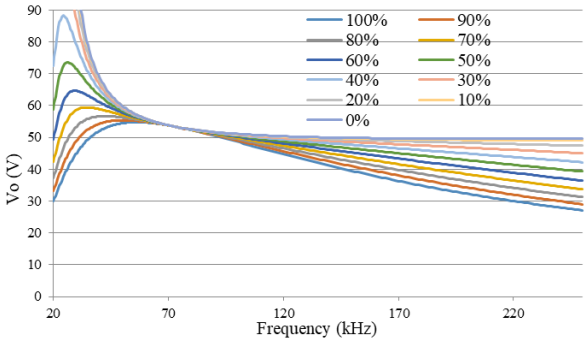

Figure 6. Large signal gain of a half-bridge LLC converter. The converter's input voltage is 400 V and the transformer turn ratio is 15:4. Therefore, its nominal unity gain corresponds to the 53.3 V output. The series in the graph are a function of the percentaje of the nominal load of the converter.

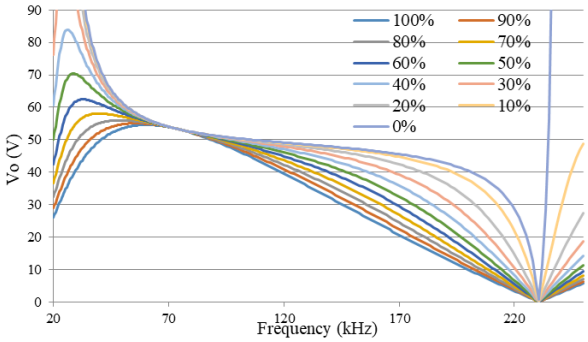

Figure 7. Large signal gain of an LCLC converter. The series in the graph are a function of the percentaje of the nominal load of the converter.

One of the main disadvantages of the LLC converter is that at light loads the gain curve in relation to the switching frequency can become flat or even non-monotonic due to the circuit parasitics [8]. There are several solutions analyzed in the literature to this problem [9]. The most common approach is the operation of the converter in the so-called burst mode. Alternatively, different configurations of the resonant tank can provide better controllability of the converter's gain at the expense of the additional circuit complexity and slightly lower efficiencies (Figure 7).

The LLC as a bidirectional converter, when operated in the reverse direction, becomes a Series Resonant Converter (SRC) (Figure 4 (a)). The SRC is a step-down converter with a maximum normalized unity gain (Figure 8) [10]. This limits the applicability of the LLC in bidirectional applications [3]. In [11] an intermediate non-isolated boost converter is introduced between the front-end ACDC and the back-end SRC to achieve the required gain in the reverse operation mode. In [12] a hybrid between the LLC and the DAB modulation is proposed to increase the gain of the SRC in the reverse mode of operation. A more common solution is the realization of a symmetric resonant tank adding an additional capacitor and an additional series inductor on both sides of the transformer, the resulting converter is therefore known as CLLC or, frequently in the literature, as bidirectional LLC [13] (Figure 9). The CLLC has the gain characteristics of an LLC while operating in both forward and reverse modes. The main drawbacks of the CLLC are the increased design and control complexity [14]-[15] and, in low voltage and high current applications, a capacitor in series in a high current path (additional losses and volume). In [16]

the two series inductors are integrated within the main transformer to achieve a higher power density and arguably a lower cost.

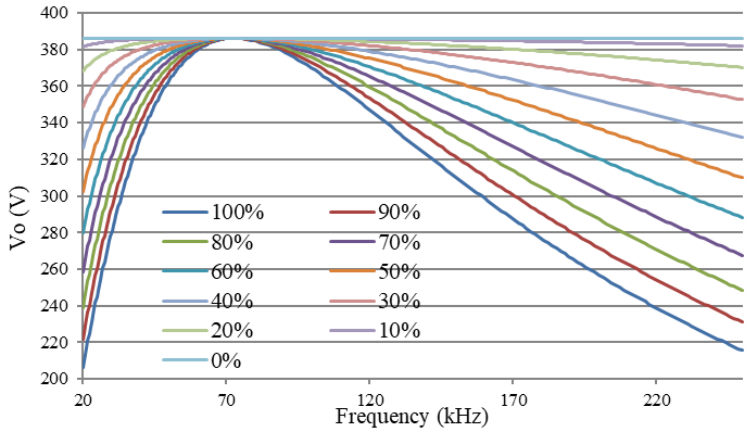

Figure 8. Large signal gain of a SRC. The converter's input voltage is 50.5 V and the transformer turn ratio is 4:15. Therefore, its nominal unity gain corresponds to the 385 V output. The series in the graph are a function of the percentaje of the nominal load of the converter.

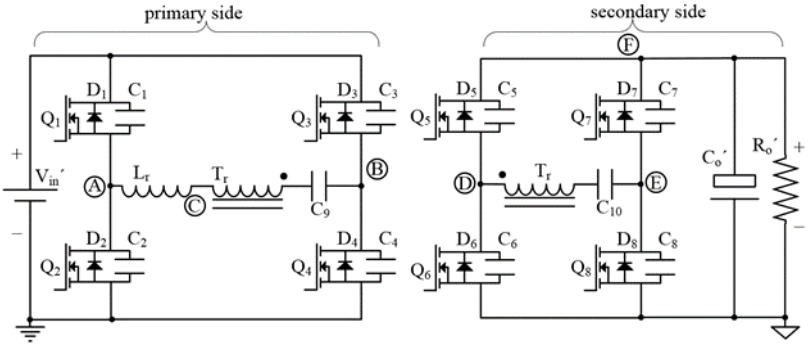

Figure 9. CLLC or bidirectional LLC converter simplified circuit.

1.2. QUASI-RESONANT CONVERTERS

Quasi-resonant converters normally operate at a fixed frequency. The large signal gain of the quasi-resonant converters can be adjusted controlling the duty: the percentage of the period during which a power transfer occurs given by the ratio of the time a set of switches are in their on-state and their off-state. Similarly to the resonant converters, quasi-resonant converters also take advantage of inductors and capacitors to achieve ZVS or ZCS.

The Dual Active Bridge (DAB) is a quasi-resonant converter which commonly comprises a full bridge in the primary side and a full bridge in the secondary side, although other configurations are possible (Figure 10). The DAB can use the energy in a series inductor to charge and discharge the parasitic capacitances of the semiconductor switches and achieve ZVS in both the primary and secondary side switches. Like the LLC, DAB can operate as a step-up or as a step-down converter. However, its main attractive is that, unlike the LLC, DAB it is a fully symmetric converter and can operate as a step-up and step-down also in its reverse mode of operation. Moreover, the steady state gain and the direction of the power flow depends on the shift between the primary and the secondary side bridges. Therefore, the operation of DAB as a bidirectional converter is seamless and straightforward.

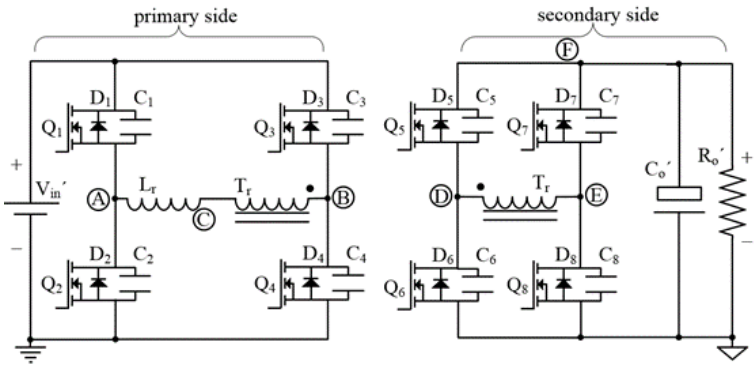

Figure 10. DAB converter simplified circuit.

However, the ZVS range of DAB is limited. Moreover, it is not very well suited for wide range converters built with Si MOSFETs. When the converter operates away from the nominal conditions the primary side devices or the secondary side devices can become hard-switched or even hard-commutated. Although it is possible to extend the ZVS range of the converter increasing the magnetizing inductance and with a careful design, the resulting circulating currents increases the overall losses and the performance of the converter becomes poor. Therefore, the DAB is mostly attractive when combined with devices which can operate reliably in hard-commutation and with a reasonable switching loss (mostly Wide Band Gap (WBG) devices).

The PSFB is a quasi-resonant buck derived isolated converter. The circuit configuration of the PSFB is very similar to the DAB. However, the PSFB includes at least one more inductor at the output [17] (Figure 11). Thanks to the output inductor, the *rms* currents in the secondary side of the converter and the output voltage ripple are lower than in the other two converters (LLC and DAB). Moreover, the output inductor provides energy for the ZVS transitions of one of the primary side legs in nearly all the load range (the ZVS range of the other primary side leg is comparatively limited). However, because of the output inductor, the drain voltage of the secondary side rectifiers is not clamped by the output capacitance of the converter. Therefore, the blocking voltage requirements for the secondary side rectifiers are higher in PSFB than in DAB or LLC. Moreover, the PSFB circulates current in the primary side during the freewheeling phase which does not contribute to the power transfer but unnecessarily increases the conduction losses.

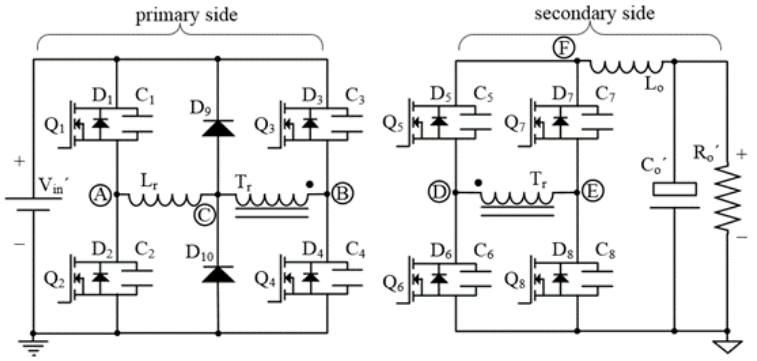

Figure 11. PSFB converter simplified circuit.

Like the LLC, the PSFB is not a symmetric converter. In its reverse mode of operation it is commonly known in the literature as current-fed isolated boost converter. In the reverse operation the secondary side switches can suffer of high drain voltage overshoots which may require auxiliary clamping, snubbering or alternative control schemes to avoid the stress conditions.

Therefore, the PSFB is well suited for high efficiency LV output applications with Si MOSFETs. Moreover, it is better suited for wide range operation with Si MOSFETs than the DAB converter. However, traditionally it is not an attractive alternative for bidirectional applications because of the well known problems of the current-fed isolated boost converters.

2. SCOPE OF THE THESIS

2.1. LLC CONVERTER

The LLC has become the most popular topology for high efficiency DCDC converters in commercial applications. The LLC converter can achieve very high efficiencies with a simple circuit and very low component count. Figure 12 represents the efficiency of a half-bridge LLC with full-bridge rectification. Moreover, the LLC can be designed to achieve its maximum efficiency at its nominal operation point while fulfilling the requirements for wide range input or wide range output. However, it is challenging to optimize the design of conventional LLC converter in wide gain range applications. A wide range of switching frequencies leads to a large transformer core, high core loss, and low power density. Furthermore, a high peak gain requires a small magnetizing inductance, which results in increased circulating currents and degraded efficiency [18].

Wide range input is required for example during hold-up time. In high reliability applications the converter should continue working up to 20 ms while the AC input is missing. During this time the voltage at the input filter of the DCDC converter drops at a ratio given by the amount of capacitance and the rated output power of the converter. The reader should note that a big amount of input capacitance is usually undesired due to its cost and high volume.

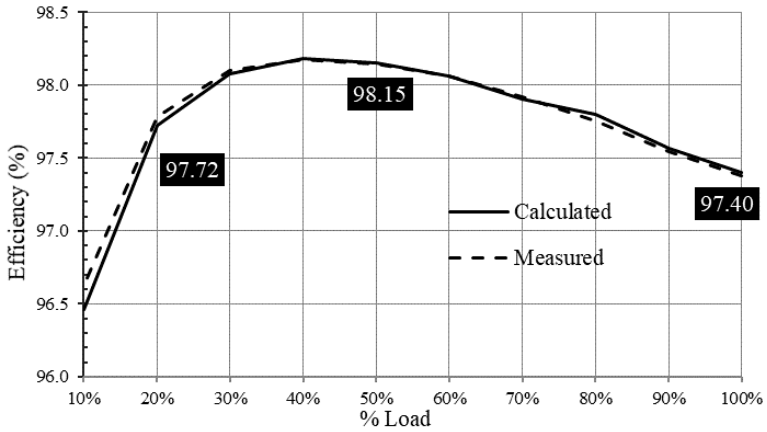

Figure 12. Calculated and measured efficiency of the half-bridge LLC in Chapter 5.

Wide range output is required for example in battery charging applications. The DCDC converter has to operate giving a constant current or constant power at the lower voltages when the battery is discharged. On the other hand, the DCDC converter has to operate at a constant voltage when the battery is fully or nearly-fully charged. The careful consideration of the operation profile of the converter is very important for the design of highly-efficient DCDC converters. One of the main design constraints of the LLC converter is the maximum gain achievable at the maximum load of the converter. Moreover, operating in the range of high-load and high-gain increases the peak flux in the magnetics (Figure 13) and the voltage and current ripple in the resonant capacitor (Figure 14). However, the battery charger does not require to provide its maximum current at its maximum output voltage. Therefore, a converter designed to provide the maximum load at the maximum gain would be over-dimensioned for its purpose in such example.

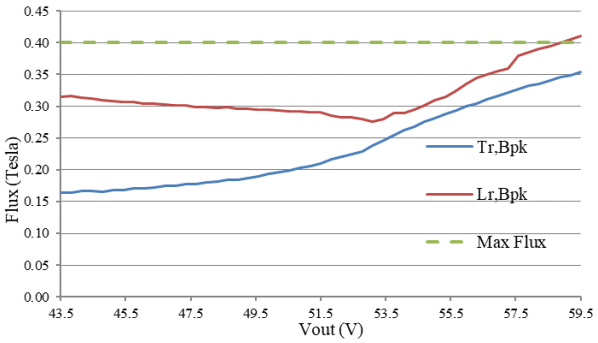

Figure 13. Estimation of peak flux in the main transformer ($T_{r,Bpk}$) and in the external resonant inductor ($L_{r,Bpk}$) in an LLC converter at 100 % of its power and different output voltages.

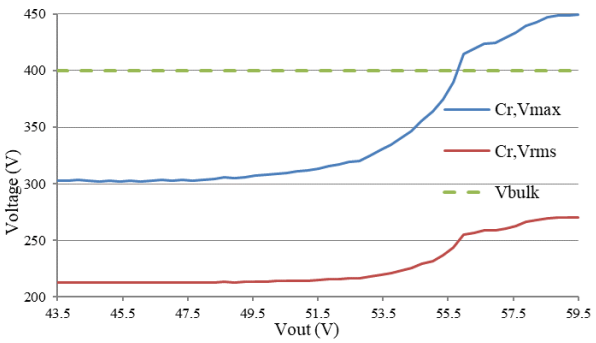

Figure 14. Estimation of maximum amplitude ($C_{r,Vmax}$) and *rms* ($C_{r,Vrms}$) of the voltage ripple in the resonant capacitors of an LLC converter at 100% of its power and different output voltages.

The maximum efficiency of the converter is achieved near the resonance between the series inductor and the series capacitor (normalized unity gain of the converter) (Figure 15). Operating in this area the primary circulating currents (transformer magnetizing current) and the related conduction losses are relatively small. Moreover, the switching frequency and the related switching and core losses are also relatively low. Moving away from this operation point increases the conduction and core losses or alternatively increases the switching losses and degrades the overall performance of the converter.

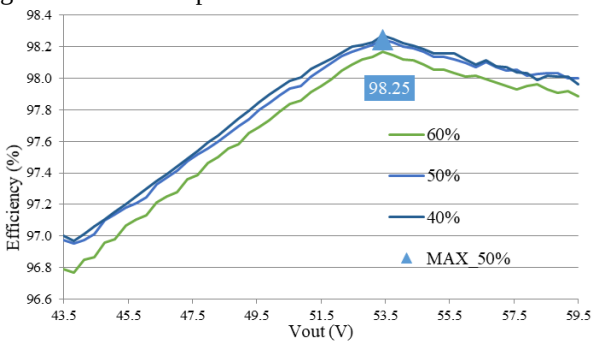

Figure 15. Efficiency of a wide output range LLC converter at different output voltages.

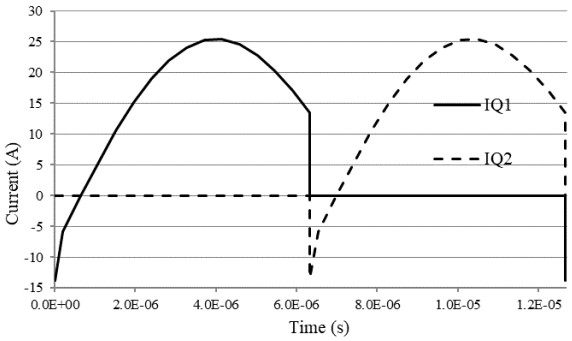

Figure 16. Current passing through the primary side devices in the LLC at full power (400 V input and 51.5 V output).

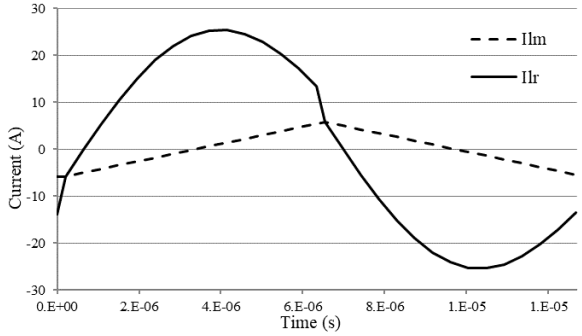

Figure 17. Current passing through the primary side of the transformer (I_{lr}) and the magnetizing component (I_{lm}) in the LLC converter at full power (400 V input and 51.5 V output).

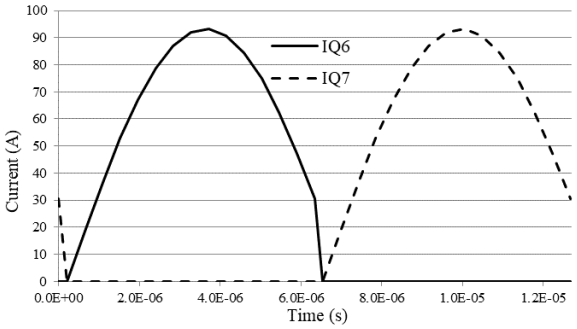

Figure 18. Current passing through the secondary side rectifiers in the LLC at full power (400 V input and 51.5 V output).

The characteristic sinusoidal shape of the currents in resonant converters can be well appreciated in Figure 17, Figure 16 and Figure 18. Observe that the *rms* of the sinusoidal waveforms is comparatively higher than the *rms* of equivalent (of same average value) trapezoidal waveforms in quasi-resonant or PWM converters. However, thanks to their sinusoidal shape the turn-off currents of the primary and secondary side devices can be relatively low in comparison to other PWM converters, which potentially decreases the switching losses.

Other advantage of the LLC converter is that it can use the energy in the series inductor and the energy in the magnetizing inductance of the main transformer for the discharge of the parasitic capacitance of the semiconductor switches and achieve ZVS. Therefore, the ZVS range can be easily extended in this topology. Moreover, because a relatively small magnetizing inductance is required for achieving the required gain in wide range converters, ZVS range is usually achievable for virtually any possible $R_{ds,on}$ in the primary side HV switches. Therefore, the increased output capacitance of Si MOSFETs in comparison to SiC MOSFETs does not have a big impact on the design criteria in such scenario. Moreover, the non-linear capacitance of Si SJ MOSFETs provides more tolerance for the adjustment of the optimum dead times (Figure 19, Figure 20, Figure 21 and Figure 22). Furthermore, the voltage drop of the SiC MOSFETs intrinsic body diode (around 3 V) is several times higher than for Si SJ MOSFETs (around 1 V), which makes it less sensitive to inaccuracies in the dead time adjustment.

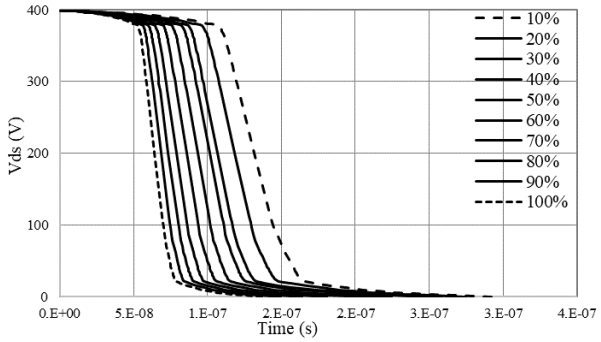

Figure 19. Simulated hard-switched turn-off transitions in a half-bridge 3.3 kW LLC at different loads with CoolMOS CFD7 31 mΩ.

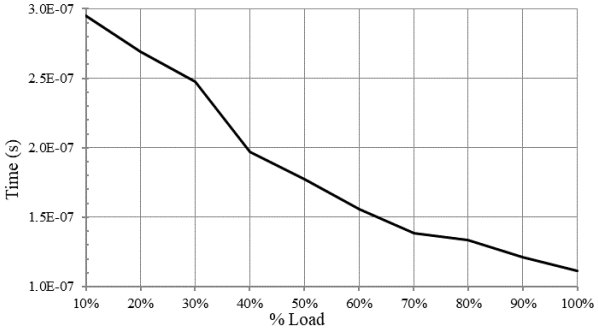

Figure 20. Simulated optimum dead time for achieving ZVS in a half-bridge 3.3 kW LLC at different loads with CoolMOS CFD7 31 mΩ.

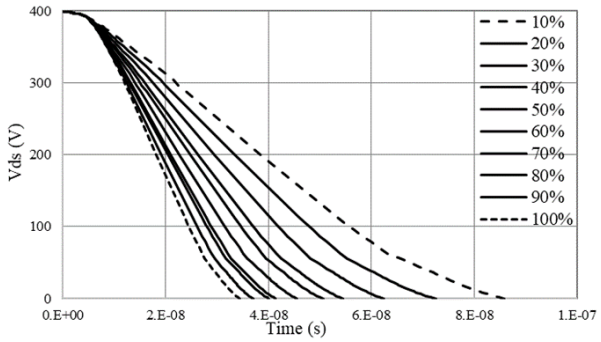

Figure 21. Simulated hard-switched turn-off transitions in a half-bridge 3.3 kW LLC at different loads with CoolSiC 31 mΩ.

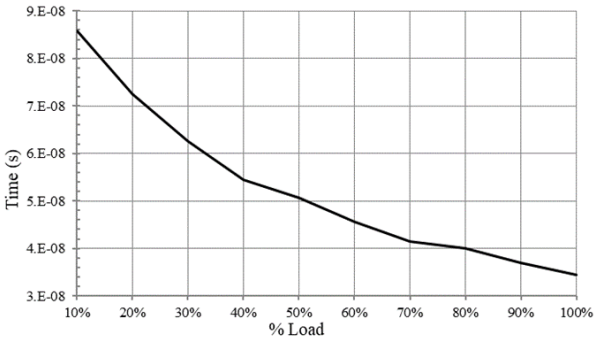

Figure 22. Simulated optimum dead time for achieving ZVS in a half-bridge 3.3 kW LLC at different loads with CoolSiC 31 mΩ.

2.2. DAB CONVERTER

The DAB is a fully symmetric converter in which the large signal gain is controlled by the overlap or phase shift between the primary side and the secondary side duty and the direction of the power flow is controlled by the sign of the phase shift between the primary and the secondary side duty [23]-[24]. In its most simple modulation scheme the primary and the secondary side devices are controlled by a fixed frequency 50 % duty signal. Other more advanced modulation schemes are possible in which the duty of the primary, the secondary or both sides can vary. Moreover, in [25]-[26] a modulation scheme with variable frequency is proposed which helps extending the achievable ZVS range of the converter. The proposed classification in [27]-[28] of possible modulation schemes includes:

- Primary and secondary side 50 % duty, control of phase shift between primary and secondary, so-called Single-Phase-Shift (SPS).
- Primary side variable duty, secondary side 50 % duty, control of phase shift between primary and secondary, so-called Extended-Phase-Shift (EPS).
- Primary and secondary side variable duty, control of phase shift between primary and secondary, which includes the so-called Double-Phase-Shift (DPS) and Triple-Phase-Shift (TPS) modulation schemes.

Whereas the most advanced modulation schemes bring the advantage of an extended ZVS range, and lower *rms* currents through the converter in part of the operation range, the control complexity greatly increases. Moreover, the simple 50 % duty modulation allows the implementation of a DAB converter with a half-bridge in the primary and center tapped rectification in the secondary, which greatly reduces the circuit complexity of the circuit and has a total component count at the level of LLC converters (Figure 23). Furthermore, the efficiency levels that can be achieved in this configuration are potentially near the level of an LLC with similar specifications (Figure 24).

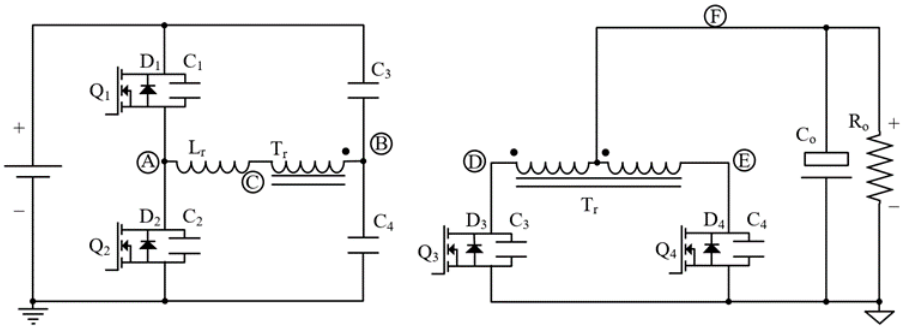

Figure 23. DAB converter realized with a half-bridge in the primary side and center tapped configuration in the secondary side.

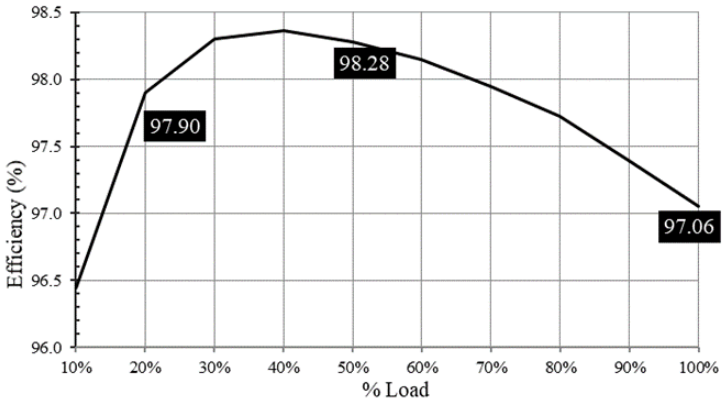

Figure 24. Calculated efficiency for a half-bridge 3.3 kW DAB with 400 V input and 51.5 V output.

The DAB converter is not well suited for wide range applications with Si SJ MOSFETs. The ZVS operation range is limited at light loads [22], [24], [29]. Moreover, the primary side or the secondary side can become hard-commutated depending on the load, the input and the output voltages. However, the issue can be alleviated increasing the primary side magnetizing currents, at the expense of the additional circulating currents and the related conduction losses (Figure 25). This approach can be effective in narrow range output converters, but would require excessively low magnetizing inductance in wide input and wide output converters where the converter is bucking (Figure 26) or boosting (Figure 27) by a relatively big ratio.

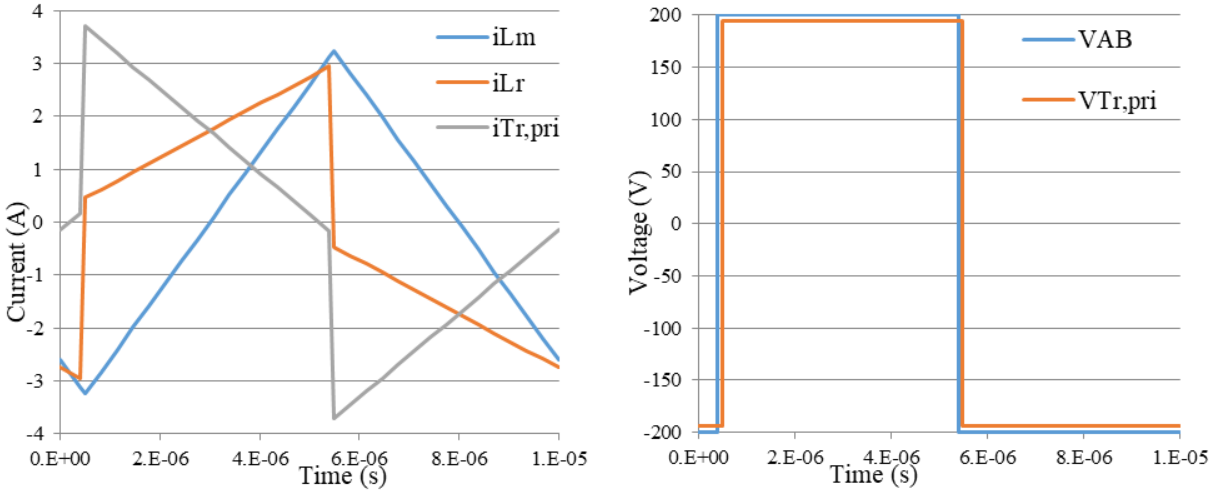

Figure 25. DAB primary side currents and primary side voltages operating near normalized unity gain with 400 V input to 51.5 V output and at 10 % of the rated load. The main transformer turns ratio is 15 to 4.

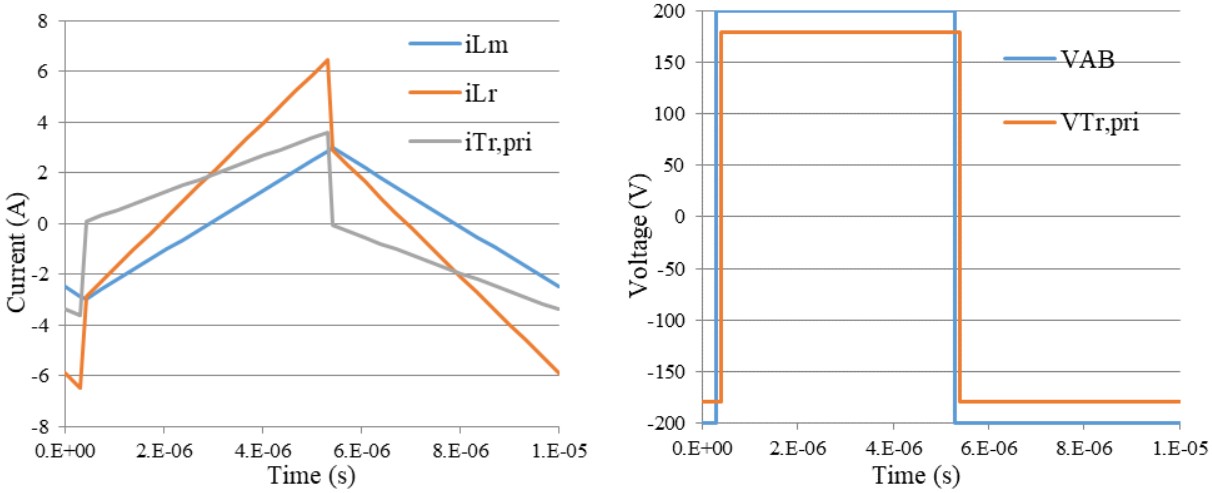

Figure 26. DAB primary side currents and primary side voltages while bucking with 400 V input to 47.5 V output and at 10 % of the rated load. The main transformer turns ratio is 15 to 4.

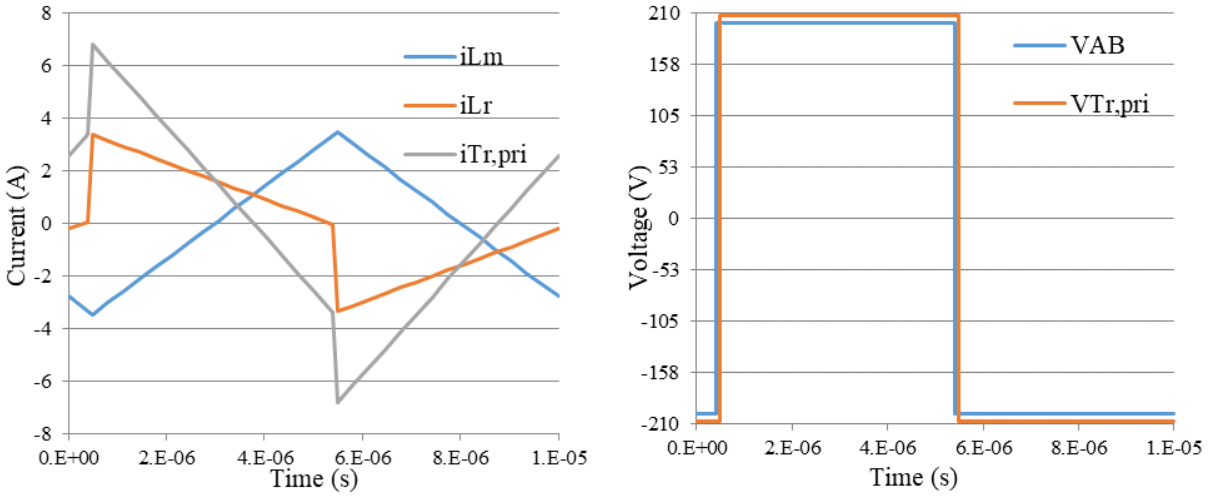

Figure 27. DAB primary side currents and primary side voltages while boosting with 400 V input to 55 V output and at 10 % of the rated load. The main transformer turns ratio is 15 to 4.

Si MOSFETs do not operate reliably nor efficiently in continuous hard-commutation. On the one hand the *di/dt* and *dv/dt* over the device and over its intrinsic body diode could cause failure of the device through several mechanisms extensively reported in the literature [19]-[21]. On the other hand, the switching losses increase greatly due to the additional reverse recovery charge Q_{rr} which adds on top of the already big output charge Q_{oss} of the device. However, Wide Band Gap (WBG) power devices have very low or no Q_{rr} and can operate reliably and

much more efficiently in continuous hard-commutation. Therefore, WBG is the common choice for the implementation of DAB converters. In spite of that, the efficiency still drops substantially when the converter losses ZVS, which can be observed in Figure 28 for the 40 % of the rated load at the higher output voltages.

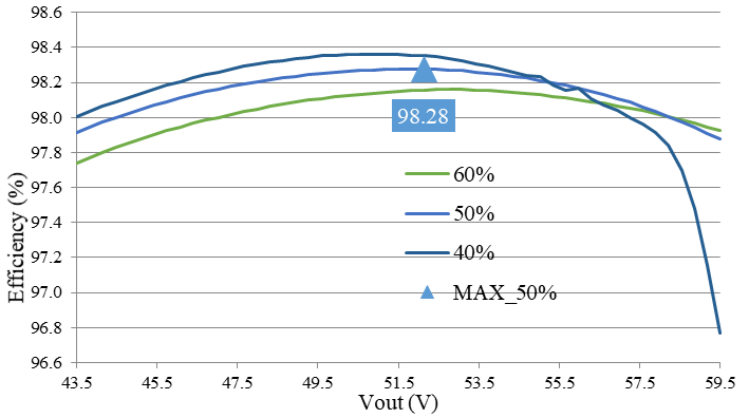

Figure 28. Calculated efficiency of a wide output range DAB converter at different output voltages.

The energy available for achieving ZVS in DAB comes solely from the energy stored in the series inductor. Therefore, the series inductor should be dimensioned in accordance to the required ZVS range. However, like in the PSFB, excessively big series inductor limits the effective available duty cycle and the maximum output power of the converter (Figure 29). It can be observed in Figure 30 how the voltage-time integral of the series inductor increases for the lower output voltages at a fixed output power (increasing output current). In [23] a design method is proposed where it is found that the series inductance should be designed to reach a maximum 30 % of the duty at the maximum load. Moreover, in [23] and [30] it is suggested varying the switching frequency depending on the output voltage to expand the ZVS region.

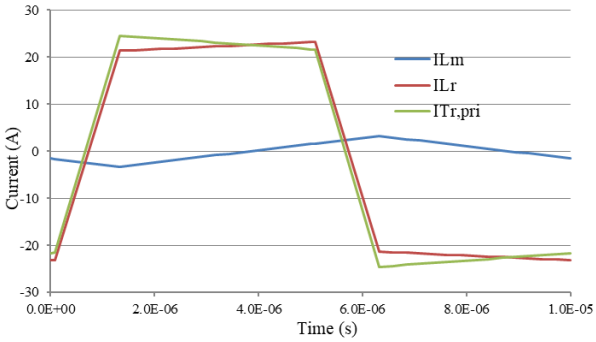

Figure 29. Current passing through the primary side of the transformer in a DAB converter at full power (400 V input and 51.5 V output).

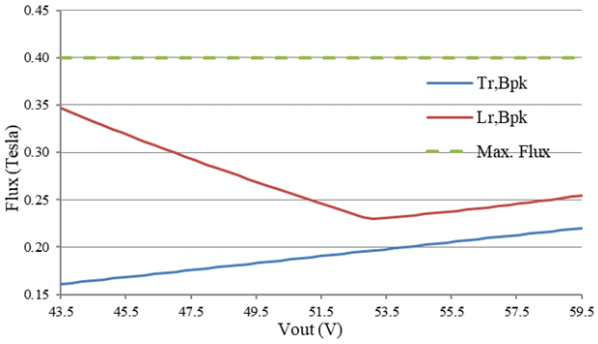

Figure 30. Estimated peak flux in the main transformer and in the external resonant inductor in a DAB converter at 100% of its power and different output voltages.

A major drawback of the DAB is the recirculating of currents from the output back to the input side of the converter. Unlike other DCDC topologies, the secondary side devices operate as active switches, not only as rectifiers or synchronous rectifiers, allowing the current to flow against the antiparallel body diode during the polarity inversion of the main transformer (Figure 31, Figure 32 and Figure 33). Therefore, apart from the related additional conduction losses, the output current ripple and output voltage ripple of this converter requires of further filtering in comparison to the LLC or the PSFB.

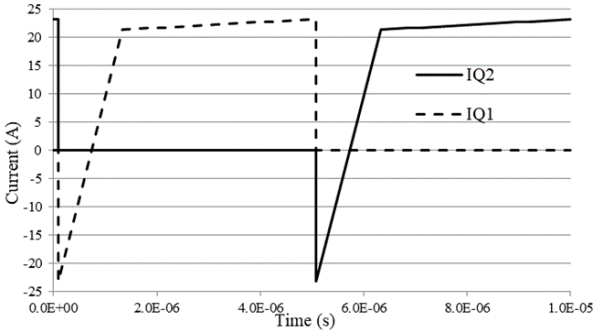

Figure 31. Current passing through the primary side devices in a DAB converter at full power (400 V input and 51.5 V output).

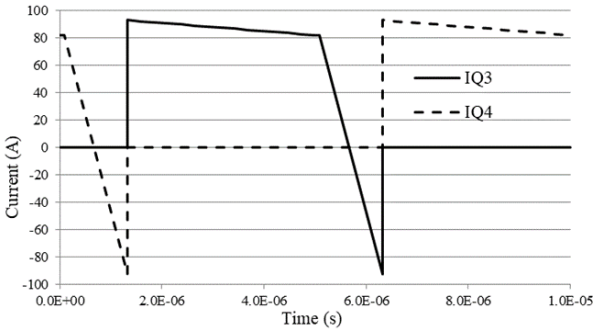

Figure 32. Current passing through the secondary side rectifiers in a DAB converter at full power (400 V input and 51.5 V output).

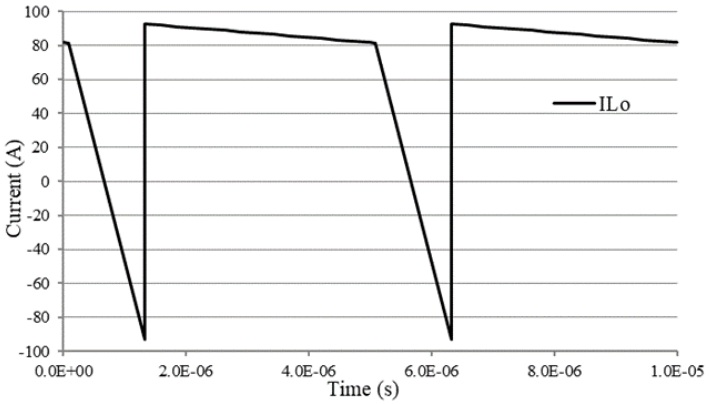

Figure 33. Current at the output of the rectification stage in a DAB converter at full power (400 V input and 51.5 V output).

Unlike in the LLC, the energy in the magnetizing inductance is not available for the quasi-resonant transitions. Therefore, the ZVS range is limited in comparison to the resonant converter (Figure 34 and Figure 35), which also makes WBG devices better suited for this topology (Figure 36 and Figure 37) thanks to their relatively smaller output capacitance.

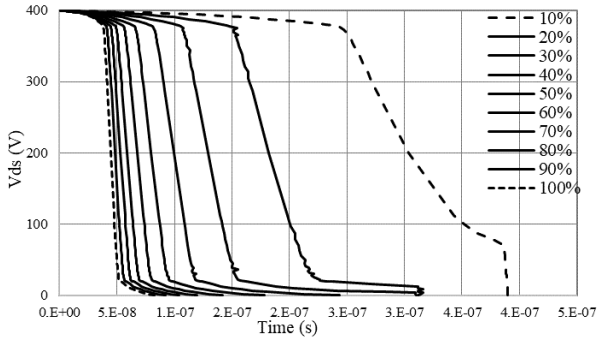

Figure 34. Simulated hard-switched turn-off transitions in a half-bridge 3.3 kW DAB at different loads with CoolMOS CFD7 31 mΩ.

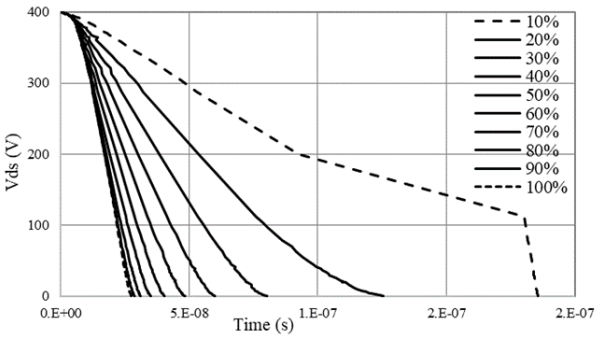

Figure 36. Simulated hard-switched turn-off transitions in a half-bridge 3.3 kW DAB at different loads with CoolSiC 31 mΩ.

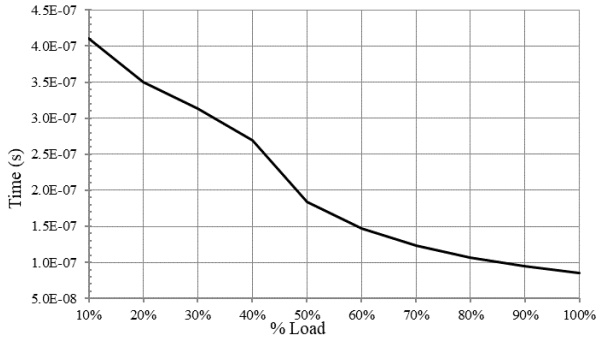

Figure 35. Simulated optimum dead time for achieving ZVS in a half-bridge 3.3 kW DAB at different loads with CoolMOS CFD7 31 mΩ.

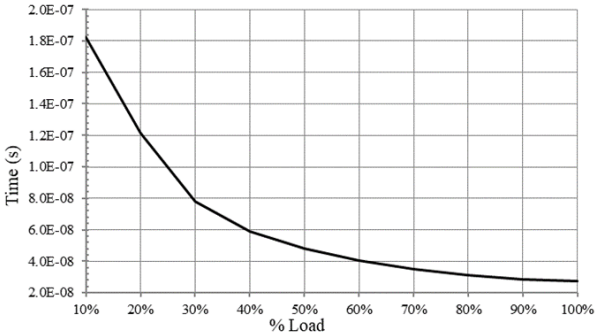

Figure 37. Simulated optimum dead time for achieving ZVS in a half-bridge 3.3 kW DAB at different loads with CoolSiC 31 mΩ.

2.3. PSFB CONVERTER

The PSFB converter is a fixed frequency PWM converter. The large signal gain of the converter is controlled by the phase shift between the two primary side legs. Each of the primary side legs or half-bridges are controlled by a fixed 50 % duty cycle PWM. Although other alternative modulation scheme exists which also vary the duty [31]-[32], they generally cause the loss of ZVS and are not commonly used. In [33] the switching frequency of the converter is modulated along the load, tracking the best steady state efficiency. However, the switching frequency does not control the large signal gain of the converter like in a resonant converter.

The PSFB is well acknowledged by its robustness, reliability [34]-[36] and relatively high efficiencies (Figure 38). The inductor at the output of the converter reduces de output current and the output voltage ripple. Moreover, limits the currents through the converter in the event of short-circuit and provides energy for the quasi-resonant transition of one of the primary side bridge legs.

However, the output inductor is also one of the main drawbacks of the topology for two main reasons. Firstly, it decouples the secondary side rectifiers from the output filter capacitors, which increases the blocking voltage requirements of the rectifiers in comparison to other topologies like DAB or LLC (Figure 39) [37]-[38]. Secondly,

it makes the converter asymmetric for its bidirectional operation, and therefore rarely considered as an alternative for bidirectional applications.

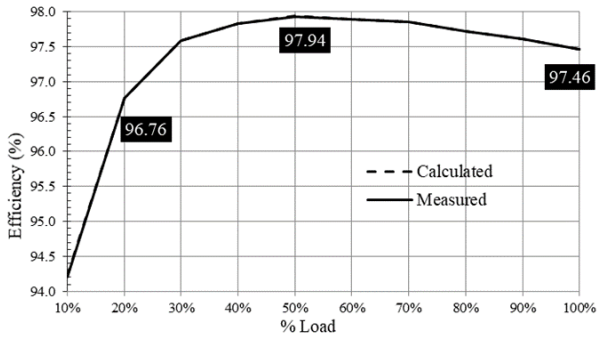

Figure 38. Calculated and measured efficiencies for a 3.3 kW PSFB with 380 V input and 54.5 V output.

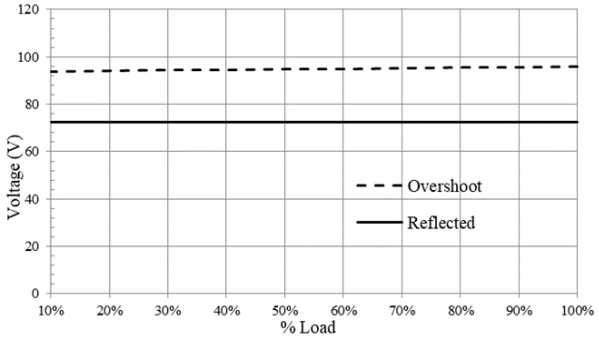

Figure 39. Secondary side overshoot and reflected voltage in a 3.3 kW PSFB with 380 V input and 54.5 V output.

In the PSFB the available energy for the quasi-resonant ZVS transitions of the two primary side bridge legs is different. The leg which transitions right after the end of the power transfer, so-called lagging, uses the energy in the series inductor and the output inductor and can easily achieve ZVS in all the load range of the converter (Figure 40 and Figure 43). The leg which transitions right before the next power transfer, so-called leading, only uses the energy in the series inductor and has a very much reduced ZVS range (Figure 41 and Figure 44). In [39]-[41] auxiliary circuitry is proposed to increase the ZVS range independently of the load in ZVS PSFB converters. However, the auxiliary circuitry requires of additional components and cause additional conduction and core losses in all the load range.

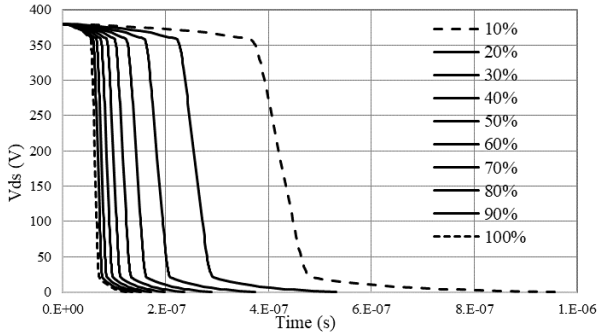

Figure 40. Simulated hard-switched turn-off transitions in the lagging leg of a 3.3 kW PSFB at different loads with two CoolMOS CFD7 75 mΩ devices in parallel.

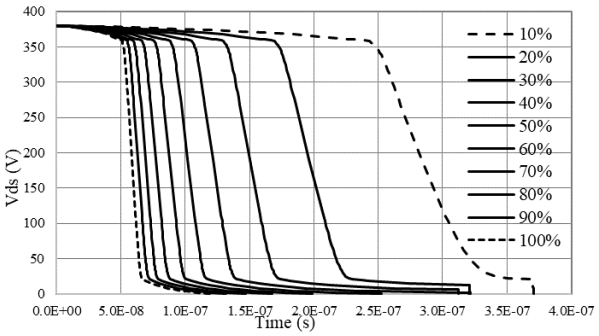

Figure 41. Simulated hard-switched turn-off transitions in the leading leg of a 3.3 kW PSFB at different loads with two CoolMOS CFD7 75 mΩ devices in parallel.

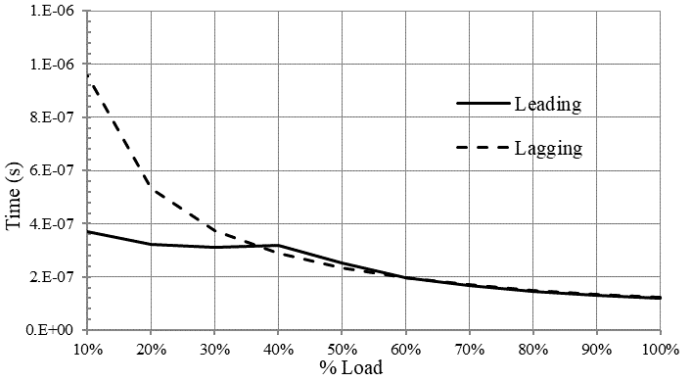

Figure 42. Simulated optimum dead time for achieving ZVS in a 3.3 kW PSFB at different loads with two CoolMOS CFD7 75 mΩ devices in parallel.

The leading and the lagging legs transition times also differ due to the different amount of energies available and the different time constant of the components involved in the resonance of the resulting equivalent LC circuits (Figure 42 and Figure 45). Therefore, the dead times in the PSFB converter can have relatively complicated adjustment and independent among each of the legs [42]-[45]. Moreover, the values of the inductances and capacitances in the circuit are subjected to tolerances which makes it difficult to achieve the optimum dead times in mass produced converters. In this aspect, Si SJ MOSFETs can be advantageous in comparison to WBG devices due to

their non-linear capacitance and the relatively low voltage drop of their intrinsic body diode. The non-linear capacitance extends the margin for a near optimum dead time in comparison to the more linear capacitance of WBG devices (Figure 40 and Figure 43).

Due to the limited ZVS range in PSFB converters it is expected that WBG devices will achieve higher efficiency thanks to their better FoM. In [46] the peak efficiency of the converter is increased from 97 % with Si MOSFETs up to 98.3 % with SiC MOSFETs. However, the potential improvement would depend on how well optimized was the original design for the particular characteristics of the Si MOSFETs or the SiC MOSFETs and has to be evaluated in every specific case.

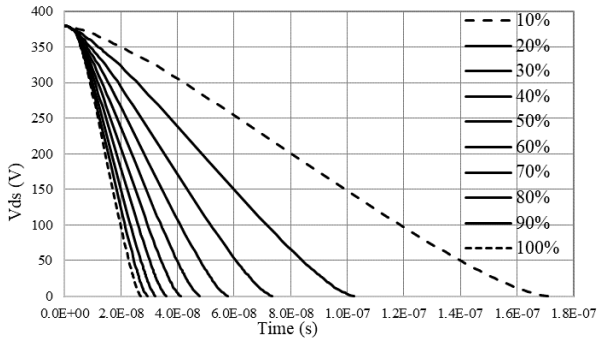

Figure 43. Simulated hard-switched turn-off transitions in the lagging leg of a 3.3 kW PSFB at different loads with two CoolSiC 75 mΩ devices in parallel.

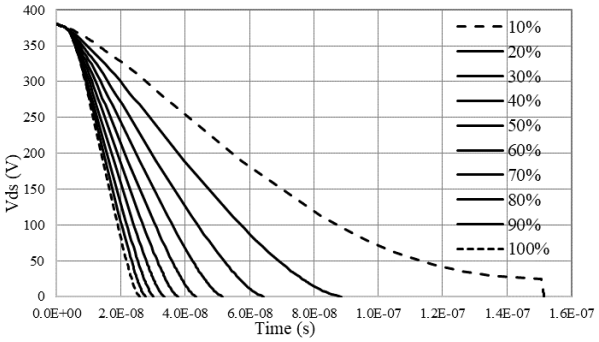

Figure 44. Simulated hard-switched turn-off transitions in the leading leg of a 3.3 kW PSFB at different loads with two CoolSiC 75 mΩ devices in parallel.

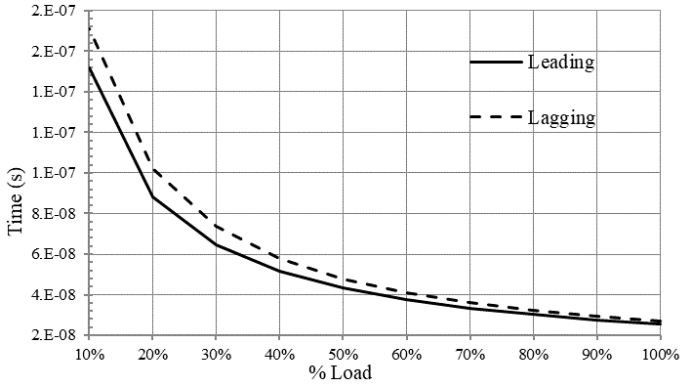

Figure 45. Simulated optimum dead time for achieving ZVS in a 3.3 kW PSFB at different loads with two CoolSiC 75 mΩ devices in parallel.

Unlike in the LLC or in the DAB, in the PSFB is preferred to realize the series inductor as a component external to the leakage of the main transformer. This allows the reduction of the secondary side rectifiers overshoot and the increase on the available energy for the ZVS transition of the leading leg [17]. Nevertheless, like in the LLC or in the DAB, in the PSFB the magnetics can also be integrated, partially cancelling the flux in the core and overall increasing the power density and cost of the converter [48].

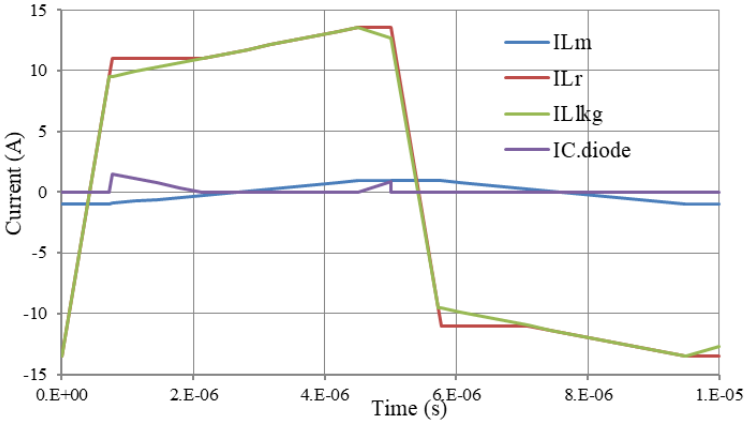

Figure 46. Current passing through the primary side of the transformer in a 3.3 kW PSFB converter at full power (380 V input and 54.5 V output).

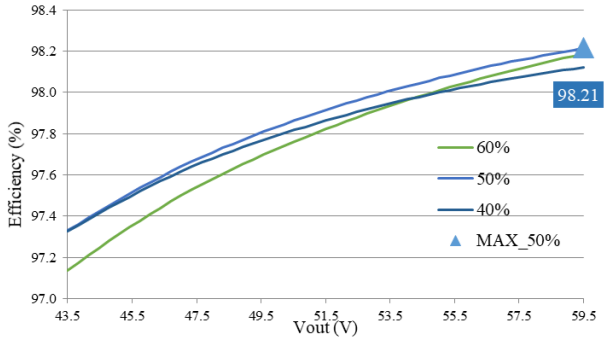

Figure 47. Calculated efficiency of a wide output range PSFB converter at different output voltages.

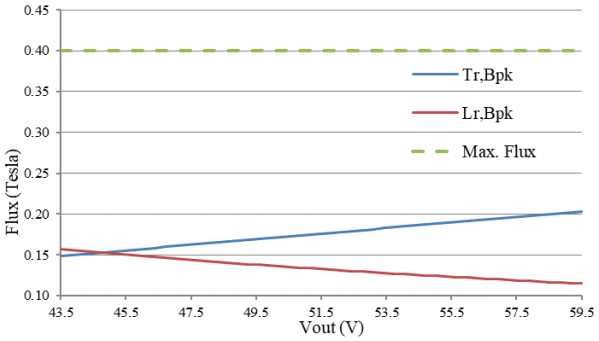

Figure 48. Peak flux in the main transformer and in the external resonant inductor in a PSFB converter at 100% of its power and different output voltages.

Another drawback of the PSFB converter is caused by the circulating currents in the primary side during the freewheeling phase (Figure 46). During the freewheeling, the transformer is virtually shorted by the secondary side rectifiers and there is no effective power transfer from the primary to the secondary. On the other hand, the converter has to be designed constrained by the required maximum gain, which is generally needed at the minimum input voltage, maximum output voltage and maximum output power. Therefore, the minimum circulating currents and the maximum efficiencies of the converter occur at the higher large signal gains (Figure 47 and Figure 48). Contrary to the LLC or DAB, the PSFB converter is not designed to operate at its maximum efficiency in nominal conditions, but during hold-up time or at its maximum output voltage.

Although the current passing through each of the primary side bridge devices is not symmetric, the *rms* values are nearly equal between them. However, the lagging leg has longer conduction time in the third quadrant, which might be a concern while using devices like IGBTs which require of a parallel diode [47].

Thanks to the output inductor, the *rms* currents through the secondary side of the converter are comparatively lower than in LLC or DAB (Figure 50 and Figure 51). Moreover, the current ripple and the voltage ripple is intrinsically lower in this topology. However, the turn-off currents of the primary and the secondary side devices are comparatively larger than in the LLC which causes additional switching losses [37]. The secondary side rectifiers additional switching losses are aggravated by the higher blocking voltage requirements which generally implies a worse FoM (with higher parasitic capacitances and reverse recovery charges for an equivalent $R_{ds,on}$).

The PSFB operated as a bidirectional converter operates as a voltage-fed converter in the forward operation and as a current-fed boost converter in the reverse flow operation [51]. The term bidirectional PSFB is often mistaken by a DAB due to the second being commonly constituted of two bridges and controlled by the phase shift between the primary and the secondary bridge. The bidirectional PSFB converter is also frequently found in the literature by the name of isolated current-fed boost converter [52]-[53]. However, it is commonly acknowledged that the bidirectional PSFB converter has several issues: high voltage overshoot in the current-fed side devices and incapability of starting with a discharged storage capacitor in the voltage-fed side [54]-[58].

We find some examples in the literature of very high efficiency PSFB DCDC converters reaching near 99 % of efficiency in a stand-alone 5 kW DCDC converter [49]-[50], or within a full 2.2 kW PSU for server applications complying with the Titanium efficiency specifications [42].

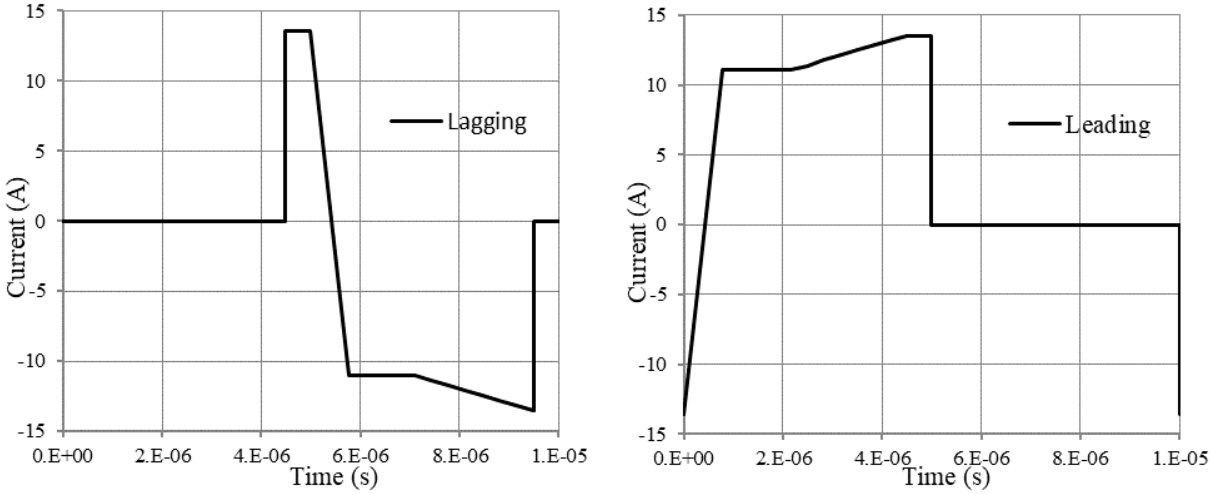

Figure 49. Current passing through the primary side devices in a PSFB converter at full power (380 V input and 54.5 V output).

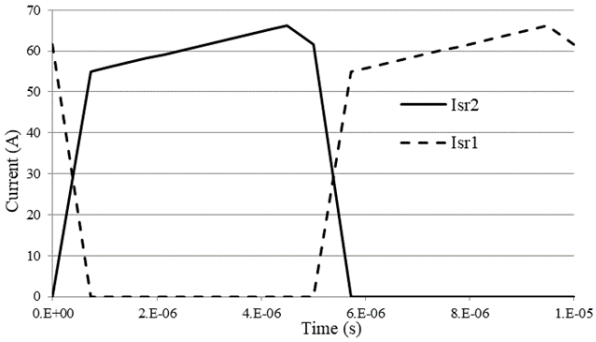

Figure 50. Current passing through the secondary side rectifiers in a PSFB converter at full power (380 V input and 54.5 V output).

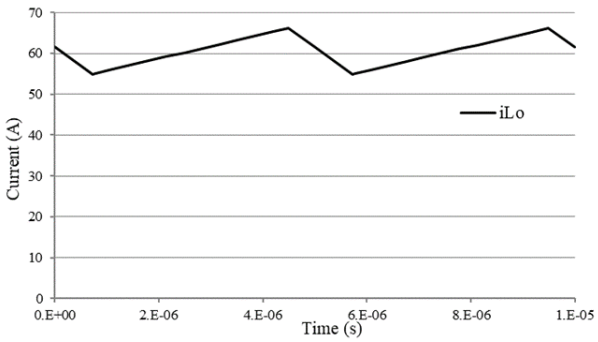

Figure 51. Current at the output of the rectification stage in a PSFB converter at full power (380 V input and 54.5 V output).

2.4. OTHER CONVERTERS

Finally it is worth to mention some benchmark examples of the highest efficiency achievable in isolated DCDC conversion stages with innovative concepts like a three phase LLC with magnetics integration [59]-[61] and a PSU comprised of three conversion stages [62]-[63].

The three phase LLC includes an integrated transformer [64] and phase shift among the three half-bridges. Thanks to the integration and the phase shift is possible to achieve partial flux cancellation in the core of the transformer reducing the core losses. Moreover, the interleaving of the three phases decreases the output current and output voltage ripple, which are two of the main disadvantages of the LLC. However, due to the complexity of the circuit and the magnetics construction, this topology is not very spread and best suited for very high power and very high efficiency. Furthermore, due to the tolerances in the values of the resonant tank elements and the accuracy of the control timings the current does not share equally between the three phases. In [65] a closed-loop phase shift control is proposed for balancing the current among phases.

A three stage PSU generally comprises a resonant or quasi-resonant converter that operates at its best efficiency point, providing isolation and the conversion ratio given by the transformer. This mode of operation is frequently known as solid-state transformer in the literature and also common in other applications requiring isolation [66]. A third stage non-isolated provides the tightly regulated output [3]. In theory both DCDC stages can achieve very high efficiency with a very good overall performance of the complete PSU. However, in spite of the increased circuit complexity it is hard to achieve the same level of efficiency in a two-step conversion than in a well design single-step resonant converter [62]. Moreover, the concept has been registered and protected by patents which limits its commercial application.

3. CONCLUSIONS

For the currently available power switching devices the resonant and quasi-resonant converters are the most attractive options for achieving high efficiency, high power density or a combination of both at a reasonable cost. The key advantage of the resonant and quasi-resonant converters is the reduction of the switching losses. The switching losses can be reduced achieving ZVS for the turn-on transition and ZCS for the turn-off transition.

Among the isolated, resonant and quasi-resonant DCDC converter topologies, the most common ones in medium and high-power, and high-voltage applications are the LLC, the PSFB and the DAB [3] due to their simplicity and high efficiencies. Among those topologies each one has its own advantages and disadvantages, which makes each of them best suited for different applications, power and voltage ranges. That can be observed by the fact that all of the alternatives are still used today commercially, and all the alternatives continue being subject of research and study. A strong motivation for research comes from the fact that the development of new semiconductor technologies, novel magnetic constructions or control techniques can overcome past limitations or enable higher levels of performance beyond the previous theoretical boundaries.

In isolated converters the transformer is key in achieving high efficiency and high power density. The main transformer has two main contributions to the losses: core loss and conduction loss. The core loss is proportional to the switching frequency and the flux density. The conduction loss in the transformer becomes increasingly complicated to estimate as the switching frequency increases (skin, proximity and fringing effects). The same principles apply to other magnetics in the converter like the series resonant choke or the output filter inductor. This is the reason why so many studies focus in improving the magnetics: reducing the flux density [64], or improving their construction to alleviate the effects of the high frequency in the conductors [67]-[68].

This thesis work will be focus in the study of the LLC and the PSFB. Both of this topologies are very promising and well suited for any of the available semiconductor technologies in the market, specifically for Si SJ MOSFETs, which are currently the most mature devices and the most competitive in cost now and in the foreseeable future.

Moreover, the objective of this work is the optimization, improved reliability and functionality of the LLC and the PSFB maintaining as much as possible the simplicity of the standard circuit configuration.

Therefore, in this thesis two converters with similar specifications and similar magnetic construction has been designed and built to study the achievable performance of the two main topologies objective of this work: LLC and PSFB. It has been found that, although PSFB can achieve higher efficiencies than is commonly expected thanks to the new devices and control techniques, the LLC is still potentially superior and capable of still higher efficiencies with less components and less cost. However, in bidirectional applications the large signal gain range of the PSFB makes it arguably superior to the LLC.

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SECTION I. CONVERTERS

CHAPTER 3. PSFB 1400 W FOR SERVER APPLICATIONS

1. INTRODUCTION

The trend in server power supplies in recent years has been towards increased power density with optimized cost. Achieving this higher power density, high efficiency is a key parameter since heat dissipation must be minimized. Towards this goal, fully resonant topologies like LLC are often considered to be the best approach in this power range and voltage class [1]. However, the 1400 W PSFB DCDC converter introduced in this chapter is an example of how the improvement in semiconductor technologies and control algorithms allow a simple and well known topology block like the PSFB to reach the high efficiency levels traditionally considered out of reach for this topology.

This chapter presents the specifications, performance and experimental results of a 1400 W PSFB DCDC converter, including its innovative magnetic construction and an innovative cooling concept for SMD devices (Figure 1). Table 1 gives a summary of the main specifications of the converter under several steady-state and dynamic conditions. The converter's nominal output is 12 V, commonly used in server applications. The stage is operated at a nominal input voltage of 400V, whereas it can maintain regulation down to 360 V at full power (and at the 12 V nominal output voltage), providing enough room for hold-up time whenever the design is part of a full ACDC converter.

Figure 1. Prototype of the 1400 W PSFB DCDC converter.

Table 1. Summary of specifications and test conditions for the 1400 W PSFB SMD

Test	Conditions	Specification
Efficiency	400 V input, 12 V output	η_{pk} >= 97 % at 700 W (50 % load)
Output voltage		12 V
Steady-state V_{out} ripple	400 V input, 12 V output	$\lvert\Delta V_{out}\rvert$ less than 200 mV_{pk-pk}
Undervoltage lockout	375 V on – 350 V off	Analog hysteresis window comparator
Load transient	5 A ↔ 60 A, 1 A/µs	$\lvert\Delta V_{out}\rvert$ less than 600 mV_{pk}
	60 A ↔ 117 A, 1 A/µs	
OCP	118 – 119 A	Shut down and resume
	120 A	Shut down and latch
	Output terminals in short-circuit	Detection within switching period. Shut down and latch

This design consists of a PSFB with synchronous rectification (SR) in center tapped configuration (Figure 2). The control is implemented in an XMC4200 Infineon microcontroller, which includes voltage regulation functionality with peak current mode control, burst mode operation, output over current protection (OCP), over voltage protection (OVP), under voltage protection (UVP), under voltage lockout (UVLO), soft-start, synchronous rectifiers control, adaptive timings (bridge dead times and synchronous rectifiers turn-on and turn-off delays) and serial communication interface. Further detail about the digital control implementation and further functionalities of the PSFB in the XMC™ 4000 family can be found in [2]-[3].

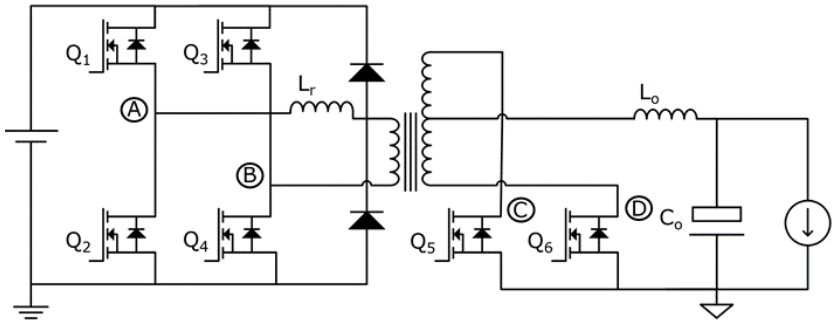

Figure 2. Simplified circuit schematic of the 1400 W PSFB converter.

2. SYSTEM DESCRIPTION

Figure 3 shows the placement of the different components in the 1400 W PSFB prototype. The outer dimensions of the prototype, enclosed in the case, are 133 mm x 64.5 mm x 44 mm which results in a power density in the range of 3.70 W/cm³ (60.78 W/in³).

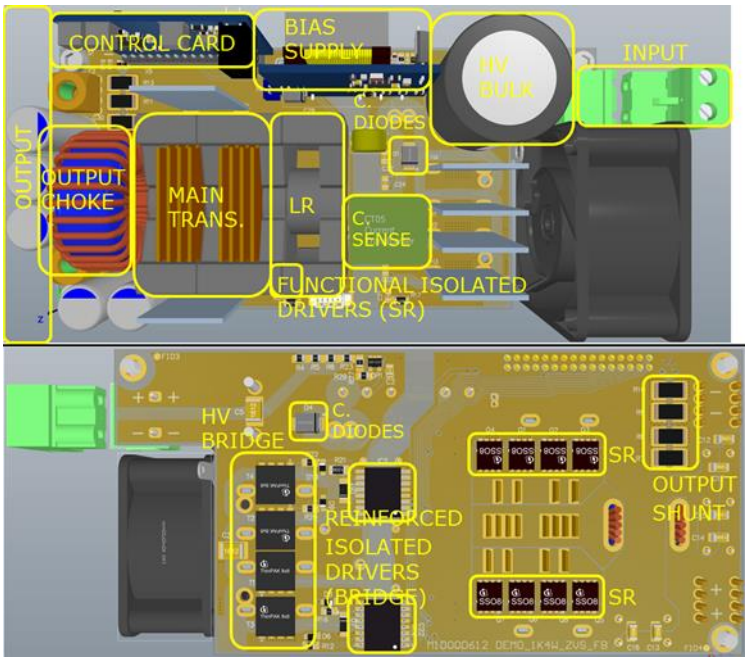

Figure 3. Placement of the different components in the 1400 W PSFB. Current sense (C. SENSE), resonant inductor (LR), synchronous rectifiers (SR), and clamping diodes (C. DIODES).

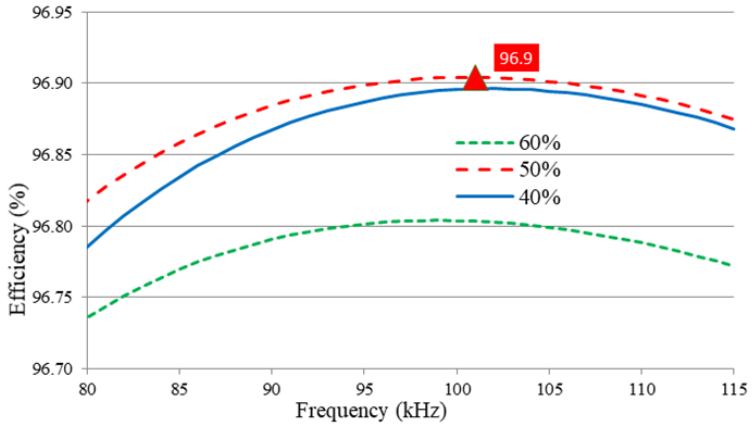

Figure 4. Estimated efficiency of the 1400 W PSFB at different switching frequencies (the fan consumption has been excluded) for the load points of interest. Estimated at 400 V input and 12 V output.

The design was optimized for frequencies in the range of 90 kHz to 110 kHz, as can be seen in the estimated efficiency versus frequency curves for the 40 %, 50 % and 60 % load points in Figure 4. The switching frequency of the converter's prototype is 100 kHz.

The estimated overall distribution of losses of the converter along the load proves the main transformer and the other magnetics as the main sources of loss (Figure 5). The power switches, both the HV primary side full-bridge and the LV synchronous rectifiers exhibit very low and well balanced switching, driving and conduction losses.

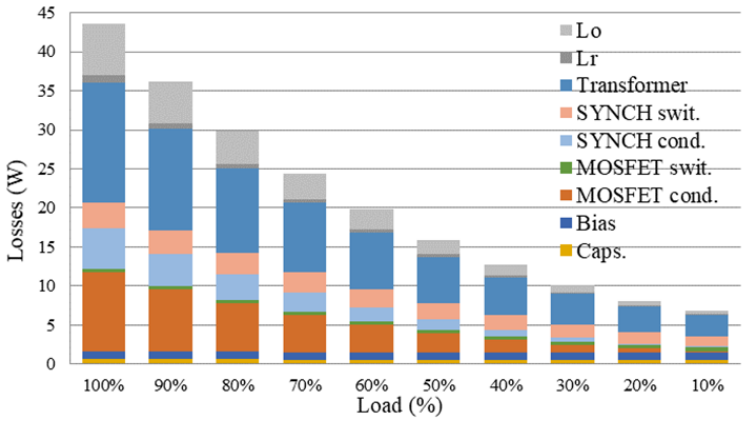

Figure 5. Overall losses breakdown of 1400 W PSFB along the load range. Estimated at nominal conditions: 400 V input and 12 V output.

2.1. PRIMARY SIDE HV DEVICES

The primary side HV switches in the prototype are IPL60R140CFD7 from Infineon. IPL60R140CFD7 stands for 140 mΩ 600 V CoolMOS™ CFD7 in ThinPAK package. CoolMOS™ CFD7 is a SJ MOSFET with a so-called intrinsic fast body-diode, which commonly refers to a device with relatively reduced Q_{rr}. This device has been selected for this design because of its low loss contribution along all load range and its good balance of conduction to switching losses at the 50% load point, becoming the right device and $R_{ds,on}$ when optimizing for high peak efficiency at that point (Figure 6).

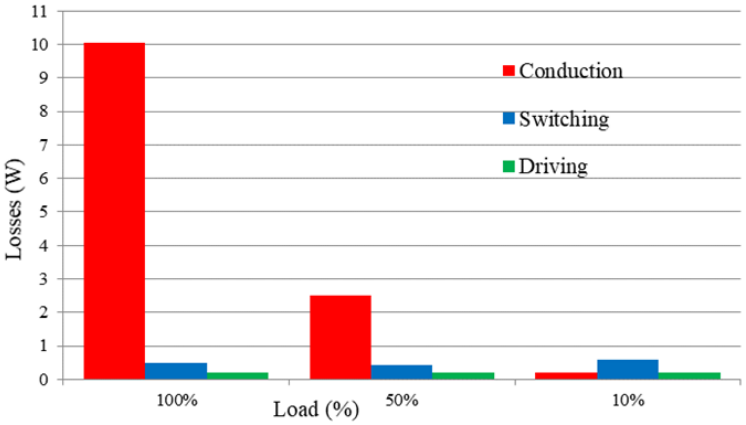

Figure 6. IPL60R140CFD7 loss distribution (percentage of MOSFET contribution) along load in the 1400 W PSFB prototype. Estimated at nominal conditions: 400 V input and 12 V output.

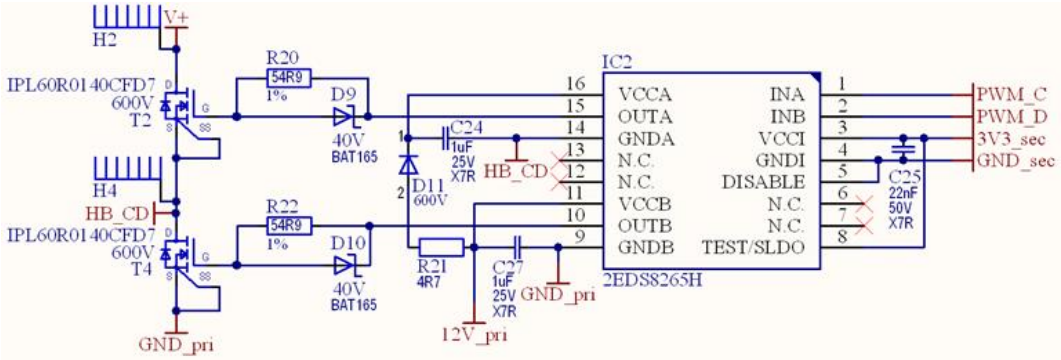

Figure 7. Proposed driving configuration for IPL60R140CFD7 (half-bridge schematic).

The proposed driving circuitry includes a single external resistor (54.9 Ω) in parallel to a medium power Schottky diode (Figure 7). The external turn-on resistor (54.9 Ω) plus the embedded MOSFET gate resistance ($R_{g,int}$) has no impact on the turn-on losses in ZVS and keeps under control *dv/dt* and *di/dt* in the event of a hard-switched turn-on (e.g. during soft-start or no-load operation). The parallel Schottky diode provides a fast and nearly lossless turning-off of the device.

2.1.1. PRIMARY SIDE DEVICES $R_{DS,ON}$

At the time of this work, the available portfolio of CoolMOS™ CFD7 in SMD ThinPAK packages ranges from 225 mΩ to 60 mΩ (Table 2). The $R_{ds,on}$ stated in Table 2 are the maximum $R_{ds,on}$ expected within the production tolerances for the listed devices (at the testing conditions, e.g. 25 °C and 10 V V_{gs}). The maximum $R_{ds,on}$ is the value commonly used during the design of the converter to account for the worst case scenario, specially when it comes to the thermal stability of the converter at the maximum operating temperatures. However, statistically most of the devices actual $R_{ds,on}$ is 10 to 20 mΩ lower.

Table 2. CoolMOS™ CFD7 in ThinPAK $R_{DS,on}$ portfolio.

$R_{DS,on}$ [Ω]	ThinPAK 8x8
225	IPL60R225CFD7
185	IPL60R185CFD7
160	IPL60R160CFD7
140	IPL60R140CFD7
115	IPL60R115CFD7
95	IPL60R095CFD7
75	IPL60R075CFD7
60	IPL60R060CFD7

For this design IPL60R140CFD7 was chosen as the best performance compromise between 100 %, 50 % and 10 % load points. However, other $R_{ds,on}$ could be used for a different distribution of losses whenever there is interest in increasing performance at a different working point of the converter. Figure 8 and Figure 9 represents the comparison of the estimated performance between three different available $R_{ds,on}$ in the CoolMOS™ CFD7 portfolio: IPL60R140CFD7 (device currently in the design), IPL60R160CFD7 (one step higher $R_{ds,on}$) and IPL60R115CFD7 (on step lower $R_{ds,on}$).

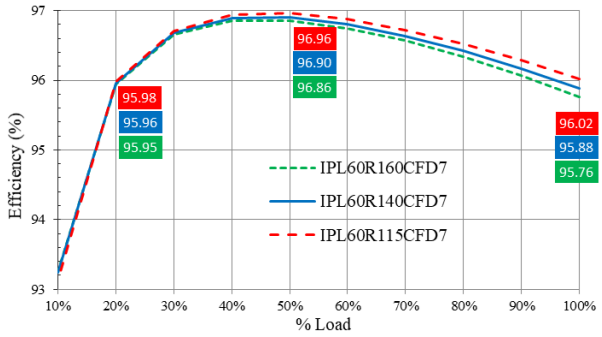

Figure 8. Estimated efficiency of the 1400 W PSFB prototype with different CoolMOS™ CFD7 $R_{DS,on}$ in ThinPAK. Estimated at nominal conditions: 400 V input and 12 V output.

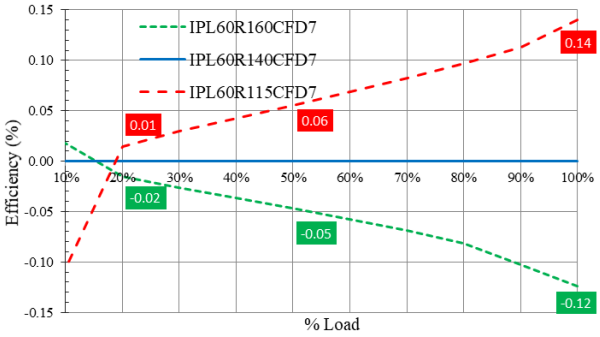

Figure 9. Differential estimated efficiency of the 1400 W PSFB prototype with different CoolMOS™ CFD7 $R_{DS,on}$ in ThinPAK. Estimated at nominal conditions: 400 V input and 12 V output.

Figure 10 represents the estimation of losses at three main working points and how they balance for the three different $R_{ds,on}$ values. Although the difference in losses at 50 % and 10 % is small in comparison to the difference in losses at 100 % the impact in efficiency is still noticeable, as seen in Figure 9. The steep change on differential efficiency comparison between 20 % and 10 % is due to the loss of full ZVS at 10 % and the different Q_{oss} values for each $R_{ds,on}$.

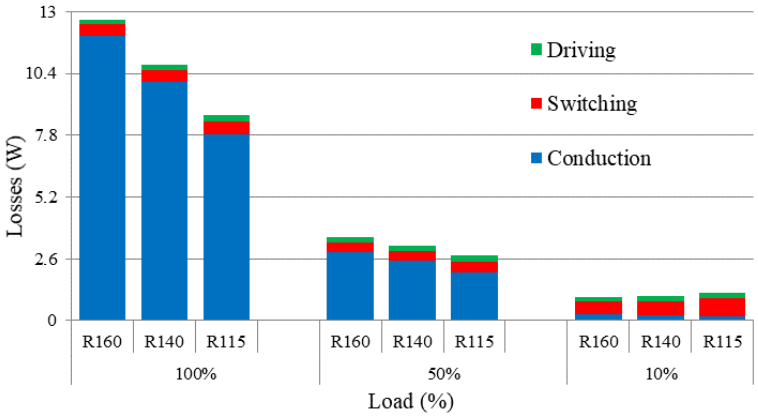

Figure 10. Estimated distribution of the HV switches losses in the 1400 W PSFB prototype with different CoolMOS™ CFD7 $R_{DS,on}$. Estimated at nominal conditions: 400 V input and 12 V output.

2.2. TRANSFORMER

The main transformer has a planar-like construction in a PQ35/28 core made of DMR95 material, which is manufactured by DMEGC. The primary winding has been realized with triple insulated Litz wire made of 7 strands of 0.3 mm diameter each, and manufactured by Furukawa. The secondary winding is made of parallel tinned copper plates of 0.6 mm thickness. Thanks to the core geometry and the winding technique with multiple primary-secondary interlaved sections, the transformer achieves a good coupling (a low leakage inductance, in the order of 500 nH), but still having relatively low intra and inter-winding capacitances (in comparison to a full planar realization). This enables low drain voltage overshoot on the secondary side devices and their optimum voltage class selection [4].

Altough the Litz wire achieves relatively less window utilization than solid round or flat conductors, when properly designed, it minimizes proximity losses (at the switching frequency and at the higher order harmonics, taking into account the spectrum of trapezoidal waveforms characteristics of the PSFB). Meanwhile, the multiple interleaving sections helps to minimize the proximity losses in the secondary side copper plates. A detailed description of the construction can be seen in Figure 11. The main transformer structure actually comprises a transformer with two primary windings in parallel integrated or stacked with the external resonant inductance (Figure 11 and Figure 12). The spacer in between the parallel windings (element 3 in Figure 11) increases the distance to the central gap and helps diminishing losses caused by the fringing fields, especially harmful for the secondary flat copper conductors.

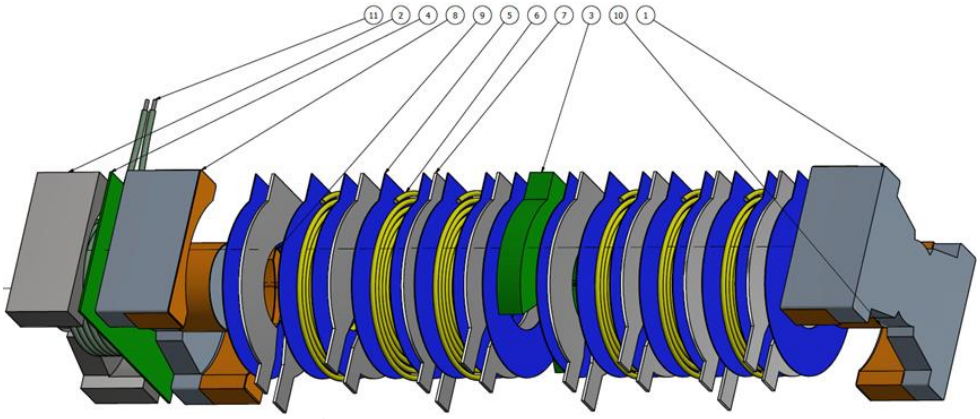

Figure 11. Main transformer and external resonant inductance. Mechanical drawing

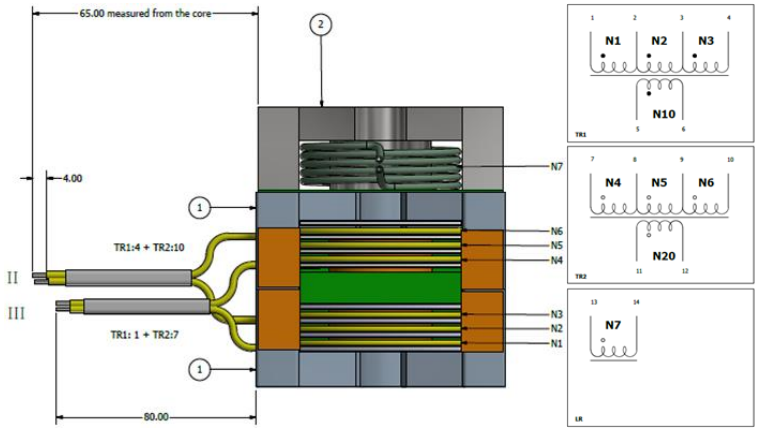

Figure 12. Main transformer and external resonant inductance. Mechanical drawing and simplified schematic.

The transformer has a turn ratio of 21 primary turns to 1 secondary turn, which operates near 63 % effective duty at nominal conditions (400 V input, 12 V output) or 3.15 µs at 100 kHz frequency of switching. Therefore, the calculated maximum flux peak (steady state) is about 0.17 T, well below the saturation flux density of the chosen core material: DMR95 from DMEGC. Figure 13 shows the estimated loss distribution of the full stacked magnetic structure. Notice the transformer core loss is nearly constant along the load (apart from the material temperature dependence) due to the nature of the converter, where the effective duty cycle or the voltage times time integral is nearly fixed for a given voltage conversion ratio (excluded non-idealities of the converter, e.g. ohmic drop).

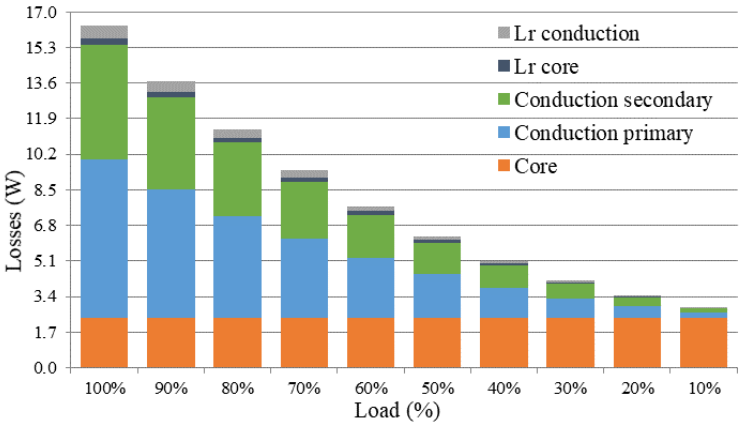

Figure 13. Estimated distribution of losses of stacked magnetic structure: transformer and resonant inductance (L_r). Estimated at nominal conditions: 400 V input and 12 V output.

2.3. COOLING SOLUTION

The proposed cooling solution in this design comprises a set of four copper plates for the HV bridge devices and two copper plates for the synchronous rectification LV devices. The construction of the transformer, where the secondary side winding is built out of copper plates, constitutes as well part of the secondary side LV devices heat-sink (Figure 14).

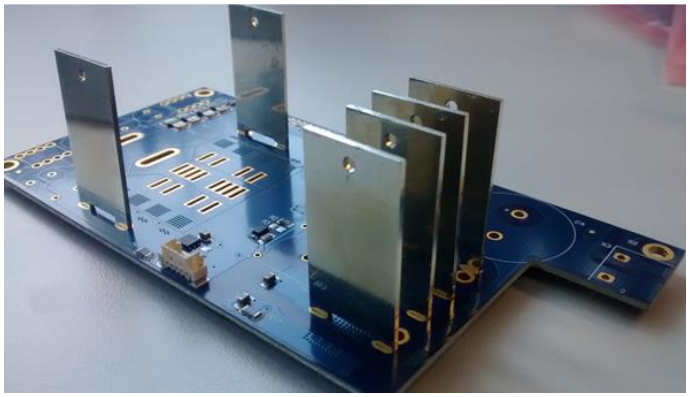

Figure 14. Heat sinks for the HV bridge devices and the LV secondary devices in a partially assembled 1400 W PSFB converter board.

A single fan extracts air from the unit which flows uninterrupted along the HV bridge heatsinks thanks to their construction. That keeps air pressure low and maximizes air flow capability of the fan. The fan speed is modulated along the load for the best overall efficiency (see Figure 15) as little cooling effort is required at light and medium loads. Moreover, the magnetic core losses reach their minimum at medium temperatures (80 °C), therefore keeping the core hot can actually improve the overall efficiency of the converter.

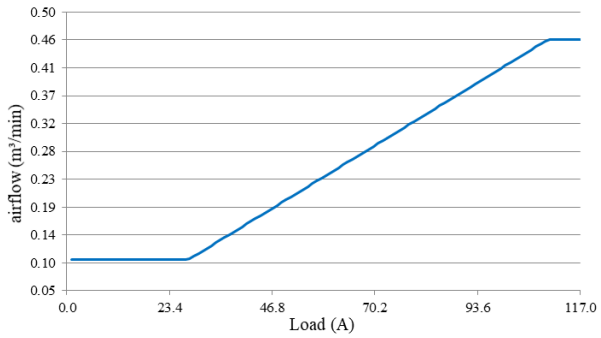

Figure 15. Fan air flow along the converter load (assuming fan is working with low pressure).

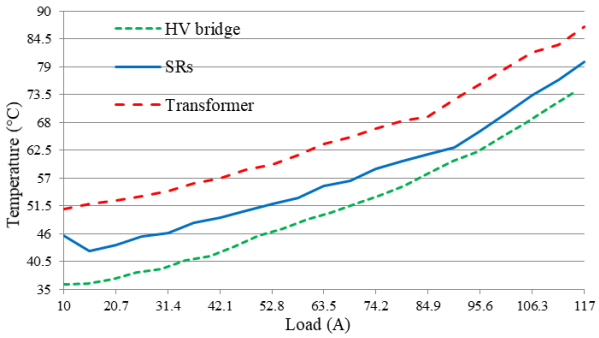

Figure 16. Measured temperatures on 1400 W PSFB converter at 25°C room temperature and within its enclosure.

Based on the estimation of losses for the HV bridge devices (four times IPL60R075CFD7), which at full load is approximately 10.55 W (considering both switching and conduction losses, but not driving, as most of the driving losses are dissipated in the external R_g and the driver), some 2.64 W per device; and the measured temperature (see Figure 16) of approximately 75 °C on the surface of the device packages, we can estimate the thermal impedance of the proposed cooling solution to be in the range of 10 °C/W from junction to air for the HV bridge devices (with the conservative assumption of 50 °C airflow, as the air is heated up by the transformer and the SRs

before reaching the HV bridge heatsinks). This demonstrates that the proposed cooling solution is effective, but of simple manufacture and assembly, and therefore of low cost. This cost saving would enable the use of even lower $R_{ds,on}$ for still a better performance.

3. EXPERIMENTAL

This section demonstrates the performance and experimental results of the 1400 W PSFB DCDC converter prototype. Figure 17 shows the measured efficiency of the converter with and without the fan being supplied by the on-board auxiliary supply, which achieves a peak of 96.71 % and 96.92 % respectively.

For testing of the 1400 W PSFB prototype the suggested setup includes:

- HV supply capable of 400 V and at least 1500 W (when testing up to full load).
- LV electronic load (0 V – 12 V), in constant current mode, capable of at least 1400 W (when testing up to full load)

The nominal input voltage of the converter is 400 V. The converter starts to operate at 375 V, turning-off with a hysteresis window when the input voltage falls below 350 V. The suggested testing setup and the valid input and output ranges are summarized in Figure 18.

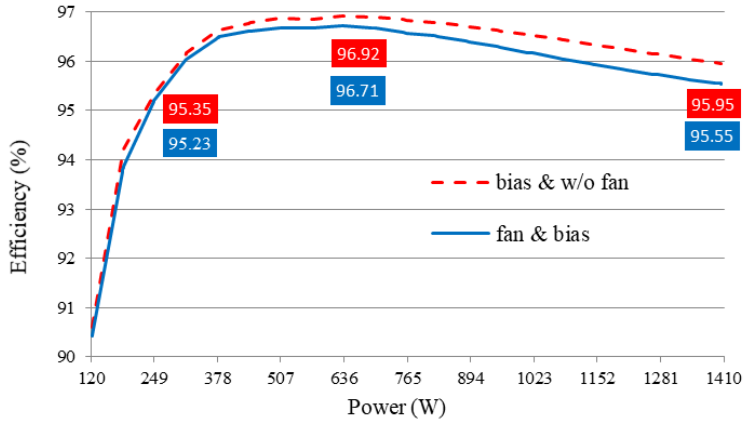

Figure 17. Measured efficiency of the 1400 W PSFB at 400 V input and 12 V output.

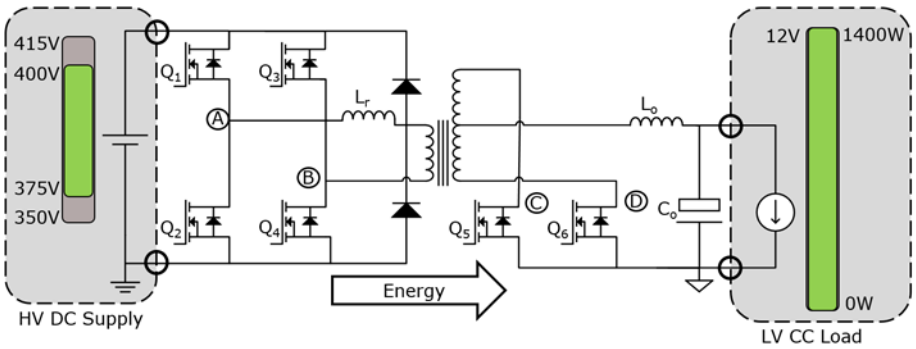

Figure 18. Recommended validation setup.

3.1. DYNAMIC AND STEADY-STATE WAVEFORMS

3.1.1. HALF BRIDGE DRIVER BOOTSTRAP CHARGE SEQUENCE

Driving the HV half bridge device configuration requires the supply of the high side driving stage, generally done with bootstrapping capacitors and a decoupling HV diode from the low side driving supply. However, bootstrapping capacitors are initially discharged and can also self-discharge while the converter is in idle state (e.g. during burst operation mode). The controller should provide a starting sequence that enables the bootstrapping capacitors to be charged up before applying pulses to the high side devices. This could be done in one of several possible ways. Here we apply charging pulses on the low side devices before starting (Figure 19) or before resuming the switching (after a configurable idle time has been detected) (Figure 20).

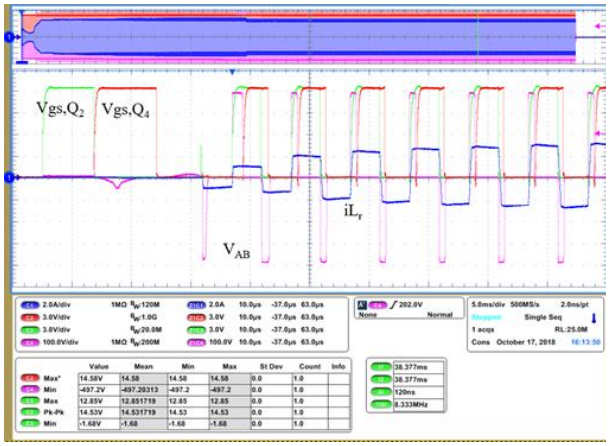

Figure 19. Soft start including a sequence for the charge of the bootstrap capacitors.

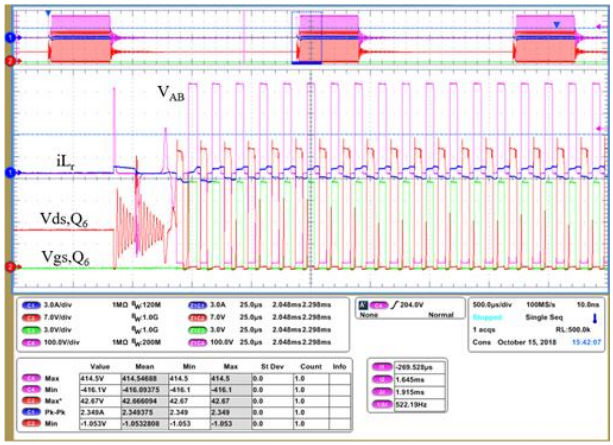

Figure 20. Burst operation including a sequence for the charge of the bootstrapping capacitors.

3.1.2. HV FULL BRIDGE

The low Q_{oss} of IPL60R140CFD7 results in full ZVS of the lagging leg (switches Q_3 and Q_4) down to 15 % load and partial ZVS of the leading leg (switches Q_1 and Q_2) in light load conditions (Figure 21) with full ZVS at 35 % load and above. With partial ZVS only a small part of the Q_{oss} is resistively charged and small part of the E_{oss} is lost, in consequence the switching losses of CFD7 are low at any load conditions and the overall loss contribution along all the load range of the converter is also relatively low (Figure 5 and Figure 6). An additional benefit of the low Q_{oss} and having near ZVS transition at no-load is the lower *dv/dt* values and lower or no drain voltage overshoot of the HV MOSFETs thanks to the smooth quasi-resonant transitions (and consequently better EMI too).

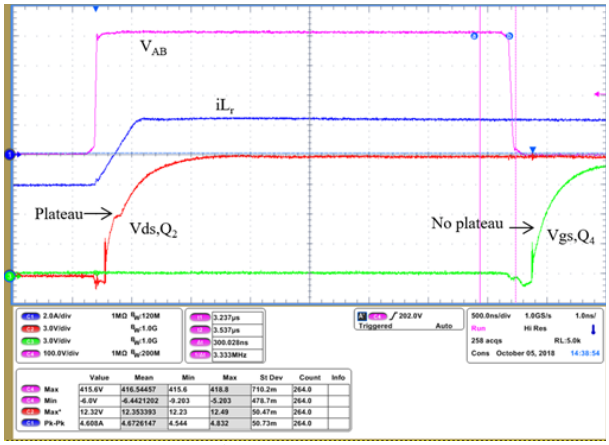

Figure 21. ZVS turn-on of lagging leg (Q_4 switch) and partially hard-switched turn-on of leading leg (Q_2 switch) at 15 % load.

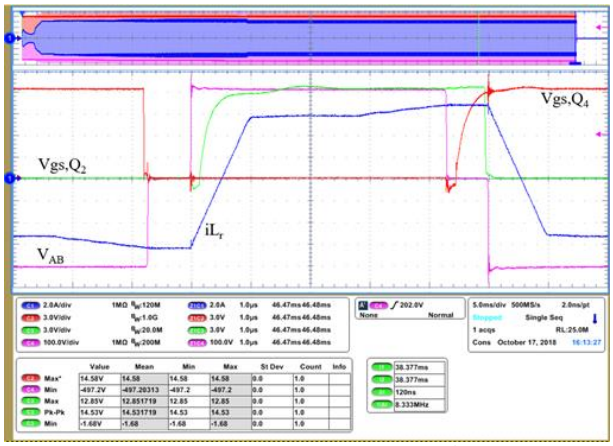

Figure 22. HV bridge drain voltage overshoot at full load. Note: measured with a differential probe Tektronix THDP0200.

The highest drain voltage overshoot in the HV MOSFETs happens at full load (Figure 22), due to relatively high current in the hard-switched turn-off transition; in these transitions the parasitic inductances of the MOSFET package and in the layout induce voltage overshoots due to the high *di/dt*. However, thanks to the low inductances of the SMD packages and the careful layout of the commutation loop, the overshoot is well under the rated maximum blocking voltage in any operating conditions of the converter (under 480 V, or rated 80 % of 600 V, which is the breakdown voltage of the device at T_j = 25 °C).

3.1.3. SYNCHRONOUS RECTIFIERS

The rectifying stage has a center tapped configuration with eight devices 1.6 mΩ 60 V OptiMOS™ 5 in Super SO-8 package in parallel. With eight packages the dissipated power can be better spread bringing higher cooling capability and performance (lower $R_{ds,on}$ increase due to temperature). The center tapped rectifying configuration enables low losses for high output current converters (117 A) but increases the required blocking capability up to two times the reflected transformer secondary voltage (38 V in nominal conditions for this design) plus the additional commutation overshoot. Nevertheless, thanks to the transformer construction (see 2.2), its low leakage, and the optimized output capacitance of OptiMOS™ 5 it is possible to use 60 V voltage class devices with more than enough margin for the maximum drain voltage overshoot (e.g. 41.5 V in Figure 23 for an allowed maximum of 48 V, the rated 80 % of 60 V).

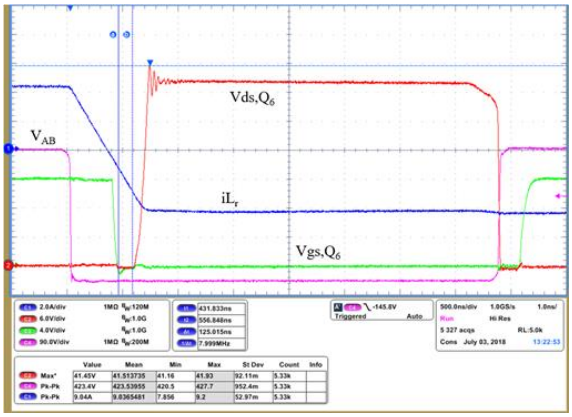

Figure 23. Standard synchronous rectification driving mode. 80 A load

The controller provides adaptive turning-on and turning-off delays of the synchronous rectifiers along the load for a minimum body diode conduction time in order to reduce conduction losses and reduce the generation of reverse recovery charges (Q_{rr}) (in consequence better efficiency and lower drain voltage overshoot).

3.1.4. DYNAMIC RESPONSE

The controller provides hardware implemented peak current control mode with software implemented digital compensation designed for a bandwidth of 18 kHz with a phase margin of 48 degrees and gain margin of 12 dB, well within standard stability criteria requirements. The dynamic response to load jumps (Figure 24) correlates well to the expected response of the designed compensation network, with an overshoot and undershoot within 2.5 % of the nominal output voltage for a 50 % load jump.

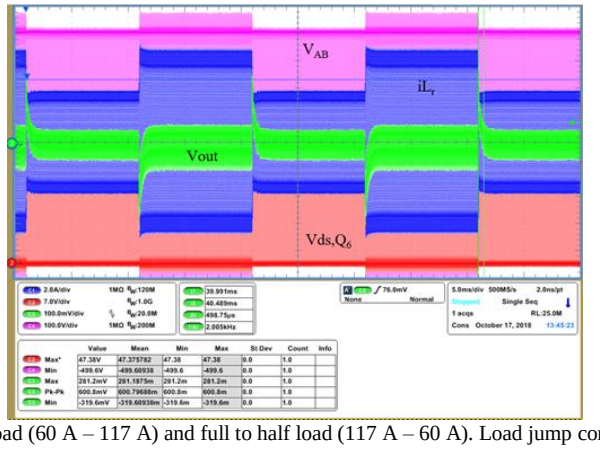

Figure 24. Load jump, half to full load (60 A – 117 A) and full to half load (117 A – 60 A). Load jump configured at 1 A/µs and 10 ms period.

3.1.5. SOFT START-UP

The controller implements a soft start-up sequence to ensure the converter powers up with minimal stress over any of the components. In the starting up sequence the output voltage is ramped up in close loop operation. The controller increments the output voltage reference within a timed sequence (Figure 25).

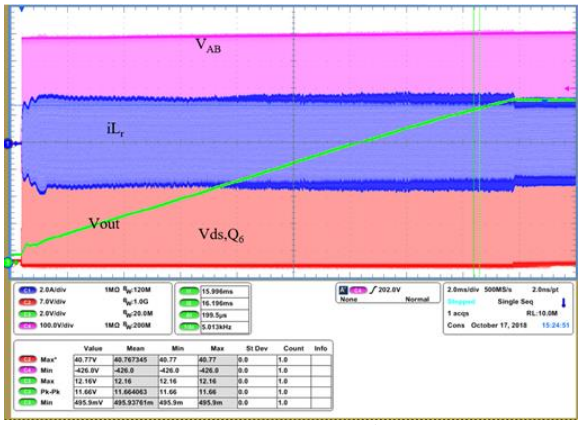

Figure 25. Output voltage soft start up.

3.1.6. BURST MODE OPERATION

For further reduction of power losses under light load conditions (≤ 3 % load) the controller implements burst operation mode. The implemented burst mode ensures that under any condition the HV MOSFETs operate under full or at least partial ZVS (Figure 26), which reduces the power loss and maintains the smooth quasi resonant transitions of the drain voltage (little or no overshoots and better EMI).

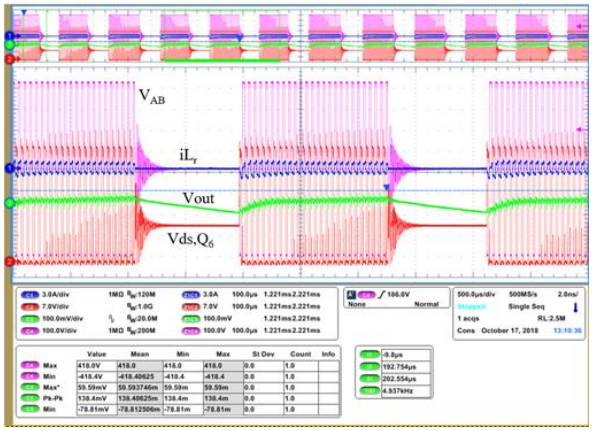

Figure 26. Burst operation mode. Output voltage (green), transformer primary current (blue), bridge voltage (pink), synchronous rectifier drain voltage (red).

3.2. THERMAL MAP

The converter is designed to run enclosed in a case so the fan can provide enough air flow by the channeling effect. However, the thermal captures in Figure 27 and Figure 28 have been taken with the converter running without enclosure for illustrative purposes (the temperature values with the converter enclosed would be lower, see section 2.3).

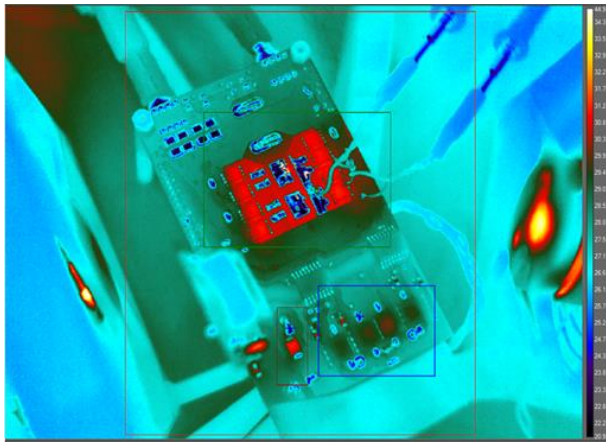

Figure 27. Thermal capture at 15 A load with open case and external auxiliary fans. Bottom view. The hot area correspond to the transformer, which lays on the opposite side of the board.

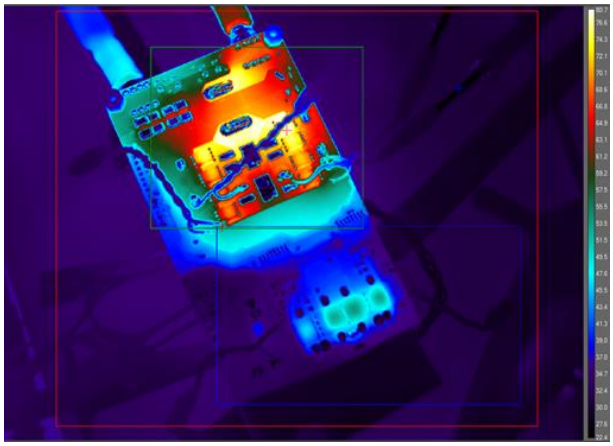

Figure 28. Thermal capture at 117 A load with open case and external auxiliary fans. Bottom view. The hot area corresponds to the synchronous rectifiers and the PCB copper where the output inductor is attached. The temperature of the output inductor spreads to the PCB copper.

4. USER INTERFACE

The controller includes serial communication interface (UART) and a proprietary protocol allowing the parametrization of the HV and the LV MOSFETs timings, output voltage setting, enabling and disabling of some of the protections and monitoring of the status of the converter. The user interface for Windows OS is an example of the capabilities of the included communication library within the controller. The user interface was specially developed to communicate with the controller through XMC™ Link (includes a UART to USB converter) [5] but other serial communication interfaces would be possible.

The communication protocol, the user interface as well and the entire firmware for the control of this and the other DCDC conveters in this work where entirely developed by the author.

Finally, there are two available versions of the GUI:

- Simplified user interface intended for monitoring of the converter during runtime (Figure 29).

- Advanced user interface (Figure 30) with runtime parametrization capabilities of dead times, voltage and current thresholds, enabling and disabling of protections and monitoring of status.

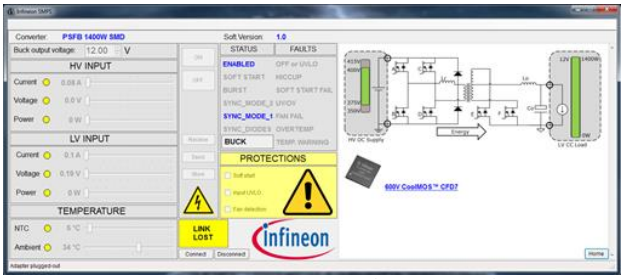

Figure 29. 1400 W PSFB simplified user interface.

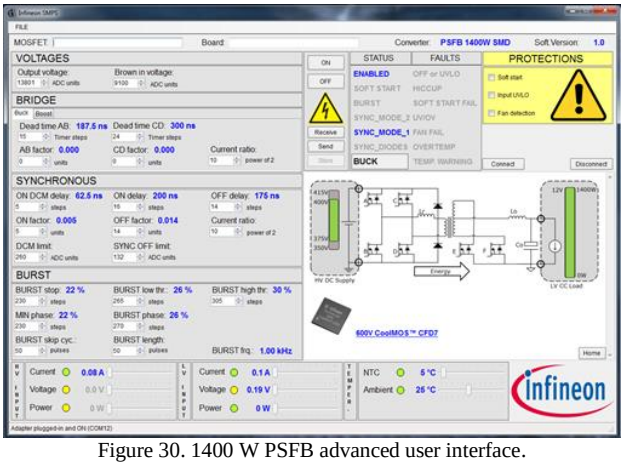

Figure 30. 1400 W PSFB advanced user interface.

5. SCHEMATICS

The converter's hardware is comprised of a main board and two separate daughter cards: a controller card and an auxiliary on-board supply card. Figure 29, Figure 30 and Figure 31 represent the schematics of the main board, the control card and the auxiliary on-board supply respectively.

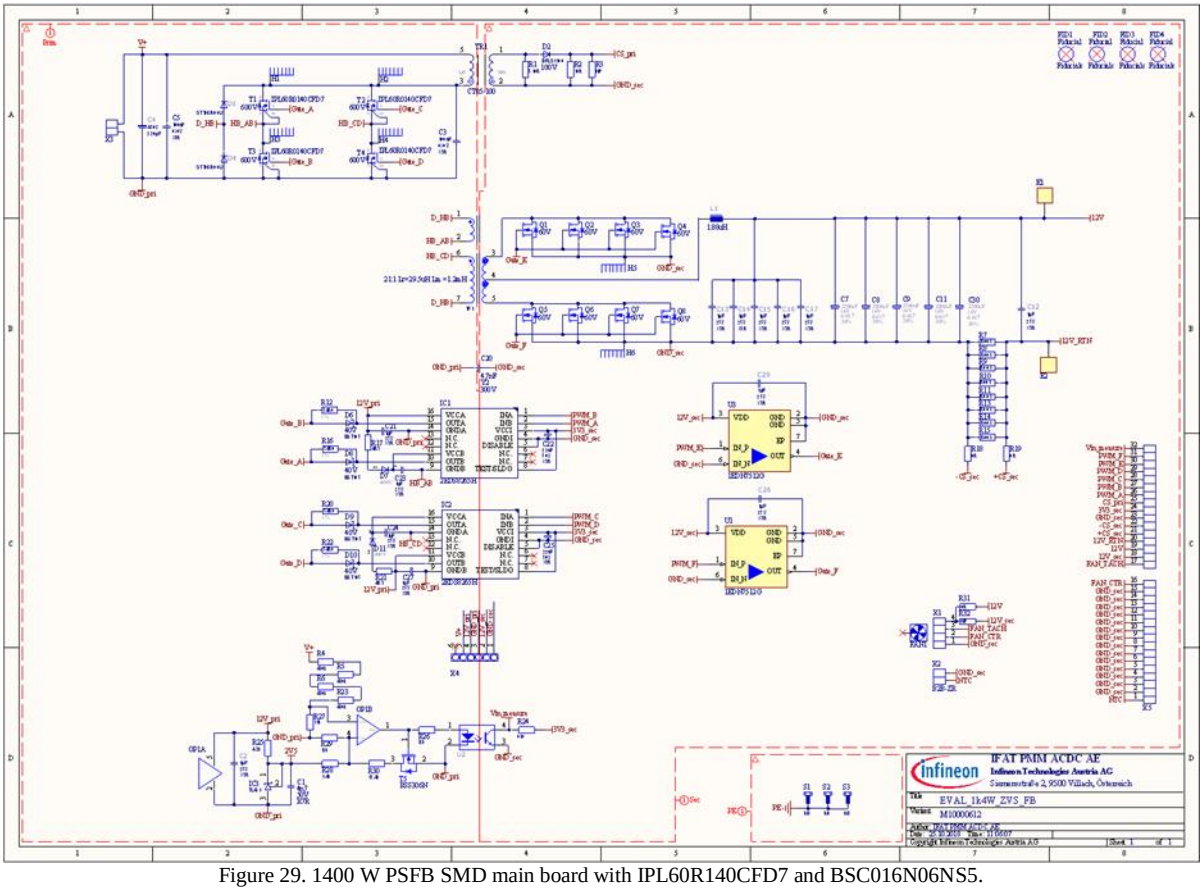

Figure 29. 1400 W PSFB SMD main board with IPL60R140CFD7 and BSC016N06NS5.

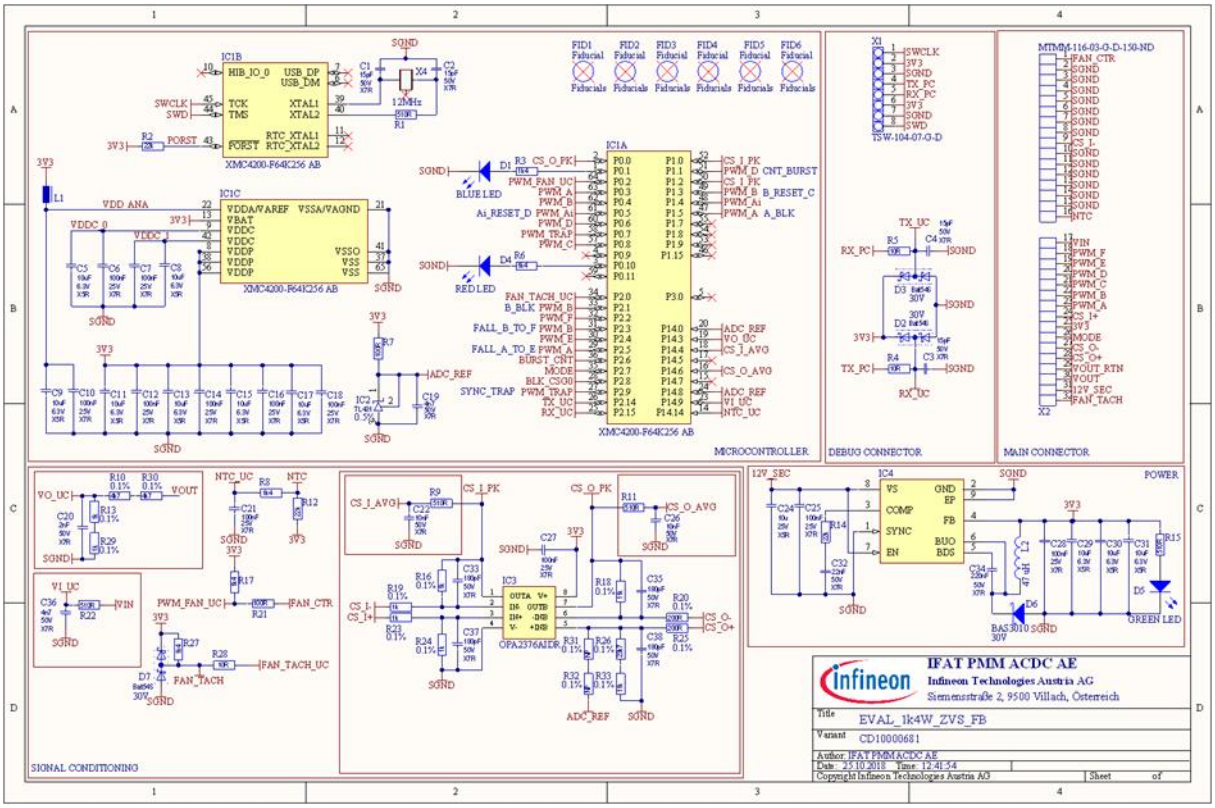

Figure 30. 1400 W PSFB SMD controller card with XMC4200-F64K256AB.

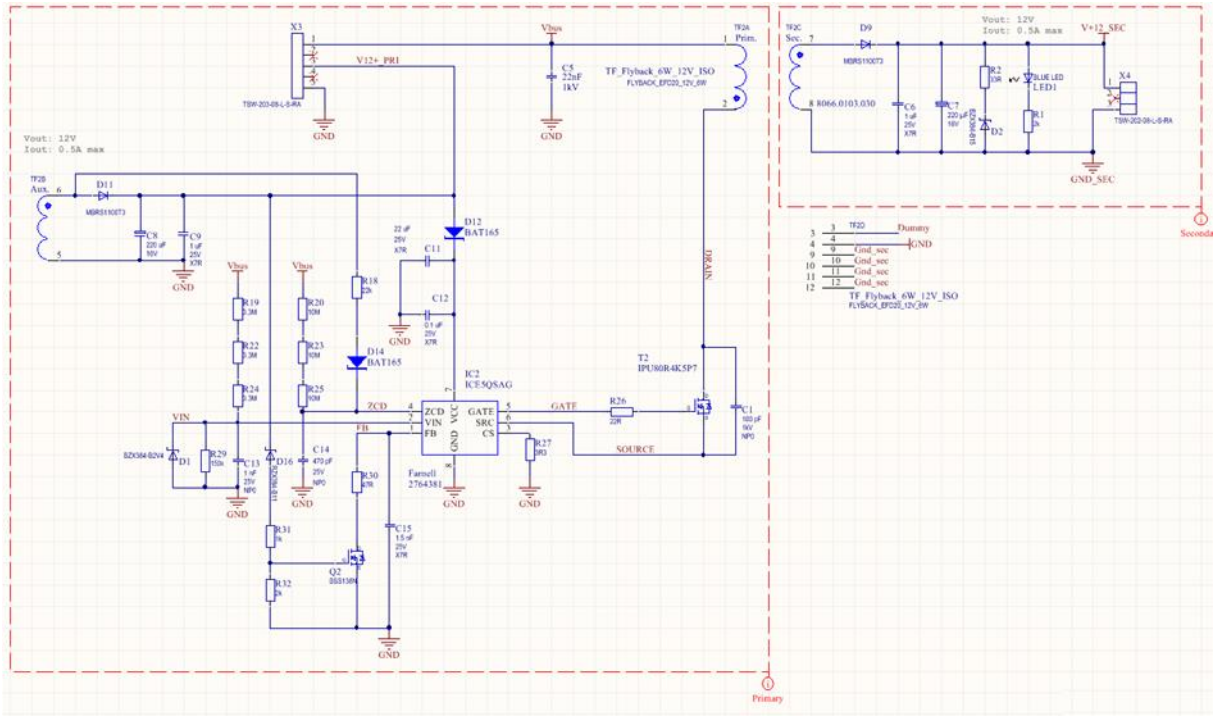

Figure 31. Auxiliary 6W power supply. Adapted from [6].

6. CONCLUSIONS

This chapter has introduced a complete system solution for a 1400 W DCDC converter from 400 V to 12 V achieving 97 % peak efficiency. The achieved power density is in the range of 3.70 W/cm³ (60.78 W/in³), which is enabled by the use of SMD packages, the innovative stacked magnetic construction and the innovative cooling solution.

This DCDC converter proves the feasibility of PSFB topology as a high efficiency topology at the level of fully resonant topologies when combined with the latest SJ MOSFETs devices. This DCDC converter proves as well that digital control, powered by XMC™ Infineon microcontrollers, is not only capable of controlling PSFB topology but also to overcome its drawbacks and enable the usage of the latest SJ MOSFET devices and the lowest possible voltage class devices, both in the HV and in the LV side, to achieve the best possible performance.

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[3] F. Di Domenico, B. Schmoelzer, M. Escudero Rodriguez, S. Raghunath, “1400 W ZVS phase shift full bridge evaluation board. Using 600 V CoolMOS™ CFD7 and digital control by XMC4200”, AN_201711_PL52_003, Infineon Technologies, November 2017

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[6] Jared Huntington, “6 W bias supply. Using the new 800 V CoolMOS™ P7, ICE5QSAG QR flyback controller, and snubberless flyback for improved auxiliary power-supply efficiency and form factor”. AN_201709_PL52_030, Infineon Technologies, November 2017

CHAPTER 4. BIDIRECTIONAL 3300 W PSFB

1. INTRODUCTION

The prototype of 3300 W PSFB in this chapter is an example of how the improvement in semiconductor technology and control algorithms allow a simple and well known topology block like the PSFB to reach the high efficiency levels traditionally considered out of reach for this topology. Furthermore, for the construction of a bidirectional DCDC stage, an LLC or a Dual Active Bridge topology would be the most common approach [1]. It is demonstrated in this chapter that, thanks to the flexibility of digital control, the traditional PSFB topology block can be used as a bidirectional DCDC converter without changes on what would be otherwise a standard PSFB design (Figure 1).

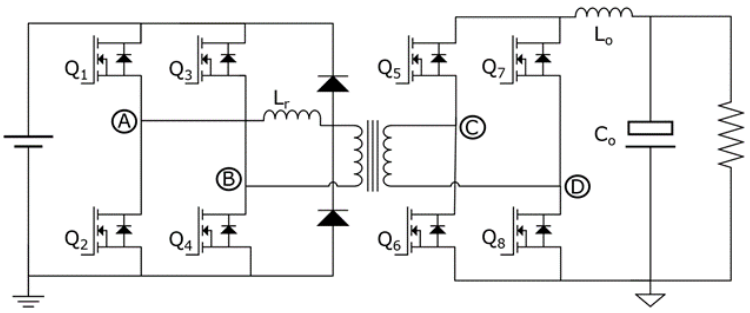

Figure 1. Simplified schematic of the 3300 W PSFB prototype.

This 3300 W PSFB DCDC converter design consists of a PSFB with synchronous rectification (SR) in full bridge configuration (Figure 1). The converter's nominal output is 54.5 V (common for telecom applications) or that of a 48 V battery charger with a working range between 60V to 40V. The stage is operated at a nominal input voltage of 400V, whereas it can regulate down to 360V at full load (at 54.5 V nominal output voltage), providing room for hold-up time whenever the design is part of a full ACDC converter. A summary of the most significant specifications can be found in Table 1.

Table 1. Summary of specifications and test conditions for the 3300 W bidirectional PSFB

Test	Conditions	Specification
Input voltage	350 V – 415 V	400 V nominal
Efficiency test	380V input, 54.5V output	η_{pk} >= 98 % at 1500 W (50 % load)
Output voltage	60V-40V	54.5 V nominal
Steady-state V_{out} ripple	380V input, 54.5V output	$\lvert\Delta V_{out}\rvert$ less than 200 mV_{pk-pk}
Brown-out		370 V on – 350 V off 415V off – 390 V on
Load transient	5 A ↔ 31 A, 0.5 A/µs	$\lvert\Delta V_{out}\rvert$ less than 450 mV_{pk}
	31 A ↔ 61 A, 0.5 A/µs	
OCP	5 min at 77A-83 A	Shut down and resume after 5 min
	1 ms at 83-85 A	
	20 µs at 85 A	Shut down and latch
	Output terminals in short-circuit	Detection within switching cycle. Shut down and latch

The control is implemented in an XMC4200 microcontroller from Infineon, including voltage regulation functionality with peak current mode control, burst mode operation, output over current protection (OCP), over voltage protection (OVP), soft-start, synchronous rectifiers control, adaptive timings (HV bridge dead times and synchronous rectifiers turn-on and turn-off delays) and serial communication interface. Further details about the digital control implementation and further functionalities of PSFB in the XMC™ 4000 family can be found in [2]-[3].

The 3300 W PSFB bidirectional DCDC converter introduced in this chapter (Figure 2) achieves 98% efficiency in buck mode and 97% in boost mode. The following sections describe the converter prototype, the innovative cooling concept for SMD devices and the novel integrated magnetic structure. Finally the experimental results are discussed.

Figure 2. 3300 W bidirectional PSFB prototype.

2. SYSTEM DESCRIPTION

The 3300 W bidirectional PSFB can operate as an isolated buck or as an isolated boost converter, i.e. with the power flowing from the HV rail to the isolated LV rail or vice-versa. The measured efficiency of the converter is plotted in Figure 3.

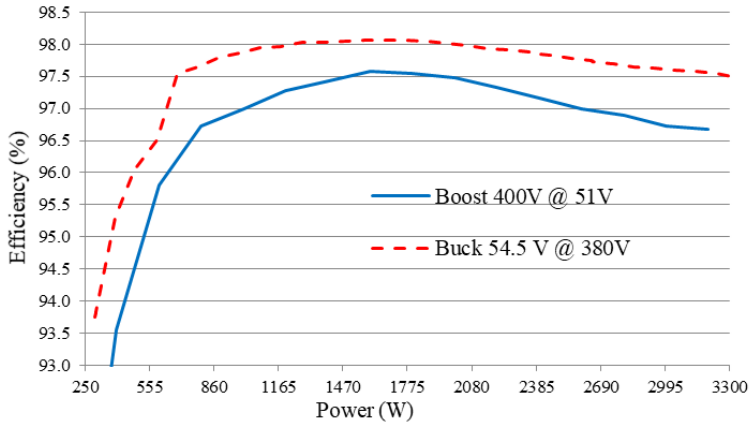

Figure 3. Measured efficiency of bidirectional 3300 W PSFB (fan consumption included).

Figure 4 shows the placement of the different components in the 3300 W bidirectional PSFB. The outer dimensions of the board, enclosed in the case, are 208 mm x 83 mm x 44 mm. Therefore, thanks to the high performance of the semiconductor devices, the innovative cooling concept for a full SMD solution and the stacked magnetic construction the converter achieves a power density in the range of 4.34 W/cm³ (71.19 W/in³).

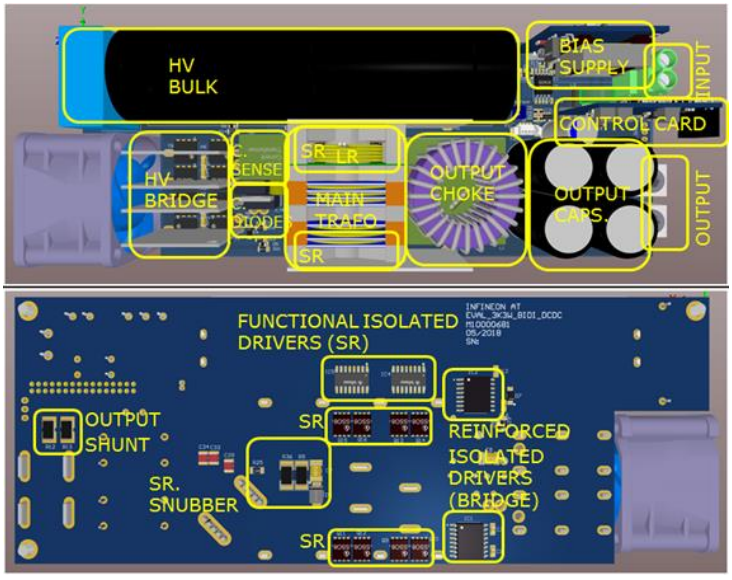

Figure 4. Placement of the different sections in the 3300 W bidirectional PSFB. High voltage (HV), synchronous rectifiers (SR), current sense (C.SENSE), clamping diodes (C. DIODES), resonant inductance (LR), transformer (TRAFO) and capacitors (CAPS).

The power density surpasses that of the prototype in Chapter 3, which was 3.70 W/cm³ (60.78 W/in³). However, both converters are not directly comparable due to their different specifications. At higher output voltages higher efficiencies can be achieved (54.5 V instead of 12 V). The higher efficiency, together with the higher power of the converter (3300 W instead of 1400 W) enables a higher power density, although not necessarily a smaller volume (this converter is overall twice as big).

The design was optimized for frequencies in the range of 110 kHz – 90 kHz, as can be observed in the plot of the estimated efficiency versus frequency curves for the 40 %, 50 % and 60 % load points in Figure 5. The switching frequency of the converter's prototype is 100 kHz

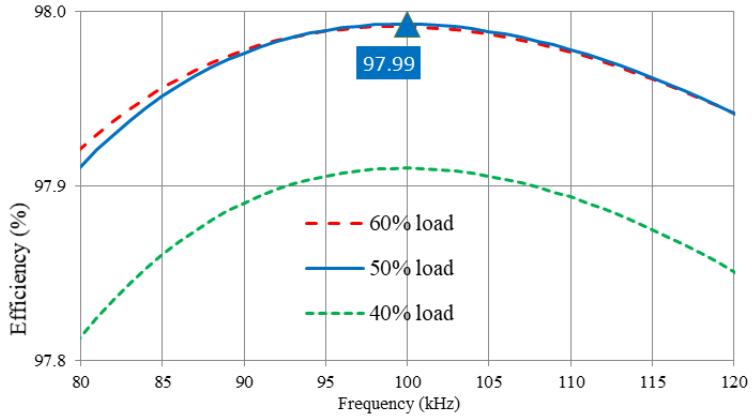

Figure 5. Estimated efficiency of 3300 W bidirectional PSFB in buck mode at different switching frequencies (the fan consumption is included) for the load points of interest.

2.1. OVERALL LOSSES DISTRIBUTION

The estimated overall distribution of losses of the converter along load proves the transformer and other magnetics as the main sources of loss (Figure 6). The main semiconductors, both 600V CoolMOS™ CFD7 and 150 V OptiMOS™ 5 exhibit a good balance of switching to conduction loss.

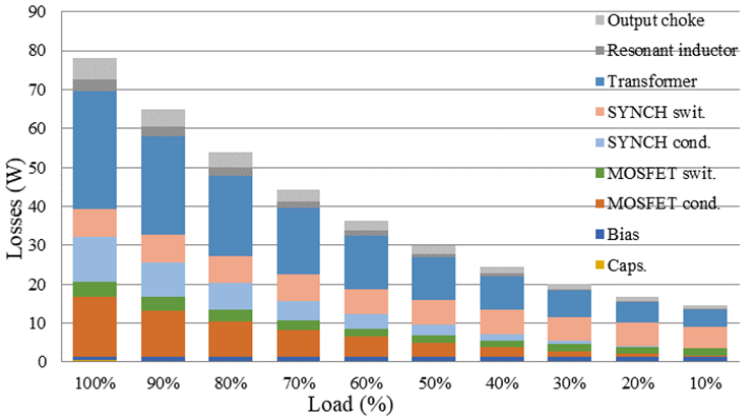

Figure 6. Overall losses breakdown of 3300 W bidirectional PSFB in buck mode along load.

2.2. PRIMARY SIDE HV DEVICES

IPL60R075CFD7 stands for 75 mΩ 600 V CoolMOS™ CFD7 in ThinPaK package, which is a SJ MOSFET with fast body-diode device from Infineon. IPL60R075CFD7 brings a low loss contribution along all load range and exhibits a good balance of conduction to switching losses at the 50% load point, becoming the right device and $R_{ds,on}$ class when optimizing for high peak efficiency at that point (Figure 7).

For a better distribution of power losses and improved cooling performance of the SMD devices, every position of the HV bridge is composed of two devices in parallel (Figure 8). This configuration brings the benefit of effectively having half the nominal $R_{ds,on}$ plus the additional benefit of the devices running at a lower temperature (consequently with lower $R_{ds,on}$ increase due to temperature).

The driving circuitry includes a single external resistor for each pair of devices, thanks to IPL60R075CFD7 already including an embedded gate resistor $R_{g,int}$ (5.9 Ω) big enough for a safe parallel operation in this application.

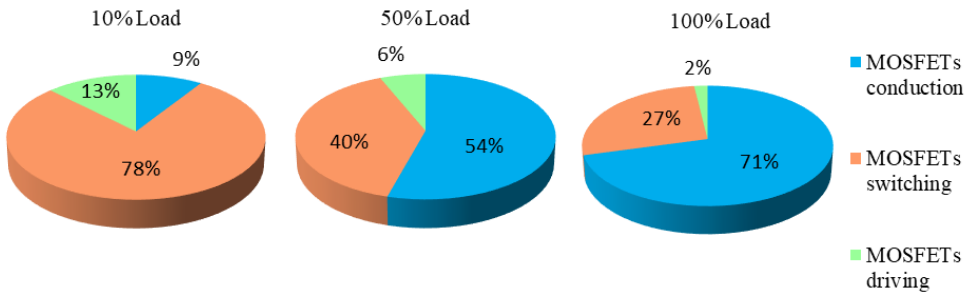

Figure 7. IPL60R075CFD7 estimated loss distribution (percentage of the MOSFET contributions) along load in the 3300 W bidirectional PSFB operating in buck mode.

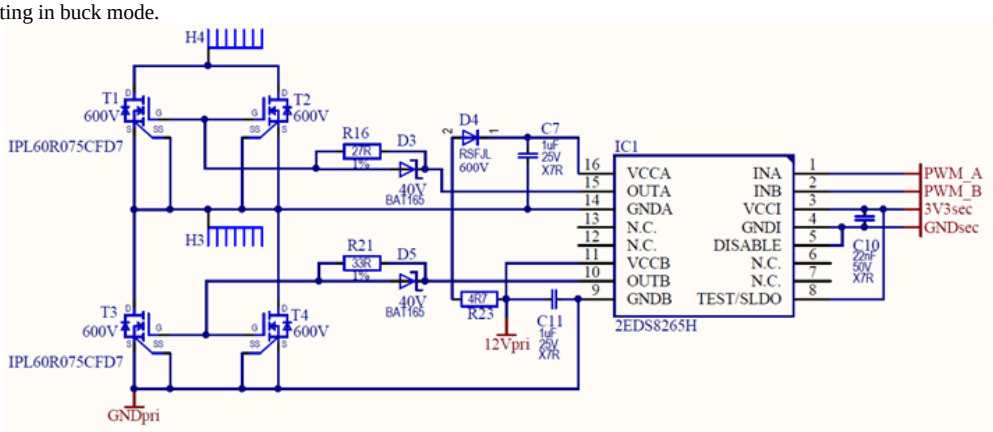

Figure 8. Driving configuration of paralleled IPL60R075CFD7 (half bridge schematic).

2.1.1. PRIMARY SIDE DEVICES $R_{DS,ON}$

At the time of this work, CoolMOS™ CFD7 portfolio in SMD ThinPAK packages (Table 2) ranges from 225 mΩ (maximum $R_{ds,on}$) to 60 mΩ (maximum $R_{ds,on}$). For this design it was chosen IPL60R075CFD7 as the best compromise between the 100%, 50% and 10% load points performances. However, other $R_{ds,on}$ could be used for a different distribution of losses whenever there is interest in increasing performance at other working points of the converter.

Table 2. CoolMOS™ CFD7 in ThinPAK $R_{DS,on}$ portfolio

$R_{DS,on}$ [Ω]	Device naming
225	IPL60R225CFD7
185	IPL60R185CFD7
160	IPL60R160CFD7
140	IPL60R140CFD7
115	IPL60R115CFD7
95	IPL60R095CFD7
75	IPL60R075CFD7
60	IPL60R060CFD7

Figure 9 and Figure 10 represent the estimated performance of three different $R_{ds,on}$ available in the portfolio: IPL60R075CFD7 (device currently on the design), IPL60R095CFD7 (one step higher $R_{ds,on}$) and IPL60R060CFD7 (on step lower $R_{ds,on}$).

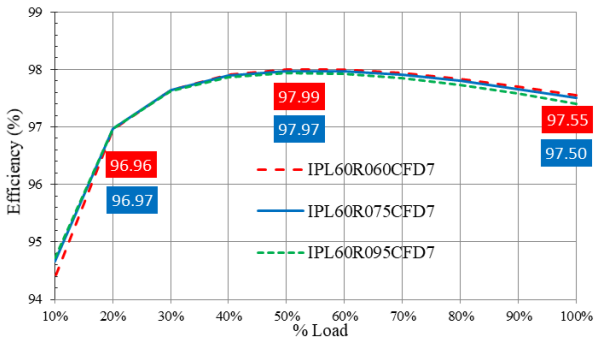

Figure 9. Estimated efficiency of 3300 W bidirectional PSFB in buck mode with different CoolMOS™ CFD7 $R_{DS,on}$ in ThinPAK.

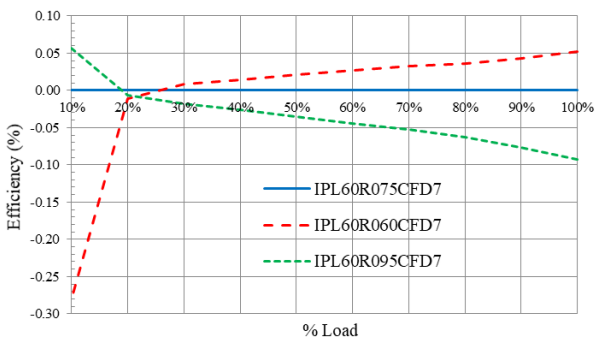

Figure 10. Differential estimated efficiency of 3300 W bidirectional PSFB in buck mode with different CoolMOS™ CFD7 $R_{DS,on}$ in ThinPAK.

Figure 11 represent the estimated losses at the three main working points of interest and how they balance for the different $R_{ds,on}$. Although the difference in losses at 50 % and 10 % is small in comparison to the difference in losses at 100 % the impact in efficiency is still noticeable as seen in Figure 10.

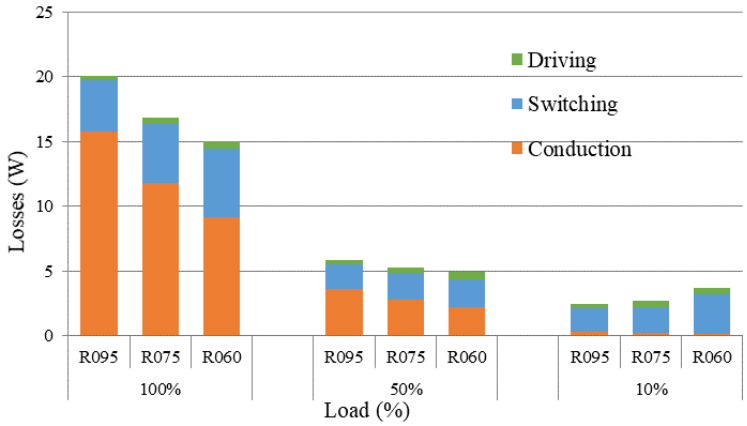

Figure 11. Estimated distribution of losses of 3300 W bidirectional PSFB in buck mode with different CoolMOS™ CFD7 $R_{DS,on}$ in Thin-PAK.

2.3. TRANSFORMER

The transformer has a planar like construction in a PQI35/23 core made of DMR95 material, which is manufactured by DMGC. The primary winding has been realized with triple insulated Litz wire of 7 strands of 0.3 mm diameter each, produced by Furukawa. The secondary winding is made of parallel tinned copper plates of 0.6 mm thickness. Thanks to the winding technique and the geometry of the core, the transformer achieves a good coupling (with low leakage, in the order of 500 nH), but still with relatively low intra and inter-winding capacitances (in comparison to a full planar realization). Moreover, the Litz wire and the interleaving of the primary and the secondary windings minimizes the proximity losses (at the main switching frequency and at the higher order harmonics, taking into account the spectrum of the PSFB trapezoidal waveforms).

Figure 12 shows a two-dimensional Finite Element simulation of the current distribution in the transformer windings. It can be observed the increment in the current density near the gaps due to the fringing fields, therefore the convenience of keeping the gaps as small as possible or alternatively increasing the distance of the conductors to the gap (that was the approach for the transformer in Chapter 3). The simulation has been realized in FEMM 4.2, a suite of programs for solving low frequency electromagnetic problems on two-dimensional planar and axisymmetric domains [4].

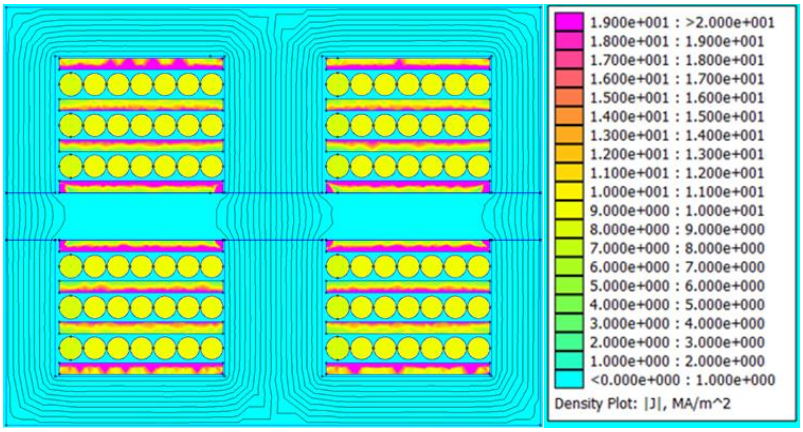

Figure 12. Main transformer current density distribution. Finite element simulation (FEMM 4.2).

The main transformer has a turn ratio of 21 primary to 4 secondary turns. Therefore, the effective duty at nominal conditions (400 V input to 54.5 V output) is 71.7 % or 3.59 µs at the switching frequency of 100 kHz. Therefore, the maximum flux peak (in steady state) is about 0.19 T, well below the saturation flux density of the chosen core material: DMR95 from DMEGC.

The main transformer actually comprises two parallel transformers integrated in the same structure. Due to the integration the flux is cancelled in part of the core with the subsequent reduction of the core losses in that part of the volume (Figure 13). Thanks to the paralleling of the two transformers it is possible to realize an equivalent smaller magnetizing inductance (the equivalent of two magnetizing inductances in parallel) with two smaller gaps, instead of a bigger single one, and therefore less losses caused by the fringing fields near it.

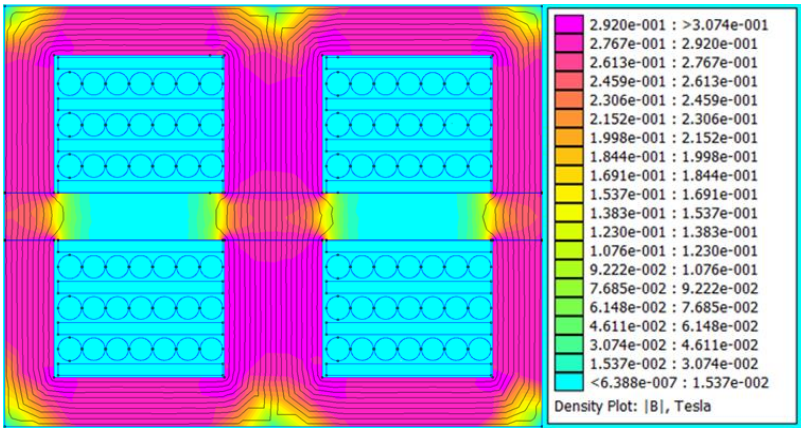

Figure 13. Main transformer flux density distribution. Finite element simulation (FEMM 4.2).

Figure 14 shows an estimated loss distribution of the full stacked magnetic structure. Notice the transformer core loss is nearly constant along the load (apart from the material temperature dependence) due to the nature of the converter, where the effective duty or the voltage times time integral is nearly fixed for a specific voltage conversion ratio.

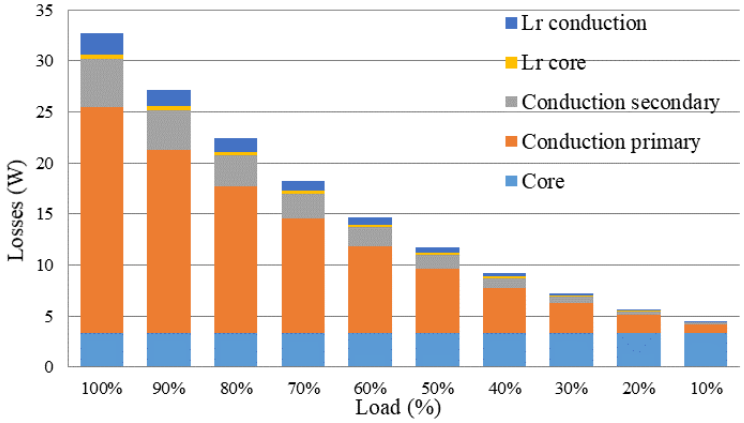

Figure 14. Estimated distribution of losses of stacked magnetic structure: transformer and resonant inductance.

2.4. COOLING SOLUTION

The proposed cooling solution for the full SMD design comprises a set of four copper plates for the HV bridge devices and two copper plates for the synchronous rectification LV devices. The construction of the transformer, where the secondary side winding is built out of copper plates, constitutes as well part of the secondary side LV devices heat sink (Figure 15).

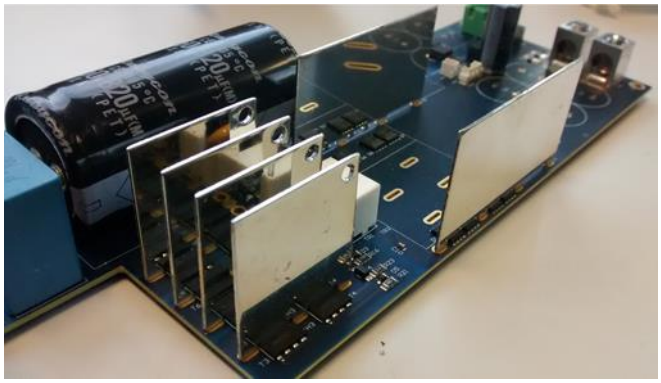

Figure 15. Heat sinks for HV bridge devices and LV secondary devices in a partially assembled PSFB 3300 W converter board.

A single fan extracts air from the unit, which flows uninterrupted along the HV bridge heatsinks thanks to their construction. That keeps the air pressure low and maximizes the air flow capabilities of the fan. The fan speed is modulated along the load for the best overall efficiency (see Figure 16), because little cooling effort is required at light loads. Moreover, the core losses for the DMR95 material diminish with temperature, reaching its minimum at around 80 °C, therefore the overall efficiency of the converter can improve at light and medium loads when the core is warm.

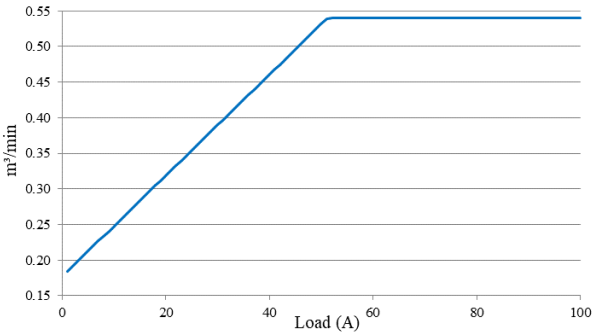

Figure 16. Estimated air flow along the converter load range (assuming fan is working with low pressure).

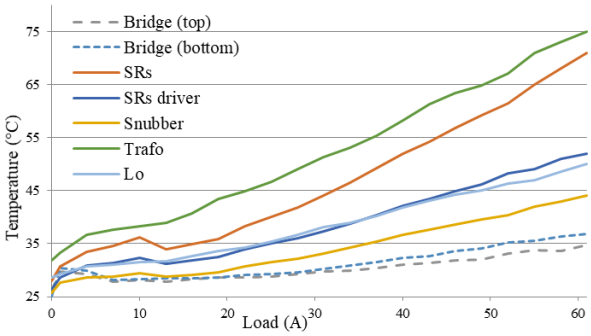

Figure 17. Measured temperatures in the PSFB 3300 W converter at 25°C room temperature and with open case.

Based on the estimation of losses for the HV bridge devices (eight IPL60R075CFD7), which at full load is approximately 16.4 W (considering both switching and conduction losses, but not driving, as most of the driving losses are dissipated on the external gate resistor R_g and in the gate driver), some 2.05 W per device, and the measured temperature of approximately 35 °C on the surface of the device packages (see Figure 17), we can estimate the thermal impedance of the proposed cooling solution in the range of 5.5 °C/W from junction to air for the HV bridge devices. Therefore, the proposed cooling solution demonstrates to be effective, of simple manufacture and assembly and consequently of low cost.

2.5. CONSTANT POWER LIMITATION

The controller includes a constant power limitation curve (Figure 18), that decreases the output voltage when the output current goes above the nominal 61 A, to maintain the maximum 3300 W output power constant. Up to 73 A and 45 V output the converter can operate steadily. If the current increases further, up to 83 A and down to 40 V output, the converter would operate up to 5 minutes before shutting down as a thermal protection. The converter will resume to a normal state after an additional 5 minutes idle time. At a hard limit of 85 A output, the converter will shut down and latch (considered as a short circuit).

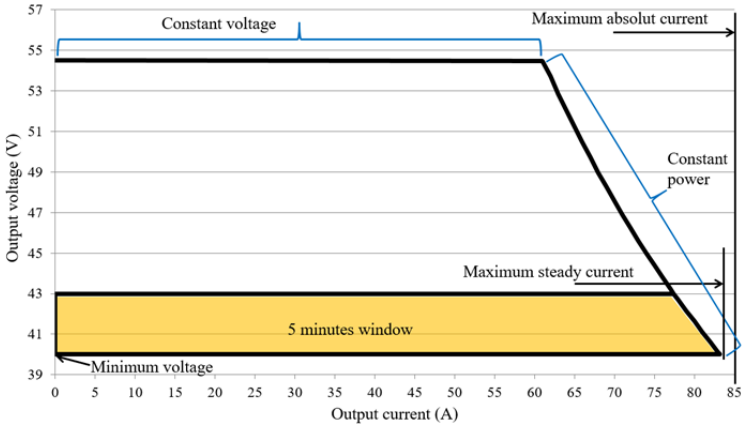

Figure 18. Constant voltage, constant power curves.

3. EXPERIMENTAL

This section demonstrate the performance and experimental results of the 3300 W bidirectional PSFB under several steady-state and dynamic conditions.

3.1. BUCK MODE TESTING SETUP

For validation of the buck mode the suggested setup includes:

- HV supply capable of 400 V and at least 3400 W (when testing up to full load).
- LV electronic load (0 V – 60 V), in constant current mode, capable of at least 3300 W (when testing up to full load)

The nominal input voltage of the converter is 400 V. The converter starts to operate at 375 V, and shuts down with a hysteresis window when the input voltage rises above 415 V or falls below 350 V. The suggested testing setup and the input voltage range is summarized in Figure 19.

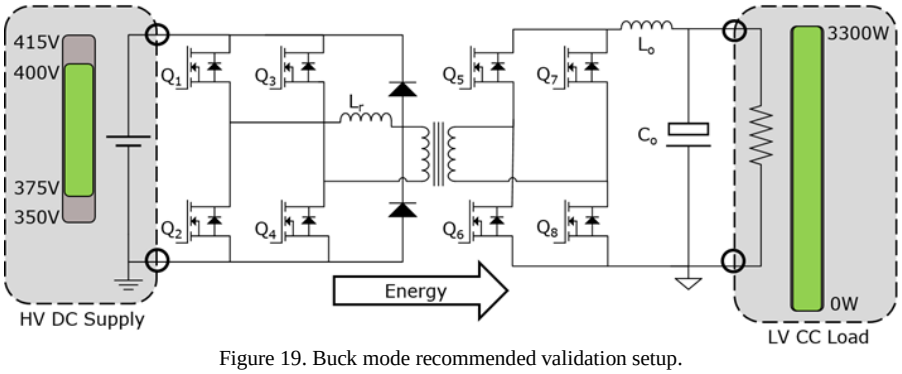

Figure 19. Buck mode recommended validation setup.

3.2. BOOST MODE TESTING SETUP

For validation of the boost mode the suggested setup includes:

- HV supply capable of 330 V – 380 V and at least 1 A (for the pre-charging of the bulk capacitor).
- HV electronic load (0 V – 400 V), in constant current mode, capable of at least 2400 W (when testing up to full load)
- LV supply capable of 0 V – 58 V and at least 2500 W (when testing up to full load)

A HV diode might be placed between the HV supply and the HV load as indicated in Figure 20 to decouple the HV supply once the 3300 W PSFB converter starts-up. The converter requires both the HV and the LV side voltages to be within the ranges indicated in Figure 20 for starting-up, while the sequence of the applied voltages is irrelevant.

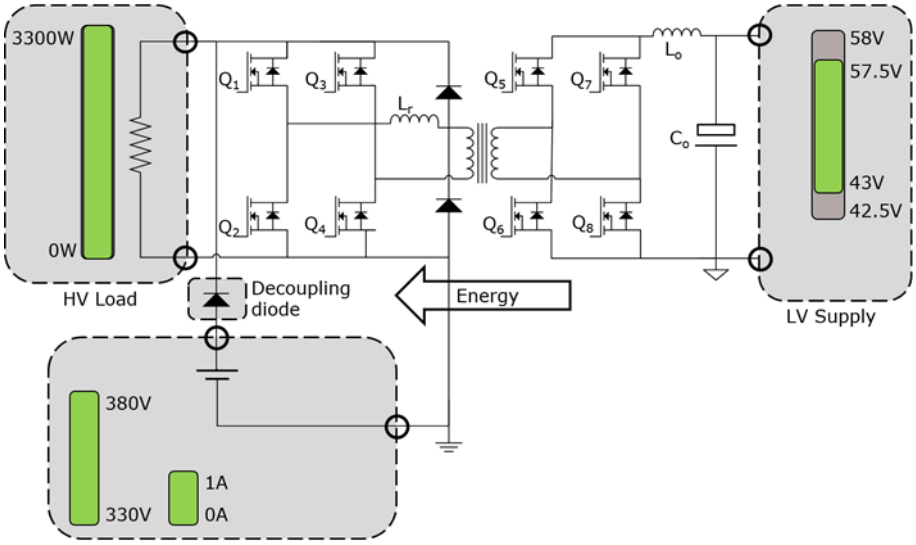

Figure 20. Boost mode recommended validation setup.

The buck and boost validation setups could be combined within a single setup with an additional diode decoupling the LV supply. However, when doing so, all the current in any of the directions of flow would be passing through one of the decoupling diodes, which may require of additional suited cooling for those external auxiliary devices.

3.3. BUCK MODE EXPERIMENTAL RESULTS

3.3.1. PRIMARY SIDE HV FULL BRIDGE

The relatively low Q_{oss} of IPL60R075CFD7 results in full ZVS of the lagging leg (switches Q_3 and Q_4) down to no load and partial ZVS of the leading leg (switches Q_1 and Q_2) in light load conditions (Figure 21) with full ZVS at 20 % load and above. With partial ZVS only a small part of the Q_{oss} is resistively charged and only a small part of E_{oss} is lost, in consequence the switching losses of the primary side switches are low at any load conditions and the overall loss contribution along all the load range of the converter is also relatively low (Figure 9 and Figure 10).

An additional benefit of the low Q_{oss} and having near ZVS transitions at no load is the relatively low *dv/dt* during the switching transitions and a low or no drain voltage overshoot of the HV MOSFETs thanks to the smooth quasi-resonant transitions (and consequently a better EMI).

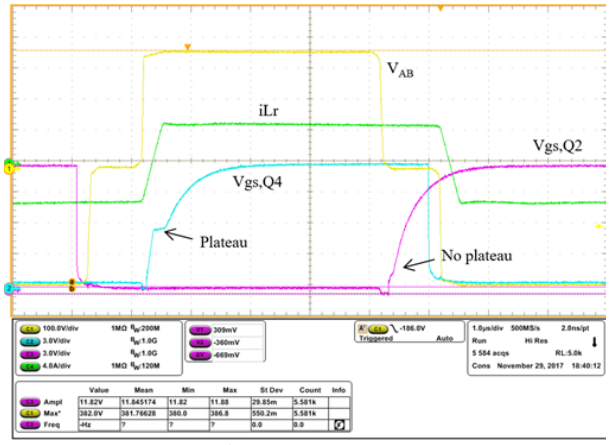

Figure 21. ZVS turn-on of lagging leg (D switch) and partially hard switched turn-on of leading leg (B switch).

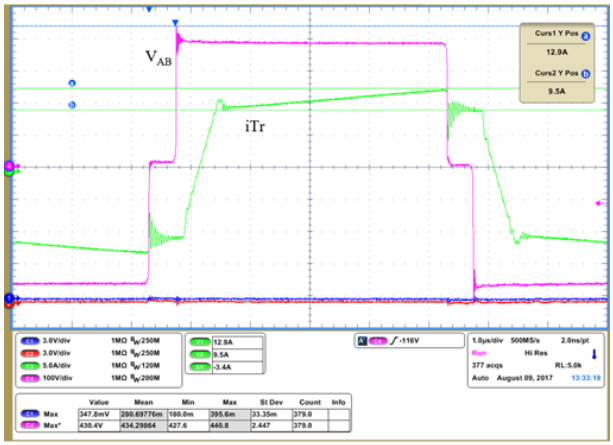

Figure 22. Full load drain voltage overshoot of the HV bridge.

The highest drain voltage overshoot in the HV MOSFETs happens at full load (Figure 22), due to the relatively high current during the hard-switched turn-off transition. In these transitions the parasitic inductances of the MOSFET package and of the layout causes voltage overshoot induced by the high *di/dt*. However, thanks to the low inductances of the SMD packages and the careful layout of the commutation loop, the overshoot is well under the maximum rated voltage (430 V in Figure 22 for an allowed maximum of 480 V, i.e. rated 80 % of 600 V, which is the nominal blocking voltage of the HV devices at T_j = 25 °C).

3.3.2. SYNCHRONOUS RECTIFIERS

The rectifying stage has a full bridge configuration with sixteen 9.3 mΩ 150 V OptiMOS™ 5 devices in Super SO-8 packages. With sixteen packages the dissipated power can be better spread bringing higher cooling capability and performance (lower $R_{ds,on}$ increase due to temperature). The full bridge configuration allows the usage of the 150 V voltage class with more than enough margin for the maximum drain voltage overshoot (90.88 V in Figure 23 for an allowed maximum of 120 V, i.e. rated 80 % of 150 V).

The controller adapts the turning-on and turning-off delays of the synchronous rectifiers along the load for a minimum body diode conduction time in order to reduce conduction losses and reduce generation of reverse recovery charges Q_{rr} (consequently better efficiency and lower drain voltage overshoot).

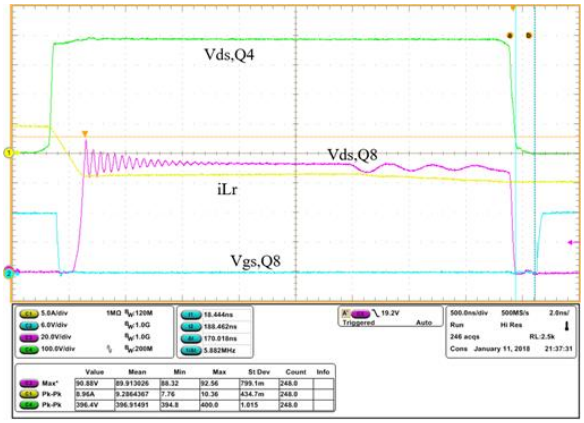

Figure 23. Standard synchronous rectification driving mode.

3.3.3. DYNAMIC RESPONSE

The controller implements hardware peak current control mode with fixed point discrete compensator implemented by software and designed for a bandwidth of 3.51 kHz, with a phase margin of 53.9 degrees and a gain margin of 15 dB, well within the standard stability criteria requirements. The dynamic response to load jumps (Figure 24) correlates well with the expected response of the designed compensation network, with an overshoot and undershoot within 1% of the nominal output voltage for a 50 % load jump.

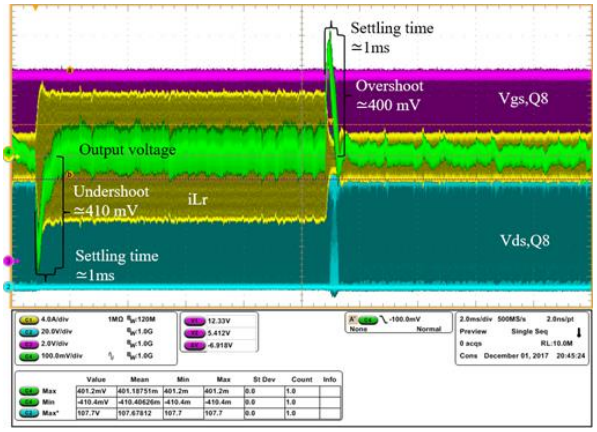

Figure 24. Load jump, half to light load and light to half load.

3.3.4. SOFT START-UP

The controller implements a soft start sequence to ensure the converter powers up with minimal stress over any of the components. During the starting-up sequence the output voltage is ramped up in close loop operation. The controller increments the output voltage reference within a timed sequence (Figure 25).

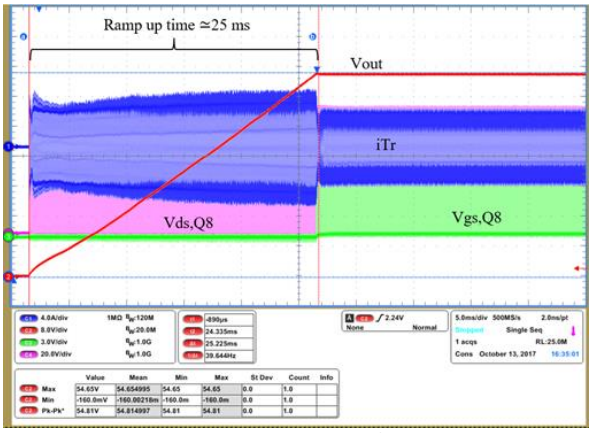

Figure 25. Output voltage soft start up.

3.3.5. BURST MODE

For further reduction of power losses under light load conditions (≤ 8 % load) the controller implements the so-called burst mode. During burst mode the converter works intermitently with a trail of switching pulses followed by an idle time. The burst mode ensures that under any condition the HV MOSFETs operate in full ZVS or at least partial ZVS (Figure 26). The burst operation reduces the power loss and maintains the smooth quasi resonant transitions of the drain voltage (little or no overshoots and better EMI). However, the output voltage ripple is usually increased in this mode of operation.

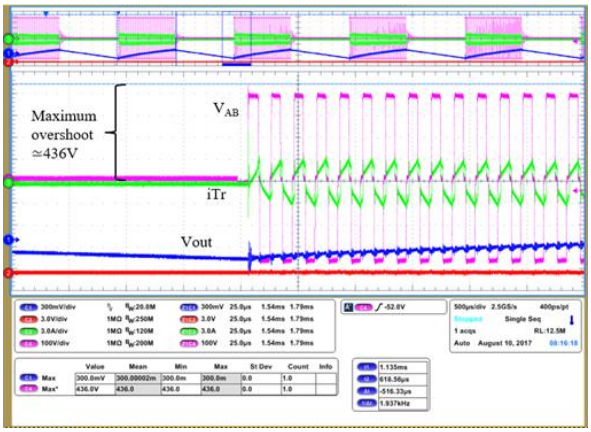

Figure 26. Burst mode sequence. Output voltage (blue), transformer primary current (green), bridge voltage (pink).

3.3.6. THERMAL MAP

The converter is designed to run enclosed in a metal chassis for the fan to provide enough air flow thanks to the channeling effect. However, the thermal captures in Figure 27 and Figure 28 have been taken with the converter running without enclosure for illustrative purposes (the temperatures with the converter enclosed in its chassis would be lower).

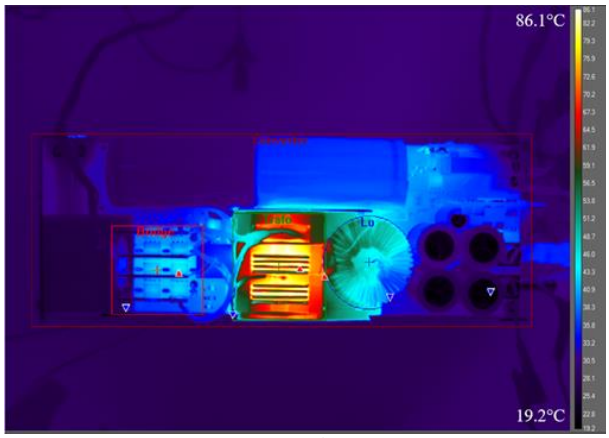

Figure 27. Thermal capture at 61 A of load with open case and external fan. Front view. The hot area corresponds to the main transformer.

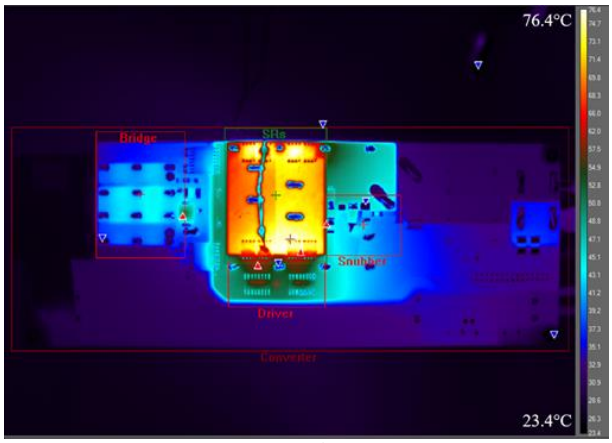

Figure 28. Thermal capture at 61 A of load with open case and external fan. Bottom view. The hot area corresponds to the main transformer and the synchronous rectifiers.

3.4. BOOST MODE EXPERIMENTAL RESULTS

In boost mode the 3300 W bidirectional PSFB behaves as a current-fed isolated boost converter. The output filter choke (L_o) becomes the boost inductor and the LV MOSFETs behave as the boost switches: short circuiting L_o between the LV supply and ground to store energy or letting the stored energy flow to the high voltage rail through the isolation transformer. In Figure 29, enclosed between the vertical markers is the effective boost duty cycle.

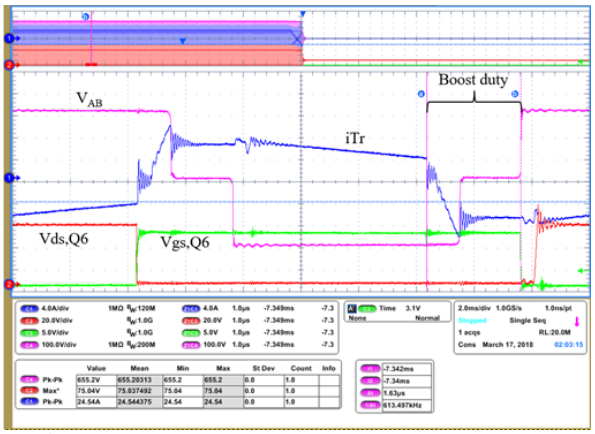

Figure 29. Boost mode duty cycle. Transformer primary current (blue), LV MOSFET drain voltage (red), LV MOSFET gate voltage (red), bridge voltage (pink). Please note that this capture was taken at scaled down input and output voltages.

The HV bridge effectively behaves in this mode as the boost diode. The HV bridge is actively driven to provide synchronous rectification and reduce drain voltage overshoot in the LV MOSFETs when working in this mode. The applied modulation scheme for the operation of a PSFB as a bidirectional converter is explained in more detail in the published article included in Chapter 7 [5]. Moreover the novel modulation scheme for the operation of PSFB as a bidirectional converter has been registered and a patent is pending.

3.4.1. PRIMARY SIDE HV FULL BRIDGE

The 3300 W bidirectional PSFB ensures full ZVS or at least partial ZVS of the HV MOSFETs at any working condition of the converter. At light or no load the converter ensures partial ZVS applying forced CCM in the LV MOSFETs side and recirculating enough energy for the quasi-resonant transitions of the HV bridge (Figure 30).

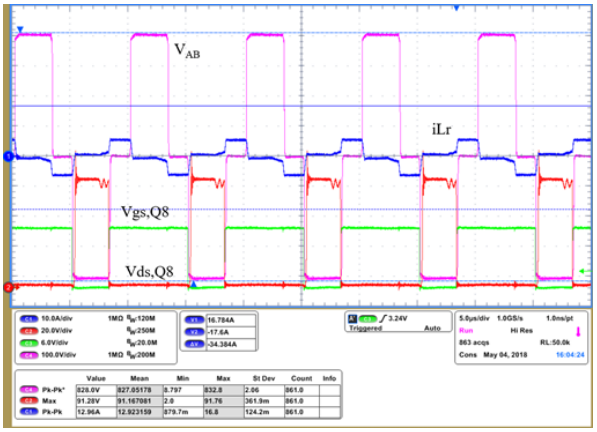

Figure 30. Partial ZVS of bridge MOSFETs at no load. Resonant inductance current (blue), LV MOSFET drain voltage (red), LV MOSFET gate voltage (green), bridge voltage (pink).

3.4.2. LV BRIDGE

In boost mode the LV MOSFETs are hard switched turned-on (Figure 31). This is the major difference between the losses distribution operating in buck or boost mode (total Q_{oss} of LV MOSFETs is relatively high) and the major reason for the difference in performance between modes (Figure 3).

The drain voltage overshoot of LV MOSFETs, like in buck mode, is well below the 80 % rated maximum (i.e. 120 V), e.g. around 92 V in Figure 30.

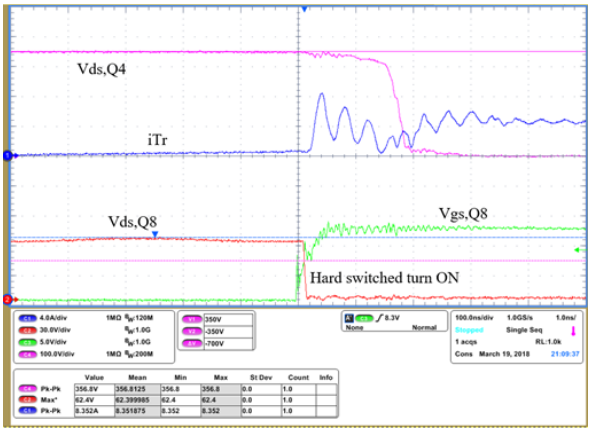

Figure 31. Hard switched turn-on of LV MOSFETs.

3.4.3. SOFT START-UP

In the boost mode the converter requires that the HV rail is pre-charged to a minimum voltage before being able to start up (see Figure 20). In a non-isolated boost converter a bypassing diode pre-charges the HV rail. However in an isolated boost converter it would require of rather more complex auxiliary circuitry [6]-[8].

The soft start sequence ensures full or partial ZVS of the HV MOSFETs from the very first pulses, with low or no drain voltage overshoot and smooth transitions (Figure 32 and Figure 33). The highest drain voltage overshoot occurs at full load, like in buck mode, due to the high currents during the hard switched turning-off transition (*di/dt* induced overshoot by parasitic inductances).

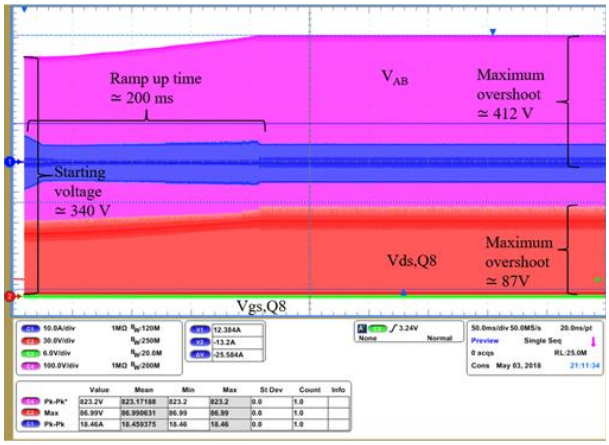

Figure 32. Soft start sequence of the isolated boost converter.

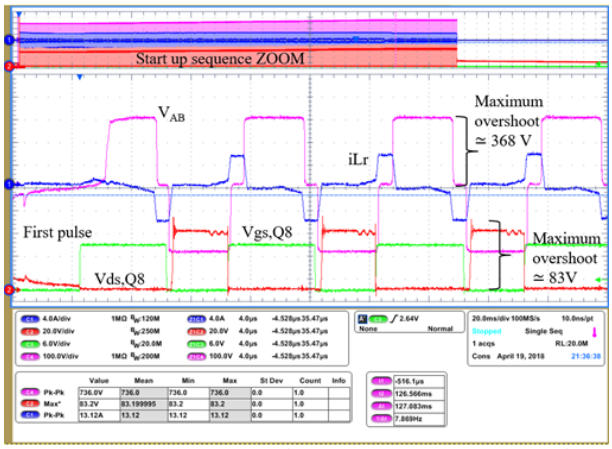

Figure 33. Soft start sequence, first pulses ensuring near ZVS for bridge transitions. Note: this capture was taken at scaled down input and output voltages.

3.4.4. BURST MODE

In boost mode the converter remains switching and recirculating enough energy for partial ZVS of the HV MOSFETs at light or no load. Burst would be only visible if the output voltage rises above the nominal regulation level (e.g. during load jumps) (Figure 34).

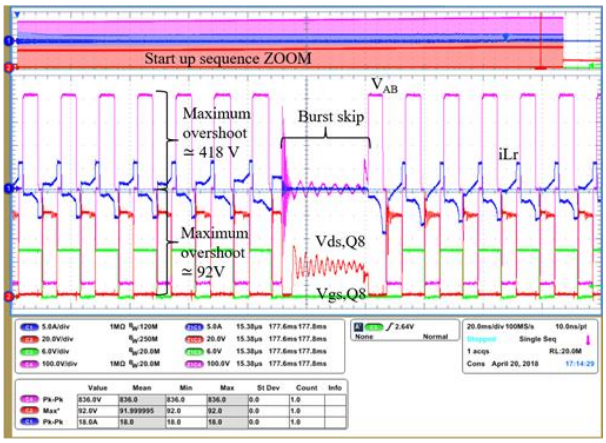

Figure 34. Burst sequence.

3.5. THERMAL MAP

The losses distribution has similar values in boost and in buck mode operation of the converter, with the main differences being the hard switched turning-on of the LV MOSFETs and the average current conducted through the clamping diodes (Figure 35).

At no load, unlike the control applied in buck mode, the converter does not stop switching but recirculates energy to achieve near ZVS transitions of the HV bridge. In Figure 35 can be appreciated a temperature raise on the HV bridge due to the partial hard switching (the speed of the fan is at the minimum in this condition contributing to the temperature increase), but still reaches only 33 °C (at 25 °C ambient temperature).

At full load (Figure 36) the main difference with the previous buck mode temperature capture is the temperature on the clamping diodes and the LV MOSFETs (hard-switched turned-on in this mode).

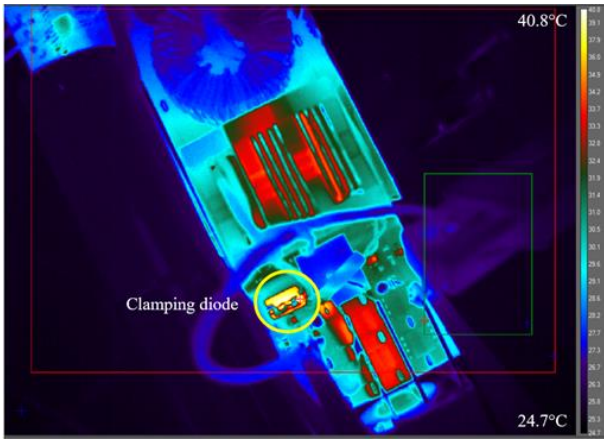

Figure 35. Thermal capture at no load. In boost mode converter does not stop switching, recirculate current enough for partial bridge ZVS. Front view.

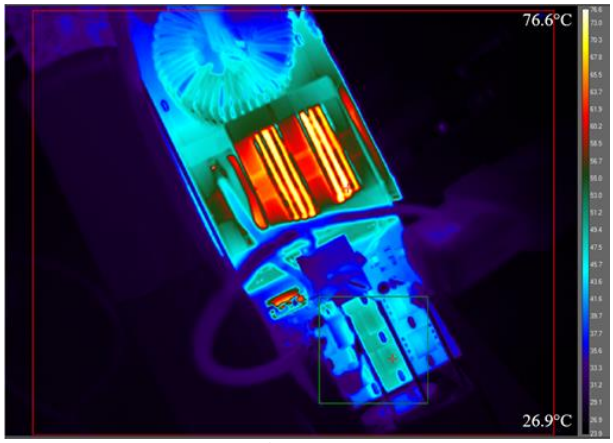

Figure 36. Thermal capture at full load. Front view.

4. USER INTERFACE

The controller includes serial communication interface (UART) and a proprietary protocol allowing the parametrization of the HV and the LV MOSFETs timings, output voltage setting, enabling and disabling of some protections and monitoring of the status of the converter. The user interface for Windows OS is an example of the capabilities of the included communication library within the controller. The user interface was specially developed to communicate with the controller through XMC™ Link (includes a UART to USB converter) [5] but other serial communication interfaces would be possible.

There are two available versions of the GUI:

- Advanced user interface (Figure 37) with run time parametrization capabilities of dead times, voltage and current thresholds, enabling and disabling of some protections and monitoring of status.
- Simplified user interface intended for monitoring of converter during runtime (Figure 38).

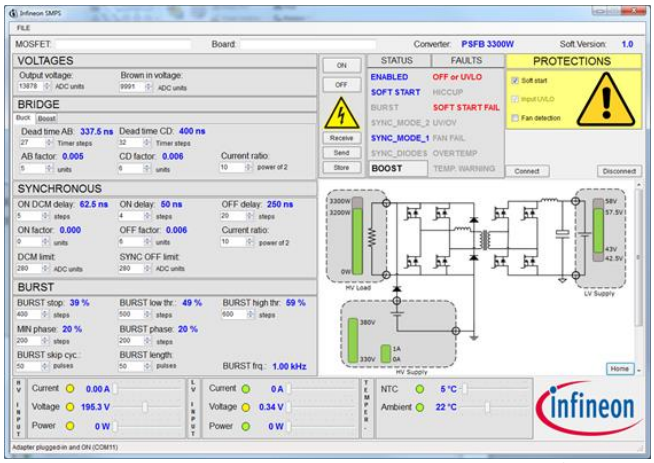

Figure 37. 3300 W bidirectional PSFB advanced user interface.

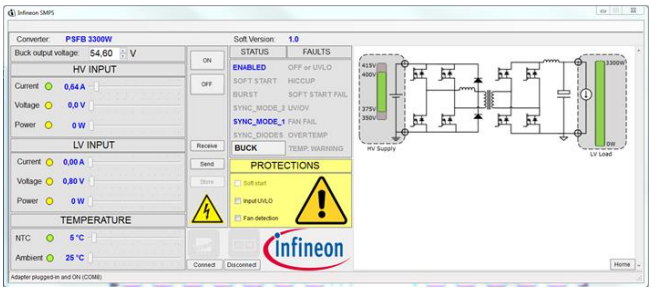

Figure 38. 3300 W bidirectional PSFB simplified user interface.

5. SCHEMATICS

The converter has been designed to be built comprised of a main board and two separate daughter cards: a controller card and an auxiliary on-board supply card. Figure 39, Figure 40 include the schematics of the main board and the control card. The auxiliary on-board supply in this converter is the same which was used in the converter in chapter 3, therefore its schematic has not been duplicated here.

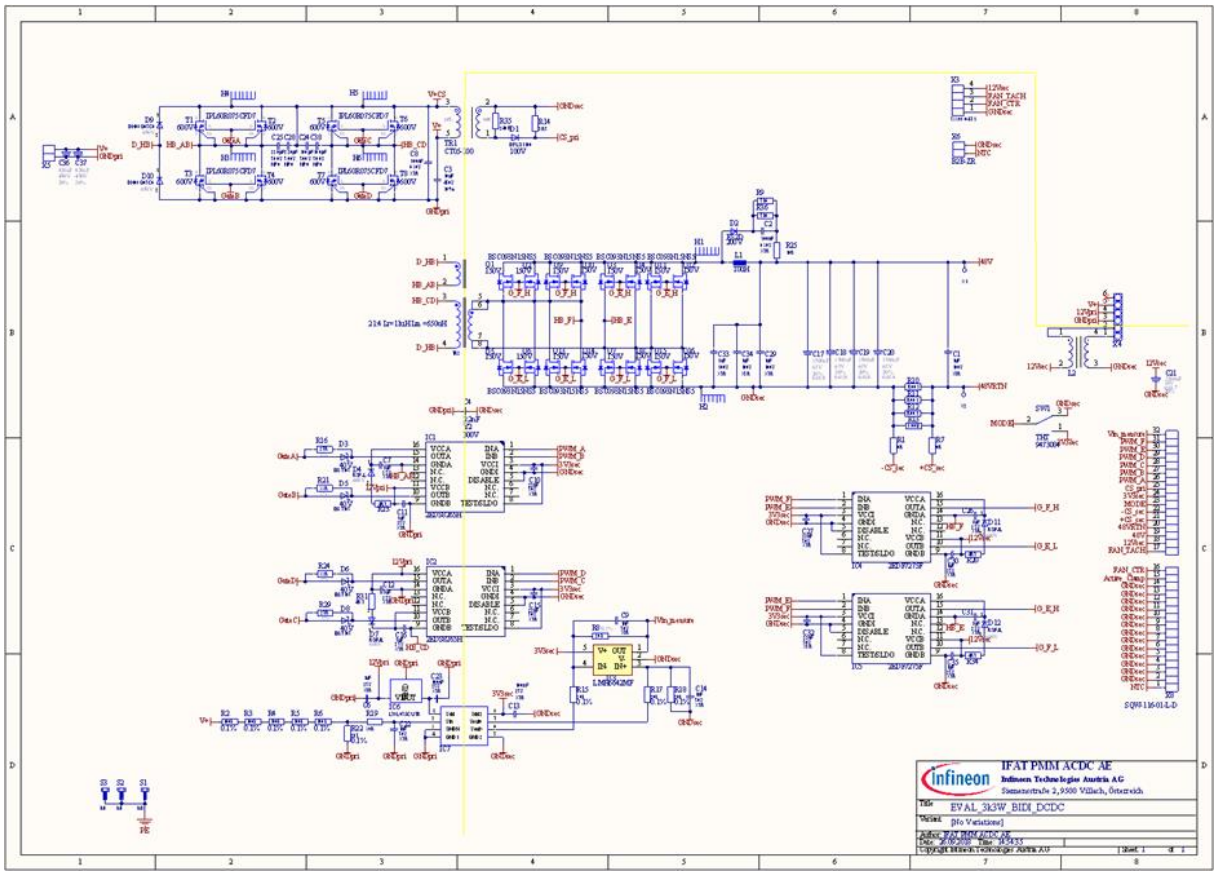

Figure 39. 3300 W bidirectional PSFB controller card with IPL60R075CFD7 and BSC093N15NS5.

6. CONCLUSIONS

This chapter has introduced a complete system solution for a 3300 W bidirectional DCDC converter achieving 98 % efficiency in forward or buck mode and 97 % in reverse or boost mode. The achieved power density is in the range of 4.34 W/cm³ (71.19 W/in³), which is enabled by the use of SMD packages, the innovative stacked magnetic construction and the innovative cooling solution.

This DCDC converter proves the feasibility of PSFB topology as a high efficiency topology at the level of fully resonant topologies when combined with the latest SJ MOSFET technologies. This DCDC converter proves as well that the PSFB topology can be used as a bidirectional DCDC stage without changes in the standard design or construction of a traditional and well known topology through innovations in control techniques powered by digital control.

The novel modulation scheme for the operation of a PSFB as a bidirectional converter is explained in more detail in the published article included in Chapter 7 [5]. Moreover the novel modulation scheme for the operation of PSFB as a bidirectional converter has been registered and is currently patent pending.

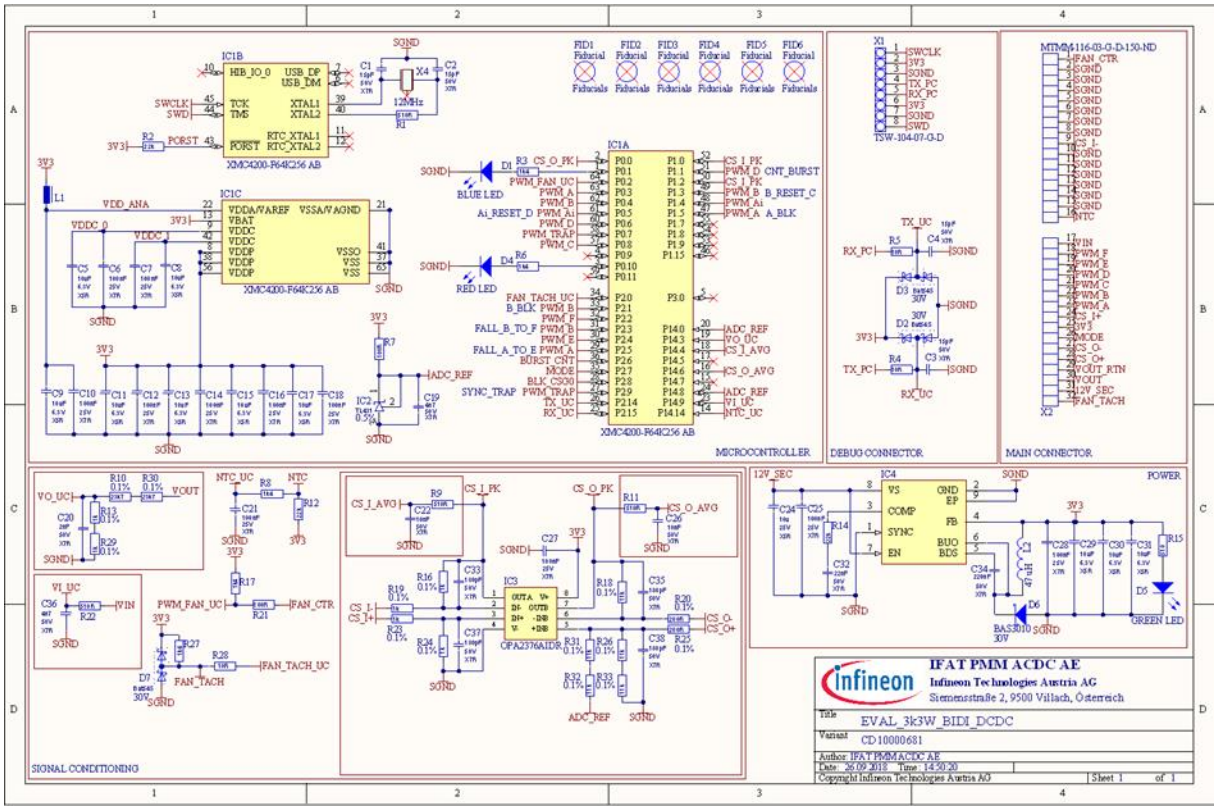

Figure 40. 3300 W bidirectional PSFB controller card with XMC4200-F64K256AB.

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CHAPTER 5. HALF BRIDGE LLC 3300 W

1. INTRODUCTION

In spite of its relatively complex design and control, the LLC topology has become increasingly common in medium and high power applications due to its high efficiency and the reduced component count of the circuit. The primary side of the converter comprises a half-bridge (HB), for low and medium power applications, or a full bridge, for higher power. The resonant tank comprises a series inductor, which can be implemented by the leakage of the transformer, a series capacitor and a parallel inductor, which can be realized by the magnetizing inductance of the transformer. The secondary side rectification stage can adopt several configurations: full bridge, voltage doubler or center tapped; however it does not influence the working principles of the converter significantly.

The LLC resonant converter has several advantages in comparison to the PSFB, due to the fact that there isn't an inductor at the output of the rectification stage:

- The voltage of the rectifiers is clamped by the output capacitance of the converter, which allows the selection of devices with a lower breakdown voltage, with the consequent improvement in their FoM.
- The secondary side rectifiers switching losses can be much lower than in a PSFB. In under resonant operation the *di/dt* is limited by the series resonance, which decreases the reverse recovery related losses. Moreover, the charge and discharge of their output capacitance can be nearly lossless because is inductively limited and clamped by the output capacitance. However, when the converter operates above resonance, like in PSFB, the secondary side rectifiers are hard-commutated from the primary, although limited by the series resonant inductor, which increases reverse recovery losses.
- After the end of a power transfer the secondary side of the transformer is unclamped, unlike in the PSFB where the freewheeling of the output inductor virtually short-circuits the secondary side of the transformer. Due to this, it is possible to use the energy in the magnetizing inductance of the transformer to achieve ZVS in the primary side switches.

However, because there is no inductor at the output of the rectification stage, the secondary side *rms* currents are comparatively higher than in a PSFB, and often require of an additional filtering stage to reduce the voltage ripple at the output of the converter.

Other noticeable advantage of LLC converters is their buck and boost capability (large signal gain). Thanks to that, this topology can be designed for its optimum performance at the nominal operating conditions and still be capable of regulation during hold-up time. Hold-up time is an important requirement for applications like server and telecom where the converter should provide full power up to 20 ms after the AC supply is missing.

This chapter introduces a complete system solution for a 3300 W HB LLC DCDC converter from 400 V to 51.5 V achieving 98.1 % peak of efficiency (Figure 1). The converter has been designed following the common requirements for telecom applications: wide range input (hold-up time) and wide range output (battery charging). This chapter describes the design and experimental results of the 3300 W LLC DCDC converter, including the novel integrated magnetic structure and the novel cooling concept, as well as the design specification requirements and the main test results.

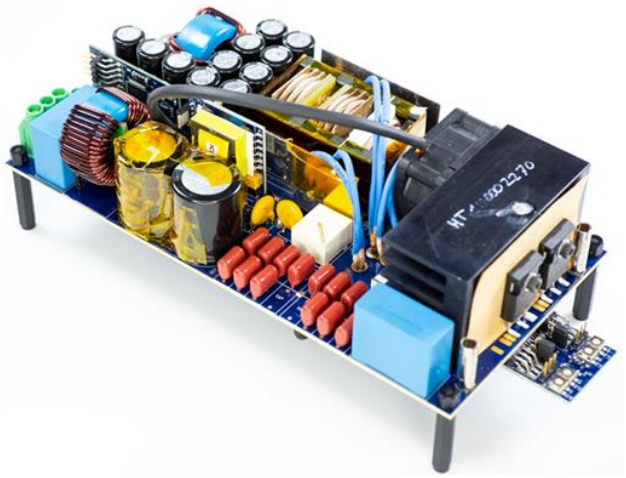

Figure 1. Prototype of 3300W LLC HB DCDC converter.

Figure 2 represents the simplified schematic of the implemented half-bridge LLC 3.3 kW DCDC converter prototype for telecom applications. The design consists of an LLC half-bridge with SRs in full bridge configuration, split capacitor and clamping diodes in the primary side. A summary of the most significant specifications

can be found in Table 1. The converter's nominal output voltage is telecom level (51.5 V) with wide range capability, also tailored for 48 V battery charger systems working within the 59.5 V to 43.5 V range. The converter is operated at a nominal input voltage of 400 V, whereas it can regulate down to 350 V at full load (at the nominal 51.5 V output voltage) providing room for hold-up time whenever the design is part of a full ACDC converter.

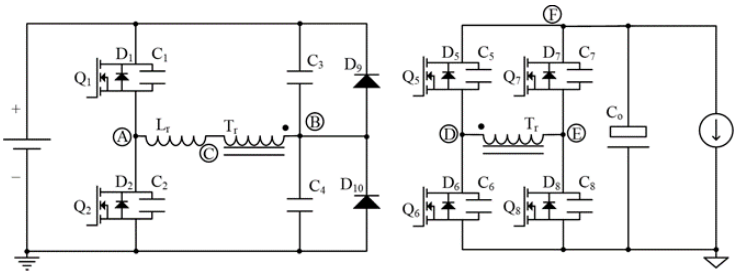

Figure 2. Simplified circuit schematic of the 3300 W HB LLC.

Table 1. Summary of specifications and test conditions for the 3300 W LLC HB

Test	Conditions	Specification
Input voltage Vin	350 V – 415 V	400 V nominal
Output voltage Vref	59.5 V – 43.5 V	51.5 V nominal
Output power	3300 W	At nominal conditions
Efficiency test	400 V input, 51.5 V output	ηpk > 98 % at 1650 W (50 % of load)
Steady-state Vout ripple	400 V input, 51.5 V output	|ΔVout| less than 200 mVpk-pk
Dynamic response	Vref ± 1 V	5 A – 35 A, 35 A – 65 A
Input UVLO	375 V on to 350 V off	Analog hysteresis window comparator
Output UVLO, OVLO	Vref ± 3 V	Shut-down and latch
Load transient	5 A ↔ 35 A, 1 A/µs	|ΔVout| less than 1 Vpk
	35 A ↔ 65 A, 1 A/µs	
OCP	68 to 75 A	Shut-down and resume
	> 75 A	Shut-down and latch
	Output terminals in short-circuit	Detection within switching period Shut-down and latch

The control of the LLC 3.3 kW prototype is implemented with an XMC4200 microcontroller from Infineon, which includes voltage regulation functionality, burst mode operation, output Over Current Protection (OCP), Over Voltage Protection (OVP), Under Voltage Protection (UVP), Under Voltage Lockout (UVLO), soft start, SR control, adaptive dead times (bridge and SRs) and serial communication interface. Further details about the digital control implementation and additional functionalities of the LLC control with the XMC™ 4000 family can be found in [1].

2. SYSTEM DESCRIPTION

The large signal voltage gain of the LLC converter is fundamentally controlled by the switching frequency (F_{sw}). It is especially noteworthy that at the normalized unity gain the converter operates at nearly fixed frequency (series resonance), independently of the load. The normalized gain excludes the transformer ratio, e.g. for a turn ratio of 15:4 the unity gain corresponds to 400 V input and approximately 53.3 V output.

Other alternative PWM and PWM/frequency hybrid control schemes are possible [9]. The PWM control schemes are useful especially at light load and in the buck operation mode where the required frequency tends to increase and where the gain can also become non-monotonic due to the converter parasitics [3]. However, some of the PWM schemes are only possible in full bridge LLC converters, and moreover can cause loss of ZVS in the HV switches.

2.1. RESONANT TANK DESIGN

The design of the converter and the resonant tank is based on the widespread First Harmonic Approximation (FHA) for resonant converters [4]. The FHA is extensively covered in the literature and would not be further explained here. However, it is known that the FHA losses accuracy at switching frequencies away from the series resonance F_{res}. The required gain of the converter at the corner cases ($V_{in,min}$, $V_{in,max}$, $V_{o,min}$, $V_{o,max}$) would have to be further investigated in circuit simulations and verified experimentally in the final hardware.

The quality factor *Q* of the resonant tank should be small enough to achieve the maximum output power at the minimum input voltage $V_{in,min}$ and the maximum output voltage $V_{o,max}$ (maximum required gain). The given maximum required boosting gain fixes the minimum resonant capacitance C_r for a chosen resonant frequency F_{res}, with F_{res} being a free design parameter that the designer can use to tune the maximum efficiency of the converter.

For each F_{res} the corresponding C_r can be calculated with equation (1) where R_{ac} stands for the reflected load resistance.

$$\begin{cases} Q = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{ac}} \\ F_{res} = \frac{1}{2\pi\sqrt{L_r C_r}} \end{cases} \xrightarrow{\text{yields}} C_r = \frac{1}{2\pi F_{res} R_{ac} Q} \quad (1)$$

In the 3300 W LLC prototype the maximum efficiencies can be achieved with a F_{res} around the 70 kHz (Figure 3). This should not be confused with the maximum efficiency of the converter happening with the converter operating at switching frequencies near the resonance. The transformer construction, the selection of the semiconductor technologies and their $R_{ds,on}$ influences the maximum achievable efficiency and at which F_{res} it can be achieved. The final selection of F_{res} and other design parameters would require of further iterations of the design procedure.

Therefore, in this design the resonant frequency was fixed to 70 kHz which results in a minimum $C_r \approx 465$ nF. In practice C_r and the other resonant tank values are approximated because not all exact values can be realized in the real hardware with discrete components and due to the tolerances in their values. Once fixed C_r the corresponding value of L_r for the selected F_{res} can be calculated with (2). In this design the resulting value is $L_r \approx 10.5$ µH.

$$L_r = \frac{1}{C_r(2\pi F_{res})^2} \quad (2)$$

$$m = \frac{L_r + L_m}{L_r} \quad (3)$$

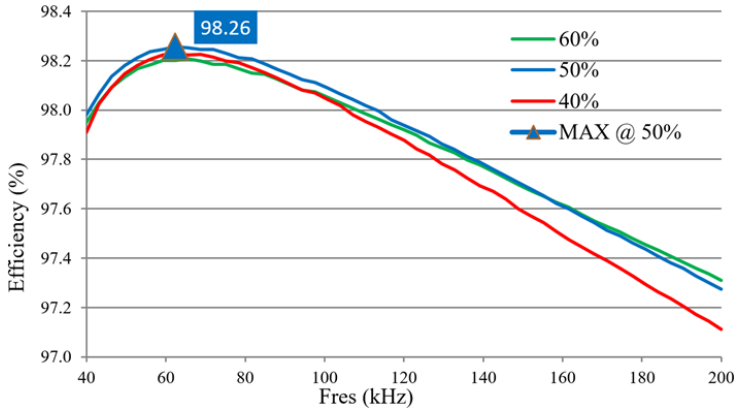

Figure 3. Estimated maximum efficiency of the 3300 W LLC design for different resonant frequencies (for a fixed *Q* and L_r to L_m ratio). Efficiency estimated at nominal operating conditions (near resonance): 400 V input and 51.5 V output.

The ratio of the total primary inductance to the resonant inductance *m* (3) is a tradeoff between the efficiency at nominal conditions and the converter gain range:

- A big ratio *m* reduces the primary side circulating currents and, in consequence, the conduction losses. However, it also reduces the available energy for ZVS in the primary side half-bridge (Figure 4 (a) and Figure 5 (a)). Furthermore, it makes difficult to maintain the regulation at reduced loads and low output voltages (minimum gain) without greatly increasing the switching frequency.
- A small ratio *m* increases the primary side circulating currents (Figure 4 (b) and Figure 5 (b)). However, it also increases the available energy for ZVS in the primary side half-bridge, which ultimately enables a lower $R_{ds,on}$ and overall higher efficiency along all the load range. Furthermore, the gain range of the converter is extended and the switching frequency span reduced.

For wide input and/or wide output converters like the 3300 W LLC prototype, it is required a small ratio *m*. Although achieving the full regulation range would still require of special considerations, especially at light load and maximum input $V_{in,max}$ or minimum output voltage $V_{o,min}$ (minimum required gain). One of the most widespread solutions for the extension of the gain range in buck operation is the burst mode control scheme [3].

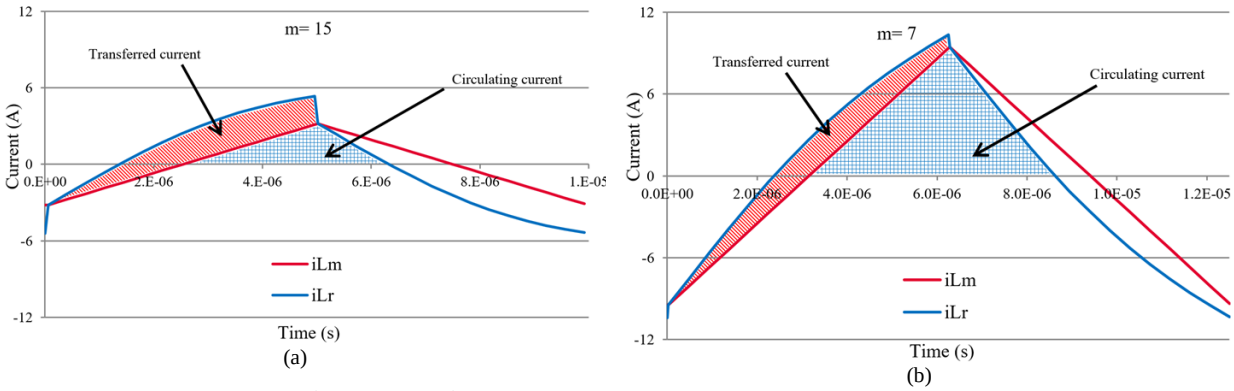

Figure 4. Primary side current waveforms at 10 % of load, 400 V input and 51.5 V output. A smaller magnetizing inductance ($_m$ = 7) increases the available energy for the HV MOSFETs transitions which ultimately extends the ZVS range.

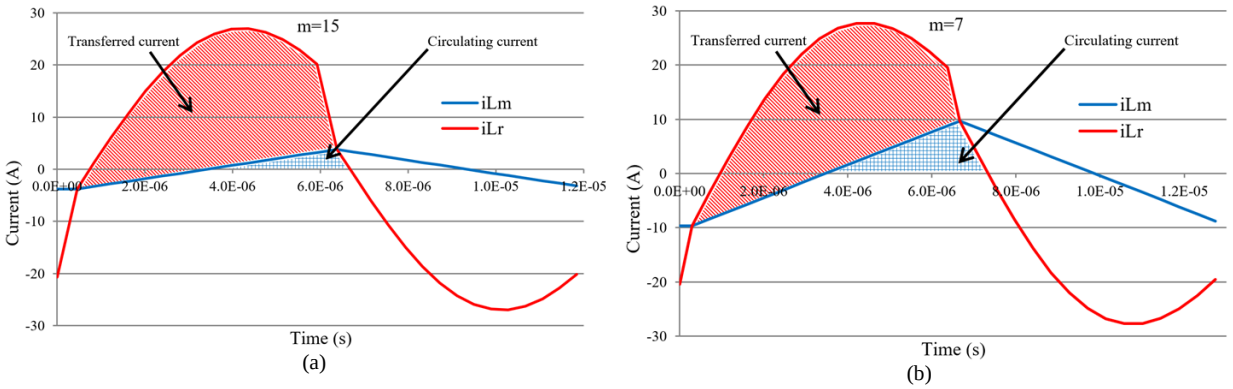

Figure 5. Primary side current waveforms at 100 % of load, 400 V input and 51.5 V output. A smaller magnetizing inductance ($_m$ = 7) increases the *rms* currents through the primary side of the converter. However, this can be compensated by a smaller $R_{DS,on}$ thanks to the extra available energy at light load.

2.1.1. CONVERTER GAIN IN NOMINAL OPERATION

The gain curves of the 3300 W LLC half-bridge converter at the nominal output voltage (51.5 V) and different loads are plotted in Figure 6. It can be observed that the frequency span along the load depends heavily on the operating point of the converter. Near resonance the frequency is almost constant along the load. However, deep under resonance (Figure 9), and especially far above resonance (Figure 11), the required frequency span for the control of the converter's gain increases dramatically.

An LLC converter is usually designed for its peak efficiency at the nominal conditions, which corresponds ideally to its most common mode of operation. This is especially useful for converters with a fixed output voltage and hold-up time requirements. For this design the specifications are 400 V input and 51.5 V output with the peak efficiency at the 50 % of load.

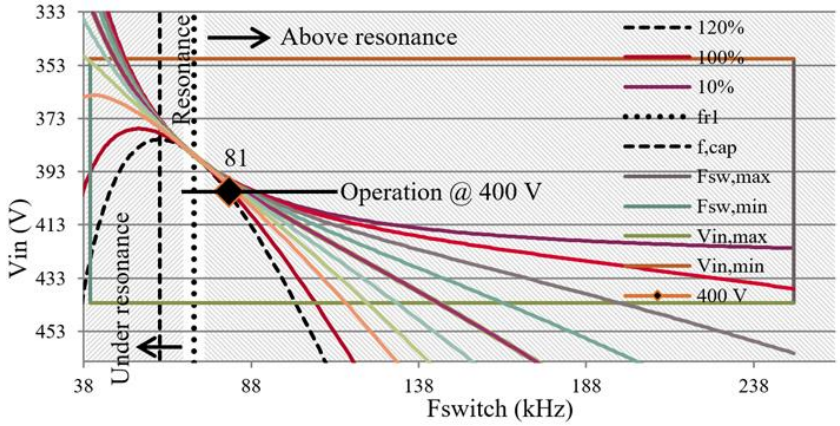

Figure 6. Estimated gain of the converter while operating at fixed 51.5 V output. Near resonance the switching frequency variation along the load range is small.

The peak efficiency of the converter (at the point of load of interest) does not necessarily happens exactly at the series resonance in every LLC converter design. Above the resonance the switching frequency increases and the switching losses become dominant. On the other hand, under resonance the core losses and the *rms* currents

and their related losses increase. In consequence the overall efficiency of the converter tends to decrease moving away of the nominal conversion ratio, but the exact location of the maximum depends on the losses balance of the design.

In this converter the peak efficiency (50 % of load) is achieved at 400 V input and 51.5 V output, as can be observed in (Figure 7 and Figure 8). This operation point is slightly above resonance, where the sum of frequency related losses and the conduction related losses are at their minimum. A different $R_{ds,on}$ selection, for example, can change the balance of losses and shift the operating conditions for the peak efficiency.

Finally, the switching frequency span of the converter ranges from 45 kHz up to 250 kHz. The mimimun switching frequency is limited to avoid operation in so-called capacitive mode (Figure 6), whereas the maximum frequency is mostly limited to avoid thermal runaway in the gate drivers and an excessive increase of the switching losses.

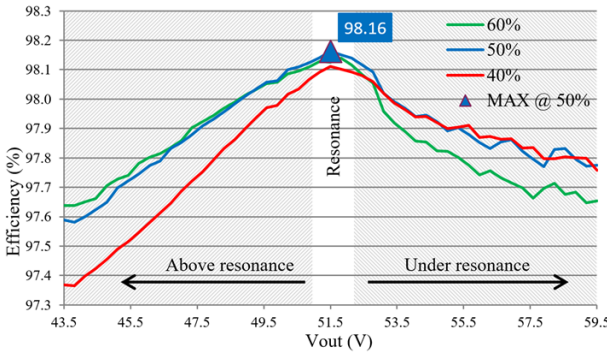

Figure 7. Estimated efficiency of the 3300 W LLC HB at different output voltages and fixed nominal input 400 V. The maximum efficiency is achieved around the resonance operation. Above resonance the switching losses become dominant. Under resonance the conduction losses dominate.

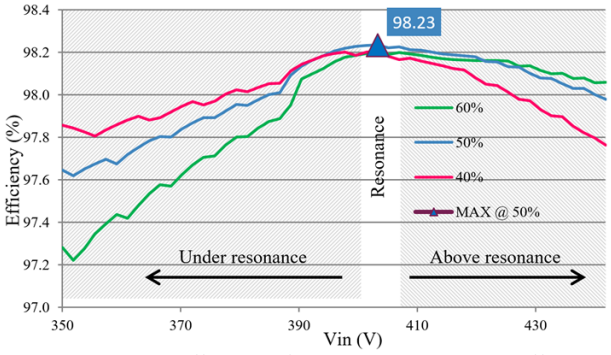

Figure 8. Estimated efficiency of the 3300 W LLC HB at different input voltages and fixed nominal output 51.5 V. In a full power supply the converter operates most of the time with the nominal input voltage. Only during hold-up time condictions the input voltage drops below nominal.

2.1.2. CONVERTER GAIN IN BOOST OPERATION

For output voltages above the nominal (higher than 52 V) the converter operates in the boost region, or the so-called under resonance (Figure 9). The boost region is also entered with low input voltages, for example during hold-up time.

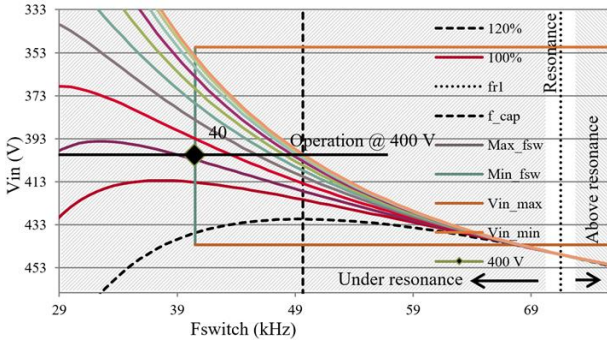

Figure 9. Estimated gain of the converter while operating at fixed 59.5 V output voltage. The converter cannot deliver the full peak power at the maximum output voltage while operating at 400 V input: the gain of the converter is limited in this region.

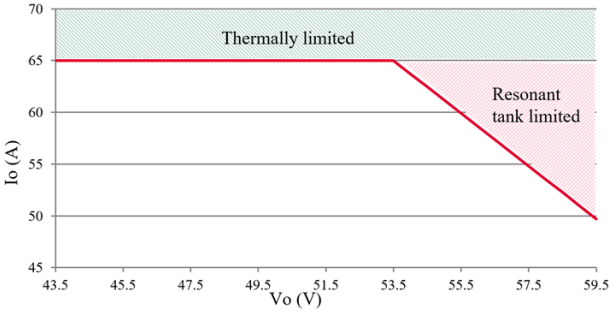

Figure 10. Adaptive over current protection limit. The gain of the converter is limited by the clamping diodes in the “resonant tank limited” area of the graph.

While under resonance and operating with heavy loads the converter risks entering the capacitive mode where the ZVS of the primary side MOSFETs is lost and they could also become hard-commutated. Nevertheless, the undesired condition can be prevented in several manners: limiting the minimum switching frequency (45 kHz in this design); limiting the maximum output current at the higher output voltages; or using clamping diodes in the primary side which avoids that the primary side current increases out of control.

Although the clamping diodes are a common solution for the capacitive mode protection, they can also limit the maximum output current at the higher output voltages (Figure 10). When the resonant capacitors voltage swings up to the HV rails, the clamping diodes conduct which ultimately limits the maximum possible gain of the converter.

2.1.3. CONVERTER GAIN IN BUCK OPERATION

For output voltages under the nominal (lower than 51 V) the converter operates in the buck region, or the so-called above resonance (Figure 11). In this region and at light loads the gain of the converter becomes almost flat.

Moreover, in practice, the large signal gain can become non-monotonic and rise again for increasing switching frequencies due to circuit parasitics and other phenomena not considered in the FHA [2].

There are several state of the art solutions for the extension of the minimum gain range in LLC. The solution adopted in this design is burst mode operation. The burst mode threshold is given by the maximum switching frequency which varies in the control of this converter depending on the different output voltages Figure 12. The adaptive threshold is required because of the dissimilar switching frequency ranges at the different output voltages (Figure 6, Figure 9 and Figure 11).

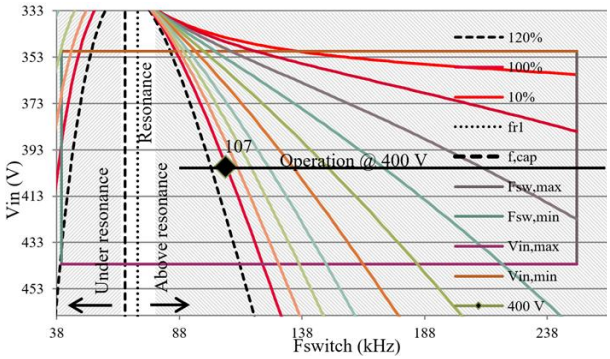

Figure 11. Estimated gain of the converter while operating at fixed 43.5 V output voltage. The frequency span is very wide. Although special control techniques can be used to reduce the gain and maintain the regulation at light loads.

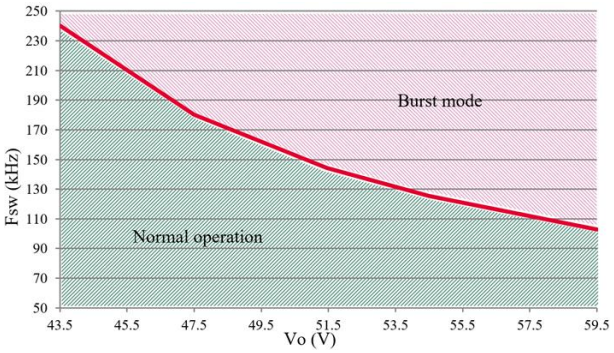

Figure 12. Adaptive burst threshold. The switching frequency increases and the range extends at the lower output voltages (buck operation, above resonance).

2.2. OVERALL LOSSES DISTRIBUTION

Figure 13 shows the placement of the different components on the 3300 W half-bridge LLC DCDC converter. The outer dimensions of the board, designed without enclosure, are 205 mm x 100 mm x 40 mm, which results in a power density in the range of 4 W/cm³ (66 W/in³).

The PSFB converter in Chapter 4 achieves a comparatively higher power density (4.34 W/cm³ or 71.19 W/in³). The main difference among the two is due to the cooling technique. The converter in Chapter 4 is enclosed in a chasis, which provides better air flow and allows the additional reduction in volume.

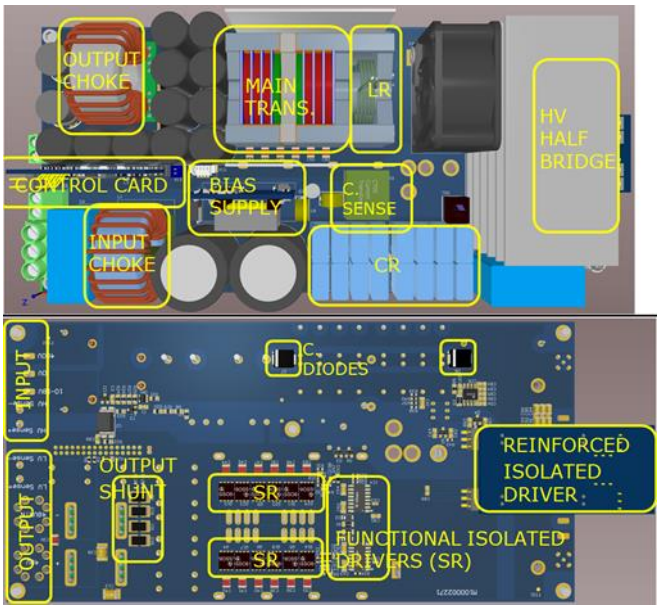

Figure 13. Placement of the different sections in the 3300 W half-bridge LLC . Current Sense (CS), resonant inductor (LR), synchronous rectifiers (SR), clamping diodes (C. DIODES), resonant capacitor (CR).

The estimated overall distribution of losses of the converter along the load proves the main transformer and the resonant inductance as the main sources of loss (Figure 14). The power switches, both the HV primary side half-bridge and the LV synchronous rectifiers exhibit very low and well balanced switching, driving and conduction losses.

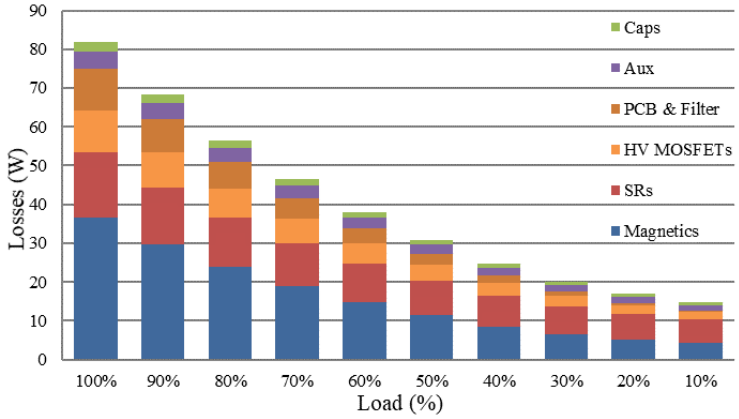

Figure 14. Overall losses breakdown of the 3300 W half-bridge LLC along the load range of the converter. Estimated at nominal conditions: 400 V input and 51.5 V output.

2.2.1. PRIMARY SIDE HV DEVICES

The primary side HV switches in the prototype are the IPW60R018CFD7 from Infineon. IPW60R018CFD7 devices are 18 mΩ, 600 V, CoolMOS™ CFD7 with fast body-diode in TO-247 package. This device has been selected in this design because of its low loss contribution along all the load range and because the good balance of conduction, driving and switching losses at the 50 % of the load, becoming the right device and $R_{ds,on}$ class when optimizing for the highest peak efficiency at that point (Figure 15).

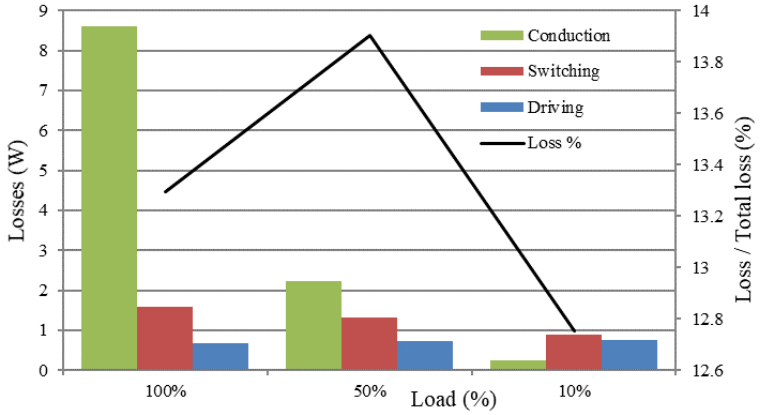

Figure 15. IPW60R018CFD7 loss distribution along load in the 3300 W LLC prototype. Absolute MOSFETs loss and its relative proportion to the total of losses in percentage. Estimated at nominal conditions: 400 V input and 51.5 V output.

The proposed driving circuitry includes an external turn-on resistor (10 Ω) in series to a medium-power Schottky diode, and an external turn-off resistor (2.5 Ω) also in series to a Schottky diode (Figure 16). The external turn-on resistor (10 Ω) plus the embedded MOSFET gate resistance ($R_{g,int}$) has little or no impact in the turn-on losses in ZVS but keeps *dv/dt* and *di/dt* under control in the event of possible hard-switched turn-on transitions (e.g. during soft-start or no-load operation). The external turn-off resistor helps dampening the voltage ringing in the gate driving loop of the MOSFET at high current turn-off transitions. Moreover, the external turn-off resistor does not have an impact on the switching losses thanks to the early channel shutdown mechanisms where the *dv/dt* is limited by the external capacitance and the resonant current (4) [5].

$$\begin{cases} \frac{dv}{dt_1} = \frac{\left(V_{plateau} - V_{driver}\right)}{C_{gd} R_{g,off}} = \frac{V_{plateau}}{C_{gd} R_{g,off}} & , \frac{dv}{dt} \leq \frac{dv}{dt_1} \\ \frac{dv}{dt_2} = \frac{I_{off}}{2C_{oss,tr}} & , \frac{dv}{dt} \leq \frac{dv}{dt_2} \end{cases} \tag{4}$$

Replacing the parameters in the equation (4) with the data from IPW60R018CFD7, the values of the proposed driving circuit and the maximum expected turn-off current in the application (I_{off}) we obtain the results in (5). In these conditions the turn-off speed would be limited by the driving path and would not be entirely lossless.

$$\begin{cases} \frac{dv}{dt_1} = \frac{5.25\ V}{75\ pF\ 2.5\ \Omega} \approx 28\ \frac{V}{ns} \\ \frac{dv}{dt_2} = \frac{30\ A}{722\ pF} \approx 41.5\ \frac{V}{ns} \end{cases} \tag{5}$$

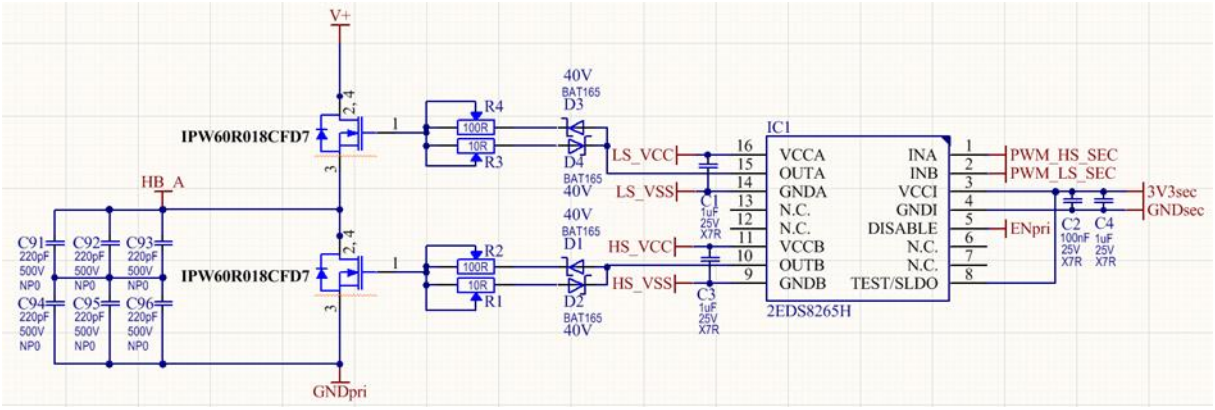

Figure 16. Proposed driving circuit for the 3300 W half-bridge LLC including the additional external capacitance for linearization and range extension of the early channel shutdown.

However, it is a standard practice to add external ceramic capacitors to linearize the SJ MOSFET switching behavior and further extend the early channel shutdown range (Figure 16). In the proposed circuit it has been added extra 330 pF in parallel that have to be considered in the previous analysis, and resulting in (6). In this scenario the turn-off transition becomes limited by the resonant charge of the equivalent capacitance of the central node of the half-bridge, and can be considered entirely lossless.

$$\begin{cases} \frac{dv}{dt_1} = \frac{5.25\ V}{75\ pF\ 2.5\ \Omega} \approx 28\ \frac{V}{ns} \\ \frac{dv}{dt_2} = \frac{30\ A}{(722+330)\ pF} \approx 28.5\ \frac{V}{ns} \end{cases} \quad (6)$$

The supply of the High Side (HS) driver has been realized by an auxiliary supply built around a single channel driver (Figure 17). The proposed biasing circuit self oscillates generating a fixed frequency square wave which is feed to a functionally isolated transformer and rectified afterwards in two separate secondary windings. Each of the secondary windings supplies one of the channels of a safety isolated half bridge driver: one channel for the high side MOSFET and other channel for the low side MOSFET.

The supply voltage of the HB driver is given by the auxiliary transformer turns ratio (stepping up 13:16) and the input voltage of the auxiliary supply circuit. The input of the auxiliary supply can be selected between the internally available 12 V (resulting approximately 14.5 V maximum driving voltage, considering the rectification diodes voltage drop) or supplied externally from 10 V up to 18 V.

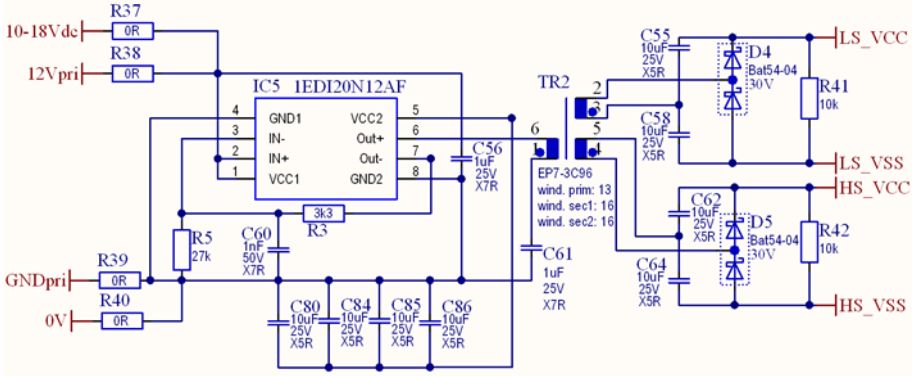

Figure 17. Proposed isolated supply for the driving of the HV half-bridge devices. The supply can be set to 12 V from the internal supply or within a 10 V up to 18 V from an additional external supply.

2.2.2. PRIMARY SIDE DEVICES $R_{DS,ON}$

At the time of this work, the 600 V CoolMOS™ CFD7 available portfolio in TO-247 package (Table 2) ranges from 170 mΩ (maximum) to the 18 mΩ (minimum).

For this design IPW60R018CFD7 was chosen because it has the best performance balance between the 100 %, 50 % and 10 % load points. However, other $R_{ds,on}$ could be used to achieve a different distribution of losses whenever there is interest in increasing performance at a different working point of the converter.

In Figure 18 and Figure 19 we present an example comparison of the estimated performance for three different $R_{ds,on}$ available in the 600 V CoolMOS™ CFD7 portfolio: IPW60R018CFD7 (device currently in the design), IPW60R070CFD7 and IPW60R055CFD7 (in between the two other $R_{ds,on}$).

Table 2. $R_{DS,on}$ portfolio for 600 V CoolMOS™ CFD7 in TO-247.

$R_{DS,on}$ [Ω]	TO-247
18	IPW60R018CFD7
31	IPW60R031CFD7
40	IPW60R040CFD7
55	IPW60R055CFD7
70	IPW60R070CFD7
90	IPW60R090CFD7
105	IPW60R105CFD7
125	IPW60R125CFD7
145	IPW60R145CFD7
170	IPW60R170CFD7

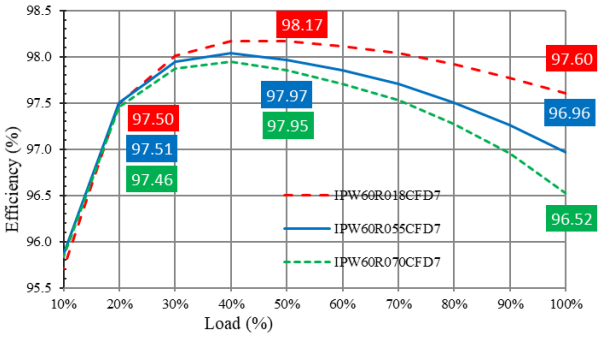

Figure 18. Estimated efficiency of the 3300 W HB LLC with different 600 V CoolMOS™ CFD7 $R_{DS,on}$ in TO-247. Estimated at nominal conditions: 400 V input and 51.5 V output.

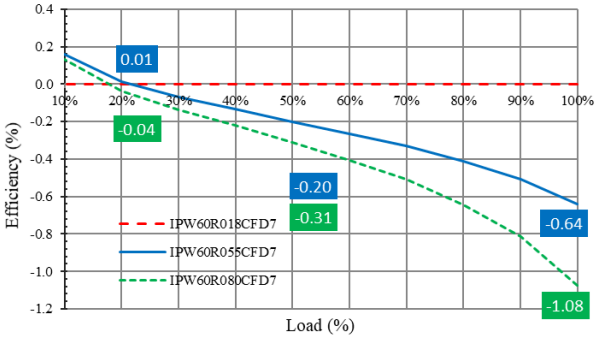

Figure 19. Differential estimated efficiency of the 3300 W HB LLC with different 600 V CoolMOS™ CFD7 $R_{DS,on}$ in TO-247. Estimated at nominal conditions: 400 V input and 51.5 V output.

Figure 20 represents the estimation of losses at the three main working points and how they balance for the three different $R_{ds,on}$ values previously chosen for the comparison. Although the difference in losses at 50 % and 10 % is small in comparison to the difference in losses at 100 % of load, the impact in efficiency is still noticeable, as can be observed in Figure 19. The steep change on the differential efficiency comparison between 20 % and 10 % is due to the partial loss of full ZVS at 10 % and the proportionally higher Q_{oss} values for the smaller $R_{ds,on}$.

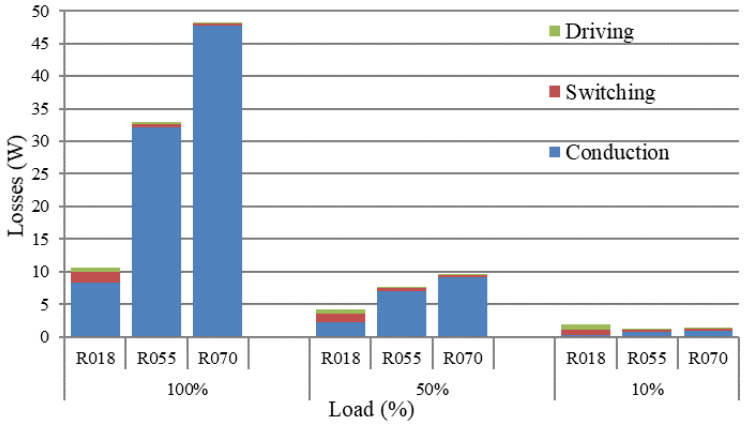

Figure 20. Estimated distribution of losses of the 3300 W HB LLC with different 600 V CoolMOS™ CFD7 $R_{DS,on}$ in TO-247. Estimated at nominal conditions: 400 V input and 51.5 V output.

2.2.3. TRANSFORMER

The main transformer has a conversion ratio of 15 primary turns to 4 secondary turns with a semi-planar construction. The cores geometry is PQ35/28 made of ferrite material DMR95 manufactured by DMEGC. The primary winding has been realized with triple-insulated Litz wire made of 175 strands of 0.1 mm diameter each, from Pack Litz Wire. The secondary winding is made of parallel tinned copper plates of 0.5 mm thickness.

The resonant inductance is stacked on top of the transformer, and also realized with half of a PQ35/28 core and six turns of Litz wire (of the same type than the primary side winding of the transformer).

The main transformer structure actually comprises two parallel transformers integrated with the external resonant inductance, which enables the realization of the required low L_m with several small gaps instead of a single large one.

Figure 21 shows an estimated loss distribution of the full stacked magnetic structure at nominal conditions. Notice that the transformer core loss is nearly constant along the load (apart from the material temperature dependence) due to the small switching frequency variation when the converter operates near resonance.

The maximum flux peak depends on the load and the operating point of the converter. It was estimated well below saturation flux density of the chosen core material (DMR95 from DMEGC) under any of the normal working conditions of the converter. An advantage of the integrated magnetic construction is the partial cancellation of flux within the parallel transformers and between the external resonant inductance and the main transformer block (Figure 22).

The winding technique and geometry of the core achieves good coupling (low leakage inductance, in the order of 500 nH), but still with relatively low intra-winding and inter-winding capacitances (in comparison to a full planar realization). Moreover, the interleaving of the primary and secondary windings minimizes proximity losses. A detailed description of the construction can be seen in Figure 23.

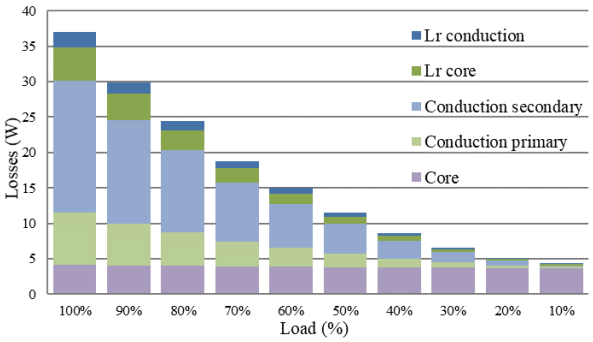

Figure 21. Estimated distribution of losses of stacked magnetic structure: transformer and resonant inductance (Lr). Estimated at nominal conditions: 400 V input and 51.5 V output.

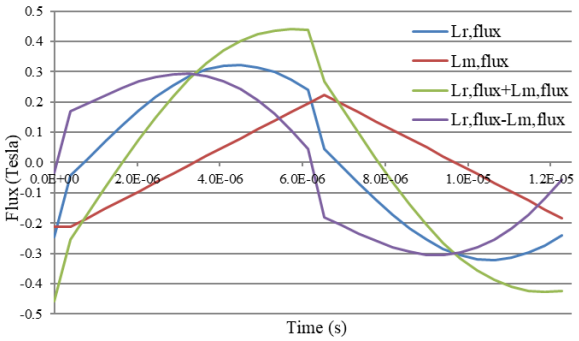

Figure 22. Estimated distribution of flux at full load and nominal operating conditions: 400 V input and 51.5 V output.

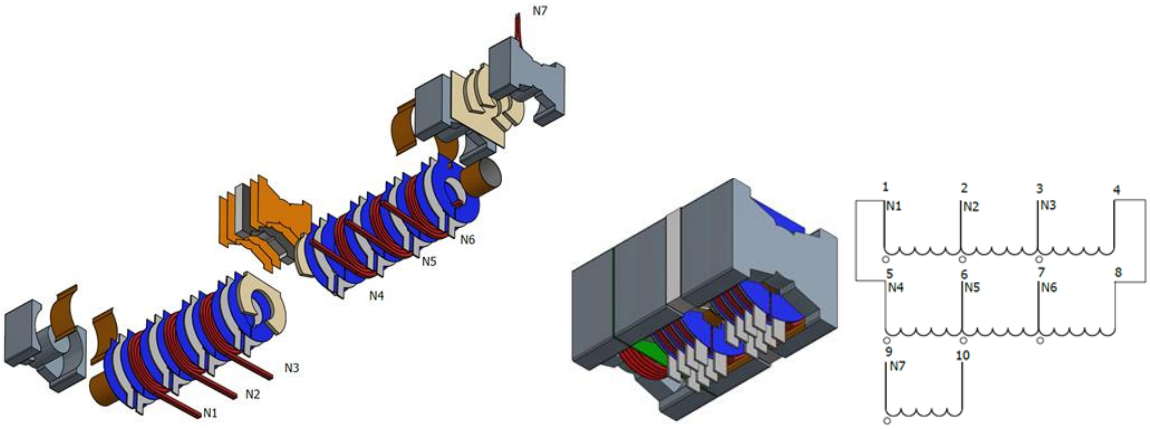

Figure 23. Main transformer and external resonant inductance. Mechanical drawing and simplified schematic.

2.3. COOLING SOLUTION

The proposed cooling solution in this design comprises an off-the-shelf aluminum heatsink for the HV half bridge devices and a set of two custom copper plates for the SR LV devices (Figure 24). The construction of the transformer, where secondary side winding is made out of copper plates, also constitutes part of the secondary side heat sink for the LV devices.

Figure 24. Heatsinks for HV half bridge bridge devices and LV secondary devices in a partially assembled 3300 W HB LLC converter board.

A single fan blows air into the integrated magnetics and the secondary side heatsinks. The same fan extracts air from the back of the primary side heatsink. Nevertheless, the primary side heatsink does not require much airflow because it has been purposely over-dimensioned to allow testing relatively high-ohmic devices in this board.

The fan speed is modulated along the load for best overall system efficiency (see Figure 25). Because of the high efficiency of the converter, little cooling effort is required at light and medium loads.

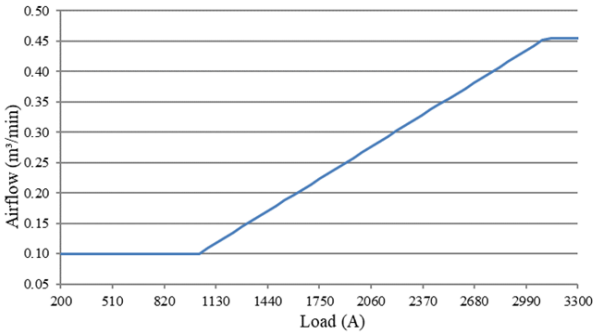

Figure 25. Fan airflow control along the converter's load range (estimated from fan datasheet and assuming fan is working with low pressure).

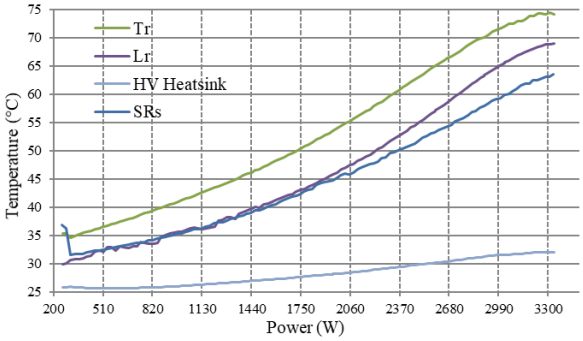

Figure 26. Measured temperatures on the 3300 W HB LLC converter at 25°C room temperature and without enclosure.

The experimental temperatures in the main components of the converter are plotted in Figure 26. Prior to the measurement of the temperatures the converter achieved thermal stability running 30 minutes at 100 % of load. Thereafter, in the same manner than for the efficiency measurements, the temperatures were registered while decrementing the load. The temperatures in Figure 26 demonstrate the effectiveness of the proposed cooling solution, besides their simple manufacture and assembly, and low cost. The cost saving enables a lower $R_{ds,on}$ for an improved performance.

3. EXPERIMENTAL

This section demonstrates the performance and experimental results of the 3300 W LLC prototype. Figure 27 shows the measured efficiency of the converter with and without the fan supplied by the included on-board auxiliary supply. Observe that the peak efficiency is comparable, although just slitghtly higher than that of the PSFB in Chapter 4.

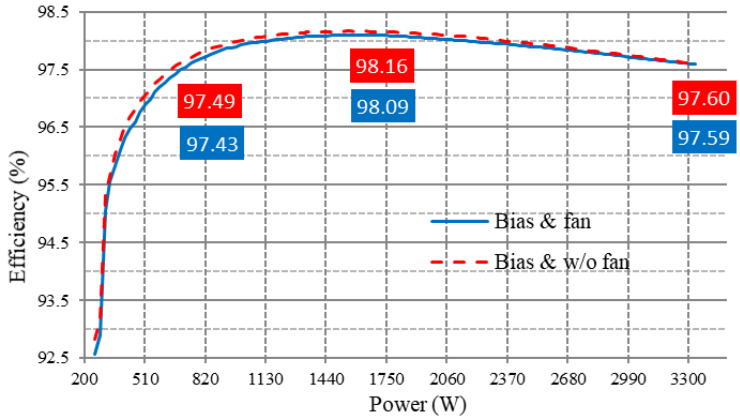

Figure 27. Measured efficiency of the 3300 W LLC HB at 400 V input and 51.5 V output.

3.1. TESTING SETUP

For the testing of the 3300 W LLC prototype, the suggested setup includes:

- HV supply capable of 400 V and at least 3500 W (when testing up to full load)
- LV electronic load (0 to 60 V), in constant current mode, capable of at least 3300 W (when testing up to full load)

The nominal input voltage of the converter is 400 V. The converter starts to operate above 375 V, turning back off when the input voltage falls below 350 V (hysteresis window). The valid input and output ranges of the converter are summarized in Figure 28.

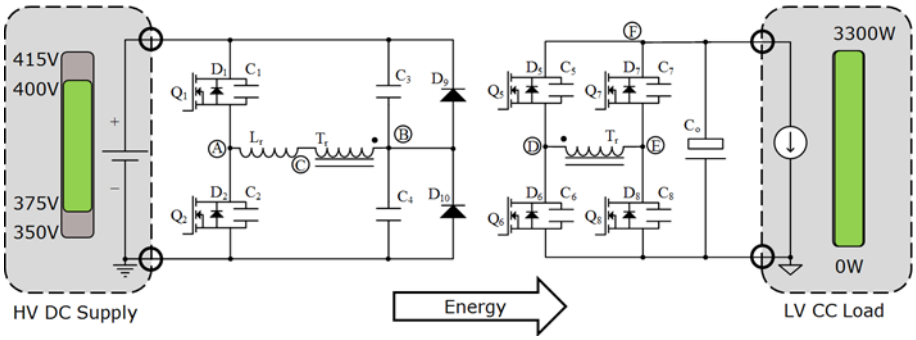

Figure 28. Recommended validation setup.

3.2. PRIMARY SIDE ZVS

The primary side HV devices achieve full ZVS above 30 % of load at nominal conditions: 400 V input and 51.5 V output (Figure 29). Moreover, the primary side half-bridge still achieves nearly full ZVS down to no load (Figure 30). In partial ZVS only a small part of the Q_{oss} is resistively charged and only a small part of the E_{oss} is lost. Thanks to this the switching loss contribution of the primary side half-bridge devices is negligible or relatively low in all working conditions of the converter (Figure 14 and Figure 15).

A benefit of the SJ MOSFETs output capacitance profile is the reduced impact of long dead times .The effective increase of output capacitance near the end of the transition delays the start of the body diode conduction while has a negligible impact on the switching losses (nearly no Q_{oss} and E_{oss} left at that point). Unlike other semiconductor devices, a conservative and robust, excessively long dead time is forgiving in SJ MOSFETs converters (Figure 31).

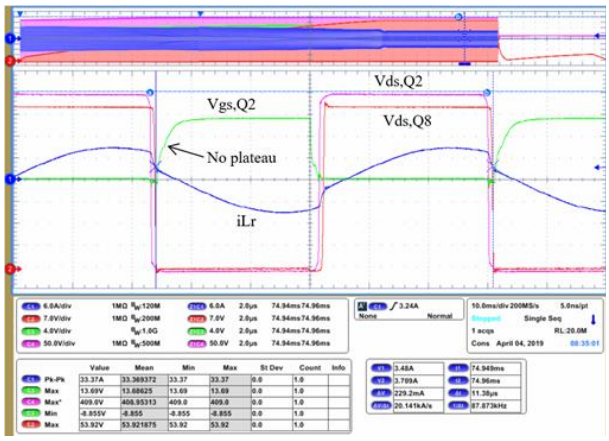

Figure 29. Converter waveforms in the threshold of full ZVS. Operating at 20 A of load, 400 V input and 51.5 V output.

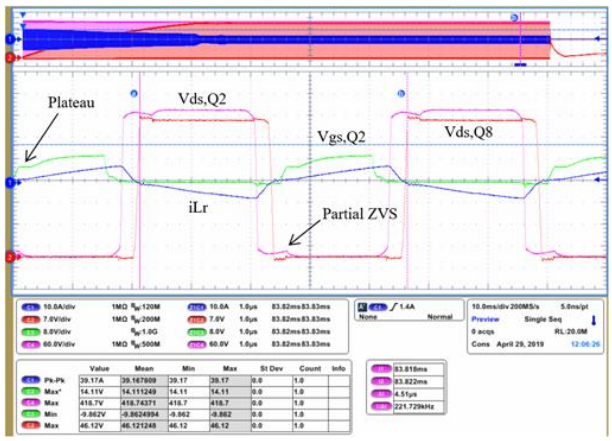

Figure 30. Converter waveforms at light load and minimum output voltages: maximum switching frequencies, lowest energy for ZVS transitions. Operating at 15 A of load, 400 V input and 43.5 V output.

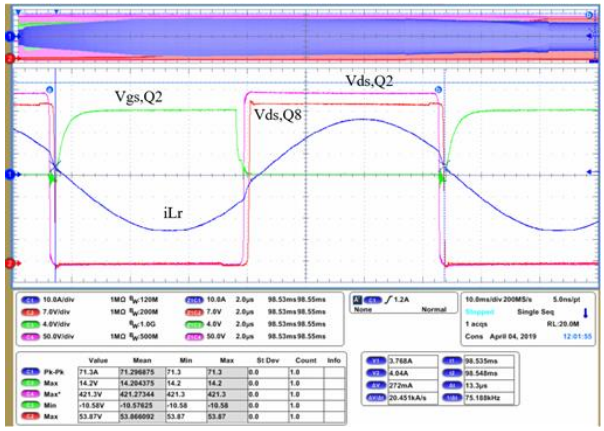

Figure 31. Converter waveforms at full load and nominal operating conditions: 65 A of load, 400V input and 51.5 V output.

The highest drain voltage overshoot in the HV MOSFETs happens at full load start-up due to relatively high-current turn-off transition (see soft start-up section). In these transitions the *di/dt* on the parasitic inductances of the MOSFET package and the layout induces the voltage overshoot. Nevertheless, in the prototype the overshoot

is maintained well under the rated maximum voltage limit in any of the operating conditions of the converter. A commonly rated limit would be 480 V (i.e. 80 % rating of 600 V at T_j = 25°C).

3.3. SYNCHRONOUS RECTIFIERS

The rectifying stage has a full-bridge configuration with twenty four 3.7 mΩ, 80 V, OptiMOS™ 5 in Super SO-8 package. With the high number of packages the dissipated power can be better spread, which brings higher cooling capability and performance (lower $R_{ds,on}$ increase due to temperature).

The full bridge rectifying configuration enables low losses for medium output voltage and medium output current converters. Thanks to the transformer construction with its low leakage, the optimized layout with minimal loop inductances, the OptiMOS™ 5 optimized output capacitance and low Q_{rr}; it is possible to use 80 V voltage-class devices with more than enough margin for the maximum drain voltage overshoot. The commonly 80 % rated limit for the 80 V devices would be 64 V maximum overshoot.

The controller includes adaptive turning-on and turning-off delays for the SRs along the load for a minimum body diode conduction time. The adaptive delays reduce conduction losses and the generation of reverse recovery charges (Q_{rr}) which translates into better efficiency and lower drain voltage overshoot.

In LLC converters, especially in wide output designs, the synchronous rectifiers have three main modes of operation [6]-[7]:

- At resonance (Figure 32) the gate signals of the SRs and the primary side HB are synchronous and have equal or similar duration.
- Above resonance (Figure 33) the SRs are delayed in relation to the primary side half bridge gate signals, although the pulse duration is still equal or similar to the half of the primary side period. The delay between the primary and secondary corresponds to the commutation time of the secondary side current, which also corresponds to the commutation time of the primary side current through L_r.
- Under resonance (Figure 34) the activations of the SRs is synchronous to the primary side half bridge. However the pulse duration of the SR is shorter than half of the primary side period, and in accordance to the natural frequency of the resonant tank.

On top of those three main modes of operation, at light loads, due to the charge of the output capacitance of the SRs, their conduction time further reduces.

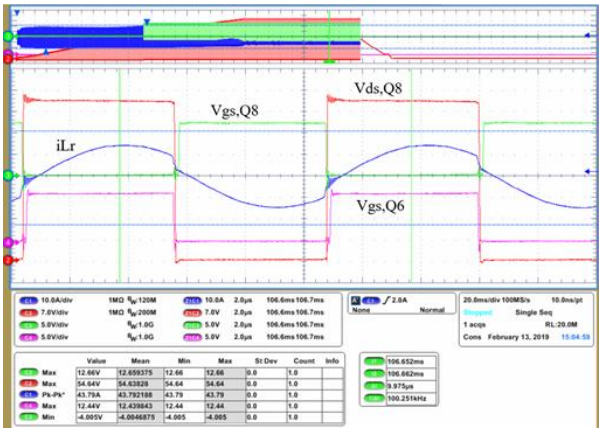

Figure 32. Gate driving pulses of the synchronous rectifiers near resonance. The SR turn-on is aligned to the primary side HB. The SR turn-off is also aligned to the primary side HB.

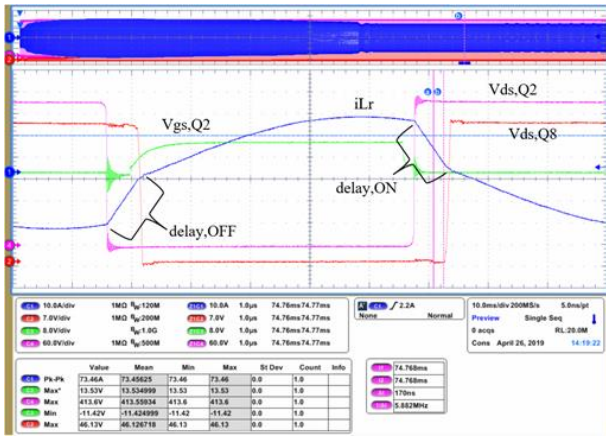

Figure 33. Gate driving pulses of the synchronous rectifiers above resonance. The SR turn-on is delayed in relation to the primary side HB. The turn-off is also delayed in relation to the primary side half-bridge by the same amount of time.

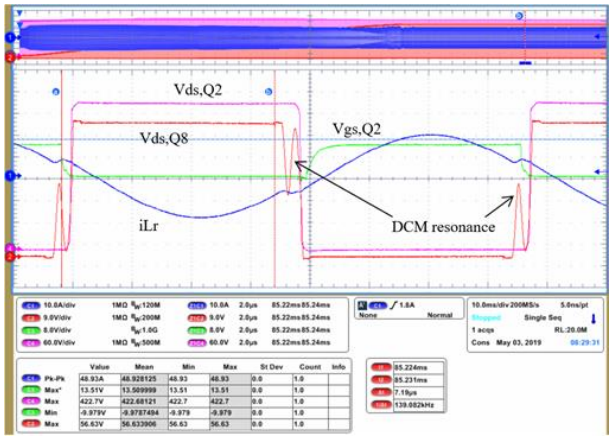

Figure 34. Gate driving pulses of the synchronous rectifiers under resonance. The SR turn-on is aligned to the primary side HB. However, the SR turn-off happens earlier than the corresponding primary side HB pulse.

3.4. DYNAMIC RESPONSE. LOAD JUMPS

The controller includes a software implemented digital compensator designed for a bandwidth of 2 kHz with a phase margin of 45 degrees and a gain margin of 12 dB, well within the standard stability criteria requirements. The dynamic response to load jumps (Figure 35, Figure 36 and Figure 37) correlates well with the expected response of the designed compensator, with an overshoot and undershoot within 2.5 % of the nominal output voltage for a 50 % of load jump.

The small signal gain and phase of an LLC converter depends strongly on the load and operation point. One possible approach is to design the compensation network for the worst case and accept a poor performance in other conditions.

In this design an adaptive PID (proportional integral derivative) compensator was implemented with variable proportional and derivative constants along the output voltage range. This enables a more consistent response of the converter (Figure 35, Figure 36 and Figure 37).

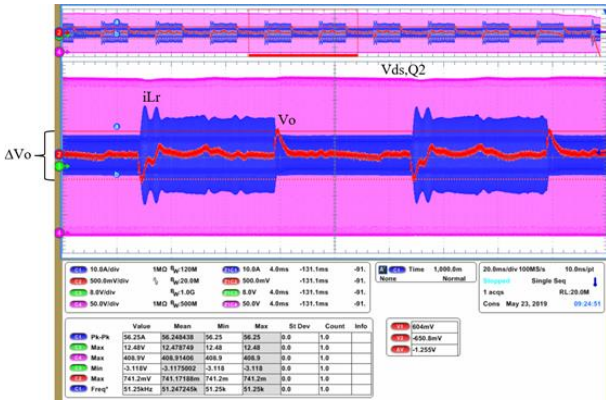

Figure 35. Load jump 5 A to 35 A at 59.5 V output. The converter gain increases and the phase marging decreases operating under resonance.

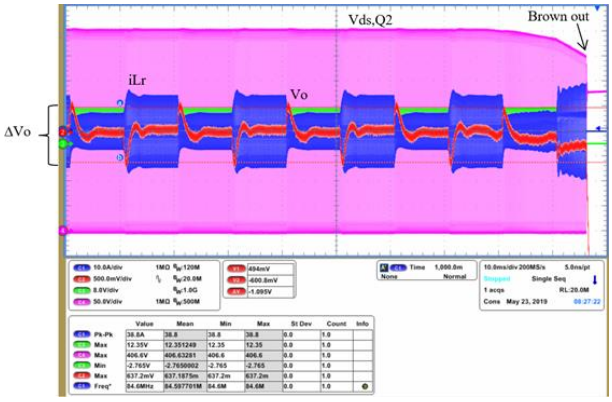

Figure 36. Load jump 5 A to 35 A at 51.5 V output.

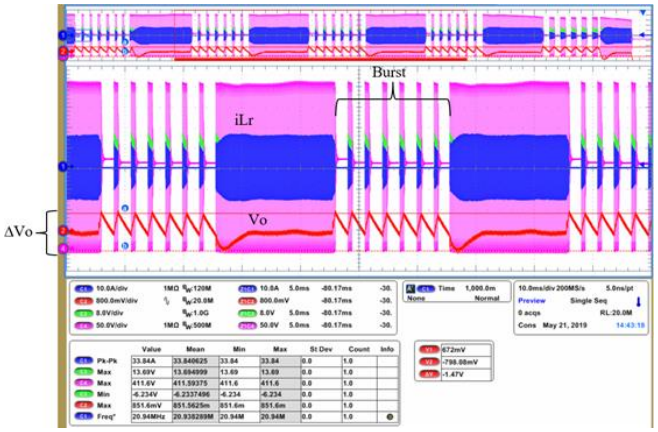

Figure 37. Load jump 5 A to 35 A at 47.5 V output. The converter gain decreases and the phase marging increases operating above resonance. At the lower output voltages the converter operates in burst mode at light loads.

3.5. SOFT START-UP

The controller implements a soft-start sequence to ensure the converter powers up with minimal stress (voltage and current) on any of the components. During the start-up sequence the output voltage is ramped up in closed-loop operation. The controller increments the output voltage reference within a timed sequence (Figure 38, Figure 39).

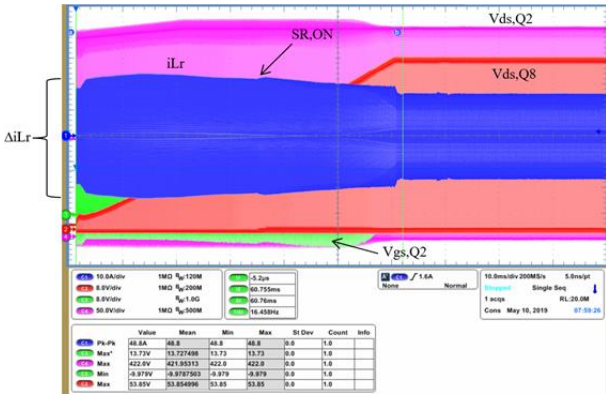

Figure 38. Start-up sequence at 40 A load, 400 V input and 51.5 V output. The maximum voltage overshoot-undershoot in drain and gate of the HV MOSFETs occurs during the start-up, where the HB operates with the highest turn-off currents.

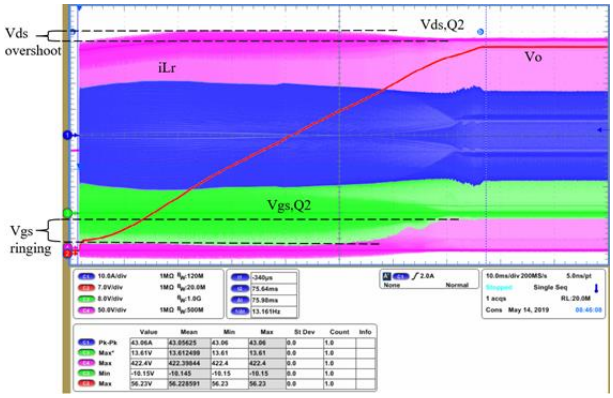

Figure 39. Start-up sequence at 40 A load, 400 V input and 55.5 V output. The maximum voltage overshoot-undershoot in drain and gate of the HV MOSFETs occurs during the start-up, where the HB operates with the highest turn-off currents.

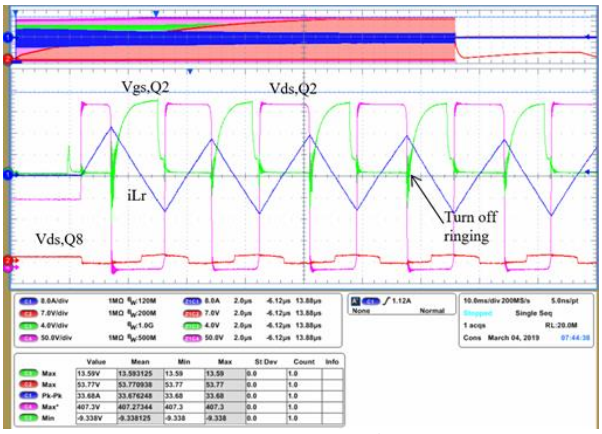

Figure 40. Starting up sequence. The pulse sequence at the start ensures ZVS of the HB devices while maintaining the peak to peak current within reasonable values.

The starting pulses follow a predefined timing sequence to ensure ZVS and avoid hard-commutation on the primary side half bridge (Figure 40). The maximum stress occurs on the drain and gate voltages of the primary side devices due to the high turn-off current transitions. Nevertheless, the maximum peak voltages can be controlled increasing the turn-off resistor in the driving path. Larger value of turning-off resistor reduces de ringing, although extreme values may increase significantly the switching losses.

3.6. RESONANT TANK

The current through the primary side of the converter is nearly perfectly sinusoidal at the resonant frequency, around 70 kHz (Figure 41).

The resonant capacitor voltage at full load and during the first pulses of the start-up sequence is plotted in Figure 42 and Figure 43 respectively. The maximum gain of the converter would be limited by the clamping diodes if the peak to peak voltage excursion of the resonant capacitors reaches the upper or lower limits of the supply rails.

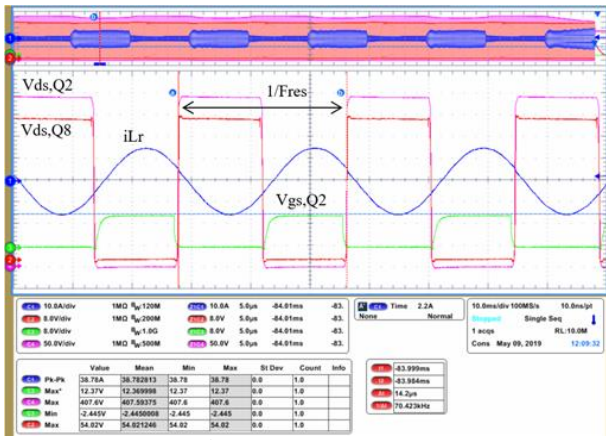

Figure 41. Resonance frequency. Characteristic sinusoidal current through L_r at the series resonant frequency of the resonant tank.

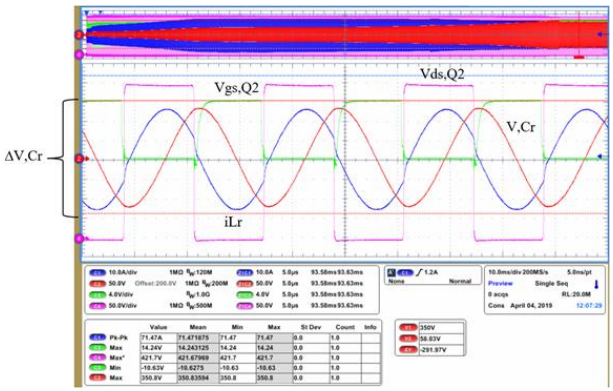

Figure 42. C_r voltage at full load (65 A), nominal input 400 V and nominal output 51.5 V.

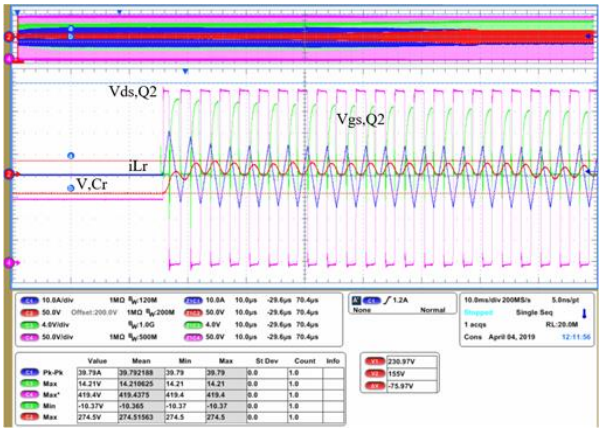

Figure 43. C_r voltage during start-up at nominal input 400 V and nominal output 51.5 V.

3.7. BROWN-IN AND BROWN-OUT

The converter starts up above 375 V input and shuts down under 350 V (Figure 44), giving room enough for the operation during hold-up time when the LLC converter is part of a full ACDC power supply. The amount of required bulk capacitance during hold-up time can be calculated with the equation (7).

$$C_{bulk}\frac{(V_{in,nom}-V_{in,min})^2}{2}=\frac{P_{o,max}}{\eta_{DCDC}}T_{hold} \quad (7)$$

At the lower input voltages the converter operates deep under resonance (Figure 45).

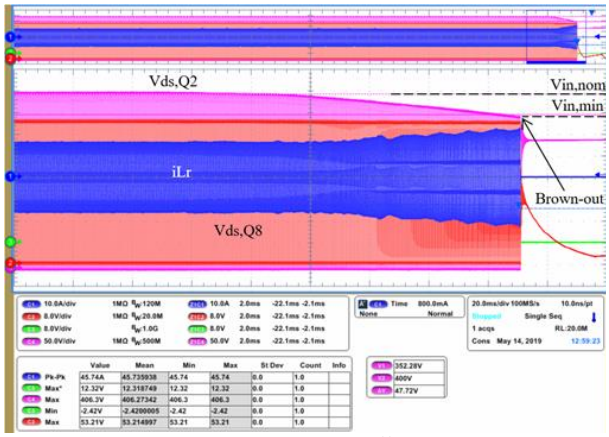

Figure 44. Brown out. The converter turns-off when the input voltage falls under approx. 350 V.

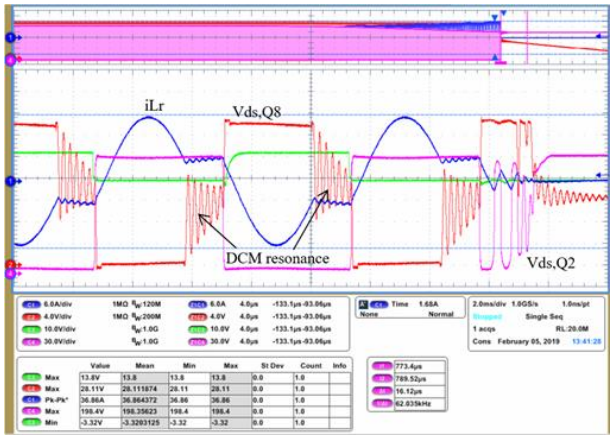

Figure 45. Brown out. The converter operates deep under resonance when the input voltage decays (boost operation). Similar scenario would occur during the hold-up time operation.

3.8. OVER CURRENT PROTECTION

Several redundant protections mechanisms have been implemented on the fully digital control solution with XMC™ microcontrollers from Infineon. The multiple protections are meant to ensure reliable operation of the converter.

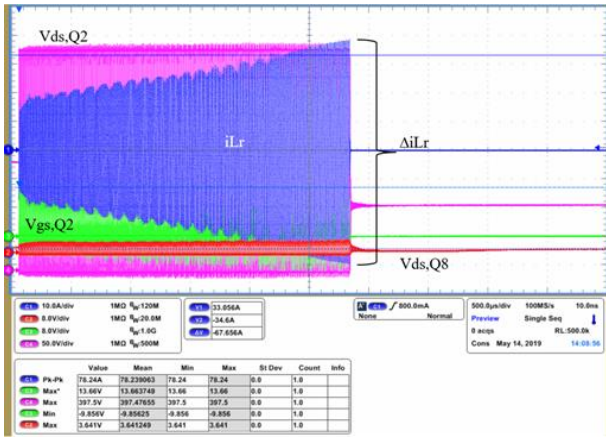

Figure 46. Over current protection at the start-up. Several redundant protection mechanisms protect the converter from overload at the start-up: cycle by cycle peack current limit, maximum load current, voltage rise time timeout.

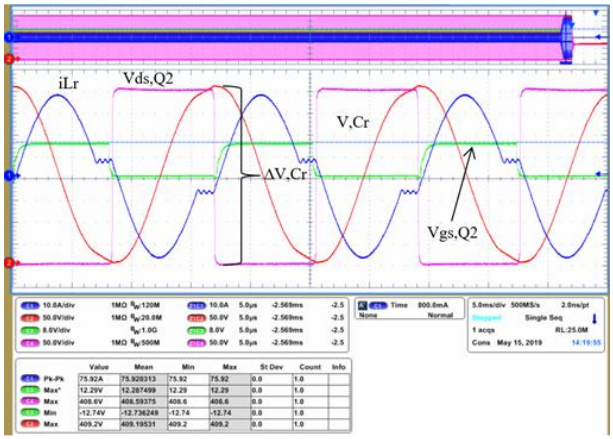

Figure 47. Over current protection, slow mechanism.

Specifically for the overload or over current protection of the converter these are the main mechanisms (including also solutions in the hardware):

- Clamping diodes on the primary side of the converter. Limits the maximum current and voltage ripple on the resonant tank capacitors. Moreover, limits the primary and secondary side maximum peak currents.
- Cycle by cycle peak current limit. An integrated analog comparator within the XMC™ limits the maximum primary side peak current to 40 A (Figure 46).
- Maximum average output current. The average output current of the converter is measured through a resistive shunt. The maximum average load current is limited to 68 A with a programmable time delay (Figure 47). The maximum average current limit is reduced at higher output voltages to avoid the clamping diodes conduction in steady state (Figure 10).
- Output under voltage lockout. In the event of short-circuit or strong overloads, the output voltage of the converter drops out of control. The converter detects the abnormal working conditions when the voltage goes out of a ±3 V window around the output voltage reference setting.

3.9. BURST MODE OPERATION

For further reduction of power losses in light-load working conditions the controller implements burst mode operation. The threshold of burst is adaptive for the different output voltages (Figure 12). The implemented algorithm limits the maximum switching frequency of the converter and enters burst mode when the output voltage goes above a programmable threshold over the reference value ($V_{o,ref}$ + 750 mV) (Figure 48).

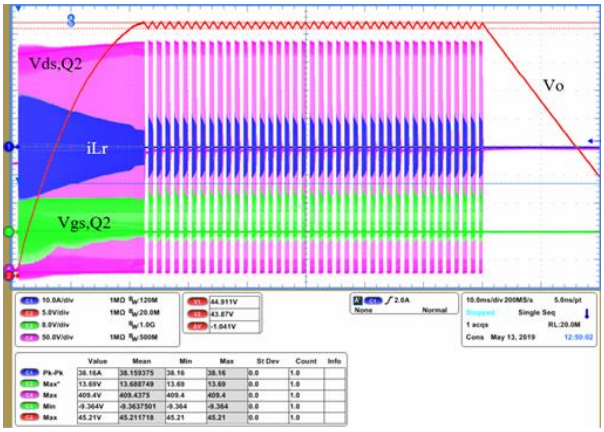

Figure 48. Burst mode. Start-up and stop at light load conditions: 4 A load, 400 V input and 43.5 V output.

Burst mode ensures that in every condition the HV MOSFETs operate under full or partial ZVS (Figure 49 and Figure 50) which reduces the power loss and maintains the smooth quasi resonant transitions of the drain and gate voltages (resulting in little or no overshoots and better EMI).

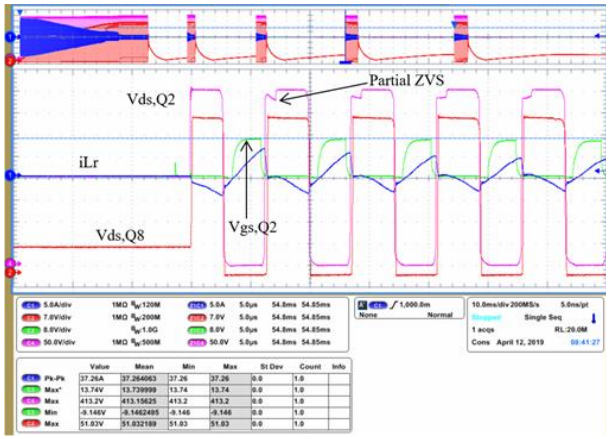

Figure 49. Burst mode. The resume of the switching happens in ZVS, without overshoot or current stress.

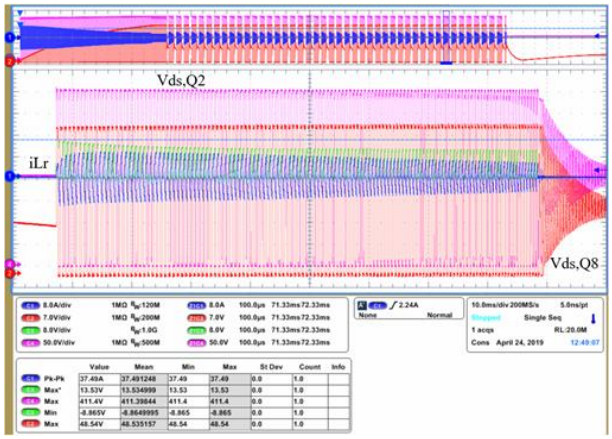

Figure 50. Burst mode. Full burst sequence. The resume of the switching happens in ZVS, without overshoot or current stress.

3.10. THERMAL MAP

The temperatures of the main components of the converter were already discussed in the previous sections. The following figures show the thermal distribution of the converter, from a bottom view (Figure 51) and from a top view (Figure 52), operating at full load and nominal conditions: 400 V input and 51.5 V output.

The hottest spot of the converter is the integrated magnetic structure. The distribution of components in the converter concentrates the losses of the secondary side MOSFETs, the transformer and the resonant inductance in a small area. Moreover, the open frame construction decreases the effectivity of the forced cooling solution.

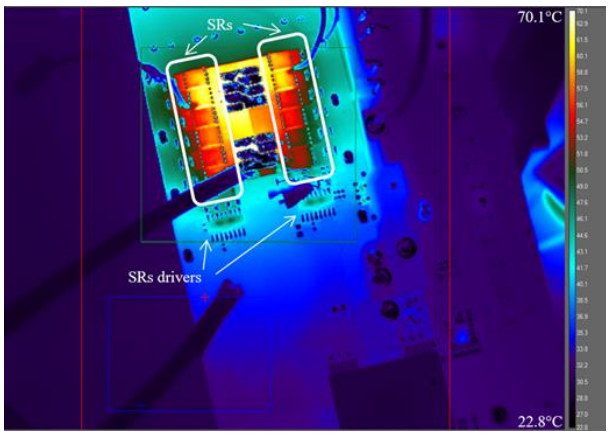

Figure 51. Thermal capture at 65 A load with open case and 25 °C ambient temperature. Bottom view.

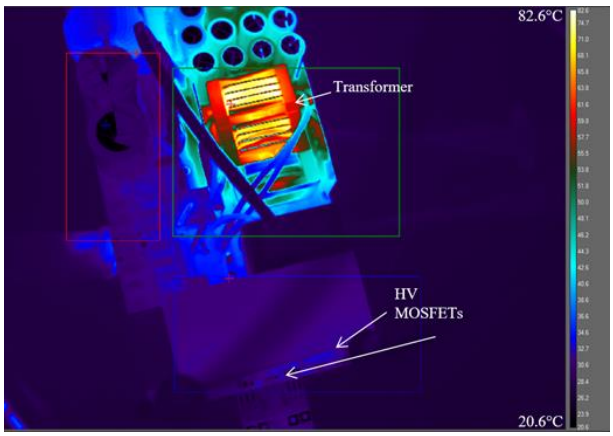

Figure 52. Thermal capture at 65 A load with open case and 25 °C ambient temperature. Top view.

4. USER INTERFACE

The controller includes serial communication interface (UART) and a proprietary protocol allowing the parametrization of the HV MOSFETs dead times, output voltage settings, protections activation/deactivation and monitoring of status. The user interface for Windows OS (Figure 53) is an example of the capabilities of the communication library included within the controller firmware. The user interface was specially developed for this work to communicate with the controller through the XMC™ Link (converts UART to USB), although other serial communication interfaces are also possible.

Finally, there are two available distinct main views of the GUI:

- Advanced user interface with parametrization capabilities of dead-times, output voltage, protections and working modes (Figure 53). The parameters can be adjusted during run-time of the converter.
- Simplified user interface intended only for monitoring the converter during run-time (Figure 54).

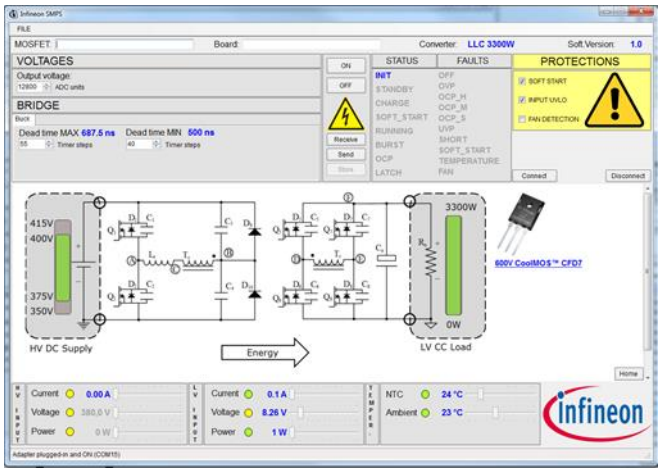

Figure 53. 3300 W LLC HB advanced user interface.

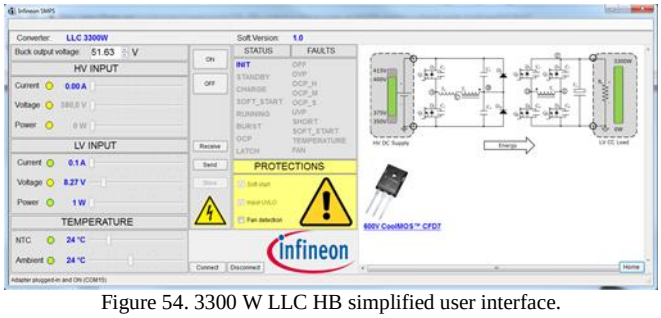

Figure 54. 3300 W LLC HB simplified user interface.

5. SCHEMATICS

The converter hardware is comprised of a main board and three separate daughter cards: a controller card, a driving card and an auxiliary on-board supply card [8]. Figure 55, Figure 56, Figure 57 represent the schematics of the main board, the driving card, and the control card. The auxiliary on-board supply in this converter is the same that was used in the converter in chapter 3, therefore it has not been duplicated here.

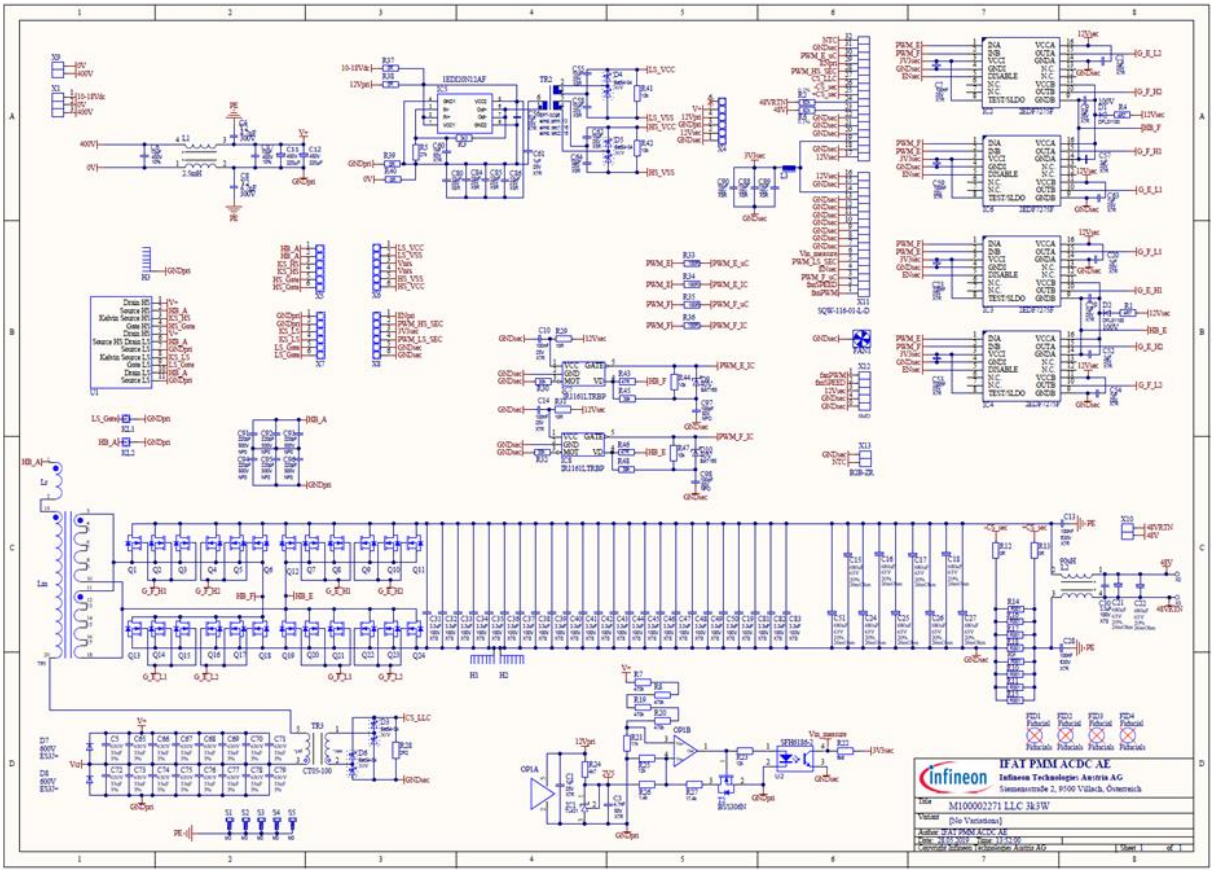

Figure 55. 3300 W HB LLC main board with IPW60R018CFD7 and BSC037N08NS5.

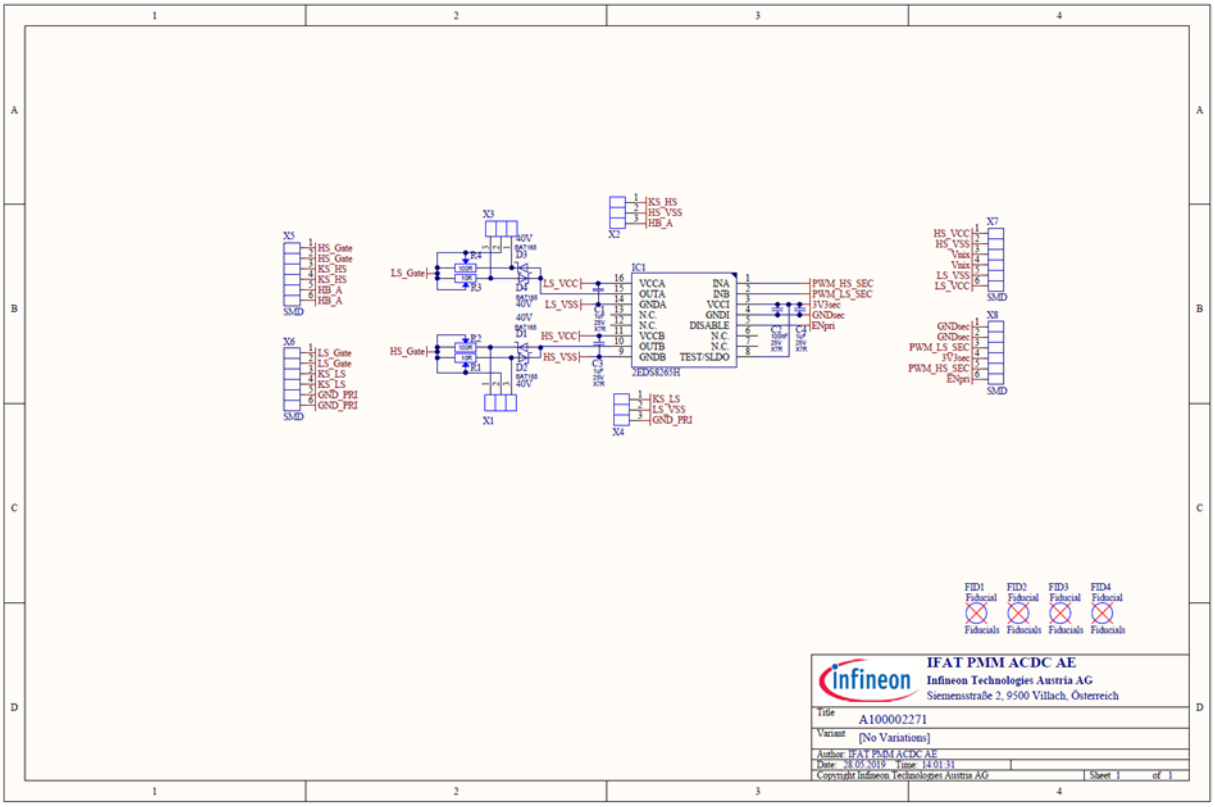

Figure 56. 3300 W HB LLC driver card with 2EDS8265H.

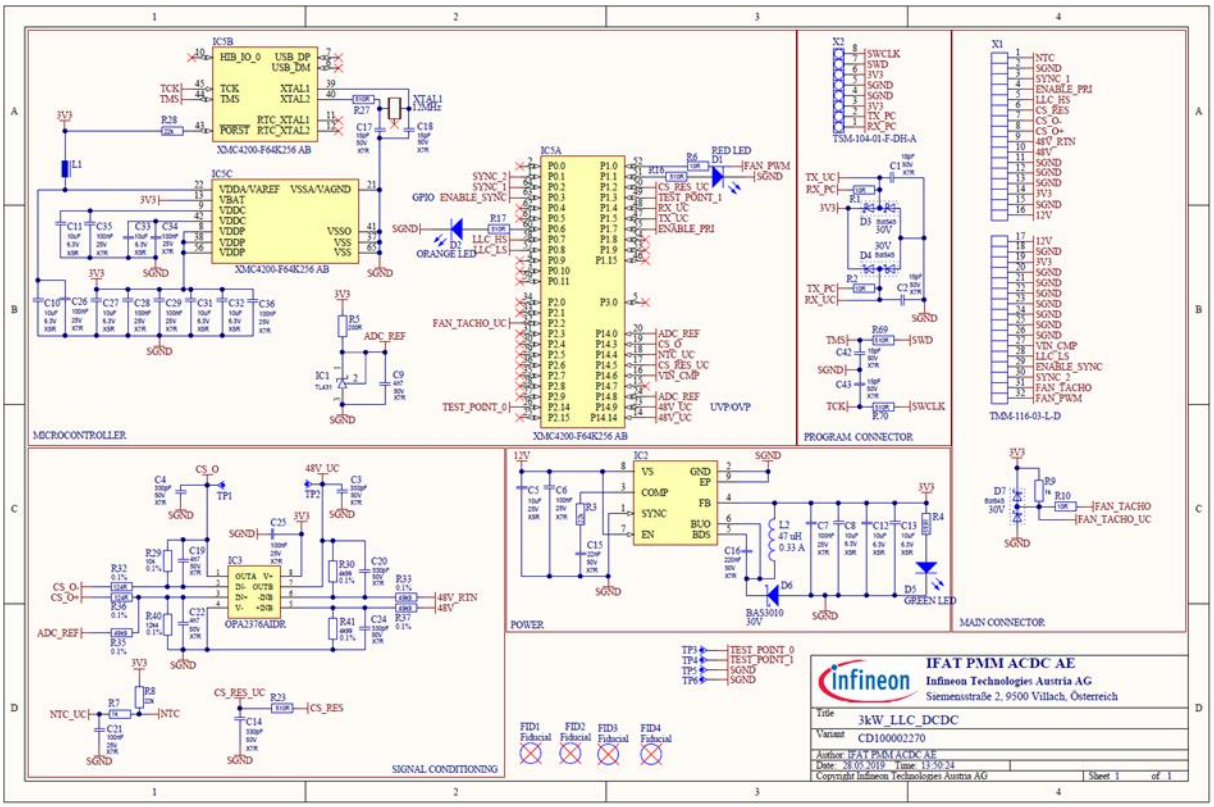

Figure 57. 3300 W HB LLC controller card with XMC4200-F64K256AB.

6. CONCLUSIONS

This chapter introduces a complete system solution for a 3300 W LLC DCDC converter from 400 V to 51.5 V achieving 98.1 % peak of efficiency. The achieved power density is in the range of 4 W/cm³ (66 W/in³) which is enabled by the use of SMD packages, the innovative stacked magnetic construction and the innovative cooling solution.

The optimized layout and an optimized driving circuitry achieves benchmark performance with minimum stress on the devices, enabled also by the innovative cooling concepts presented in this board. This DCDC converter proves the feasibility of the half-bridge LLC as a high-efficiency topology for a 3300 W converter, at the level of full-bridge LLC or dual stage LLC.

This DCDC converter also proves that digital control, powered by XMC™ Infineon microcontrollers, is not only capable of controlling the LLC topology but the most effective way to overcome its difficulties and pitfalls. Moreover, the included protections mechanisms and control schemes further boost the reliability and performance of the converter achieving the best possible efficiency.

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CHAPTER 6. SERVER AND DATACENTER 3 kW 50 V PSU

1. INTRODUCTION

Due to the increasing power demand in server and data center applications the requirements of power density and efficiency for the Power Supply Units raise continuously. This is due to the operational cost of the infrastructure: on the one hand the cost of the electricity and on the other hand the cost of the space and maintenance of the installations. Moreover, the high reliability demand in the server and data center applications has a severe impact in the hold-up requirements, which can be as large as 20 ms delivering full power.

These tendencies in power density, efficiency and reliability requirements can be observed in the newly released OCP rectifier V3 specifications for server and datacenter PSU [1]-[2]. The main changes in relation to the previous PSU specifications (Open Rack V1 and V2) are the higher requirements in terms of efficiency (97.5 % peak) and power density (1.96 W/cm³ or 32.15 W/inch³), together with the large hold-up time (20 ms at full power). Moreover, the maximum outer dimensions of the PSU are 520 mm x 73.5 mm x 40 mm. However, the output voltage has been increased to 50 V_{DC}, although still in a narrow range, which should help with achieving the challenging target specifications.

This chapter introduces a 3 kW power supply unit (PSU) targeting the newly released OCP rectifier V3 specifications for servers and data centers. The PSU comprises a front-end ACDC bridgeless totem pole converter followed by a back-end DCDC isolated half-bridge LLC converter. The front-end totem pole converter provides power factor correction (PFC) and total harmonic distortion (THD). The LLC converter provides safety isolation and a tightly regulated output voltage. Figure 1 shows a photograph of the PSU outside of its chassis.

The measured peak efficiency of the complete PSU at 230 V_{AC} is 97.5 %, not including the internal fan, and 97.4 %, including the internal fan. The overall outer dimensions of the PSU are 73.5 mm x 520 mm x 40 mm, which yields a power density in the range of 32 W/inch³ (1.95 W/cm³).

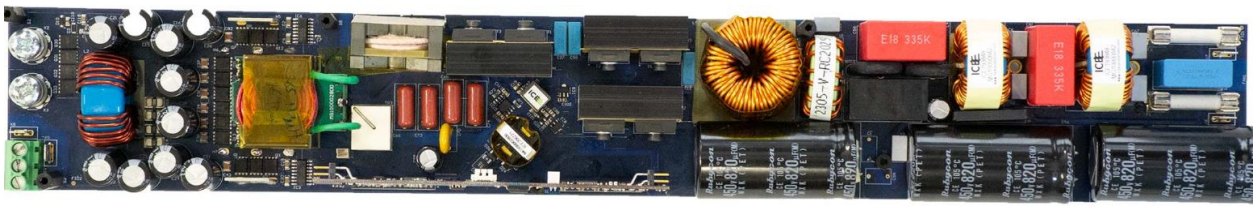

Figure 1. Photo of the EVAL_3KW_50V_PSU – outside of its chassis.

Table 1 and Figure 2 are a summary of the main specifications and requirements of the OCP V3 rectifier. A more detailed and complete specification can be found in [2].

Table 1. Summary of the requirements and specifications for the OCP rectifier V3 PSU [2]

Requirements	**Conditions**	**Specification**
Input voltage V_{in}	180 V_{AC} to 275 V_{AC}	230 V_{AC} nominal
Output voltage V_{ref}	50 V_{DC}	50 V_{DC} nominal
Output power	180 V_{AC} to 275 V_{AC}	3000 W
Efficiency peak	230 V_{AC} input, 50 V_{DC} output	η_{pk} = 97.5 % above 18 A (30 % of load)
Steady-state V_{out} ripple	230 V_{AC} input, 50 V_{DC} output	$\lvert\Delta V_{out}\rvert$ less than 200 mV_{pk-pk}
Power factor and THD	180 V_{AC} to 275 V_{AC}	EN/IEC 61000-3-2 and EN 60555-2
Input UVLO	175 V_{AC} on to 170 V_{AC} off	Digital hysteresis window comparator
Output UVLO, OVLO	V_{ref} ± 3 V	Shut-down and latch
Load transient	5 A ↔ 30 A, 1 A/µs	$\lvert\Delta V_{out}\rvert$ less than 1 V_{pk}
	30 A ↔ 60 A, 1 A/µs	
Over current protection	63 to 70 A	Shut-down and resume
	More than 70 A	Shut-down and latch
	Output terminals in short-circuit	Detection within switching period Shut-down and latch
ORing		Hot insertion/removal
Front-to-back air cooling		Intenally controlled variable-speed fan
Hold-up time		0 V for 20 ms

It is worth highlighting the very high efficiency requirements, where the peak efficiency should exceed 97.5 %, at some point between 40 % and 100 % of the rated load. Moreover, the efficiency shall be above 96.5 %, from 40 % to 100 % of the load, and above 94 %, between 10 % to 30 % of the load. Therefore, a typical efficiency curve of a compliant PSU will look somewhat similar to the plotted curves in Figure 2.

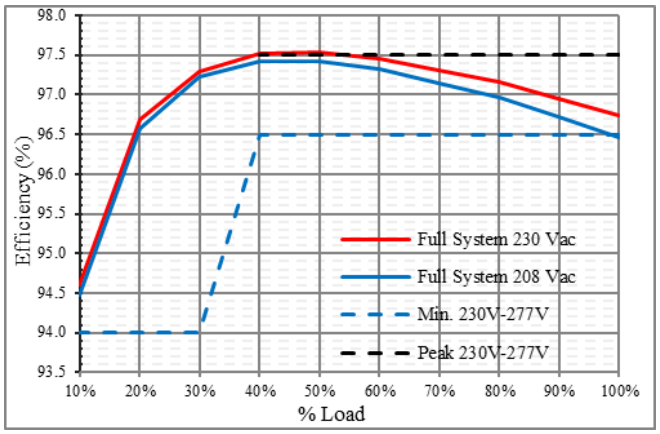

Figure 2. OCP rectifier V3 efficiency requirements at 230 V_{AC} and estimated efficiency curve of a compliant PSU.

The rest of this chapter describes the converter hardware, a summary of the experimental results and several design recommendations for the complete solution, also including the construction of an innovative planar magnetic construction.

2. SYSTEM DESCRIPTION

The PSU comprises two stages: a front-end bridgeless totem pole ACDC converter, which provides PFC and THD, followed by a half-bridge LLC DCDC converter that provides safety isolation and a tightly regulated output.

Figure 3 shows a very simplified diagram of the PSU, including the main power semiconductor switches, and the controllers and drivers of the two main conversion stages. While the PFC controller is located at one of the input V_{AC} rails, the LLC controller is referenced to the ground of the insulated output of the complete PSU. It is worth mentioning that the totem pole PFC and the LLC controllers are communicated via UART through the safety isolation barrier thanks to a digital isolator.

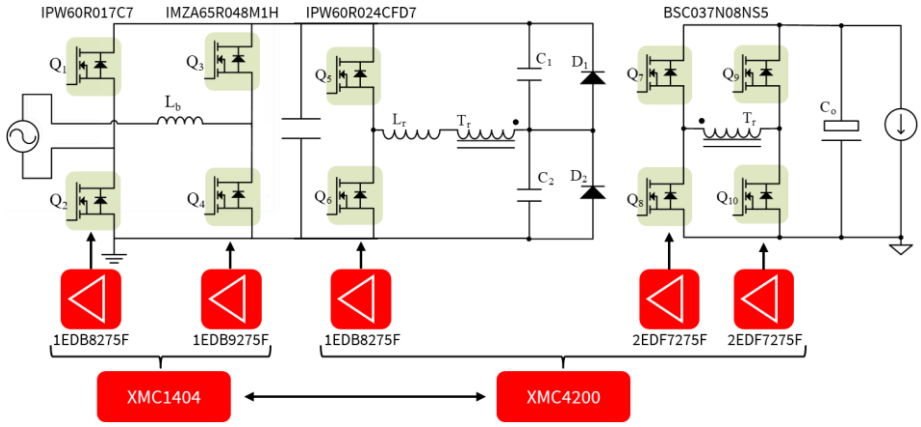

Figure 3. Simplified schematic of the prototype PSU. Front-end totem pole PFC followed by a half-bridge LLC resonant converter.

The control of the totem pole ACDC converter is implemented with a XMC1404 Infineon microcontroller, which includes PFC, THD, voltage regulation, input overcurrent protection (OCP), overvoltage protection (OVP), undervoltage protection (UVP), undervoltage lockout (UVLO), soft-start, SR control, adaptive dead-times (boosting half-bridge) and serial communication interface. Further details about the digital control implementation and additional functionalities of the totem pole control with the XMC1400 family can be found in [3].

The control of the half-bridge LLC is implemented with a XMC4200 Infineon microcontroller, which includes voltage regulation functionality, burst-mode operation, output OCP, OVP, UVP, UVLO, soft-start, SR control, adaptive dead-times (bridge and SRs) and serial communication interface. Further details about the digital control implementation and additional functionalities of the LLC control with the XMC4000 family can be found in [4].

In the following the two conforming blocks of the complete power supply would be studied and evaluated separately. Thereafter, the union of the two blocks would be validated experimentally.

2.1. BRIDGELESS TOTEM POLE PFC

The estimated efficiency of the totem pole PFC, part of the complete PSU, is plotted in Figure 4**.** It is worth noticing the very high peak efficiency, near 99 % at 50 % of the rated load.

The estimated overall distribution of losses of the the totem pole PFC converter at 230 V_{AC} and 50 % of the rated load is summarized in Figure 5. It can be observed that the main contributors to the losses are the half-bridge boosting switches (IMZA65R048M1H). In a totem pole PFC the boosting switches operate mostly in hard-commutation, explaining the relatively high switching loss. However, thanks to the small parasitic capacitances of the CoolSiC™ devices and the high switching speed achievable with the 4-pin packages, the converter can still achieve very high performance. On the other hand, the low temperature dependence of the CoolSiC™ $R_{ds,on}$ reduces the conduction loss at mid and full load, and at the lowest input voltages (where the conduction loss dominates) [5].

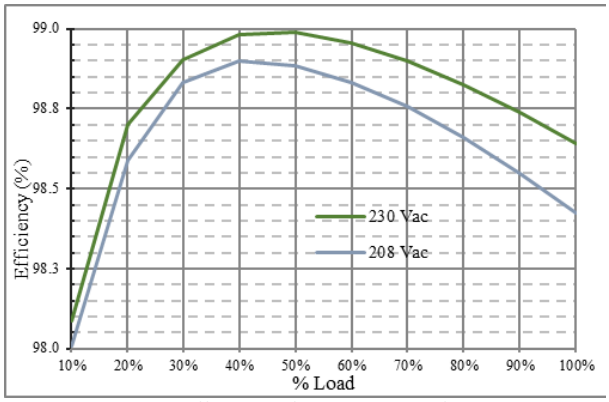

Figure 4. Estimated efficiency of the totem pole front-end ACDC converter.

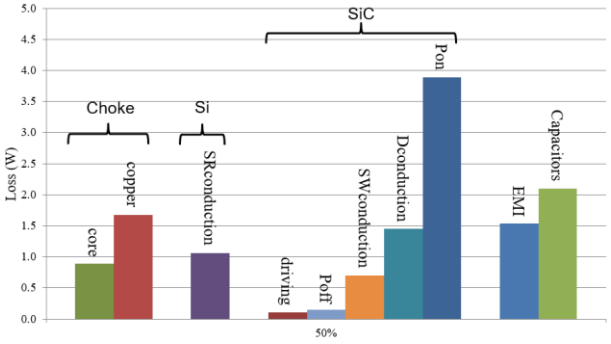

Figure 5. Estimated overall distribution of loss in the totem pole PFC at 230 V_{AC} and 50 % of the load.

2.1.1. TOTEM POLE PFC MAGNETICS

The other main contributors to the losses to consider in the design of the totem pole ACDC converter are the main inductor and the EMI filter. The main inductor of this design is made of two stacked toroidal cores from Chang Sung: one CH330060GT and one CH330060GT14. The winding is made of 62 turns of AWG 15 insulated solid copper wire, with a total inductance of 539 µH at no load, and of approximately 271 µH at full load and 230 V_{AC}. Figure 6 shows a simplified diagram of the recommended construction technique for the main boost inductor, in order to minimize unwanted parasitic capacitances.

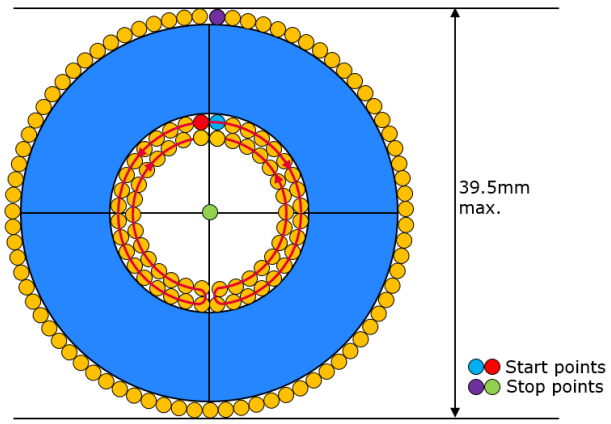

Figure 6. Simplfied recommended building instructions for the main boost inductor.

2.2. HALF-BRIDGE LLC

The estimated efficiency of the redesigned half-bridge LLC converter part of the complete PSU is plotted in Figure 7. It is worth mentioning the very high peak efficiency, near 98.5 % at 50 % of the rated load. Note that the overall efficiency of the complete PSU is the result of multiplying the separate efficiencies of the conforming blocks, and is necessarily lower than any of them separately. However, some of the loss contributions are shared between the two blocks (e.g., auxiliary bias) and therefore, the resulting overall efficiency is still expected to fall withing the target specifications.

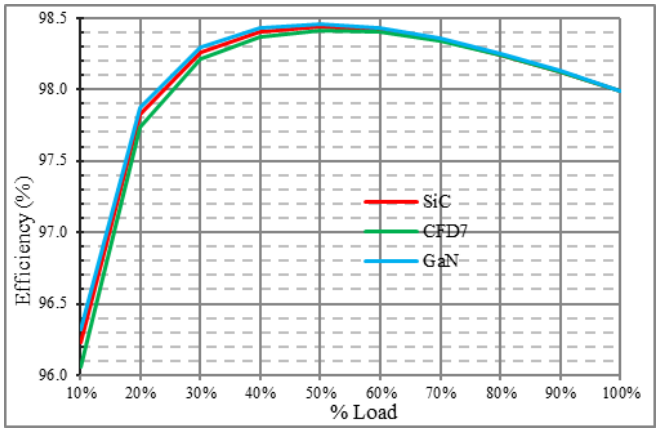

Figure 7. Estimated efficiency of the back-end LLC DCDC converter.

The estimated overall distribution of losses of the LLC DCDC converter at 410 V_{DC} and 50 % of the rated load is summarized in Figure 8. It can be observed that the main contributors to losses are the main transformer, followed by the SRs and the primary-side half-bridge MOSFETs. Moreover, it is worth highlighting that the switching and driving losses comprise a large portion of the total losses, and therefore the optimal series resonant frequency of this converter was found to be a relatively low 93 kHz. On the other hand, the analysis shows that even at this low switching frequency the wide-bandgap (WBG) alternatives provide improved efficiency, especially noticeable at mid and light loads.

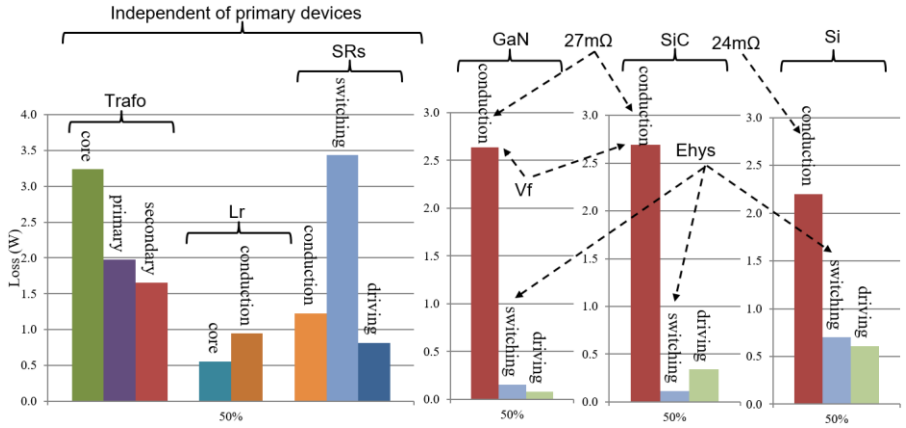

Figure 8. Estimated overall distribution of loss of the back-end LLC DCDC converter at 50 % load.

2.2.1. HALF-BRIDGE LLC MAGNETICS

The resonant tank of the half-bridge LLC series-parallel resonant converter comprises two equivalent inductors and one equivalent capacitor (hence its name). However, one of the advantages of this topology is that it is possible to realize the series resonant inductor (L_r) by the leakage of the main transformer, and the parallel resonant inductor (L_m) by the magnetizing inductance of the main transformer. Nevertheless, that integration approach constrains the design and compromises the performance of the converter. Therefore, in the PSU object of this work the series inductor (L_r) and the parallel inductor (L_m) are realized as discrete components, although L_m is integrated within the same structure of the main transformer.

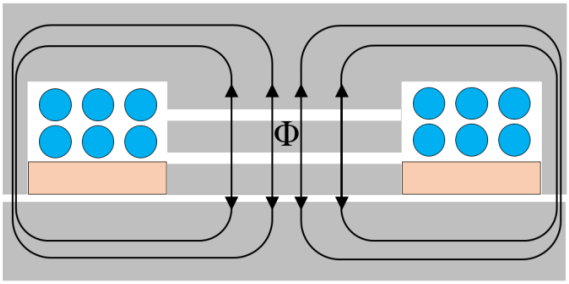

Figure 9. Simplified construction of the series resonant inductor of the LLC DCDC converter.

Figure 9 shows a simplified view of the construction of the series inductor (L_r). L_r is built with a PC95 PQ35/13 DG core and a PQI35 core from TDK. The distributed gap helps reduce the losses caused by the stray magnetic

fields in the winding itself and the surrounding conductors (in the main board and the chassis). Moreover, a spacer maintains the windings away from three of the gaps.

The winding is made of six turns of Litz wire with 245 strands of 0.1 mm diameter.

Figure 10 shows a simplified view of the construction of the parallel inductor (L_m) and the main transformer. The parallel inductor is built with a PC95 PQ35/28 core from TDK, while the main transformer is built with two PC95 PQI35/23 cores from TDK. The L_m is stacked on top of the main transformer and wound in the same direction as the primary-side winding. As a result of this, the flux in part of the volume is effectively cancelled and the total core loss is partly reduced. On the other hand, the magnetizing inductance of the main transformer can be made arbitrarily high, which contributes to the reduction of proximity loss and other loss caused by stray magnetic fields.

The winding of the L_m is made of 16 turns of Litz wire with 512 strands of 0.05 mm diameter. The main transformer windings are made of planar copper conductors built-in independent PCBs for the primary and for the secondary. The proposed construction is highly flexible and modular. The proposed interleaving realized in the PSU is demonstrated in Figure 10 and Figure 11. It is worth mentioning that the transformer turn ratio is 16 to 4. Each of the primary-side winding PCBs (in blue in Figure 11) comprises eight turns while each of the secondary-side winding PCBs (in green in Figure 11) comprises four turns.

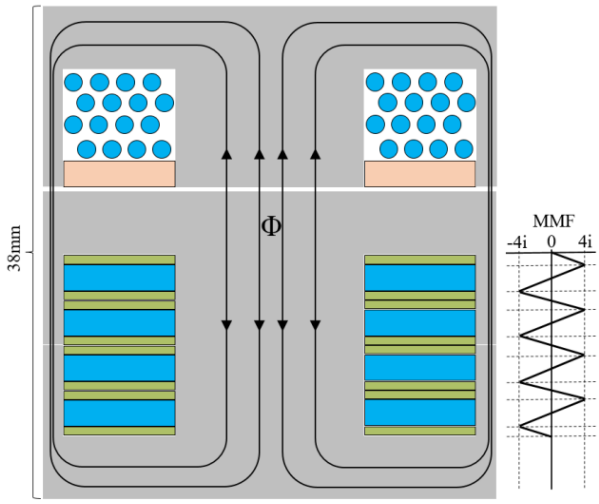

Figure 10. Simplified construction of the integrated transformer plus the parallel resonant inductor of the LLC DCDC converter.

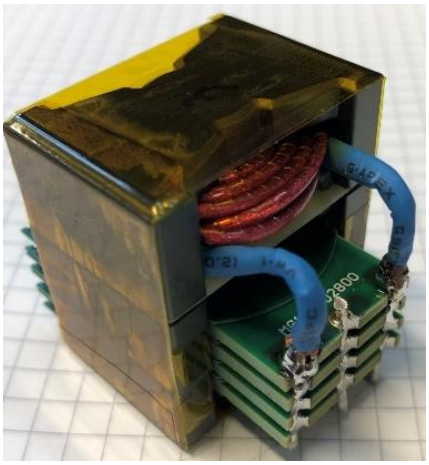

Figure 11. Photo of the assembled integrated structure of the transformer plus the parallel resonant inductor.

Due to the height limitation of the PSU (40 mm) the main board needs to be cut out to accommodate the height of the integrated L_m plus the main transformer structure (approximately 38 mm).

3. EXPERIMENTAL RESULTS

This section is a summary of the main experimental results of each of the conforming blocks separately (totem pole PFC and half-bridge LLC), and of the complete PSU.

3.1. TOTEM POLE PFC

In the bridgeless totem pole ACDC converter the boosting half-bridge operates mostly in hard-commutation. Therefore, the switching loss depends on the switching speed of the devices, i.e. the longer the overlap of voltage and current, the higher the loss. For this purpose, the 4-pin TO-247 package with Kelvin source connection helps by removing the negative feedback caused by the power source during the switching transients and making the device switch faster. On the other hand, the switching speed of the devices shall be controlled to avoid excessive drain voltage overshoot and gate ringing, which can be achieved with a properly dimensioned external gate resistor.

Figure 12 is an example of the drain voltage overshoot and gate ringing in the boosting half-bridge of the totem pole PFC. Both the drain voltage and the gate voltage have been measured referenced to the Kelvin source connection. It can be observed that the maximum drain overshoot is 487 V, well within the rated limits of the devices.

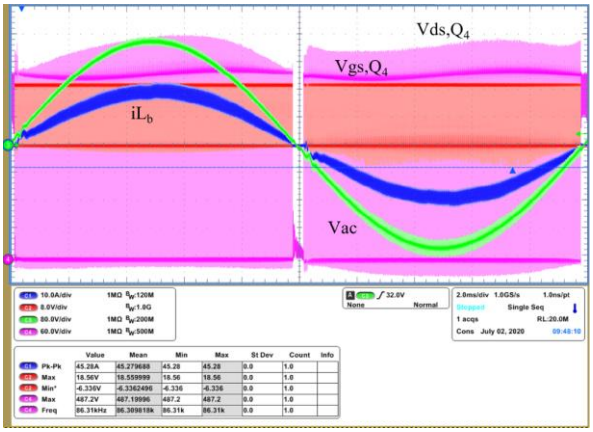

Figure 12. PFC drain voltage overshoot and gate ringing at full load.

3.1.1. BOOST DIODE OPERATION

The devices in the boosting half-bridge of the totem pole ACDC converter operate alternately as the boost converter diode and the boost converter switch. The modes alternate at twice the V_{AC} frequency.

The switching transients are clearly different while the device operates as a diode or as a switch. During operation as a diode, the device is zero voltage switched (ZVS) both at turn-on and turn-off. After the opposite boost switch turns off, the inductor current freewheels to the intrinsic body diode of the boost diode device. After an idle time (dead-time) the device switches on in ZVS (Figure 13) and the current passes through the channel of the device (instead of its instrinsic body diode).

After the boost diode device switches off in ZVS, the current continues to freewheel through its intrinsic body diode. After the corresponding idle time (dead-time) the opposite boost switch hard-switches on and hard-commutates the boost diode, which can be identified by instant where the V_{DS} rises in Figure 14.

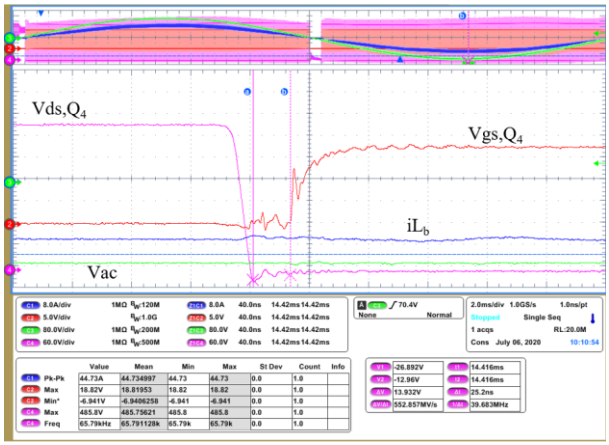

Figure 13. ZVS switch-on of the boost diode.

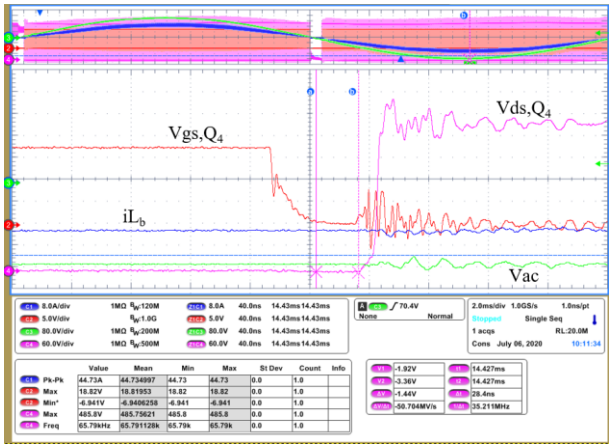

Figure 14. ZVS switch-off of the boost diode followed by its hard-commutation caused by the hard-switching on of the opposite boost switch.

3.1.2. BOOST SWITCH OPERATION

Unlike the diode operation, the boost switch operation is hard-switched during most of the V_{AC} cycle and along most of the load range. Only when the current ripple through the inductor is at least twice as large as the average current can both the diode and the switch operate in ZVS.

Figure 15 shows a hard-switched turn-off transition of the boost switch. During the hard-switched turn-off transition the *dv/dt* and the V_{DS} overshoot can be controlled with an external gate resistor.

Figure 16 shows a hard-switched turn-on transition of the boost switch (hard-commutation of the opposite boost diode). The device is not only hard-switching turn-on but also hard-commutating the opposite diode, hence the need to use low Q_{rr} devices in the boosting half-bridge of the totem pole ACDC converter.

Like during the hard-switched turn-off transition, the *dv/dt* and the gate ringing can be controlled with an external gate resistor.

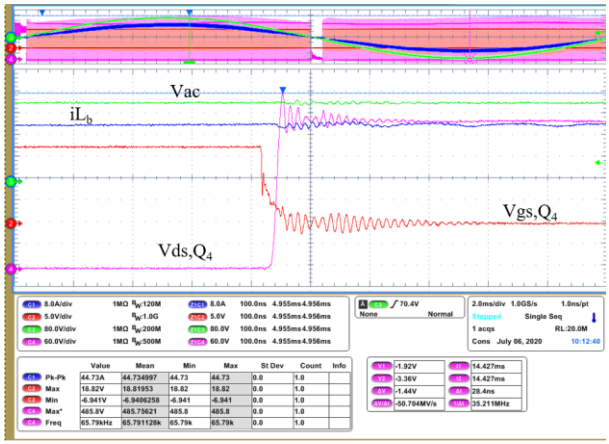

Figure 15. Hard-switched turn-off of the boost switch.

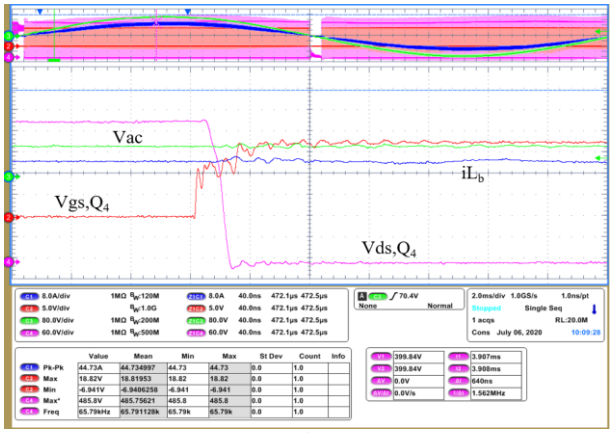

Figure 16. Hard-swiched turn-on of the boost switch and hard-commutation of the boost diode.

3.1.3. SRS POLARITY DETECTIONS

Totem pole rectification can be implemented with diodes or with SRs. The SRs are only switching at twice the V_{AC} frequency, and they are normally zero current switched (ZCS). Therefore, the SRs can be implemented with very low-ohmic devices for best performance of the converter.

The SRs are normally switched around the V_{AC} crossing, with a certain idle window near the zero crossing (Figure 17). Moreover, this window is preferably narrow for best THD.

The implemented control can recognize an incorrect polarity detection of the SRs, turn them off and restart the next V_{AC} semi-cycle normally. In Figure 18 it can be observed how the V_{AC} oscillation, after the V_{AC} is lost, causes the wrong polarity to be detected by the control. Nevertheless, it is noticeable that the control has recognized the wrong polarity and turns off the switches safely.

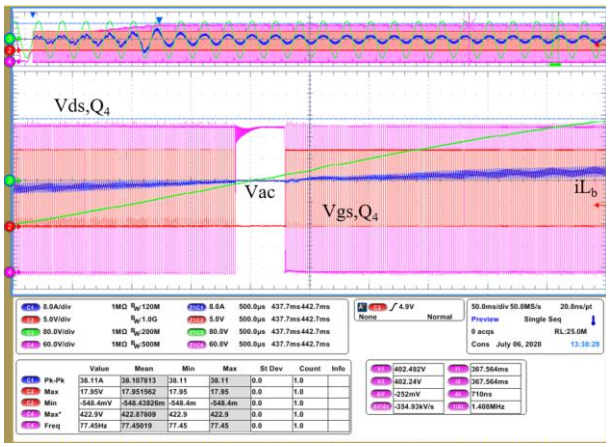

Figure 17. Detailed view of the V_{AC} zero crossing in the PFC totem pole.

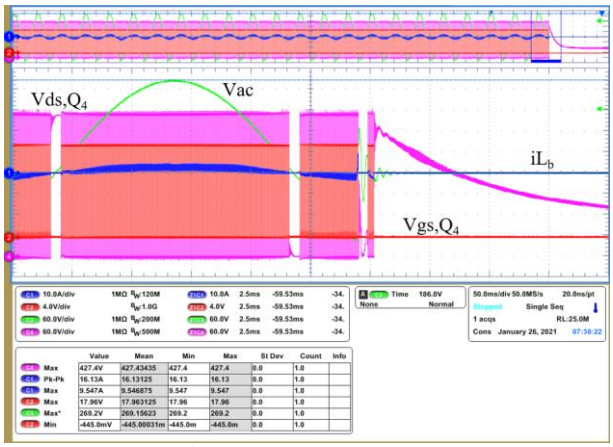

Figure 18. Filtering of V_{AC} polarity during V_{AC} loss.

3.1.4. SOFT-START

During soft-start the totem pole ACDC converter has to charge-up the bulk capacitance to the steady-state voltage (410 V_{DC}). At 380 V_{DC} the back-end DCDC converter starts up and the totem pole ACDC converter must then provide the load power plus the remaining bulk voltage charge-up.

Figure 19 shows the soft-start sequence of the totem pole PFC at 10 A load. The start-up of the back-end DCDC converter is visible in the current of the PFC, near the end of the ramp-up of the voltage, with an increase due to the charge of the output capacitance of the DCDC converter itself.

Figure 20 shows the start-up of the totem pole PFC at the minimum rated input voltage (180 V_{AC}) and at 55 A load. The start-up of the DCDC converter can also be observed by the increase in the sinusoidal current near the end of the ramping-up of the bulk voltage, which afterward goes into steady-state at near full power.

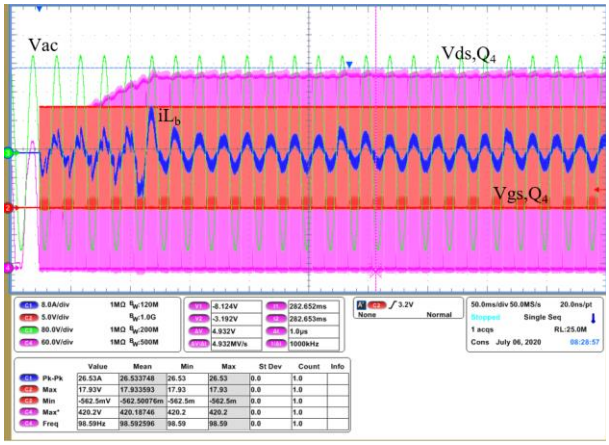

Figure 19. Soft-start sequence of the totem pole PFC at 180 V_{AC} and 10 A load.

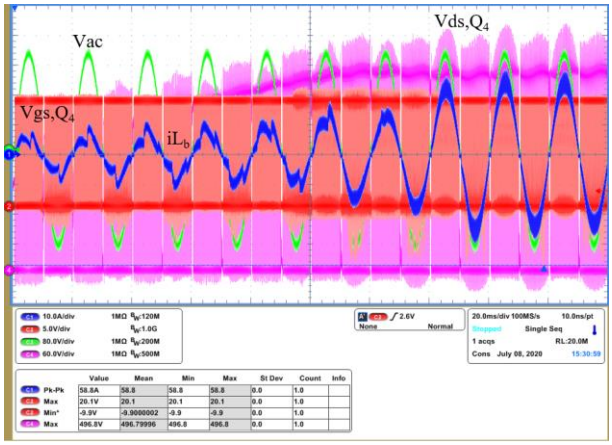

Figure 20. Soft-start sequence of the totem pole PFC at 180 V_{AC} and 55 A load.

3.2. HALF-BRIDGE LLC

The half-bridge LLC can achieve ZVS turn-on in the primary-side half-bridge along all the load range. On the other hand, the turn-off is hard-switched. However, if the *dv/dt* is not limited by the device during the resonant transition, the turn-off transition becomes lossless [6]. Figure 21 shows the ZVS turn-on and the lossless turn-off of the half-bridge LLC at 10 % of the rated load – the lack of Miller plateau can be observed during the turn-on transition and also during the turn-off transition.

The half-bridge LLC converter operates slightly above the series resonance in nominal conditions. Therefore, it operates in buck mode, near the normalized unity gain, where the converter achieves its highest efficiency. Figure 22 shows the primary-side reflected load current on top of the parallel inductor current. Because the main transformer magnetizing inductor is very large (approximately 1 mH) the magnetizing inductance contribution to the primary-side current can be safely ignored.

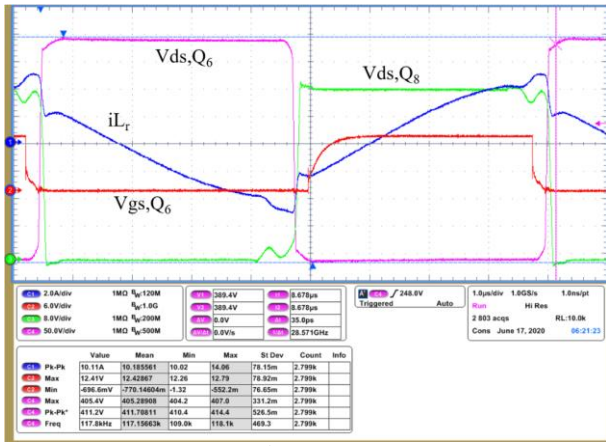

Figure 21. Full ZVS at 10 % of the rated load.

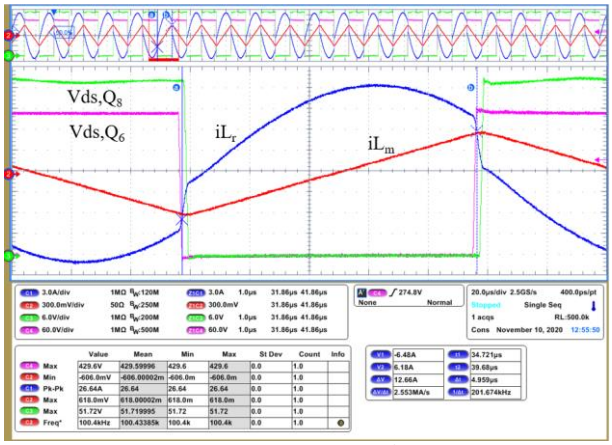

Figure 22. Steady-state operation at 50 % of the rated load and at 410 V input voltage.

The secondary-side SRs in the LLC converter are ZVS switched on and ZVS switched off. The gate driving voltage of the SRs can be observed in Figure 23. It should be noted that the SRs' gate driving voltage is 8.5 V to minimize the gate driving losses without much effect on their effective $R_{ds,on}$.

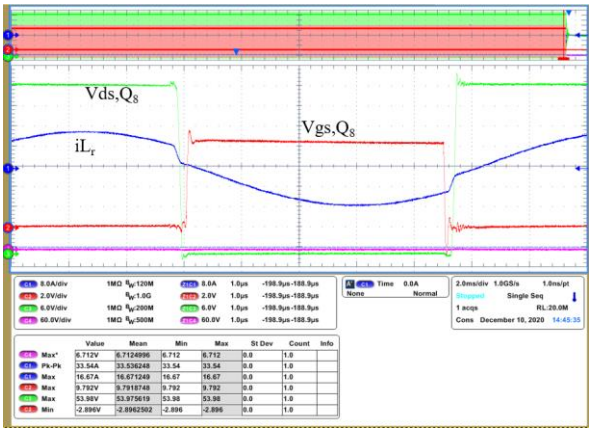

Figure 23. SRs gate driving at 40 A load and 410 V input voltage.

3.2.1. ZVS SWITCHING

Figure 24 and Figure 25 offer a more detailed view of the ZVS turn-on and the lossless hard-switched turn-off transitions of the primary-side half-bridge. Note the very low overshoot of the SRs' drain voltage, i.e. 52.64 V in Figure 25**,** well below the maximum rated voltage of the selected devices (80 V device class).

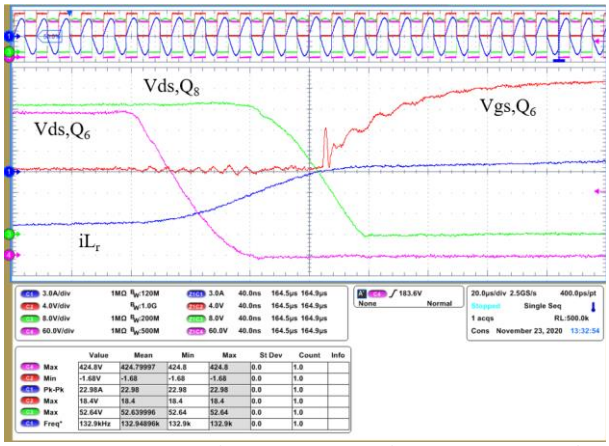

Figure 24. Detail view of the ZVS turn-on of the primary-side half-bridge.

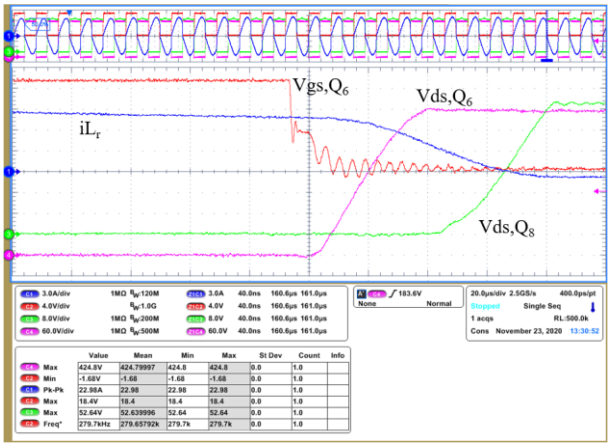

Figure 25. Detail view of the lossless hard-switched turn-off of the primary-side half-bridge.

3.2.2. SOFT-START

The start-up sequence is normally one of the most stressful operation modes for the semiconductor devices in the half-bridge LLC converter. During the start-up sequence the converter has to charge up the output capacitance of the converter, which causes high peak currents during the hard-swiched turn-off transition. Therefore, the highest drain voltage overshoots and ringing in the gate appear during this operation mode, which can be reduced by controlling the switching speed of the devices with external gate resistors.

The monotonic rising output voltage of the converter can be observed in Figure 26**.**

The control of the LLC converter should ensure no hard-commutation occurs in the primary-side devices during the start-up sequence. Because the discharged output capacitors behave virtually as a short-circuit, the first pulses during the start-up sequence are at a much higher frequency (Figure 27).

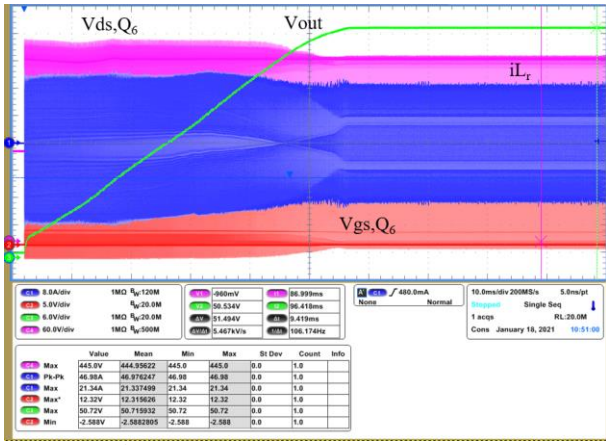

Figure 26. Soft-start sequence at 40 A load.

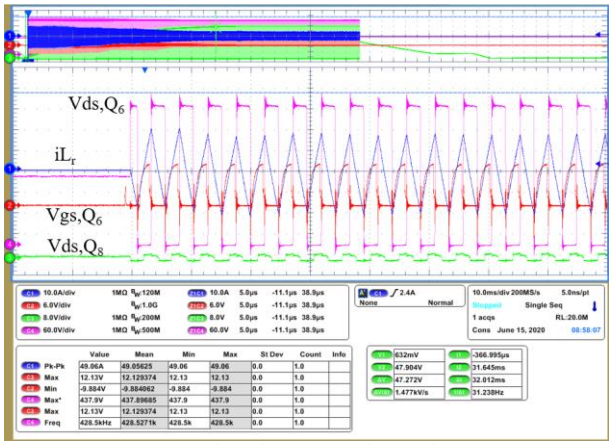

Figure 27. Detail view of the first pulses of the soft-start sequence.

Because of the split-capacitor configuration of the half-bridge LLC converter, the mid-point of the primary-side half-bridge is charged up to half of the bulk voltage prior to the very first pulse. Thanks to this, the very first hard-switched turn-on pulse is only hard-switching half of the input voltage. This explains the very low overshoot seen in the first hard-switched on transition (Figure 28).

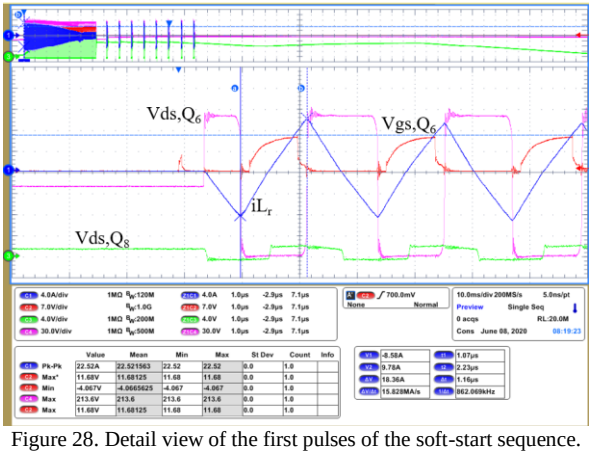

Figure 28. Detail view of the first pulses of the soft-start sequence.

3.2.3. OUTPUT VOLTAGE RIPPLE

At the output of the designed LLC converter there is an additional inductor that forms a CLC filter, which helps reduce the output voltage ripple of the converter, as well as the common-mode noise injected into the output. The high-frequency ripple is within 230 mV peak-to-peak in steady-state and at full load (Figure 29).

During the dynamic load jumps the peak-to-peak voltage variation is approximately 1.4 V for a 50 % load jump, which falls within less than ±2 % of the nominal output voltage (50 V_{DC}). Moreover, the settling time is in the order of 2.5 ms (Figure 30) and with a good margin of phase, in accordance with the observable step response.

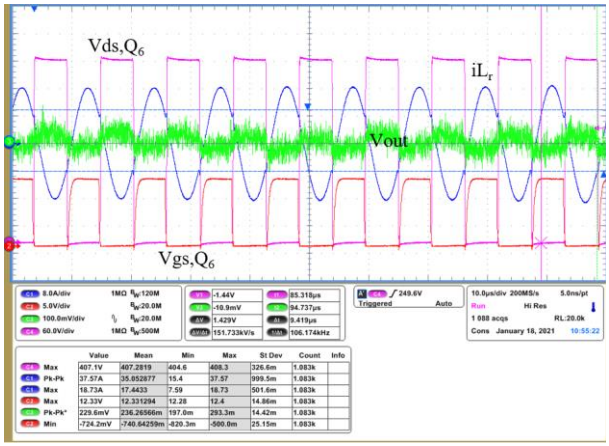

Figure 29. Output voltage ripple at full load.

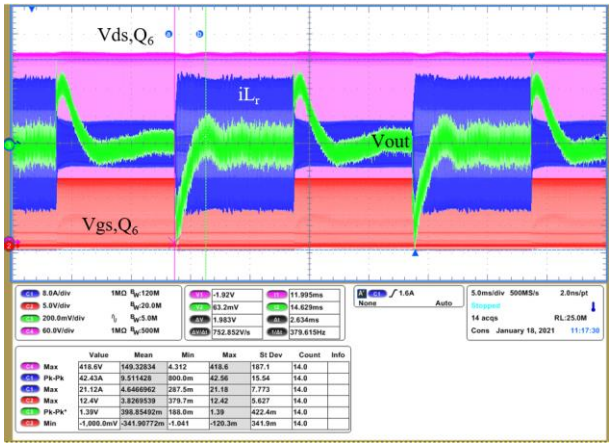

Figure 30. Dynamic load jump 10 A load to 40 A load, 1 A/µs, 100 Hz.

3.2.4. RESONANT CAPACITOR VOLTAGE

It is well known that while the clamping diodes provide overcurrent and overload protection to the LLC converter, they also limit the maximum voltage excursion possible in the split resonant capacitors. Furthermore, as the input voltage decreases, e.g., during hold-up time, the clamping voltage decreases as well. Therefore, it should be taken into account, during the design, that the maximum available gain of the converter will be limited by the clamping diodes during the hold-up time and the resonant capacitors should be dimensioned accordingly.

Alternatively, the clamping diodes can be removed from the circuit, although other overload and overcurrent mechanisms should be then considered. Figure 31 shows the peak-to-peak voltage excursion of the resonant capacitor being clamped when the input voltage falls down to 300 V_{DC}.

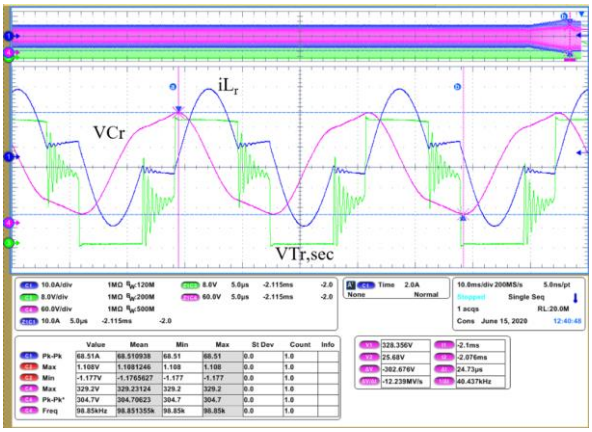

Figure 31. Clamping diodes limit the maximum V_{Cr} voltage amplitude, and therefore the gain of the converter.

3.3. POWER SUPPLY UNIT

This section provides a summary of experimental results of the complete power supply. Figure 32 and Figure 33 show the soft-start and brown-out sequences of the LLC integrated into the complete power supply. Unlike in Figure 26**,** the superimposed ripple in the bulk voltage due to the PFC operation can be seen.

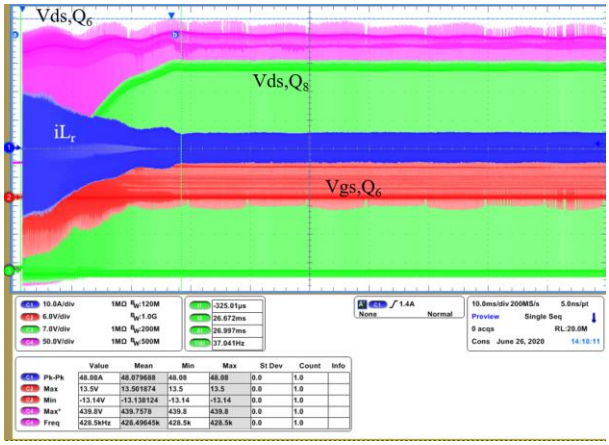

Figure 32. Soft-start sequence of the LLC converter at 10 A load while integrated into the complete PSU.

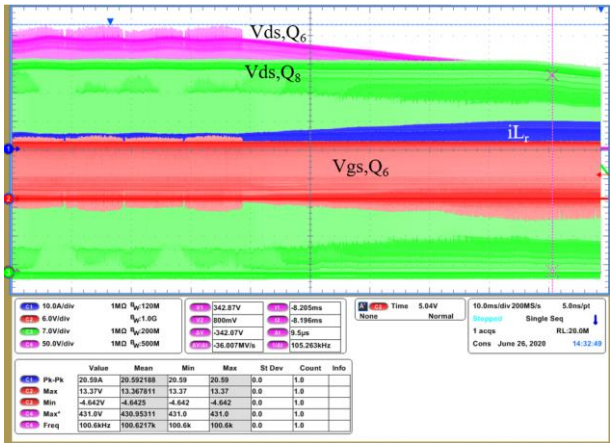

Figure 33. Brown-out sequence of the LLC converter at 10 A load while integrated into the complete PSU.

3.3.1. HOLD-UP TIME

The OCP V3 specifications require up to 20 ms hold-up time at full power, although the output voltage of the PSU is allowed to drop down to 48 V_{DC}. It is worth mentioning that the Rack & Power specifications include a battery unit at the rack level, which continues to provide power to the system at 48 V_{DC} if the V_{AC}, and therefore the PSU output voltage, is missing.

Figure 34 shows a capture of the response totem pole PFC and the output voltage of the PSU during a 20 ms hold-up time at full power. Meanwhile Figure 35 shows a capture of the response of the totem pole and the PSU during a 20 ms hold-up time at full power repeteadly.

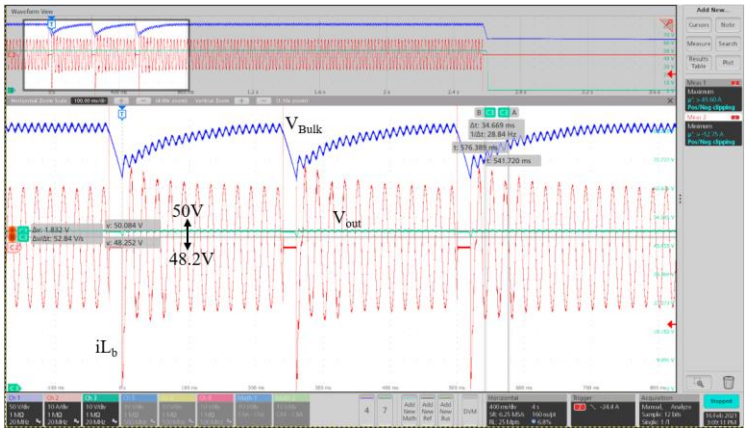

Figure 34. Detail view of 20 ms hold-up time at 60 A load and 230 V_{AC}.

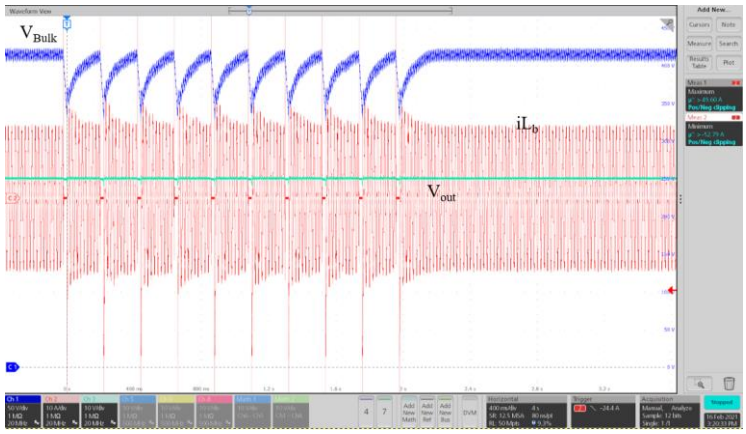

Figure 35. 20 ms hold-up time at 60 A load and 230 V_{AC}. Ten times sequence at 200 ms intervals.

3.3.2. TEMPERATURE

The temperature of the converter has been measured outside and inside of its chassis. The temperature image in Figure 36, captured with the PSU outside of its chassis, enables identification of the main hot-spots within the converter, which happen also to be the main sources of losses, discussed earlier in this document. More specifically, we can identify in the lower-left corner the main transformer and the secondary-side SRs, and in the upper-right corner the boosting half-bridge of the totem pole PFC.

The temperature of the identified hot-spots was also measured at the minimum input voltage (180 V_{AC}) and with the PSU enclosed in the chassis and the internal fan supplied by the internal auxiliary bias. The measured temperatures, registered after running the converter for 30 minutes at full load, have been plotted in Figure 37.

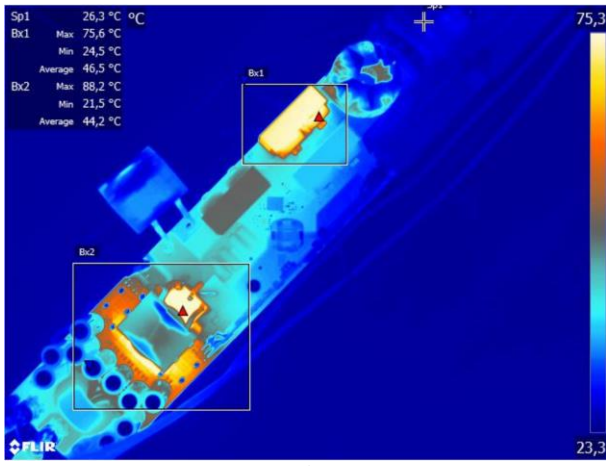

Figure 36. Measured temperature of the complete power supply prototype at full load, 230 V_{AC} and outside of its chassis.

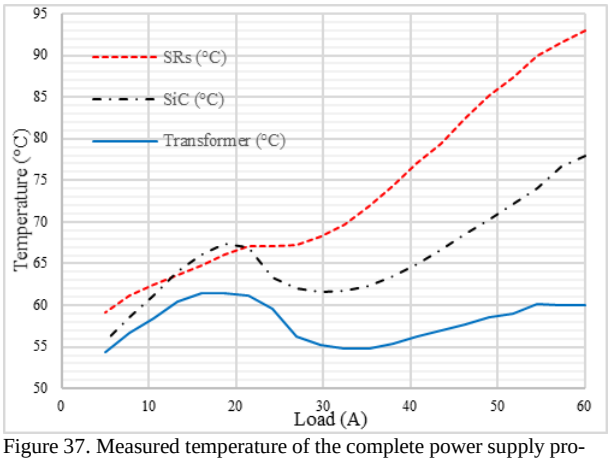

Figure 37. Measured temperature of the complete power supply prototype at full load, 180 V_{AC} and inside of its chassis.

3.3.3. EFFICIENCY

The efficiency of the complete power supply has been measured after running the converter for 30 minutes at full load. While the peak efficiency of the PSU not including the internal fan reaches 97.5 %, it falls down to 97.47 % when the consumption of the internal fan is also included (as required by OCP V3). Therefore, the overall efficiency of the PSU is slightly under the target specifications at the 230 V input voltage.

On the other hand, at full load the efficiency is also slightly under the requirements (Figure 38). However, at lighter loads the measurements exceed the limits by some margin.

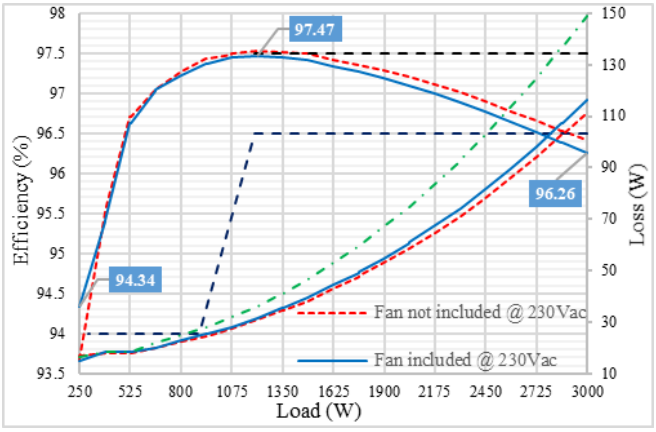

Figure 38. Measured efficiency of the complete power supply prototype at 230 V_{AC}.

3.3.4. POWER FACTOR AND THD

The power factor and THD have been measured at several input voltages within the input voltage range specifications. In accordance with these measurements the PSU complies with both the PF (Figure 39) and the THD (Figure 40) requirements of the OCP V3 specifications.

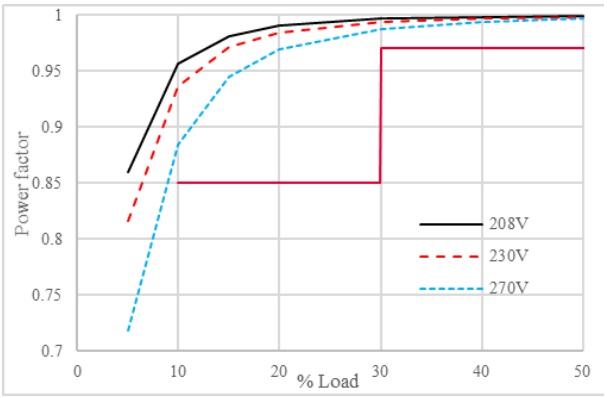

Figure 39. Measured PF of the complete power supply prototype at several input voltages. The specification limits are shown in red.

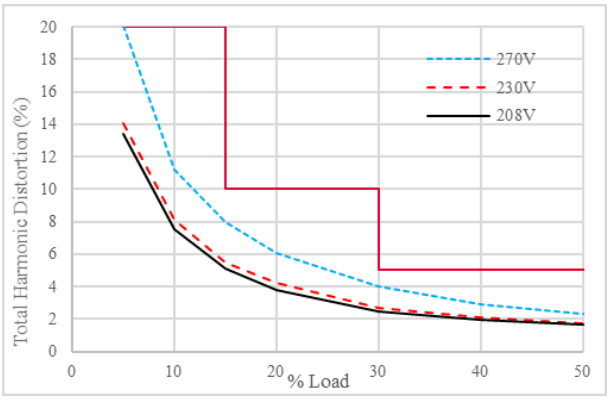

Figure 40. Measured THD of the complete power supply at several input voltages. The specification limits are shown in red.

3.3.5. EMI

Finally, the conducted electromagnetic interference (EMI) of the converter has been measured operating at 2.5 kW of load with a passive resistive load. Figure 41 and Figure 42 show the results of the average, the peak and the quasi-peak measurements. While the peak measurement touches the quasi-peak limit at some frequencies (blue curve in Figure 41), when measuring the quasi-peak (blue waveform in Figure 42), a very wide margin of more than 10 dB can be observed. Moreover, a wide margin of more than 10 dB can also be observed for the average measurement (green curve in Figure 41 and Figure 42).

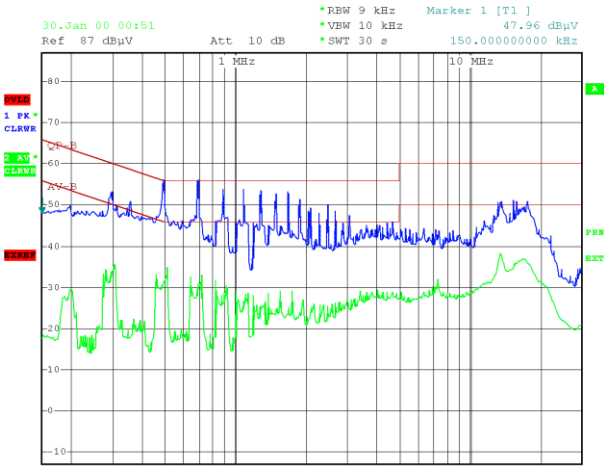

Figure 41. Measured EMI spectrum of the complete power supply prototype at 230 V_{AC} and 2.5 kW. Peak is shown in blue and average in green.

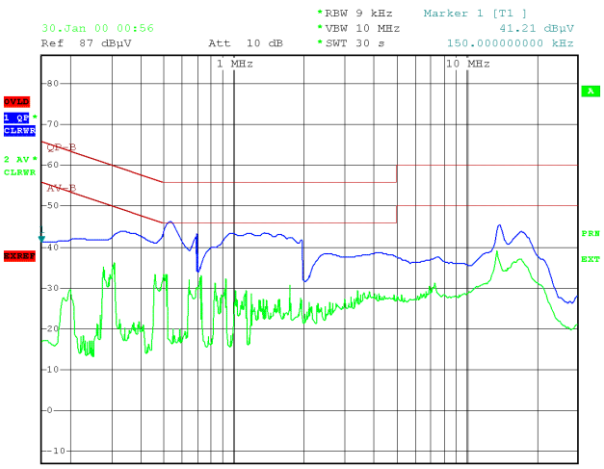

Figure 42. Measured EMI spectrum of the complete power supply prototype at 230 V_{AC} and 2.5 kW. Quasi-peak is shown in blue and average in green.

4. DESIGN TIPS

This section gives a summary of several features worth mentioning with regard to the hardware design of the PSU attaining the power semiconductors.

4.1. DRIVING 4-PIN COOLSIC™

For the best performance of the boosting half-bridge of the totem pole ACDC converter the use of devices in 4-pin packages with Kelvin source connection is recommended. The Kelvin source connection diminishes the negative feedback in the driving loop caused by the power source path, reducing the switching losses in hard-switched or hard-commutated topologies.

For the driving of the CoolSiC™ MOSFETs the recommended driver is the 1EDB9275F, which is a single-channel driver with a 14.4 V UVLO, specially designed for CoolSiC™ (Figure 43).

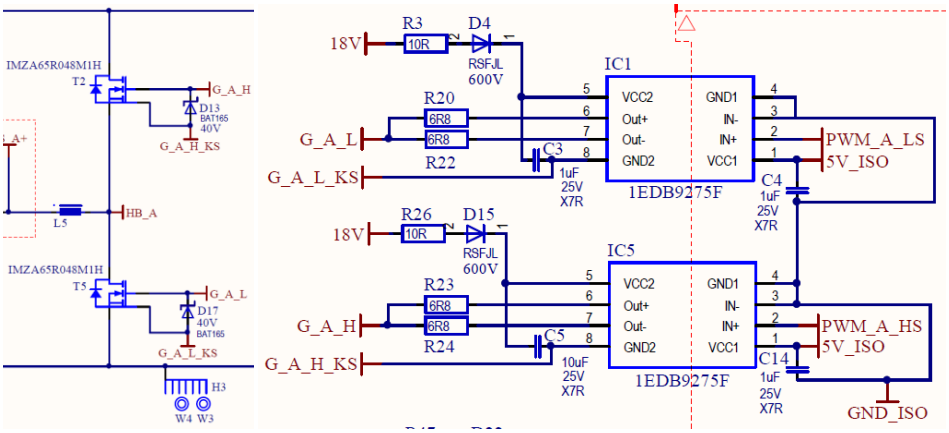

Figure 43. Recommended driving circuitry for the boosting half-bridge in the totem pole PFC.

4.2. DRIVING 3-PIN COOLMOS™

The SRs in the totem pole ACDC converter are ZCS and at only twice the frequency of the grid (100 Hz to 120 Hz). Therefore, the switching speed is not critical. Moreover, a high-ohmic turn-on helps reduce common-mode noise caused by the transition of the SRs.

The recommended driving circuitry (Figure 44) includes two single-channel drivers (1EDB8275F), especially designed for driving CoolMOS™, with a UVLO of 7 V.

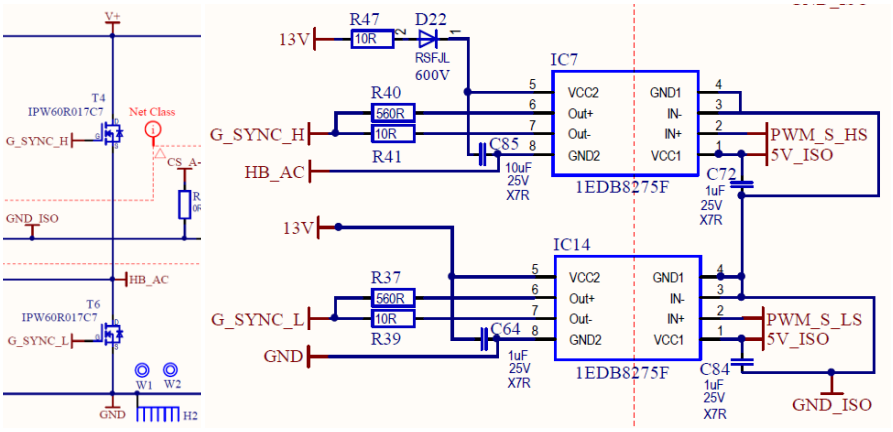

Figure 44. Recommended driving circuitry for the SRs in the totem pole PFC.

The primary-side devices in the half-bridge LLC are ZVS turn-on and hard-switched turn-off at relatively low currents (therefore mostly lossless). Because of this, 4-pin devices with Kelvin source connection are not strictly needed. Therefore, in the PSU the primary-side MOSFETs are designed in 3-pin TO-247 packages.

The recommended driving circuitry (Figure 45) also includes two single-channel drivers, 1EDB8275F, designed for CoolMOS™. It is worth mentioning that the safety isolation in the LLC half-bridge driving is not required in this case because a digital isolator has been used to transfer the signal from the secondary side, where the LLC controller is located.

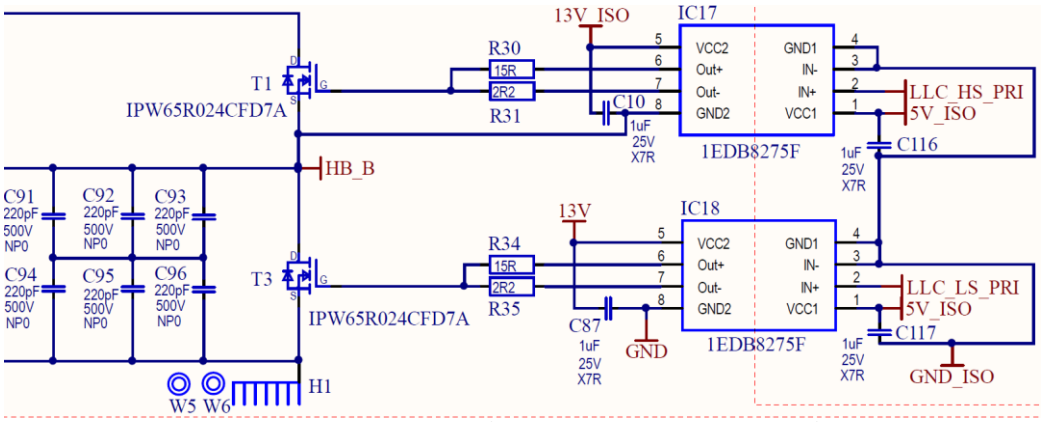

Figure 45. Recommended driving circuitry for the primary-side devices in the half-bridge LLC.

4.3. DRIVING THE ORING OPTIMOS™

The ORing MOSFETs are located in the positive rail of the output of the PSU. Therefore, the driving of the ORing devices shall be referenced to the 50 V_{DC} output. To generate the required auxiliary voltage the proposed circuit in Figure 46 is used.

The principle of operation of the circuit is of a capacitive charge pump. The capacitor C120 is referenced to one of the secondary-side SRs' half-bridge mid-point, which during the operation of the converter alternates between ground and the output voltage of the PSU at the switching frequency of the converter (square wave). Therefore, thanks to the decoupling diodes D9 and D5, the capacitor C120 is alternately charged from the auxiliary 12 V_{DC}, and discharged to the capacitor C119. Finally, the capacitor C119 supplys the ORing driver with 12 V_{DC} above the output PSU rail.

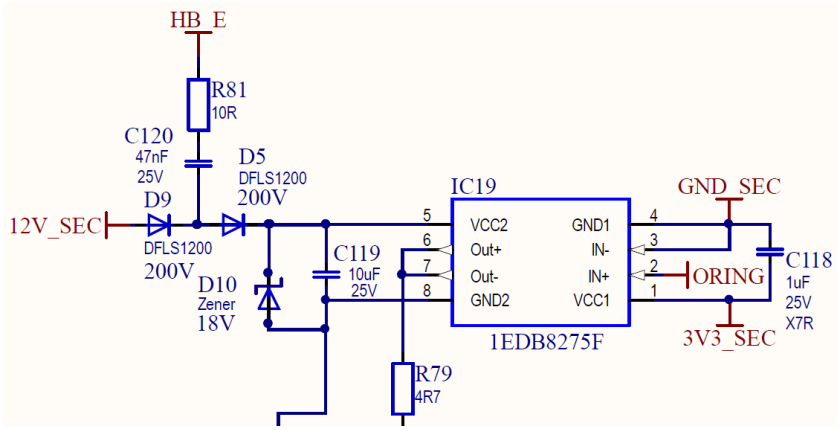

Figure 46. Proposed driving circuit for the ORing of the PSU.

4.4. DRIVING THE SR OPTIMOS™

The rectification of the half-bridge LLC DCDC converters has a full-bridge configuration with a total of 24 devices, six devices per position. Although the SRs are switched on and off in ZVS, and there are no switching losses caused by slow switching, is is still recommended to have four separate drivers. On one hand, the driving losses can be better spread between the four packages. On the other hand, the additional driver strength helps ensure accurate and fast switch-on and -off and proper clamping of the Miller feedback during the transitions.

The driving circuit for the SRs (Figure 47) includes four 2EDF7275F dual-channel, functional isolated MOSFET gate drivers, with up to 650 V_{DC} isolation channel-to-channel.

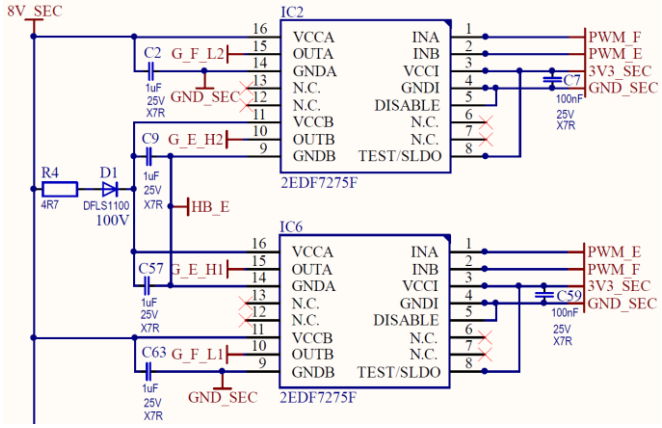

Figure 47. Proposed driving circuitry for the SRs of the LLC DCDC converter.

4.5. GENERATING THE MULTIPLE AUXILIARY DRIVING VOLTAGES

The complete PSU requires several distinct supply voltage rails:

- 3.3 V_{DC} for the supply of the LLC DCDC control circuitry (XMC4200)
- 5 V_{DC} for the supply of the totem pole ACDC control circuitry (XMC1404)
- 8.5 V_{DC} for the driving of the LLC DCDC converter SRs (OptiMOS™)
- 12 V_{DC} for the driving of the primary-side half-bridge of the LLC DCDC converter and the driving of the totem pole ACDC converter SRs (CoolMOS™), and the supply of the internal fan
- 18 V_{DC} for the driving of the boosting half-bridge in the totem pole ACDC converter (CoolSiC™)

The onboard auxiliary flyback provides several of these supply rails. However, it is not practical to realize a flyback transformer with that many distinct windings. Therefore, the auxiliary circuitry proposed in Figure 48 provides several of the above listed voltages from one of the flyback 12 V_{DC} outputs.

The core of the circuit in Figure 48 is a 1EDB8275F single-channel driver, which generates a fixed-frequency square wave at its output (approximately 350 kHz). The square wave is fed to two different smaller converters. On the one hand, a charge pump (C101 and D28) raises the 12 V_{DC} at the input up to 24 V_{DC} (at C99), which is then regulated down to 18 V_{DC} by an LDO (C98 and IC8). On the other hand, a three-winding transformer with voltage-doubler rectification generates two separate isolated supply rails for the totem pole PFC control card and the high-side driver of the half-bridge LLC.

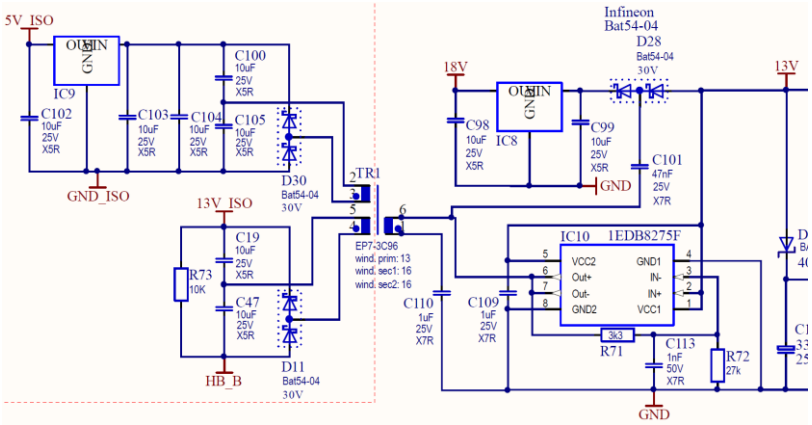

Figure 48. Proposed auxiliary supply circuit implemented with the single-channel driver 1EDB8275F.

5. SCHEMATICS

The converter hardware is comprised of a main board and a controller card. Figure 49 and Figure 50 represent the schematics of the main board, and the control card. Unlike in the other converters in this thesis, the auxiliary on-board supply has been integrated into the main board PCB.

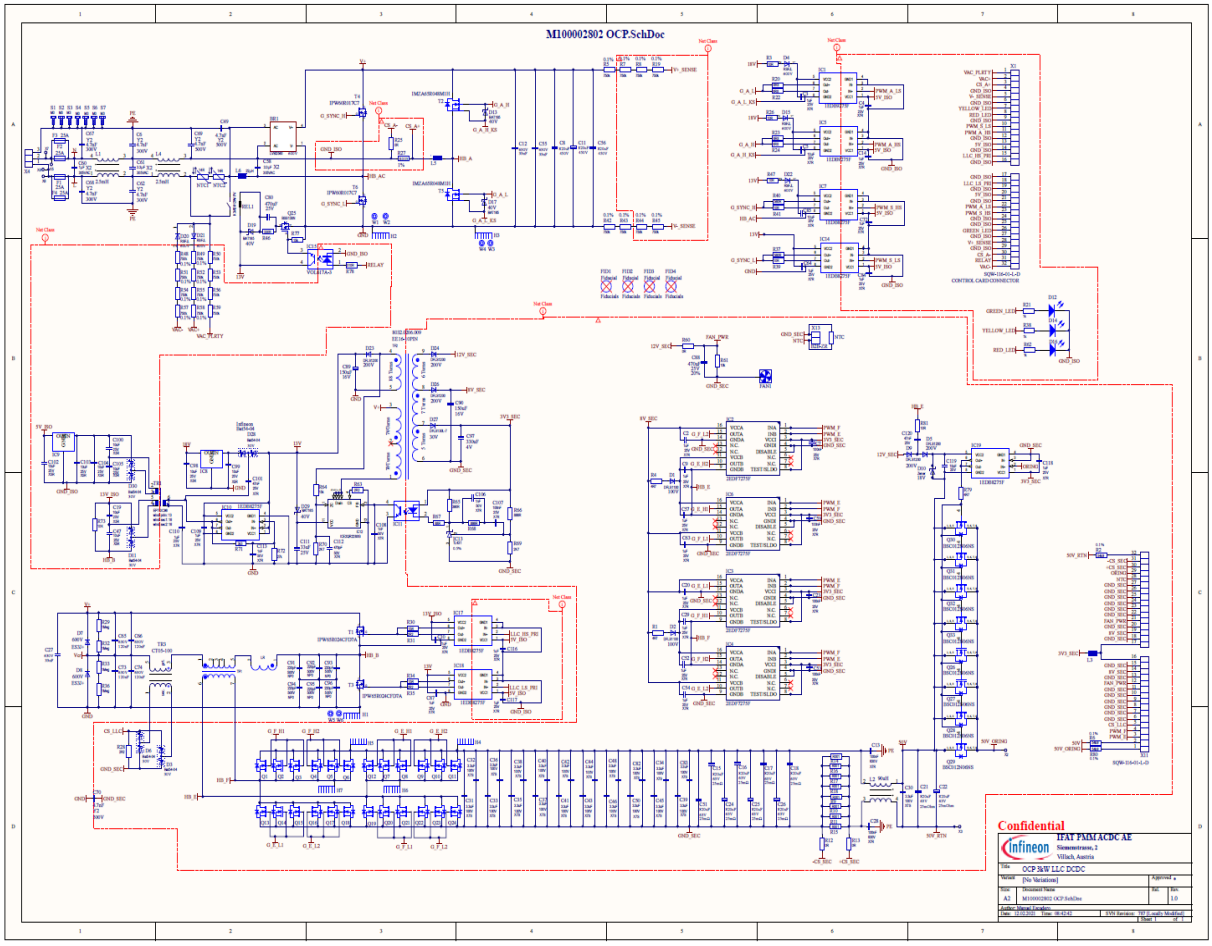

Figure 49. 3000 W 50 V PSU main board with IPW60R024CFD7 and IMZ65R048M1H.

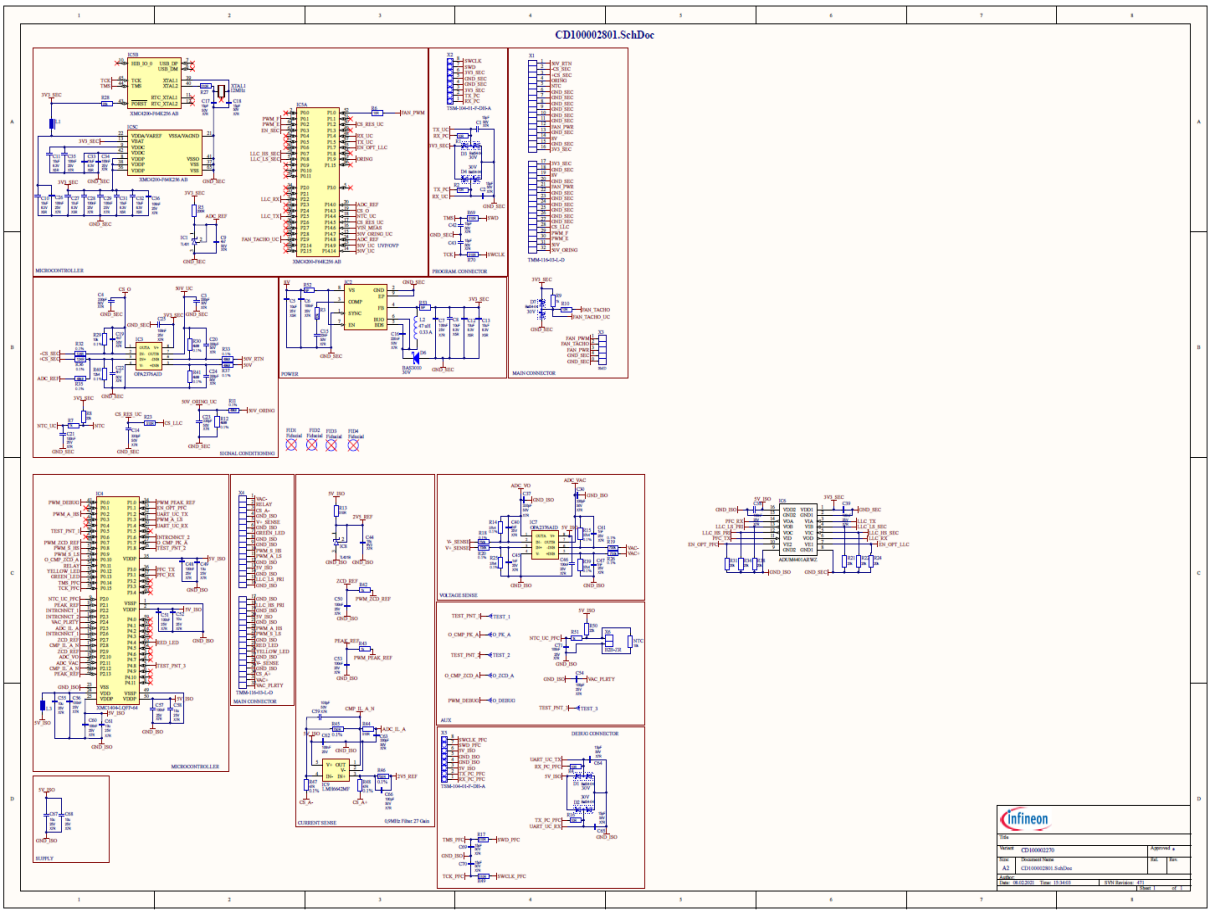

Figure 50. 3000 W 50 V PSU controller card with XMC4200-F64K256AB and XMC1404-LQFP-64.

6. CONCLUSIONS

Due to the increasing power demand in server and data center applications the requirements of power density and efficiency for the PSU raise continuously. This is due to the operational cost of the infrastructure: on the one hand the cost of the electricity and on the other hand the cost of the space and maintenance of the installations. Moreover, the high reliability demand in the server and data center applications has a severe impact in the hold-up requirements, which can be as large as 20 ms delivering full power. These tendencies in power density, efficiency and reliability requirements can be observed in the newly released OCP rectifier V3 specifications for server and datacenter PSU. The main changes in relation to the previous PSU specifications are the higher requirements in terms of efficiency and power density, together with the large hold-up time (20 ms at full power). However, the output voltage has been increased to 50 V_{DC}, although still in a narrow range, which should help with achieving the challenging target specifications.

This chapter introduces a 3 kW power supply unit (PSU) targeting the newly released OCP rectifier V3 specifications for servers and data centers. The PSU comprises a front-end ACDC bridgeless totem pole converter followed by a back-end DCDC isolated half-bridge LLC converter. The front-end totem pole converter provides power factor correction (PFC) and total harmonic distortion (THD). The LLC converter provides safety isolation and a tightly regulated output voltage. Figure 1 shows a photograph of the PSU outside of its chassis.

The measured peak efficiency of the complete PSU at 230 V_{AC} is 97.5 %, not including the internal fan, and 97.4 %, including the internal fan. The overall outer dimensions of the PSU are 73.5 mm x 520 mm x 40 mm, which yields a power density in the range of 32 W/inch³ (1.95 W/cm³).

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SECTION II. PUBLICATIONS

CHAPTER 7. FIRST PUBLICATION

Modulation scheme for the bidirectional operation of the Phase Shift Full Bridge Power Converter

Manuel Escudero, David Meneses, Noel Rodriguez, and Diego Pedro Morales[1]

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- Impact factor: 7.224
- JRC rank: (Q1)

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***Abstract*—This paper proposes a novel modulation technique for the bidirectional operation of the Phase Shift Full Bridge (PSFB) DC/DC power converter. The forward or buck operation of this topology is well known and widely used in medium to high power DC to DC converters. In contrast, backward or boost operation is less typical since it exhibits large drain voltage overshoot in devices located at the secondary or current-fed side; a known problem in isolated boost converters. For that reason other topologies of symmetric configuration are preferred in bidirectional applications. In this work, we propose a modulation technique overcoming the drain voltage overshoot of the isolated boost converter, without additional components other than the ones in a standard PSFB and still achieving full or nearly full ZVS in the primary or voltage-fed side devices along all the load range. The proposed modulation has been tested in a bidirectional 3.3 kW PSFB achieving a 98 % of peak efficiency in buck mode (380 V input, 54.5 V output), and a 97.5 % in boost mode (51 V input, 400 V output). This demonstrates that the PSFB converter may become a relatively simple and efficient topology for bidirectional DC to DC converter applications.**

***Index Terms*—Bidirectional converter, current-fed, isolated boost converter, modulation technique, Phase Shift Full Bridge, soft switching.**

I. INTRODUCTION

Bidirectional converters are commonly used in uninterrupted power supplies (UPS) and battery energy storage systems where charging and discharging functionalities are desired to be integrated to reduce volume and cost. UPS converters are usually AC/DC converters composed of two stages: an AC/DC first stage, providing power factor correction (PFC), and a tightly regulated DC/DC second stage providing isolation and battery management [1]. Other applications like on board chargers are in general designed with bidirectional capability only on the DC/DC stage: they charge the battery from an AC/DC source and transfer energy from the battery to the motor, other car systems or back to the grid (provided an external inverter) [2]-[3]. Further examples of bidirectional converter applications are found in battery manufacturing processes where batteries are charged and partially discharged for testing: a bidirectional DC/DC converter can reuse the discharging energy to charge up other batteries, saving energy and costs [4].

The commonly used bidirectional DC/DC topologies are symmetric in their design and operation in forward (in this paper referred as the charge of a battery, or buck mode operation) and reverse mode (here referred as discharge of a battery, or boost mode operation). This might seem logic or more straightforward for the designer as the converter operates basically on the same manner when working in forward and reverse directions. However, this is achieved at the expense of added complexity, design compromises and normally a negative impact on efficiency, lower than uni-directional converters. That is the case of Dual Active Bridge (DAB) (Fig. 1), LLC or

CLLC (Fig. 2) resonant converters [5]-[8].

The Phase Shift Full Bridge (PSFB) is an isolated DC/DC buck-derived converter topology that comprises a primary side full bridge at the input (Q_1, Q_2, Q_3 and Q_4 in Fig. 3), an isolation transformer, a rectification stage (Q_5, Q_6, Q_7 and Q_8) and an output LC filter (L_o and C_o). The rectification stage may have different configurations: center tapped, current doubler or full bridge; each of them having its advantages in different applications: low voltage, high current or high voltage outputs respectively [9]; however these alternatives have no major impact on the working principles of the converter.

One of the major advantages of PSFB over the other topologies is the comparatively lower *rms* currents through the converter components thanks to the output filter inductance. Table I summarizes the *rms* currents calculated numerically from the simulated waveforms of three designs with same input voltage range, output voltage range and maximum output power specifications, and working in the same conditions (same input voltage, output voltage and output current). On the other hand, the secondary side devices are hard commutated and exhibit higher switching losses than in fully resonant converters (LLC) [10]. Additionally, the output inductance constitutes an additional source of losses which makes the design of a high efficiency PSFB a challenging task. A thorough comparative analysis is, however, out of the scope of this paper.

TABLE I
RMS CURRENTS IN THE MAIN COMPONENTS

Parameter	PSFB	CLLC	DAB
Primary MOSFETs I	4.12 A	4.51 A	4.57 A
Primary MOSFETs II	4.02 A	4.51 A	4.57 A
Transformer primary	5.73 A	6.43 A	6.67 A
Transformer secondary	30.07 A	34.90 A	35.02 A
Secondary MOSFETs	21.46 A	24.93 A	24.76 A
Resonant inductor	5.73 A	6.43 A	6.67 A
Output inductor	30.61 A	N/A	N/A

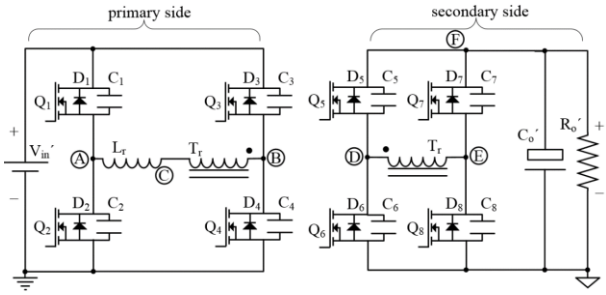


Fig. 1 Simplified schematic of a conventional DAB DC/DC converter configuration.

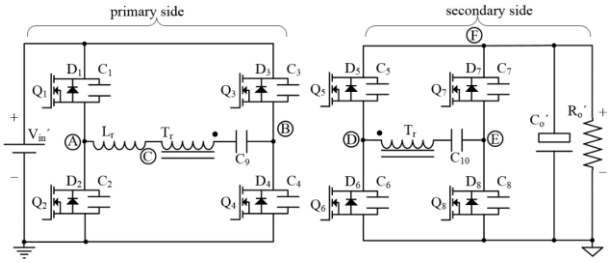


Fig. 2 Simplified schematic of a conventional full bridge CLLC DC/DC converter configuration with full bridge rectification.

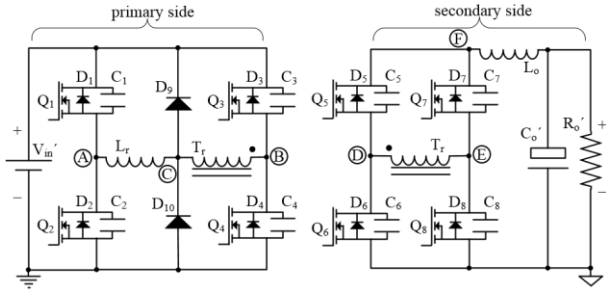


Fig. 3 Simplified schematic of a conventional Phase Shift Full Bridge DC/DC converter configuration with full bridge rectification and primary side clamping diodes.

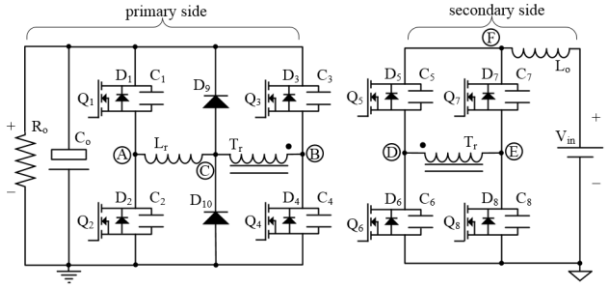


Fig. 4 Conventional Phase Shift Full Bridge working as isolated boost converter.

Although the PSFB converter is not a symmetric bidirectional converter, it can work in reverse direction, transferring power from the secondary side to the primary side (as referred in this document), and operating as a current-fed isolated boost converter. The output filter inductance (L_o) becomes then the boost inductor in this operation mode. The energy is stored in L_o when the secondary or current-fed side devices effectively short it between ground and the energy supply, a battery in the intended application, as shown in Fig. 4. The energy is transferred when one of the diagonals in the current-fed side turns-off, so the current is forced through the transformer and reflected into the primary side. The primary or voltage-fed side of the converter acts as the rectification stage when working in boost mode. The voltage-fed devices could be used as pure diode rectifiers, taking advantage of the intrinsic body diode of the devices, or by mounting parallel diodes whenever the devices do not have intrinsic body diodes or their characteristics make them not appropriated for diode operation (case of Wide Band-Gap devices) [11]-[12].

Despite PSFB is a known alternative for bidirectional converters, it is often excluded from comparative evaluations [13] due to the intrinsic problems of isolated boost converters. If the primary side operates as diode-like rectifiers, performance of the converter is poor due to three main reasons:

- High conduction losses with passive rectification, even though the primary side operates with high voltage and low current levels for the intended application.
- High switching losses due to reverse recovery (Qrr) and output capacitance (Qoss) charge loss, even though PSFB converters usually mount devices with low or virtually no Qrr (Schottky, SiC diodes or "fast body diode" MOSFETs) [14].
- High secondary side drain voltage overshoots that increases electromagnetic interference (EMI) and compromises the reliability of the converter forcing to use devices of a high voltage class, which relates in a worse figure of merit (FOM) and the consequent increase on the converter losses [15]. The overshoot is induced by the mismatch between the current of the boost inductor and other inductances in the converter at the start of a power transfer.

A possible solution to the secondary side voltage overshoot consist in using secondary side snubbers as suggested in [16], at the expense of increased complexity and cost and still having a negative impact on performance (low efficiency). A modulation scheme for bidirectional operation of PSFB that overcomes current-fed voltage overshoot has already been reported in [17], achieving Zero Current Switching (ZCS) in the primary side HV bridge; however, it fails to achieve Zero Voltage Switching (ZVS) which is much more convenient than ZCS for modern HV silicon based devices (Super Junction MOSFETs) [18]. Another alternative modulation scheme is proposed in [19] but it can only achieve ZVS of the HV primary side devices in a limited load range. In the modulation scheme analyzed in [20] the power transfer requires of two control variables, and the body diode conduction of the secondary side devices is unnecessarily extended, with the consequent expected increase in conduction losses; furthermore, it does not address the effects of the clamping diodes D_9 and D_{10}.

The proposal in this work solves the above mention issues in isolated boost converters by introducing a novel modulation scheme for bidirectional operation of PSFB, which overcomes the secondary side induced overshoot on a standard converter configuration (Fig. 4) without affecting the forward operation performance, nor including design tradeoffs, additional circuit complexity or additional cost. The proposed modulation achieves full or nearly full ZVS in the voltage-fed side devices (HV bridge) along all load range. It requires, however Q_1-Q_4 to be active devices that can be controlled independently.

The rest of this paper is organized as follows. In Section II a detailed analysis of the origins of the secondary side drain overshoot is conducted. In section III a new control scheme for the bidirectional operation of PSFB is analyzed in detail. The study is confirmed by experimental results presented in Section IV; and finally, Section V presents a summary of conclusions out of this work.

II. BOOST MODE DRAIN VOLTAGE OVERSHOOT

In the boost operation, when a power transfer starts, the primary side becomes effectively connected in series to the boost inductor L_o. A simplified equivalent circuit of this situation is presented in Fig. 5 with $i_{Lo''}$ being the primary side reflected current of L_o, i_{Lr} the current flowing through primary side resonant inductance and $i_{Llkg''}$ reflected current through the leakage of the transformer. If $i_{Lo''}$ is greater than zero (which would be the case when operating in boost mode), and i_{Lr} and $i_{Llkg''}$ are lower than $i_{Lo''}$, it will necessarily induce a voltage in V_{CA} and V_E high enough to force the current through L_r and L_{lkg} to increase until all currents match.

Due to the action of the clamping diodes and to the assumption of L_r being significantly larger than $L_{lkg''}$, even in the worst case overshoot, the voltage V_C will clamp to one of the supply rails effectively decoupling L_r from the other inductances. Therefore, for simplicity but without loss of generality, we will omit L_r in the subsequent analysis.

The induced overshoot by L_{lkg} and other parasitic inductances of the circuit cannot be clamped by diodes, as there is no possibility of accessing the node between transformer and its leakage in real applications. A possible solution would be removing the inductances causing the overshoot; however, realizing a transformer with zero or nearly zero leakage is impractical.

On the other hand, if the overshoot provoked by L_r is snubbed by the clamping diodes (which one drives the current depends on the secondary side switches configuration) most of of current pass through D_9 or D_{10}, as they become the lowest impedance path (Fig. 6(a)); leading to an increase in conduction losses and underutilization of Q_1 and Q_2.

The induced voltage overshoot is directly related to the inductance values (L_o, L_{lkg}), their initial stored energy (current) and the output capacitance of the secondary side devices (C_5, C_6, C_7, C_8). The time constant of the resonance can be calculated as (1). Assuming zero current at the initial state through L_o and L_{lkg}, the voltage at V_E can be calculated as (2), and assuming L_o much bigger than L_{lkg} we can rewrite the previous relation as (3) where the peak overshoot depends mostly on V_{in}, and with a maximum amplitude of two times its value. In an actual

case, the energy of the resonance will be partially dampened by the parasitic resistances of the circuit; which we will omit in this analysis to obtain the maximum, worst case, possible overshoot.

$$\omega = \frac{\sqrt{L_{lkg}+L_o}}{\sqrt{(C_5+C_8)L_{lkg}L_o}} = \frac{\sqrt{L_{lkg}+L_o}}{\sqrt{(C_6+C_7)L_{lkg}L_o}} \tag{1}$$

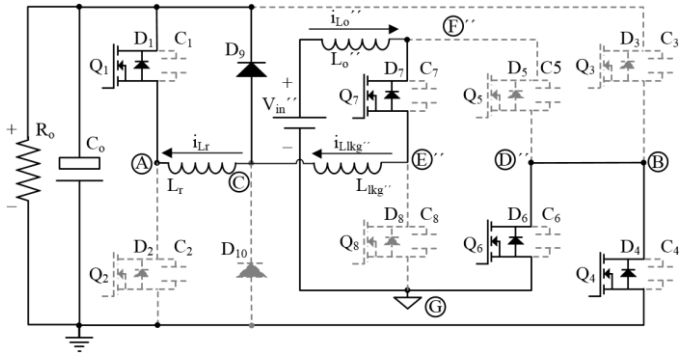
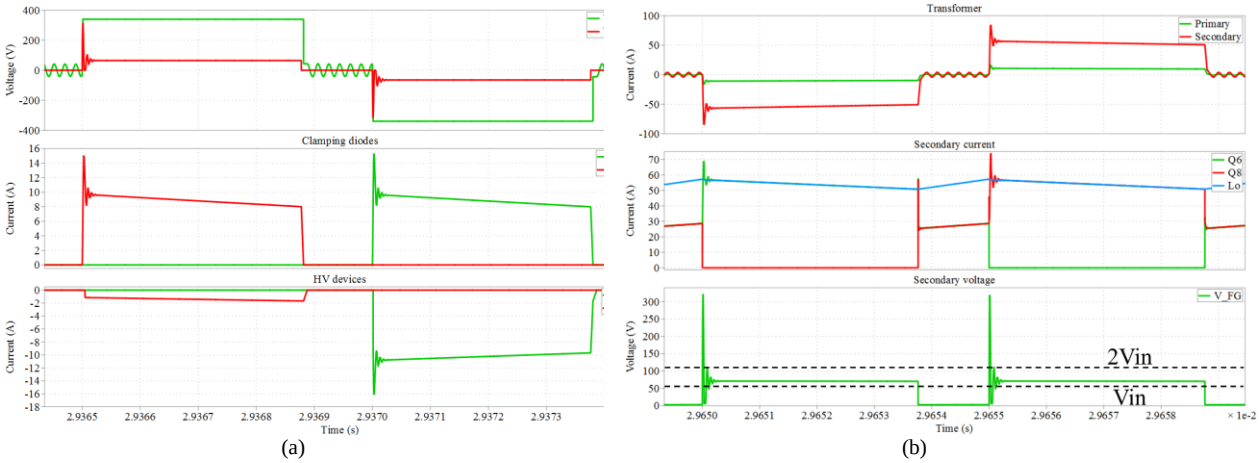


Fig. 5 Equivalent configuration of the Phase Shift Full Bridge during a power transfer as an isolated boost converter.



(a) (b)

Fig. 6 Simulated waveforms of a conventional Phase Shift Full Bridge working as isolated boost converter with passive rectification. (a) Current through the clamping diodes and primary side devices. Clamping diodes drive most of the primary side current. (b) Current-fed devices drain voltage overshoot induced by iLo(0) > 0.

$$V_E(t)|_{\substack{iLo(0)=0 \\ iLr(0)=0}} = V_X(t) = \frac{(L_o V_{in} + \frac{L_{lkg} V_o}{n})}{(L_{lkg}+L_o)}(1-\cos(t\omega)) \tag{2}$$

$$L_{lkg} \ll L_o \xrightarrow{yields} V_E(t)|_{\substack{iLo(0)=0 \\ iLr(0)=0}} \approx V_{in}(1-\cos(t\omega)) = V_Y(t) \tag{3}$$

In the case where the initial current through L_o is larger than zero, the additional stored energy induces always a larger overshoot than the expressed in (3) (Fig. 6(b)). In this case V_E can be estimated by (4) or otherwise approximated by (5), with the overshoot amplitude proportional to the initial current i_{Lo} and the square root of L_{lkg}.

$$V_E(t)|_{\substack{iLo(0)>0 \\ iLr(0)=0}} = V_X(t) + \frac{iL_o(0)\frac{\sqrt{L_o L_{lkg}^3}+\sqrt{L_{lkg}L_o^3}}{\sqrt{(C_5+C_8)(L_{lkg}+L_o)}}}{(L_{lkg}+L_o)}\sin(t\omega) \tag{4}$$

$$L_{lkg} \ll L_o \xrightarrow{yields} V_E(t)|_{\substack{iLo(0)>0 \\ iLr(0)=0}} \approx V_X(t) + iL_o(0)\sqrt{\frac{L_{lkg}}{(C_5+C_8)}}\sin(t\omega) \tag{5}$$

However, in the case where the initial current through L_{lkg} is larger than zero, the overshoot induced by the initial current through L_o can be effectively cancelled by matching $i_{Llkg}(0)$ with $i_{Lo}(0)$, as expressed in (6) and (7). The reader can observe that, because of the oscillation components are in phase, the initial current through L_{lkg} cannot, theoretically, cancel the overshoot in (2)-(3).

$$V_E(t)|_{\substack{iLo(0)>0 \\ iLr(0)>0}} = V_X(t) + \frac{(iL_o(0)-iL_{lkg}(0))\frac{\sqrt{L_o L_{lkg}^3}+\sqrt{L_{lkg}L_o^3}}{\sqrt{(C_5+C_8)(L_{lkg}+L_o)}}\sin(t\omega)}{(L_{lkg}+L_o)} \quad (6)$$

$$L_{lkg} \ll L_o \xrightarrow{yields} V_E(t)|_{\substack{iLo(0)>0 \\ iLr(0)>0}} \approx V_Y(t) + (iL_o(0) - iL_{lkg}(0))\sqrt{\frac{L_{lkg}}{(C_5+C_8)}}\sin(t\omega) \quad (7)$$

A. PRECHARGE OF PRIMARY INDUCTANCES

The core idea of the proposed solution is a modulation scheme that increases the current through L_r and L_{lkg} in the primary side of the converter up to the level of the reflected secondary side L_o current before a power transfer. In this manner, the coupling of currents at the start of a power transfer occurs effectively with no additionally induced voltage stress, as expressed in (8); furthermore, it reduces the conduction losses of D_9, D_{10} and enables soft switching of the primary side HV devices.

$$iL_o(0) \le iL_{lkg}(0) \xrightarrow{yields} V_E(t) \approx V_{in}(1-\cos(t\omega)) \quad (8)$$

The current through L_r, L_{lkg} increases when one of the diagonals in the primary side bridge is active (Q_1 and Q_4, or Q_2 and Q_3) while the transformer is effectively shorted by the secondary side devices (which is the case during the charge of the boost inductor L_o, so-called boost duty), hereafter referred as precharge in this paper. The time required for precharging L_r, L_{lkg} current up to the required value can be estimated by (9) and the calculation can be easily implemented in a controller measuring i_{Lo} current and the voltage V_o (Fig. 7). In the prototype developed in this work, the control of the precharging time is done on a cycle by cycle scheme based on the measurements of L_o current and output voltage from the previous switching period. Since the time constant of L_o and C_o are large in relation to the switching period, we can safely assume the current and the voltage not varying between switching cycles for the estimation of the required precharging time.

It follows that the maximum available precharging time is limited to the boost duty time, which constrains the minimum output to input voltage ratio required to operate the converter, as expressed by the relations (9)-(12), where T corresponds to half of the switching period.

$$T_{precharge} = \frac{(L_r+L_{lkg''})\cdot iL_{lkg}(0)}{nV_o} \ge \frac{2(L_r+L_{lkg''})iL_o(0)}{nV_o} \quad (9)$$

$$duty_{boost} = \frac{(V_o-V_{in''})}{V_o}\cdot T \quad (10)$$

$$T_{precharge} \le duty_{boost} \xrightarrow{yields} iL_o(0) \le \frac{n(V_o-V_{in''})}{2(L_r+L_{lkg''})}\cdot T \quad (11)$$

$$iL_o(0) \ge 0 \xrightarrow{yields} V_o \ge V_{in''} \quad (12)$$

From the previous equations we can derive the maximum current and power that the converter can deliver while maintaining the proposed modulation scheme, which can be estimated by (13). Nevertheless, the theoretical limits fall beyond the thermal capabilities of most practical designs (Fig. 8).

$$\Delta iL_o \ll iL_{o\_max} \xrightarrow{yields} iL_{o\_max} \approx \frac{n(V_o-V_{in''})}{2(L_r+L_{lkg''})}\cdot T \quad (13)$$

Fig. 9 demonstrates experimentally the previous analysis comparing the secondary side voltage overshoot while operating the converter in boost mode: with the proposed equalization of currents prior to a power transfer, so-called precharge (Fig. 9(a)); with a traditional boost operation of the converter (Fig. 9(b)); and operating the converter while V_o is lower than the input voltage $V_{in''}$ where, as we have already analyzed, the proposed pre-charge is not possible (Fig. 9(c)).

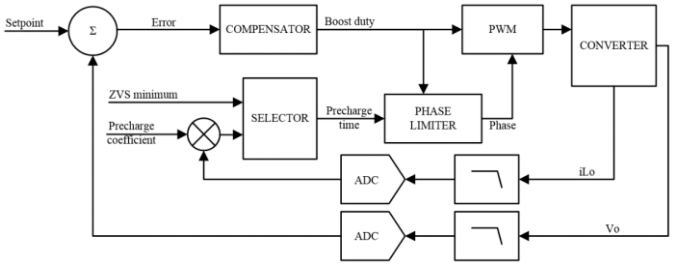


Fig. 7 Simplified control blocks for the proposed boost mode operation of PSFB.

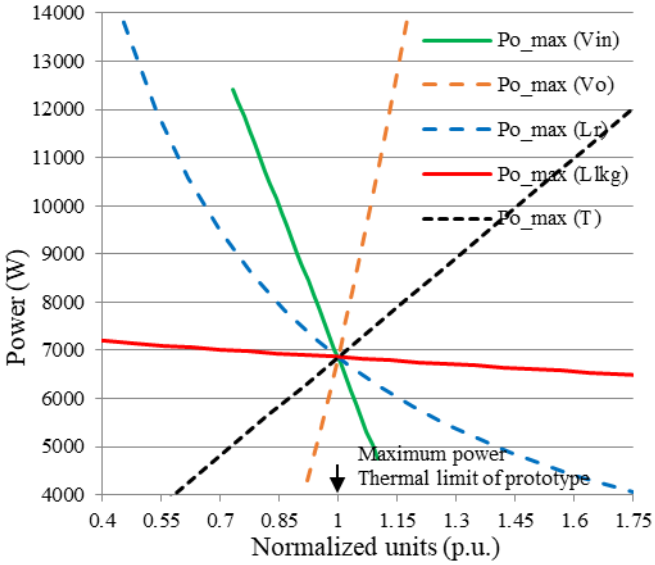
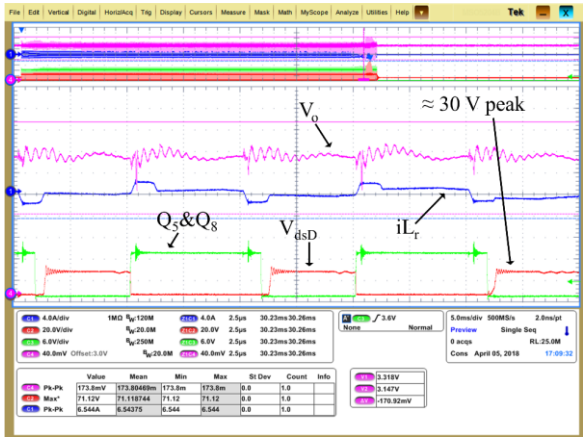
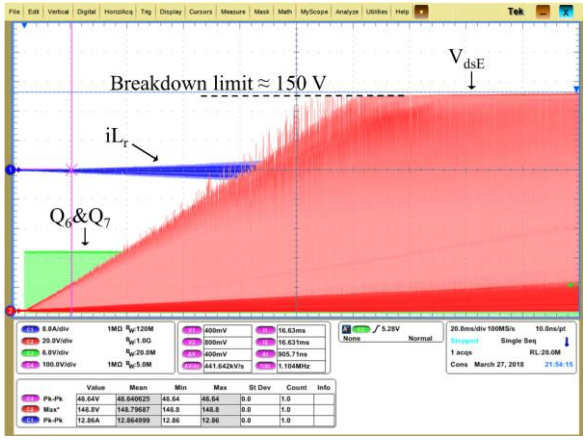


Fig. 8 Dependency between design parameters and theoretical maximum output power for the proposed boost operation of PSFB for a design with the following nominal parameter values: L_{lkg} = 1 µH, L_r = 11 µH, L_o = 9 µH, V_{in} = 380 V, V_o = 54.5 V and T = 5 µs.



(a)

(b)



(c)

Fig. 9 Current-fed secondary side devices drain voltage overshoot cancellation. (a) With the proposed precharge of Llkg and Lr currents. (b) Without precharge of Llkg and Lr currents. (c) The proposed solution requires V_o to be equal or greater than V_{in}.

III. OPERATING PRINCIPLE

A. STANDARD (FORWARD/BUCK) OPERATION

In the standard or most commonly used modulation scheme for the PSFB converter, the primary side bridge is controlled by two complementary pulse-width modulated (PWM) signals with fixed frequency and fixed duty cycle. The duty of the PWM signals is nearly 50 %, excluding dead times to avoid cross conduction of the stacked

devices (bridge legs Q_1-Q_2 and Q_3-Q_4). A phase delay between the two PWM signals defines the voltage-time window or effective duty cycle of the main transformer (T_r). The voltage applied to the transformer is then a symmetric three level square wave which is subsequently rectified and filtered in the secondary side of the converter.

Fig. 10 shows the main driving signals and waveforms of a standard modulation scheme for PSFB in T_r-lead configuration (L_r connected between transformer and the leading leg Q_1-Q_2) [21] with clamping diodes exemplified as in Fig. 1.

In Fig. 10 the converter is operating at a load point where the output filter is in continuous conduction mode (CCM) and the secondary side rectifiers are working as active switches. Freewheeling time [t_3-t_5] is relatively long as it is the case for practical designs where the converter has to be able to regulate on a wide input range during hold-up time conditions. Currents through L_r (i_{Lr}) and through the transformer T_r (i_{Tr}) differ due to the action of the clamping diodes D_9, D_{10} that snub the resonance between L_r and the secondary side rectifiers output capacitance at the start and at the end of a power transfer ([t_1] and [t_3]).

B. PROPOSED REVERSE/BOOST OPERATION

Fig. 11 shows the main driving signals and waveforms of the proposed modulation scheme for the reverse operation of a standard PSFB. The reader may notice the similitudes between Fig. 10 and Fig. 11 waveforms, where the same direction of flow was considered for i_{Lo}.

In the following paragraphs we analyze the operation principles for the proposed reverse operation of the PSFB. Before the analysis some assumptions are made: 1) all diodes and switches are ideal; 2) all switches are MOSFETs with intrinsic anti-parallel body diode 3) all capacitors and inductors are ideal 4) C_1=C_2=C_3=C_4, C_5=C_6=C_7=C_8 5) $L_m = \infty$.

1) Mode 1[t_2, t_3] [Fig. 12(a)]

During the interval [t_2, t_5] L_o is shorted to ground by the secondary side switches (Q_5-Q_8), and the primary side of the converter is effectively decoupled from the secondary, as the transformer is also shorted. The current through the output inductor increases at a rate given by (14)-(15).

$$iL_o(t) = iL_o(t_2) + \frac{V_{in}}{L_o}t, \qquad t_2 < t < t_5 \tag{14}$$

$$iL_o(t_2) = \frac{\Delta iL_o}{2} = I_{Lo} - \frac{V_{in}}{L_o}duty_{boost} \tag{15}$$

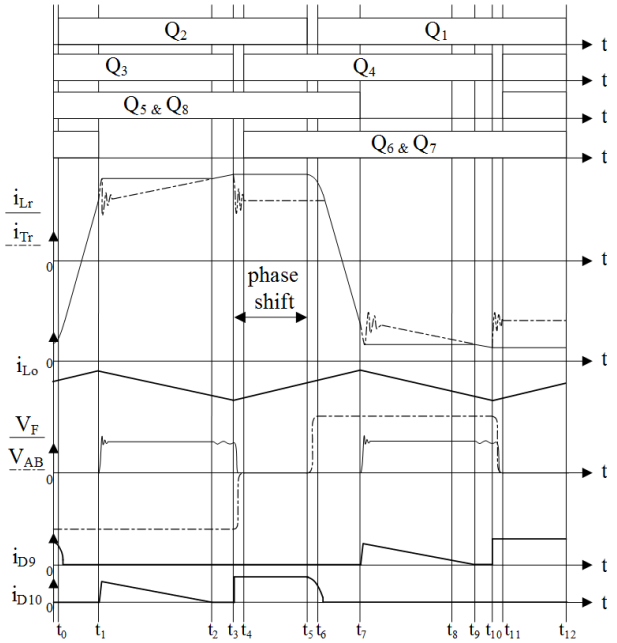


Fig. 10 Main signals scheme in the circuit for the standard forward operation of the PSFB. The same direction of flow in Fig. 5 is considered here for i_{Lo} (current is positive for boost mode operation).

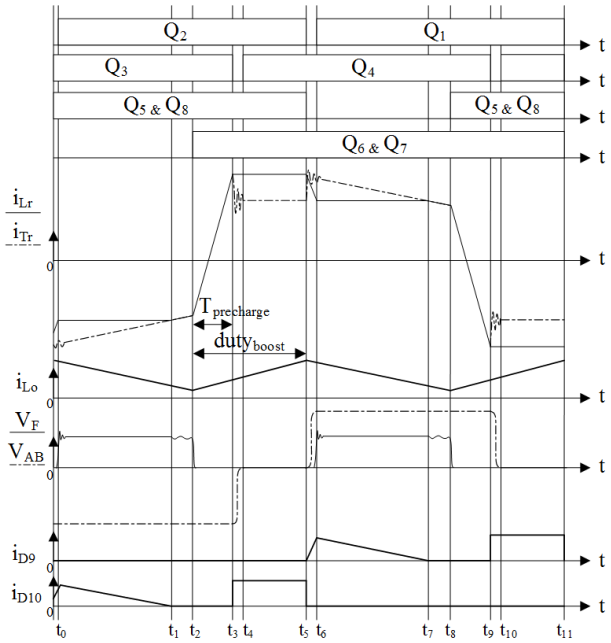


Fig. 11 Main signals scheme in the circuit for the proposed reverse operation of the PSFB.

The primary side switches Q_2 and Q_3 are on and conducting with the voltage at the output of the converter applied between points B and A ($V_{AB} \approx -V_o$). Since the transformer is virtually shorted, all the primary voltage is applied to L_r and L_{lkg}, whereas the transformer magnetizing current remains nearly constant (16). The current through L_r and L_{lkg} reverses polarity and subsequently increases near or above the value of the reflected secondary current, at a rate given by (17). At that point, the controller turns-off Q_3 finishing the so-called precharging stage,

which is one of the key differences between the proposed modulation and the conventional boost operation of a PSFB.

$$iL_m(t) \approx iL_m(t_2), \quad t_2 < t < t_3 \tag{16}$$

$$iL_r(t) = iL_{lkg''}(t) = iL_r(t_2) + \frac{V_o}{(L_r + L_{lkg''})} t, \ t_2 < t < t_3 \tag{17}$$

2) Mode 2[t3, t4] [Fig. 12(b)-Fig. 12(c)]

At [t_3], Q_3 turns-off and the current through L_r, and L_{lkg} starts to charge the output capacitance of Q_3 and discharge the output capacitance of Q_4 (Fig. 12(b)). For simplicity, the effect of the transition on the currents through the inductors would be omitted; in the intended application the output capacitances of the HV devices are small in comparison to the other elements involved in the resonance.

The current through the transformer and its leakage (i_{Tr}) drops since part of its energy is used for charging the clamping diodes capacitance, as expressed by (18). Also due to the clamping diodes, the current through L_r remains nearly constant during [t_3, t_5] (19)-(20), dismissing the effect of the forward voltage drop of the diode and the ohmic losses along the recirculation path. The difference between i_{Lr} and i_{Tr} passes through D_{10} until [t_5].

$$iT_r(t) = iL_r(t_3) - \frac{\sqrt{V_o\left(Q_{oss_{D10}} + Q_{oss_{D9}}\right)}}{L_{lkg''}}, \ t_4 < t < t_5 \tag{18}$$

$$iL_r(t) \approx iL_r(t_3), \quad t_3 < t < t_5 \tag{19}$$

$$iL_r(t_3) \geq \frac{iL_o(t_5)}{n} = \frac{I_{Lo}}{n} + \frac{V_{in}}{nL_o} duty_{boost} \tag{20}$$

After the output capacitance of Q_3 is fully charged and the output capacitance of Q_4 is fully discharged (whenever there was enough energy in L_{lgk}, L_r and L_m prior to [t_3]) the intrinsic body diode of Q_4 will become forward biased and will start conducting (Fig. 12(c)). At [t_4] Q_4 turns-on in partial or full ZVS (depending on the balance of energies).

3) Mode 3[t4, t5] [Fig. 12(d)]

The primary side current freewheels through Q_2 and Q_4, with the transformer still effectively shorted by the secondary side switches; i_{Lr} and i_{Tr} remain constant, dismissing conduction losses. However, the current through L_o keeps increasing as it remains shorted between V_{in} and secondary ground.

4) Mode 4[t5, t6] [Fig. 12(e)-Fig. 12(f)]

At [t_5] ends the boost inductor charging stage, so-called boost duty. Q_5 and Q_8 turn-off and only one of the secondary side branches remains active (Fig. 12(e)), and the primary no longer decoupled from the secondary side.

The secondary side transformer voltage V_{ED} starts to rise while Q_5 and Q_8 output capacitances are charged up through L_r and L_{lkg}. Due to the clamping diodes, after the charge of Q_5 and Q_8, i_{Lr} remains nearly constant until [t_7], see (21), while i_{Tr} rises up to the secondary side reflected current (22). In this mode, the difference between i_{Lr} and i_{Tr} passes through D_9. It follows that the clamping diodes conduct two times per power transfer (or four times per period) when using T_r-lead configuration, both in reverse and in forward operation [21].

$$iL_r(t) = iL_r(t_5) - \frac{\sqrt{V_o\left(Q_{oss_{Q5}} + Q_{oss_{Q8}}\right)}}{n^2(L_r + L_{lkg''})}, \ t_6 < t < t_7 \tag{21}$$

$$iT_r(t) = iL_{lkg''}(t) = \frac{iL_o(t)}{n}, \ t_5 < t < t_8 \tag{22}$$

On the primary side, Q_2 turns-off at [t_5]. The output capacitance of Q_1 will be discharged and the output capacitance of Q_2 charged by stored energy in L_r, L_m, L_{lkg}, and L_o, until the intrinsic body diode of Q_2 becomes forward biased and conducts (Fig. 12(f)) (whenever there was enough energy stored in the inductances prior to [t_5]). Full ZVS during this transition is easier to attain than during the transitions of Q_3-Q_4 as the energy in L_o also contributes to the energy balance. At [t_6] Q_1 turns-on in partial or full ZVS and a power transfer stage starts.

5) Mode 5[t6, t8] [Fig. 12(g)]

In this mode the power transfer from the secondary to the primary continues. The current through L_r remains nearly constant, aside from conduction losses, while iT_r drops following the reflected L_o current (23). D_9 continues conducting the difference between the currents i_{Tr} and i_{Lr}.

$$iL_o(t) = iL_o(t_5) - \frac{(Vo - nV_{in})}{L_o n} t, \quad t_5 < t < t_8 \tag{23}$$

At [t_7] i_{Tr} decreases down to i_{Lr} and D_9 stops conducting (24). From the inspection of the voltage waveform of V_F after [t_7] it can be seen that V_C and V_F are no longer clamped: the output capacitance of Q_5 and Q_8 resonates with L_r, L_{lkg} and other stray inductances during [t_7, t_8].

$$iT_r(t) = iL_r(t), \quad t_7 < t < t_8 \tag{24}$$

6) Mode 6[t8, t9] [Fig. 12(h)]

At [t_8] finishes the power transfer and starts a new precharging sequence (25), and a new boost duty time. Q_5 and Q_8 are hard switched turned-on forcing L_o and the secondary side of the transformer to be shorted to the secondary ground; this secondary side switching loss contribution does not exist in buck operation where the LV devices are soft switched. Nevertheless, the primary side HV devices can operate under full or nearly full ZVS along all load range.

$$iL_r(t) = iL_{lkg''}(t) = iL_r(t_8) - \frac{V_o}{(L_r + L_{lkg''})}t, \quad t_8 < t < t_9 \tag{25}$$

The sequence repeats in a similar manner alternating the polarity of the currents and voltages applied to the transformer. The reader may notice that with the proposed modulation scheme the primary side leg transitioning after a power transfer in buck mode (so-called leading leg) becomes the leg transitioning before a power transfer in boost mode (so-called lagging leg). This is an important difference, as it is not rare to design PSFB converters with different devices in Q_1, Q_2, Q_3, and Q_4 to account for the different available energies in the leading and lagging leg transitions. The recommendation here, for bidirectional operation, is to have the same type of devices within the primary side bridge.

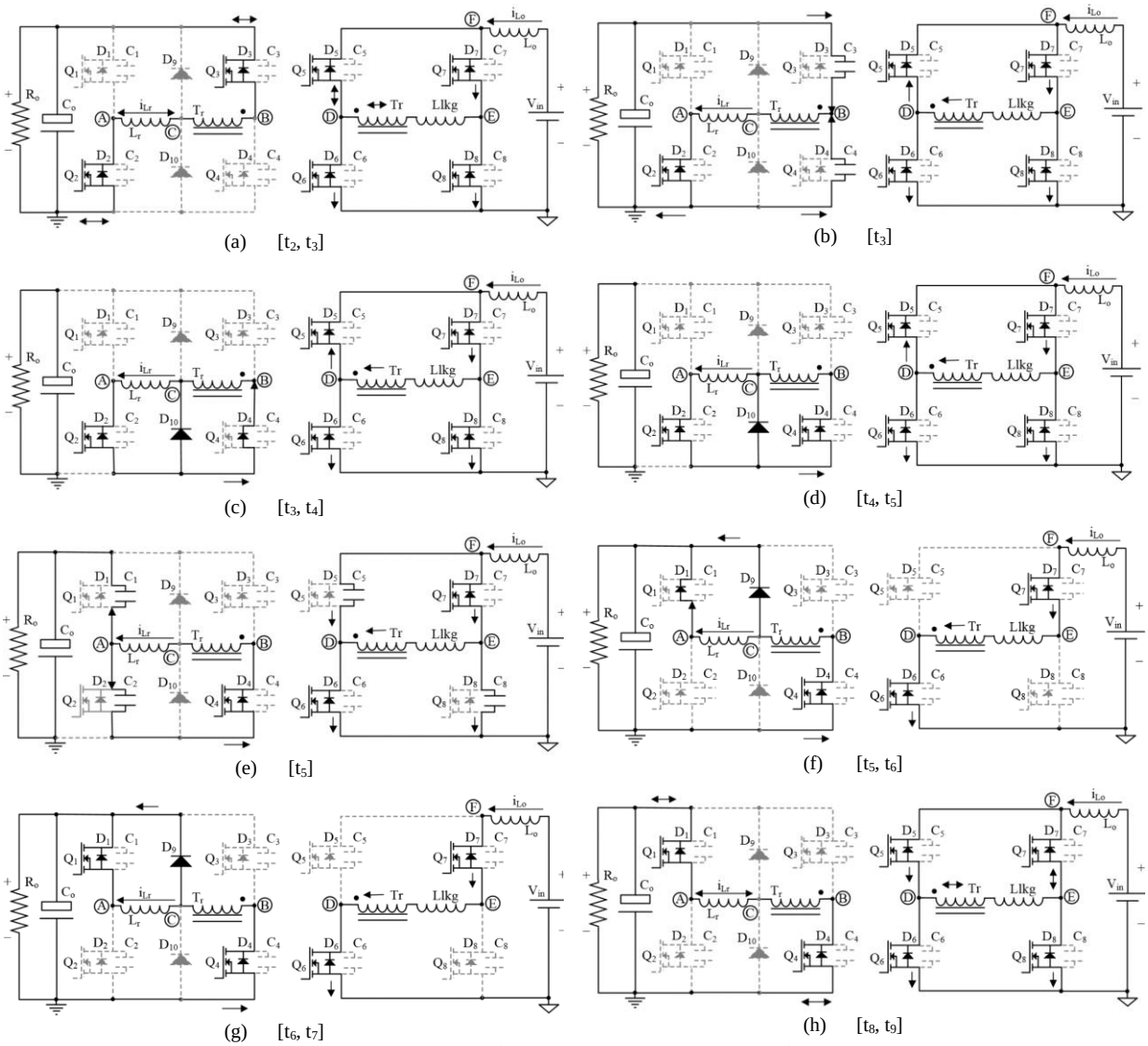


Fig. 12 Main operation modes for the proposed reverse operation of the PSFB.

C. SOFT SWITCHING RANGE

The main characteristic of the PSFB is the harnessing of the energy in the primary and secondary inductances to reach ZVS of the primary side devices. An efficiency optimized PSFB design would ideally work in full or nearly full ZVS along all load range of the converter, which is especially critic at light and medium loads, where the switching losses might be dominant [10],[22]. Fig. 13 and Fig. 14 demonstrate that the prototype achieves soft switching in those particular scenarios: even if the output capacitance of the devices is not fully discharged when the device turns-on, the remaining losses are not significative for modern HV superjunction MOSFETs [23].

The conditions required to reach ZVS are summarized in (26)-(28) with $C_{leading}$ equal to the sum of capacitances C_3 and C_4, and $C_{lagging}$ equal to the sum C_1 and C_2. The lumped capacitance of the transformer C_{tr} constitutes an important contribution to the leading leg transition; however, it does not have an influence on the lagging leg.

$$\frac{V_o^2}{2}(C_{leading}+C_{tr}) \le \frac{iL_r^2}{2}L_r + \frac{iL_{lkg}^2}{2}L_{lkg} + \frac{iL_o^2}{2}L_o + \frac{iL_m^2}{2}L_m \tag{26}$$

$$with\ iL_r \approx \frac{iL_o}{n}\ and\ L_{o''} = L_o n^2 \gg L_r\ and\ iL_m \ll iL_r \xrightarrow{yields} \frac{V_o^2}{2}(C_{leading}+C_{tr}) \le \frac{iL_o^2}{2}\left(L_o + \frac{L_r}{n^2}\right) \tag{27}$$

$$\frac{V_o^2}{2}C_{lagging} \le \left(\frac{iL_r^2}{2}L_r + \frac{iL_{lkg}^2}{2}L_{lkg}\right) \approx \frac{iL_o^2}{2n^2}L_r \tag{28}$$

Among other alternatives, the most commonly accepted way of increasing ZVS range while operating in buck mode, when possible, is the usage of an external resonant inductance (L_r), conveniently dimensioned to reach the maximum power of the converter at the minimum specified input voltage [10],[22]. The secondary side overshoot induced during the commutation by the additional inductance can be effectively reduced by the usage of primary side clamping diodes, as is suggested in [21].

With the proposed modulation scheme it is possible to extend the lagging leg ZVS range while operating in boost mode: the precharge time can be extended above the minimum required for the overshoot reduction, thus increasing the energy available during the transition, as expressed by (29)-(30); conduction losses, on the other hand, would increase. Fig. 15 illustrates the amount of charge that could be provided by the inductances during the primary side transitions while operating in boost mode and applying the proposed ZVS range extension for the lagging leg.

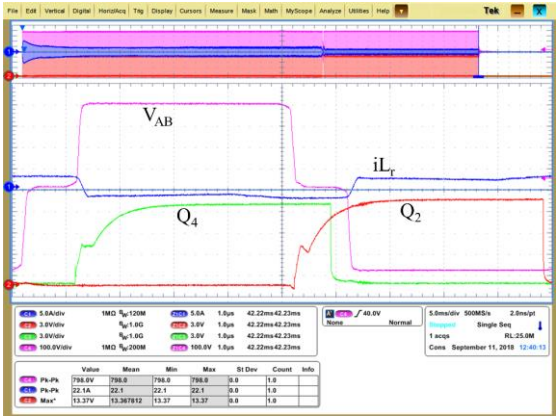
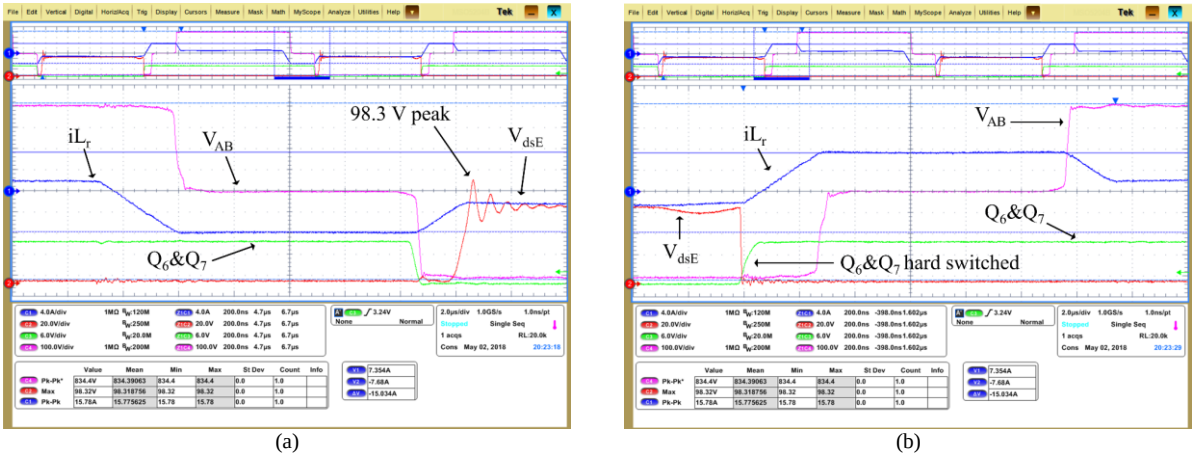


Fig. 13 Detail of primary side ZVS transitions of lagging and leading legs at 10% of load in buck mode.



(a) (b)

Fig. 14 Detail of ZVS transition of lagging and leading legs. Secondary side LV device drain voltage overshoot is also visible (98.32 V peak). Light load conditions. (a) Detail of ZVS transition of lagging and leading legs. (b) Detail of secondary side hard switched transition turn-on.

The prototype designed mounts two 75 mΩ devices in parallel for each of the primary side full bridge placeholders (Q_1-Q_4), eight of them in total, whereas four of them should be considered for the energy balance calculations during the half bridge transitions.

$$with\ iL_r > \frac{iL_o}{n} \xrightarrow{yields}$$
$$\frac{V_o^2}{2} C_{lagging} \leq \left(\frac{iL_r^2}{2} L_r + \frac{iL_{lkg}^2}{2} L_{lkg} \right) \approx \frac{iL_r^2}{2} L_r \tag{29}$$

$$iL_r = \begin{cases} \frac{V_o}{\sqrt{L_r}} C_{lagging}, & \frac{iL_o^2}{2n^2} L_r < \frac{V_o^2}{2} C_{lagging} \\ \frac{iL_o}{n}, & \frac{iL_o^2}{2n^2} L_r \geq \frac{V_o^2}{2} C_{lagging} \end{cases} \tag{30}$$

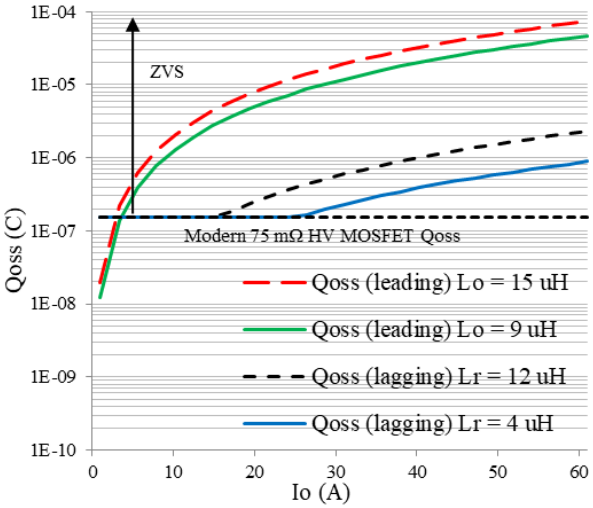


Fig. 15 Available energy during the transitions for charging and discharging the output capacitance of the HV MOSFETs at nominal Vo of 400 V for the prototype operating in boost mode with the proposed ZVS range extension. A MOSFET half bridge with a total Qoss of 154 nC achieves full ZVS where the curves fall above the horizontal dotted line.

D. TRANSITION BETWEEN OPERATING MODES

In the proposed bidirectional modulation for PSFB the transition from forward to reverse and from reverse to forward operating modes is possible without interruption of power flow or control signals. This has been already reported in the literature in [24] as an unexpected bidirectional operation of standard PSFB with the output filter working in forced CCM and the converter connected in parallel to other units.

Here we analyze how the control signals change between operation modes, and give suggestions for one of the possible transition sequences, from forward to reverse operation without stopping the converter; starting from the standard modulation of PSFB in Fig. 10 (Fig. 16(a)) and ending up in the proposed modulation scheme in Fig. 11:

- Q_6&Q_7 and Q_5&Q_8 turn-on point shifts left in time towards the falling edge of V_F and overlap it (becoming a hard switched transition). The overlap will induce a fast increase of the primary side current only limited by L_r and L_{lkg} (here so-called precharge time) (Fig. 16(b)).
- Q_5&Q_8 and Q_6&Q_7 turn-off point shifts left in time aligning to the turning-off point of Q_1 and Q_2. Unlike in the forward operation mode there is no delay between the falling edge of Q_2 and rising edge of V_F (power transfer) (Fig. 16(c)).
- Q_3 and Q_4 turn-off point shifts to the right in time, overlapping Q_5&Q_8 and Q_6&Q_7 until they reach the required precharging time, which is adjusted hereafter by the delay between Q_3, Q_4 falling edge, and Q_5&Q_8 and Q_6&Q_7 rising edge (Fig. 16(c) and (d)).
- In boost mode steady state Q_6&Q_7 and Q_5&Q_8 overlap time becomes the manipulated variable of control, the so-called boost duty time (Fig. 16(d)).

Note that in the proposed boost operation mode it is required that, before turning-off all devices in the secondary side (shut down procedure), the converter changes back to forward operation mode (Fig. 17). While working in boost mode, the current iL_o flows against the intrinsic body diodes of the devices. If they are all turned-off while the current is still flowing, the energy stored in L_o is transferred to their output capacitances with the consequent drain voltage overshoot (Fig. 18). Since the output capacitance of the devices is relatively small (C_5, C_6, C_7, C_8) in relation to L_o the voltage easily rises up to the breakdown limit and, at that point the remaining energy would be dissipated within the switches (with the consequent stress and risk of damage when there are no other countermeasures).

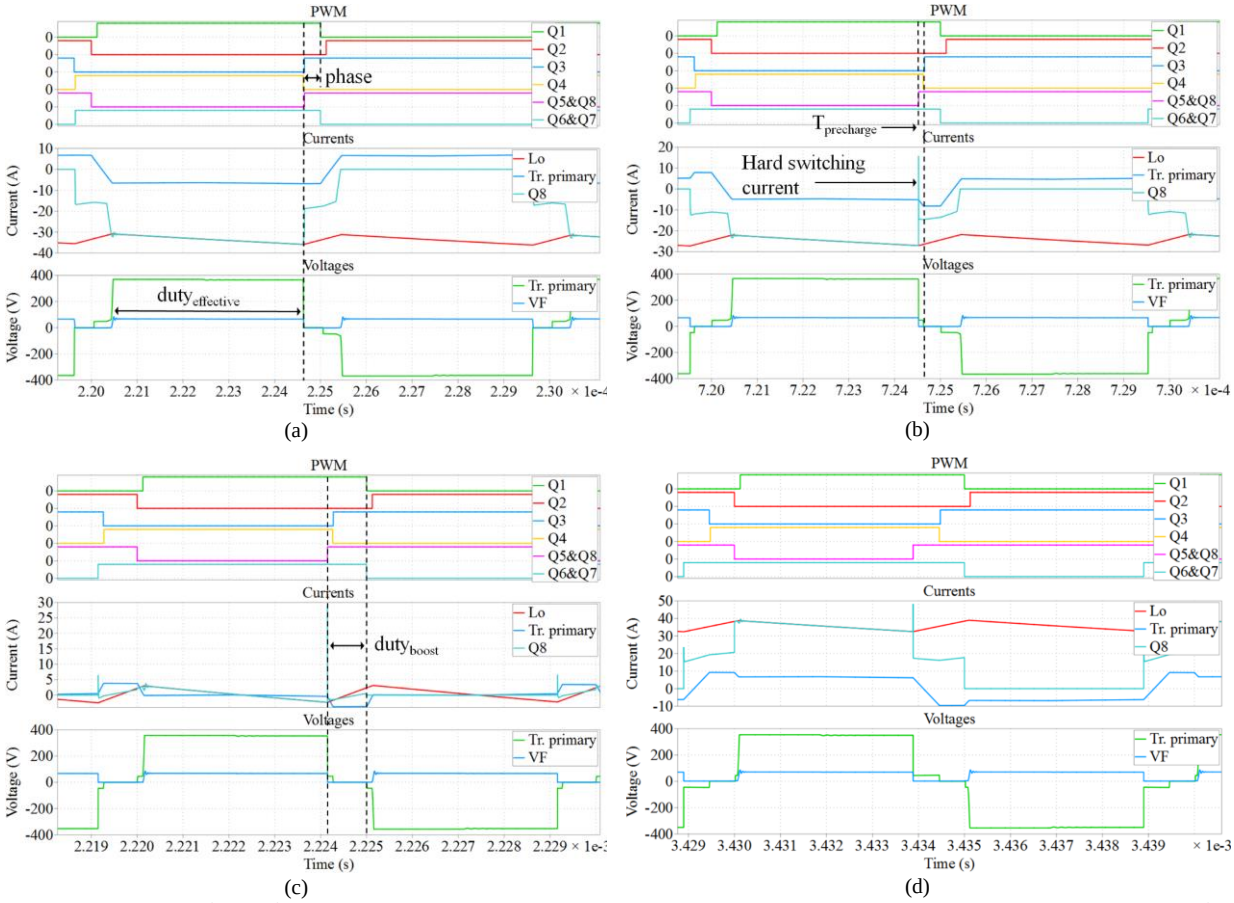


Fig. 16 Simulated waveforms of the transition between buck and boost operating modes. (a) Buck mode steady state operation. (b) Overlap of Q_3, Q_4 falling edge and Q_5&Q_8, Q_6&Q_7 rising edge, the so-called precharge time. (c) Increase of overlap between Q_5&Q_8 and Q_6&Q_7, the so-called $boost_{duty}$. (d) Boost mode steady state operation.

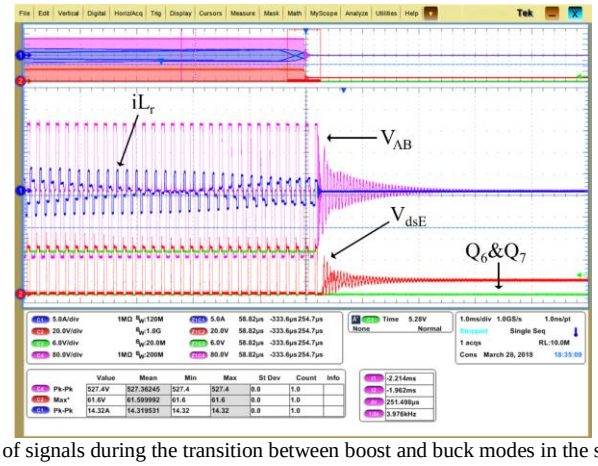
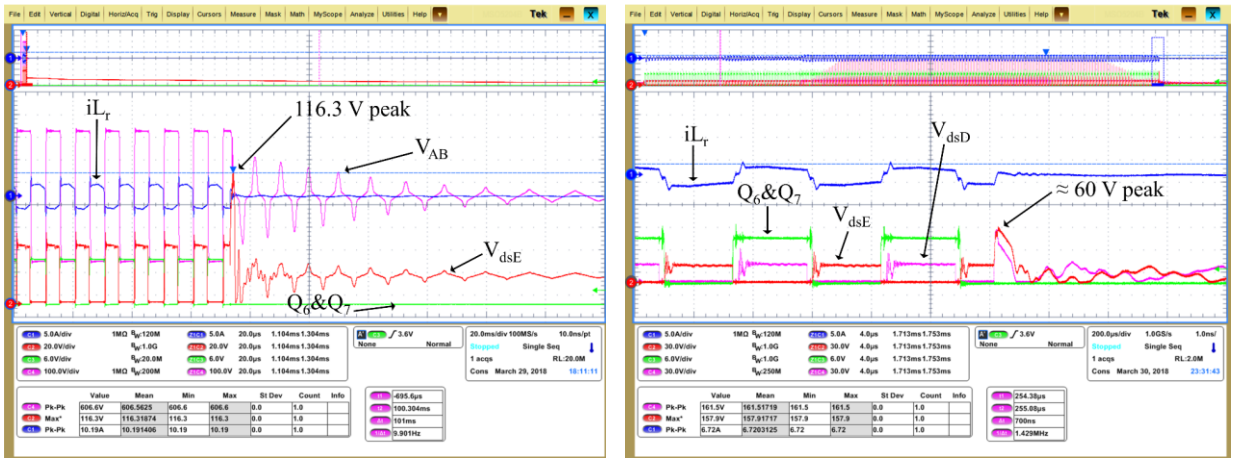


Fig. 17 Detail view of signals during the transition between boost and buck modes in the shut-down sequence.



(a) (b)

Fig. 18 Large secondary side drain voltage overshoot occurs when the devices turn-off while iL_o is still flowing towards their intrinsic body diodes. (a) A protection mechanism triggers improper shut down sequence during soft start with V_o = 300 V. (b) Drain overshoot occurs in both rectification branches.

IV. EXPERIMENTAL RESULTS

A bidirectional 3300 W DC/DC PSFB converter was designed and built to test the proposed modulation scheme under the context of this work with the specifications in Table I for buck mode operation, and the specifications in Table II for boost mode operation. The control has been implemented and tested on a XMC™ 4200 ARM® Cortex®-M4 microcontroller from Infineon Technologies AG. Table III and Table IV summarize the main converter components. Fig. 19 shows an actual snapshot of the converter within its case.

A. EFFICIENCY

Table VI shows a summary of the overall estimation of losses for the converter operating in forward mode at the main points of interest for the intended application: 20 %, 50 % and 100 % load. The distribution was estimated out of the measured efficiency of the real converter, thermographic captures, finite element (FEA), circuit and numeric simulations.

Based on the results, the transformer appears to be the main contributor to losses at 50 % loads and above. This supports the hypothesis that the performance of the converter for this power and voltages depends mostly on the design of the magnetics.

When the converter operates in the reverse operation mode (boost) the overall efficiency of the system is relatively lower due to the additional losses contributions: clamping diodes conduction, and secondary side devices hard switched transitions. All of the other contributions to losses are expected to remain approximately the same due to the nearly symmetric current and voltage waveforms in the different operating modes.

TABLE II
KEY PARAMETERS OF PROTOTYPE (BUCK MODE)

Parameter	Value
Nominal input voltage	400 V
Input voltage range	360 V - 410 V
Nominal output voltage	54.5 V
Output voltage range	43 V - 60 V
Maximum output power	3300 W
Maximum output current	85 A
Switching frequency	100 kHz
Height of the converter	1 U
Transformer turns ratio (Np : Ns)	21:4
Magnetizing inductance (Lm)	750 µH
Resonant inductance (Lr)	11 µH
Output choke inductance (Lo)	9.8 µH

TABLE III
KEY PARAMETERS OF PROTOTYPE (BOOST MODE)

Parameter	Value
Nominal input voltage	51 V
Input voltage range	43 V - 57 V
Nominal output voltage	400 V
Maximum output power	3300 W
Maximum output current	8.25 A
Switching frequency	100 kHz

TABLE IV
SI MOSFETS AND DIODES

	IPL60R075CFD7	BSC093N15NS5	IDP08E65D1
$V_{ds,max}$	600 V	150 V	650 V
$R_{DS,on,max}$	75 mΩ @ 25 °C	9.3 mΩ @ 25 °C	N/A
$C_{oss(er)}$	96 pF	604 pF	N/A

TABLE V
MAGNETIC CORE SELECTION

	Core	Material	Manufacturer
Transformer	PQI 35/28	DMR95	DMEGC
L_r	PQI 35/28	DMR95	DMEGC
L_o	Toroid	HP 60 µ	CHANG SUNG

TABLE VI
3300 W FORWARD PSFB LOSSES BREAKDOWN

Loss contribution	100% power	50% power	20% power
Auxiliary circuitry	1.02 W	1.02 W	1.02 W
Fan	4.91 W	0.64 W	0.64 W
Transformer	29.43 W	10.71 W	5.34 W
Lr	2.51 W	0.76 W	0.18 W
Lo	5.22 W	1.77 W	0.85 W
Primary bridge	16.89 W	5.28 W	2.69 W
Secondary bridge	19.24 W	9.61 W	6.95 W
Clamping diodes	2.11 W	2.47 W	2.65 W
Capacitors	0.38 W	0.35 W	0.34 W
PCB conduction	7.60 W	1.91 W	0.32 W

The efficiency of the 3300 W PSFB prototype was measured at nominal conditions in buck (380 V input and 54.5 V output) and boost (51 V input and 400 V output) operating modes (Fig. 20). As expected, the efficiency in reverse operation is lower than in the forward operation: in boost mode the secondary side devices are hard switched and the clamping diodes conduction losses also increase.

The prototype was designed to operate with forced air cooling and enclosed in a case. Due to thermal limitations of the design and the lower efficiency in the reverse mode of operation, the maximum steady state power that the converter could deliver in boost mode was rated to 3200 W during the efficiency measurements.

Fig. 19 Prototype of bidirectional PSFB converter.

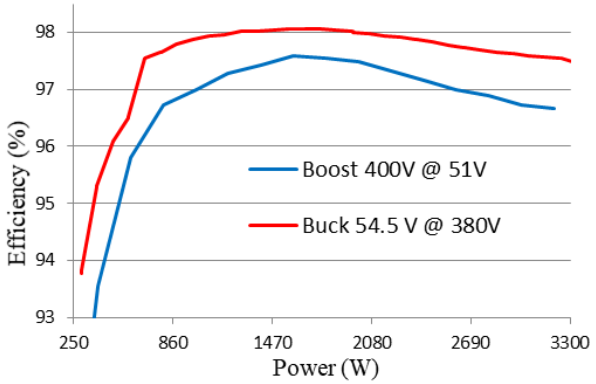


Fig. 20 Overall efficiency of the 3300 W PSFB converter prototype operating in forward and in reverse modes. Auxiliary bias and fan consumption were included in the measurements.

B. STEADY STATE WAVEFORMS

The reader may compare the experimental steady state waveforms in Fig. 21 and Fig. 22 with the diagrams in Fig. 10 and Fig. 11 respectively for their better understanding. Fig. 21 captures the forward operation at full load

(3300 W), nominal 380 V input and 54.5 V output, approximately 61 A average output current. Some details of interest in Fig. 21 are:

- The primary side bridge operates in full ZVS. The gate voltage of the bridge is not captured here, but V_{AB} (green curve) shows the characteristic smooth transitions without noticeable overshoot indicative of soft switching.
- The secondary side drain voltage (blue curve) overshoot (around 95 V) is well under the breakdown limit of the devices mounted (150 V).
- The secondary side devices are soft switched. The gate voltage (purple curve) rises after the drain voltage has fallen and falls before the drain voltage rises again. They are however hard commutated by the transformer reflected voltage.
- The difference between the transformer current (black curve) and the resonance inductance current (red curve) passes through the clamping diodes D_9, D_{10} (area enclosed by red and black curves).

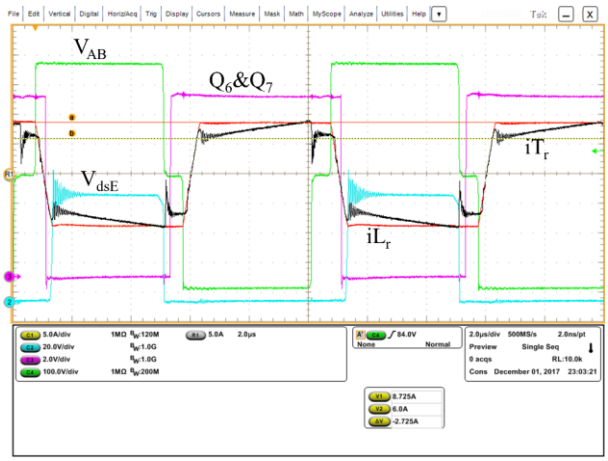


Fig. 21 Full load, steady state forward operation of the 3300W PSFB converter prototype.

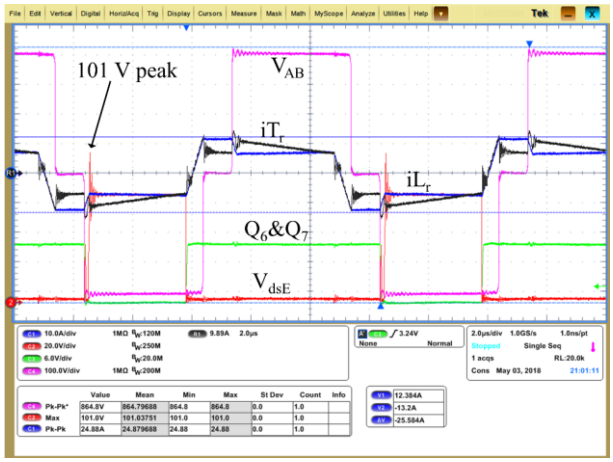


Fig. 22 Capture of the signals during steady state reverse operation of the 3300 W PSFB prototype converter at full load.

Fig. 22 captures the boost mode operation at full load (3300 W), 54.5 V input and 400 V output, leading to approximately 8.25 A average output current. Some details of interest are shown in Fig. 22:

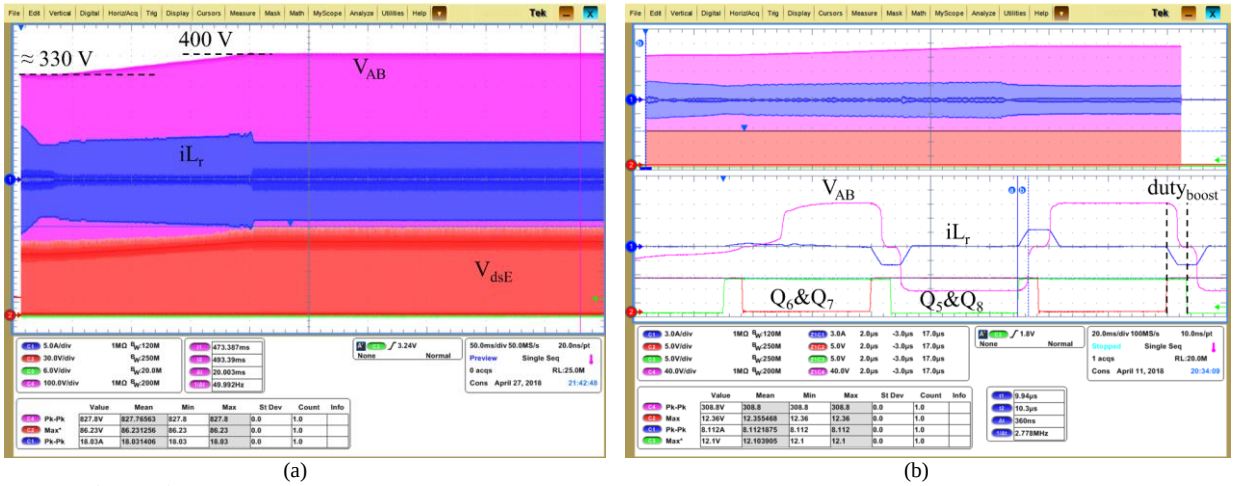
- The primary side bridge operates in ZVS. V_{AB} (pink curve) exhibits higher drain overshoot (432 V) than Fig. 22, but still well under the breakdown limit of the mounted devices (600 V). This is due to the higher turn-off current peak in this operating condition (notice the change in scale of the current waveforms between Fig. 21, 5 A per division, and Fig. 22, 10 A per division).
- The secondary side drain voltage overshoot (red curve) is larger than in forward mode (101 V) but still well under the limit for the selected devices.
- The secondary side devices are hard switched turned-on: there is no delay between the gate signals (green curve) and the drain voltage at the turn-on point, and a closer look at the transition shows the indicative Miller plateau in the gate voltage.
- i_{Lr} is precharged just at the value of the reflected current at the start of the power transfer. Transformer current drops below i_{Lr} during the freewheeling time due to the clamping diodes output charge. The analysis and the experiments have demonstrated that there is a tradeoff between the secondary side voltage overshoot and the primary side circulating current losses given by the so-called precharge.
- In comparison to the forward operation mode, the clamping diodes conduct more current: the area enclosed between i_{Tr} (black curve) and i_{Lr} (blue curve).

C. SOFT START

It was concluded from the analysis in section II that the proposed modulation scheme requires $V_{in''}$ to be equal or larger than V_o (in reverse operation mode the converter can only boost, just like in forward operation mode the converter can only buck). Additionally, by the nature of boost converters, if V_o is lower than $V_{in''}$ the current through the boost inductor (L_o) rises without control (phenomenon commonly known as in-rush current); normally addressed in non-isolated boost converters through parallel negative temperature coefficient (NTC) thermistors and in-rush diodes that charge up the bulk capacitor prior to the converter starts working. However, in isolated boost converters it requires of a more elaborated solution.

Those limitations make the so-called cold start of the converter not possible with the proposed modulation scheme. Some alternatives have been already proposed in the literature: when the bidirectional PSFB is part of a full AC/DC multi-stage converter, it would be possible to integrate the charging up of the bulk capacitance from the AC/DC stage whenever the AC grid voltage is present, like for example in photovoltaic applications; some

other alternatives require additional auxiliary circuitry [16], [25]-[26]. Nevertheless, those matters are out of the scope of this work. Our approach, for testing the prototype, was the charging up of the bulk capacitance prior to the start-up (Fig. 23) through a low power auxiliary supply decoupled from the load and the bidirectional converter by a HV diode.



(a) (b)

Fig. 23 Soft start of converter operating in boost mode. An external auxiliary converter charges up C_o prior to the starting sequence. (a) Zoom out of the sequence followed by steady state operation. (b) Detail of soft start sequence first pulses.

V. CONCLUSION

In this paper a modulation scheme for the operation of the PSFB as a bidirectional DC/DC converter has been proposed to overcome well-known problems on isolated boost converters: high drain voltage overshoot on the secondary or current-fed side devices, and the lack of ZVS capability on the primary or voltage-fed side devices. Furthermore, these issues are addressed without penalties in complexity, cost or performance: the design optimization procedure (selection of the output inductor, leakage or magnetizing inductance among other parameters) is not constrained by the proposed bidirectional operation of the converter.

The main issues and the solutions given by the proposed control techniques have been analyzed in detail. The proposed modulation allows boost operation with minimized drain voltage overshoot equalizing the currents through the boost inductor and other inductances of the converter (L_r, L_{lkg} and stray) prior to a power transfer. Moreover, it enables the usage of primary side clamping diodes, with their advantages in forward or buck operation.

With the proposed modulation the primary side devices achieve full or nearly full ZVS along all load range of the converter in both forward and reverse operation. In addition, a method for extending ZVS range of the lagging leg while operating in boost mode with the proposed modulation has been introduced: precharging the inductances above the minimum required for reducing the overshoot.

In the proposed boost mode operation the secondary side devices are turned-on in hard switching conditions, whereas they are soft switched in buck operation mode. The conduction loss of the primary side clamping diodes is also relatively higher in the boost mode. Those additional contributions to losses, which are the main drawbacks of the modulation presented in this paper, decrease the overall system efficiency of the converter when working in reverse or boost mode in comparison to the forward or buck mode.

A high efficiency prototype of bidirectional 3300 W PSFB was designed and built to demonstrate the feasibility of the proposed solution. The experimental results confirm the analysis introduced in this paper. The prototype achieves a peak efficiency of 98.05 % in the buck mode and 97.5 % in the boost mode at nominal conditions and 50 % load points. Overall, this work demonstrates that the PSFB is a competitive alternative when building highly efficient and cost-competitive bidirectional DC/DC converters.

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CHAPTER 8. SECOND PUBLICATION

Synchronous rectifiers drain voltage overshoot reduction in PSFB converters

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***Abstract*— The requirements for the blocking voltage of the rectification devices on the secondary side of Phase Shift Full Bridge DCDC converter topology are, by nature, higher than for other quasi-resonant or fully resonant topologies (DAB, LLC). This is especially aggravated in wide range operation converters and further increased by the rectifiers' drain voltage overshoot. Unlike other resonant topologies, the inductor at the output of the PSFB effectively decouples the capacitor bank from the rectification stage, which otherwise acts as a strong lossless snubber. Higher blocking voltage requirements for the rectification devices worsen their Figure of Merit, increasing their related losses and decreasing the overall efficiency of the converter. In this paper the main causes of the rectifiers drain voltage overshoots in PSFB are analyzed. Design guidelines for the mitigation of the different causes are introduced, as well as a novel modulation scheme for the overshoot reduction while the output filter operates in DCM, without penalties in performance, complexity or cost. A prototype of PSFB DCDC converter of 3300 W, with 400 V input to 54.5 V output nominal voltages, was designed and built to test the proposed solutions achieving a peak efficiency of 98.12 % at 50 % of load.**

***Index Terms*— Phase Shift Full Bridge, modulation technique, synchronous rectifier, drain voltage overshoot.**

I. INTRODUCTION

The Phase Shift Full Bridge (PSFB) is a buck derived isolated converter topology commonly used in medium to high power (one to several kW) DCDC converter applications as a single stage or as the output stage of a full ACDC converter. PSFB is commonly used with the input at high voltage (350 V to 450 V) and the output at low voltage (12 V to 60 V) and relatively high current for server, telecom and battery charging applications [1]. High output voltage designs are not common since the high-voltage (HV) requirements of the rectification devices on the secondary side make other alternatives more attractive [2]-[3].

Like other resonant or quasi-resonant topologies PSFB can achieve zero voltage switching (ZVS) on the primary side devices, nearly suppressing switching losses, which are especially high for HV devices in hard-switched converters [4]. ZVS enables higher efficiency, lower cost, higher power density or a combination of those.

Like other isolated topologies, the blocking voltage of the secondary side devices depends on the rectification stage configuration: it is two times the transformer reflected secondary voltage for center tapped and current doubler, or one time the transformer reflected secondary voltage for full bridge [5].

Unlike other resonant topologies, the output filter stage of the PSFB converter is composed, at least, of an inductor L_o and a bank of capacitors C_o. The inductor at the output effectively decouples the secondary side rectification devices from the output capacitance bank (Fig. 1). Therefore, the drain voltage of the secondary side devices is not as effectively clamped as in other converters such as LLC or DAB [6]-[8].

Moreover, the secondary reflected voltage of the transformer does not depend on the output voltage (V_o) and it is always necessarily higher than it. In the PSFB converter the output of the rectification stage is a square wave of duty cycle D_{eff}, with the amplitude of the transformer reflected voltage and the average value V_o. The reflected

voltage is proportional to the transformer turns ratio and the input voltage, as expressed in (1) where V_E and V_D represents the amplitude of the output voltage of the rectification stage, and N_P and N_S respectively the primary and secondary turns of the main transformer.

$$V_o = \frac{N_S}{N_P} V_{in} D_{eff} = V_{in} \frac{D_{eff}}{n} = V_D D_{eff} = V_E D_{eff} \quad (1)$$

D_{eff} is necessarily less than or equal to one and, in practical converters, commonly much smaller, as the transformer turns ratio *n* is constrained by the input and output voltage range requirements: the converter should be capable of regulation at the minimum specified input voltage $V_{in,min}$ and maximum specified output voltage $V_{o,max}$.

Wide input voltage is required, for example, during hold-up time conditions [7], [9]-[11]. The power supply needs to maintain its output voltage during a time period of 20 ms (T_{hold}) after the input AC line is lost. Hold-up operation is required in applications with demanding requirements on power supply continuity and reliability, such as sever power supply and telecommunication systems. This results in a minimum input voltage $V_{in,min}$ at the end of T_{hold}.

The wide regulation requirement makes PSFB converter not to be operated with its maximum duty in nominal state. Additionally, because of the time it takes to the current through the transformer to reverse polarity, part of the ideally available duty is lost (D_{loss}), which further constraints the maximum possible transformer turn ratio, the external resonant inductance and the leakage of the transformer, which should be conveniently dimensioned to reach the maximum power of the converter at the minimum specified input voltage (2)-(6). During the remaining duty, the so-called freewheeling (D_{frw}), the primary current recirculates without transferring energy to the output of the converter.

$$D_{loss} = 2F_{sw} \frac{(L_r + L_{lkg})}{V_{in}} \Delta iL_{r,1} \quad (2)$$

$$\Delta iL_{r,1} \approx \frac{2iL_{o,avg}}{n} \ , L_o \text{ in CCM} \quad (3)$$

$$D_{loss,max} = 4F_{sw} \frac{(L_r + L_{lkg})}{V_{in,min}} \frac{iL_{o,avg,max}}{n} \quad (4)$$

$$D_{eff} + D_{frw} + D_{loss} = 1 \quad (5)$$

$$D_{frw} \geq 0 \xrightarrow{\text{yields}} V_{in,min} \geq \left(nV_{o,max} + \frac{4F_{sw}(L_r + L_{lkg}) iL_{o,avg,max}}{n} \right) \quad (6)$$

Any additional overshoot above the nominal blocking voltage (V_D and V_E) would require to further increase the maximum limits of the blocking voltage capabilities of the rectification devices (Fig. 2); or alternatively to use clamping or snubbering mechanisms that bring additional power losses, complexity and cost [12]-[13]. Furthermore, it is a common practice, in the design of switched mode power supplies (SMPS), to limit the maximum stress on the components (voltage, current, temperature) to a rated percentage of their safe maximum limits under any normal working conditions of the converter [14]. The rating percentage depends on the application, lifetime and reliability requirements, but 80 % is a common choice. For semiconductor devices the commonly rated parameters are the maximum drain voltage and the working temperature.

Because there is only a limited variety of voltage classes available in the market, increasing the blocking voltage may force the designer to go for a rather high voltage class where the available device technology has a worse figure of merit and could be further constrained to a limited $R_{ds,on}$ portfolio. A summary of the characteristics of two devices with similar $R_{ds,on}$ in Table I shows the influence of the blocking voltage in their characteristic charges and forward voltage drop, which ultimately affects the switching and conduction losses.

In PSFB converters several mechanisms induce or could induce the above mentioned secondary side rectifiers drain voltage overshoot [5], mostly not properly explored in the literature. In the following sections we analyze the most common causes, and provide design guidelines and control solutions for the reduction or suppression of the parasitic overshoots enabling high efficiency PSFB designs with the minimum possible secondary side voltage class devices. The rectification stage may have different configurations: center tapped, current doubler or full bridge; each of them having its advantages in different applications: low voltage, high current or high voltage outputs respectively [15]; however these alternatives have no major impact on the working principles of the converter and the solutions proposed here.

TABLE I
SI LV MOSFETS

	BSC093N15NS5	BSC098N10NS5
$V_{DS,max}$	150 V	100 V
$R_{DS,on,max}$	9.3 mΩ @ 25 °C	9.8 mΩ @ 25 °C
Q_{oss}	91 nC	30 nC
Q_g	33 nC	22 nC
Q_{rr}	58 nC	73 nC
V_f	0.88 V	0.9 V

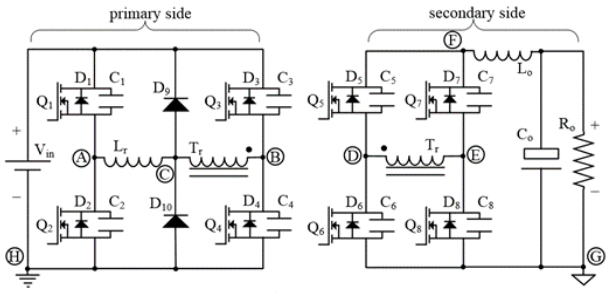


Fig. 1. Conventional phase shift full bridge DC/DC converter configuration with full bridge rectification and primary side clamping diodes.

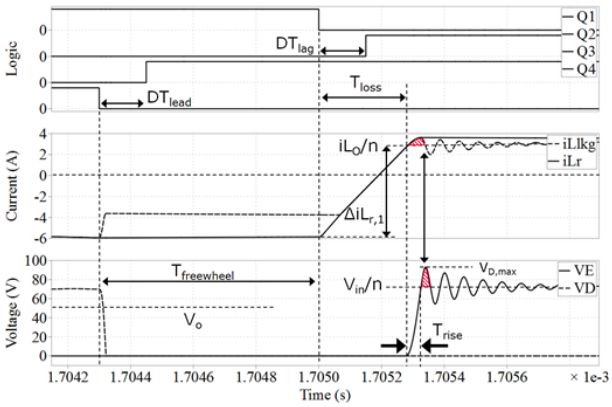


Fig. 2. Secondary side drain voltage overshoot increases the blocking voltage requirements for the rectification devices.

The rest of this document is organized as follows: in Section II a detailed analysis of the overshoot causes is conducted and previous literature is reviewed; in Section III a comprehensive analysis of the proposed overshoot reduction techniques are presented including a novel discontinuous conduction mode (DCM) control scheme; the study is confirmed by experimental results presented in Section IV; and finally, Section V presents a summary of conclusions out of this work.

II. OVERSHOOT MECHANISMS ANALYSIS

A. COMMUTATION OVERSHOOT

The secondary side rectification devices are naturally commutated by the transformer reflected voltage, which is an effect of the primary side devices alternating the polarity of the voltage applied to the primary of the transformer. Thanks to that, the synchronous rectifiers (SRs) can be turned both on and off under ZVS conditions. They are, however, hard commutated and because certain body diode conduction is unavoidable in most practical cases, they require reverse recovery charge (Q_{rr}) for the diodes with the consequent additional related losses [16]-[17].

The energy required to charge the output capacitance (Q_{oss}) and Q_{rr} of the rectification devices during their commutation comes from the primary side through the transformer. Meanwhile, in the process of charge, all inductances appearing on the charging path (L_r, L_{lkg}, L_{stry}) (Fig. 3) store energy, which can be estimated by (7). That stored energy will subsequently cause a resonance together with the secondary side rectifier's output capacitance (C_{oss}) at the frequency given by (8) [5]. The energy of that resonance would cause a maximum peak voltage that can be calculated by (9)-(10). Subsequently the resonance energy will be partially lost in the resistive path as the resonance dampens or within other snubber, or clamping mechanisms [12].

$$\left.\begin{matrix} Q_{oss,5}=Q_{oss,6}=Q_{oss,7}=Q_{oss,8}=Q_{oss} \\ Q_{rr,5}=Q_{rr,6}=Q_{rr,7}=Q_{rr,8}=Q_{rr} \end{matrix}\right\} \xrightarrow{\text{yields}} \left(\frac{iL_{r,com}^2}{2}L_r+\frac{iL_{lkg,com}^2}{2}L_{lkg}\right)=\frac{V_{in}}{n}(Q_{rr}+Q_{oss}),t_1=\frac{\pi}{2\omega_1} \quad (7)$$

$$C_5=C_6=C_7=C_8=C_{SR} \xrightarrow{\text{yields}} \omega_1=\frac{1}{\sqrt{2C_{SR}(L_{lkg}+L_r)}} \quad (8)$$

$$V_F(t)=V_E(t)=V_D(t)=V_{F,pk}(1-\cos(t\omega_1)) \quad (9)$$

$$V_{F,pk}=\left(\frac{iL_{F,com}^2}{2Q_{oss}}L_r+\frac{iL_{lkg,com}^2}{2Q_{oss}}L_{lkg}\right)+\frac{V_{in}}{n},t_2=\frac{\pi}{\omega_1} \quad (10)$$

High frequency and high amplitude resonances can jeopardize driver and power switch integrity, and often cause electromagnetic interference (EMI) issues because of their high *dv/dt* and *di/dt* nature. The common mode

(CM) noise of SMPS, which propagates in phase through both the power lines and returns from the ground, is mainly associated with high *dv/dt* nodes in the circuit and the parasitic capacitance between these nodes and ground. The CM noise characteristic of the converter is therefore determined by the voltage spectrum characteristics of the voltage pulsating nodes in the circuit [18]. The ringing is known to cause broadband EMI problems, the frequency of which is centered at the ringing frequency [19]-[20].

In [21] the analysis of the commutation resonance includes L_r, the parasitic capacitance and leakage of the transformer, the parasitic capacitance of the rectifier, and the capacitor of a snubber in a fifth-order model. This implies that the voltage ringing across the rectifiers should be a waveform including more than one frequency component. However, aside from the limited effectivity and applicability of the proposed method, the fact that only a small amount of the resonance could be cancelled probes the minor contribution of the other frequency components.

The traditional RC dampening snubber is not frequently used because of its large losses. Alternatively, an RCD snubber circuit limits the peak voltage of the resonance and its dampening with acceptable losses [22]-[23]. However, the design of the RCD network is not straightforward and requires a tradeoff between effectivity and power losses (11).

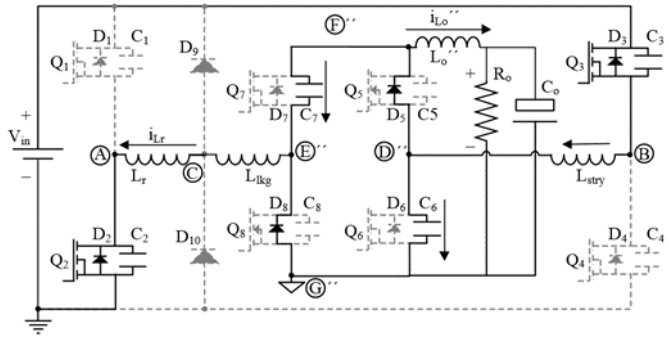


Fig. 3. Simplified equivalent circuit of the converter during the commutation of Q_6 and Q_7.

$$E_{RCD} \propto \left(V_{F,pk} - \frac{V_{in}}{n}\right) Q_{oss} \tag{11}$$

A comparison of considered "lossless" snubber circuits is presented in [12] and [24]. These circuits recover part of the clamped oscillation energy and consist entirely of a combination of passive components: diodes and capacitors. However, they are difficult to optimize for wide range converters: the resulting peak voltage overshoot depends on the effective duty of the converter. The best result is obtained with a combination of a diode and extra windings on the secondary side of the transformer, which complicates the manufacture of the magnetics and the layout of the board. The same working principle is applied with less complexity in [25] where the clamping diodes are placed on the primary side winding of the transformer.

An active clamp circuit on the secondary side consisting of an additional switch and a capacitor was proposed in [26]-[27]. While the solution seems promising, it has the added complexity of controlling an extra active switch in the converter. Furthermore, the related additional losses cannot be neglected: conduction and switching losses of the switch, and charge-discharge loss of the snubber capacitor. Another alternative snubber configuration is proposed in [28] where the additional switch is placed in the main path of the current at the output. However, the placement is not practical for converters with low voltage and high current outputs.

In [29]-[30] a regenerative Flyback converter replaces the resistor in an RCD snubber circuit thus recovering part of the energy. Additionally, this Flyback provides isolation and enables soft-start capability of the proposed bidirectional converter in [29]. The active regenerative snubber concept can be extended to other isolated or non-isolated topologies. In [31] a non-isolated buck converter feeds the clamped oscillation energy to the output of the converter. However, the conclusion in [30] is that the extra complexity does not justify the efficiency improvement considering that the traditional RCD snubber demonstrates to be far more effective reducing the voltage overshoot.

B. DCM OVERSHOOT

Under certain load conditions the average output current of the converter becomes lower or equal than half of the current ripple through L_o, which can be calculated with (12), where F_{sw} represents the switching frequency of the converter. In this scenario there are three main alternatives for the operation of the converter [17]:

- The output filter works naturally in DCM. This is the case of converters with passive rectification devices, like diodes, or not enabled active devices taking advantage of their intrinsic body diode.
- The output filter works in DCM but the SRs are enabled and driven in a similar manner to ideal diodes. This mode increases the efficiency of the converter, at least along certain load range where the additional driving losses are compensated by the reduction in forward voltage drop (Fig. 4).

- The output filter is forced to work in continuous conduction mode (CCM) when the active rectification devices are driven maintaining the same standard CCM modulation scheme along all load range.

$$\Delta I_{Lo,CCM} = V_o \frac{(1-D_{eff})}{2F_{sw}L_o} \tag{12}$$

A potential problem arises when the converter operates in any of the above mentioned DCM modes and L_o resonates back together with the output capacitance of the rectification devices. The maximum induced peak voltage of this resonance can be as high as twice the output voltage of the converter.

At the start of the resonance both the energy in L_o and the output capacitance of the rectifiers is zero (13). When the output capacitance of the rectifiers has been charged up to V_o, equal energy has been stored in L_o and the capacitors (14)-(15). Subsequently all the energy in L_o flows into the output capacitance of the devices (16).

$$E(t_0) = E_{Lo}(t_0) + E_{Csr,total}(t_0) = 0 \tag{13}$$

$$\omega_2 = \frac{1}{\sqrt{4C_{oss}L_o}} \ , \ t_1 = \frac{\pi}{2\omega_2} \ , \ t_2 = \frac{\pi}{\omega_2} \tag{14}$$

$$E(t_1) = E_{Lo}(t_1) + E_{Csr,total}(t_1) = \frac{1}{2}L_o I_{Lo}^2 + \frac{1}{2}2Q_{oss}V_o \tag{15}$$

$$E(t_2) = E_{Lo(t_2)} + E_{Csr,total}(t_2) = 0 + 2Q_{oss}V_o \tag{16}$$

In a full bridge rectification stage configuration the peak voltage of the above mentioned DCM overshoot is blocked by two stacked devices and it is likely to be distributed near equally between them (considering all devices have near equal output capacitance) (17). For the center tapped or current doubler configurations the devices are anyhow dimensioned to block at least two times the transformer reflected voltage [5]. It follows that, in any of those scenarios the induced DCM resonance peak voltage is well under the blocking voltage limits for the secondary side devices already considered in normal working conditions.

$$\begin{cases} V_F(t) = 2V_o\,(1-\cos(t\omega_2)) \\ V_E(t) = V_D(t) = V_o\,(1-\cos(t\omega_2)) \end{cases}, V_{CB} = 0 \tag{17}$$

However, in the special case where the commutation of the rectification devices occurs in the middle of a DCM resonance, the voltage already stored in their C_{oss} effectively stacks on top of the transformer secondary reflected voltage, now likely exceeding the nominal blocking voltage limits (18). Additionally, the previously described commutation overshoot will also appear in a cumulative manner to this mechanism.

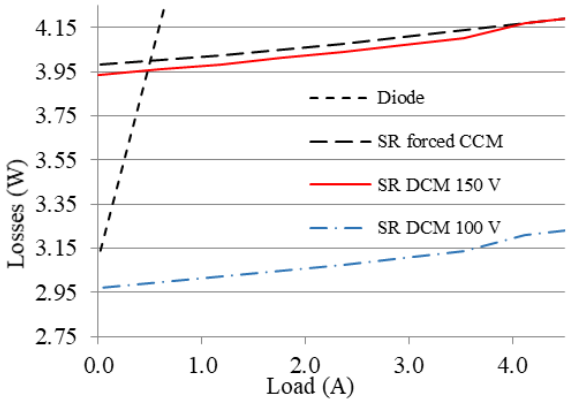


Fig. 4. Comparison of losses between the alternative operation modes of the SRs at light load. The estimated values account for the driving, switching and conduction losses of the SRs of the converter prototype in section IV.

$$\begin{cases} V_E(t) = V_o\,(1-\cos(t\omega_2)) + \frac{V_{in}}{n} \\ V_D(t) = V_o\,(1-\cos(t\omega_2)) \end{cases}, V_{CB} = V_{in} \tag{18}$$

C. FORCED CCM OVERSHOOT

If the converter works in forced CCM but the active rectifiers happens to turn-off while the current through L_o is flowing back against their intrinsic body diodes, the current path becomes blocked and the energy stored in L_o instead charges up the output capacitance of the devices (Fig. 5). Like in the previously described DCM overshoot scenario, the mechanism of these phenomena is a resonance between L_o and the output capacitance of the SRs. However, since in forced CCM the current through L_o becomes more negative than during DCM operation, there would be more energy stored at the start of the resonance (19). The induced drain voltage overshoot easily becomes large enough to reach the drain voltage breakdown limit of the rectification devices (20)-(21).

$$E_{Lo}(t_0) = \frac{1}{2} L_o I_{Lo}^2(t_0) \gg 0 \quad , \quad E_{Csr,total}(t_0) = 0 \tag{19}$$

$$E(t_2) = E_{Lo}(t_2) + E_{Csr,total}(t_2) = 0 + E_{Lo}(t_0) \tag{20}$$

$$\begin{cases} V_F(t) = \frac{L_o I_{Lo}^2(t_0)}{4Q_{oss}} (1 - \cos(t\omega_2)) + \frac{V_{in}}{n} \ , \ V_{CB} = V_{in} \\ V_F(t) = \frac{L_o I_{Lo}^2(t_0)}{4Q_{oss}} (1 - \cos(t\omega_2)) \ , \ V_{CB} = 0 \end{cases} \tag{21}$$

To avoid this problem it is required that the SRs always turn-off while the current through L_o is positive (flowing towards the output of the converter), zero or nearly zero. The controller has to ensure that the transition from CCM to DCM operation happens before the output inductor current changes polarity or to ensure a proper turn-off sequence when the converter operates in forced CCM.

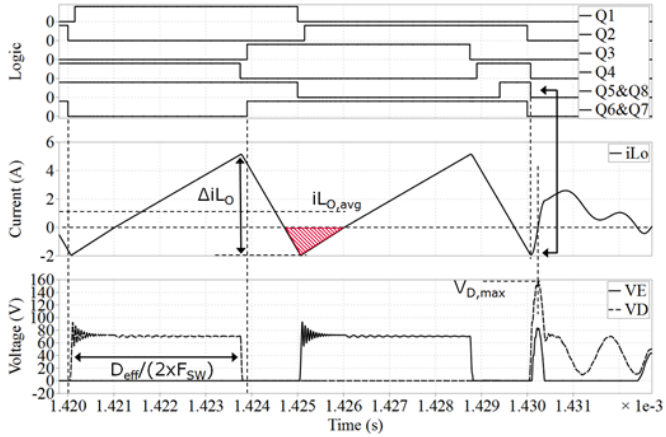


Fig. 5. Forced CCM. Induced drain voltage overshoot when the SRs are turned-off while iL_o is lower than zero.

III. OVERSHOOT REDUCTION TECHNIQUES

A. COMMUTATION OVERSHOOT REDUCTION

The use of an external resonant inductance (L_r) in the primary side of PSFB, while increasing the component count, helps achieving ZVS in light to medium load conditions and thus increases the overall efficiency of the converter. Although it is possible to increase the leakage of the transformer for the same purpose, using an external resonant inductance on the primary side of the converter and placing clamping diodes between the transformer and L_r helps to reduce the secondary side rectifiers overshoot as well as reducing their switching/commutation related losses [25], [32]. The solution, previously reported in the literature, is analyzed in detail in this section.

It has been mathematically demonstrated in [33]-[34] that charging a capacitor inevitably causes energy losses. When charged through a resistive path the resistor dissipates energy equal to the one eventually stored (22)-(24). The analysis shows that a capacitor can be charged with only a modest energy loss in a series RLC circuit only if the source is disconnected after one half of a resonance cycle. Otherwise the remaining energy is dissipated during the dampening of the resonance and the energy loss becomes also equal to the stored. Their analysis is consistent with the formula for the estimation of switching losses in SRs in [35].

$$E_{sourced} = E_{stored} + E_{loss} = (2Q_{oss} + 2Q_{rr}) \frac{V_{in}}{n} \tag{22}$$

$$E_{loss,1} = (Q_{oss} + 2Q_{rr}) \frac{V_{in}}{n} \quad , \quad E_{stored} = Q_{oss} \frac{V_{in}}{n} \tag{23}$$

$$P_{sw} = 2F_{sw}(Q_{oss} + 2Q_{rr})V_F \tag{24}$$

During the charge of Q_{rr} and Q_{oss} in the secondary side rectification devices an equal energy is stored in the inductances along the charging path (L_r, L_{lkg}, L_{stray}). It follows that the bigger L_r is in relation to the other inductances (L_{lkg} and L_{stray}) the more energy it stores comparatively. Due to the action of the primary side clamping diodes, the energy in L_r is actually recirculated on the primary side of the converter and does not contribute to the secondary side commutation resonance.

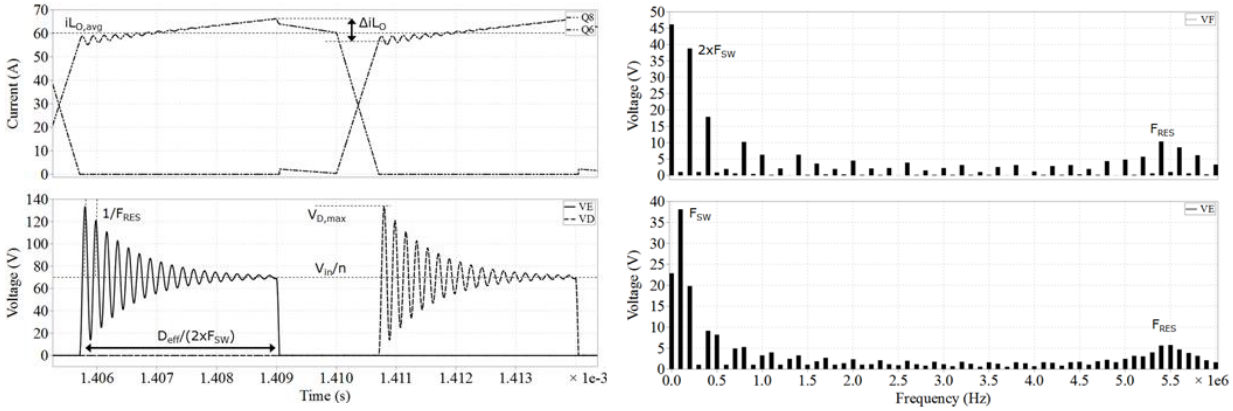


Fig. 6. Spectrum of SRs voltage and current without camping diodes on the primary side.

Additionally, an increase in the overall inductance along the charging path decreases the transformer and secondary side devices *di/dt* during the commutation, which is known to reduce Q_{rr} related losses in diodes [35]-[36].

Both of these mechanisms contribute to the reduction of Q_{oss} and Q_{rr} related losses in the SRs (25)-(26) as well as to the reduction of the commutation drain voltage overshoot, which can be estimated by (27)-(28), where $iL_{r,com}$ and $iL_{lkg,com}$ represents the current passing through the inductances at their peak during the first cycle of the resonance. The conduction loss of the clamping diodes E_{clmp} can be estimated from their average current, which is analyzed in the next section.

$$E(t_1) = \left(\frac{iL_{r,com}^2}{2}L_r + \frac{iL_{lkg,com}^2}{2}L_{lkg}\right) = (Q_{oss} + Q_{rr})\frac{V_{in}}{n} \;,\; t_1 = \frac{\pi}{2\omega_1} \tag{25}$$

$$E_{loss,2} = \frac{V_{in}}{n}\left(Q_{oss}\frac{L_{lkg}}{L_r} + Q_{rr}\left(1 + \frac{L_{lkg}}{L_r}\right)\right) + E_{clmp} \tag{26}$$

$$\omega_3 = \frac{1}{\sqrt{2C_{oss,sr}L_{lkg}}} \tag{27}$$

$$V_F(t) = \frac{iL_{lkg,com}^2 L_{lkg}}{2Q_{oss}}(1 - \cos(t\omega_3)) \tag{28}$$

Fig. 6 and Fig. 7 compare the waveforms and the drain voltage spectrum of the secondary side rectifiers for two converters with the same total value of inductances in the commutation path (L_r plus L_{lkg}). Both converters are operating in the same conditions, however, the converter in Fig. 7 uses clamping diodes in the primary side and has maximized its ratio of L_r to L_{lkg}.

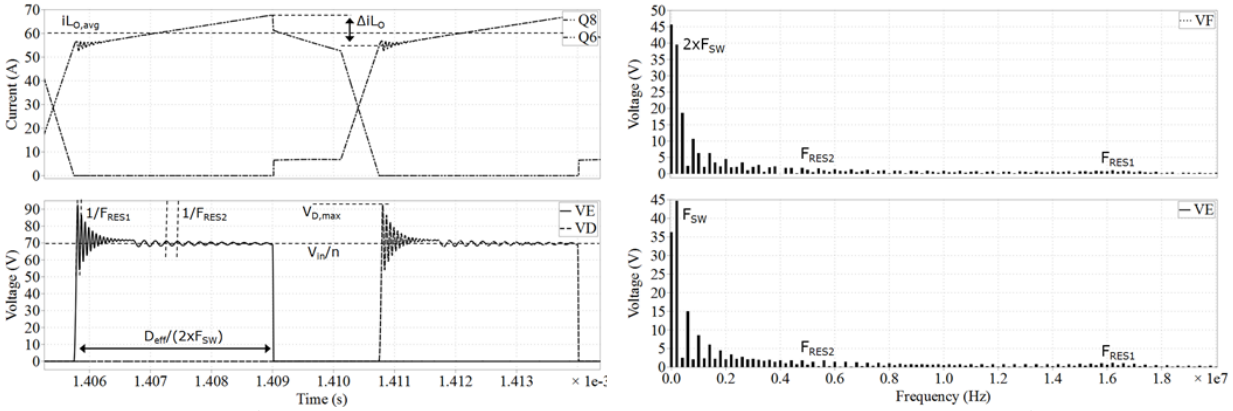


Fig. 7. Spectrum of SRs voltage and current with clamping diodes on the primary side and maximized ratio of L_r to L_{lkg}.

B. DCM OVERSHOOT SUPPRESSION

The output filter of the converter could be dimensioned in a way to ensure CCM or DCM in the boundary to CCM operation in all working conditions. This is however impractical in high efficiency converters, as it is difficult to design an efficient high value of inductance [2]. In this work we propose a solution to the induced DCM overshoot consisting of a novel modulation scheme, which does not constrain the converter design or its performance in any manner.

The key strategy is to use active rectification to overcome the DCM overshoot problem (Fig. 8). Switching on the devices prior or during the buildup time of the transformer secondary reflected voltage allows the output

capacitance of the rectification devices to be discharged out from the DCM resonance energy (Fig. 9). The discharge of the precharged voltage limits the overshoot to that of a normal commutation, as in any other operating condition of the converter.

With the proposed modulation scheme the secondary side devices become hard switched. However, the switched voltage depends on the turn-on instant during the resonance, which maximum amplitude was demonstrated to be V_o. This makes it difficult to estimate the related losses in a real application. The worst possible scenario can be estimated by (29).

$$P_{sw,DCM} = 2F_{sw}\left(E_{loss,2} + 2Q_{oss}V_o\right) \tag{29}$$

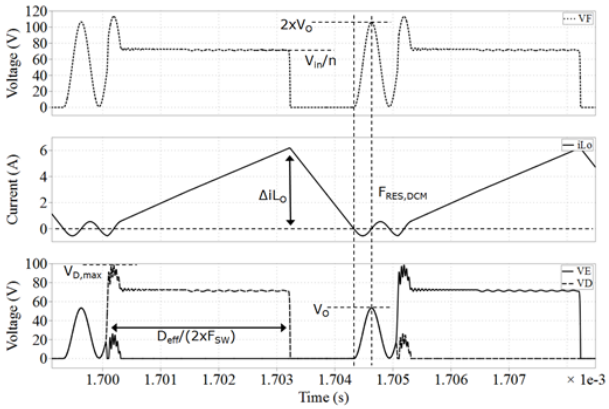


Fig. 8. Secondary side DCM overshoot where commutation occurs at the peak of L_o and C_{oss} resonance.

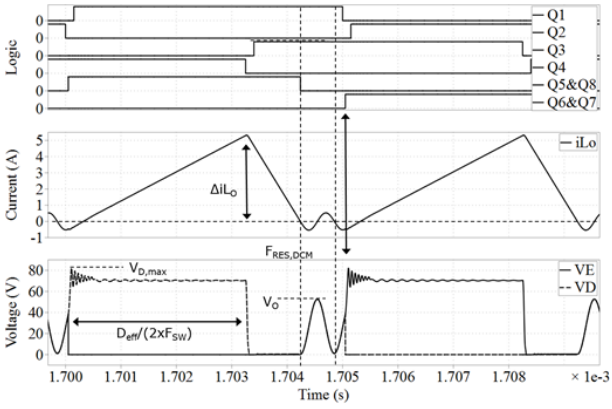


Fig. 9. Secondary side DCM overshoot where commutation occurs at the peak of L_o and C_{oss} resonance with the proposed modulation scheme applied.

IV. DCM PROPOSED MODULATION SCHEME

A. DCM MODULATION ANALYSIS

Fig. 10 shows the main driving signals and waveforms of a standard modulation scheme for PSFB in Tr-lead configuration [32] with external resonant inductance and clamping diodes in the primary side, as exemplified in Fig. 1. In Fig. 10, the converter operates at a load point where the output filter is working in CCM and where the secondary side SRs are enabled and driven with a standard CCM modulation. The so-called freewheeling time [t_3, t_5] is relatively long as it is the case for most practical designs with a wide input and/or output voltage range. Currents through L_r (iL_r) and through the transformer T_r (iT_r) differ due to the action of the clamping diodes D_9 and D_{10} diverting the L_r current after charging the secondary side rectifiers Q_{oss} and Q_{rr} at the start and at the end of a power transfer ([t_1], [t_3], [t_7] and [t_{10}]).

Fig. 11 shows the main driving signals and waveforms of the proposed modulation scheme for the same converter in Fig. 1 while the output filter operates in DCM. In the example of Fig. 11 there is a single resonance period between the SR capacitance and L_o. In this scenario the stored voltage in C_{oss} is at its minimum value at the start of a new power transfer, which is the best possible case. However, the point within the resonance where the converter commutates varies depending on many factors (converter load, duty cycle, frequency of DCM resonance, etc.) that cannot be easily estimated or ensured by the controller. The novel solution we propose here is independent of the commutation point within the resonance, does not require additional measurements by the controller and can be tuned based on design parameters.

In the following we analyze the operation principle of the proposed novel DCM operation of the PSFB. Before the analysis some assumptions are made: 1) all diodes and switches are ideal; 2) all switches are MOSFETs with intrinsic anti-parallel body diode; 3) all capacitors and inductors are ideal; 4) C_1=C_2=C_3=C_4, C_5=C_6=C_7=C_8.

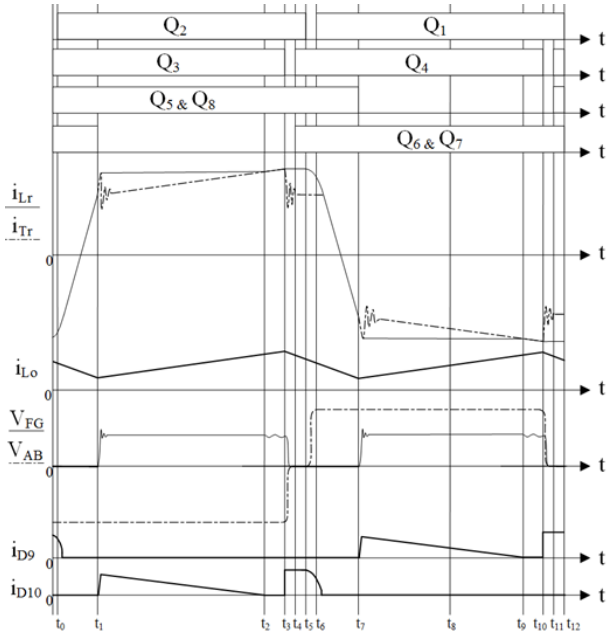


Fig. 10. Main signals in the circuit for the proposed forward operation of PSFB with output filter working in CCM.

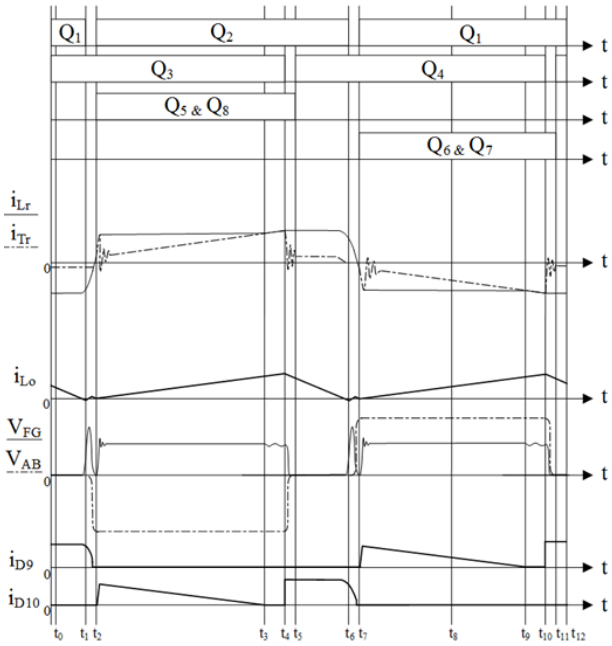


Fig. 11. Main signals in the circuit for the proposed forward operation of PSFB with the output filter working in DCM.

1) Mode 1 [t2, t3] [Fig. 12(a)] - Deff

During this stage the power is being transferred from the primary to the secondary. A single secondary side rectification branch conducts while the complementary branch blocks the reflected voltage of the transformer.

The current through the external resonant inductance iL_r rises above the reflected primary side current of the transformer i_{Tr} due to the charge of the rectifier's Q_{oss} and Q_{rr} at the start of the power transfer (30)-(34). Thanks to the primary side clamping diodes, the additional energy stored in L_r is diverted and freewheels through Q_2 and D_{10} (35).

$$iL_r(t) = iL_r(t_2) + iL_{r,comm},\ t_2 < t < t_3 \tag{30}$$

$$iL_{r,comm} = \sqrt{\frac{2V_{in}}{n(L_r+L_{lkg})}(Q_{rr}+Q_{oss})} \tag{31}$$

$$\begin{cases} iL_r(t_2) = \frac{iL_{o,avg}-\frac{\Delta iL_o}{2}}{n} - \frac{D_{eff}V_{in}}{L_m 2F_{sw}}\ , CCM \\ iL_r(t_2) = iL_m(t_2) = -\frac{D_{eff}V_{in}}{L_m 2F_{sw}}\ ,\ DCM \end{cases} \tag{32}$$

$$iL_{Tr}(t) = \frac{iL_o(t)}{n} + \frac{iL_{r,comm}L_{lkg}}{(L_r+L_{lkg})}(1-\cos(t\omega_3)) + iL_m(t)\ ,\ t_2 < t < t_3 \tag{33}$$

$$\begin{cases} iL_o(t) = iL_o(t_2) + \frac{\left(\frac{V_{in}}{n}-V_o\right)}{L_o}t\ ,\ CCM \\ iL_o(t) = \frac{\left(\frac{V_{in}}{n}-V_o\right)}{L_o}t\ ,\ DCM \end{cases},\ t_2 < t < t_4 \tag{34}$$

$$iD_{10}(t) = iL_r(t) - iL_{Tr}(t),\ t_2 < t < t_3 \tag{35}$$

2) Mode 2 [t3, t4] [Fig. 12(b)] - Deff

At t_3 the current through the external resonant inductance (iL_r) and through the primary side of transformer (iT_r) becomes equal and D_{10} stops conducting (36). The voltage at the node C (V_C) is no longer clamped to one of the primary side supply rails, as could be appreciated by the secondary reflected voltage oscillations (V_F). Notice, however, that D_{10} does not necessarily stop conducting during the interval [t_2, t_4], it depends on the converter duty, peak value of iL_r and the slopes of iL_r and iT_r [25].

$$iL_r(t) = iL_{Tr}(t) = \frac{iL_o(t)}{n} + iL_m(t),\ t_3 < t < t_4 \tag{36}$$

The current through the output inductor (L_o) keeps rising, as so does the reflected primary current through the transformer. The external resonance inductor current iL_r equals that of the transformer and rises as well: L_r and

the reflected output filter impedance effectively form a voltage divider, but since the reflected output impedance is much larger than L_r, as exemplified in (37)-(38), this effect can be normally neglected, especially in step down converters.

$$L_{o,,} = L_o n^2 \tag{37}$$

$$N_P > N_S \xrightarrow{\text{yields}} L_{o,,} \gg L_r \xrightarrow{\text{yields}} V_{in} = V_{BC} + V_{CA} \approx V_{BC} \tag{38}$$

3) Mode 3 [t4, t6] [Fig. 12(c), Fig. 12(f)] - Dfreewheel

Q_3 turns-off at t_4 forcing the current flowing through L_r and L_o to discharge C_4 and to charge C_3. Since V_{AB} decreases towards zero, so does the reflected transformer voltage V_{DE} forcing as well the discharge of Q_6 and Q_7 output capacitances (C_6 and C_7) on the secondary side. The discharging of C_6 and C_7 distributes iL_o between the secondary side rectification branches, not necessarily and, normally, not equally. Because part of iL_o does not pass through the secondary side of the transformer after this redistribution, the primary reflected iT_r decreases proportionally (39)-(40). However, iL_r remains nearly constant due to the action of D_{10} (41)-(42).

$$iL_{Tr}(t) = iL_{Tr}(t_4) - iL_{lkg,OFF}\ ,\ t_4 < t < t_6 \tag{39}$$

$$iL_{lkg,OFF} = \sqrt{\frac{V_{in}}{nL_{lkg}} 2Q_{oss}} \tag{40}$$

$$iL_r(t) \approx iL_r(t_4),\ t_4 < t < t_6 \tag{41}$$

$$iD_{10}(t) = iL_r(t) - iL_{Tr}(t),\ t_2 < t < t_3 \tag{42}$$

At some point during this interval C_4 is fully discharged and C_3 fully charged. The intrinsic body diode of Q_4 becomes then forward biased and carries all iT_r. Notice that the intrinsic body diode of Q_4 does not necessarily conduct before t_5, especially at light load conditions where the available energy for the transition is low, and most likely the case in Fig. 11 scenario where the output filter works in DCM. At t_5 Q_4 turns-on and the channel of the device carries all the current iT_r.

On the secondary side C_6 and C_7 have become equally discharged and the intrinsic body diode of all the rectifier transistors conduct part of the output current, effectively shorting the transformer.

During this stage, the so-called freewheeling, the primary current recirculates through the two lower HV bridge devices (the two upper in the alternate polarity sequence) without actually transferring energy to the output of the converter. The secondary side devices continue sharing the output current (43)-(44), although most of it flows through D_5 and D_8.

$$iL_o(t) = iL_o(t_4) - \frac{\left(\frac{V_{in}}{n} - V_o\right)}{L_o} t\ ,\ t_4 < t < t_6 \tag{43}$$

$$iL_o(t_4) = iL_{o,pk} \tag{44}$$

In Fig. 11 Q_5 and Q_8 turn-off at the start of the freewheeling stage. This simple approach, despite not being optimum in terms of efficiency, does not require the estimation or measurement of iL_o zero crossing and prevents the above mentioned forced CCM overshoot. Some other common alternative modulation schemes include [17]:

- Delaying the turn-off of the SRs after the end of a power transfer by an estimated falling time of L_o current to zero.
- Sensing the current through L_o or through the SRs by the controller that turns-off at zero crossing, perfectly mimicking the behavior of an ideal diode.

Near t_6, iL_o crosses zero and starts to flow back charging up all the secondary rectifiers output capacitance. Since the devices output capacitances are equal, charge and voltage will be equally distributed among all of them.

4) Mode 4 [t6, t7] [Fig. 12(g), Fig. 12(i)] - Dloss

Q_2 turns-off at t_6 and the current flowing through L_r plus L_{lkg} charges C_2 and discharges C_1.

The resonance between L_o and the output capacitance of the SRs continues as could be observed in the V_F waveform in Fig. 11. The frequency of the oscillation depends on the value of those two components (45), relatively slow in comparison to the commutation overshoot phenomena. Due to this low frequency, the dampening effects of the circuit impedances are less noticeable.

$$iL_o(t) = \sqrt{\frac{4Q_{oss}V_o}{L_o}} (1 - \cos(t\omega_2))\ ,\ t_6 < t < t_7 \tag{45}$$

At certain point during this mode C_2 could become fully charged and C_1 fully discharged. If this occurs, the intrinsic body diode of Q_1 starts conducting the current through the external resonant inductor iL_r. Near t_7 Q_1 is

turned-on, ideally in ZVS conditions if there was enough energy stored in L_r prior to the transition. iL_r reverses polarity (46)-(48) and, since there is near zero reflected current, right after crossing the magnetizing current, the voltage starts to build up on the primary side of the transformer and, at the same time, on its secondary side.

$$iL_r(t) \approx iL_r(t_4) - \frac{V_{in}}{(L_r+L_{lkg})}t \ , \ t_6 < t < t_7 \tag{46}$$

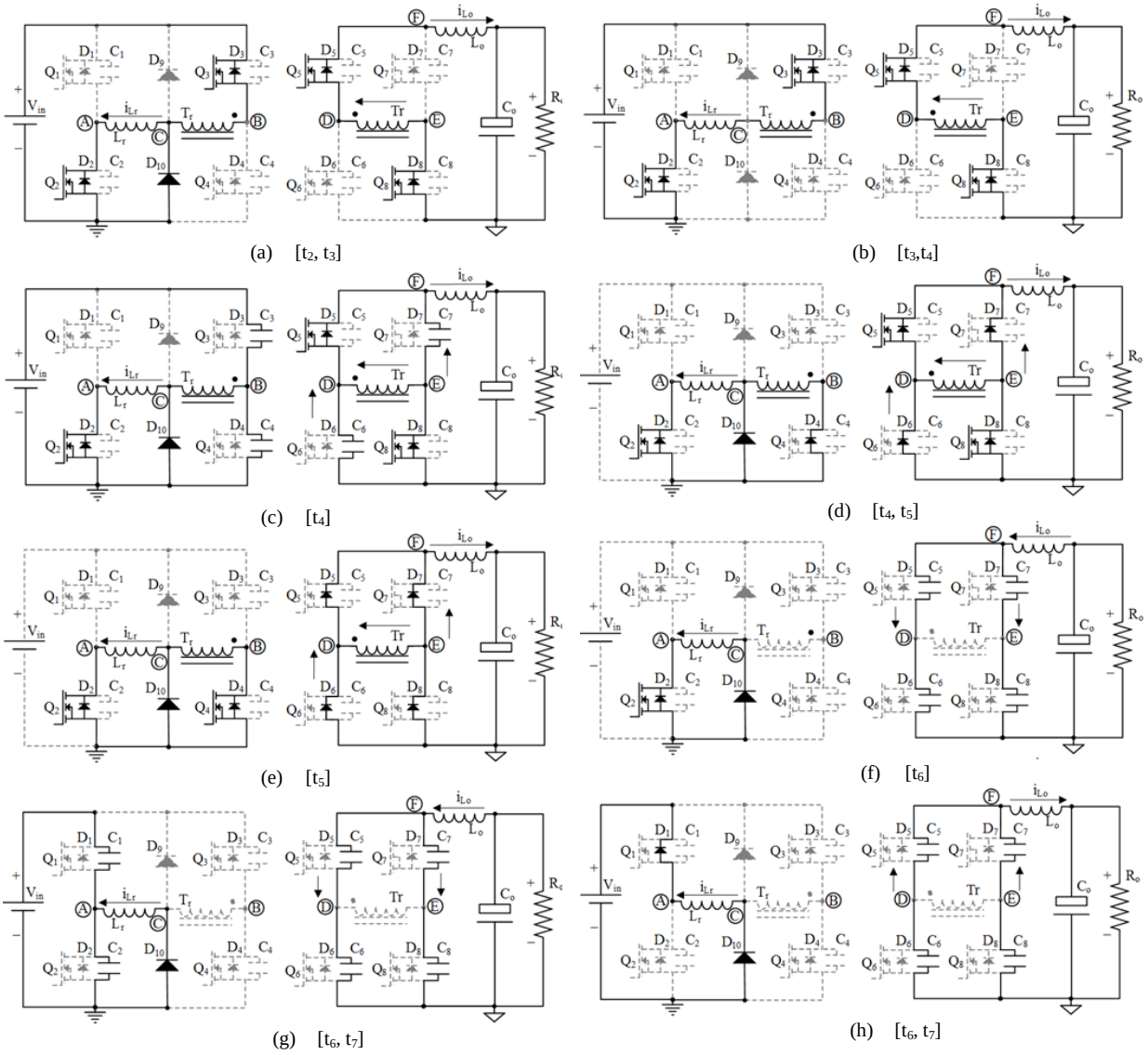
$$iL_{Tr}(t) = iL_r(t) \ , \ t_x < t < t_7 \text{ with } t_6 < t_x \tag{47}$$

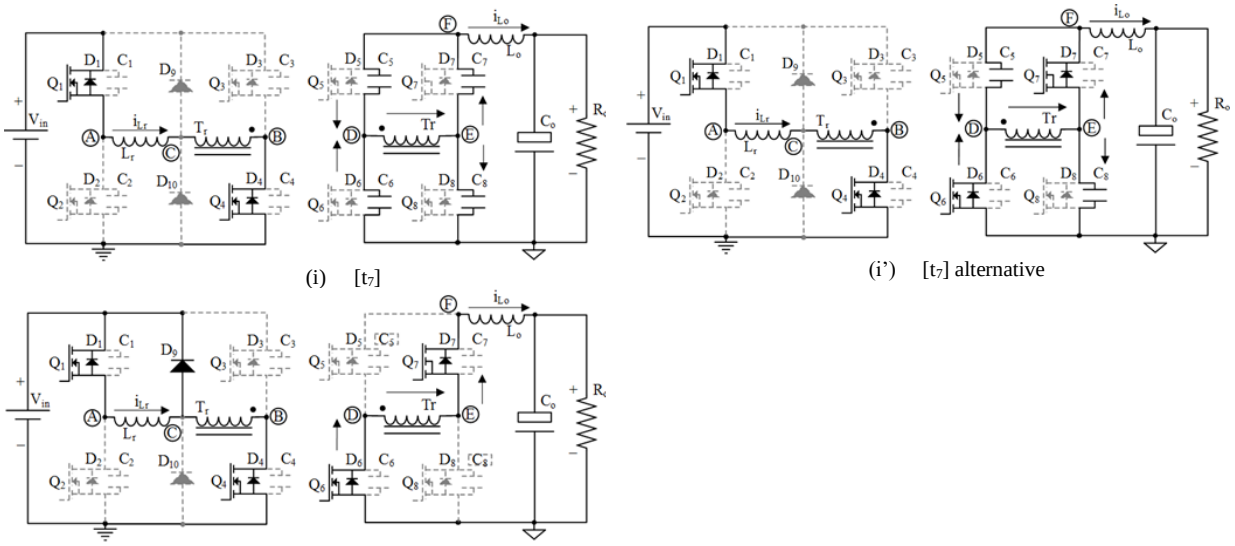
$$iD_{10}(t) = 0 \ , \ t_x < t \tag{48}$$

$$T_{rise} = \pi\sqrt{(L_r + L_{lkg})2C_{oss}} \tag{49}$$

In Fig. 12(i), before the proposed solution is applied, the secondary side voltage builds up on top of the already precharged capacitances C_5 and C_8 (Fig. 8). However, in Fig. 12(i'), with the proposed modulation scheme, around t_7, while the voltage of transformer builds up, the secondary side rectifying branch about to conduct is turned-on (Fig. 9). In this scenario Q_6 and Q_7 are hard switched and the energy of their output capacitances C_6 and C_7 is dissipated within these two devices. Subsequently V_F equals to the rising reflected voltage of the transformer V_{DE}.

It is crucial for the effectivity of the solution that the switching on point of Q_6 and Q_7 falls within the building up time of the reflected voltage. The time constant of the rising time depends on L_r, leakage of transformer, stray inductances and output capacitance of the secondary side rectifying devices. The rising time can be estimated by (49) where C_{oss} accounts for C_5 and C_8.





(i) [t_7] (i') [t_7] alternative

(h) [t_7, t_{10}]

Fig. 12. Operation modes for the proposed forward operation of PSFB in DCM.

5) Mode 5 [t7, t10] [Fig. 12(j)] - Deff

At some point after t_7 the output capacitances C_5 and C_8 are fully charged up to the nominal blocking voltage, and Q_6 and Q_7 conduct all the secondary side current in a new power transfer stage. Afterwards all the detailed sequence repeats but in the alternate polarity. On the primary side, like in mode 1, the difference between currents through L_r and the transformer flows through one of the clamping diodes: D_9.

B. INFLUENCE OF TIMING

Fig. 13 shows the effect of turning-on the SRs too early while operating the converter in DCM: before the transformer voltage starts building up. The current through Lo grows negative (flowing against the rectifiers) prior to the start of a power transfer. Once the power transfer starts, the additional stored energy induces an overshoot potentially higher than the original scenario in Fig. 8, as more energy could have been unintentionally stored in L_o.

A late activation of the SR devices does not help either in the reduction of the maximum peak voltage of the drain overshoot. Fig. 13 also shows the effect of turning-on short after that the transformer secondary reflected voltage has built up while the output filter works in DCM. The low frequency oscillation is clamped, but only after the prior high drain voltage overshoot.

The turn-on instant for the SR ($t_{sr,on}$) can be referenced to the turn-off instant of the primary side lagging leg ($t_{lagg,off}$) (50). The start of the voltage build up (T_{rise}) is delayed by the time it takes iL_r to reverse polarity, which can be calculated by (51)-(54). After this delay $T_{dly,on}$ the SR turn-on instant should happen within the T_{rise} interval for an effective clamping of the DCM overshoot (Fig. 14). The minimum turn-on time $t_{sr,on,min}$ and the maximum turn-on time $t_{sr,on,max}$ for an effective reduction of the overshoot can be derived from the previous equations and calculated by (55)-(56).

$$\left(t_{lagg,off} + T_{dly,on}\right) < t_{sr,on} < \left(t_{lagg,off} + T_{dly,on} + T_{rise}\right) \tag{50}$$

$$T_{dly,on} = \frac{\left(iL_r(t_{lagg,off}) - iL_m(t_{lagg,off})\right)(L_r + L_{lkg})}{V_{in}} \tag{51}$$

$$iL_r\left(t_{lagg,off}\right) \approx \frac{iL_{o,pk}}{n} + iL_{m,pk} \tag{52}$$

$$iL_m\left(t_{lagg,off}\right) = iL_{m,pk} = \frac{V_{in}}{L_m}\frac{iL_{o,pk}L_o}{(V_{in} - V_o)} \tag{53}$$

$$iL_{o,pk} = \sqrt{\frac{iL_{o,avg}V_o(V_{in} - V_o)}{F_{sw}V_{in}L_o}} \tag{54}$$

$$t_{sr,on,min} = t_{lagg,off} + \sqrt{\frac{iL_{o,avg}V_o(V_{in} - V_o)}{F_{sw}V_{in}L_o}}\frac{(L_r + L_{lkg})}{V_{in}n} \tag{55}$$

$$t_{sr,on,max} = t_{lagg,off} + \sqrt{\frac{iL_{o,avg}V_o(V_{in} - V_o)}{F_{sw}V_{in}L_o}}\frac{(L_r + L_{lkg})}{V_{in}n} + \pi\sqrt{\left(L_r + L_{lkg}\right)2C_{oss}} \tag{56}$$

Fig. 15 shows a proposal for the implementation of $T_{sr,on}$ in a controller. The voltages and currents through the converter are measurements typically available. Although, depending on the application, they can be considered constant ($V_{in,nominal}$, $V_{o,nominal}$) or estimated out from other of the measurements ($iL_{o,avg} \approx |iT_{r,avg}|n$). The rest of parameters, including converter inductances and turns ratio can be programmed as constants. The impact on the proposed implementation of the tolerances in the values of the converter's inductances and capacitances can be estimated with (55)-(56).

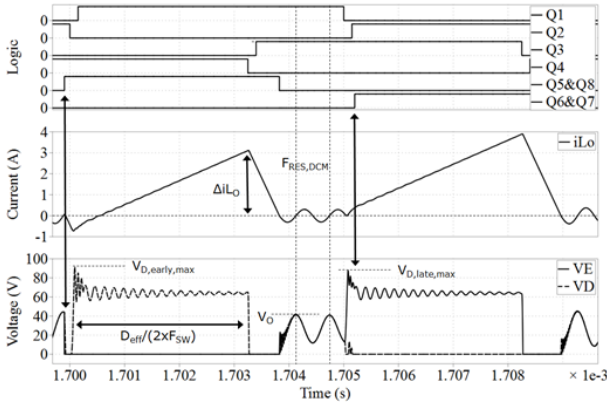


Fig. 13. Secondary side DCM overshoot with the proposed modulation scheme. SR has been turned-on too early for the pulse in the left side. SR has been turned-on too late for the pulse in the right side.

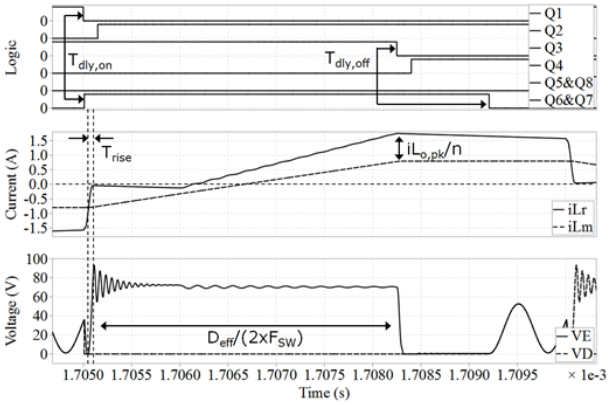


Fig. 14. Secondary side DCM overshoot with the proposed modulation scheme. SR has been turned-on right at the start of the rising time T_{rise}.

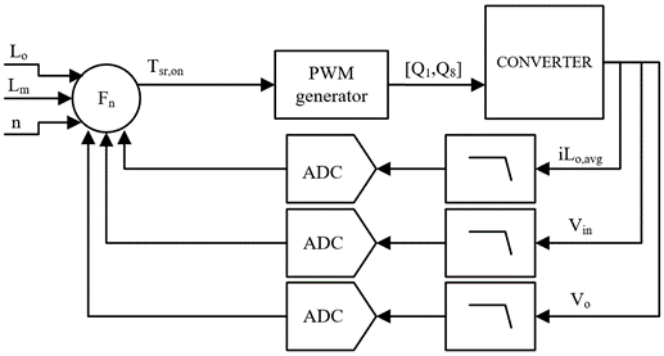


Fig. 15. Simplified control blocks for a possible implementations of $T_{sr,on}$ calculation in a PSFB controller.

V. EXPERIMENTAL RESULTS

A 3300 W PSFB DC/DC converter (Fig. 16) was designed with the specifications given in Table II and built to test the proposed solutions and guidelines presented in this work. Table III and Table IV summarize the main components of the converter. The control was implemented with XMC™ 4200 ARM® Cortex®-M4 microcontroller from Infineon Technologies AG.

Fig. 16 Prototype of the 3300 W PSFB converter.

The output filter inductor L_o was designed for an optimal overall efficiency of the converter at 50 % load point while fulfilling space constraints, high power density and maintaining the output voltage ripple within specifications. Fig. 17 shows a summary of the estimation of losses for the output inductor within the load range of the

converter. Table V is a summary of the estimation of losses for the main components of the converter. The distribution was estimated out of the measured efficiency of the real converter, thermographic captures, data from components manufacturer, finite element analysis (FEM), and circuit and numeric simulations.

TABLE II
KEY PARAMETERS OF PROTOTYPE

Parameter	Value
Nominal input voltage	400 V
Input voltage range	360 V - 410 V
Nominal output voltage	54.5 V
Output voltage range	43 V - 60 V
Maximum output power	3300 W
Maximum output current	85 A
Switching frequency	100 kHz
Height of the converter	1 U (44.4 mm)
Transformer turns ratio (Np : Ns)	21:4
Magnetizing inductance (Lm)	750 µH
Resonant inductance (Lr)	11 µH
Output choke inductance (Lo)	9.8 µH

TABLE III
SI MOSFETS AND DIODES

	IPL60R075CFD7	BSC093N15NS5	IDP08E65D1
V_{ds}	600 V	150 V	650 V
$R_{DS,on,max}$	75 mΩ @ 25 °C	9.3 mΩ @ 25 °C	
$C_{oss(er)}$	96 pF	604 pF	
V_f	1 V	0.88 V	1.35 V
Q_{rr}	570 nC	58 nC	200 nC
Q_g	67 nC	33 nC	
Count	8 devices	16 devices	2 devices

Observe in Fig. 17 that the current ripple through the output inductor changes with the load due to the influence of the DC bias on the permeability of the material. The transition between CCM and DCM occurs at the point where the two lines ΔiL_o and iL_o cross each other, around a load of 8 A. The DCM threshold is relatively high, about 13 % of the load, because of the small value of the output inductance. Nevertheless, the controller of the prototype was adjusted to change between operating modes at 12 A (18 %) of load to ensure safe operation in all conditions (e.g. load jumps) and avoid risk of forced CCM overshoot. Thereafter DCM overshoot is likely to occur and had to be prevented by the proposed modulation scheme.

TABLE IV
MAGNETIC CORE SELECTION

	Core	Material	Manufacturer	Turns
Transformer	PQI 35/28	DMR95	DMEGC	21:4
L_r	PQI 35/28	DMR95	DMEGC	6
L_o	Toroid	HP 60 µ	Chang Sung	9

TABLE V
3300 W PSFB LOSSES BREAKDOWN

Loss contribution	100% power	50% power	20% power
Auxiliary circuitry	1.02 W	1.02 W	1.02 W
Fan	4.91 W	0.64 W	0.64 W
Transformer	30.17 W	10.95 W	5.45 W
Lr	2.98 W	1.00 W	0.26 W
Lo	5.47 W	2.01 W	1.08 W
Primary bridge	19.65 W	5.91 W	2.77 W
Secondary switching	7.30 W	6.38 W	5.81 W
Secondary conduction	11.32 W	2.53 W	0.42 W
Secondary driving	0.84 W	0.84 W	0.84 W
Clamping diodes	1.89 W	2.32 W	2.52 W
Capacitors	0.41 W	0.37 W	0.36 W
PCB conduction	7.60 W	1.92 W	0.32 W

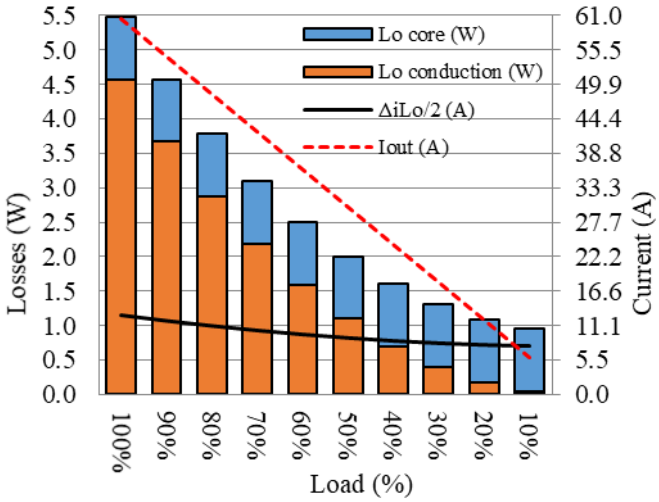


Fig. 17. Output inductor distribution of losses of the 3300 W PSFB prototype.

A. WAVEFORMS

1) Commutation overshoot

Since L_{lkg} and L_{stray} in the prototype are relatively small inductances, the commutation overshoot has high resonant frequency, low energy and dampens quickly. Fig. 18 shows a capture of the SR drain voltage overshoot at full load. Observe that the peak voltage is well below the rated limit for the 150 V of the secondary side devices in this design (limit would be 120 V at a standard 80 % rating). Devices with a maximum 120 V blocking voltage would be preferred on the secondary side since the improved Q_{oss} and Q_{rr} characteristics for the same $R_{ds,on}$ would further reduce commutation overshoot and losses [16] and would be still within their rated limits (96 V at a 80% rating). However, at the time of this work there were no available devices within that voltage class that could be used.

Besides, a weak snubber could be added to further reduce the peak voltage and/or improve the dampening of the commutation resonance without much of an impact on the losses.

2) DCM overshoot

In Fig. 19, during a load jump, the output filter of the converter goes into DCM during a few switching cycles whereas the controller did not apply the proposed DCM modulation scheme. It is worth to mention the difference between the drain voltage overshoot of the first three pulses compared to the last one: of lower frequency and higher energy, as caused by the resonance between Lo and the output capacitance of the SRs with L_o much larger than the leakage inductance of the transformer or other stray inductances in the commutation path.

Fig. 20 shows a deeper level of DCM operation of the output filter at very light load condition (no load start-up). A full resonance period is followed by the worst possible DCM overshoot scenario where a power transfer starts at the peak of charge of the output capacitances. It can be observed how the precharged energy stacks on top of the transformer reflected voltage.

Fig. 21 shows a similar scenario to those in Fig. 19 and Fig. 20, but this time applying the proposed DCM modulation scheme. DCM resonance is visible before the transformer secondary side reflected voltage builds up, however, the drain voltage overshoot resembles that of Fig. 18 and it is much lower than the one in Fig. 19 and Fig. 20.These results confirm the analysis in section III.

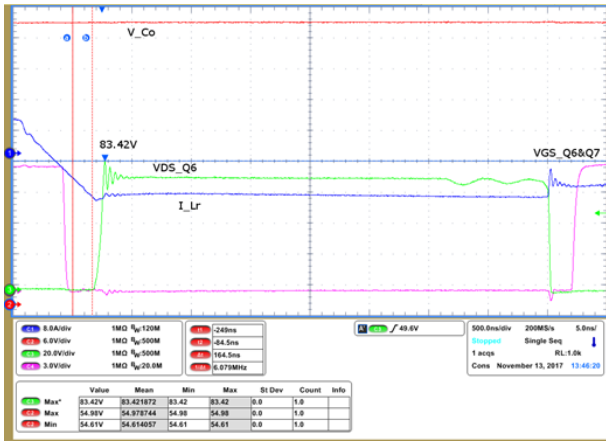


Fig. 18. SR overshoot at full load.

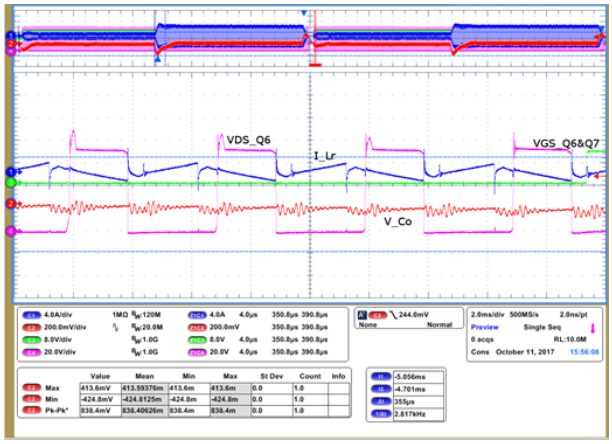


Fig. 19. SR DCM overshoot in a load jump without the proposed modulation scheme.

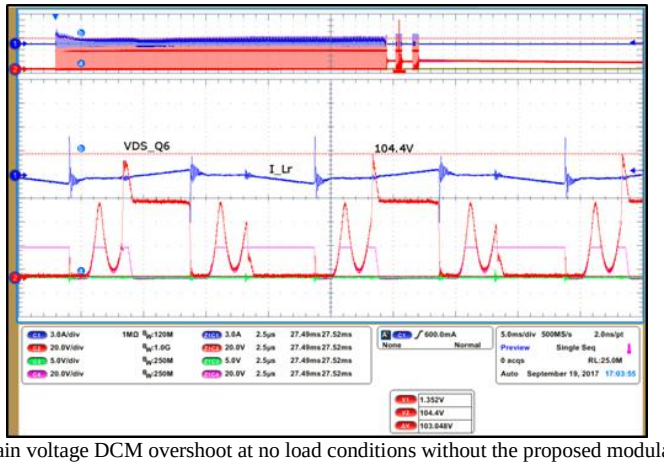


Fig. 20. SR drain voltage DCM overshoot at no load conditions without the proposed modulation scheme.

3) Influence of timing

Fig. 22 shows the effect of turning-on the SRs too early, before the transformer voltage starts building up, while operating the converter in DCM.

Fig. 23 shows the effect of turning-on short after that the transformer secondary reflected voltage has built up, while the output filter works in DCM. The low frequency oscillation is clamped, but only after the prior high drain voltage overshoot.

The results in Fig. 22 and Fig. 23 corroborate the analysis in section IV. B. The estimated T_{rise} for the prototype is approximately 740 ns, which can also be observed in Fig. 22.

Table VI is a summary of the experimental results in this section. Whereas the 150 V class falls within the 80 % rating criteria in all the cases, the 120 V class is only enabled by the proposed novel DCM modulation scheme.

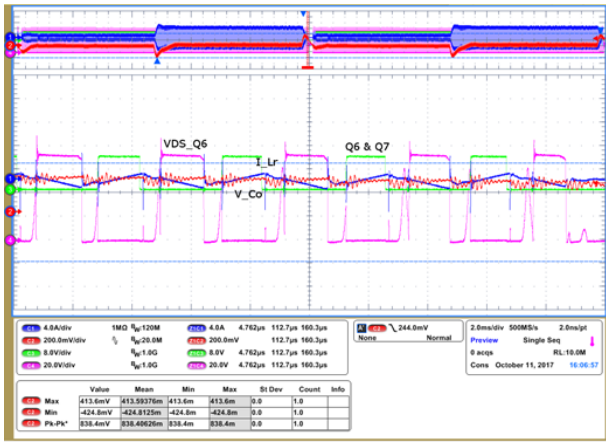


Fig. 21. SR drain voltage DCM overshoot in a load jump with the proposed modulation scheme.

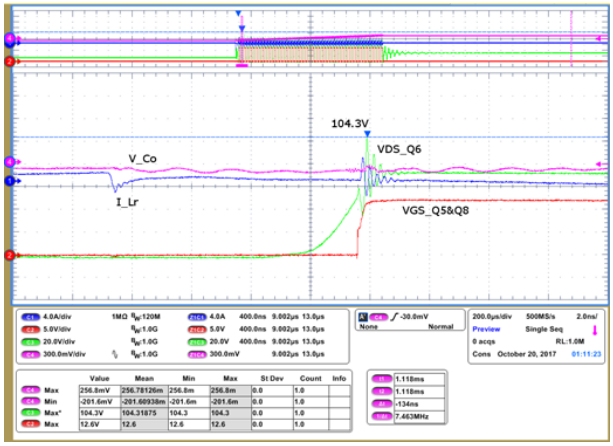


Fig. 22. SR drain voltage DCM overshoot when the devices turn-on too early.

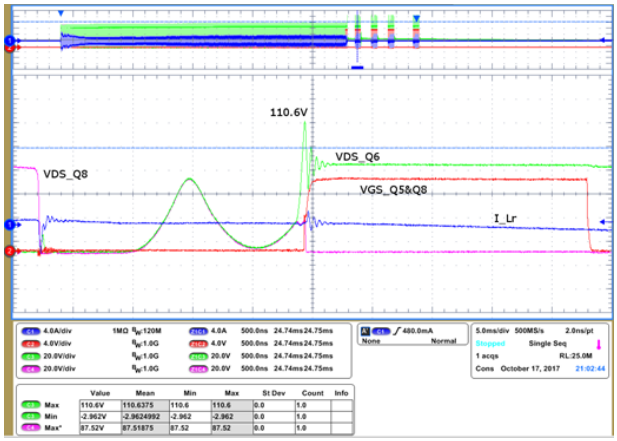


Fig. 23. SR drain voltage DCM overshoot when the device is activated too late.

TABLE VI
OVERSHOOT COMPARISON SUMMARY

	Overshoot	% of 150 V	% of 120 V
CCM	83.42 V	55.61 %	69.52 %
DCM State of Art	104.4 V	69.6 %	87 %
DCM Proposed Late	110.6 V	73.73 %	92.16 %
DCM Proposed Early	104.3 V	69.53 %	89.92 %
DCM Proposed	90 V	60 %	75 %

B. EFFICIENCY

The efficiency of the 3300 W PSFB prototype was measured at nominal input and output voltages along all the load range and plotted in Fig. 24. The experimental results are plotted together with simulated efficiencies for the 150 V devices and the 100 V devices of similar $R_{ds,on}$. The improved FoM of the 100 V technology has a noticeable impact along all the load range of the converter.

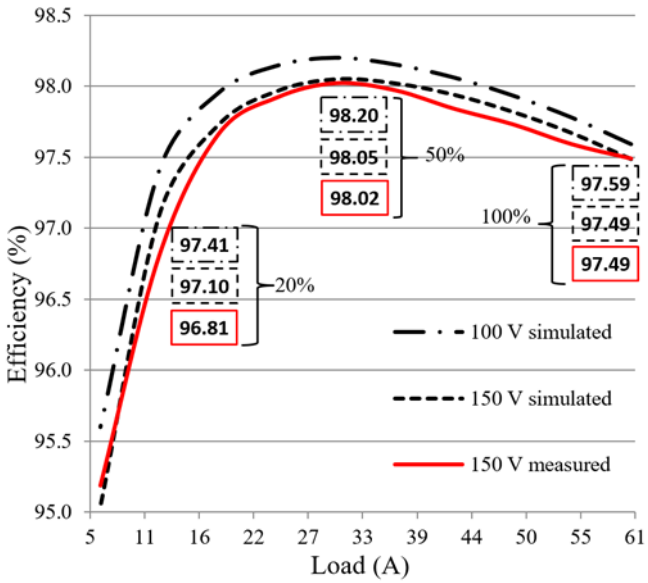


Fig. 24. Overall efficiency of the 3300 W PSFB converter. Auxiliary bias and fan were included in the measurements. Experimental and simulated results for the 150 V devices. Simulated results for the 100 V devices.

VI. CONCLUSION

One of the main disadvantages of the PSFB topology in comparison to other resonant topologies is the higher blocking voltage required for the SRs. This is especially detrimental in wide range operation converters and further aggravated by the SRs drain voltage overshoot. Unlike other resonant topologies, the inductor at the output of the PSFB effectively decouples the capacitor bank from the rectification stage, which otherwise becomes a strong lossless snubber.

Traditionally the main criterion for the selection of the external resonant inductance has been the available energy for the ZVS of the HV primary side devices and the loss of duty cycle at full load. However, the analysis

in this work demonstrates that, from the point of view of the overall performance of the system, the impact on the secondary side drain voltage overshoot and the reduction of the secondary side switching losses has to be taken into account for the dimensioning of the transformer's turns ratio *n* and the external inductance L_r.

In this work the main causes for the secondary side rectifiers drain voltage overshoot in PWM converters, specifically in PSFB converters, have been analyzed. Design guidelines and solutions for each of the scenarios, including a novel modulation scheme for the operation of PSFB with the output filter operating in DCM have been proposed. The proposed solution is based on an active rectification scheme switching on the devices prior or during the buildup time of the transformer secondary reflected voltage.

The proposed strategies enable the design of DCDC PSFB converters targeting high efficiency without penalties in reliability, complexity or cost. Lower blocking voltage requirements for the rectification devices improve their Figure of Merit, potentially reducing their related losses and increasing the overall efficiency of the converter.

A high efficiency DCDC PSFB converter prototype of 3300 W was designed and built to demonstrate the feasibility of the proposed solutions. The drain voltage overshoot has been proven to remain well within standard rated limits in all working conditions of the converter. The prototype achieved a peak efficiency of 98.12 % at nominal input and output voltages and 50 % of load. Overall, this work demonstrates that the PSFB can be a competitive alternative when building highly efficient and cost-competitive DC/DC converters.

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CHAPTER 9. THIRD PUBLICATION

A Practical Approach to the Design of a High Efficient PSFB DC-DC Converter for Server Applications

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***Abstract*— The Phase Shift Full Bridge (PSFB) is a widely known isolated DCDC converter topology commonly used in medium to high power applications, and one of the best candidates for the front-end DCDC converter in server power supplies. Since the server power supplies consume an enormous amount of power, the most critical issue is to achieve high efficiency. Several organizations promoting electrical energy efficiency, like the 80PLUS, keep introducing higher efficiency certifications with growing requirements extending also to light loads. The design of a high efficiency PSFB converter is a complex problem with many degrees of freedom which requires of a sufficiently accurate modeling of the losses and of efficient design criteria. In this work a losses model of the converter is proposed as well as design guidelines for the efficiency optimization of PSFB converter. The model and the criteria are tested with the redesign of an existing reference PSFB converter of 1400 W for server applications, with wide input voltage range, nominal 400 V input and 12 V output; achieving 95.85 % of efficiency at 50 % of load. A new optimized prototype of PSFB was built with the same specifications, achieving a peak efficiency of 96.68 % at 50 % of load.**

***Index Terms*— Phase Shift Full Bridge, Server, DCDC, Design, High-Efficiency.**

I. INTRODUCTION

As the number of devices connected to the internet and the available services increase, the volume of data transferred and processed by server systems is growing exponentially. The amount of data centers is rising consequently. Therefore, the server power systems are under continuous development. Since the server power supplies consume massive amounts of power, the most critical matter is to achieve high efficiency [1]. To promote electrical energy efficiency of server systems several organizations have setup initiatives like Climate-Savers-Computing-Initiative (CSCI) [2] and 80PLUS [3] which certifies individual power supplies corresponding to their performance level. CSCI and 80PLUS keep introducing higher efficiency certifications such as Gold, Platinum, and Titanium with growing requirements extending also to light loads (Table 1). Noticeably, the required efficiency at 50% load condition for each certification is the highest and the most difficult to achieve, based on the redundant configuration of server power system. The redundant structure is widely used in the server power supply applications because of the very high reliability demands characteristics of the application. A redundant structure means parallel power supplies sharing the total load and capable of taking over in case of a fault in one of the supplies [4]-[5]. Moreover, low power consumption of the server system in idle/sleep is becoming increasingly important. This is confirmed by efficiency requirements extending down to 10% load in 80PLUS Titanium [6]. Meanwhile the power rating of the Power Supply Unit (PSU) tends to increase to maximize the performance of

the server system. A smaller volume requirement allows a greater processing power at a lower cost in the building infrastructure [7]. This leads to very high power density server PSU because the server system is required to reduce its mechanical size [6].

A server PSU is primarily composed of two stages: a back-end Power Factor Correction (PFC) ACDC stage powered by universal AC input (90~265 VAC *rms*) followed by a front-end DCDC isolated step-down converter [8]. Among these parts, the front-end DCDC converter stage has the biggest impact on the efficiency of the server power system because of its high conversion ratio of voltages and currents, and the required isolation transformer, which results in large power losses [1]. The output voltage typically ranges between 12 VDC to 48 VDC. In the literature many different topologies have been proposed for this application. The DCDC stage can be a single switch isolated converter like a fly-back for low power applications (under 250 W), and half bridge converter or full bridge converter for higher power applications [8]-[9].

Half bridge LLC resonant converter is a popular isolated DCDC topology. This is mostly due to its high efficiency and simple circuit structure, which helps to achieve high power density. However, the switching frequency (F_{sw}) span of the LLC is very wide, especially when a wide gain range of operation is required [10]-[11]. DCDC converters with wide gain range capability are common in many power conversion applications. Server power supplies have demanding requirements on continuity and reliability which includes hold-up time operation. During hold-up time the AC input of the back-end ACDC converter is lost, while the DCDC should maintain a stable output. During this time the intermediate storage capacitor continues to provide the energy while the DC bus voltage drops considerably. Therefore, the DCDC converter needs to work normally with a wide input voltage range [10].

The other most common alternative for high efficiency and high power density DCDC converters in server PSU is the PSFB with synchronous rectifier (SR) MOSFETs, external resonant inductor and clamping diodes, shown in Figure 1. Its most remarkable characteristic is the wide zero-voltage-switching (ZVS) range from mid to full load [6], nearly suppressing switching losses, which are especially high for HV devices in hard-switched converters [12]. Moreover, the constant switching frequency allows a simple control and EMI design [9], [13]. One of the major advantages of PSFB over other resonant soft-switching topologies is the comparatively lower *rms* currents through the converter thanks to the output filter inductance. However, hold-up time regulation requirements makes PSFB converter not to be operated with its maximum effective duty in nominal conditions and causes a long freewheeling period [14]. The freewheeling period increases circulating currents and conduction losses [1].

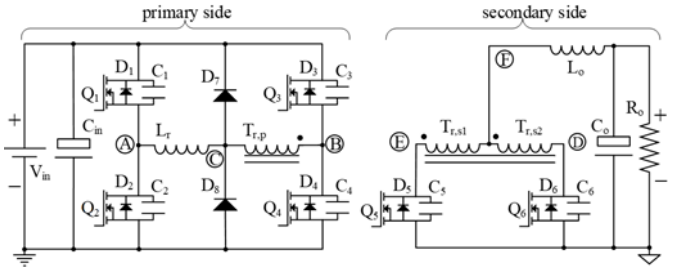


Figure 1. PSFB converter with center tapped rectification stage, external resonant inductance and clamping diodes.

TABLE I
SUMMARY OF EFFICIENCY REQUIREMENTS OF 80 PLUS CERTIFICATION FOR REDUNDANT POWER SUPPLIES

80 PLUS Certification	**230 V Internal Redundant (Complete PSU)**			
% of Rated Load	**10 %**	**20 %**	**50 %**	**100 %**
80 PLUS Bronze	-	81 %	85 %	81 %
80 PLUS Silver	-	85 %	89 %	85 %
80 PLUS Gold	-	88 %	92 %	88 %
80 PLUS Platinum	-	90 %	94 %	91 %
80 PLUS Titanium	90 %	94 %	96 %	91 %

The design of the DCDC converter has many degrees of freedom which complicates the selection of the components values resulting in the best solution. Finding the design solution with the highest power density and/or efficiency and/or cost requires an optimization procedure based on comprehensive analytical models and equations considering the losses in the converter components [9], [15]. With this procedure, the optimal design parameters could be determined. In [13] a design process is presented to reach the point of highest efficiency η_{max} and highest power density ρ_{max} for a 5kW PSFB DCDC converter. The design process is based on an automatic optimization procedure which finds the optimal component values of the converter system. The space of solutions is limited by a curve in the η-ρ-plane, so called Pareto front, which presents the optimal points for varying weights of the efficiency and of the power density [13]. However, the automated process obscures the nature of the design parameters influence on the converter behavior, the design parameter interdependencies and limits the design engineer understanding of the converter.

In this work we present a complete losses model of the PSFB, which should prove useful for practicing engineers in their understanding on the origin of losses in the converter. The provided set of equations is based on a

simplified model of the PSFB: all capacitances are linear; it does not include the clamping diodes; and it does not include the secondary side rectifiers' capacitance. Furthermore, possible improvements in the losses calculation will be discussed. Those and other additional considerations have been included by the authors in an extended set of equations, excluded from this document for clarity. The design criteria for a semi-automated design process presented in a following section has been performed on the authors extended version of the model. The losses model is tested and the design criteria is demonstrated with the design of a PSFB DCDC 1.4kW 12 V output converter for server applications. The optimized PSFB design is compared to a reference converter with the same specifications. The rest of this paper is organized as follows. In Section II we propose a comprehensive losses model for the PSFB converter. The model is later used in section III to analyze the influence of several of the design parameters in the converter performance. Section III also includes design guidelines or criteria for a semi-automated design procedure. In IV the losses model and the design criteria have been applied to optimize a 1.4kW PSFB DCDC converter with 12 V output for server applications. Section V presents a summary of result comparing a previous reference design of PSFB with the new optimized prototype. Finally Section VI presents a summary of conclusions out of this work.

II. LOSSES MODEL

A sufficiently detailed and accurate losses analysis model is necessary in order to perform efficiency optimization. The losses model and the design procedure should be a trade-off between accuracy and usability. Excessively precise and accurate estimations may lead to heavy computation requirements and long calculation times which makes the design process, iterative by nature, slow and tedious. Moreover, the complexity of the problem and the difficulty of estimating the real values of parameters in the circuit makes a precise estimation impractical. Ideally, the losses model is later on updated or corrected based on the results of the real hardware, giving more accurate results each design iteration. The power losses analysis is discussed in this section to help understanding where the losses are originated. There are three types of power losses for a switching power converter, as follows [15]: conduction losses; switching losses (including gate-driving power losses), magnetic core losses.

The PSFB converter's operation can be classified into Discontinuous Conduction Mode (DCM), if the output filter inductor current ripple is higher than the average output; and Continuous Conduction Mode (CCM) otherwise. The circuit analysis in CCM is quite different from that in DCM because of the different operation modes [15]. In this work we will consider only the CCM working mode (the proposed losses model does not include DCM operation). The high-efficiency designs operate in CCM in all load range of interest. Moreover, the DCM control of the SRs could be challenging. Therefore, the PSFB converter is normally preferred not operate in DCM [16].

A. CONDUCTION LOSSES

These losses are caused by the currents passing through the parasitic resistances in the circuit, such as the on resistance of the switches $R_{ds,on}$, the transformer and inductor winding resistance. These losses can be calculated with the equivalent resistance and the *rms* current value in the different components of the converter [15].

1) TRANSFORMER CONDUCTION LOSSES

The principles of operation of the PSFB converter have been already widely covered in the literature [17]. Briefly, the PSFB converter has three main working modes, which can be identified in Figure 2:

- Effective duty (D_{eff}). In this mode the primary side bulk voltage (V_{in}) is applied to the resonant inductance L_r and the primary side of the transformer. Power is being transferred from primary to secondary through the transformer (overlap of current and voltage of same sign).
- Duty losses (D_{loss}). Before the next power transfer the current has to reverse polarity on the primary side of the transformer. The current through the resonant inductance (L_r) and leakage of the transformer (L_{lkg}) require of certain time to reach the reflected output current with reverse sign.
- Freewheeling duty (D_{frew}). During the remaining time the current recirculates on the primary side without effective power transfer (there is no overlap of current and voltage on the primary side of transformer) while it freewheels on the secondary side.

Figure 2 shows a simplified representation of the primary side current in a PSFB converter: all capacitances are linear; it does not include the clamping diodes; and it does not include the secondary side rectifiers' capacitance. The enclosed area between iT_r and iL_m corresponds to the reflected secondary current during D_{eff}, while power is being transferred from the primary to the secondary. The enclosed shaded areas correspond to currents recirculating on the primary side without effective power being delivered to the secondary side. From Figure 2 it can be inferred that two parameters have the most impact on the circulating currents: the effective duty (D_{eff}) and the magnetizing current (iL_m).

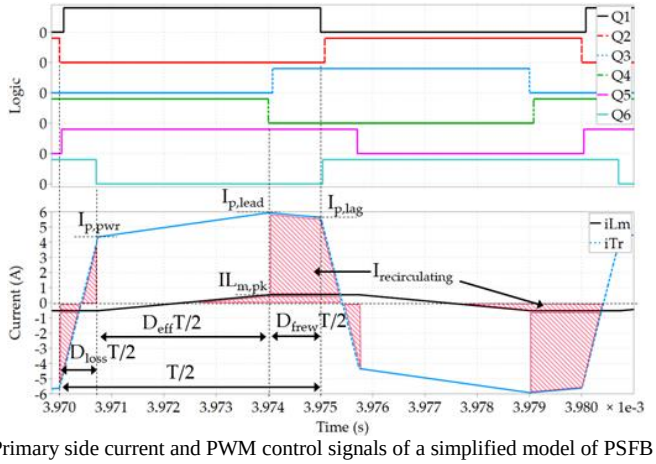


Figure 2. Primary side current and PWM control signals of a simplified model of PSFB converter.

The current passing through the primary side of the transformer, excluding the effect of the magnetizing inductance, can be calculated with the equations (1)-(4). The secondary side reflected current could be calculated from (1)-(4) multiplying by the turns ratio of transformer *n*.

$$\begin{cases} \mathrm{iT_r} = \frac{\mathrm{V_{in}}}{\mathrm{L_r+L_{lkg}}}\mathrm{t} - \mathrm{IT_{r,lag}}\ ,\ \mathrm{t} \in \left[0, \mathrm{D_{loss}}\frac{\mathrm{T}}{2}\right] \\ \mathrm{iT_r} = \frac{(\mathrm{V_{in}}-\mathrm{V_o}n)}{\mathrm{L_r+L_{lkg}+L_o}n^2}\left(\mathrm{t} - \mathrm{D_{loss}}\frac{\mathrm{T}}{2}\right) + \mathrm{IT_{r,pwr}}\ ,\ \mathrm{t} \in \left[\mathrm{D_{loss}}\frac{\mathrm{T}}{2}, (\mathrm{D_{eff}}+\mathrm{D_{loss}})\frac{\mathrm{T}}{2}\right] \\ \mathrm{iT_r} = \frac{-\mathrm{V_o}n}{\mathrm{L_r+L_{lkg}+L_o}n^2}\left(\mathrm{t} - (\mathrm{D_{eff}}+\mathrm{D_{loss}})\frac{\mathrm{T}}{2}\right) + \mathrm{IT_{r,lead}}\ ,\ \mathrm{t} \in \left[(\mathrm{D_{eff}}+\mathrm{D_{loss}})\frac{\mathrm{T}}{2}, \frac{\mathrm{T}}{2}\right] \end{cases} \quad (1)$$

$$n = \frac{\mathrm{N_p}}{\mathrm{N_s}} \quad (2)$$

$$\mathrm{IT_{r,pwr}} = n\left(\mathrm{IL_{o,avg}} - \frac{\Delta \mathrm{IL_o}}{2}\right) \quad (3)$$

$$\mathrm{IT_{r,lead}} = n\left(\mathrm{IL_{o,avg}} + \frac{\Delta \mathrm{IL_o}}{2}\right) \quad (4)$$

The magnetizing current is proportional to the input voltage and inversely proportional to the magnetizing inductance. It can be calculated with (5)-(6):

$$\begin{cases} \mathrm{iL_m} = -\mathrm{IL_{m,pk}}\ ,\ \mathrm{t} \in \left[0, \mathrm{D_{loss}}\frac{\mathrm{T}}{2}\right] \\ \mathrm{iL_m} = \frac{\mathrm{V_{in}}}{\mathrm{L_m+L_r+L_{lkg}}}\left(\mathrm{t} - \mathrm{D_{loss}}\frac{\mathrm{T}}{2}\right) - \mathrm{IL_{m,pk}}\ ,\ \mathrm{t} \in \left[\mathrm{D_{loss}}\frac{\mathrm{T}}{2}, (\mathrm{D_{eff}}+\mathrm{D_{loss}})\frac{\mathrm{T}}{2}\right] \\ \mathrm{iL_m} = \mathrm{IL_{m,pk}}\ ,\ \mathrm{t} \in \left[(\mathrm{D_{eff}}+\mathrm{D_{loss}})\frac{\mathrm{T}}{2}, \frac{\mathrm{T}}{2}\right] \end{cases} \quad (5)$$

$$\mathrm{iL_{m,pk}} = \mathrm{D_{eff}}\frac{\mathrm{V_{in}T}}{2(\mathrm{L_m+L_r+L_{lkg}})} \approx \mathrm{D_{eff}}\frac{\mathrm{V_{in}T}}{2\mathrm{L_m}} \quad (6)$$

Taking into account the magnetizing current the resulting primary side current can be calculated with (7)-(9):

$$\begin{cases} \mathrm{i_p} = \frac{\mathrm{V_{in}}}{\mathrm{L_r+L_{lkg}}}\mathrm{t} - \mathrm{I_{p,lag}}\ ,\ \mathrm{t} \in \left[0, \mathrm{D_{loss}}\frac{\mathrm{T}}{2}\right] \\ \mathrm{i_p} = \mathrm{i_{Tr}} + \mathrm{i_m} + \mathrm{I_{p,pwr}}\ ,\ \mathrm{t} \in \left[\mathrm{D_{loss}}\frac{\mathrm{T}}{2}, (\mathrm{D_{eff}}+\mathrm{D_{loss}})\frac{\mathrm{T}}{2}\right] \\ \mathrm{i_p} = \mathrm{i_{Tr}} + \mathrm{i_m} + \mathrm{I_{p,lead}}\ ,\ \mathrm{t} \in \left[(\mathrm{D_{eff}}+\mathrm{D_{loss}})\frac{\mathrm{T}}{2}, \frac{\mathrm{T}}{2}\right] \end{cases} \quad (7)$$

$$\mathrm{I_{p,pwr}} = \mathrm{IT_{r,pwr}} - \mathrm{IL_{m,pk}} \quad (8)$$

$$\mathrm{I_{p,lead}} = \mathrm{IT_{r,lead}} + \mathrm{IL_{m,pk}} \quad (9)$$

The *rms* current of the primary side of transformer and secondary side of transformer can be calculated from the previous equations which result in (10)-(12):

$$\mathrm{I_{p,rms}}^2 = \frac{2}{\mathrm{T}}\left[\int_0^{\mathrm{D_{loss}}\frac{\mathrm{T}}{2}} \mathrm{i_p}^2\,\mathrm{dt} + \int_{\mathrm{D_{loss}}\frac{\mathrm{T}}{2}}^{(\mathrm{D_{eff}}+\mathrm{D_{loss}})\frac{\mathrm{T}}{2}} \mathrm{i_p}^2\,\mathrm{dt} + \int_{(\mathrm{D_{eff}}+\mathrm{D_{loss}})\frac{\mathrm{T}}{2}}^{\frac{\mathrm{T}}{2}} \mathrm{i_p}^2\,\mathrm{dt}\right] \quad (10)$$

$$\mathrm{I_{p,rms}}^2 = \frac{1}{3}\left(\begin{array}{c}\left(\mathrm{I_{p,pwr}}^2 + \mathrm{I_{p,lead}}^2 + \mathrm{I_{p,pwr}I_{p,lead}}\right)\mathrm{D_{eff}} + \left(\mathrm{I_{p,lag}}^2 + \mathrm{I_{p,lead}}^2 + \mathrm{I_{p,lag}I_{p,lead}}\right)\mathrm{D_{frew}} + \\ \left(\mathrm{I_{p,lag}}^2 + \mathrm{I_{p,pwr}}^2 + \mathrm{I_{p,pwr}I_{p,lag}}\right)\mathrm{D_{loss}}\end{array}\right) \quad (11)$$

$$I_{s,rms}{}^2 = \frac{n^2}{3}\left(\begin{array}{c}\left(IT_{r,pwr}{}^2 + IT_{r,lead}{}^2 + IT_{r,pwr}IT_{r,lead}\right)D_{eff} + \left(IT_{r,lag}{}^2 + IT_{r,lead}{}^2 + IT_{r,lag}IT_{r,lead}\right)D_{frew} + \\ \left(IT_{r,lag}{}^2 + IT_{r,pwr}{}^2 + IT_{r,pwr}IT_{r,lag}\right)D_{loss}\end{array}\right) \quad (12)$$

The conduction losses of the transformer can be estimated with the *rms* currents and equation (13), where $R_{Tr,p}$ stands for the primary side equivalent resistance of the transformer, $L_{r,ESR}$ the equivalent resistance of the resonant inductance and $R_{Tr,s}$ the equivalent resistance of the secondary side of the transformer. Additionally the contribution to conduction losses of the Printed Circuit Board (PCB) could be added both in the primary and in the secondary of the converter, which have a noticeable impact in high output current converters.

$$P_{cond,Tr} = I_{p,rms}{}^2(R_{Tr,p} + L_{r,ESR}) + I_{s,rms}{}^2 R_{Tr,s} \quad (13)$$

The skin and proximity effects increase the equivalent resistance of the windings and should be included for an accurate estimation of the transformer conduction losses. The magnetic fields generated by the alternating currents through the windings reduces the effective conduction area of the conductor itself (skin) and of other surrounding conductors (proximity). The studies in [18] show that the proximity effect dominates at high frequencies.

In the extended authors' model, the AC resistance R_{AC} of the primary and secondary windings of the transformer was estimated at different frequencies with Finite Element Analysis (FEA) software [19]. The spectrum of the transformer's primary and secondary currents was calculated from the previously analyzed waveforms. The total conduction losses was approximated by the sum of the *rms* current for each of the frequency components multiplied by the R_{AC} at that frequency.

2) PRIMARY SIDE HV MOSFETS

As suggested in [20] the power losses of the leading and lagging legs, which is dependent on MOSFETs current and voltage waveforms, should be analyzed separately. Therefore, the key waveforms for the MOSFETs in both of the primary side full bridge legs are shown in Figure 3 and will be described analytically. The proposed loss model is precise enough and easily computable using datasheet parameters.

The current waveform for the lagging leg (Q_1, Q_2 in Figure 1) can be calculated with the equations (14):

$$\begin{cases} i_{Q1} = \frac{V_{in}}{L_r+L_{lkg}}t - I_{p,lag}\ ,\ t \in \left[0, D_{loss}\frac{T}{2}\right] \\ i_{Q1} = \frac{(V_{in}-V_o n)}{L_r+L_{lkg}+L_o n^2}\left(t - D_{loss}\frac{T}{2}\right) + I_{p,pwr}\ ,\ t \in \left[D_{loss}\frac{T}{2}, (D_{eff}+D_{loss})\frac{T}{2}\right] \\ i_{Q1} = 0\ ,\ t \in \left[(D_{eff}+D_{loss})\frac{T}{2}, T\right] \end{cases} \quad (14)$$

The current waveform for the leading leg (Q_3, Q_4 in Figure 1) with the equations (15):

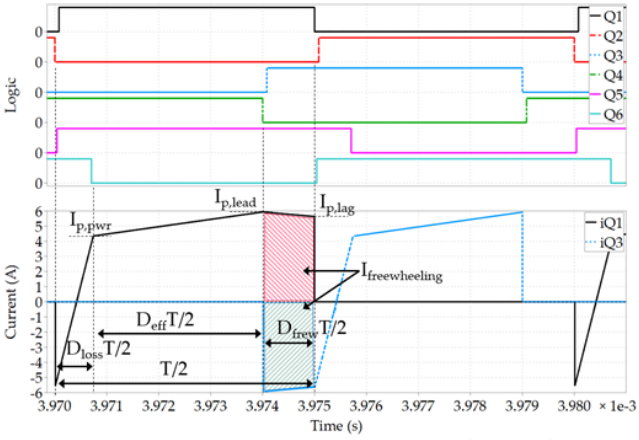


Figure 3. Primary side HV MOSFETs current and PWM control signals of a simplified model of PSFB converter.

$$\begin{cases} i_{Q3} = \frac{V_o n}{L_r+L_{lkg}+L_o n^2}\left(t - (D_{eff}+D_{loss})\frac{T}{2}\right) - I_{p,lead}\ ,\ t \in \left[(D_{eff}+D_{loss})\frac{T}{2}, \frac{T}{2}\right] \\ i_{Q3} = \frac{V_{in}}{L_r+L_{lkg}}\left(t - \frac{T}{2}\right) - I_{p,lag}\ ,\ t \in \left[\frac{T}{2}, \frac{T}{2}(1+D_{loss})\right] \\ i_{Q3} = \frac{(V_{in}-V_o n)}{L_r+L_{lkg}+L_o n^2}\left(t - (1+D_{loss})\frac{T}{2}\right) + I_{p,pwr}\ ,\ t \in \left[\frac{T}{2}(1+D_{loss}), \frac{T}{2}(1+D_{loss}+D_{eff})\right] \end{cases} \quad (15)$$

The *rms* currents of the both legs result to be equal in this simplified model, calculated from the previous formulas and resulting in the equation (16):

$$I_{Q1-4,rms}{}^2 = \frac{1}{6}\left(\begin{array}{c}(I_{p,pwr}{}^2 + I_{p,lead}{}^2 + I_{p,pwr}I_{p,lead})D_{eff} + (I_{p,lag}{}^2 + I_{p,lead}{}^2 + I_{p,lag}I_{p,lead})D_{frew} + \\ (I_{p,lag}{}^2 + I_{p,pwr}{}^2 + I_{p,pwr}I_{p,lag})D_{loss}\end{array}\right) = I_{Q3,rms}{}^2 \quad (16)$$

The conduction losses of the HV switches can be estimated from their *rms* currents with the equation (17), where $R_{ds,on}$ stands for the equivalent resistance of the MOSFETs. Note that the $R_{ds,on}$ of MOSFETs increases with temperature and it is also influenced by the gate driving voltage. Most of the conduction losses, like in MOSFETs, increase with temperature. This should be taken into account in the computation of the equivalent resistance of the components.

$$P_{cond,HV} = 4I_{Q1-4,rms}{}^2 R_{DS(on),p} \quad (17)$$

In the authors' extended model, the equivalent resistance of MOSFETs is estimated at the operating junction temperature T_J from their temperature coefficient, available in the manufacturer's datasheet. Because of the conduction losses are consequently updated, the temperature is recalculated until the solution of the equations converge. The process is also performed for other of the converter components: transformer windings, transformer core, secondary side rectifiers, PCB and output inductor winding. The iterative calculation can be easily automated in a computer, e.g. in a calculation sheet.

The estimations of components temperature require of additional values for the thermal impedances, for example from junction to air for the HV and the LV MOSFETs. This was estimated with thermal simulation tools and thermal captures of the real hardware.

Additionally, the conduction losses of the HV MOSFETs body diode could be estimated accounting for the turn-on delay of the switches, so-called dead times. Not included here for simplicity, since for a reasonably well adjusted control of the dead times the body diode contribution is minor in Silicon devices. Moreover, because of the strong non-linearity of the output capacitance in modern super-junction MOSFETs, the equivalent C_{oss} in the depletion region is big, which enables relatively high tolerance for the turn-on delay prior to the body diode conducts.

3) SECONDARY SIDE RECTIFIER LV MOSFETS

The Schottky Barrier Diode (SBD) or Fast Recovery Diode (FRD) are commonly used as secondary side rectification devices in PSFB DCDC converters because of its low cost and the simplified control of the converter. However, the forward voltage drop of diodes cause relative high conduction losses. By replacing diode with an active switching element, so called synchronous rectifier (SR), the losses can be notably reduced [21].

The rectification stage may have different configurations: center tapped, current doubler or full bridge [17]. Although these alternatives have no major impact on the working principles of the converter they do have a significant impact on the current and voltage stress over the rectification devices and their related conduction and switching losses. The blocking voltage of the secondary side devices is two times the transformer reflected secondary voltage for center tapped and current doubler, or one time the transformer reflected secondary voltage for full bridge. However the effective $R_{ds,on}$ is twice as big for full bridge rectification [22]. Therefore current doubler and center tapped rectifiers are the most appropriate for low voltage and high current applications. In [23] both configurations are analyzed and compared. The center tapped rectifier presents only one output inductor, which operates at double the switching frequency of the semiconductors, becoming an interesting alternative at low and medium current applications.

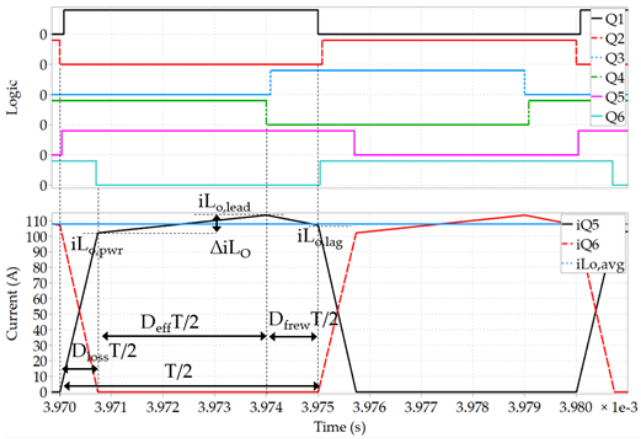


Figure 4. Secondary side LV MOSFETs current and PWM control signals of a simplified model of PSFB converter.

The current of the SRs (Q_5, Q_6 in Figure 1) is plotted in Figure 4 and can be calculated with the equations (18)-(21):

$$\begin{cases} i_{Q5} = \frac{IL_{o,pwr}}{D_{loss}\frac{T}{2}}t \ , \ t \in \left[0, D_{loss}\frac{T}{2}\right] \\ i_{Q5} = \frac{\left(\frac{V_{in}}{n}-V_o\right)}{\frac{L_r+L_{lkg}}{n^2}+L_o}\left(t - D_{loss}\frac{T}{2}\right) + IL_{o,pwr} \ , \ t \in \left[D_{loss}\frac{T}{2}, (D_{eff}+D_{loss})\frac{T}{2}\right] \\ i_{Q5} = \frac{-V_o}{L_r+L_{lkg}+L_o n^2}\left(t - (D_{eff}+D_{loss})\frac{T}{2}\right) + IL_{o,lead} \ , \ t \in \left[(D_{eff}+D_{loss})\frac{T}{2}, \frac{T}{2}\right] \end{cases} \quad (18)$$

$$IL_{o,pwr} = n\left(IL_{o,avg} - \frac{\Delta IL_o}{2}\right) \quad (19)$$

$$\Delta IL_o = \frac{T}{2}\frac{\left(\frac{V_{in}}{n}-V_o\right)D_{eff}}{\frac{L_r+L_{lkg}}{n^2}+L_o} \quad (20)$$

$$IL_{o,lead} = n\left(IL_{o,avg} + \frac{\Delta IL_o}{2}\right) \quad (21)$$

The *rms* currents of the both legs are equal in this ideal case and can be calculated from the previous formulas as expressed by (22):

$$I_{Q5-6,rms}{}^2 = \frac{1}{6}\begin{pmatrix} IL_{o,pwr}{}^2 D_{loss} + \left(IL_{o,pwr}{}^2 + IL_{o,lead}{}^2 + IL_{o,pwr}IL_{o,lead}\right)D_{eff} + \\ \left(IL_{o,pwr}{}^2 + IL_{o,lag}{}^2 + IL_{o,pwr}IL_{o,lag}\right)D_{frew} \end{pmatrix} = I_{Q6,rms}{}^2 \quad (22)$$

Out of the *rms* currents the conduction losses of the secondary side rectifiers can be estimated with (23) where $R_{ds,on,SR}$ stands for the equivalent resistance of the secondary side switches:

$$P_{cond,SR} = 2I_{Q5-6,rms}{}^2 R_{DS(on),SR} \quad (23)$$

Additionally the conduction losses of the body diode of the secondary side rectifiers could be estimated accounting for the unavoidable turn-on and turn-off delays of the switches. Not included here for simplicity, since for a good adjusted control of the SRs the body diode contribution is minor in Silicon devices.

4) INPUT AND OUTPUT FILTER

The output filter includes the output choke L_o and the output capacitance of the converter C_o. The input filter includes the bulk capacitance between the back-end ACDC converter and the front-end DCDC converter. In reality part of the current ripple through the input filter caused by the DCDC stage is cancelled by the output current ripple of the ACDC converter but, for simplicity, we will only consider the *rms* current of the DCDC as a standalone converter.

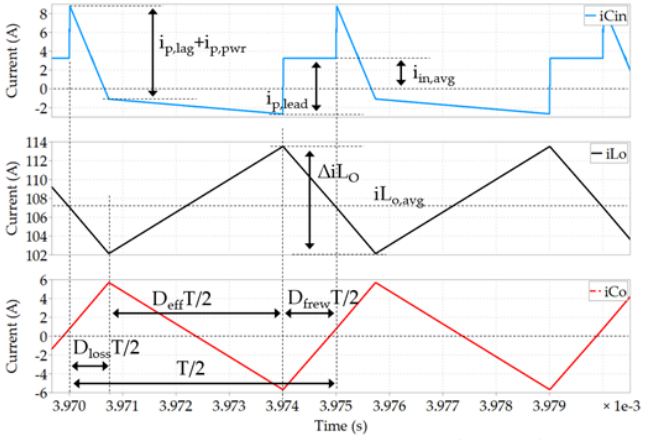


Figure 5. Input capacitor, output choke and output capacitor currents of a simplified model of PSFB converter.

The current of the output choke is plotted in Figure 5 and can be calculated with equations (24):

$$\begin{cases} iL_o = IL_{o,avg} - \frac{\Delta IL_o}{2} + \frac{\left(\frac{V_{in}}{n}-V_o\right)}{\frac{L_r+L_{lkg}}{n^2}+L_o}\left(t - D_{loss}\frac{T}{2}\right) \ , \ t \in \left[D_{loss}\frac{T}{2}, (D_{eff}+D_{loss})\frac{T}{2}\right] \\ iL_o = IL_{o,avg} + \frac{\Delta IL_o}{2} - \frac{V_o\left(t-(D_{eff}+D_{loss})\frac{T}{2}\right)}{\frac{L_r+L_{lkg}}{n^2}+L_o} \ , \ t \in \left[(D_{eff}+D_{loss})\frac{T}{2}, (1+D_{loss})\frac{T}{2}\right] \end{cases} \quad (24)$$

The *rms* current through the output choke can be estimated with (25):

$$\mathrm{IL_{o,rms}}^2 = \frac{1}{3}\left(\left(\mathrm{IL_{o,avg}} - \frac{\Delta \mathrm{IL_o}}{2}\right)^2 + \left(\mathrm{IL_{o,avg}} + \frac{\Delta \mathrm{IL_o}}{2}\right)^2 + \left(\mathrm{IL_{o,avg}} - \frac{\Delta \mathrm{IL_o}}{2}\right)\left(\mathrm{IL_{o,avg}} + \frac{\Delta \mathrm{IL_o}}{2}\right)\right) \tag{25}$$

The current of the output capacitor can be calculated with (26):

$$\begin{cases} \mathrm{iC_o} = \frac{\left(\frac{\mathrm{V_{in}}}{n} - \mathrm{V_o}\right)}{\frac{\mathrm{L_r}+\mathrm{L_{lkg}}}{n^2}+\mathrm{L_o}}\left(\mathrm{t} - \mathrm{D_{loss}}\frac{\mathrm{T}}{2}\right) - \frac{\Delta \mathrm{IL_o}}{2} \ , \ \mathrm{t} \in \left[\mathrm{D_{loss}}\frac{\mathrm{T}}{2}, (\mathrm{D_{eff}} + \mathrm{D_{loss}})\frac{\mathrm{T}}{2}\right] \\ \mathrm{iC_o} = \frac{\Delta \mathrm{IL_o}}{2} - \frac{\mathrm{V_o}\left(\mathrm{t} - (\mathrm{D_{eff}} + \mathrm{D_{loss}})\frac{\mathrm{T}}{2}\right)}{\frac{\mathrm{L_r}+\mathrm{L_{lkg}}}{n^2}+\mathrm{L_o}} \ , \ \mathrm{t} \in \left[(\mathrm{D_{eff}} + \mathrm{D_{loss}})\frac{\mathrm{T}}{2}, (1 + \mathrm{D_{loss}})\frac{\mathrm{T}}{2}\right] \end{cases} \tag{26}$$

The *rms* current through the output capacitor can be estimated with (27):

$$\mathrm{IC_{o,rms}}^2 = \frac{1}{3}\left(\frac{\Delta \mathrm{IL_o}}{2}\right)^2 \tag{27}$$

The current through the input capacitor can be calculated with the equations (28)-(29):

$$\begin{cases} \mathrm{iC_{in}} = \mathrm{I_{p,lag}} - \mathrm{I_{in,avg}} - \frac{\mathrm{V_{in}}}{\mathrm{L_r}+\mathrm{L_{lkg}}}\mathrm{t} \ , \ \mathrm{t} \in \left[0, \mathrm{D_{loss}}\frac{\mathrm{T}}{2}\right] \\ \mathrm{iC_{in}} = \mathrm{I_{p,pwr}} - \mathrm{I_{in,avg}} - \frac{(\mathrm{V_{in}} - \mathrm{V_o}\mathrm{n})}{\mathrm{L_r}+\mathrm{L_{lkg}}+\mathrm{L_o}n^2}\left(\mathrm{t} - \mathrm{D_{loss}}\frac{\mathrm{T}}{2}\right) \ , \ \mathrm{t} \in \left[\mathrm{D_{loss}}\frac{\mathrm{T}}{2}, (\mathrm{D_{eff}} + \mathrm{D_{loss}})\frac{\mathrm{T}}{2}\right] \\ \mathrm{iC_{in}} = -\mathrm{I_{in,avg}} \ , \ \mathrm{t} \in \left[(\mathrm{D_{eff}} + \mathrm{D_{loss}})\frac{\mathrm{T}}{2}, \frac{\mathrm{T}}{2}\right] \end{cases} \tag{28}$$

$$\mathrm{I_{in,avg}} = \left[\left(\frac{\mathrm{I_{p,lag}}+\mathrm{I_{p,pwr}}}{2} - \mathrm{I_{p,pwr}}\right)\mathrm{D_{loss}} + \left(\frac{\mathrm{I_{p,lead}}-\mathrm{I_{p,pwr}}}{2} - \mathrm{I_{p,lead}}\right)\mathrm{D_{eff}}\right] \tag{29}$$

The *rms* current through the input capacitor can be estimated with (30):

$$\mathrm{IC_{in,rms}}^2 = \frac{1}{3}\left[\begin{array}{l}\left(\left(\mathrm{I_{p,lag}} + \mathrm{I_{in,avg}}\right)^2 + \left(\mathrm{I_{in,avg}} - \mathrm{I_{p,pwr}}\right)^2 + \left(\mathrm{I_{p,lag}} + \mathrm{I_{in,avg}}\right)\left(\mathrm{I_{in,avg}} - \mathrm{I_{p,pwr}}\right)\right)\mathrm{D_{loss}} + \\ \left(\left(\mathrm{I_{in,avg}} - \mathrm{I_{p,lead}}\right)^2 + \left(\mathrm{I_{in,avg}} - \mathrm{I_{p,pwr}}\right)^2 + \left(\mathrm{I_{in,avg}} - \mathrm{I_{p,lead}}\right)\left(\mathrm{I_{in,avg}} - \mathrm{I_{p,pwr}}\right)\right)\mathrm{D_{eff}}\end{array}\right] + \mathrm{I_{in,avg}}^2\mathrm{D_{frew}} \tag{30}$$

The conduction losses of the input and output filter can be estimated with the *rms* currents and the equation (31) where $\mathrm{C_{in,ESR}}$ stands for the equivalent resistance of the input capacitor, $\mathrm{C_{o,ESR}}$ stands for the equivalent resistance of the output capacitor and $\mathrm{L_{o,ESR}}$ for the equivalent series resistance of the output choke:

$$\mathrm{P_{cond,filter}} = \mathrm{IL_{o,rms}}^2\mathrm{L_{o,ESR}} + \mathrm{IC_{in,rms}}^2\mathrm{C_{in,ESR}} + \mathrm{IC_{o,rms}}^2\mathrm{C_{o,ESR}} \tag{31}$$

B. SWITCHING AND DRIVING LOSSES

The voltage and current cross over during switching transitions results in switching power losses. Additionally charging and discharging of the MOSFETs gate capacitance causes gate-driving power losses [15].

1) PRIMARY SIDE HV MOSFETS SWITCHING AND DRIVING LOSSES

If the primary side MOSFETs operate under zero voltage switching there is no overlap between voltage and current and transitions could be considered near lossless. However, it is known that in modern super-junction devices the charging and discharging of the device output capacitance shows a hysteresis which is source of an additional power losses that should be considered [24].

The minimum energy required to achieve ZVS transitions for the lagging and the leading leg can be estimated with (32)-(33), with $\mathrm{C_{leading}}$ equal to the sum of capacitances $\mathrm{C_3}$ and $\mathrm{C_4}$, and $\mathrm{C_{lagging}}$ equal to the sum of $\mathrm{C_1}$ and $\mathrm{C_2}$. The lumped capacitance of the transformer $\mathrm{C_{Tr}}$ constitutes an important contribution to the leading leg transition but it does not have an influence on the lagging leg.

$$\frac{\mathrm{V_{in}^2}}{2}(\mathrm{C_{leading}} + \mathrm{C_{tr}}) \le \left(\frac{\mathrm{IL_{r,lead}^2}}{2}\mathrm{L_r} + \frac{\mathrm{IL_{lkg,lead}^2}}{2}\mathrm{L_{lkg}} + \frac{\mathrm{IL_{o,lead}^2}}{2}\mathrm{L_o}\right) \tag{32}$$

$$\frac{\mathrm{V_{in}^2}}{2}\mathrm{C_{lagging}} \le \left(\frac{\mathrm{IL_{r,lag}^2}}{2}\mathrm{L_r} + \frac{\mathrm{IL_{lkg,lag}^2}}{2}\mathrm{L_{lkg}}\right) \tag{33}$$

An efficiency optimized PSFB design operates in full or nearly full ZVS in all the load range. The ZVS is especially important at light and medium loads, where the switching losses become dominant [15], [25]. During partial ZVS the capacitance of the switches is not fully discharged when the device turns-on. For modern HV super-junction MOSFETs the remaining losses are not significative [26]. The use of an external resonant inductance ($\mathrm{L_r}$) in the primary side of PSFB, while increasing the component count, helps achieving ZVS in light to

medium load conditions and thus increases the overall efficiency of the converter. Although it is possible to increase the leakage of the transformer for the same purpose, using an external resonant inductance on the primary side of the converter and placing clamping diodes between the transformer and L_r helps to reduce the secondary side rectifiers overshoot as well as reducing their switching/commutation related losses [27]-[28]. The solution, previously reported in the literature, is analyzed in detail in [29].

To achieve full ZVS, whenever there is enough energy available, a minimum dead time is also required for the transition of the drain voltage. The time it takes for the transition to happen depends on the transfer of energy from the inductances to the capacitances involved in the resonance. The output capacitance of modern MOSFETs is non-linear, an accurate estimation of the transition times is not straightforward. A simple approximation can be estimated with (34), where the capacitance is modelled by an equivalent time related fixed value of capacitance ($C_{o(tr)}$) and the current from the inductances is considered also as a constant current source. $C_{o(tr)}$ is a parameter often provided by the manufacturer in the datasheet of the device.

$$T_{ZVS} \approx \frac{2C_{O(tr)}}{IL} V_{in} \tag{34}$$

However, if there is not enough energy to achieve full ZVS, the transition time could be better approximated by the resonance between the inductors and the capacitors (35)-(36). Because the reflected value of L_o is relatively big the transition of the leading leg can be well approximated by the previous linear model in all working conditions of the converter. However for the lagging leg, the dead time has to match one fourth of the resonance period to switch at the minimum possible voltage.

$$T_{ZVS,leading} \approx \frac{1}{4\omega_1} = \frac{\pi}{2}\sqrt{2C_{o(tr)}(L_{lkg} + L_r + L_o n^2)} \tag{35}$$

$$T_{ZVS,lagging} \approx \frac{1}{4\omega_1} = \frac{\pi}{2}\sqrt{2C_{o(tr)}(L_{lkg} + L_r)} \tag{36}$$

Assuming the dead time to be always optimum (with the devices switching at the minimum possible drain voltage), the switching losses can be estimated with (37) where E_{OFF} is a function of the current and voltage overlap during the turn-off transition. In general, for modern super-junction MOSFETs E_{OFF} is relatively small, but not zero.

$$P_{SW,p} = P_{SW,ZVS} \approx E_{OFF}(i, v) F_{SW}\,,\ v = V_{DS} \leq 0 \tag{37}$$

If the energy is not enough to achieve ZVS part or all the energy stored in the output capacitance is dissipated. The switching losses then becomes (38) where E_{ON} is a function of the current and drain voltage overlap and the E_{OSS} is the stored energy in the output capacitance of the switch, which is also a function of the drain voltage.

$$P_{SW,p} = P_{SW,HARD} \approx (E_{ON}(i, v) + E_{OSS}(v)) F_{SW}\,,\ v = V_{DS} \geq 0 \tag{38}$$

The switching losses could be calculated, measured or simulated and tabulated for different values of current and switching voltages. The switching losses are computationally costly to calculate accurately. Moreover, it is difficult to estimate the real layout parasitics which have a relatively big impact on the losses. Therefore, in the authors' extended model the switching losses where interpolated from a table extracted from experimental measurements and characterization.

The driving losses are a function of the driving voltage V_{drive} and the switching frequency. The reader may note that the gate charge differs in soft switching (ZVS) (39) and hard switching (40). In ZVS the Q_{gd} has been supplied by the power stage during the resonant transition prior to the charge of the switch input capacitance from the driver path.

$$P_{drive,p} = \frac{4(Q_g - Q_{gd}) V_{drive} F_{SW}}{\eta_{bias}}\,,\ v = V_{DS} > 0 \tag{39}$$

$$P_{drive,p} = \frac{4 Q_g V_{drive} F_{SW}}{\eta_{bias}}\,,\ v = V_{DS} \leq 0 \tag{40}$$

2) SECONDARY SIDE LV MOSFETS SWITCHING AND DRIVING LOSSES

It was mathematically demonstrated in [30]-[31] that charging a capacitor inevitably causes energy losses. When charged through a resistive path the resistor dissipates energy equal to the one eventually stored (41)-(43). The analysis shows that a capacitor can be charged with only a modest energy loss in a series RLC circuit only if the source is disconnected after ½ resonance cycle. Otherwise the remaining energy is dissipated during the dampening of the resonance and the energy loss becomes also equal to the stored. Their analysis is consistent with the formula for the estimation of switching losses in SRs in [32].

$$E_{sourced} = E_{stored} + E_{loss} = (2Q_{oss} + 2Q_{rr}) \frac{V_{in}}{n} \tag{41}$$

$$E_{loss} = (Q_{oss} + 2Q_{rr})\frac{V_{in}}{n} \quad , \quad E_{stored} = Q_{oss}\frac{V_{in}}{n} \tag{42}$$

$$P_{sw} = 2F_{sw}(Q_{oss} + 2Q_{rr})\frac{V_{in}}{n} \tag{43}$$

When using clamping diodes on the primary side of the converter part of the energy of the resonance is recovered. During the charge of Q_{rr} and Q_{oss} of the secondary side rectification devices an equal energy is stored in the inductances along the charging path (L_r, L_{lkg}). It follows that the larger L_r is in relation to L_{lkg}, the more energy it stores comparatively. Due to the action of the primary side clamping diodes, the energy in L_r is actually recirculated on the primary side of the converter and does not contribute to the secondary side commutation resonance. Therefore, the switching losses calculated in (41)-(43) are reduced down to the energy calculated in (44)-(46) where E_{clmp} stands for the conduction losses of the clamping diodes which can be estimated from their average current (45).

$$E_{loss} = \frac{V_{in}}{n}\left(Q_{oss}\frac{L_{lkg}}{L_r} + Q_{rr}\left(1 + \frac{L_{lkg}}{L_r}\right)\right) + E_{clmp} \tag{44}$$

$$E_{clmp} = 2V_{F,clmp}I_{avg,clmp} \tag{45}$$

$$P_{SW,SR} = F_{SW}E_{loss} \tag{46}$$

Q_{rr} is not constant but depends on the average forward current of the diode, the conduction time, the temperature of the device and the slope of the current among other factors [32]-[33]. This was taken into consideration in the complete and more accurate model where Q_{rr} might is a linear fitting function of the average current and the slope (47). The coefficients of the relation were extracted from experimental measurements and characterization of the devices.

$$Q_{rr} \propto I_{avg} \ \ and \ \ Q_{rr} \propto \frac{di}{dt} \tag{47}$$

Driving losses is a function of the driving voltage and the switching frequency (48). Because the SRs are operated in ZVS, we can exclude the plateau charge (Q_{gd}) from the driving losses. Notice that the driving voltage V_{drive} is not necessary equal to the driving voltage of the HV MOSFETs. Because of the higher gate charge of the LV MOSFETs in high current output converters, it is usually desirable to lower their driving voltage, always in accordance to the device characteristics.

$$P_{drive,SR} = \frac{2Q_gV_{drive}F_{SW}}{\eta_{bias}} \tag{48}$$

C. CORE LOSSES

The empirical methods based on measurement results are one major group of core losses calculations. A widely used empirical-method is the Steinmetz equation (47) [15]. The frequency of the flux variation F_{core} in (49) is the switching frequency F_{sw} for the main transformer and the resonant inductance but two times the switching frequency for the output choke $2F_{sw}$. V_{core} is the volume of the core, B_{pk} is the peak magnetic flux density, and *k*, *a* and *b* are called the Steinmetz coefficients, which are material parameters generally found empirically from the materials B-H hysteresis curves. The coefficients for the Steinmetz equations are frequently given by the magnetic core manufacturers.

$$P_{Core} = V_{Core}F_{Core}^{a}B_{pk}^{b}k \tag{49}$$

The temperature of the cores also influences the core losses, with some materials having an optimum operating temperature. The relation of core-losses to temperature is often found in the material datasheets. In the authors' extended model the core losses of the transformer are recalculated until the solution converges, also taking into account the transfer of heat from the windings.

The Steinmetz equation accuracy is frequently discussed. In [34] an improved core-loss calculation is proposed. However, there is currently no agreement in a better estimation method. Moreover, manufacturers frequently provide the Steinmetz coefficients or only experimental data for pure sinusoidal excitation at several flux and frequency conditions. In the authors' extended model the core losses are interpolated from the manufacturer's experimental data for the main frequency component of the flux.

D. OTHER LOSSES

1) CONTROL CIRCUITRY AND FAN

The control circuitry in server PSU is generally powered by an auxiliary supply. The efficiency of the auxiliary bias (a converter itself) has to be taken into account in the power consumption of the control circuitry. Moreover,

an internal PSU fan is also commonly supplied from the bias. Therefore, the efficiency of the bias has to be considered also in this case (50).

$$P_{bias} = \frac{(P_{ctrl}+P_{fan})}{\eta_{bias}} \ , \ \eta_{bias} \in [0,1] \tag{50}$$

Alternatively, the fan or the control circuitry could be supplied by the main converter itself. This is especially convenient in server PSU because of their output voltage is commonly equal to the control and fan supplies (12 V). Because of the efficiency of the main converter is normally higher than the small auxiliary converter, this technique slightly improves the overall efficiency of the system. In contrast to the reference converter in this document, in the optimized prototype the fan is supplied by the main converter.

2) CAPACITORS LEAKAGE

In addition to the previously analyzed conduction losses for the input and output capacitors there is an additional contribution from their current leakage (51). The values of current leakage can be often found in the manufacturer's datasheet.

$$P_{cap,leak} = V_{in}IC_{in,leak} + V_oIC_{o,leak} \tag{51}$$

E. OVERALL LOSSES

The overall losses of the converter include all previously analyzed contributions that should be evaluated for each of the load points P_o of interest (52)-(53):

$$P_{cond}(P_o) = P_{cond,Tr}(P_o) + P_{cond,HV}(P_o) + P_{cond,SR}(P_o) + P_{cond,filter}(P_o) \tag{52}$$

$$P_{total}(P_o) = \begin{pmatrix} P_{cond}(P_o) + P_{SW,p}(P_o) + P_{drive,p}(P_o) + P_{SW,SR}(P_o) + \\ P_{drive,SR}(P_o) + P_{bias}(P_o) + P_{Core}(P_o) + P_{cap,leak}(P_o) \end{pmatrix} \tag{53}$$

Because the losses distribution is load dependent, some different losses mechanisms are dominant at different load points. More interesting, reducing the conduction losses at full load often impacts negatively on the switching and core losses at light load and vice versa. Achieving the highest efficiency at mid load is the greatest challenge, because most of the losses contributions have a noticeable impact in that range. Therefore, a converter with the highest efficiency at mid load will have a balanced light and full loads efficiencies, so-called flat efficiency curve.

III. DESIGN CRITERIA

Following the Platinum 80PLUS requirements, the objective for the proposed design was to achieve maximum efficiency at the 50% of load of the converter while having a balanced light (20 %) and full load (100%) performances. The volume is constrained by the standard PSU height (1U). Additionally, the converter should have a reasonable Bill Of Materials (BOM) and/or production cost.

In this section we analyze the impact on the converter's efficiency of the most influential design parameters. In the analysis, the effects of the parameters are described sequentially, in the preferred order of design, and isolated from the other parameters effects. However, the design process is an iterative process and normally with more than one optimal solution. Because of the complex interrelations between the parameters, the possible alternative might be constrained by previous design choices. It is therefore convenient to explore the full space of solutions.

A. CLAMPING DIODES POSITION

The ZVS range of the converter can be extended adding an external resonant inductance (L_r) to the leakage of the transformer. However, the additional inductance causes loss of effective duty cycle and limits the maximum power of the converter at the minimum required input voltage [15], [25]. On the other hand, the secondary side overshoot induced during the commutation of the SRs can be effectively reduced by the usage of clamping diodes between the transformer and L_r, as is suggested in [28].

When using clamping diodes on the primary side of the converter part of the energy of the resonance is recovered. During the charge of Q_{rr} and Q_{oss} of the secondary side rectification devices an equal energy is stored in the inductances along the charging path (L_r, L_{lkg}). It follows that the larger L_r is in relation to L_{lkg}, the more energy it stores comparatively. Due to the action of the primary side clamping diodes, the energy in L_r is actually recirculated on the primary side of the converter and does not contribute to the secondary side commutation resonance.

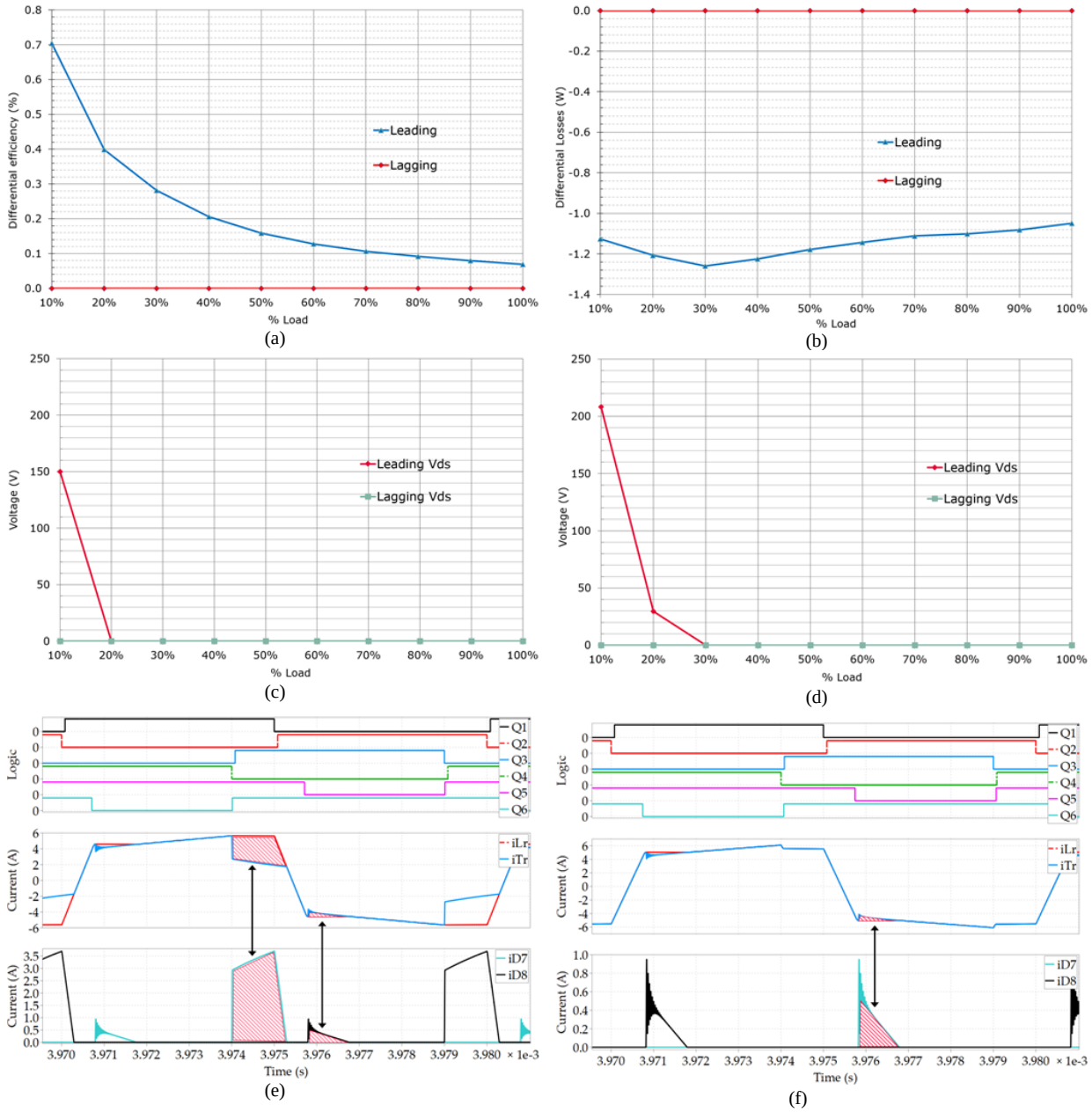


Figure 6. Efficiency for different clamping diodes configuration and the effect on switching voltage of the primary side HV MOSFETs and the primary side circulating currents: (a) Differential efficiencies; (b) Differential losses; (c) Leading and lagging leg switching voltages with the clamping diodes on the lagging leg position; (d) Leading and lagging leg switching voltages with the clamping diodes on the leading leg position; (e) Primary side and clamping diodes current with clamping diodes in the lagging leg; (f) Primary side and clamping diodes current with clamping diodes in the leading leg.

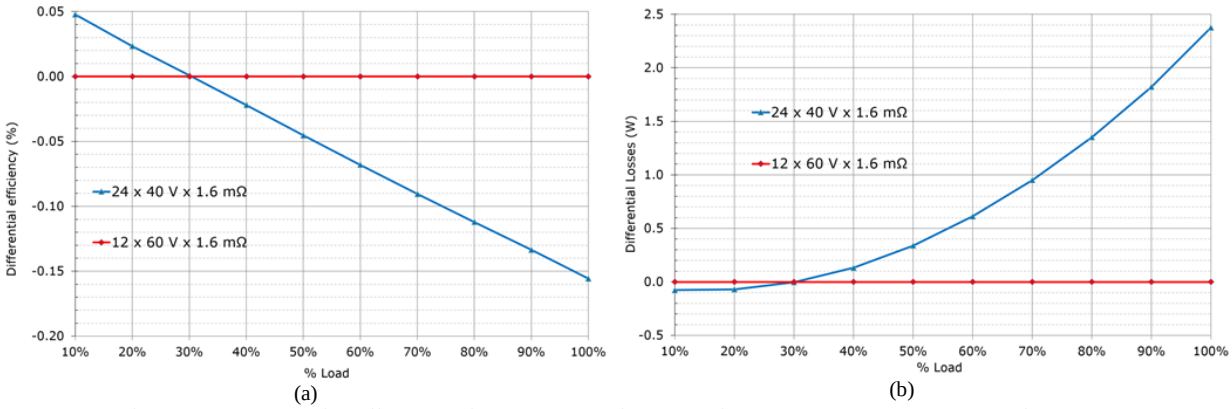
The position of the clamping diodes and the external resonant inductance L_r influences on the current waveforms of the converter and on the overall efficiency of the system [28]. The clamping diodes in the leading position reduces notably the conduction losses along all the load range of the converter (Figure 6). However, the available energy for the ZVS transition of the leading leg is heavily reduced which has a major impact on the switching losses, in the reliability and the control of the converter: the non-linearity of the output capacitance of the HV super-junction MOSFETs makes it challenging to track the optimum dead time for the leading leg, which ultimately increases the switching losses.

In summary, the leading leg configuration of the clamping diodes is not recommended. In the new optimized design the clamping diodes have been placed in the lagging leg position, as in Figure 1, whereas in the reference design the diodes were placed in the leading leg position.

B. RECTIFICATION STAGE CONFIGURATION

Figure 7 shows a comparison between full bridge rectification and center tapped rectification configurations in low voltage server applications. Twice as much switches are required in full bridge configuration to achieve an equivalent $R_{ds,on}$ because the current passes always through two devices along the rectification path. Although the

Figure Of Merit (FOM) of the lower voltage class MOSFETs is better, it is not near twice as better. Therefore, overall the switching and driving losses increase in the full bridge configuration. Moreover, the high number of rectification devices is not practical from power density and cost point of view.



(a) (b)

Figure 7. Performance comparison for different rectification stage configuration of equivalent $R_{DS,on}$. Full bridge rectification with 24 units of 40 V class devices in blue, and center tapped with 12 units of 60 V class devices in red. (a) Differential efficiency; (b) Differential losses.

C. TRANSFORMER TURNS RATIO SELECTION

In PSFB converter, like in other isolated topologies, the blocking voltage of the secondary side devices depends on the rectification stage configuration. However, unlike other resonant topologies, the secondary reflected voltage of the transformer does not depend on the output voltage V_o and it is always necessarily higher than it. The reflected voltage is proportional to the transformer turns ratio and the input voltage, as expressed in (54) where V_E and V_D represents the amplitude of the output voltage of the rectification stage, and N_P and N_S respectively the primary and secondary turns of the main transformer.

$$V_{E,max} = V_{D,max} = V_{in,max}\frac{N_S}{N_P} = \frac{V_{in,max}}{n} \quad , \quad \frac{N_S}{N_P} = n \tag{54}$$

In the PSFB converter the output voltage of the rectification stage is a square wave of duty cycle D_{eff}, with the amplitude of the transformer reflected voltage and the average value V_o (55). D_{eff} is necessarily less than or equal to one and, in practical converters, commonly much smaller, as the transformer turns ratio *n* is constrained by the input and output voltage range requirements: the converter should be capable of regulation at the minimum specified input voltage $V_{in,min}$ and maximum specified output voltage $V_{o,max}$.

$$V_o = V_{in}\frac{D_{eff}}{n} = V_D D_{eff} = V_E D_{eff} \tag{55}$$

Wide input voltage is required, for example, during hold-up time conditions [8], [10], [35]. The power supply needs to maintain its output voltage during a time period of 20 ms (T_{hold}) after the input AC line is lost. The resulting minimum input voltage at the end of T_{hold} depends on the power supply intermediate storage capacity C_{bulk}, the nominal operating voltage, the maximum power of the DCDC converter $P_{o,max}$ and its efficiency η_{DCDC} (56). A simple solution to hold-up is to increase the amount of intermediate storage, which however increases the cost and reduces the power density.

$$C_{bulk}\frac{V_{in,nom}{}^2 - V_{in,min}{}^2}{2} = \frac{P_{o,max}}{\eta_{DCDC}}T_{hold} \tag{56}$$

The wide regulation requirement makes PSFB converter not to be operated with its maximum duty in nominal state. The turns ratio of the transformer is constrained by $V_{in,min}$ and $V_{o,max}$. Additionally, because of the time it takes the current through the transformer to reverse polarity part of the otherwise available duty is lost (D_{loss}), which further constraints the maximum possible transformer turn ratio (57)-(61). During the remaining duty, the so-called freewheeling (D_{frew}), the primary current recirculates without transferring energy to the output of the converter.

$$D_{loss} = 2F_{sw}\frac{(L_r + L_{lkg})}{V_{in}}\Delta IL_{r,1} \tag{57}$$

$$\Delta IL_{r,1} \approx \frac{2IL_{o,avg}}{n} \quad , L_o \text{ in CCM} \tag{58}$$

$$D_{loss,max} = 4F_{sw}\frac{(L_r + L_{lkg})}{V_{in,min}}\frac{IL_{o,avg,max}}{n} \tag{59}$$

$$D_{eff} + D_{frew} + D_{loss} = 1 \tag{60}$$

$$D_{frew} \geq 0 \xrightarrow{\text{yields}} V_{in,min} \geq \left(nV_{o,max} + \frac{4F_{sw}(L_r+L_{lkg})IL_{o,avg,max}}{n}\right) \quad (61)$$

On the other hand, the realizable transformer turns ratio is constrained by its mechanical construction: the available room for the windings, the wire size, and the amount of interleaving between primary and secondary windings. A planar construction reduces the transformer leakage which impacts the secondary side overshoot and consequently the required rectifier's voltage class. The bigger transformer capacitance in planar construction does not have a big impact on the ZVS capability, but does have an impact on the EMI performance. For isolated power converters, the inter-winding capacitance of the transformer and is a critical coupling path for Common Mode (CM) noise. The (CM) noise model of PSFB converter is analyzed in detail in [36]-[37]. However, the capacitance can be adjusted with low dielectric constant isolation between primary and secondary windings. In both of the designs analyzed in this work the transformers have a planar or semi-planar construction:

- In the reference design the primary winding of the transformer is made of forty-four turns built in PCB and distributed in three sections and the secondary winding of the transformer is made of four times two plus two turns (center tapped) interleaved with the primary in four sections.
- In the new design the primary winding of the transformer is made of two times twenty-one turns of Litz wire distributed in six sections and the secondary winding of the transformer is made of four times one plus one turns interleaved with the primary in eight sections.

Figure 8 shows a comparison among the reference design turns ratio (44:2:2), the new design turns ratio (21:1:1) and some possible similar variants (24:1:1 and 18:1:1). To fulfill the input wide range requirements of the converter L_r was adjusted consequently for each of the turn ratios. From the results in Figure 8 we can extract some conclusions:

- More primary turns reduces the core losses of the transformers which helps to improve the light load efficiency. However it also increases the conductions losses at mid and full load because of the extra winding length and the relatively reduced wire size.
- A larger turns ratio decreases the transformer secondary side reflected voltage, which reduces the freewheeling time and circulating currents. Potentially it could also enable a lower voltage class for the secondary side devices. However it limits the maximum possible L_r which in turn limits the ZVS range of the lagging leg. This can be noticed by the comparison among the 24:1:1 and 21:1:1 variants where the higher ratio performs worse at light load because of the extra switching losses.

In summary, primary side turns should be as high as possible without compromising conduction losses, and turns ratio high enough to fit the best possible SRs' voltage class. Additionally, increasing the primary winding number of turns also helps to implement a bigger magnetizing inductance L_m. Increasing the magnetizing inductance helps reducing the primary side circulating currents, reducing conduction losses and overall improving efficiency (Figure 9).

On the other hand, a compromise in L_m value is required since reducing the magnetizing inductance increases the available energy for the ZVS transition of the primary side HV switches. As shown in Figure 10, this enables full ZVS for the lagging leg at very light loads.

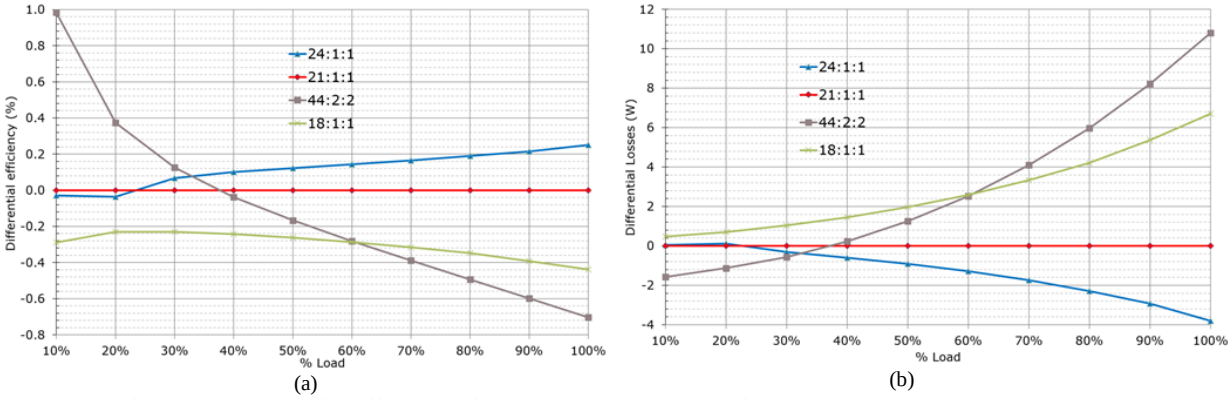
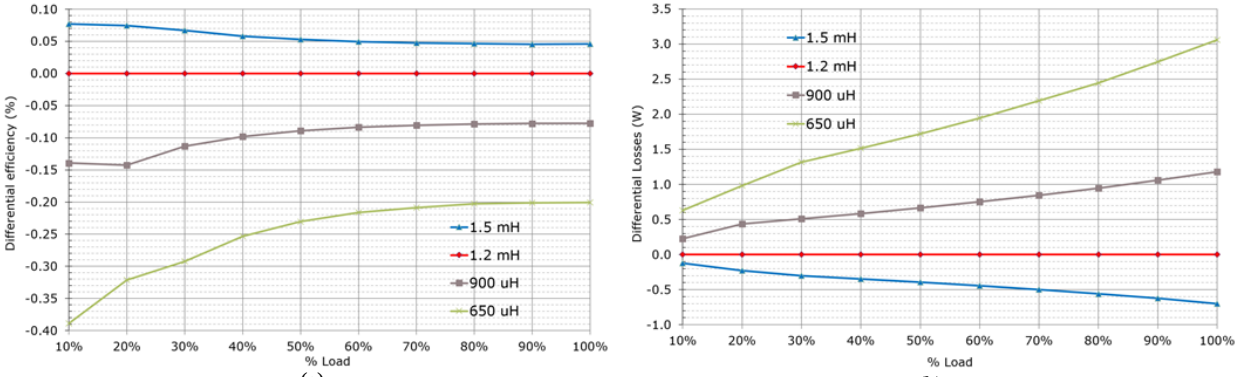


Figure 8. Performance comparison for different transformer turns ratios. The value of L_r is adjusted to maintain the required input voltage range. The original reference converter had a turn ratio of 44:2:2. The optimized converter has a turn ratio of 21:1:1. (a) Differential efficiency of the converter with the different configurations; (b) Differential power loss of the converter with the different configurations.



(a) (b)

Figure 9. Performance comparison for different magnetizing inductances: (a) Differential efficiency; (b) Differential losses.

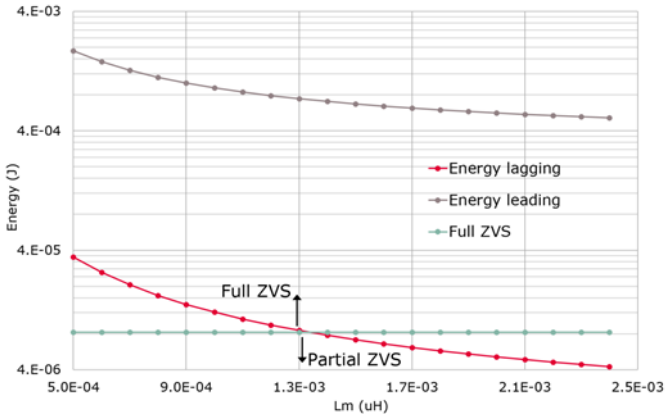
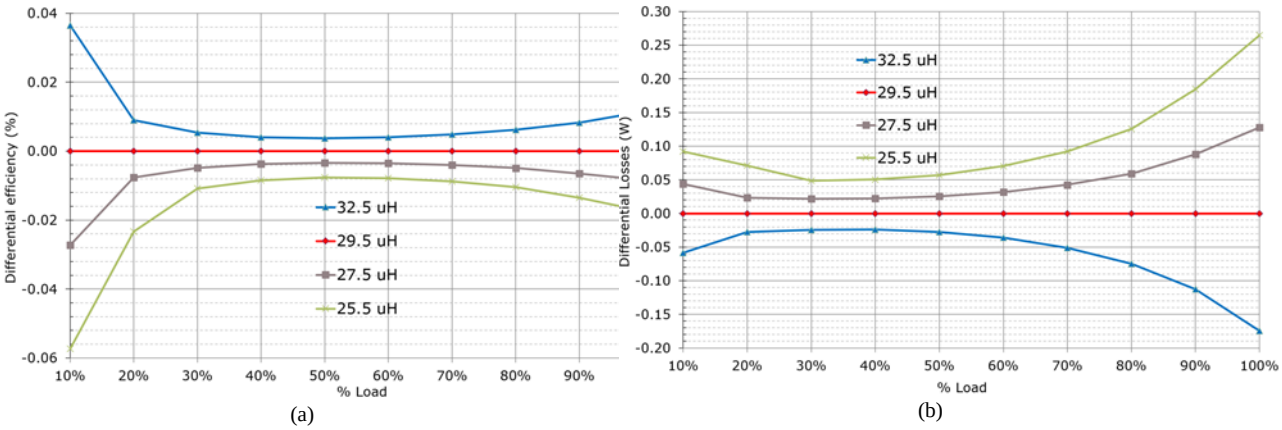


Figure 10. Available energy for the ZVS transitions depending on the value of the magnetizing inductance with the converter operating at 10 % of load.

D. EXTERNAL RESONANT INDUCTANCE AND LEACKAGE

Figure 11 shows the impact of increasing and decreasing the external resonant inductance with the reference being the nominal L_r value of the optimized prototype. The inductance is modified by changing the gap size between the ferrite cores, but keeping the same amount of turns. A larger resonant inductance decreases the conduction losses because the circulating currents are effectively reduced, however the hold-up time regulation cannot be fulfilled unless the transformer turn ratio or the amount of bulk capacitance is adjusted in consequence. Additionally a larger L_r increases ZVS energy at light load, which potentially reduces switching losses or enables a lower HV MOSFETs $R_{ds,on}$.



(a) (b)

Figure 11. Performance comparison for different external resonant inductances: (a) Differential efficiency; (b) Differential losses.

E. OUTPUT FILTER INDUCTOR

The output filter inductor selection is constrained by the output current ripple and the maximum output voltage ripple requirements. The output current ripple can be calculated with the equation (62), which has an impact on the *rms* losses in the output capacitors (63). The maximum output voltage ripple is also a function of the total

amount of output capacitance and its parasitic equivalent resistance (64)-(66). Moreover, a small value of inductance at the output makes the secondary side rectifiers operate in DCM at light loads. When operating with SRs this can introduce additional complexity and reliability issues [29].

$$\Delta IL_o \approx \frac{T}{2}\frac{\left(\frac{V_{in}}{n}-V_o\right)D_{eff}}{L_o} \tag{62}$$

$$\begin{cases} iC_o \approx \frac{\left(\frac{V_{in}}{n}-V_o\right)}{L_o}t - \frac{\Delta IL_o}{2} \ , \ t \in \left[0, D_{eff}\frac{T}{2}\right] \\ iC_o \approx \frac{\Delta IL_o}{2} - \frac{V_o\left(t-D_{eff}\frac{T}{2}\right)}{L_o} \ , \ t \in \left[D_{eff}\frac{T}{2}, \frac{T}{2}\right] \end{cases} \tag{63}$$

$$vC_{o,ripple} = C_{o,ESR}iC_o + \int_0^t \frac{iC_o}{C_o}dt + V_{o,ripple}\Big|_{t=0} \tag{64}$$

$$VC_{o,ripple,min} = \frac{(V_o n - V_{in})\left(16{C_o}^2{C_{o,ESR}}^2 + {D_{eff}}^2T^2\right)}{32C_oL_on} \tag{65}$$

$$VC_{o,ripple,max} = \frac{V_o\left(4{C_o}^2{C_{o,ESR}}^2 + {D_{eff}}^2T^2\right)}{8C_oL_o} \tag{66}$$

A side effect of L_o value is the available energy for the ZVS transitions on the primary side of the converter. In the simplified model, not considering the effect of the clamping diodes, because $I_{p,lead}$ increases and $I_{p,lag}$ decreases for bigger output current ripples, the ZVS range of the lagging leg is extended for larger values of L_o. However, because of the effect of the clamping diodes in the lagging position, both $I_{p,lead}$ and $I_{p,lag}$ increase for larger output current ripples, and the ZVS range of the lagging leg can be further extended with smaller values of L_o (Figure 12).

In the realization of L_o a low permeability core is preferred because maintains a more stable value of inductance along the load and the core losses are normally lower. For a given core geometry and core material the core losses and copper losses can be balanced adjusting the number of turns and the number of parallel wires. However, the available winding room in the core limits the possible combinations. In Figure 13 we compare the effect of only changing the number of turns in the output choke of the optimized prototype design: 1.88 µH corresponds to the five turns of five parallel wires of the prototype; 2.70 µH corresponds to six turns and five parallel wires; 1.20 µH corresponds to four turns and five wires; and 3.68 µH to seven turns and five wires. Although for the estimation of losses in Figure 13 the number of wires or their diameter has not been adjusted the impact on the conduction losses is already visible because of the variations in winding length.

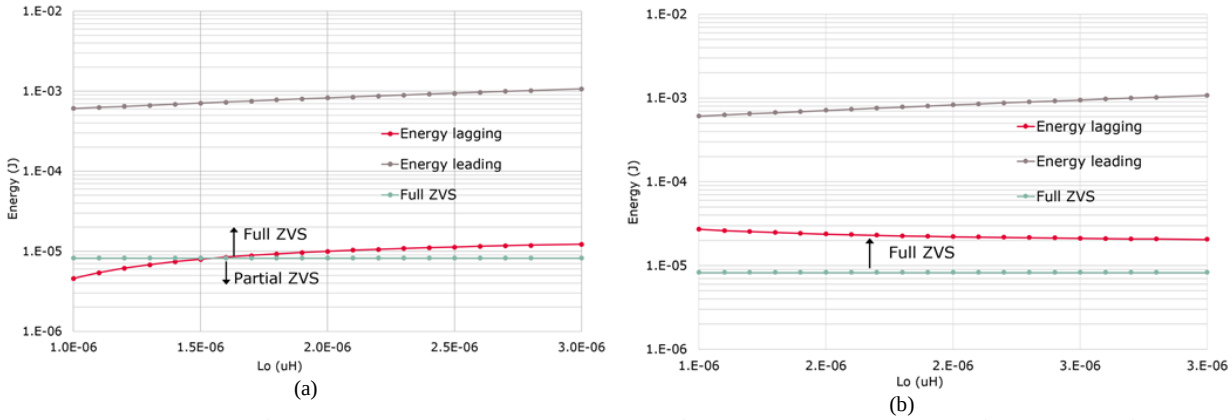
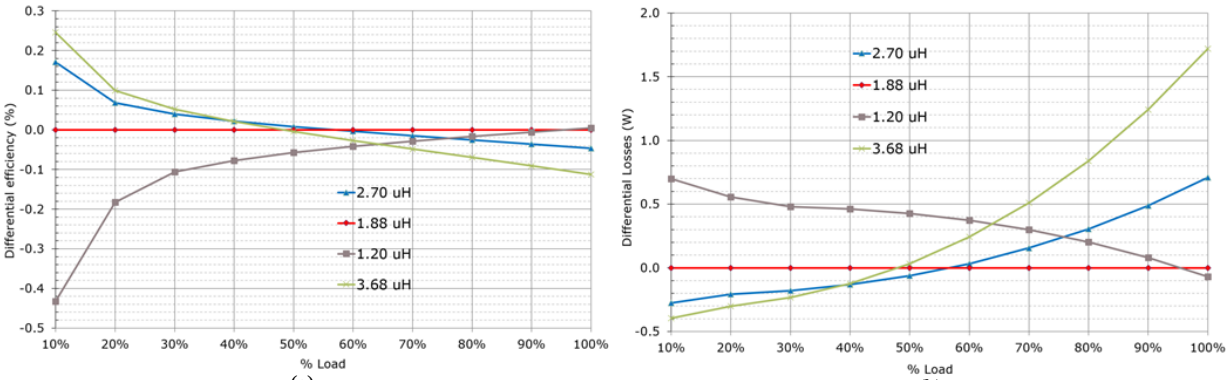


Figure 12. Available energy for the ZVS transitions depending on the value of the output inductor Lo. At 10 % of load. (a) Simplified model without clamping diodes. (b) With primary side clamping diodes in the lagging leg.



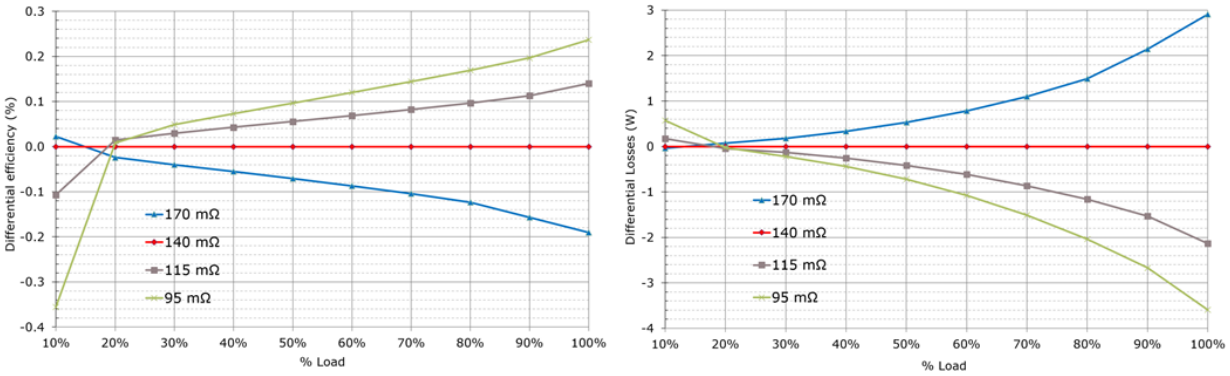
(a) (b)

Figure 13. Performance comparison for different number of turns of the output inductor: (a) Differential efficiency; (b) Differential losses.

F. PRIMARY SIDE HVS MOSFETS AND SECONDARY SIDE SRS LV MOSFETS

The balance of switching losses and conduction losses for the different $R_{ds,on}$ allows the balance of the efficiency curve. The possible values are limited to the available portfolio of the selected MOSFET technology. Unfortunately there have been reports of failures of the primary HV MOSFETs during load jumps, light-load operation and start-up of the converter. The failure modes are linked to the incomplete clearance of the reverse recovery charge of the intrinsic body diode followed by the turn-on of the opposite half bridge device, so called hard-commutation. The remaining charge creates a large current at turn-on which may cause the failure of the MOSFET. To overcome this problem the use of MOSFETs with reduced Q_{rr} and rugged body diode has been suggested in [38]. Therefore, the most recommendable choice for the primary side HV MOSFETs is CoolMOS™ CFD7.

The available $R_{ds,on}$ also depends on the package selection (the package itself contributes to the equivalent resistance). In the optimized prototype all semiconductors are Surface Mount Devices (SMD). The selected $R_{ds,on}$ for the final design is 140 mΩ. The resulting efficiency for a few of the available $R_{ds,on}$ is compared in Figure 14. Because of the large available ZVS energy of the converter 115 mΩ is performing nearly better in all load range. The final selection of $R_{ds,on}$ is a matter of cost.



(a) (b)

Figure 14. Efficiency for different HV MOSFETs $R_{DS,on}$: (a) Differential efficiencies; (b) Differential losses.

G. SECONDARY SIDE SRS LV MOSFETS

The voltage class selection of the SRs is key for the final performance of the system. The voltage class influences heavily on the MOSFET characteristics, frequently benchmarked by their Figure Of Merit (FOM) [39]. A summary of the characteristics of two devices with similar $R_{ds,on}$ in Table 2 shows the influence of the blocking voltage in their characteristic charges and forward voltage drop, which ultimately affects the switching and conduction losses. A lower voltage class is enabled by a proper design of the transformer turns ratio, a reduction in the leakage combined with a big external resonant inductance and clamping diodes [29]. Any additional overshoot above the nominal blocking voltage would require to further increase the maximum limits of the blocking voltage capabilities of the rectification devices; or alternatively to use clamping or snubbering mechanisms that bring additional power losses, complexity and cost [22], [25]. Furthermore, it is a common practice in the design of switched mode power supplies (SMPS), to limit the maximum stress on the components (voltage, current, temperature) to a rated percentage of their safe maximum limits under any normal working conditions of the converter [40]. The rating percentage depends on the application, lifetime and reliability requirements, but 80 % is a common choice. For semiconductor devices the commonly rated parameters are the maximum drain voltage and the working temperature.

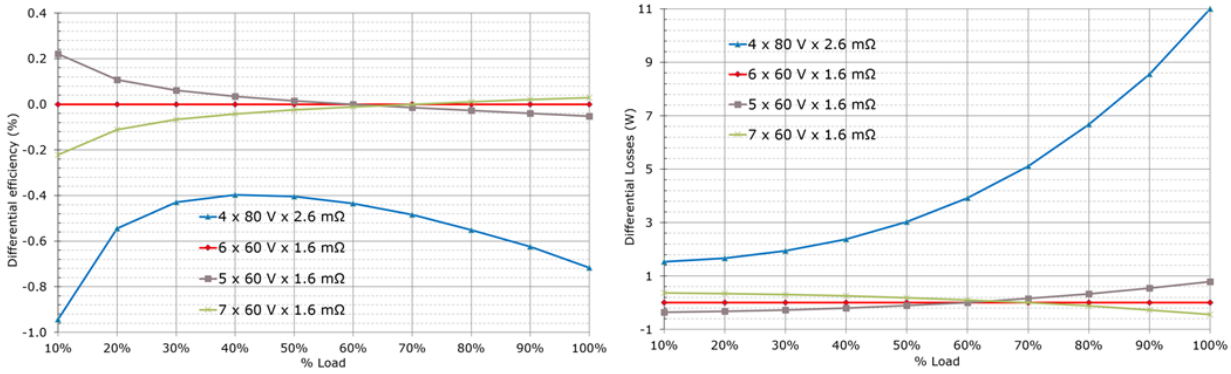
TABLE II
SI LV MOSFETS

Parameter	BSC026N80NS5	BSC027N60LS5
$V_{DS,max}$	80 V	60 V
$R_{DS,on,max}$	2.6 mΩ @ 25 °C	2.7 mΩ @ 25 °C
Q_{oss}	88 nC	43 nC
Q_{rr}	92 nC	36 nC

Figure 15 shows the impact of the selection of voltage class between the former reference design, with 80 V MOSFETs, and the selection of the optimized prototype design, with 60 V devices. The losses both at light load and full load are higher, which indicates an increase in both the switching and conduction losses that cannot be balanced by $R_{ds,on}$ or paralleled devices. Like for the HV MOSFETs, the selection of the SRs $R_{ds,on}$ can balance the efficiency between light and full load by modifying the distribution of switching to conduction losses.

The number of paralleled devices adds another degree of freedom, at the expense of the extra cost and PCB area. Figure 15 compares the efficiency of different number of rectification devices, which effectively decrease the equivalent resistance of the rectification stage.

The Si-MOSFETs have been widely used to improve power density and efficiency. However, the SiC MOSFET and the GaN HEMT are promising alternatives to achieve high efficiency and high switching frequency. The advantages of Wide Band Gap (WBG) devices are lower parasitic capacitances, lower equivalent $R_{ds,on}$, zero reverse recovery charge and higher operating temperature capabilities. In [41] the efficiency of 2kW PSFB designs based on Si and SiC MOSFETs is measured and compared. In [21] the efficiency improvement in a 500 W PSFB converter with GaN HEMT SRs is verified experimentally.



(a) (b)

Figure 15. Efficiency for different LV MOSFETs voltage class and number of devices: (a) Differential efficiencies; (b) Differential losses.

H. INPUT AND OUTPUT CAPACITANCE

The previous analysis demonstrates the influence of the input and output capacitances in the hold-up time operation and the output voltage ripple. However, the capacitors occupy large a volume and are costly, which will ultimately constraint their selection. Although the leakage current of the capacitors adds some losses, these losses are relatively small and in general can be dismissed.

I. SWITCHING FREQUENCY SELECTION. BALANCE OF LOSSES

The switching frequency is a key parameter to be optimized for the converter. A specific frequency achieves its maximum efficiency only under a given set of operating conditions. In [15] a variable switching frequency control method has been adopted in a PSFB DCDC converter to improve the efficiency. This method imply wide variations in switching frequency, which makes it difficult to design filter and control circuits, so these techniques are hard to implement in the PSFB converter.

For the two designs in this document the switching frequency was selected to be in the range of 100 kHz and all the other design variables chosen consequently. The transformer construction and the magnetics volume have the major impact in the resulting range of optimum switching frequencies for the converter, and/or vice versa. Figure 16 plots the efficiency patterns of the optimized prototype for different switching frequencies. For the point of load of interest (50 %) the estimated peak efficiency is reached around the target switching frequency.

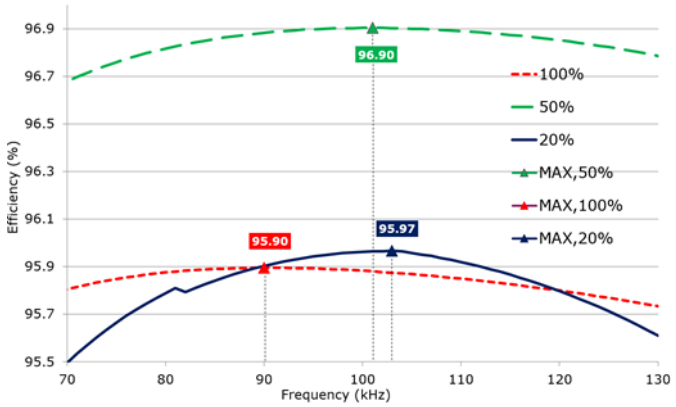
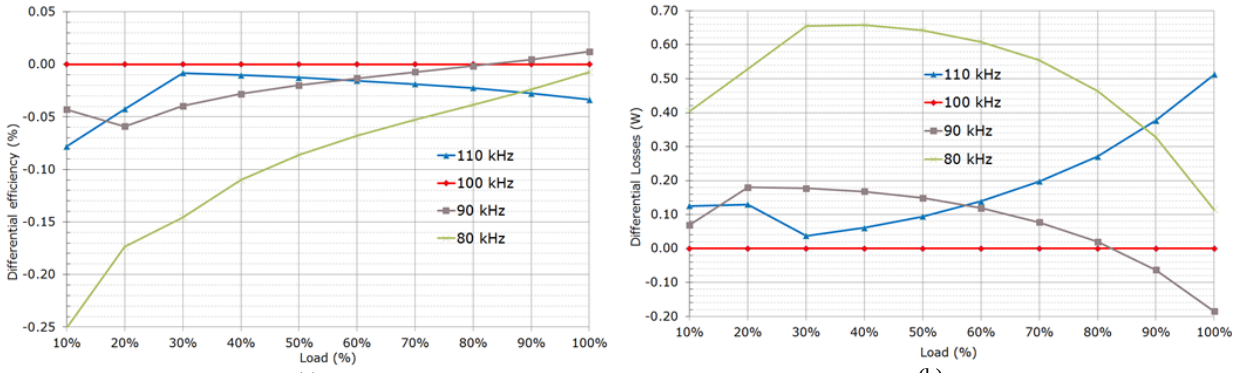


Figure 16. Efficiency plot of the system as a function of the switching frequency. Not including fan. Keeping the wide input design maintaining a minimum freewheeling time (Lr is updated for each frequency in consequence).



(a) (b)

Figure 17. Performance comparison for different switching frequencies: (a) Differential efficiencies; (b) Differential losses.

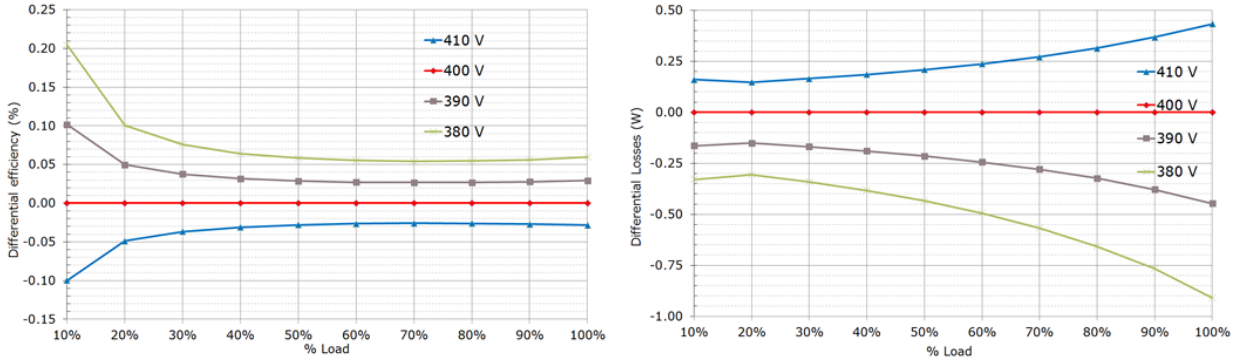
Figure 16 compares the overall system efficiency along the load range only modifying the switching frequency in the optimized prototype design, which was designed for peak efficiency at 50 % of load at 100 kHz F_{sw}. In the estimation of efficiencies L_r was also modified to account for the different freewheeling times available when the switching frequency changes. As depicted on Figure 17 the efficiency at 100 % of load peaks at 90 kHz F_{sw}, like previously reported in Figure 16.

J. THERMAL MANAGEMENT

Although the fan consumption is normally not taken into account while measuring efficiency for the 80 plus certification, the temperature of the converter has a major impact on the performance. Most of the losses contributions have a positive coefficient in relation to the temperature: the $R_{ds,on}$ of MOSFETs increases with temperature, like also does the resistance of the metallic conductors. However, some of the losses have a negative temperature coefficient: the forward voltage drop of diodes decreases with temperature; and the core losses of some magnetic materials has a minimum at a relatively high temperature. Controlling the temperature, or the fan speed, could impact notably the efficiency along all the load range.

K. INPUT AND OUTPUT VOLTAGE

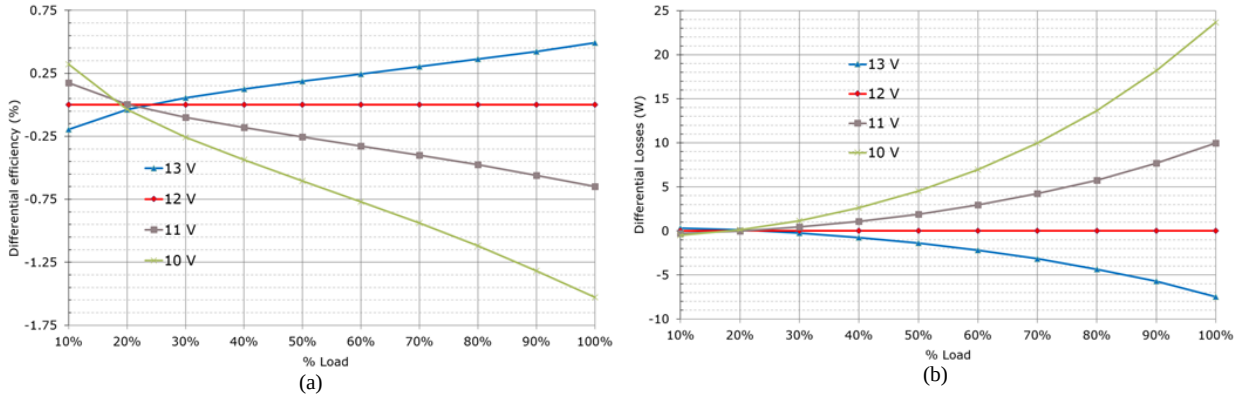
Whereas the output voltage depends on the application and it is usually fixed to a certain value, the nominal input voltage can be adjusted taking into account the previously discussed hold-up time requirements. Moreover, other system restrictions apply: the bulk voltage has to be higher than the maximum VAC peak voltage for the PFC functionality to work (the front end is most commonly a boost converter). For the PSFB DCDC converter the efficiency is higher for lower input voltages mostly because of the reduction in switching, core losses and magnetizing currents. For the results in Figure 18 and Figure 19 the converter design was fixed only varying the input voltage operating point and the output voltage operating point, consequently the freewheeling time and the circulating currents are also reduced.



(a) (b)

Figure 18. Performance comparison for different nominal input voltages: (a) Differential efficiency; (b) Differential losses.

Increasing the output voltage operation point has a similar effect than reducing the input voltage reducing the freewheeling time and the circulating currents. However, this is usually fixed by the application requirements. In the intended application, in server power supplies typically 12 V.



(a) (b)

Figure 19. Performance comparison for different nominal output voltages: (a) Differential efficiency; (b) Differential losses.

IV. COMPARISON OF TWO PSFB CONVERTER DESIGNS

In this section two different designs of DCDC PSFB converters for server applications are compared. Both converters have a maximum power of 1.4kW, same input voltage range, nominal input voltage 400 V and 12 V output voltage. The first design serves as a reference with state-of-the-art performance levels. The second converter has been designed with the provided loss model and design criteria. The new design improves the performance of the reference design in all working conditions while also achieving a higher power density.

A. SUMMARY OF SPECIFICATIONS

For a fair comparison, both converters have the same basic requirements, summarized in Table 3, targeting the front-end DCDC converter of a full PSU for server applications. The nominal operating voltage is 400 V, while the converters should be capable of regulation at full load down to 360 V required during hold-up time. The nominal output voltage is 12 V. During dynamic load jumps the overshoot and undershoot should fall within less than ±5 % of the nominal output voltage. The load jumps are defined from 5% to 50% of load and from 50% of load up to 100% of load with a *di/dt* of 1A/µs.

TABLE III
SUMMARY OF CONVERTER DESIGN SPECIFICATIONS

Parameter	Minimum	Nominal	Maximum
Vin	360	400	415
Vout	11.5	12	12.5
Iout	0	-	117

B. SUMMARY OF DESIGN DATA

Both designs use the same HV MOSFETs technology, 600 V CoolMOS™ CFD7 from Infineon Technologies AG. The reference design mounts through-hole devices, which are capable of higher power dissipation. The optimized design mounts all semiconductor switches in SMD. Although the power dissipation could be more challenging, an SMD solution achieves easily higher power density with less building complexity. In the new design

the $R_{ds,on}$ of the HV MOSFETs is slightly reduced (Table 4 and Table 5) taking advantage of the higher amount of energy available for the ZVS transitions at light loads.

The voltage class of the secondary side rectifier MOSFETs has been improved from 80V in the reference design down to 60V in the new optimized design. The improved transformer construction (less leakage), improved PCB layout, bigger value of external resonant inductance together with novel control techniques ensure that the drain voltage overshoot remains well within rated limits in all working conditions of the new converter. The better figure of merit of the 60 V technology enables the usage of lower $R_{ds,on}$ and higher number of devices without sacrificing light or medium load efficiency thanks to the comparative reduction in switching and driving losses.

TABLE IV
PRIMARY SIDE HV MOSFETS AND SRS MOSFETS IN REFERENCE DESIGN

Designator	Part Number	Units	V(BR)DSS	$R_{DS,on}$
Bridge (Q1-Q4)	IPP60R170CFD7	4	600 V	170 mΩ
SR (Q5-Q6)	BSC026N80NS5	8	80 V	2.6 mΩ

TABLE V
PRIMARY SIDE HV MOSFETS AND SRS MOSFETS IN OPTIMIZED DESIGN

Designator	Part Number	Units	V(BR)DSS	$R_{DS,on}$
Bridge (Q1-Q4)	IPL60R140CFD7	4	600 V	140 mΩ
SR (Q5-Q6)	BSC016N60NS5	12	60 V	1.6 mΩ

The transformer turns ratio is very similar in both cases (44:2:2) and (21:1:1). The higher number of primary turns of the reference design reduces notably the core losses at light and medium loads, furthermore aided by the smaller core volume (Table 6 and Table 7). However, the high number of turns and the smaller room for the windings penalizes heavily on the conduction losses at full load. The new design has a more balanced relation between core and conduction losses among light, medium and full load. Moreover, the novel mechanical construction improves the coupling and reduces the leakage without excessive impact on the intra-winding and inter-winding capacitances thanks to the usage of an isolation with low dielectric constant.

TABLE VI
INDUCTANCE VALUES AND THEIR WINDING REALIZATION IN REFERENCE DESIGN

Designator	Inductance	Turns	Windings	Strands	Diameter
Lm	1.2 mH	44	1	1	0.35 mm
Lr	12 µH	6	1	105	0.071 mm
Lo	5.65 µH	6	5	1	1.25 mm

TABLE VII
INDUCTANCE VALUES AND THEIR WINDING REALIZATION IN OPTIMIZED DESIGN

Designator	Inductance	Turns	Windings	Strands	Diameter
Lm	1.2 mH	21	2	7	0.3 mm
Lr	29.5 µH	8	1	140	0.1 mm
Lo	1.88 µH	5	5	1	1.45 mm

The nominal magnetizing inductance is equal in both designs, aiming to reduce the circulating currents. The external resonant inductance, however, is twice as big in the optimized design, which extends the full ZVS range for the lagging leg down to almost no load, whereas in the former reference design the lagging leg is partially hard switched up to near full load (further exacerbated by the clamping diodes position).

In the new design the output inductance value has been reduced using a core with lower permeability material but improved core losses (Table 8 and Table 9). The balance of core losses to conduction losses has been also improved reducing the number of turns and increasing the wire diameter. Furthermore, the smaller output inductance provides additional energy for the lagging leg ZVS, as previously analyzed.

TABLE VIII
MAGNETIC CORE SELECTION IN REFERENCE DESIGN

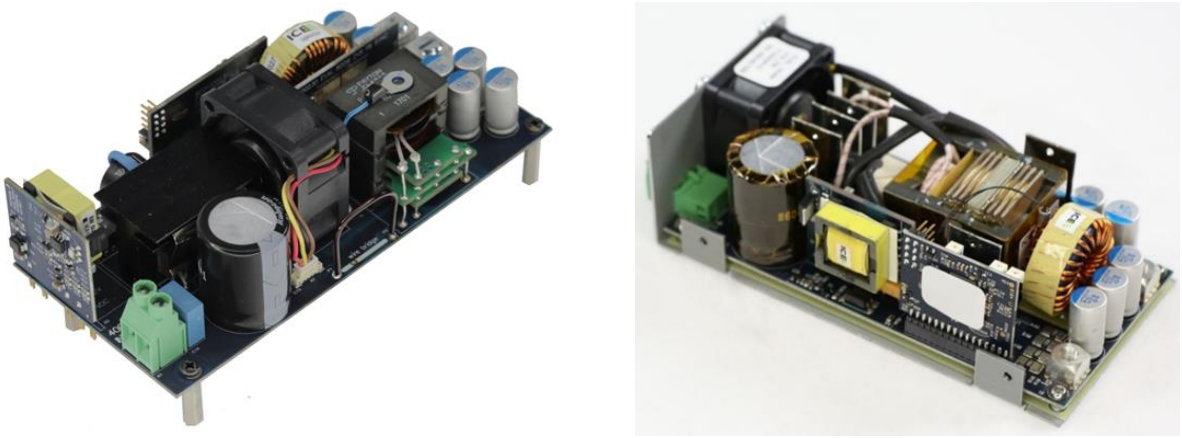
Designator	Part Number	Manufacturer	Material	Permeability
Tr. Core	EQ30	TDG	TP4A	2400 µ
Lr. Core	EQ30	TDG	TP4A	2400 µ
Lo. Core	C058930A2	Magnetics	High Flux	125 µ

TABLE IX
MAGNETIC CORE SELECTION IN OPTIMIZED DESIGN

Designator	Part Number	Manufacturer	Material	Permeability
Tr. Core	PQ35/28	DMEGC	DMR95	3300 µ
Lr. Core	PQI35/23	DMEGC	DMR95	3300 µ
Lo. Core	HP 270	Chang Sung	HP	60 µ

The stacked magnetic structure integrated by the transformer and the external resonant inductance has a bigger core volume in the new design, which incurs in higher core losses and impacts in the light and medium load

converter losses. On the other hand, there is more room for the windings which enables more conduction area and decreases the conduction losses at medium and full load.



(a) (b)

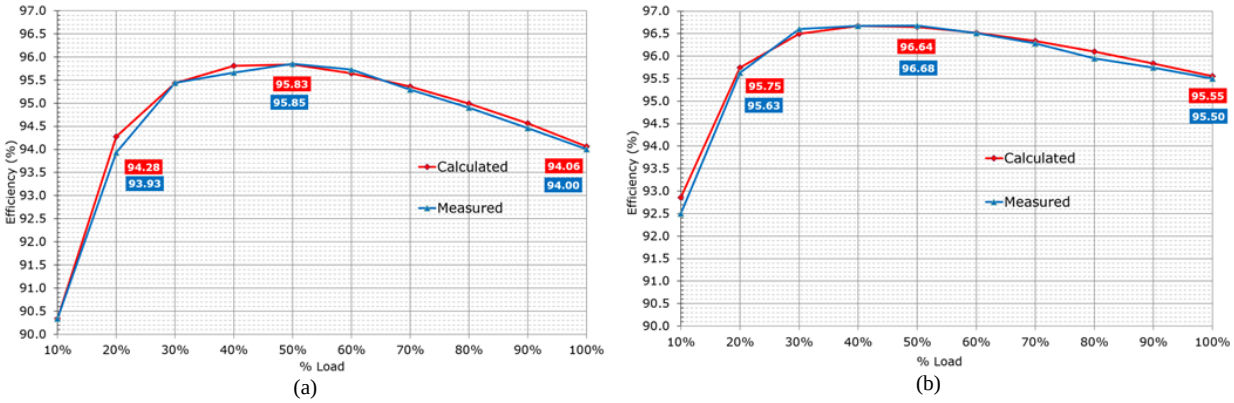
Figure 20. Prototypes of PSFB DCDC converter for server applications: (a) Original reference design; (b) Optimized design.

V. RESULTS

Two prototypes of PSFB converter, one of the reference design [42] and one of the new optimized design [43] were built and tested to compare their performance. Figure 20 shows a capture of both converters. While the reference design operates with open frame, the new design operates within an enclosure, not shown in Figure 20 for clarity. Many of the building components among the two converters are the same and have no impact on the difference in performance: input capacitor (size and model), output capacitors (size and model, but not number), fan, auxiliary bias supply and controller. The overall dimensions of the reference designs are 150 mm x 70 mm x 44 mm, which results in a power density in the range of 3.03 W/cm³ (49.66 W/in³). The overall dimensions of the new design are 133 mm x 64.5 mm x 44 mm, which results in a power density in the range of 3.70 W/cm³ (60.78 W/in³).

C. SUMMARY OF PERFORMANCE

Figure 21 shows the measure efficiency of the reference and the new design. The efficiency was notably improved in all load range. Table 10 is a summary of the requirements for the back-end PFC ACDC converter, which may accompany the new PSFB design in a full PSU achieving one of the 80 PLUS certification level (Table 1). This demonstrates the impact of the efficiency of the front-end DCDC stage in the final efficiency of the system and/or the imposed constraints on the back-end stage by a poorly designed DCDC. The efficiency levels for the ACDC PFC stage listed in Table 10 for the 80 PLUS Platinum can be achieved with a classic Continuous Conduction Mode (CCM) Boost converter with passive diode bridge rectification. This confirms the suitability of the design for an 80 PLUS Platinum server PSU. However, the required PFC efficiency levels for the 80 PLUS Titanium listed in Table 10 are beyond the levels commonly achieved with classic topologies.



(a) (b)

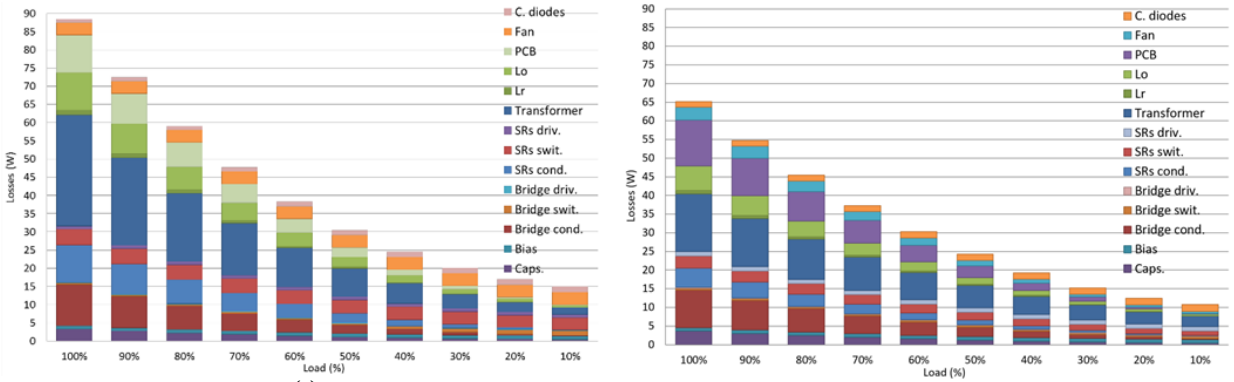
Figure 21. Overall efficiency of the converters, including fan consumption. (a) Original reference design. (b) New optimized design.

TABLE X
SUMMARY OF EFFICIENCY REQUIREMENTS FOR BACK-END PFC ACDC STAGE

80 PLUS Certification	**230 V Internal Redundant (PFC ACDC stage)**			
% of Rated Load	**10 %**	**20 %**	**50 %**	**100 %**
80 PLUS Bronze	-	84.5 %	87.7 %	84.6 %
80 PLUS Silver	-	88.7 %	91.9 %	88.8 %
80 PLUS Gold	-	91.8 %	95.0 %	91.9 %
80 PLUS Platinum	-	**93.9 %**	**97.0 %**	**95.1 %**
80 PLUS Titanium	96.9 %	98.1 %	99.1 %	95.1 %

The calculated efficiency was based on the losses model presented previously in this document which was further adjusted based on the measurements of efficiency and temperature of the different components in the converter. The losses model and its adjustment based on the measurements of the real hardware allows the estimation of the losses distribution of the two converters for the different points of load. The estimated distribution of losses is summarized in Figure 22. From the estimations, in both designs the main losses contribution corresponds to the stacked magnetic structure integrated by the transformer and the external resonant inductance. Table 11 and Table 12 details the previous Figure 22 numerically.

At full load, the difference in losses between the reference design and the new design is near 25 W. The extra losses make much more difficult to cool down the converter. This is confirmed by the position of the fan in the reference design, directly blowing over the integrated magnetic structure and the SRs.



(a) (b)

Figure 22. Overall estimation of losses based in the loss model and the experimental results. (a) Reference design. (b) Optimized design.

TABLE XI
SUMMARY OF THE DISTRIBUTION OF LOSSES IN THE REFERENCE DESIGN

Contribution	**100% Load**	**50% Load**	**20% Load**
Bias	0.96 W	0.96 W	0.96 W
Fan	3.45 W	3.45 W	3.45 W
Tr. Core	0.53 W	1.28 W	1.59 W
Tr. Conduction	29.98 W	6.53 W	1.07 W
Lr Core	0.18 W	0.08 W	0.02 W
Lr Conduction	1.20 W	0.26 W	0.04 W
Lo Core	0.58 W	0.58 W	0.58 W
Lo Conduction	9.65 W	2.17 W	0.33 W
Bridge Conduction	11.24 W	2.29 W	0.33 W
Bridge Switching	0.42 W	0.42 W	1.29 W
Bridge Driving	0.18 W	0.18 W	0.18 W
SRs Conduction	10.29 W	2.63 W	0.48 W
SRs Switching	4.33 W	3.70 W	3.35 W
SRs Driving	0.89 W	0.89 W	0.89 W
Clamping Diodes	0.9 W	1.30 W	1.50 W
Capacitors	3.28 W	1.13 W	0.53 W
PCB	10.32 W	2.58 W	0.41 W
Total	**88.38 W**	**30.43 W**	**17.00 W**

TABLE XII
SUMMARY OF THE DISTRIBUTION OF LOSSES IN THE OPTIMIZED DESIGN

Contribution	100% Load	50% Load	20% Load
Bias	0.96 W	0.96 W	0.96 W
Fan	3.45 W	1.55 W	0.60 W
Tr. Core	2.37 W	2.37 W	2.37 W
Tr. Conduction	13.04 W	3.61 W	0.96 W
Lr Core	0.30 W	0.15 W	0.05 W
Lr Conduction	0.64 W	0.17 W	0.04 W
Lo Core	0.39 W	0.39 W	0.39 W
Lo Conduction	6.18 W	1.43 W	0.23 W
Bridge Conduction	10.05 W	2.51 W	0.53 W
Bridge Switching	0.49 W	0.42 W	0.42 W
Bridge Driving	0.22 W	0.22 W	0.22 W
SRs Conduction	5.19 W	1.28 W	0.25 W
SRs Switching	3.26 W	2.10 W	1.40 W
SRs Driving	1.17 W	1.17 W	1.17 W
Clamping Diodes	1.47 W	1.67 W	1.77 W
Capacitors	3.65 W	1.25 W	0.58 W
PCB	12.33 W	3.09 W	0.50 W
Total	**65.16 W**	**24.34 W**	**12.44 W**

Table 13 details the difference between the components losses of the reference design and the improved design. Although in some of the losses contribution the losses actually have increased, the overall result is a general improvement in all points of load. In Table 13 it can be observed that the main improvements come from the transformer conduction and the SRs (conduction and switching), the output inductor (conduction and core), L_r conduction, the fan and the HV bridge (conduction and switching).

TABLE XIII
SUMMARY OF DIFFERENCE OF LOSSES BETWEEN THE OPTIMIZED AND THE REFERENCE DESIGNS

Contribution	100% Load. Difference	50% Load. Difference	20% Load. Difference
Bias	0 W	0 W	0 W
Fan	0 W	**-1.9 W**	**-2.85 W**
Tr. Core	1.84 W	1.09 W	0.78 W
Tr. Conduction	**-16.94 W**	**-2.92 W**	**-0.11 W**
Lr Core	0.12 W	0.07 W	0.03 W
Lr Conduction	**-0.56 W**	**-0.09 W**	0 W
Lo Core	**-0.19 W**	**-0.19 W**	**-0.19 W**
Lo Conduction	**-3.47 W**	**-0.74 W**	**-0.1 W**
Bridge Conduction	**-1.19 W**	0.22 W	0.2 W
Bridge Switching	0.07 W	0 W	**-0.87 W**
Bridge Driving	0.04 W	0.04 W	0.04 W
SRs Conduction	**-5.1 W**	**-1.35 W**	**-0.23 W**
SRs Switching	**-1.07 W**	**-1.6 W**	**-1.95 W**
SRs Driving	0.28 W	0.28 W	0.28 W
Clamping Diodes	0.57 W	0.37 W	0.27 W
Capacitors	0.37 W	0.12 W	0.05 W
PCB	2.01 W	0.51 W	0.09 W
Total	**-23.22 W**	**-6.09 W**	**-4.56 W**

D. WAVEFORMS REFERENCE DESIGN

The steady state operation of the reference design was tested and summarized in the captures in this section.

It was already analyzed in the previous sections the different energy available for the ZVS transitions of the leading and the lagging leg of the primary side bridge. Figure 23 shows captures of the leading leg drain and gate voltages at different loads. Whereas Figure 24 shows captures of the lagging leg drain and gate voltage also operating at different loads.

The leading leg operates in full ZVS in all load range of the converter, which can be observed in the gate voltages in Figure 23, where the drain voltage is zero prior to the gate voltage rising and no Miller Plateau can be observed. The full bridge is driven with an isolated pulse transformer which outputs $\pm V_{drive}$. Only during the dead time the gate voltage is zero. Certain C_{gd} feedback can be observed at higher loads where the *dv/dt* of the V_{DS} transition increases because of the higher starting currents involved in the resonant transition.

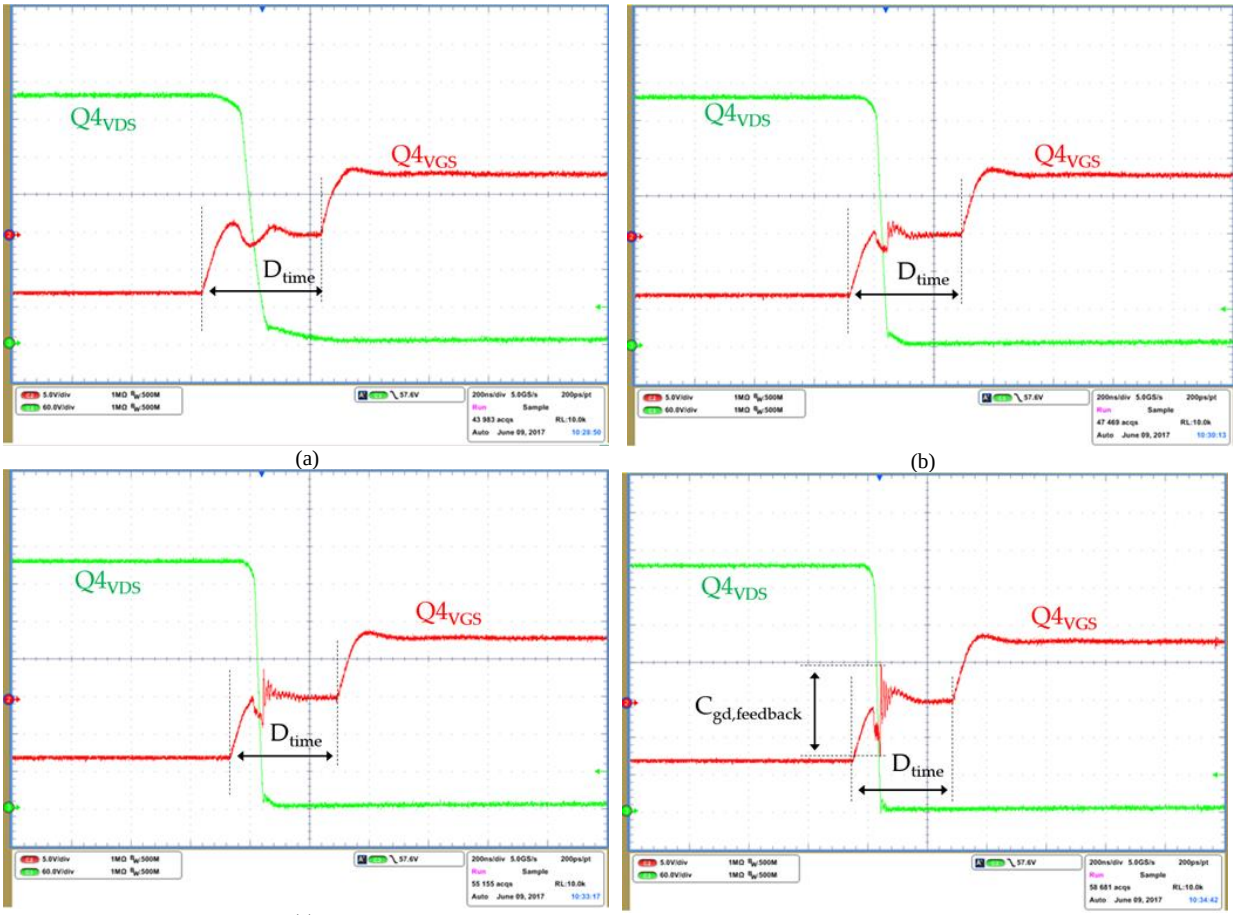
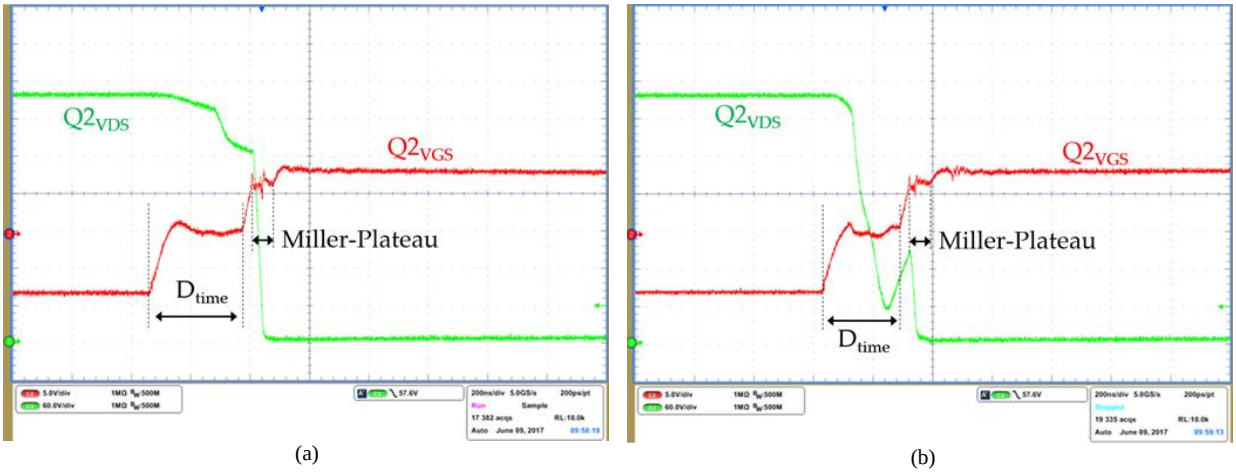
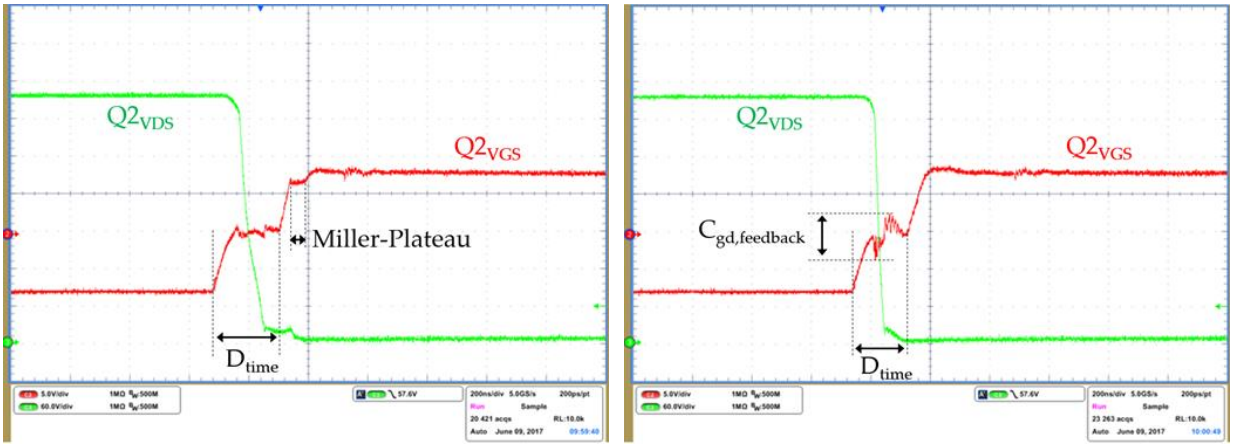


Figure 23. Turn-on switching waveforms of the low side switch of the leading leg at different loads ($I_{o,avg}$). (a) 25 A. (b) 60 A. (c) 75 A. (d) 117 A.

The lagging leg achieves full ZVS only at full load (Figure 24). The main reasons for the lack of energy for the ZVS transitions are the small external resonant inductance and the position of the clamping diodes. The reference design mounts the clamping diodes in the leading leg. The clamping diodes in the leading leg reduces circulating currents and conduction losses all along the load range of the converter. However it also reduces the current through L_r at the end of the freewheeling stage, which directly impacts the energy available for ZVS.

The lack of energy for the ZVS transitions of the leading leg increases the switching losses. Moreover, because of the non-linearity of the output capacitance of super-junction MOSFETs, the optimum dead time varies non-linearly with the load. The non-linear variation of the dead times makes it difficult to optimize the control with may further increase the switching losses. Further aggravated by the variation of capacitances and inductances between the components in different converters.



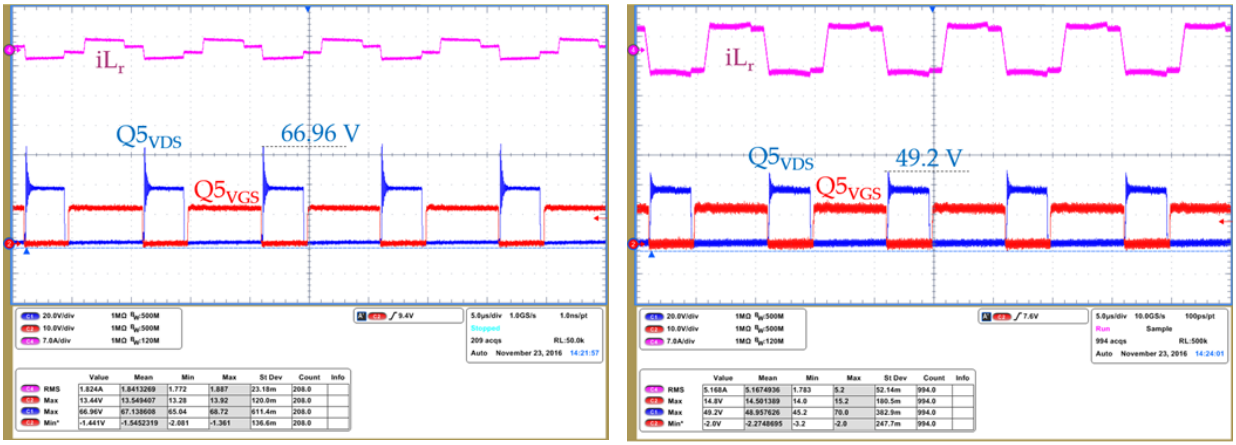


(c) (d)

Figure 24. Turn-on switching waveforms of the low side switch of the lagging leg at different loads ($I_{o,avg}$). (a) 25 A of load; (b) 60 A of load; (c) 75 A of load; (d) 117 A of load (100 %).

Moreover, the fast *dv/dt* induced by the partial hard switching of the leading leg impacts on the secondary side overshoot at light loads. It can be observed in Figure 25 how the overshoot of the SRs is higher at light load in the former converter, exceeding the 80 % rating of the 80 V breakdown limit.

These results corroborate the drawbacks of the clamping diodes on the leading leg position, and support the recommendation of placing them in the lagging leg, instead.



(a) (b)

Figure 25. SRs drain voltage overshoot: (a) Working at 140 W of output power (10 % of load); (b) Working at 1400 W of output power (full load).

Figure 26 shows in more detail the secondary side overshoot of the SRs in steady state and the effect on the primary side current of the clamping diodes on the leading leg position.

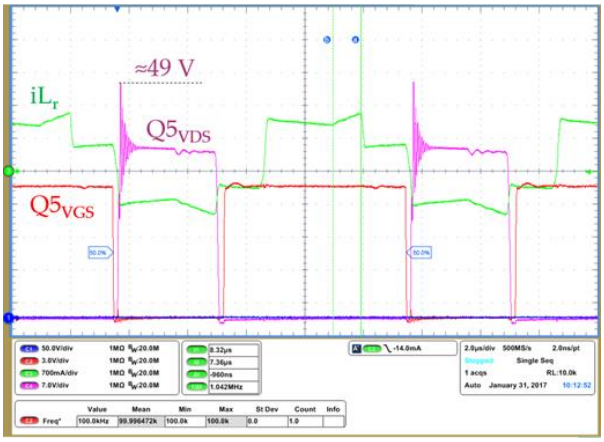
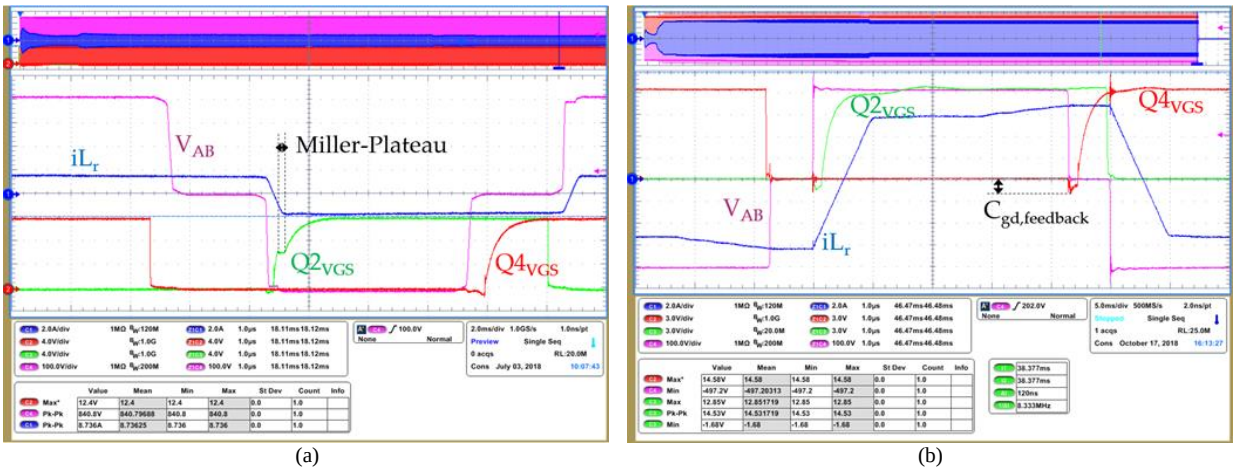


Figure 26. Detail on the SRs overshoot and the primary side current with the clamping diodes on the leading leg position.

E. WAVEFORMS OF NEW OPTIMIZED DESIGN

The leading leg of the new design achieves full ZVS above 20 % of the load (Figure 27). Moreover, it achieves nearly full ZVS down to no load. The lagging leg, like in the reference design achieves also full ZVS along all load range. However, the C_{gd} feedback effects on the gate voltage at full load are less noticeable thanks to the improved layout and driving scheme.



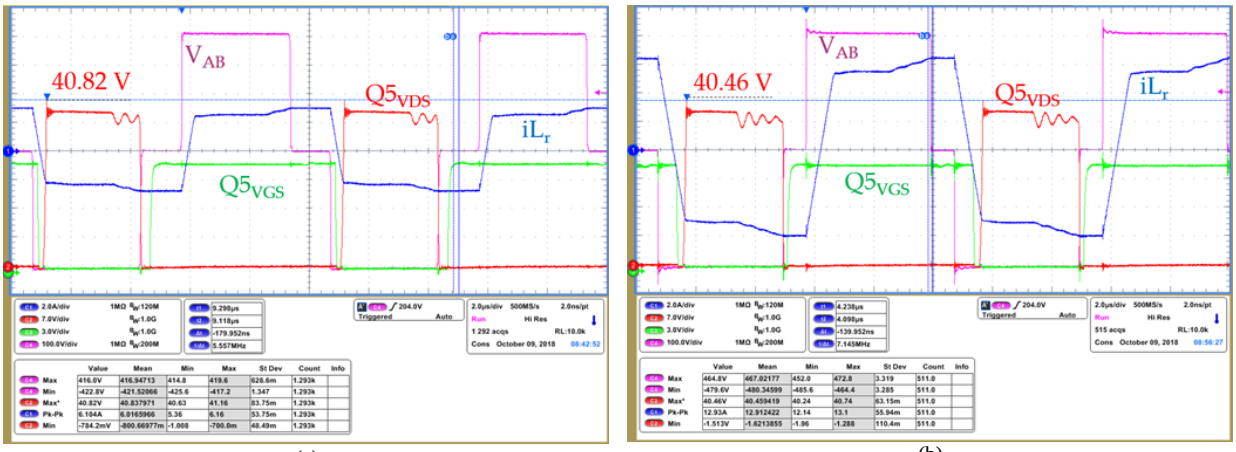
(a) (b)

Figure 27. Primary side HV MOSFETs ZVS: (a) ZVS at 20 A of load; (b) ZVS at full load.

The overshoot on the secondary side rectifiers is very much improved in all load range, and well within the 80 % rated limit of the 60 V breakdown voltage (Figure 28).

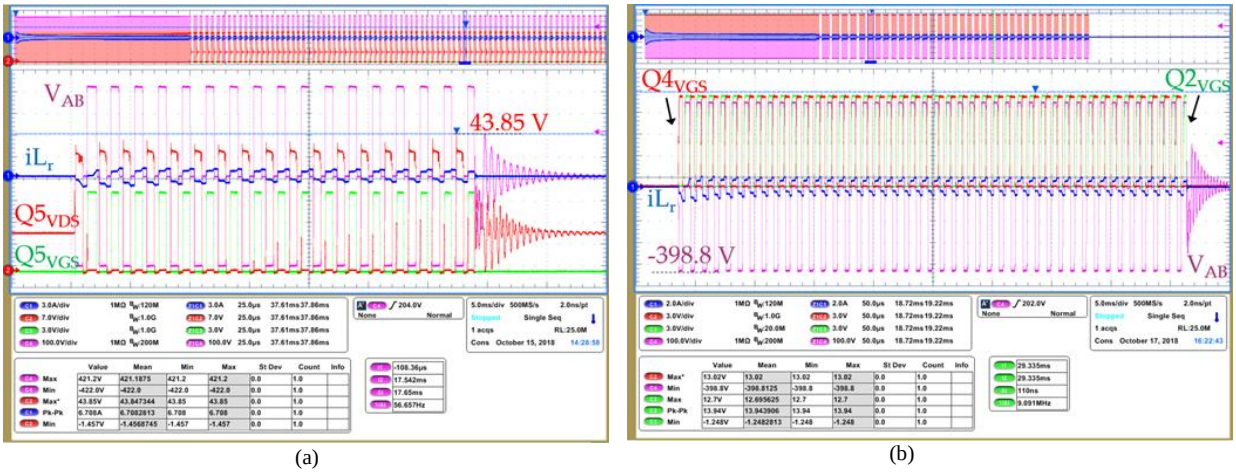
Near no load, both the reference design and the optimized design, implement burst mode operation. The burst mode operation enables soft switching at no load operation. Figure 29 shows captures of the drain voltage overshoot on the primary side devices and the secondary side devices of the optimized converter. Also in burst mode operation the drain and gate voltages remain well within their rated limits.

Load jumps are usually considered critic for the PSFB topology. Figure 30 shows a capture of dynamic load jumps where the reader can observe that the drain voltage of the primary and secondary switches is well within the limits.



(a) (b)

Figure 28. SRs drain voltage overshoot: (a) Working at 140 W of output power (10 % of load); (b) Working at 1400 W of output power (full load).



(a) (b)

Figure 29. SRs and HV bridge MOSFETs overshoot during BURST: (a) SRs drain voltage overshoot; (b) HV bridge overshoot.

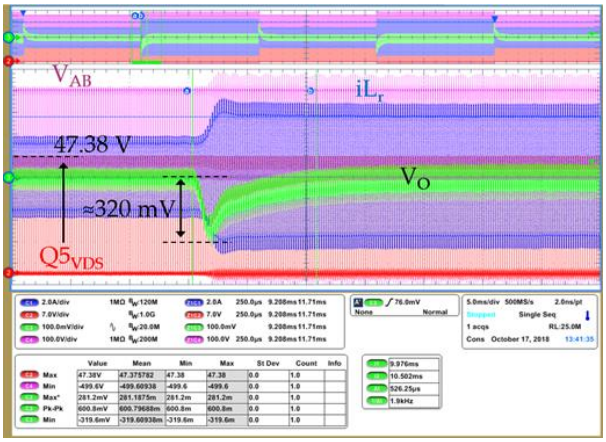


Figure 30. SRs overshoot during load jump

VI. CONCLUSIONS

Since the server power supplies consume an enormous amount of power, the most critical issue is high efficiency. In order to implement a high efficiency and high power density server PSU, PSFB converter with SRs MOSFETs, external resonant inductor and clamping diodes is the perfect topology for the DCDC stage. Its main characteristic is the wide ZVS operation from mid to full load, nearly suppressing switching losses. Moreover, the constant switching frequency allows a simple control and EMI design. One of the major advantages of PSFB over other resonant soft-switching topologies is the comparatively lower *rms* currents through the converter thanks to the output filter inductance. However, hold-up time regulation requirement makes PSFB converter not to be operated with its maximum effective duty in nominal conditions and causes long freewheeling period.

The design of a high efficiency PSFB converter is a complex problem with many degrees of freedom which requires of a sufficiently accurate modeling of the losses of the converter and of efficient design criteria. In this work a losses model of the converter has been proposed as well as design guidelines for the efficiency optimization of the PSFB converter. The losses model and the criteria have been tested with the redesign of an existing reference PSFB DCDC converter for server applications that achieved 95.85 % of efficiency at 50 % of load. The new converter was designed following the same specifications as the reference: 1400 W of maximum power; 400 V nominal input voltage; hold-up regulation down to 360 V input voltage; and 12 V output. The new optimized prototype of PSFB converter was built and tested achieving a peak efficiency of 96.68 % at 50 % of load, notably exceeding the performance of the reference converter in all load range and operating conditions.

The main differences between both designs are related to the magnetics construction, with an improved balance of core and conduction losses along the load range of the converter. Furthermore, the transformer turns ratio and the dimensioning of the external resonant inductance enabled lower $R_{ds,on}$ in the primary side HV devices and lower voltage class (and consequently also lower $R_{ds,on}$) in the secondary side LV devices. Moreover, all semiconductors in the new optimized design are SMD, which together with the high efficiency at full load enables a power density in the range of 3.70 W/cm³ (60.78 W/in³).

In summary, the key of an efficient and reliable DCDC PSFB converter in this power range and output voltage is in the magnetics design, more specifically the transformer and the external resonant inductance. This demonstrates that the PSFB converter is a relatively simple and efficient topology for DCDC converter applications at the level of fully resonant topologies.

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CHAPTER 10. FOURTH PUBLICATION

Non-linear capacitance of Si SJ MOSFETs in resonant Zero Voltage Switching applications

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***Abstract*— The parasitic capacitances of modern Si SJ MOSFETs are characterized by their non-linearity. At high voltages the total stored energy $E_{oss}(V_{DC})$ in the output capacitance $C_{oss}(v)$ differs substantially from the energy in an equivalent linear capacitor $C_{oss(tr)}$ storing the same amount of charge. That difference requires the definition of an additional equivalent linear capacitor $C_{oss(er)}$ storing the same amount of energy at a specific voltage. However, the parasitic capacitances of current SiC and GaN devices have a more linear distribution of charge along the voltage. Moreover, the equivalent $C_{oss(tr)}$ and $C_{oss(er)}$ of SiC and GaN devices are smaller than the ones of a Si device with a similar $R_{ds,on}$. In this work, the impact of the non-linear distribution of charge in the performance and the design of resonant ZVS converters is analyzed. A Si SJ device is compared to a SiC device of equivalent $C_{oss(tr)}$, and to a GaN device of equivalent $C_{oss(er)}$, in single device topologies and half-bridge based topologies, in full ZVS and in partial or full hard-switching. A prototype of 3300 W resonant LLC DCDC converter, with nominal 400 V input to 52 V output, was designed and built to demonstrate the validity of the analysis.**

***Index Terms*— Hard-switching, non-linear capacitance, resonant converter, Wide Band Gap, Zero Voltage Switching.**

NOMENCLATURE

C_{ds}	Drain to source capacitance.
C_{gd}	Gate to drain capacitance.
C_{gs}	Gate to source capacitance.
C_{iss}	Input capacitance. C_{gs} plus C_{gd}.
$C_{oss,1}$	Output capacitance of the device turning-on in a half-bridge.
$C_{oss,2}$	Output capacitance of the device turning-off in a half-bridge.
$C_{oss(er)}$	Effective output capacitance, energy related.
$C_{oss(tr)}$	Effective output capacitance, time related.
C_{oss}	Output capacitance. C_{ds} plus C_{gd}.
E_{ind}	Energy stored in the series inductor.
$E_{ind,1}$	Required stored energy in single device topologies.
$E_{ind,2}$	Required stored energy in single device topologies starting at higher voltage than V_{DC}.
$E_{ind,3}$	Required stored energy in single device topologies starting at voltage lower than V_{DC}.
$E_{ind,4}$	Required stored energy for charging $C_{oss,2}$.
$E_{ind,5}$	Total required stored energy in half-bridge topologies.
$E_{ind,linr,1}$	Required stored energy in single device topologies for linear capacitances.
$E_{ind,linr,2}$	Required stored energy in single device topologies starting at voltage higher than V_{DC} for linear capacitances.

$E_{ind,linr,3}$ Required stored energy in single device topologies starting at voltage lower than V_{DC} for linear capacitances.
E_{oss} Stored energy in the C_{oss}.
$E_{oss,linr}$ Stored energy in a linear C_{oss}.
i_{ch} Channel current.
i_d Drain current.
i_{dg} Drain to gate current.
i_{ds} Drain to source current.
L_r Series resonant inductor.
Q_{gd} Stored charge in C_{gd}.
Q_{oss} Stored charge in C_{oss}.
$V_{gs,max}$ Maximum induced gate to source voltage by the Miller feedback effect.
$V_{G,off}$ Turn-off driving voltage.
V_{Miller} Miller-Plateau voltage.
$R_{ds,on}$ Drain to source on-state resistance.
R_g Integrated gate resistance.
$R_{g,off}$ Turn-off gate resistance.
R_s Series resistance.
V_{DC} Nominal voltage of the converter's supply.
V_{ds} Drain to source voltage.
V_{end} Final supply voltage.
V_{start} Initial supply voltage.
V_{supply} Converter's supply voltage.
V_{th} Gate threshold voltage.
$\Delta E_{loss,tot}$ Total energy loss in the hard-switched turn-on transition of a half-bridge.
$\Delta E_{loss,t,linr}$ Total energy loss in the hard-switched turn-on transition of a half-bridge for linear capacitances.
$\Delta E_{loss,2}$ Energy lost in the hard-switched charge of $C_{oss,2}$.
$\Delta E_{loss,2,linr}$ Energy lost in the hard-switched charge of $C_{oss,2}$ for linear capacitances.
$\Delta E_{supply,2}$ Supplied energy for the hard-switched charge of $C_{oss,2}$.
$\Delta E_{supply,2,linr}$ Supplied energy during the hard-switched. charge of $C_{oss,2}$ for linear capacitances.
ΔQ Variation of stored charge.
ΔV_{supply} Variation in the supply voltage.

I. INTRODUCTION

The development of Switched Mode Power Supplies (SMPS) continuously moves towards improvements in efficiency, volume and cost, which can be observed in the trend of high efficiency standards, like the Climate-Savers-Computing Initiative (CSCI) [1] or the 80 PLUS qualification program [2], with increasing requirements extending also to light load operation. The efficiency, volume and cost are parameters of performance closely interdependent in the design of SMPS [3]-[4]. The improvements in one of the parameters often implies a negative impact in one or, often, several of the other ones. It is only through new design paradigms or technology breakthroughs that it is possible to push further the limits in terms of efficiency, volume, cost or the overall performance of power converters.

One of the key design paradigms in modern high-efficiency SMPS is the reduction or the elimination of the switching losses in the power semiconductors devices, which has limited traditionally the maximum switching frequencies and, consequently, the maximum power density of the converter. The switching losses can be reduced limiting the overlap of current and voltage during the switching transitions by one of these means: turning the switch at Zero Voltage (ZVS), at Zero Current (ZCS) or a combination of both. The ZVS turn-on of High Voltage (HV) devices is especially beneficial because the high amount of energy stored in the parasitic capacitances would be otherwise lost [5]-[7]. The ZVS can be achieved discharging and charging the parasitic capacitances in a lossless manner prior to the switching transition.

The charge and discharge of a capacitor can be near lossless when the energy is transferred from an inductor and such transfer is not resistively limited. This can be considered true when the charge and discharge transient is underdamped: the RC time constant of the circuit is several orders of magnitude smaller than the time constant of the LC resonance [8]-[9]. This property is the key attribute in the so-called resonant and quasi-resonant converters, all of which comprise at least one inductor, which charges and discharges the parasitic capacitances of the switches in a resonant manner. Apparently, in some cases a variable series resistance within the output capacitance of power semiconductor devices may limit resistively its charge and discharge causing additional losses that will not be analyzed in this work [10].

Commonly used resonant converter topologies may comprise one single switching device or several of them, stacked in pairs and conforming one or several building blocks, so-called half bridges. Examples of single switch resonant or quasi-resonant topologies are the fly-back and its variants [11], and the Critical Conduction Mode (CrCM) [12] boost converter. For high-power applications are common two switch topologies, like the Transition Conduction Mode (TCM) [13] boost converter and the half-bridge LLC [14], and four switch topologies, like the Phase Shift Full Bridge (PSFB) [15]-[16], the Dual Active Bridge (DAB) [17] and the full-bridge LLC. The general analysis in this work will be applied to the two basic scenarios, a single device and a half-bridge (or stacked devices), which can be conveniently extended to any of the above-mentioned topology examples.

Another key design paradigm in modern high-efficiency SMPS is the reduction of switching losses by the improvement of the characteristics of the switching device itself. Silicon (Si) based power switching devices have continuously improved their Figure Of Merit (FOM) becoming closer and closer to the theoretical limit of the material itself [18]-[19]. Frequently, the improvement of the FOM implies certain side effects on the device characteristics, e.g. the distribution of charge in the parasitic capacitance along the blocking voltage becomes highly non-linear (Fig. 1). The non-linear distribution of charge in the output capacitance of modern Super Junction (SJ) MOSFETs allows the total stored energy to be much less of what would be stored in an equivalent linear capacitor with the same amount of charge $C_{oss(tr)}$ (Fig. 2). This divergence requires the definition of an additional energy related equivalent linear capacitor $C_{oss(er)}$ (Fig. 3), which would store the same amount of energy than the non-linear output capacitance of the semiconductor switch. The equivalent $C_{oss(tr)}$ and $C_{oss(er)}$ (1-4) have been previously defined in the literature [20] and are commonly available in the datasheet of commercial devices.

$$Q_{oss}(V_{DC}) = \int_0^{V_{DC}} C_{oss}(v)\,dv \tag{1}$$

$$C_{oss(tr)}(V_{DC}) = \frac{Q_{oss}(V_{DC})}{V_{DC}} \tag{2}$$

$$E_{oss}(V_{DC}) = \int_0^{Q_{oss}(V_{DC})} v\,dq = \int_0^{V_{DC}} v \cdot C_{oss}(v)\,dv \tag{3}$$

$$C_{oss(er)}(V_{DC}) = \frac{2E_{oss}(V_{DC})}{{V_{DC}}^2} \tag{4}$$

Moreover, the commercial availability of switching devices made of Wide Band Gap (WBG) semiconductor materials promises to bring a considerable leap in performance in power converters [21]-[23]. Currently, the most promising technologies are Silicon Carbide (SiC) MOSFETs and Gallium Nitride (GaN) HEMTs. The devices made of WBG semiconductors can have parasitic capacitances several orders of magnitude smaller than a Si device with similar $R_{ds,on}$. Furthermore, the distribution of charge along the voltage of currently available WBG devices is more linear than the distribution of charge in Si devices (Fig 1). It can be observed in Fig. 4 and Fig. 5 that the equivalent $C_{oss(tr)}$ and $C_{oss(er)}$ for SiC and GaN technologies do not diverge as much as in the Si example.

In this work the impact on the performance and design of resonant converters originated by the absolute stored charge within the parasitic output capacitance and its distribution along the voltage excursion is analyzed. This works aims to bring further insights in the behavior of the power switches' non-linear capacitances in resonant converters, to extend and complete the analysis presented in [5] and [20]. Moreover, this works includes the analysis of single device and half-bridge device topologies.

For the sake of a meaningful comparison of their output capacitances, a Si SJ MOSFET (IPP60R170CFD7) [24] is compared to a SiC MOSFET (IMZA65R027M1H) [25] with nearly equal total stored charge, and compared to a GaN HEMT (IGT60R070D1) [26] of nearly equal total stored energy. A summary of the main characteristics of the devices is listed in Table I. For the sake of simplicity, only the parasitic capacitances of the device itself will be considered in the following analysis: the effects of the packaging, the heat-sink mounting or the PCB layout will be omitted. In the following, the compared devices will be referred simply as Si, SiC and GaN unless otherwise noted.

The rest of this work is organized as follows. In Section II, the required initial stored energy in the resonant inductor to achieve full ZVS in single and half-bridge based topologies is analyzed. In Section III, the impact on the losses of partial or full hard switching in single and half bridge based topologies is analyzed. In Section IV, the impact of the parasitic capacitance characteristics on the *dv/dt* during hard-switched turn-off and the impact on the losses of purposely decreasing the maximum *dv/dt* is analyzed. In Section V, the analysis is verified experimentally on a 3.3 kW half-bridge LLC DCDC converter prototype with nominal 400 V input and wide range output: 43.5 V – 59.5 V. Finally, in Section V the conclusions of this work are summarized.

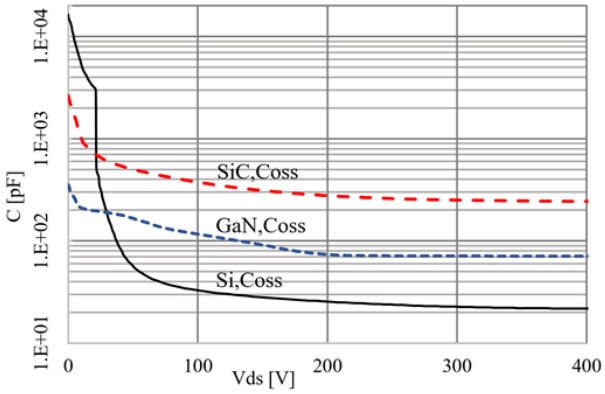

Fig. 1. IPP60R170CFD7 (Si), IMZA65R027M1H (SiC) and IGT60R070D1 (GaN) typical output capacitances C_{oss}. Data extracted from the datasheets of the devices.

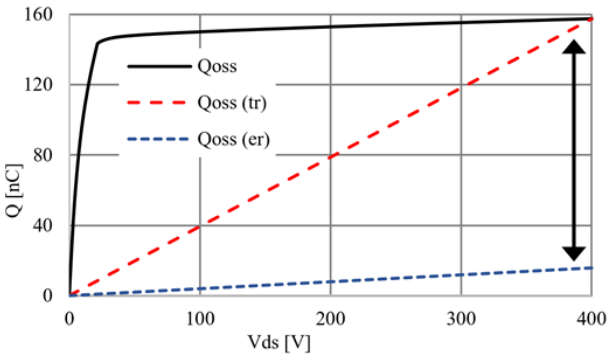

Fig. 2. Si typical stored charge in its C_{oss} and the stored charge in an equivalent $C_{oss(tr)}$ and an equivalent $C_{oss(er)}$.

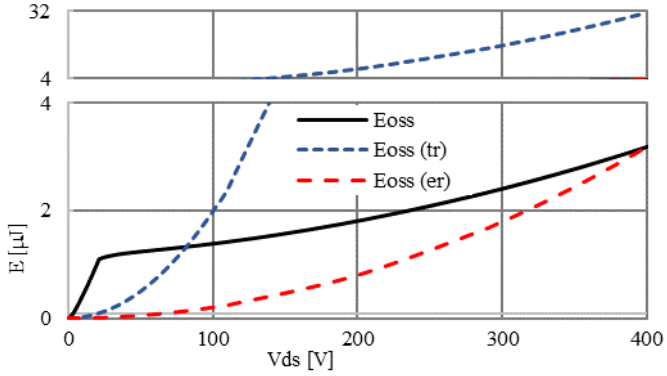

Fig. 3. Si typical stored energy in C_{oss} and the stored energy in an equivalent $C_{oss(tr)}$ and in an equivalent $C_{oss(er)}$.

TABLE I
SUMMARY OF DEVICE CHARACTERISTICS

	IPP60R170CFD7	IMZA65R027M1H	IGT60R070D1
$R_{DS,on}$	144 mΩ @ 25 °C	27 mΩ @ 25 °C	55 mΩ @ 25 °C
Q_{oss}	157 nC @ 400 V	147 nC @ 400 V	40.5 nC @ 400 V
E_{oss}	3.18 µJ @ 400 V	29.46 µJ @ 400 V	8.10 µJ @ 400 V
Q_{gd}	3.18 nC @ 400 V	12.2 nC @ 400 V	2.08 nC @ 400 V
C_{gs}	1208 pF	2114 pF	380 pF
R_g	10.9 Ω	3 Ω	0.78 Ω
V_{th}	4 V	4.5 V	1.2 V

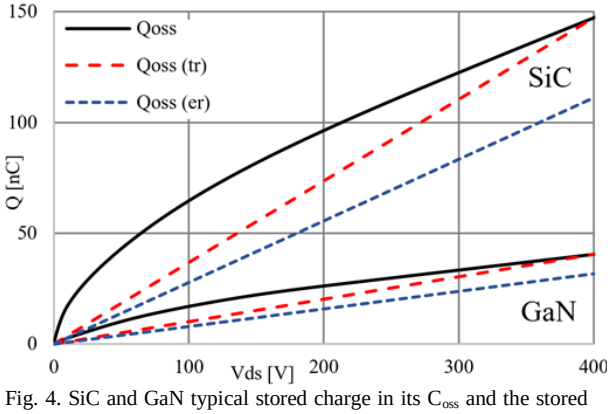

Fig. 4. SiC and GaN typical stored charge in its C_{oss} and the stored charge in an equivalent $C_{oss(tr)}$ and an equivalent $C_{oss(er)}$.

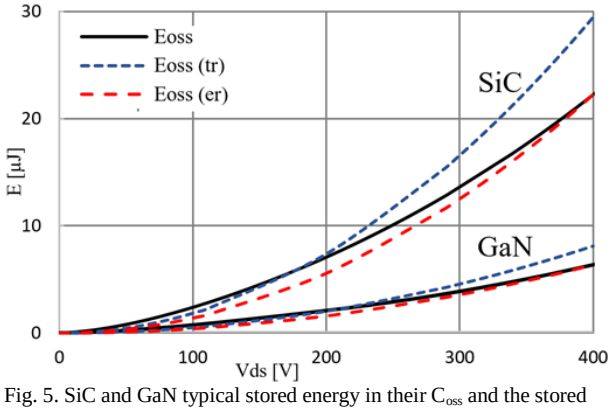

Fig. 5. SiC and GaN typical stored energy in their C_{oss} and the stored energy in an equivalent $C_{oss(tr)}$ and in an equivalent $C_{oss(er)}$.

II. ANALYSIS OF ZERO VOLTAGE SWITCHING ENERGIES

A. *SINGLE DEVICE TOPOLOGIES*

For the sake of generality in the analysis, a single device resonant converter during the switching transition is represented by the simplified equivalent circuit in Fig. 6. In this simplified circuit there is a capacitor C_1 that stands for the equivalent output capacitance C_{oss} of the power switch. The inductor L_r stands for a discrete auxiliary

resonant inductance or other equivalent inductances in the circuit (e.g. the leakage of a transformer), which provides the initial energy for the ZVS transition. An equivalent series resistor R_s stands for all of the series resistances along the charging and discharging path.

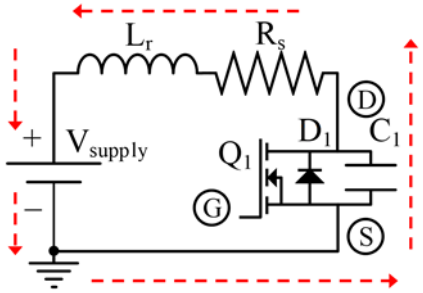

Fig. 6. Simplified circuit for the analysis of the resonant discharge of the output capacitance of the power switch in a single device topology.

In its initial state the switch is off or in its blocking state, and the output capacitor C_{oss} is charged-up to a starting voltage V_{DC} equal to the voltage in V_{supply}. Because the drain to source voltage V_{ds} equals to the supply voltage V_{DC}, the circuit is stable and would remain in this state indefinitely unless there is a certain initial energy E_{ind} in the inductor that forces the output charge Q_{oss} out of C_{oss} and into V_{supply}. Thanks to that initial energy (E_{ind}) the capacitor C_{oss} would be effectively discharged and with zero stored energy (E_{oss}) at the end of the transition, enabling a ZVS turn-on. Like a transfer between two capacitors in series, the total amount of charge that is transferred corresponds to the initial amount of charge in the smallest of the capacitors, which is C_{oss} in this scenario. Because C_{oss} is a non-linear capacitor the total amount of charge in C_{oss} when it is charged up to a voltage V_{DC} is referred as $Q_{oss}(V_{DC})$.

Although less lossy than a purely resistively limited charging, the resonant charge and discharge of C_{oss} still causes conductive losses due to the required circulating currents passing through the circuit and its equivalent series resistance R_s. Notice that the related conductive losses would be proportional to the square of the current passing through the circuit, while the required ZVS current is proportional to the square root of E_{ind} and inversely proportional to the square root of the resonant inductor L_r.

Continuing with the simile of the two capacitors in series, assuming V_{supply} to be a linear capacitor, the amount of energy that is stored in it because of the charge ΔQ that has been transferred from C_{oss}, can be calculated with (5). Because we can safely assume the capacitance of V_{supply} to be much bigger than the equivalent capacitance of C_{oss}, we can neglect the variation of voltage ΔV_{supply} in equation (5) and simplify the expression into (6).

$$\Delta E_{supply} = \Delta Q \cdot \frac{V_{end}+V_{start}}{2} = \Delta Q \cdot \frac{(V_{DC}+\Delta V_{supply})+V_{DC}}{2} \tag{5}$$

$$\Delta E_{supply} = Q_{oss}(V_{DC}) \cdot \frac{2 \cdot V_{DC}}{2} = Q_{oss}(V_{DC}) \cdot V_{DC} \tag{6}$$

The energy extracted from C_{oss} during its discharge corresponds to the initial energy that was stored in it at the supply voltage V_{DC}, which is referred as $E_{oss}(V_{DC})$. Because C_{oss} is a non-linear capacitor, $E_{oss}(V_{DC})$ has to be calculated with equation (3). The energy extracted from C_{oss} is not lost during the transition, but transferred to and later stored in V_{supply}. The rest of the energy that is stored in V_{supply} has to be provided by the resonant inductor, and corresponds to the minimum initial energy required at the start of the transition for achieving full ZVS (7-8).

$$E_{ind,1} = \Delta E_{supply} - E_{oss}(V_{DC}) \tag{7}$$

$$E_{ind,1} = Q_{oss}(V_{DC}) \cdot V_{DC} - E_{oss}(V_{DC}) \tag{8}$$

In the case of C_{oss} being a linear capacitor, the energy stored in it can be calculated with (9) and the previous formula can be simplified into (10). In this case, the required energy results to be equal to the initial energy stored in C_{oss}.

$$E_{oss,linr}(V_{DC}) = Q_{oss}(V_{DC}) \cdot \frac{V_{DC}}{2} \tag{9}$$

$$E_{ind,linr,1} = Q_{oss}(V_{DC}) \cdot \frac{V_{DC}}{2} \tag{10}$$

The clear consequence of this analysis is that in single device resonant topologies the most relevant parameter is the total stored charge in the output capacitance of the device. Moreover, the bigger the divergence between the equivalent charge related capacitance $C_{oss(tr)}$ and energy related capacitances $C_{oss(er)}$ the higher the required initial energy in the inductor (11). Si SJ MOSFETs have the biggest divergence between the values among the three compared devices. Consequently, while the Si and the SiC devices have very similar $C_{oss(tr)}$ the initial required energy is nearly twice as much for the Si device due to the much smaller $E_{oss}(V_{DC})$ of the Si device in comparison

to the SiC device. In the case of GaN, because its output charge $Q_{oss}(V_{DC})$ is much smaller, the required initial energy is also much smaller.

$$E_{oss}(V_{DC}) < E_{oss,linr}(V_{DC}) \xrightarrow{\text{yields}} E_{ind,1} > E_{ind,linr,1} \tag{11}$$

The previous analysis is verified by the calculation of the required initial energies for achieving ZVS in the three example devices (Si, SiC and GaN), and the simulation of the energy distribution in time during the transition, represented in Fig. 7 and Fig. 8. The drain to source voltage along time during the transition has been represented in Fig. 9, where it can be observed that the transition time also depends mostly on the total stored charge $Q_{oss}(V_{DC})$. Table II summarizes the results of the simulations, which has been represented in the previous figures.

TABLE II
SINGLE DEVICE SUMMARY

	IPP60R170CFD7	IMZA65R027M1H	IGT60R070D1
V_{DC}	400 V	400 V	400 V
$E_{ind,1}$	62.95 µJ	37.05 µJ	9.97 µJ
E_{supply}	66.13 µJ	59.29 µJ	16.32 µJ
Time	28.90 ns	28.83 ns	15.24 ns

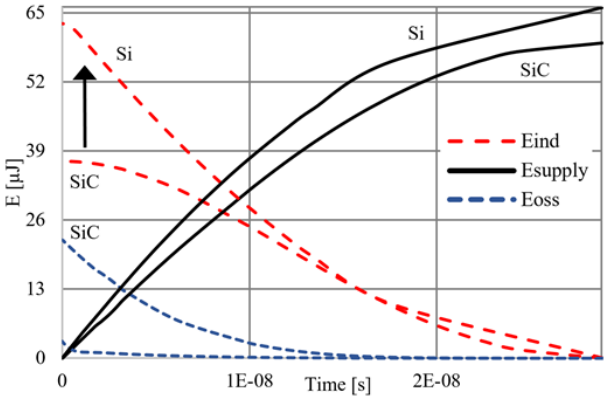

Fig. 7. Si and SiC typical distribution of energies during the resonant discharge of the C_{oss}.

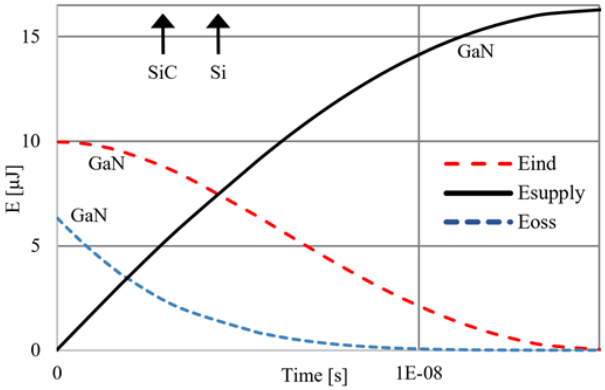

Fig. 8. GaN typical distribution of energies during the resonant discharge of the C_{oss}.

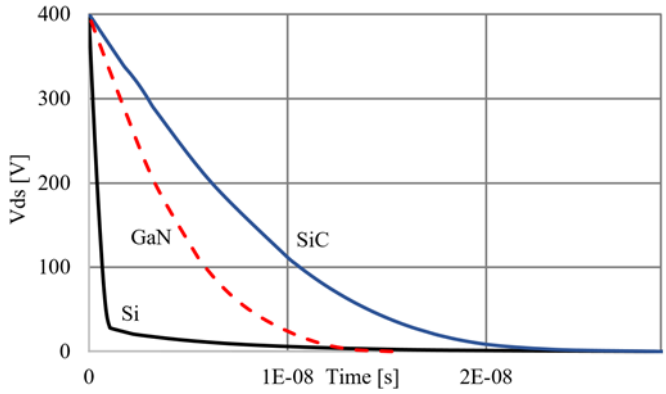

Fig. 9. Si, SiC and GaN typical V_{ds} voltage during the resonant discharge of C_{oss}.

B. SINGLE DEVICE AT A HIGHER VOLTAGE

In certain topologies, the voltage stored in C_{oss} before the discharge transition could be higher than the voltage in the supply V_{DC}. Since the initial voltage in C_{oss} is higher than the voltage in V_{supply}, both capacitors will tend to balance naturally. If we assume the equivalent capacitance of V_{supply} to be much bigger than the equivalent capacitance of C_{oss}, the balance voltage will be, for all purposes, equal to V_{DC}.

When the voltages become equal, the total amount of charge that has been transferred from C_{oss} into V_{supply} can be calculated with (12) and the energy that has been consequently stored in V_{supply} can be estimated with equation (13). The energy that has been extracted from C_{oss} can be calculated with (14). Because the ΔQ was stored in C_{oss} at a higher voltage than V_{DC}, the initial energy in C_{oss} was always necessarily higher than the energy that has been transferred into V_{supply}. The rest of the energy would have been stored in the resonant inductor (15-16).

$$\Delta Q = Q_{oss}(V_{DC} + \Delta V) - Q_{oss}(V_{DC}) \tag{12}$$

$$\Delta E_{supply} = \Delta Q \cdot V_{DC} \tag{13}$$

$$\Delta E_{oss} = E_{oss}(V_{DC} + \Delta V) - E_{oss}(V_{DC}) \quad (14)$$

$$\Delta E_{ind} = \Delta E_{oss} - \Delta E_{supply} \quad (15)$$

$$\Delta E_{oss} > \Delta E_{supply} \xrightarrow{\text{yields}} \Delta E_{ind} > 0 \quad (16)$$

After both C_{oss} and V_{supply} have reached the same voltage, V_{DC}, the scenario becomes equal to the one analyzed in the previous section for single device topologies, where the initial energy required in the inductor is equal to $E_{ind,1}$ (8). Therefore, the initial energy required at the start of the transition would be $E_{ind,1}$ minus the additional ΔE_{ind} that has already been stored in the inductor during the natural balance of the capacitor voltage (17-19).

$$E_{ind,2} = E_{ind,1} - \Delta E_{ind} \quad (17)$$

$$E_{ind,2} = Q_{oss}(V_{DC}) \cdot V_{DC} + \Delta Q \cdot V_{DC} - E_{oss}(V_{DC} + \Delta V) \quad (18)$$

$$E_{ind,2} = Q_{oss}(V_{DC} + \Delta V) \cdot V_{DC} - E_{oss}(V_{DC} + \Delta V) \quad (19)$$

Because of this, the higher the initial difference between the voltages the lower the required initial stored energy in the resonant inductor. The turning point is the one where the initial required energy in the inductor $E_{ind,2}$ equals zero, which occurs when ΔE_{ind} is greater than or equal to $E_{ind,1}$ (20).

$$E_{ind,2} = 0 \xrightarrow{\text{yields}} Q_{oss}(V_{DC} + \Delta V) \cdot V_{DC} = E_{oss}(V_{DC} + \Delta V) \quad (20)$$

For a linear capacitor, the previous expression (20) can be simplified into the well-known condition that the starting voltage should be at least twice of the supply voltage V_{DC} (21-23).

$$E_{oss,linr,2}(V_{DC} + \Delta V) = Q_{oss}(V_{DC} + \Delta V) \cdot \frac{(V_{DC}+\Delta V)}{2} \quad (21)$$

$$Q_{oss}(V_{DC} + \Delta V) \cdot V_{DC} = Q_{oss}(V_{DC} + \Delta V) \cdot \frac{(V_{DC}+\Delta V)}{2} \quad (22)$$

$$V_{DC} = \frac{(V_{DC}+\Delta V)}{2} \xrightarrow{\text{yields}} \Delta V = V_{DC} \quad (23)$$

For modern Si SJ MOSFETs the variation in stored energy at high voltages is comparatively smaller than in a charge equivalent linear capacitor $C_{oss(tr)}$. Consequently, the decrease on the required starting energy in the inductor at starting voltages higher than the supply is comparatively smaller than in the SiC or GaN example devices. Practically, without additional stored energy in the inductor the full ZVS range is very much constrained (e.g. CrCM boost converter). Another side effect of the same phenomena is that a small amount of residual energy in the parasitic inductances during the charge of the C_{oss} potentially induces a higher V_{ds} overshoot in Si SJ switches than in an equivalent linear $C_{oss(tr)}$ capacitance. This effect makes this technology less suited for applications like synchronous rectification [27]. The required initial energy in the inductor for different starting voltages and a V_{DC} equal to 200 V has been calculated for the three example devices (Si, SiC and GaN) and represented in Fig. 10.

The previous analysis is verified by the calculation of the required initial energies for achieving ZVS in the three example devices (Si, SiC and GaN), and the simulation of the energy distribution in time during the transition, which is represented in Fig. 11 and Fig. 12. For the simulated examples in Fig. 11 and Fig. 12 the starting voltage in C_{oss} was 400 V and the V_{supply} voltage was half of it (200 V). Table III makes a summary of the results in the previously stated conditions.

TABLE III
SINGLE DEVICE AT A HIGHER VOLTAGE SUMMARY

	IPP60R170CFD7	IMZA65R027M1H	IGT60R070D1
V_{DC}	200 V	200 V	200 V
ΔV	200 V	200 V	200 V
$E_{ind,2}$	30.08 µJ	7.45 µJ	1.76 µJ
$Q_{oss}(V_{DC})$	153.01 nC	96.35 nC	26.08 nC
$E_{oss}(V_{DC})$	1.80 µJ	7.06 µJ	2.05 µJ
E_{supply}	33.25 µJ	29.69 µJ	8.12 µJ
Time	41.32 ns	43.99 ns	23.52 ns

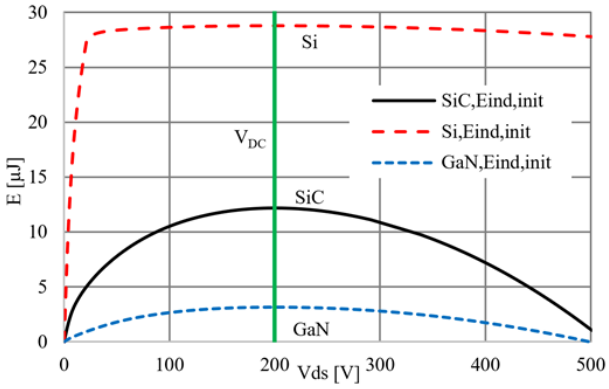

Fig. 10. Si, SiC and GaN typical additional required energy for discharge of C_{oss} for different initial V_{ds} voltages when the supply voltage is 200 V.

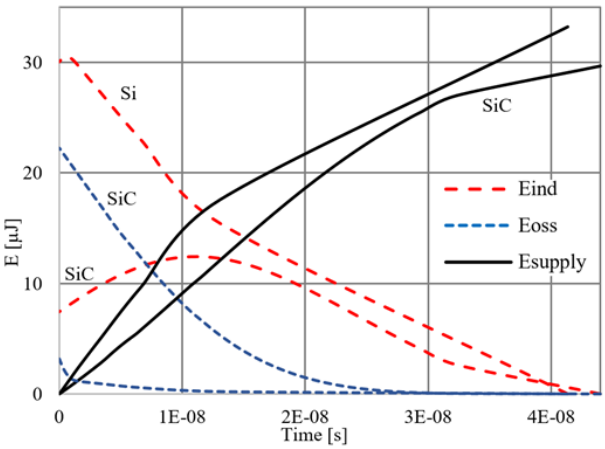

Fig. 11. Si and SiC typical distribution of energy during the discharge of the C_{oss} with starting voltage equal to 400 V and V_{DC} voltage equal to 200 V.

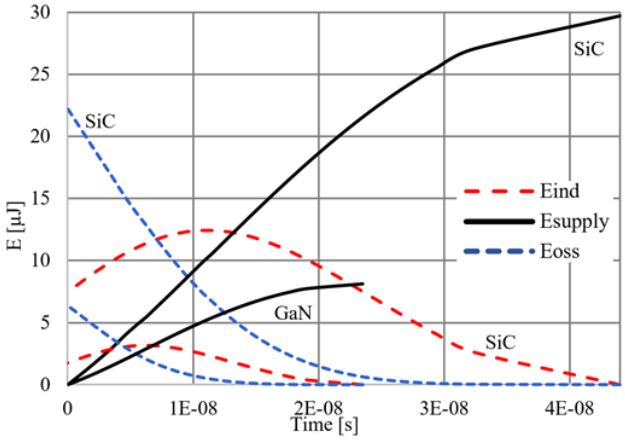

Fig. 12. SiC and GaN typical distribution of energy during the discharge of the C_{oss} with starting voltage equal to 400 V and V_{DC} voltage equal to 200 V.

C. SINGLE DEVICE AT A LOWER VOLTAGE

For completeness, the required energy for the discharge of C_{oss} when its initial voltage is lower than V_{DC} is analyzed in this section. The remaining charge in C_{oss} will be transferred into V_{supply}, which yields a net energy variation in V_{supply} that can be estimated by (24). The energy extracted from C_{oss} can be calculated with equation (25). The required initial energy in the inductor at the start of the transitions equals to the difference between the stored and the extracted energies, which can be calculated with equations (26-27).

$$\Delta E_{supply} = Q_{oss}(V_{DC} - \Delta V) \cdot V_{DC} \tag{24}$$

$$E_{oss}(V_{DC} - \Delta V) = \int_0^{(V_{DC}-\Delta V)} v \cdot C_{oss}(v)\, dv \tag{25}$$

$$E_{ind,3} = \Delta E_{supply} - E_{oss}(V_{DC} - \Delta V) \tag{26}$$

$$E_{ind,3} = Q_{oss}(V_{DC} - \Delta V) \cdot V_{DC} - E_{oss}(V_{DC} - \Delta V) \tag{27}$$

For an equivalent charge related linear capacitor $C_{oss(tr)}$ the stored energy can be alternatively calculated with (28), whereas the expression in (27) can be simplified into (29-30). In this scenario, the energy required is equal to the energy initially stored in C_{oss}.

$$E_{oss,linr}(V_{DC} - \Delta V) = Q_{oss}(V_{DC} - \Delta V) \cdot \frac{(V_{DC}-\Delta V)}{2} \tag{28}$$

$$E_{ind,linr,3} = Q_{oss}(V_{DC} - \Delta V) \cdot \left(V_{DC} - \frac{(V_{DC}-\Delta V)}{2}\right) \tag{29}$$

$$E_{ind,linr,3} = Q_{oss}(V_{DC} - \Delta V) \cdot \left(\frac{V_{DC}+\Delta V}{2}\right) \tag{30}$$

Like in the other two previous scenarios for single device topologies, the non-linear distribution of charge in the output capacitance of Si SJ devices requires comparatively more initial energy stored in the inductor than SiC

or GaN for achieving full ZVS. The results of the analysis were already represented in Fig. 10 for a supply voltage V_{DC} equal to 200 V and starting V_{ds} voltages lower than 200 V. Table IV makes a summary of the results for an alternative scenario where VDC equals 400 V and the starting V_{ds} equals half of it (200 V).

TABLE IV
SINGLE DEVICE AT A LOWER VOLTAGE SUMMARY

	IPP60R170CFD7	IMZA65R027M1H	IGT60R070D1
VDC	400 V	400 V	400 V
ΔV	-200 V	-200 V	-200 V
$E_{ind,3}$	62.86 µJ	31.95 µJ	8.44 µJ
E_{supply}	64.65 µJ	39.02 µJ	10.52 µJ
Time	28.61 ns	22.61 ns	11.82 ns

D. HALF-BRIDGE TOPOLOGIES

For the sake of generality in the analysis, a half-bridge in a resonant or quasi-resonant converter during the switching transition is represented by the simplified equivalent circuit in Fig. 13. In the simplified circuit there is a capacitor C_2 that stands for the output capacitance $C_{oss,2}$ of the device which is turning-off. The capacitor C_1 stands for the output capacitance $C_{oss,1}$ of the device which is turning-on. The inductor L_r is connected to the mid-point of the half-bridge and stands for an equivalent resonant inductance that provides the required energy for the ZVS transition. The equivalent series resistor R_s stands for all of the parasitic series resistances along the charging and discharging path.

In this scenario, the output capacitance $C_{oss,1}$ of the device that is turning-on is discharged towards the supply V_{supply} just like in the single device topology example. However, the output capacitance $C_{oss,2}$ of the device that is turning-off is being charged up to the supply voltage from the resonant inductor. Because the conduction path for the discharge of the $C_{oss,1}$ and the conduction path for the charge of $C_{oss,2}$ closes around different paths, the energy required for each of the transitions can be analyzed separately and later joined together to get the complete result. Notice that the analysis of the discharging transition of $C_{oss,1}$ is equivalent to the single device scenario analyzed in the previous section.

The previous analysis for single device topologies can also be applied for the charge of the capacitance $C_{oss,2}$ in Fig. 13. The supply voltage in V_{supply} is assumed equal to zero, which is effectively a short circuit. Substituting the values in equation (8) and taking into account the inverted polarity of voltages yields the well-known expression in (31). Alternatively, a more simple analysis methodology for the charge of $C_{oss,2}$ would be based on the balance of energies. All the energy stored in the inductor at the start of the transition would be moved and stored without loss into $C_{oss,2}$, which comprehensively yields as well to the expression in (31).

$$E_{ind,4} = Q_{oss}(-V_{DC}) \cdot 0 - E_{oss}(-V_{DC}) = E_{oss}(V_{DC}) \tag{31}$$

To the result previously obtained in equation (8) has to be added the result of equation (31) accounting for the additionally required charge of $C_{oss,2}$ and resulting in a single expression which can be used to calculate the minimum required inductor energy to reach ZVS in a half-bridge (32). For simplicity in the analysis, both stacked devices and their capacitances have been considered to be equal.

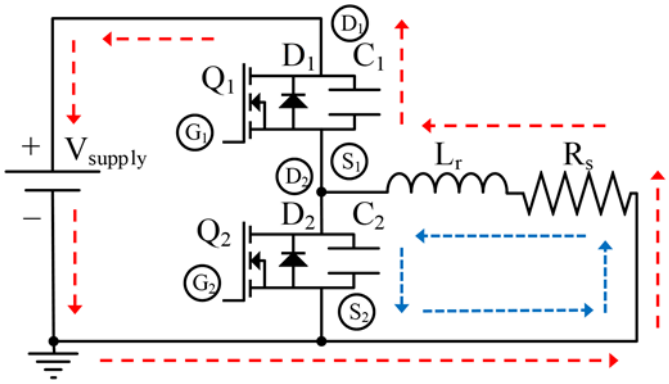

Fig. 13. Simplified equivalent circuit for the analysis of the required initial energy to achieve ZVS in a half bridge configuration.

$$E_{ind,5} = E_{ind,1} + E_{ind,4} = Q_{oss}(V_{DC}) \cdot V_{DC} \tag{32}$$

The consequence of the analysis is that in stacked devices topologies the required initial energy to achieve ZVS is independent of the stored energy $E_{oss}(V_{DC})$ and depends exclusively on the stored charge $Q_{oss}(V_{DC})$ and the supply voltage of the system V_{DC}. Unlike in the previous single device topology scenario, the non-linear distribution of charge in Si does not have a drawback on the ZVS range compared to other devices with an equivalent $C_{oss(tr)}$.

On the other hand, the $R_{ds,on}$ of a SiC or GaN device with an equivalent $C_{oss(tr)}$ is smaller than the $R_{ds,on}$ of the Si, which potentially decreases the conduction losses and improves the overall performance of the system. Therefore, the optimum results in the replacement of a Si device with a specific $R_{ds,on}$ by a SiC or GaN device with a similar or equal $R_{ds,on}$ requires to redesign the converter taking into account the reduced ZVS energy requirements. A simple one to one $R_{ds,on}$ based replacement would not take full advantage of the potential reduction in circulating currents and the overall benefits of the improved semiconductor technology characteristics.

The previous analysis is verified by the calculation of the required initial energies for achieving ZVS with the three example devices (Si, SiC and GaN), and the simulation of the energy distribution in time during the transition, represented in Fig. 14 and Fig. 15. The drain to source voltage along time during the transition has been represented in Fig. 16, where it can be observed that the total transition time also depends mostly on the total stored charge $Q_{oss}(V_{DC})$, similar for Si and SiC but much smaller for GaN. Table V makes a summary of the results represented in the previously stated figures.

TABLE V
HALF-BRIDGE SUMMARY

	IPP60R170CFD7	IMZA65R027M1H	IGT60R070D1
V_{DC}	400 V	400 V	400 V
$E_{ind,5}$	66.13 µJ	59.29 µJ	16.32 µJ
E_{supply}	66.13 µJ	59.29 µJ	16.32 µJ
Time	42.62 ns	42.19 ns	22.20 ns

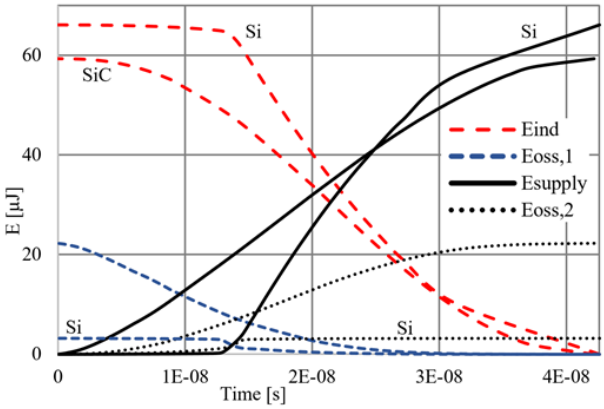

Fig. 14. Si and SiC typical distribution of energy during the discharge of $C_{oss,1}$ and the charge of $C_{oss,2}$.

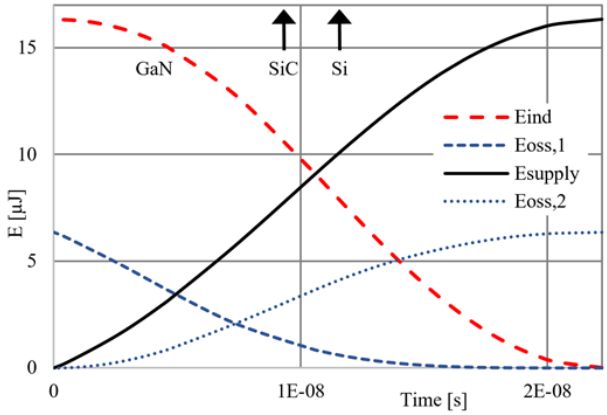

Fig. 15. GaN typical distribution of energy during the discharge of $C_{oss,1}$ and the charge of $C_{oss,2}$.

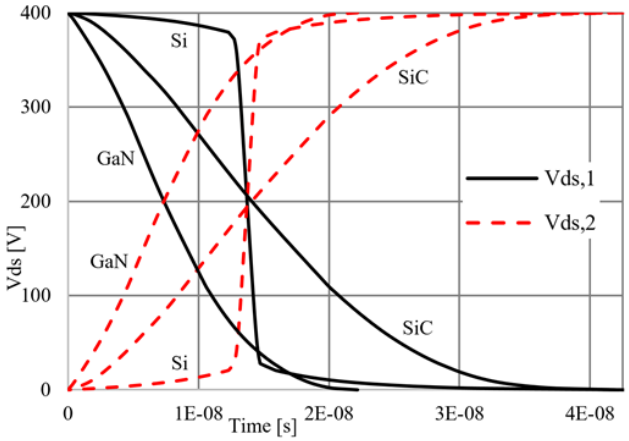

Fig. 16. Si, SiC and GaN typical V_{ds} voltage during the resonant discharge of $C_{oss,1}$ and the resonant charge of $C_{oss,2}$.

III. HARD SWITCHED TURN ON LOSSES

A. *SINGLE DEVICE TOPOLOGIES*

The conclusions extracted from the analysis in the previous sections are valid whenever full ZVS is ensured in all the operating conditions of interest of the resonant converter. However, it is not always possible or necessarily better performing a converter designed to operate in full ZVS in all conditions. Depending on the balance of switching to conduction losses in a specific design, it could be more effective to allow partial ZVS (or partial hard-switching). The impact of partial ZVS, and the non-linear stored charge distribution along the voltage in C_{oss} in the event of partial ZVS will be analyzed in this section.

In single device topologies it is only necessary to consider the remaining stored energy $E_{oss}(\Delta V)$ at the voltage ΔV at which the device turns-on under partial or full hard-switching [5]. That remaining energy will be dissipated within the device itself. In this scenario, the switching losses of Si compared to the other two devices would be bigger or smaller depending on the hard-switched voltage. In Fig. 17 can be observed that the Si device is superior to an equivalent $C_{oss(tr)}$ SiC device in the range between 75 V and 400 V (V_{DC}). More noticeably, it can be observed in Fig. 17 that the Si device is superior to a similar $C_{oss(er)}$ GaN device in the voltage range between 175 V and 375 V. However, the Si device performs worse than the other two devices in partial or full hard-switching out of those ranges. Fig. 18 represents the comparative increment of losses between Si and the other two devices while hard-switching them at 22 V and at different frequencies.

Consequently, the non-linear distribution of charge in Si output capacitance C_{oss} could be theoretically advantageous to other equivalent $C_{oss(tr)}$ devices and/or $C_{oss(er)}$ devices when partial ZVS occurs within a defined voltage range. However, in practice, for a decreasing initial inductor energy, Si would perform initially worse until the remaining E_{oss} of SiC and GaN goes beyond the remaining E_{oss} of Si (Fig. 19). Table VI makes a summary of the results in a scenario with low initial E_{ind}, which is enough for GaN to achieve full ZVS but causes SiC to present more switching losses than Si.

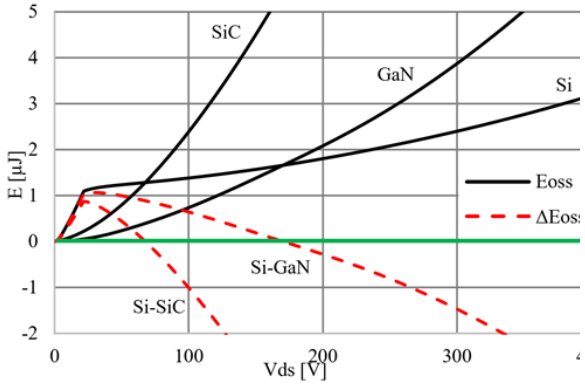

Fig. 17. Si, SiC and GaN typical hard switching losses at different V_{ds} voltages and comparative loss between the Si and the SiC and GaN devices.

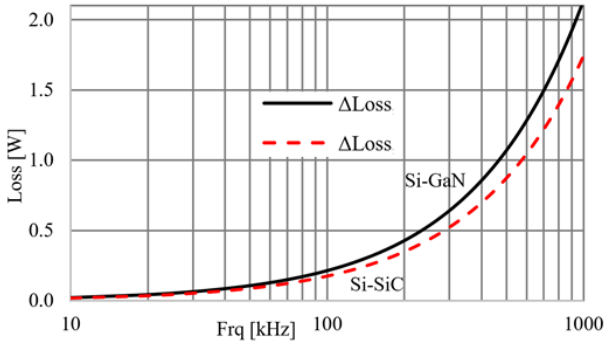

Fig. 18. Comparative increase of losses for the hard switching of the Si, SiC and GaN devices at 22 V and different switching frequencies.

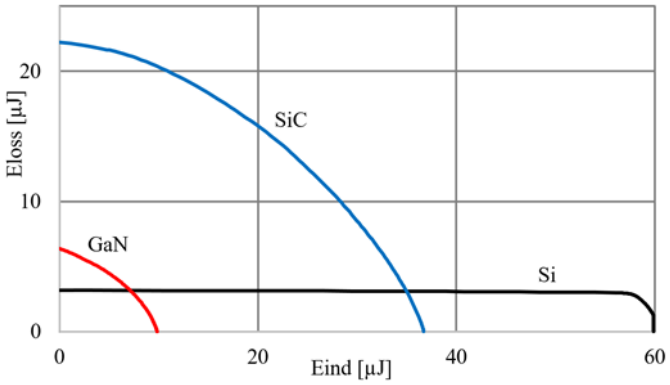

Fig. 19. Comparative increase of loss for the hard switching of the Si, SiC and GaN devices with different starting energies in the resonant inductor.

TABLE VI
SINGLE DEVICE HARD-SWITCHED SUMMARY

	IPP60R170CFD7	IMZA65R027M1H	IGT60R070D1
V_{DC}	400 V	400 V	400 V
E_{ind}	10 µJ	10 µJ	10 µJ
$V_{ds,1}$	398 V	379 V	0 V
$E_{oss,1}(V_{ds,1})$	3.16 µJ	20.24 µJ	0 µJ
E_{loss}	3.16 µJ	20.24 µJ	0 µJ

B. HALF-BRIDGE TOPOLOGIES

In the event of partial or full hard-switching in the stacked configuration in Fig. 13, the device which is hard-switched turned-on (Q_1 in this analysis) dissipates within itself the remaining stored energy in its output capacitance $E_{oss}(\Delta V)$, similarly to the single device scenario. However, in a half-bridge configuration, in the event of partial or full hard-switching the capacitance which was being charged ($C_{oss,2}$), completes its charge resistively.

The energy that is extracted from the supply during the resistive charge of $C_{oss,2}$ can be calculated with (33), whereas the energy stored into $C_{oss,2}$ can be calculated with (34-35). The difference between the supplied and the stored energy (36) corresponds to the energy that has been dissipated within the series resistances in the charging path R_s, mostly in the channel of the opposing device Q_1.

$$\Delta E_{supply,2} = \left(Q_{oss}(V_{DC}) - Q_{oss}(V_{DC} - \Delta V)\right) \cdot V_{DC} \tag{33}$$

$$\Delta E_{oss,2} = E_{oss}(V_{DC}) - E_{oss}(V_{DC} - \Delta V) \tag{34}$$

$$\Delta E_{oss,2} = \int_{(V_{DC}-\Delta V)}^{V_{DC}} v \cdot C_{oss}(v)\, dv \tag{35}$$

$$\Delta E_{loss,2} = \Delta E_{supply,2} - \Delta E_{oss,2} \tag{36}$$

The total loss in the event of partial or full hard-switched turn-on in a half-bridge is the sum of the loss within the switching device Q_1 plus the loss caused by the completion of the charge of the opposing device Q_2 (37).

$$\Delta E_{loss,tot} = \Delta E_{loss,2} + E_{oss,1}(\Delta V) \tag{37}$$

In the case of a linear capacitor the stored energy $\Delta E_{oss,2}$ calculated in (35) can be simplified into (38-40). Whereas the energy extracted from the supply can be further simplified into (41), and the expression for the dissipated energy during the completion of the charge simplified into (42-43).

$$E_{oss,2,linr}(V_{DC}) = Q_{oss}(V_{DC}) \cdot \frac{V_{DC}}{2} = C_{oss(tr)} \cdot \frac{V_{DC}^2}{2} \tag{38}$$

$$E_{oss,2,linr}(V_{DC} - \Delta V) = C_{oss(tr)} \cdot \frac{(V_{DC}-\Delta V)^2}{2} \tag{39}$$

$$\Delta E_{oss,2,linr} = C_{oss(tr)} \cdot \left(\frac{V_{DC}^2}{2} - \frac{(V_{DC}-\Delta V)^2}{2}\right) \tag{40}$$

$$\Delta E_{supply,2,linr} = C_{oss(tr)} \cdot (V_{DC}^2 - (V_{DC} - \Delta V) \cdot V_{DC}) \tag{41}$$

$$\Delta E_{loss,2,linr} = \Delta E_{supply,2,linr} - \Delta E_{oss,2,linr} \tag{42}$$

$$\Delta E_{loss,2,linr} = C_{oss(tr)} \cdot \frac{(\Delta V)^2}{2} \tag{43}$$

The total loss in the event of partial or full hard-switched turn-on in a half-bridge with linear capacitances $C_{oss(tr)}$ results in the expression in (44). Therefore, when partial ZVS occurs within certain voltage range the non-linear distribution of charge in the Si output capacitance C_{oss} is theoretically advantageous with regard to other equivalent $C_{oss(tr)}$ devices or equivalent $C_{oss(er)}$ devices (Fig. 20 and Fig. 21). However, the required resonant energy to reach a certain switching voltage is very distinct. Consequently, for a certain available resonant energy the switching losses are directly related to the equivalent $C_{oss(tr)}$, which has been represented in Fig. 22, where the SiC and GaN devices outperform the Si device in all the energy range. Moreover, notice how the total switching loss of Si increases dramatically near the end of the supply range V_{DC} because most of the charge in $C_{oss,2}$ is stored under a V_{ds} of 22 V.

$$\Delta E_{loss,t,linr} = C_{oss(tr)} \cdot (\Delta V)^2 \tag{44}$$

Table VII makes a summary of the results in Fig. 22 in a scenario with low initial E_{ind}, which is not enough for any of the devices to achieve full ZVS.

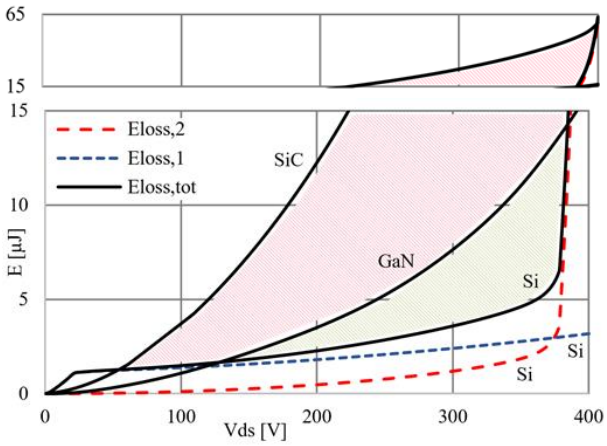

Fig. 20. Si, SiC and GaN typical half bridge hard-switching loss at different Q_1 turn-on voltages.

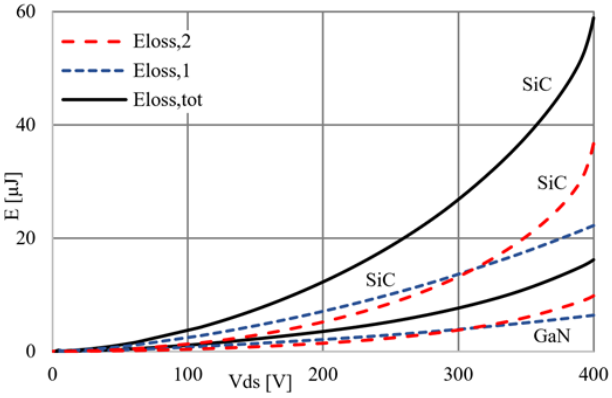

Fig. 21. SiC and GaN typical half bridge hard-switching loss at different Q_1 turn-on voltages.

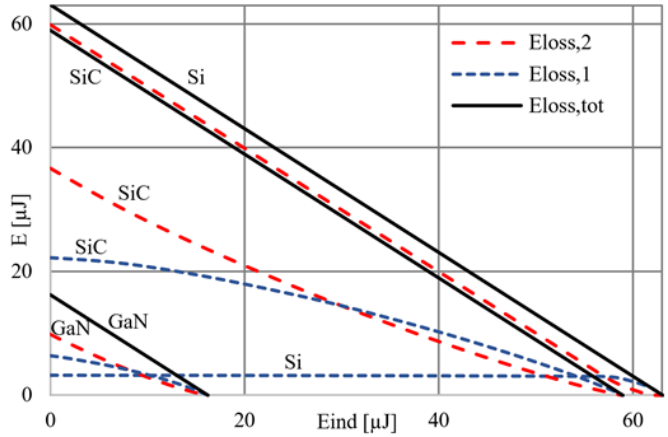

Fig. 22. Si, SiC and GaN typical half bridge hard-switching loss for different starting energies in the resonant inductor.

TABLE VII
HALF-BRIDGE HARD-SWITCHED SUMMARY

	IPP60R170CFD7	IMZA65R027M1H	IGT60R070D1
V_{DC}	400 V	400 V	400 V
E_{ind}	10 µJ	10 µJ	10 µJ
$V_{ds,1}$	398 V	384 V	129 V
$V_{ds,2}$	2 V	16 V	271 V
$Q_{oss,2}(V_{ds,2})$	26.79 nC	22.25 nC	20.15 nC
$E_{oss,1}(V_{ds,1})$	3.16 µJ	20.73 µJ	3.28 µJ
E_{loss}	52.35 µJ	48.67 µJ	6.16 µJ

C. *MILLER FEEDBACK EFFECT*

The charge of the gate to drain capacitance C_{gd}, which is part of C_{oss}, causes the injection of current into the gate to source capacitance C_{gs} and into the gate-driving path. Depending on the rising slope of the drain voltage, the ratio of the capacitance values and the impedance of the gate-driving path, it could happen that the device turns-on unexpectedly by the so-called Miller feedback effect. The phenomena could occur during the turn-off transition, effectively delaying the turn-off and increasing the switching losses, or during the hard-switching turn-on of the opposing device, causing a short circuit of the half-bridge that may destroy the devices. This mechanism is frequently confused with hard-commutation, which could also cause the failure of the devices by other means [28]-[29].

Applying a similar analysis to one in the previous sections for the charge of two capacitors in series, we can stablish criteria for the minimum prerequisites for the Miller feedback induced turn-on to occur. The worst possible scenario is where all the charge in C_{gd} ($Q_{gd}(V_{DC})$ in equation (45)) is transferred into C_{gs} fast enough that negligible voltage is discharged through the gate driving path. The induced voltage raise in C_{gs} (which is approximately equal to C_{iss}) should reach at least the threshold voltage of the device V_{th} for the feedback induced turn-on to occur (46). With the parameters in Table I, it can be calculated that for the Si device the $V_{gs,max}$ would be 2.63 V, well under its threshold, whereas for the SiC device is 5.77 V and for the GaN device is 5.47 V, both of which are above their respective thresholds.

$$Q_{gd}(V_{DC}) = \int_0^{V_{DC}} C_{gd}(v)\,dv \tag{45}$$

$$V_{gs,max} \cong \frac{Q_{gd}(V_{DC})}{C_{iss}} < V_{th} \tag{46}$$

IV. HARD SWITCHED TURN OFF LOSSES

A contribution to the switching losses that is frequently neglected in resonant ZVS topologies is the one caused by the hard-switched turn-off transition. In resonant ZVS topologies, in spite of the devices turning-on under ZVS conditions, the prior turn-off necessarily happens in hard-switching. However, it is true that hard-switching turn-off losses can be significatively lower than the hard-switched turn-on losses, and that whenever the device turns-off fast enough the losses are in fact negligible. In this section, we analyze the conditions for a fast and near lossless turn-off and the consequences of a slow or delayed turn-off.

The *dv/dt* during a resonant turn-off transition is given by the available resonant current and the size of the output capacitances of the semiconductor device. The output capacitance C_{oss} of the semiconductor power switch can be split conveniently into the equivalent drain to source capacitance C_{ds} and the gate to drain capacitance C_{gd}. While the drain voltage raises, both capacitances are charged simultaneously, but through different paths. Whenever the *dv/dt* is limited by the C_{gd} charging path, the turn-off of the device is slowed down, and the channel carries part of the resonant current, which is therefore not fully stored in C_{oss} (47-50). Moreover, the overlap of current and voltage during a slowed down turn-off causes losses.

$$\frac{dv}{dt} = \frac{i_{dg}(t)}{C_{dg}(v)} = \frac{i_{ds}(t)}{C_{ds}(v)} \tag{47}$$

$$i_d(t) = i_{ch}(t) + i_{dg}(t) + i_{ds}(t) \tag{48}$$

$$i_{ch}(t) = 0 \xrightarrow{\text{yields}} i_{ds}(t) = i_d(t) - i_{dg}(t) \tag{49}$$

$$\frac{C_{ds}(v)}{C_{dg}(v)} = \frac{i_d(t) - i_{dg}(t)}{i_{dg}(t)} = \frac{i_d(t)}{i_{dg}(t)} - 1 \tag{50}$$

The maximum gate current $i_{dg}(t)$ capability depends on the driver's turn-off path total impedance $R_{g,off}$, the off-state driving voltage $V_{G,off}$ and the voltage at the gate during the voltage transition (V_{Miller} or approximately V_{th} when the channel does not conduct) (51). We can substitute (51) in (50) and simplifiy it into (52) assuming the driver turn-off voltage to be zero, which is the most frequent case for the devices in this comparison. The expression (52) summarizes the condition for a lossless resonant turn-off. Notice that $C_{ds}(v)$ and $C_{dg}(v)$ are a function of the voltage. Moreover, the condition is a function of the drain current $i_d(t)$, which is load dependent in most of the converters. From the previous analysis it can be concluded that the fast turn-off range can be extended by several means: decreasing $R_{g,off}$, increasing V_{th} of the device, or increasing the ratio of $C_{ds}(v)$ to $C_{dg}(v)$ (e.g. placing an additional capacitor in parallel to $C_{ds}(v)$).

$$i_{dg}(t) = \frac{V_{gs}(t) - V_{G,off}}{R_{g,off}} \approx \frac{V_{th}}{R_{g,off}} \tag{51}$$

$$\frac{C_{ds}(v)}{C_{dg}(v)} \geq \frac{i_d(t) \cdot R_{g,off}}{V_{th}} - 1 \tag{52}$$

The previous analysis is verified by the simulation of the slow turn-off losses in the three example devices (Si, SiC and GaN) and represented in Fig. 23 and Fig. 24. Whereas all the devices in the simulated examples are turning-off with the same resonant current of 12 A, the driving impedance has been adjusted for all of them to cause the same amount of total loss ($E_{loss,tot}$). Notice, however, that the driving impedance for the Si device already accounts for the integrated resistance and cannot be further decreased, whereas the driving impedance of the SiC and GaN devices has been increased with additional external resistances.

On the other hand, it is sometimes desirable to slow down the maximum *dv/dt* during the switching transitions in certain applications or due to EMI constraints [30]. The *dv/dt* can be controlled limiting the charge of C_{gd} at the expense of the additional switching losses. Fig. 25 represented the switching losses while limiting the maximum *dv/dt* for the three devices in the comparison (Si, SiC and GaN). It can be observed that, whereas the non-linearity of Si causes extremely high maximum *dv/dt*, the SiC device is very well suited for low *dv/dt* applications because its capacitances are quasi-linear and relatively big in comparison to GaN. Table VIII makes a summary of the results of the required conditions for achieving similar turn-off losses with the same initial current and voltage in the three analyzed devices.

TABLE VIII
HARD-SWITCHED TURN-OFF LOSS SUMMARY

	IPP60R170CFD7	IMZA65R027M1H	IGT60R070D1
V_{DC}	400 V	400 V	400 V
$R_{g,off}$	10.90 Ω	19.06 Ω	19.30 Ω
i_d	12 A	12 A	12 A
dv/dt_{max}	216.01 V/ns	17.45 V/ns	71.96 V/ns
$E_{loss,tot}$	2.01 µJ	2.01 µJ	2.01 µJ
Time	36.99 ns	37.37 ns	16.82 ns

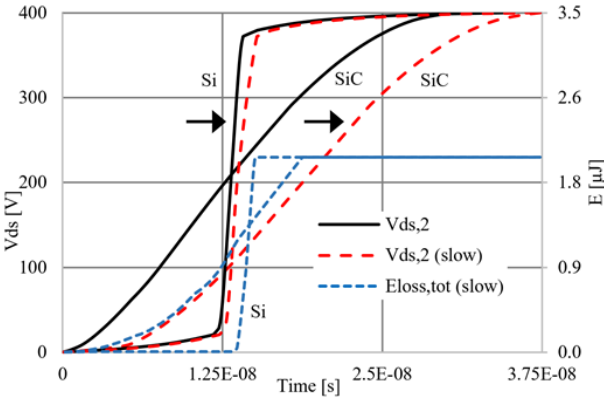

Fig. 23. Si and SiC typical hard switched turn-off slowed down by the gate impedance. Si: $R_{g,off}$ = 10.9 Ω (value of the embedded R_g) and 12A turn-off current. SiC: $R_{g,off}$ = 19 Ω (including embedded R_g) and 12A turn-off current.

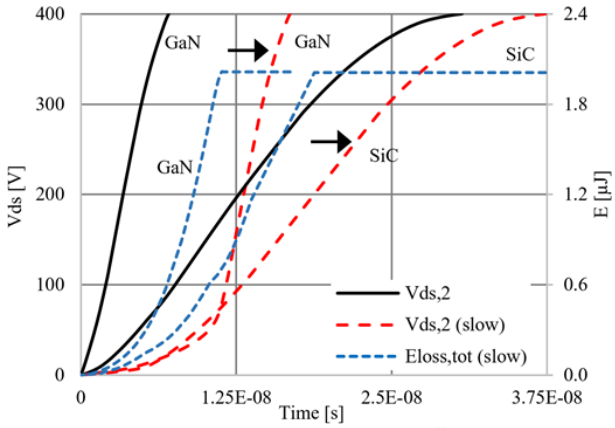

Fig. 24. SiC and GaN typical hard switched turn-off slowed down by the gate impedance. SiC and GaN: $R_{g,off}$ = 19 Ω (including embedded R_g) and 12 A turn-off current.

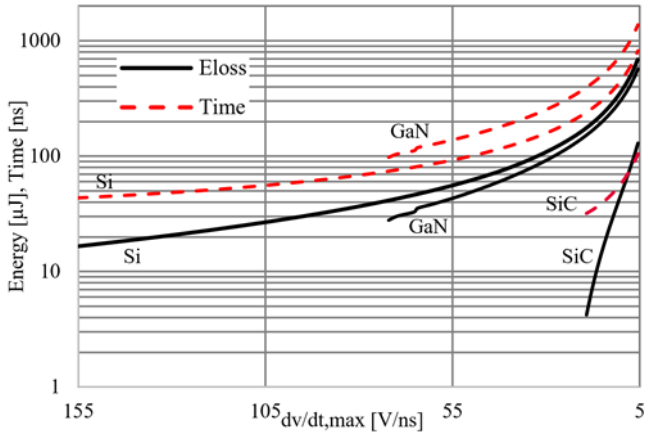

Fig. 25. Slow turn-off with limited *dv/dt*. Total time of the transition and switching losses for the three different capacitance profiles.

V. EXPERIMENTAL

A 3300 W LLC DCDC converter [31] (Fig. 26) was designed and built with the specifications given in Table IX to test the analysis and guidelines presented in this work. The Si device IPW60R031CFD7 in Table X was mounted for its test in the primary side HV half-bridge of the converter. The control was implemented with XMC™ 4200 ARM® Cortex®-M4 microcontroller from Infineon Technologies AG. The equivalent simplified circuit of the prototype corresponds to the one in Figure 13. A complete schematic can be found in [31].

TABLE IX
KEY PARAMETERS OF PROTOTYPE

Parameter	Value
Nominal input voltage	400 V
Input voltage range	350 V - 415 V
Nominal output voltage	52 V
Output voltage range	43.5 V – 59.5 V
Maximum output power	3300 W
Maximum output current	65 A
Switching frequency	45kHz-250 kHz
Resonant frequency	70 kHz
Magnetizing inductance (Lm)	100 µH
Resonant inductance (Lr)	10 µH

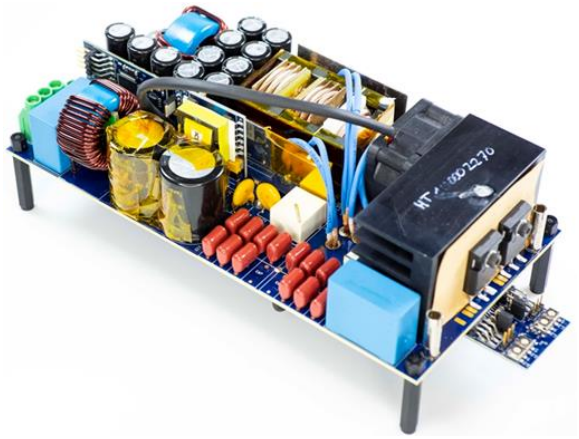

Fig. 26. Prototype of the 3.3 kW LLC resonant converter.

TABLE X
SUMMARY OF DEVICE CHARACTERISTICS

	IPW60R031CFD7	IMZA65R027M1H	IGT60R070D1
$R_{DS,on}$	26 mΩ @ 25 °C	27 mΩ @ 25 °C	55 mΩ @ 25 °C
Q_{oss}	840 nC @ 400 V	147 nC @ 400 V	40.5 nC @ 400 V
E_{oss}	16.24 µJ @ 400 V	29.46 µJ @ 400 V	8.10 µJ @ 400 V
C_{gs}	5623 pF	2114 pF	380 pF
R_g	3.8 Ω	3 Ω	0.78 Ω
V_{th}	4 V	4.5 V	1.2 V

Because of the wide input and wide output range requirements of the prototype the circulating currents are relatively high and the converter switches in full ZVS along most of its operating range. In Fig. 27 the characteristic change of slope in the drain voltage caused by the non-linear capacitance of Si can be observed. Notice in Fig. 27 a slight evidence of Miller plateau that can be identified during the turn-on because of a slightly short dead-time. In Fig. 28 illustrates the lossless turn-off transition while the converter operates slightly above resonance. Notice in Fig. 28 the Miller plateau at a voltage near the threshold during the resonant charge of C_{oss}.

In the LLC topology, at light loads and low output voltages the relation between the switching frequency and the gain of the converter becomes non-monotonic. This effect is caused by the parasitic capacitances of the transformer and the secondary side rectifiers [14]. In these operating conditions, the switching frequency of the converter increases to maintain the regulation, while the resonant current and the available energy for the ZVS transition decreases. In Fig. 29 the partial hard-switching when the converter's frequency raises up to 130 kHz can be observed. As previously analyzed, the switching losses of the Si device would be higher than an equivalent $C_{oss(tr)}$ SiC device in this very same condition. Furthermore, a SiC or GaN device of equivalent $R_{ds,on}$ will be still capable by far of achieving full ZVS.

During the start-up, at high loads and low voltages the converter operates switching off relatively high currents. In these conditions the switching losses could increase significatively if the turn-off transition is limited by the driving path. Moreover, because of the high resonant currents, the *dv/dt* and *di/dt* within the commutation loop increase, causing the voltage ringing in Fig. 30. However, the speed of the transition can be controlled by the impedance of the driving path $R_{g,off}$ or by adding a capacitance in parallel to C_{ds}.

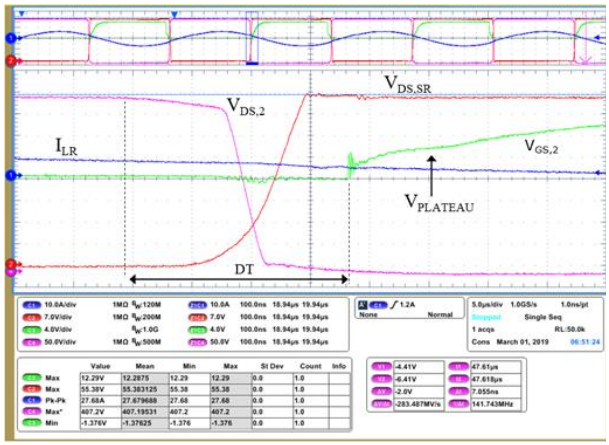

Fig. 27. ZVS turn-on in the LLC 3.3 kW converter switching at its resonant frequency.

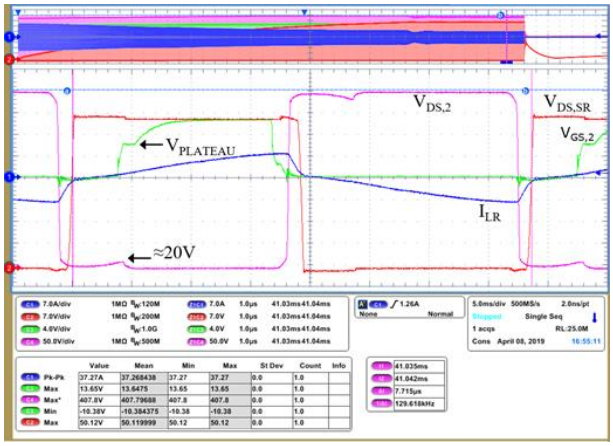

Fig. 29. Partial ZVS turn-on in the LLC 3.3 kW converter operating at light load and switching far above its resonant frequency.

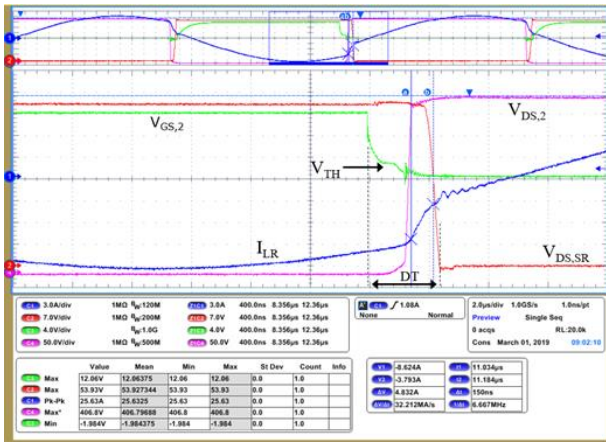

Fig. 28. Fast and lossless hard-switched turn-off in the LLC 3.3 kW switching above its resonant frequency.

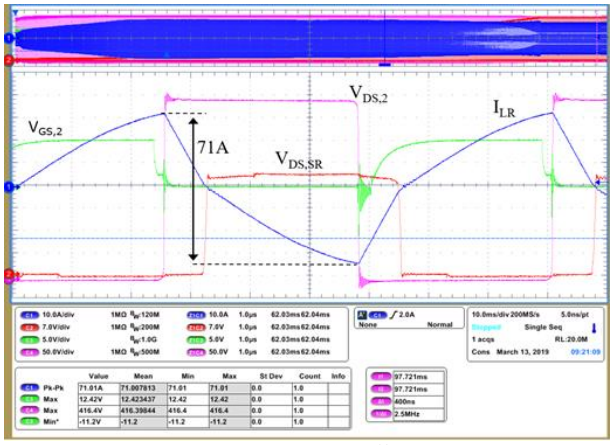

Fig. 30. High current hard-switched turn-off transitions in the LLC 3.3 kW. The high resonant current causes high *dv/dt* and *di/dt* within the commutation loop.

VI. CONCLUSION

The parasitic capacitances of modern Si SJ MOSFETs are characterized by its non-linearity. At high voltages the total stored energy $E_{oss}(V_{DC})$ in the output capacitance $C_{oss}(v)$, differs substantially from the energy in an equivalent linear capacitor $C_{oss(tr)}$ that stores the same amount of charge. That difference requires the definition of an additional equivalent linear capacitor $C_{oss(er)}$ that stores the same amount energy at a specific voltage. However, the parasitic capacitances of current SiC and GaN devices have a more linear distribution of charge along the voltage. Moreover, the equivalent $C_{oss(tr)}$ and $C_{oss(er)}$ of SiC and GaN devices is smaller than the ones of a Si device with a similar $R_{ds,on}$.

In this work the impact of the non-linear distribution of charge in the output capacitance of modern Si devices on the performance and requirements for the design of resonant ZVS converters has been analyzed. Furthermore, the non-linear capacitance of Si has been compared to the quasi-linear capacitance of a SiC device of equivalent time related output capacitance $C_{oss(tr)}$, and compared to the quasi-linear capacitance of a GaN device of similar energy related output capacitance $C_{oss(er)}$. The advantages and disadvantages of each of the alternatives have been analyzed for single device and half-bridge based topologies, as well as in full ZVS and partial or full hard-switching operating conditions.

In half-bridge topologies the required energy to achieve full ZVS depends exclusively on the total output stored charge $Q_{oss}(V_{DC})$ and the supply voltage V_{DC}, whereas in single device topologies the required energy is further increased by a relatively smaller $E_{oss}(V_{DC})$. In summary, in the full ZVS scenario, the equivalent SiC and the GaN devices are superior to the Si device in single device and half bridge topologies.

In partial hard-switching turn-on, within certain hard-switching turn-on voltage, the losses of the Si device could be lower than the switching losses of the equivalent $C_{oss(tr)}$ SiC or the equivalent $C_{oss(er)}$ GaN device. However, for a certain energy in the resonant inductor the switching voltage of the SiC or the GaN devices is much lower. Moreover, the Si advantage window dramatically diminishes when is compared to equivalent $R_{ds,on}$ SiC or GaN devices.

Overall, this work demonstrates that a meaningful one-to-one replacement of devices without a redesign of the converter would be among devices with an equivalent $C_{oss(tr)}$. Moreover, to fully unleash the potential improvement in the overall performance of the converter while replacing a Si device by an equivalent $R_{ds,on}$ SiC or GaN device requires the redesign of the resonant ZVS converter accounting for the reduced ZVS energy requirements. Finally, a highly efficient 3300 W DCDC LLC resonant converter prototype was designed and built to demonstrate the validity of the analysis.

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CHAPTER 11. FIFTH PUBLICATION

High Efficiency, Narrow Output Range and Extended Hold-Up Time Power Supply with Planar and Integrated Magnetics for Server Applications

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***Abstract*— In this paper, the design of a new complete power supply for server applications is discussed. The main constraints of the new solution are the very high peak efficiency, the long hold-up time and the maximum outer dimension. The PSU is comprised of a front-end ACDC bridgeless totem-pole PFC and a back-end DCDC half-bridge LLC. Due to the extended hold-up time, the PSU requires large intermediate energy storage and an extended gain range for the LLC. Due to the outer dimension limits, a planar transformer with reduced height and volume is preferred. Finally, the very high efficiency target requires a careful design based on the accurate modeling of the overall losses of the converter. The analysis is demonstrated experimentally with a 3 kW PSU achieving 97.47 % of efficiency at 230 V_{AC}.**

GLOSSARY

Dconduction	Boost diode conduction loss
Ehys	C_{oss} charge-discharge loss
EMI	Electromagnetic interference filter
Poff	Turn-off loss
Pon	Turn-on loss
SWconduction	Boost switch conduction loss
Vf	Diode forward voltage

I. INTRODUCTION

Due to the continuous increment in processing power in server applications, the requirements of efficiency and power density in the server Power Supply Unit (PSU) also increase consequently. On the one hand, the electric power consumption raises the operating cost of the infrastructure. On the other hand, the wasted power produces unwanted heat that requires additional cooling of the system at all levels, e.g. PSU, server rack, and building.

In 2019 the Open Compute Project (OCP) [1] released a draft of the third version of the OCP rectifier specifications. The main changes between this version and the previous ones are the higher output voltage and the higher power density and efficiency. The output voltage has been increased from 12 V to 50 V [2]-[3], which significantly decreases the conduction losses in the bus bars at a rack level. Moreover, it makes it easier to achieve higher power and efficiency in the PSU. The required peak efficiency of the rectifier at 230 V_{AC} input is 97.5 %. Further efficiency constraints are summarized in Fig. 1.

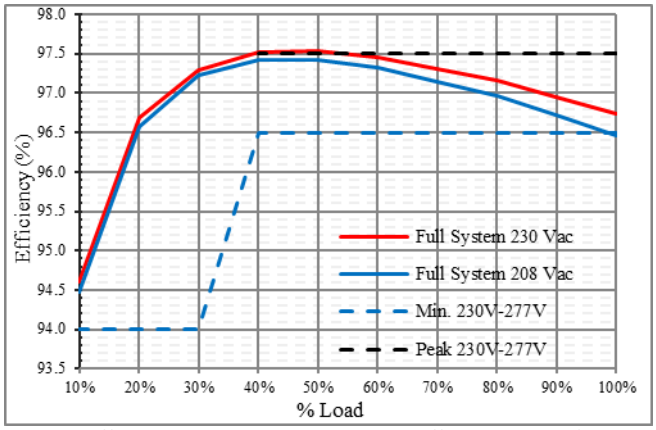

Fig. 1: OCP v3 efficiency requirements and estimated efficiency curve of a compliant PSU.

The preliminary analysis indicated that the most feasible solution for achieving the target specifications is a PSU comprised of two stages [4]. The front-end ACDC conversion stage provides power factor correction (PFC) and total harmonic distortion (THD), while the back-end DCDC conversion stage provides tight regulation of the output and safety isolation. The PFC is realized by a bridgeless totem-pole PFC with Silicon Carbide (SiC) MOSFETs [5], while the back-end isolated DCDC is realized by a half-bridge LLC series-parallel resonant converter [6] with Silicon (Si) Superjunction (SJ) High-Voltage (HV) MOSFETs and Si Low-Voltage (LV) MOSFETs rectifiers. Fig. 2 shows a simplified schematic of the complete PSU.

Although the nominal output voltage of the converter has narrow range 50 V_{DC}, due to the long hold-up time requirements, up to 20 ms at full rated power, the PSU requires large intermediate storage energy and extended gain range of the LLC [7]-[8].

The large intermediate storage can be achieved with a large bulk capacitance value and/or a higher bulk capacitance voltage. Whereas a large bulk capacitance value requires additional volume and cost, a higher bulk capacitance voltage requires capacitors and power semiconductor switches with a higher voltage rating, which are costly and, in general, with a worse Figure of Merit (FoM).

The extended gain range of the LLC requires reducing the magnetizing inductance of the main transformer, therefore increasing the conduction losses and overall reducing the peak efficiency of the converter. Moreover, the clamping diodes further limit the theoretical boosting gain capability during the hold-up time.

In this regard, the high peak efficiency requirements together with the constrained dimensions and the extended hold-up time make the design of a PSU compliant with the newly released OCP v3 a challenging task.

In this work, a complete power supply has been built and tested with a peak efficiency of 97.47 %. The analysis of the results and the thermal captures show that the main contributions to the overall losses are the main transformer of the LLC, and the switching losses of the SiC MOSFETs in the PFC and the Si SRs in the LLC.

The rest of this document is organized as follows. The design and estimated performance of the totem-pole PFC stage are discussed in section II. The design and estimated performance of the LLC stage is discussed in section III, together with a detailed description of its magnetics construction. The experimental results are discussed in section IV. Finally, section V presents a summary of conclusions out of this work.

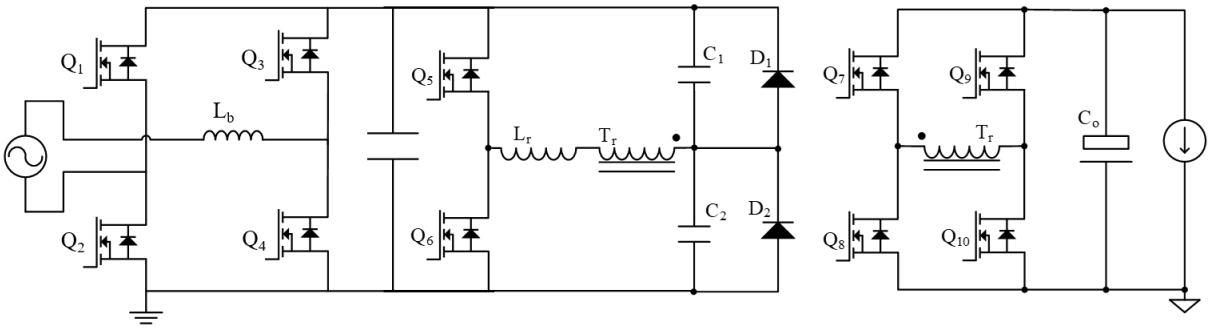

Fig. 2: Simplified schematic of the prototype PSU. Front-end totem-pole PFC followed by a half-bridge LLC resonant converter.

II. TOTEM-POLE PFC

The totem-pole PFC is a bridgeless ACDC converter capable of achieving very high efficiencies (Fig. 3). Unlike the classic boost ACDC converter, there is only one semiconductor in the rectification path at any given time (Q_1 and Q_2). The rectification losses can be further reduced by actively switching Q_1 and Q_2 and implementing them

with very low $R_{DS(on)}$ devices. It should be noted that the switching and driving loss contribution of Q_1 and Q_2 is very limited because they switch at only twice the grid frequency (50 Hz-60 Hz).

However, one of the main drawbacks of this topology is that the boost switches (Q_3 and Q_4) operate most of the time in hard-commutation. Therefore, Q_3 and Q_4 need to be implemented with low or very low reverser recovery charge (Q_{rr}) devices for the best efficiency and reliability. Due to this, the preferred alternatives are Wide Bandgap (WBG) semiconductor devices (SiC or GaN). However, alternative modulations may enable the use of Si SJ MOSFETs in what is commonly known as ZVS totem-pole or Triangular Current Mode (TCM) totem-pole [9].

A summary of the key design parameters of the prototype is presented in Table 1. Due to the extended hold-up time requirements, the bulk capacitance is comprised of three times 820 µF and the nominal voltage is set at 410 V_{DC}. Therefore, the bulk consumes a large part of the volume of the PSU. Nevertheless, a positive side effect of the large capacitance is the reduced voltage ripple at the input of the back-end DCDC stage, which can operate at its most efficient point in steady state.

Table 1: Key specifications of the totem-pole prototype.

Parameter	**Value**
Nominal input voltage	180 V_{AC} – 277 V_{AC}
Nominal output voltage	410 V_{DC}
Rated power	3 kW
Switching frequency	65 kHz
Boost inductor (L_b)	539 µH
Core material	High Flux GT 60 µ
Inductor turns	62 (AWG 15)
SR MOSFETs (Q_1, Q_2)	IPW60R017C7
Boost MOSFETs (Q_3, Q_4)	IPZA65R048M1

Figure 4 summarizes the estimated overall distribution of losses in the totem-pole PFC converter stage operating at 50 % of the rated power (1.5 kW) and at 230 V_{AC}. It can be observed that the major contribution of loss is due to the boost switch and diode (Q_3 and Q_4, which are SiC MOSFETs). Therefore, Q_3 and Q_4 should be dimensioned considering their operation at the worst case as well, i.e. minimum input voltage (180 V_{AC}) and maximum ambient temperature (50°C). At those conditions, both the switching losses and the conduction losses increase. Although, the low temperature dependency of the $R_{DS(on)}$ in SiC and its high temperature capability provides more freedom in their selection and the design of the cooling system [10].

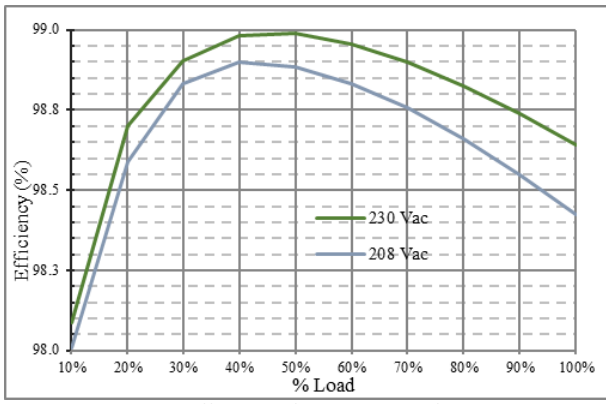

Fig. 3: Estimated efficiency of the totem-pole front-end ACDC converter.

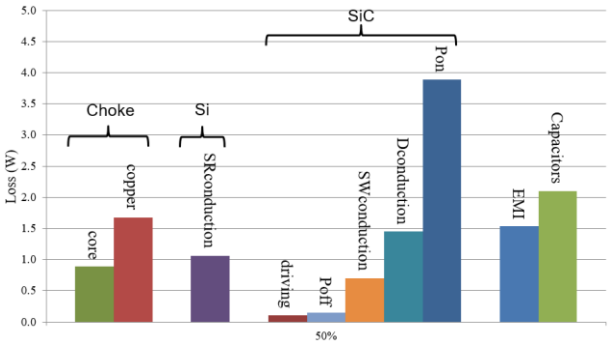

Fig. 4: Estimated overall distribution of loss in the totem-pole front-end PFC.

III. HALF-BRIDGE LLC

The back-end isolated DCDC is a half-bridge series-parallel resonant converter (LLC). The LLC can achieve Zero Voltage Switching (ZVS) in the primary side HV switches in all the load range. Moreover, the secondary side LV Synchronous Rectifiers (SRs) operate in ZVS but can be Zero Current Switched (ZCS) as well. Therefore,

the switching losses can be nearly eliminated. However, other loss phenomena due to the charge and discharge of the switches' capacitances could still have a noticeable contribution [11].

Table 2 includes a summary of the key specifications of the prototype. The nominal input voltage at which the converter achieves its best efficiency is 410 V_{DC}, where the LLC operates slightly above the series resonance freqeuncy (93 kHz). It should be noted that, although the output voltage range is narrow (fixed 50 V_{DC}), due to the large hold-up time, the input voltage range is relatively wide (320 V_{DC} - 420 V_{DC}), therefore constraining the design.

Figure 5 is a summary of the estimated overall distribution of losses at 50 % of the rated power and at the nominal input and output voltages. It can be observed that the major contributions of losses are the main transformer, the secondary side SRs, and the primary side switches. Moreover, three different alternative semiconductor devices for the HV primary side devices are compared in Fig. 6. It is worth noting that due to their lower capacitances, the switching loss of the WBG devices is comparatively lower than that of the Si SJ MOSFETs.

Table 2: Key specifications of the LLC prototype.

Parameter	**Value**
Nominal input voltage	320 V_{DC} – 420 V_{DC}
Nominal output voltage	50 V_{DC}
Rated power	3 kW
Series resonant frequency	93 kHz
Series resonant inductor	6 µH
Parallel resonant inductor	65 µH
Resonant capacitor	480 nF
Transformer turn ratio	16:4
Primary MOSFETs	IPW60R024CFD7
SR MOSFETs	ISC031N08NM6

Figure 6 shows the estimated efficiency of the LLC converter stage at the nominal input and nominal output voltages, and along the load range. Moreover, the performance of the converter with three different alternative devices is compared. It can be observed that in spite of the different loss contributions (Fig. 5), the variation of the overall efficiency of the converter is relatively small at the somewhat low switching frequencies of this design.

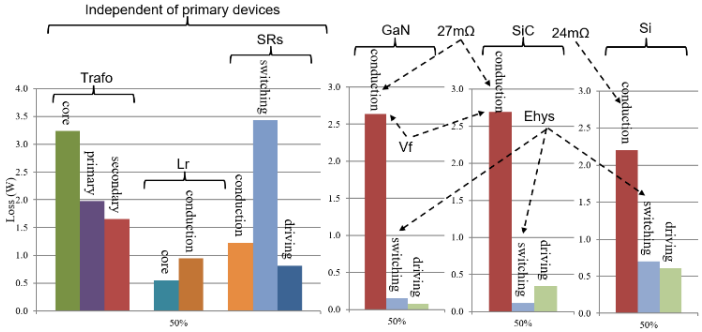

Fig. 5: Estimated overall distribution of loss of the back-end LLC DCDC converter.

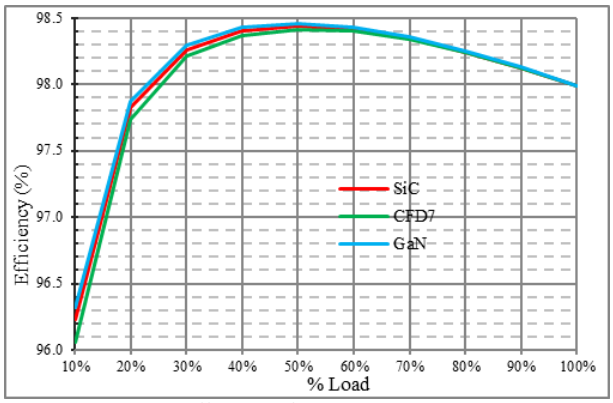

Fig. 6: Estimated efficiency of the back-end LLC DCDC converter.

It is worth highlighting that the efficiency of the complete PSU is the result of multiplying the respective efficiencies of the two stages (Fig. 3 and Fig. 5), and therefore necessarily lower than any of them. However, it shall be noted that some of the loss contributions appear only once in the complete PSU, e.g. capacitors current leakage and auxiliary circuitry.

A. **HALF-BRIDGE LLC MAGNETICS**

The resonant tank of the LLC converter comprises a series resonant inductor (L_r), a parallel resonant inductor (L_m) and a resonant capacitor C_r. One of the advantages of this topology is that L_r and L_m can be realized by the leakage and the magnetizing inductance of the main transformer. Although this alternative reduces the component count, it constrains the freedom of the design and the achievable performance of the converter. Therefore, in the prototype, the series inductor and the parallel inductor are built as discrete components. In the following, the construction of the magnetics will be further discussed.

1) SERIES RESONANT INDUCTOR

The series inductor is constructed with a PC95 PQ35/13 DG core from TDK and six turns of Litz wire (245 strands of diameter 0.1 mm). The multiple small gaps in the ferrite core's central column help reduce the losses caused by the stray fields in the winding and in the surrounding conductors. A spacer (represented in beige in Fig. 7) maintains the winding away from the remaining gaps between the PQ and the I piece (Fig. 7).

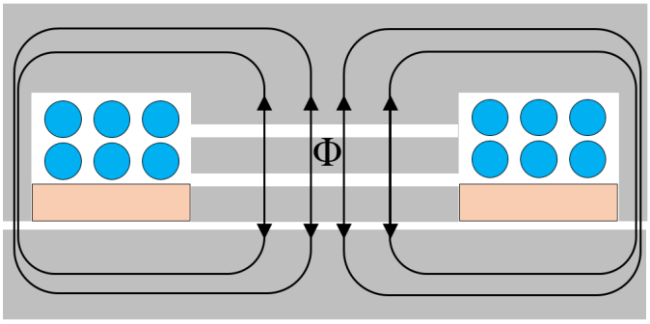

Fig. 7: Simplified construction structure of the series resonant inductor of the LLC DCDC converter.

2) MAIN TRANSFORMER AND PARALLEL INDUCTOR

The main transformer and the parallel resonant inductor (L_m) have been integrated into the same structure (Fig. 8). In this structure, the flux in part of the volume is effectively canceled, therefore, reducing the total core loss. L_m is made of a PC95 PQ35/28 core from TDK and 16 turns of Litz wire (512 strands of diameter 0.05 mm). A spacer maintains the winding away from the gaps, therefore reducing the loss caused by the stray fields.

The main transformer is made of two PC95 PQI35/23 cores from TDK and four separate planar PCB windings for the primary (in blue in Fig. 8) and eight planar PCB windings for the secondary (in green in Fig. 8).

One of the main advantages of the separation between the parallel resonant inductor and the main transformer is the improved coupling of the transformer. The magnetizing inductance of the main transformer can be made arbitrarily high. Therefore, the magnetizing current becomes neglectably small. On the one hand, this reduces the proximity losses, especially important in planar windings. On the other hand, the gap of the main transformer is virtually zero, therefore, reducing the effect of the stray fields, also very harmful in planar windings.

One of the main disadvantages of this approach is the loss caused by the additional core volume. However, in this design, the improvement in the conduction loss is larger than the additional loss caused by the core volume, therefore becoming the preferred solution.

Figure 9 represents the structure of the planar PCB windings. The FR-4 material is represented in blue, and the copper is represented in green. The primary side HV winding requires safety isolation; therefore, demanding the double FR-4 layer in the outer sides and the large margin to the lateral walls (1 mm). The secondary side windings only require functional isolation to the core; therefore, less margin to the lateral walls is required (0.5 mm). It follows that a large percentage of the transformer window is taken by the insulation. Moreover, the kind reader may observe that for smaller transformer geometries (smaller cores), the portion of the window consumed by the insulation increases.

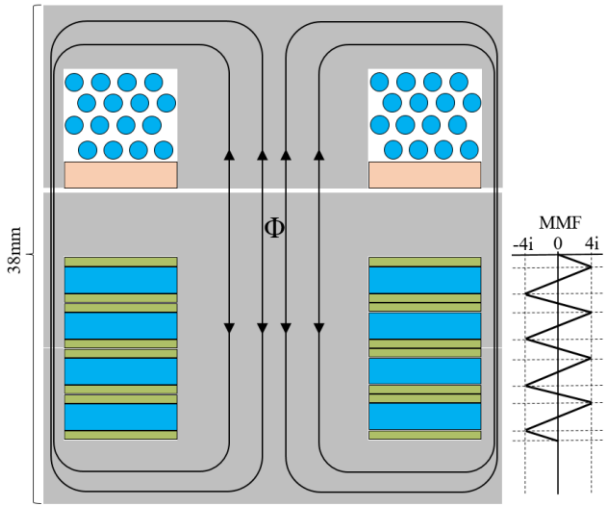

Fig. 8: Simplified construction structure of the integrated transformer plus the parallel resonant inductor of the LLC DCDC converter.

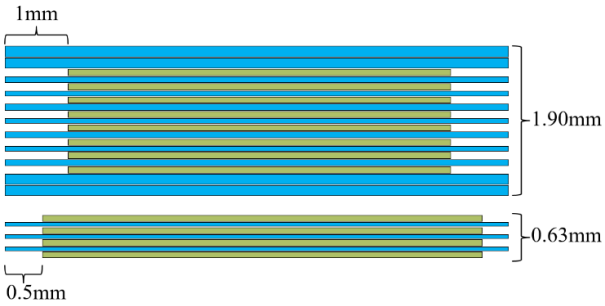

Fig. 9: Simplified cross-section of a primary side winding PCB (upper) and a secondary side winding PCB (lower).

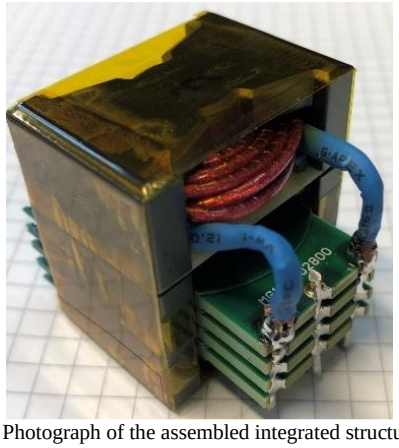

Fig. 10: Photograph of the assembled integrated structure of the transformer and the parallel resonant inductor.

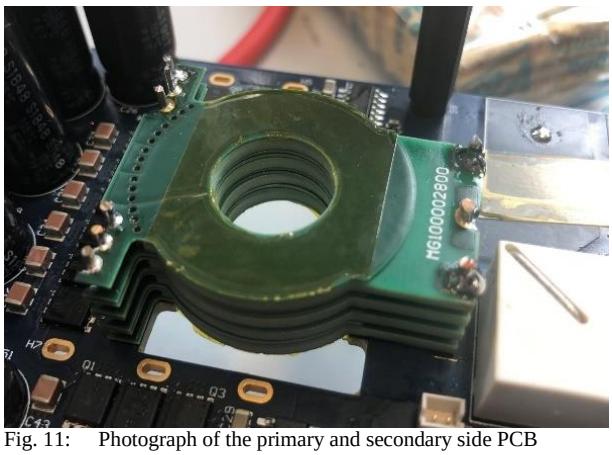

Fig. 11: Photograph of the primary and secondary side PCB windings of the planar transformer soldered onto the main board.

Figure 10 and Fig. 11 show two different assembly stages of the main transformer and the integrated parallel resonant inductor. It can be observed that due to the height constraints of the converter (40 mm), the main PCB needs to be cut out (the transformer's total height is 38 mm).

IV. EXPERIMENTAL RESULTS

This section summarizes the main experimental results of the two separate conversion stages and the complete PSU.

A. **TOTEM-POLE PFC**

It was already discussed in previous sections that one of the major contribution of loss in the totem-pole PFC are the switching losses of the boost switch and boost diode. Aiming to reduce the switching loss in this converter, Q_3 and Q_4 are devices with Kelvin-source connection (IPZA65R048M1) that cancel the otherwise negative feedback in the gate driving loop caused by the power source of the package, and therefore enabling a faster turn-on and turn-off.

Nevertheless, the switching speed of the devices still needs to be controlled due to the remaining parasitic inductances in the commutation loop, which may cause undesirably high overshoots in the drain or excessive ringing in the gate. It can be observed in Fig. 12 that the stress in the devices is well within the rated limits at the worst case (maximum load). Note that the drain (V_{DS}) and the gate (V_{GS}) voltage were measured referenced to the Kelvin-source connection.

Figure 13 offers a detailed view of the V_{AC} zero crossing where the polarity of the SRs (Q_1 and Q_2) changes. The idle time at the zero crossing shall be kept relatively narrow for improved THD of the converter.

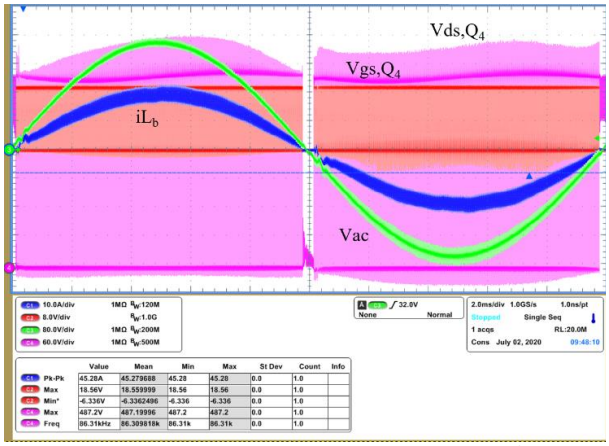

Fig. 12: PFC drain voltage overshoot and gate ringing at full load.

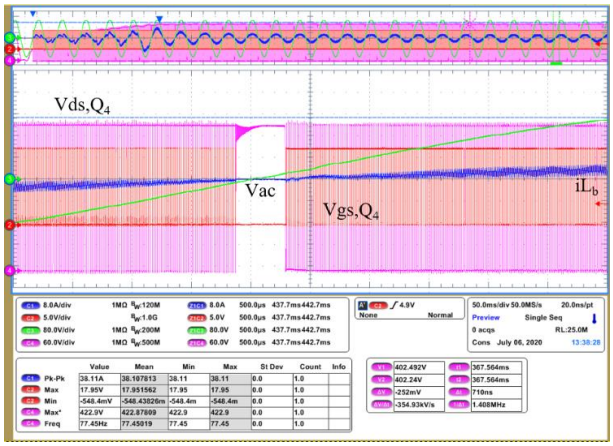

Fig. 13: Detailed view of the V_{AC} zero crossing in the PFC totem-pole.

B. **LLC DCDC**

In Fig. 14, it can be observed that the primary side devices achieve ZVS relatively easily at all load ranges. Thanks to the relatively small parallel resonant inductor (65 µH), which is required due to the extended hold-up time, the magnetizing current is large enough to provide energy for the full ZVS even without load current (light load) [12].

Figure 14 also demonstrates the very small overshoot in the secondary side SRs. The LLC does not require a filter inductor at the output of the rectification stage. Therefore, filtering capacitors can be placed directly after, effectively clamping the commutation overshoot and enabling the best voltage class for the rectifiers (ISC031N08NM6, which are 80 V devices).

The clamping diodes D_1 and D_2 (Fig. 2) are not strictly required for the operation of the half-bridge LLC. However, they provide protection features, e.g. effectively limiting the peak current through the converter during spurious over-load events. On the other hand, the clamping diodes effectively limit the maximum achievable gain of the converter. Moreover, at the lower input voltages, the allowed voltage excursion in C_r further decreases (Fig. 15). This needs to be considered during the design and the sizing of C_r.

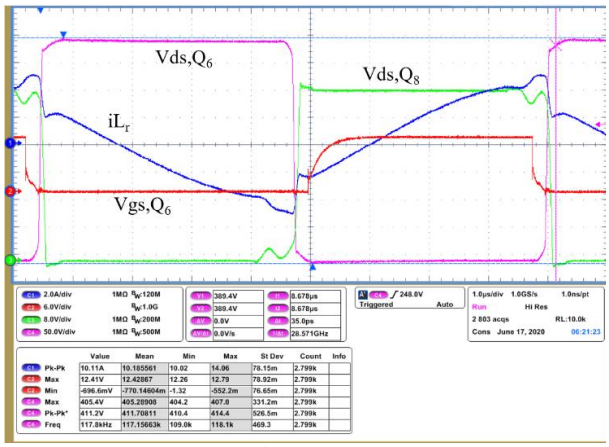

Fig. 14: Full ZVS at 10% of the rated load.

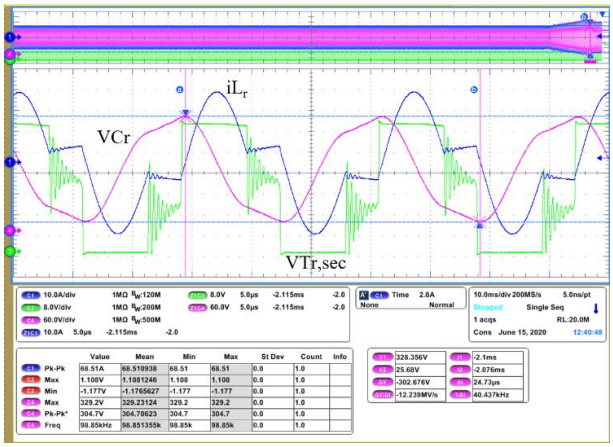

Fig. 15: Clamping diodes limit the maximum VC_r voltage amplitude, and therefore the gain of the converter.

1) TEMPERATURE

Figure 16 shows a temperature capture of the complete PSU at full load and at 230 V_{AC} input. It should be noted that the capture was taken with the PSU out of its chassis and with an auxiliary fan at the side.

Mainly two hot areas can be identified that correspond to the SiC switches in the totem-pole (upper-right area), and the main transformer and the secondary side SRs (lower-left area). This further corroborates the estimated overall distribution of losses discussed in the previous sections.

Further temperature measurements were captured with the PSU inside of its chassis, cooled by the PSU internal fan, and after running the PSU at full load for 30 min. The results of the main hot spots are represented in Fig. 17. In further revisions, to increase the safety margin in the SRs, two additional heat-sinks will be added and one of the output capacitors removed for improved airflow. It is worth mentioning that in this PSU, unlike in the most common cases, the fan blows into the unit, carrying hot air from the PFC into the DCDC stage.

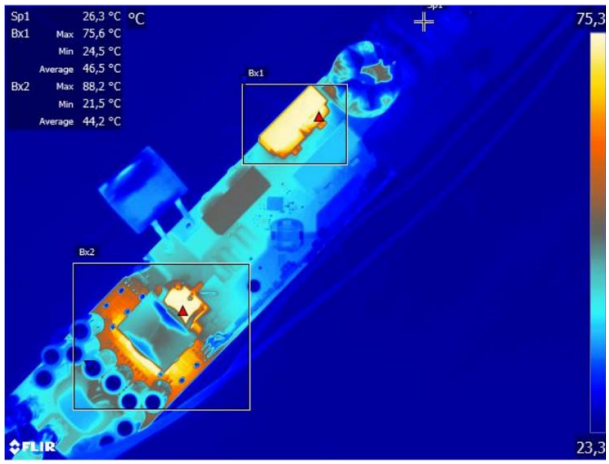

Fig. 16: Measured temperature of the complete power supply prototype at 230 V_{AC}.

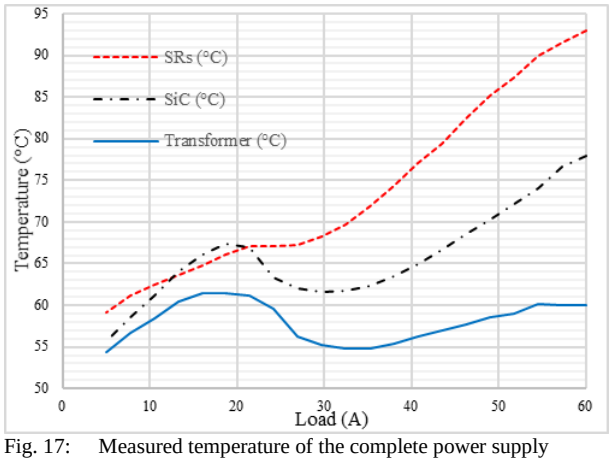

Fig. 17: Measured temperature of the complete power supply prototype at 180 V_{AC}.

C. *EFFICIENCY*

The efficiency of the complete power supply was measured at 230 V_{AC} with the fan supplied externally as well as by the PSU itself (as required by the OCP v3 specification). The results are represented in Fig. 18, together with the efficiency requirements at 230 V_{AC} given by the specifications

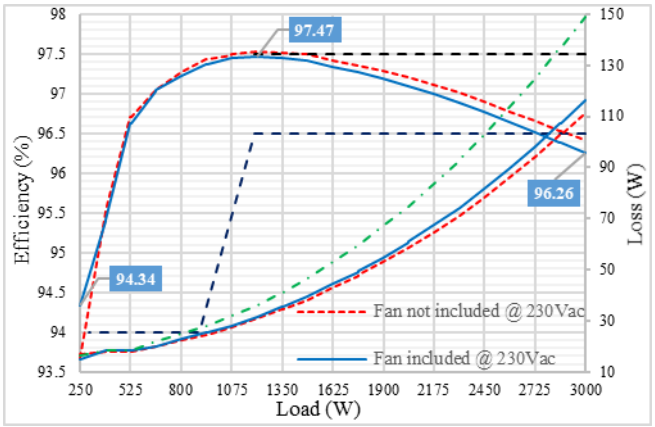

Fig. 18: Measured efficiency of the complete power supply prototype at 230 V_{AC}.

Although the efficiency at 10 % exceeds the requirements, and the efficiency at 50 % load is very close to the target, the efficiency at full load falls below the minimum by nearly 0.14 %. Further revisions of the converter with improvements in the conduction and switching losses are still needed.

V. CONCLUSION

In 2019 the Open Compute Project released a draft of the third version of the OCP rectifier specifications. The main changes between this version and the previous ones are the higher output voltage (50 V_{DC}), the higher power density (3 kW), and the efficiency requirements (97.5 % at 230 V_{AC}). Moreover, although the output voltage range is narrow, due to the large hold-up time (20 ms), the input voltage range of the back-end DCDC stage of the PSU is still wide.

Therefore, the design of a complete PSU compliant with the specifications is a challenging task. The preliminary analysis shows that the best alternative is a PSU comprised of two stages: a front-end bridgeless totem-pole PFC ACDC converter followed by a back-end half-bridge series-parallel resonant (LLC) isolated DCDC converter.

The complete power supply has been built and tested, achieving a peak efficiency of 97.47 %. The analysis of the results and the thermal captures shows that the main contributions to the overall losses are the main transformer of the LLC, the switching losses of the SiC MOSFETs in the PFC, and the switching losses of the secondary side SRs in the LLC.

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SECTION III. PATENTS

CHAPTER 12. FREQUENCY MODULATION OF PSFB FOR INPUT VOLTAGE RANGE EXTENSION

1. INTRODUCTION

In PSFB converters the range of ZVS is given by the energy stored in the magnetics L_r, L_{lkg}, L_o and L_m. The two bridge legs (Q_1, Q_2, Q_3 and Q_4 in Figure 1) behave differently during the switching transitions. One of the legs turns on/off after a power transfer primary to secondary (lagging the power transfer, Figure 2), while the other leg turns on/off before the following power transfer (leading the power transfer, Figure 2).

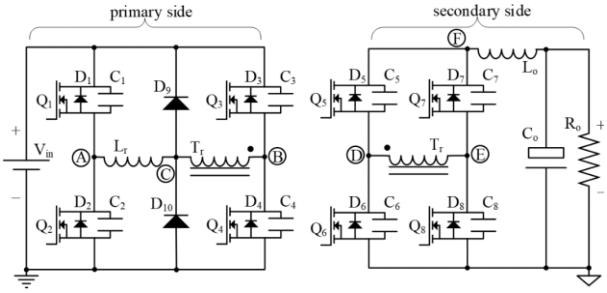

Figure 1. Simplified model of a phase shift full bridge with equivalent parasitic capacitances and inductances.

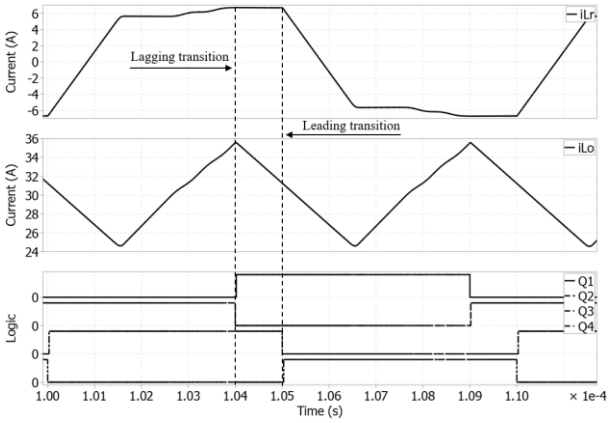

Figure 2. Lagging and leading power transfer transitions of the full bridge switches.

1.1. LEADING LEG

The leading leg (in this example Q_3 and Q_4) transition occurs before a power transfer from the primary side to the secondary side and after the freewheeling phase (Figure 3). Because during the freewheeling phase the transformer is effectively shorted by the rectification stage, the output filter inductance and the magnetizing inductance of the transformer do not contribute to this transition (Figure 3). The energy available for charging-discharging the parasitic capacitances of the leading leg half bridge can be calculated with (5).

$$E_{leading} = \frac{I_{Lr}^2 L_r + I_{Llkg}^2 L_{lkg}}{2} \quad (1)$$

Q_{oss} stands for the charge stored in the output capacitance one of the HV bridge devices, to which we may have to add other stray capacitances of the half bridge node for a more accurate result. For achieving full ZVS on the leading leg the available energy should be big enough to discharge the capacitance of the device which was off and to charge the capacitance of the device turning-off (2) [1].

$$Q_{oss} V_{in} \leq \frac{I_{Lr}^2 L_r + I_{Llkg}^2 L_{lkg}}{2} \quad (2)$$

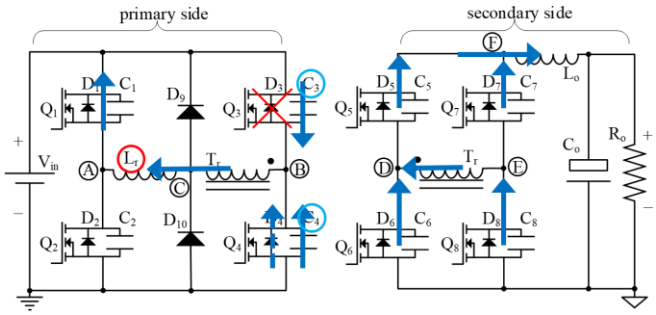

Figure 3. Leading leg transition. Switch Q_3 has turned-off and the energy of the inductances flows into the parasitic capacitances until the parallel diode of D_4 conducts enabling ZVS of Q_4.

In this leg ZVS does not occur easily along all the load range and requires careful design of the transformer and/or external resonant inductances. In general increasing L_r, L_{lkg} or reducing L_m (because it will effectively increase current through L_r and L_{lkg}) will increase the available energy. However, both approaches have their tradeoffs:

- Decreasing L_m increases primary circulating current and conduction losses.
- Increasing L_r, L_{lkg} reduces the available duty cycle and limits the maximum load at which the converter can regulate.

1.2. LAGGING LEG

The lagging leg (in this example Q_1 and Q_2) transition occurs right after a power transfer from the primary side (input side of the converter) to the secondary side (rectification stage). Because during this transition the filter inductance L_o is effectively connected to the bridge through the transformer (Figure 4), it also contributes to the quasi-resonant transition. The energy available for charging-discharging the parasitic capacitances of the lagging leg half bridge can be calculated with (3).

$$E_{lagging} = \frac{I_{Lr}^2 L_r + I_{Lm}^2 L_m + I_{Lo}^2 L_o + I_{Llkg}^2 L_{lkg}}{2} \tag{3}$$

For achieving full ZVS of the lagging leg the available energy should be larger than the energy required to move the stored charge into the input supply (4).

$$Q_{oss} V_{in} \leq \frac{I_{Lr}^2 L_r + I_{Lm}^2 L_m + I_{Lo}^2 L_o + I_{Llkg}^2 L_{lkg}}{2} \tag{4}$$

For a step down converter (where there are more primary turns than secondary turns in the transformer, $N_p > N_s$) the contribution of energy by the output filter inductance is in general much larger than the contribution by the other inductances, so ZVS is usually easily achieved through all the load range for this leg. $L_{o,pri}$ stands for the equivalent reflected value of the output filter inductance through the transformer (5-6). Replacing (6) in (3) we can derive the relation in (7), which proves that the available lagging leg energy (3) is always much bigger than the leading leg energy (1).

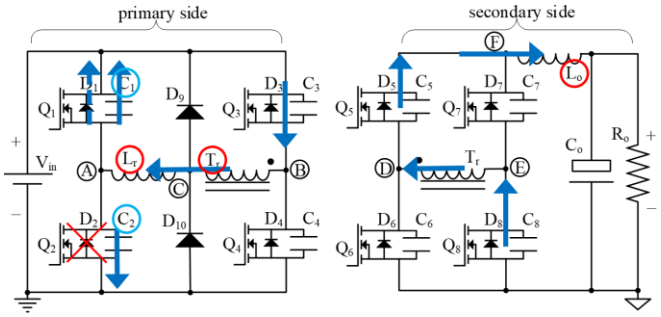

Figure 4. Lagging leg transition. Switch Q_2 has turned-off and the energy of the inductances flows into the parasitic capacitances until the parallel diode D_1 conducts enabling ZVS of Q_1.

$$n = \frac{N_p}{N_s} \tag{5}$$

$$L_{o,pri} = L_o n^2 \tag{6}$$

$$\frac{I_{Lm}^2 L_m + (I_{Lr} - I_{Lm})^2 L_{o,pri}}{2} \gg \frac{I_{Lr}^2 L_r + I_{Llkg}^2 L_{lkg}}{2} \tag{7}$$

1.3. DUTY CYCLE LOSS

The effective duty cycle of the converter depends only on the input voltage, the output voltage and the transformer turns ratio. Therefore the effective duty is constant along the load range (8), dismissing the minor effects of the circuit voltage drops at the higher currents.

$$duty_{effective} = \frac{V_o}{V_{in}} n \tag{8}$$

The duty cycle loss occurs due to the time it takes to the primary current to reverse polarity along L_r and L_{lkg}, and reduces the available freewheeling time (Figure 6). Therefore, the remaining freewheeling time depends on load, because the primary current is the sum of the reflected secondary current plus the transformer magnetizing current (9-11). Should be noted that the freewheeling duty has to be always bigger than or equal to zero for the converter to maintain regulation (Figure 5).

$$duty_{loss} = \frac{L_r + L_{lkg}}{V_{in}} \Delta I_p 2 F_{sw} \tag{9}$$

$$\Delta I_p = \frac{2\overline{I_o}}{n} \tag{10}$$

$$\text{duty}_{freew} = 1 - \text{duty}_{loss} - \text{duty}_{effective} \quad (11)$$

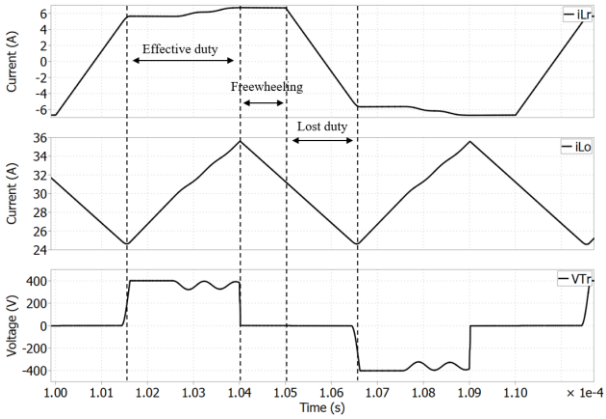

Figure 5. Freewheeling time at medium load with plenty of regulation room available.

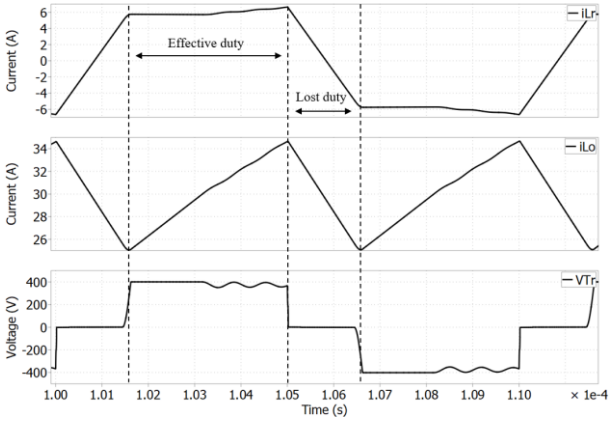

Figure 6. Extreme case where there is no more regulation room available.

1.4. TRADEOFF BETWEEN PERFORMANCE AND HOLD-UP TIME

From the point of view of performance, it would be desirable to design the converter for having zero freewheeling time at full load, due to the following reasons:

- Maximum ZVS range for the full bridge (specifically for the leading leg), maximizing the size of L_r and L_{lkg}.
- Minimum freewheeling time causing less circulating current in primary side.
- Maximum effective duty, maximizing the transformer turn ratio and lowering the secondary side reflected voltage and consequently having better secondary side voltage class switches (better FoM).

However, in a full ACDC converter the design has to ensure that the DCDC stage can maintain output regulation at full load during a specified hold-up time (time during which the AC input voltage is missing). During hold-up time, the output voltage of the primary ACDC stage will drop (e.g. from 400V to 350V). The DCDC stage has to maintain regulation at full load within that input voltage range (Figure 7). It was previously analyzed that the available duty cycle depends on the input voltage (9). In consequence, from the point of view of the hold-up time specification, the transformer turns ratio, L_r and L_{lkg} has to be dimension for the lowest input voltage, effectively decreasing the maximum possible performance at the nominal conditions.

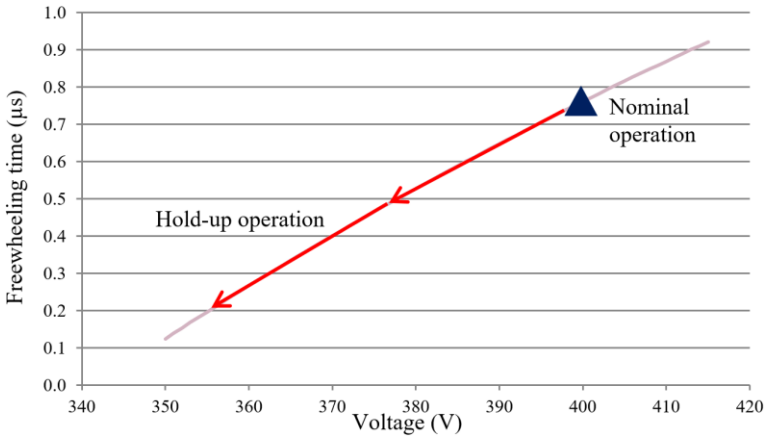

Figure 7. Variation of freewheeling time at full load (available duty cycle) at different input voltages when all other parameters fixed. Standard hold-up operation. Sweeping voltage with a fixed L_r (11.1 µH) at 100 kHz switching frequency.

2. FREQUENCY MODULATION FOR INPUT VOLTAGE RANGE EXTENSION

The effective duty time can be calculated from (8) considering that the effective frequency at the output of the converter is twice the switching frequency of the primary side half-bridges (12). The same applies to the duty loss time which can be calculated from (9) dividing by twice the switching frequency and resulting in (13). Therefore, from (11) it can be derived the expression for the available regulation time (freewheeling time) as a function of the switching frequency (14). The expression can be further simplified into the equation (15), where it can be observed that, all other parameters fixed, freewheeling time increases when the switching frequency decreases.

$$\text{duty}_{\text{effective,time}} = \frac{\text{nV}_o}{\text{V}_{in}2\text{F}_{\text{sw}}} \quad (12)$$

$$\mathrm{duty}_{\mathrm{loss,time}} = \frac{\mathrm{L}_r + \mathrm{L}_{lkg}}{\mathrm{V}_{in}} \Delta \mathrm{I}_p \tag{13}$$

$$\mathrm{duty}_{\mathrm{freew,time}} = \frac{1}{2\mathrm{F}_{\mathrm{sw}}} - \mathrm{duty}_{\mathrm{loss,time}} - \mathrm{duty}_{\mathrm{effective,time}} \tag{14}$$

$$\mathrm{duty}_{\mathrm{freew,time}} = \frac{\mathrm{n}^2 \mathrm{V}_o - \mathrm{n}\mathrm{V}_{in} + 4\overline{\mathrm{I}_o}\mathrm{L}_r\mathrm{F}_{\mathrm{sw}}}{2\mathrm{n}\mathrm{V}_{in}\mathrm{F}_{\mathrm{sw}}} \tag{15}$$

For the PSFB design in Figure 1 the freewheeling time dependency on the switching frequency at different input voltages has been plotted in Figure 8. The core of the proposed technique is to vary the switching frequency of the converter to compensate for the loss of duty cycle due to the drop in the input voltage (e.g. during hold-up time). This would allow the design for optimal performance at nominal conditions while fulfilling the hold-up time requirements. The expression (15) can be rewritten to calculate the required switching frequency to maintain regulation based on the design parameters, load, input voltage and output voltage (16).

$$\mathrm{F}_{\mathrm{sw}} = \frac{\mathrm{V}_o \mathrm{n}^2 - \mathrm{V}_{in}\mathrm{n}}{4\overline{\mathrm{I}_o}\mathrm{L}_r + 2\mathrm{n}\mathrm{V}_{in}\mathrm{duty}_{\mathrm{freew,time}}} \tag{16}$$

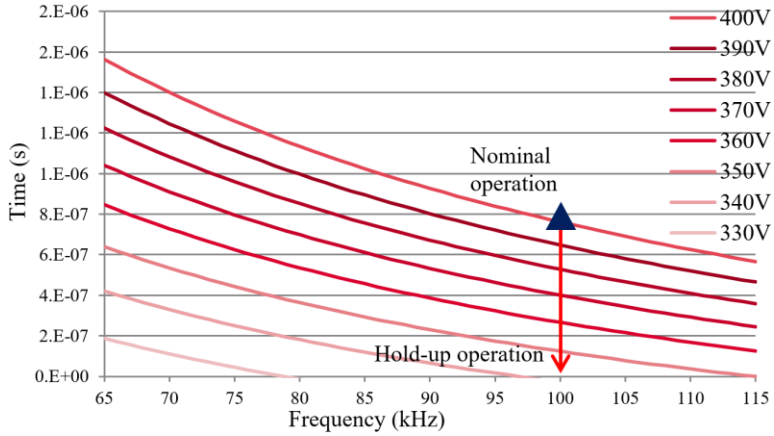

Figure 8. Variation of freewheeling time at different switching frequencies and voltages when all other parameters are fixed. The arrow indicates the frequency trajectory of standard modulation in Figure 7. Sweeping the switching frequency with a constant L_r (11.1 µH).

Thanks to this technique, L_r, L_{lkg} can be increased up to zero freewheeling time at the maximum possible load at the nominal input voltage. Alternatively, the turn ratio of the transformer can be modified for a longer duty and lower secondary reflected voltage. This technique can bring these benefits to the system:

- Improved ZVS range for the full bridge (especially for the leading leg), reducing switching losses at light load.
- The magnetizing current can be reduced, as L_r and L_{lkg} can provide more energy for the transitions, therefore reducing conduction losses.
- Minimize the freewheeling time, therefore decreasing the circulating currents in the primary side and reducing the conduction losses.
- Maximize the effective duty, therefore lowering the secondary side reflected voltage and allowing better secondary side voltage class switches.

2.1. PRACTICAL IMPLEMENTATION

In one possible implementation of the proposed modulation technique the controller modifies the switching frequency of the converter as a function of the input voltage. The dependency of the switching frequency on the input voltage can maintain (but not necessarily) a constant freewheeling time or apply some other non-linear frequency variation schemes, which includes the following alternatives:

- Switch to a minimum switching frequency under certain input voltage threshold (e.g. Trajectory B in Figure 9 and Figure 10).
- Decrease the switching frequency proportionally to the input voltage variation (e.g. Trajectory A in Figure 9 and Figure 10).
- Follow some other arbitrary trajectory varying frequency as a function of one or more of the variables in equation (16).

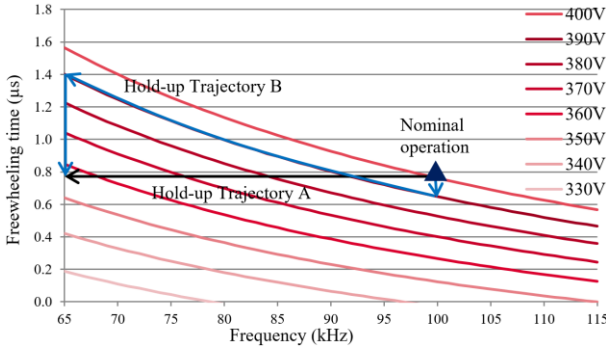

Figure 9. Example of possible frequency trajectories. Sweeping the switching frequency with a constant Lr (11.1 µH).

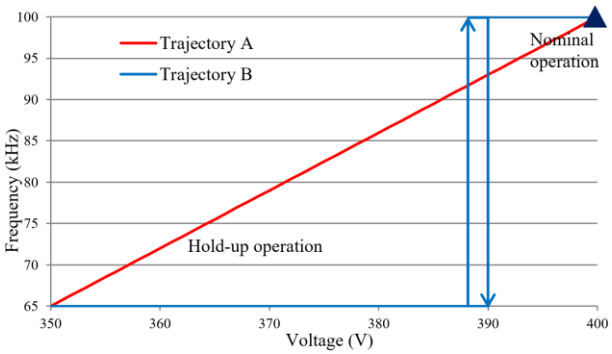

Figure 10. Example of frequency trajectories. Trajectory A maintains constant freewheeling time. Trajectory B implements two input voltage windows with two different switching frequencies.

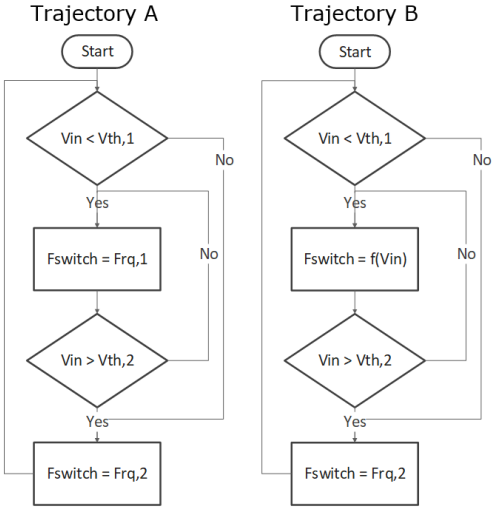

Figure 11. Example of frequency trajectory algorithms. Trajectory A sets the switching frequency at different discrete values within different ranges of the input voltage. Trajectory B sets the switching frequency as function of the input voltage or at a discrete value (nominal frequency) out of certain range of input voltage.

A digital controller can modify the switching frequency in relation to the input voltage whenever the input voltage measurement is available. Alternatively the input voltage can be estimated out of other measurements (e.g. reflected secondary voltage). In case that an analog controller is used, external circuitry can be added to provide the proposed switching frequency variation depending of the input voltage. How to implement this solution would depend of the specific analog controller being used and is out of the scope of this work. Figure 11, Figure 12 and Figure 13 show simplified diagrams of the proposed practical implementations.

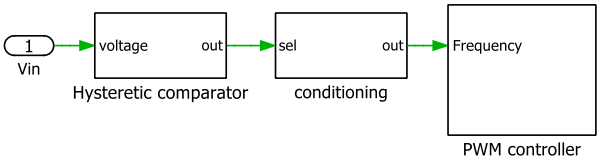

Figure 12. Simplified example of Trajectory A implemented with analog circuit blocks. PWM controller with at least one frequency setting input (observe that the controller would have more inputs and outputs, as needed).

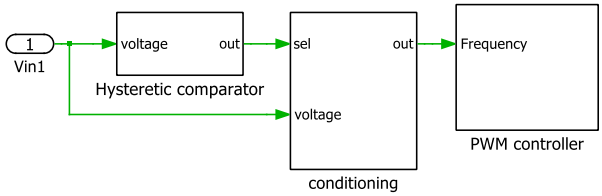

Figure 13. Simplified example of Trajectory B implemented with analog circuit blocks. PWM controller with at least one frequency setting input (observe that the controlled would have more inputs and outputs, as needed).

3. SIMULATION RESULTS

In the following we compare an optimized design with standard modulation to an optimized design applying the proposed new modulation:

- The standard design implements L_r = 8.5 µH and a transformer ratio of 21:4 for having enough available duty at the minimum input voltage (350 V) (Figure 14). The reflected secondary voltage is 76.19 V at nominal conditions. Consequently the required SRs rated voltage class is at least 120 V.

- The proposed design applying the proposed modulation technique implements L_r = 8.5 µH and a transformer ratio of 24:4 for having enough available duty at the minimum input voltage (350 V) (Figure 15) and the minimum desired switching frequency (43 kHz). The reflected secondary voltage is 66.66 V at nominal conditions. Consequently the rated voltage class of 100V could be used for the SRs.

At nominal conditions the estimated performance of the proposed design exceeds that of a standard design around 0.2-0.5 % of efficiency along all the load range (Figure 16).

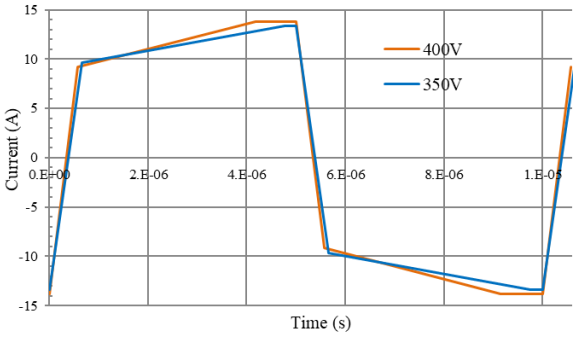

Figure 14. Transformer primary current at different input voltages for standard modulation scheme with a transformer ratio 21:4 and L_r equal to 8.5 µH

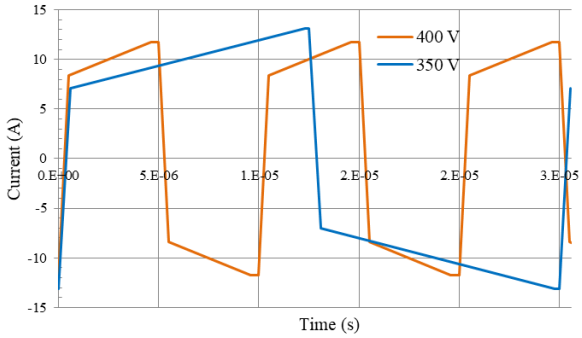

Figure 15. Transformer primary current at different input voltages for the proposed modulation scheme with a transformer ratio 24:4 and L_r equal to 8.5 µH.

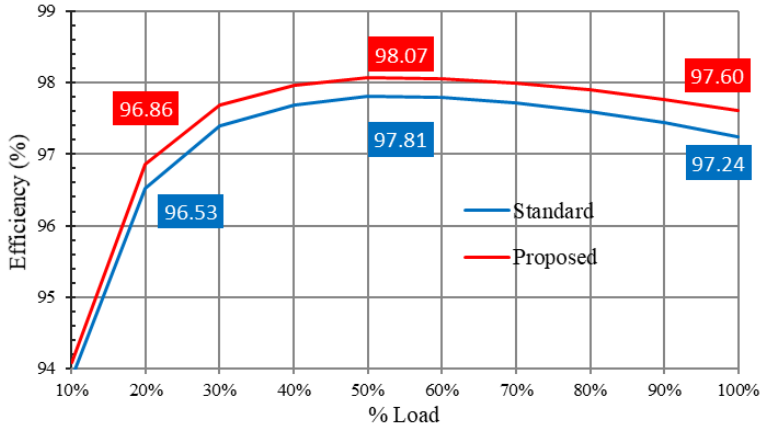

Figure 16. Effect of the proposed modulation technique on the design optimization of a 3300 W PSFB design. Efficiency estimation including the fan and the auxiliary bias consumption.

4. CONCLUSIONS

The proposed modulation technique in this chapter decreases the switching frequency of the PSFB DCDC converter to compensate for the loss of duty cycle due to the drop in the input voltage (e.g. during hold-up time). The proposed control scheme allows the design of PSFB for its optimal performance at the nominal operating conditions while fulfilling the specifications for hold-up time. Alternatively, the proposed control scheme allows increasing the input voltage regulation range and/or the output voltage regulation range.

The proposed modulation technique in this chapter is patent pending, and the application has been already published [2].

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[2] M. Escudero, M. Kutschak, inventors; Infineon Technologies Austria AG, assignee. Frequency Modulation Control for Phase-Shift Full Bridge Converters. United States patent application 16/362138. March 22, 2019

CHAPTER 13. MODULATION SCHEME FOR THE RESET OF CIRCULATING CURRENT IN PSFB

1. INTRODUCTION

The PSFB is a buck derivate, isolated DCDC converter topology. Like other resonant or quasi-resonant converters it can achieve ZVS in the primary side devices. However, unlike other fully resonant topologies (LLC or DAB) it suffers of circulating current losses in the primary side during the so-called freewheeling phase that do not contribute to the power transfer to the secondary side.

An example of a standard PSFB configuration is given in Figure 1. The problem and solution discussed in this chapter applies both for passive (diode) or active rectification (synchronous rectifiers). For simplicity we will assume diode rectification in the following examples. As discussed in previous chapters, the clamping diodes in the primary side (D_1 and D_2) help reducing the voltage overshoot of the secondary side rectifiers. Table 1 is a summary of the key component values that have been used in the simulations to obtain the results in this chapter.

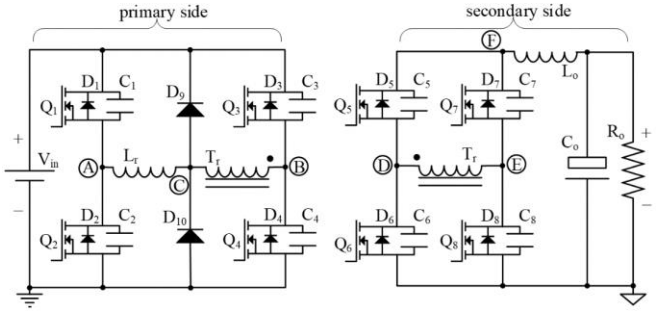


Figure 1. PSFB DCDC converter with clamping diodes in the primary and diode rectification.

Table 1. Summary of component values in the simulations.

Component	Parameter	Value
Q_1-Q_4	$R_{ds,on}$	37.5 mΩ
D_1-D_2	V_f	1 V
Q_5-Q_8	$R_{ds,on}$	2.32 mΩ
Transformer primary	Turns	21
Transformer secondary	Turns	4
L_r	Inductance	2.3 µH
L_o	Inductance	9.8 µH

1.1. PRIMARY SIDE CIRCULATING CURRENTS IN PHASE SHIFT FULL BRIDGE CONVERTERS

The standard modulation of PSFB converter is widely covered in the literature [1]. Figure 2 shows the main waveforms of the converter operating at full load and at the nominal input voltage. The modulation scheme is briefly summarized in Figure 3. In this condition there are circulating currents in the primary side during the freewheeling time. Moreover the clamping diodes D_1 and D_2 conduct two times per period.

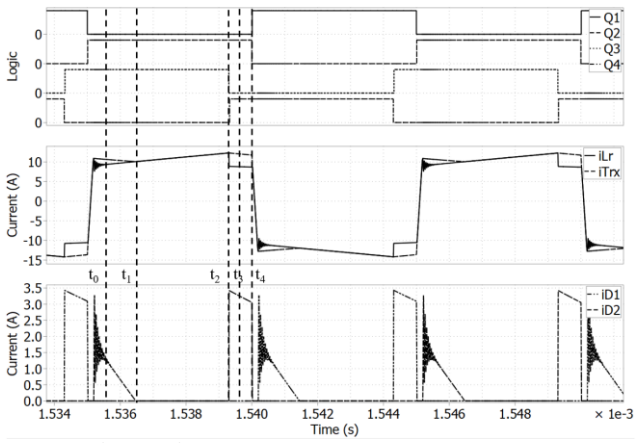


Figure 2. Converter waveforms at full load, nominal input voltage (400 V) and nominal output voltage.

The circulating currents are especially significant in wide input and/or wide output PSFB DCDC converters. Although the wide input voltage range can be reduced increasing the bulk capacitance between the ACDC (PFC) stage and the DCDC isolated output stage, it is however at the expense of cost and volume, which is not practical.

Other fully resonant topologies like LLC can be fully optimized for its nominal operation. However, the secondary side *rms* currents are higher in LLC designs in comparison to PSFB. Therefore, reducing the primary side circulating currents in PSFB converters can potentially increase the performance of the topology at the level of fully resonant converters. Table 2 is a summary of currents through the main components of the converter for the standard modulation scheme and the example converter in Figure 2.

Table 2. Summary of *rms* currents for the example design at different input voltages.

	Minimum input (350 V)	Nominal input (400 V)
Q_1-Q_2 Irms (A)	8.29	8.45
Q_3-Q_4 Irms (A)	8.09	7.91
D_1-D_2 Iavg (A)	0.14	0.37
Transformer primary Irms (A)	11.50	11.26
Transformer secondary Irms (A)	60.12	58.26

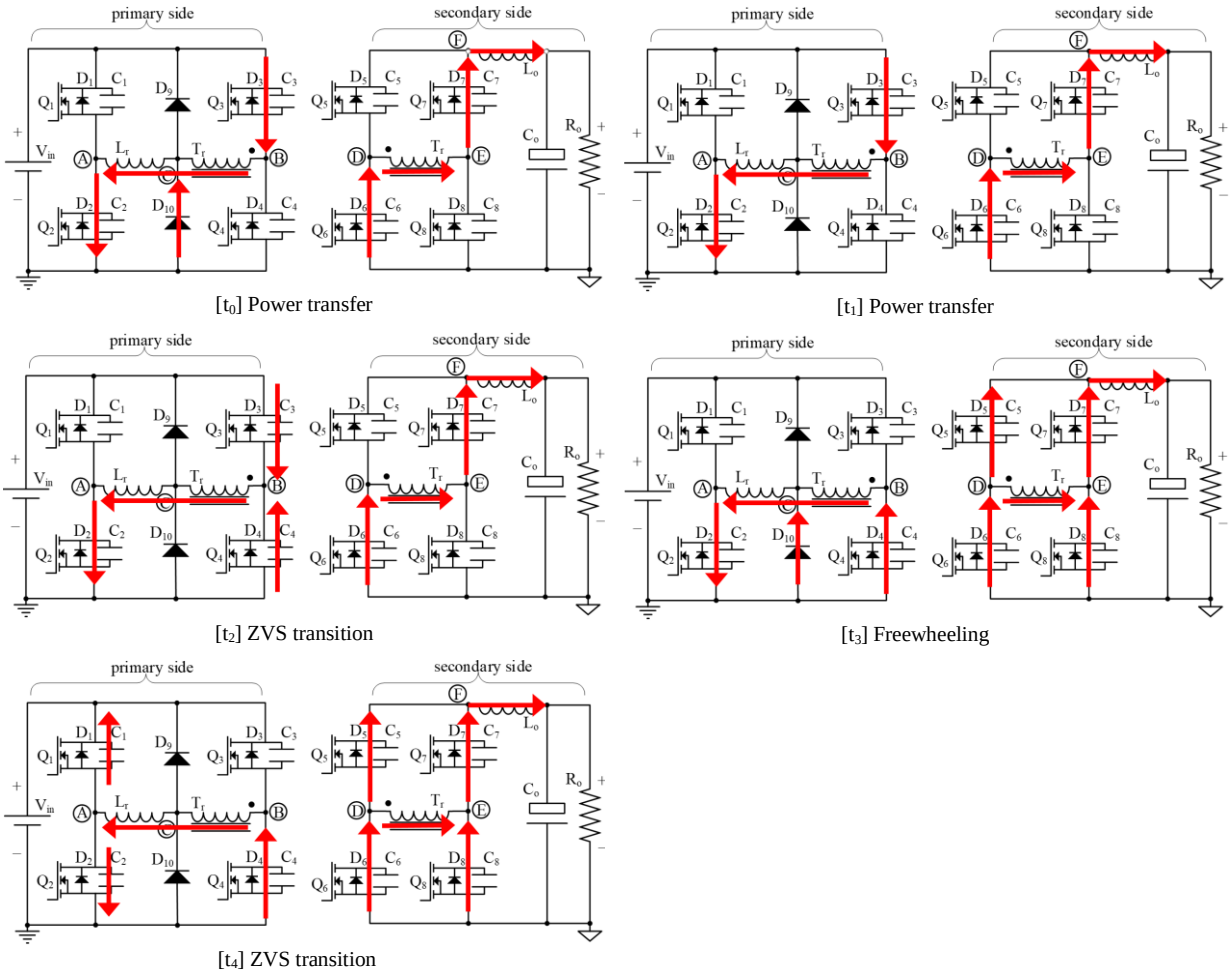


Figure 3. PSFB DCDC converter standard modulation scheme. Simplified power flow.

2. MODULATION SCHEME FOR THE RESET OF CIRCULATING CURRENTS IN PSFB

The newly proposed modulation scheme for PSFB converters resets the primary side circulating currents and provides ZCS for one of the primary side bridge legs. Figure 4 and Figure 5 show the main waveforms of the proposed modulation scheme (compare to Figure 2). In Figure 4, unlike in Figure 2, Q_2 is turned-off at the same instant than Q_3. The current flowing throw the primary side is therefore blocked by Q_2 and forced to discharge the output capacitance of Q_1. Because Q_2 has blocked the current circulation path, the circulating current resets to zero. Although, in practice there is a small current flow of reverse polarity by the resonance between the output capacitances of Q_1 and Q_2, and the inductances L_r and L_{lkg}.

Figure 6 summarizes the key operating modes for the proposed modulation scheme. Compare the simplified power flow in Figure 6 with the power flow of the standard modulation in Figure 3.

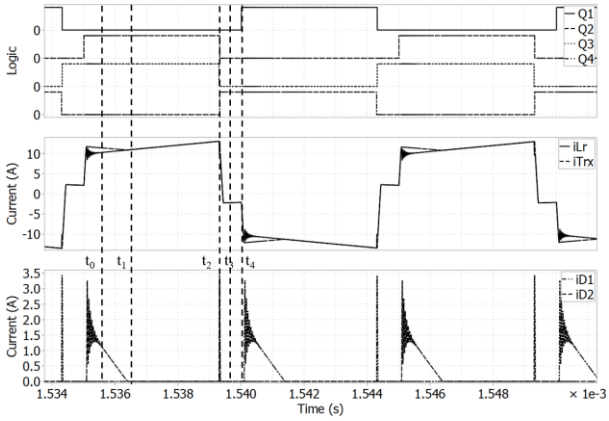


Figure 4. Full load at nominal input voltage (400 V) and nominal output voltage applying the proposed modulation scheme. Clamping diodes conduction.

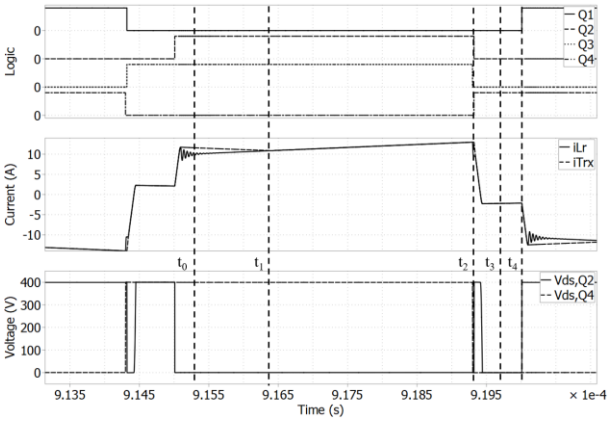
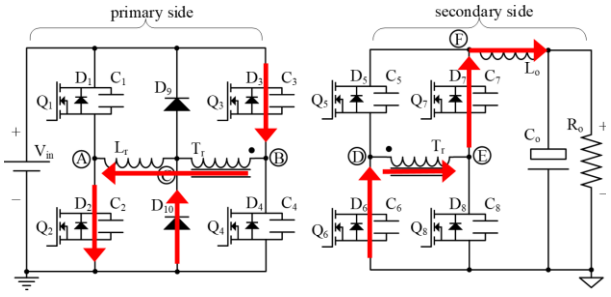
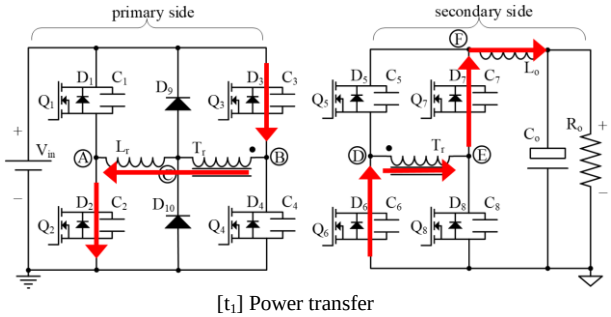


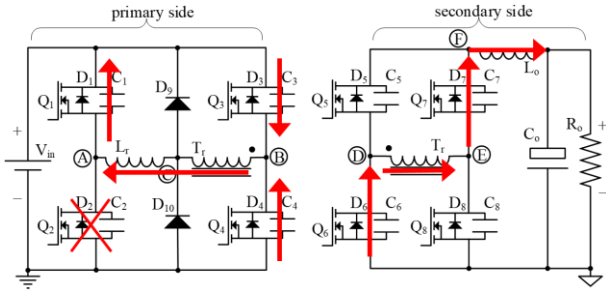
Figure 5. Full load at nominal input voltage (400 V) and nominal output voltage applying the proposed modulation scheme. HV MOSFETs ZVS transition in the lagging leg and hard commutated transition in the leading leg.



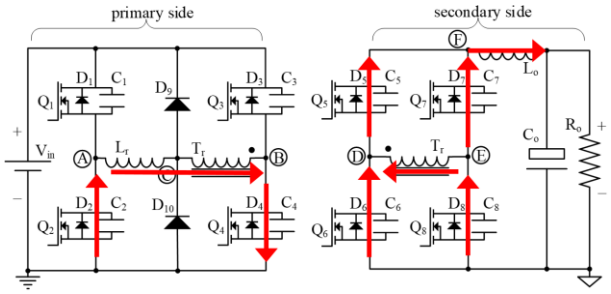
[t_0] Power transfer



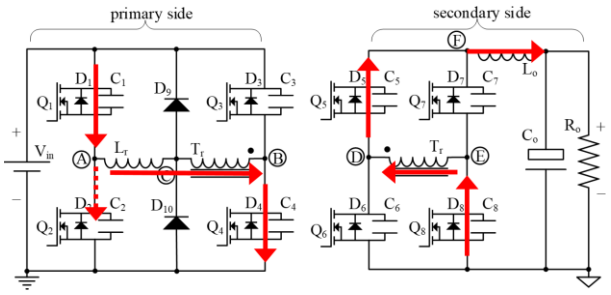
[t_1] Power transfer



[t_2] ZVS transition



[t_3] Freewheeling



[t_4] Hard commutation

Figure 6. PSFB DCDC converter proposed novel modulation scheme which resets primary side circulating currents. Simplified power flow.

Because Q_1 is still turned-off after Q_2 transition, L_r and L_{lkg} current resonates back and forward bias the body diode of Q_2. Because Q_2 body-diode would be conducting during Q_1 transition, Q_1 turns-on in hard-switching and hard-commutates D_2. It follows that for low output capacitance devices (e.g. Wide Band Gap devices) the circulating current would be closer to zero than in the case of SJ MOSFETs. Moreover, the reduced reverse recovery charge of WBG will decrease the related switching losses of the hard-commutated transition. Table 3 is a summary of the currents passing through the main components of the converter for the proposed novel modulation scheme, both at minimum and at nominal input voltages.

Table 3. Summary of *rms* currents for the example design at different input voltages with the proposed novel modulation scheme.

	Minimum input (350 V)	Nominal input (400 V)
Q_1-Q_2 Irms (A)	8.23	7.76
Q_3-Q_4 Irms (A)	8.02	7.54
D_1-D_2 Iavg (A)	0.11	0.12
Transformer primary Irms (A)	11.47	10.75
Transformer secondary Irms (A)	60	56.42

3. SIMULATION RESULTS

The proposed modulation scheme could be implemented with a standard PSFB controller and a few additional logic gates. As described above, Q_1 would be turned-off at the same instant than Q_3 turns-off, and Q_2 would be turned-off at the same instant than Q_4 is turned-off.

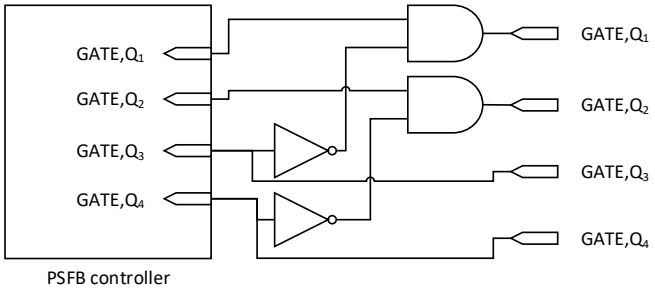


Figure 7. Simplified circuit blocks of a possible implementation of the proposed modulation scheme.

The captured waveforms in the figures as well as the estimated *rms* currents to illustrate the novel modulation scheme are obtained by simulation in PLECS [2]. Table 4 and Table 5 summarize the main conduction loss contributions for the standard modulation scheme and for the new proposed modulation scheme in the example converter and at the nominal input voltage. Overall the proposed modulation scheme achieves an estimated loss saving around 2.74 W. For the converter used as an example, where the losses at full load (3300 W) are in the range of 89.38 W, the estimated saving in power loss represents a reduction of 3% of the total losses.

Table 4. Standard modulation scheme. Conduction losses of the main components at the nominal input voltage (400 V).

	Nominal input (400 V)	$R_{ds,on}$ (mΩ)	Loss (W)
Q_1-Q_2 Irms (A)	8.45	37.5	5.36
Q_3-Q_4 Irms (A)	7.91	37.5	4.70
D_1-D_2 Iavg (A)	0.37	V_f = 0.85 V	0.32
Transformer primary Irms (A)	11.26	98.6	12.50
Transformer secondary Irms (A)	58.26	1.69	5.74
S. Rectifiers Irms (A)	41.58	2.32	8.02
		TOTAL	36.64

Table 5. Proposed modulation scheme. Conduction losses of the main components at the nominal input voltage (400 V)

	Nominal input (400 V)	$R_{ds,on}$ (mΩ)	Loss (W)
Q_1-Q_2 Irms (A)	7.76	37.5	4.51
Q_3-Q_4 Irms (A)	7.54	37.5	4.26
D_1-D_2 Iavg (A)	0.12	V_f = 0.85 V	0.10
Transformer primary Irms (A)	10.75	98.6	11.39
Transformer secondary Irms (A)	56.42	1.69	5.38
S. Rectifiers Irms (A)	42.19	2.32	8.26
		TOTAL	33.90

3.1. WIDE BAND GAP DEVICES

For devices with a smaller output capacitance the current would reset to nearly zero (see Figure 8 and compare to Figure 4). Table 6 is a summary of the currents passing through the main components of the converter for the proposed novel modulation scheme while using WBG devices in the primary side of the converter. Although there is no evident conduction loss advantage in comparison to Table, it should be expected that the switching losses would decrease significantly because of the reduction in Q_{oss} and Q_{rr} (the leading leg is hard-commutated in the proposed modulation).

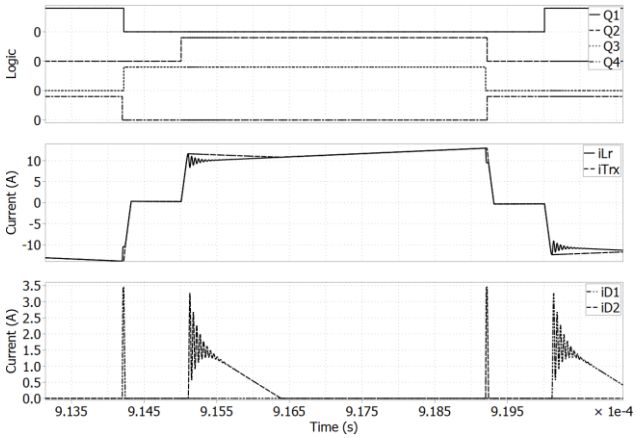


Figure 8. Full load at nominal input voltage and nominal output voltage applying the proposed modulation scheme. The HV switches in this simulation are ideal devices with no output capacitance. ZVS of lagging leg and ZCS of leading leg.

Table 6. Proposed modulation scheme. Conduction losses of the main components at the nominal input voltage (400 V) for WBG like devices.

	Nominal input (400 V)	$R_{ds,on}$ (mΩ)	Loss (W)
Q_1-Q_2 Irms (A)	7.74	37.5	4.49
Q_3-Q_4 Irms (A)	7.54	37.5	4.26
D_1-D_2 Iavg (A)	0.12	V_f = 0.85 V	0.10
Transformer primary Irms (A)	10.75	98.6	11.39
Transformer secondary Irms (A)	56.32	1.69	5.36
S. Rectifiers Irms (A)	41.54	2.32	8.00
		TOTAL	33.60

4. CONCLUSIONS

The primary side *rms* current in PSFB DCDC converters is larger than in other quasi-resonant or fully resonant converter (DAB or LLC). During the freewheeling phase the current recirculates in the primary side of the converter without effective power transfer to the secondary side. There are techniques described in the literature for resetting the primary circulating currents but always with additional circuitry in the primary or in the secondary side of the converter. The newly proposed modulation scheme for PSFB DCDC converters resets the primary side circulating currents without additional circuitry.

The control scheme presented in this chapter reduces the primary side conduction losses in PSFB topology for highly efficient DCDC converters. The new modulation is especially advantageous in designs with Wide Band Gap devices in the primary side of the converter. The lower reverse recovery charges (Q_{rr}) and output charges (Q_{oss}) of the devices further helps reducing the circulating currents and the additional switching losses caused by the loss of ZVS of one of the primary side full-bridge legs.

The proposed modulation technique in this chapter is patent pending, and the application has been already published [3].

REFERENCES

[1] X. Ruan, Soft-Switching PWM Full-Bridge Converters: Topologies, Control, and Design. Science Press, 2014.
[2] PLECS, The Simulation Platform for Power Electronic Systems, https://www.plexim.com/plecs, accessed 12 July 2020
[3] M. Escudero, M. Kutschak, inventors; Infineon Technologies Austria AG, assignee. Switching Converter. European patent application EP3723258A1. October 15, 2020

CHAPTER 14. SWITCHED CAPACITOR DRIVING SCHEME FOR POWER SEMICONDUCTORS

1. INTRODUCTION

The switching loss of a MOSFET increases with the time it takes to the voltage and current to complete the transition from off to on and from on to off states (Figure 1 and Figure 2). Discarding other phenomena, and for the area of interest of this chapter, losses are mostly given by the overlap of current and voltage during the switching time [1]-[2].

A standard driver circuit (Figure 3) would provide a low ohmic path to the positive driving voltage rail V_{GG} when the device is turning-on, typically in the range of 12-15V for high voltage SJ MOSFETs; and a low ohmic path to the negative driving voltage rail V_{SS} when the device is turning-off (to simplify we will reference the off driving voltage as V_{SS}, when it could be zero or negative in reference to the source potential).

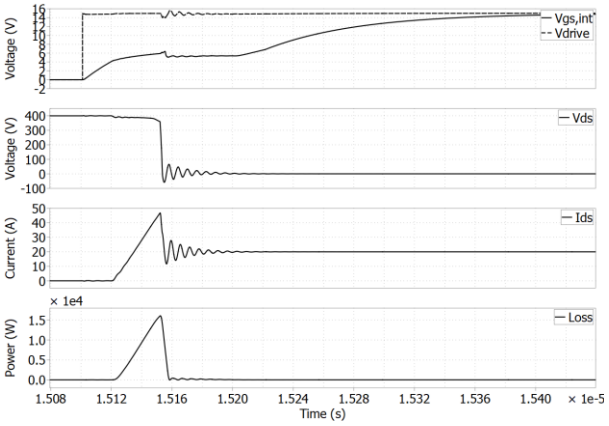


Figure 1. Hard switching turn-on.

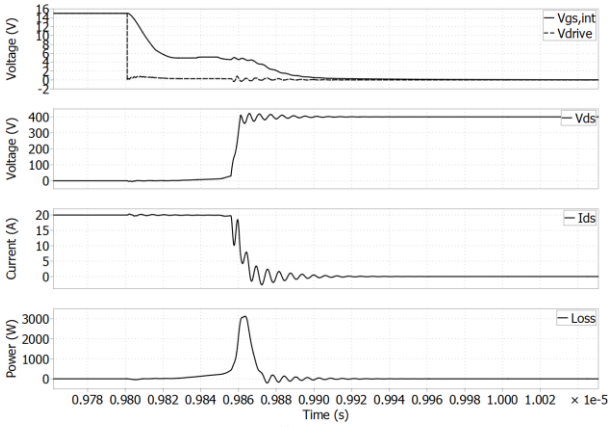


Figure 2. Hard switching turn-off.

The turn-on speed is usually limited by an external resistor ($R_{g,on}$) in order to keep *dv/dt* and *di/dt* under acceptable values, especially in hard-switched turn-on topologies. Turn-off speed is usually not purposely slowed down externally by the driving path, but desired to be as fast as possible because *dv/dt* and/or *di/dt* is limited itself by the resonant elements in the power commutation loop. A low impedance path from gate to source with small $R_{ds,on}$ in the low side MOSFETs of the driver is, in general, the best option. Therefore, it is common to place a diode in parallel to the $R_{g,on}$ resistor (Figure 3).

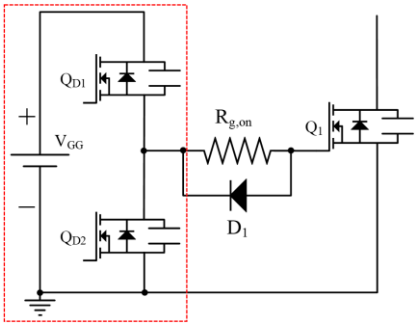


Figure 3. Standard driving scheme for MOSFETs

1.1. TURN-OFF AID

A fast hard switched turn-off transition (inductively limited) can be divided into four stages (Figure 4):

- [t_0, t_1] V_{gs} decreases from V_{GG} down to the Miller plateau voltage, which value depends on the current passing through the channel of the device, the threshold voltage and the transconductance.
- [t_1, t_2] V_{gs} stays constant at the Miller voltage, all the driving current discharges C_{gd} capacitance of the MOSFET. C_{oss} (C_{gd} plus C_{ds}) is charged up by the load (inductances in the circuit). At the end of this stage V_{ds} has risen up to the upper rail voltage (power rail). During this stage, voltage and current overlap causing losses.
- [t_3, t_4] V_{gs} decreases from the Miller voltage down to V_{th}. The current through the channel decreases down to zero at the end of the transition. During this stage the voltage and the current overlap causing additional switching losses. The device can be considered off at the end of this stage.
- [t_5, t_6] V_{gs} decreases down to the source voltage or to a negative value under the source reference voltage (V_{SS}).

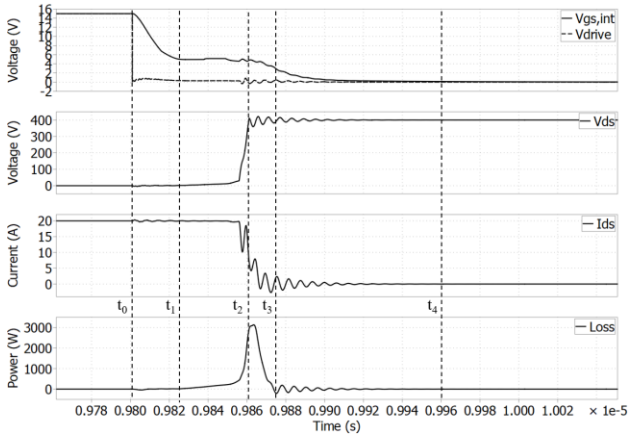


Figure 4. Turn-off transition stages.

The turn-off loss is given mostly by the *dv/dt* stage (second step above) and the *di/dt* stage (third step above) where there is overlap of voltage and current. The turn-off loss could be reduced whenever *dv/dt* (second stage) is not limited by the gate current, but by the C_{oss} resonant charge. In this condition all current diverts from the channel to the capacitances and the linear losses are negligible. Turn-off loss could be also reduced having a faster *di/dt* transition (third stage) whenever some current remains in the channel after the previous stage. In order to speed-up the whole turn-off transition, a negative voltage (in reference to the source) can be applied. At the end of the transition the negative voltage can be removed and go back to the source reference potential (Figure 5 and Figure 6) or be kept negative in reference to the source, which could be advantageous in some scenarios (Miller clamp).

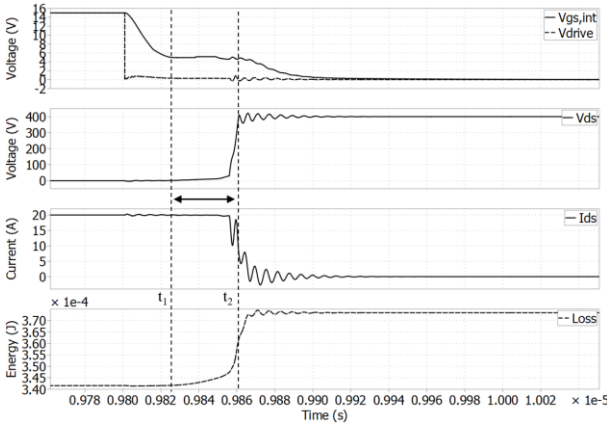


Figure 5. Voltage transition stage during a hard switched turn-off with a standard solution.

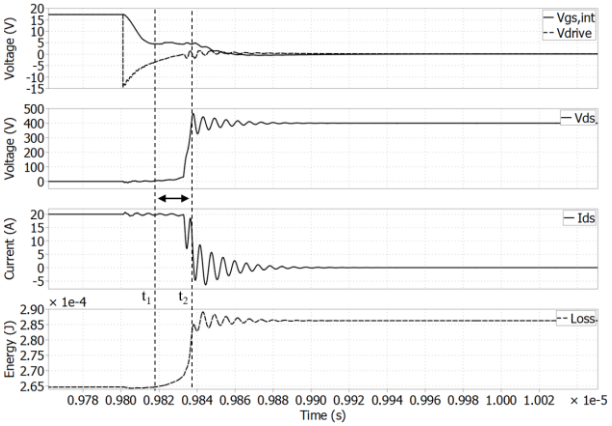


Figure 6. Voltage transition stage during a hard switched turn-off with the proposed solution.

1.2. TURN-ON AID

A fast hard switched turn-on transition can be divided into four stages (Figure 7):

- $[t_0, t_1]$ V_{gs} rises up to the threshold voltage (V_{th}) of the MOSFET. The channel of the switch can be considered open, with no current flowing.
- $[t_1, t_2]$ V_{gs} crosses V_{th}, closing the channel, and raises up to the Miller voltage, which depends on the channel final current. During this time current and voltage overlap causing losses. At the end of this stage, current is at its final value.
- $[t_2, t_3]$ V_{gs} stays constant, all the driver current charges the C_{gd} capacitance of the MOSFET. The driving impedance together with the size of C_{gd} determines the *dv/dt*. During this stage there is still overlap of voltage and current, which causes additional losses.
- $[t_3, t_4]$ V_{gs} rises up to the final V_{GG}. The voltage in the drain (V_{ds}) corresponds to the ohmic drop in the channel.

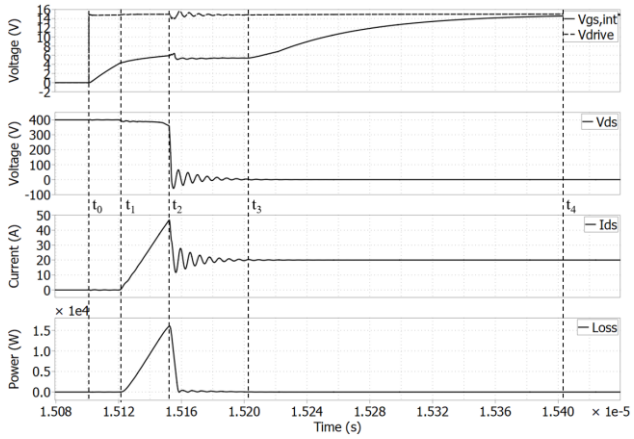


Figure 7. Turn-on transition stages.

Turn-on loss is given mostly by the *di/dt* stage (second step above) and the *dv/dt* stage (third step above). Turn-on loss could be reduced, still keeping under control *dv/dt*, having a faster *di/dt* transition (second stage). In order to speed up the *di/dt* stage, a voltage higher than V_{GG} is applied at the output of the driver during the second phase (Figure 8 and Figure 9). This higher driving voltage goes back to V_{GG} at the end of the stage.

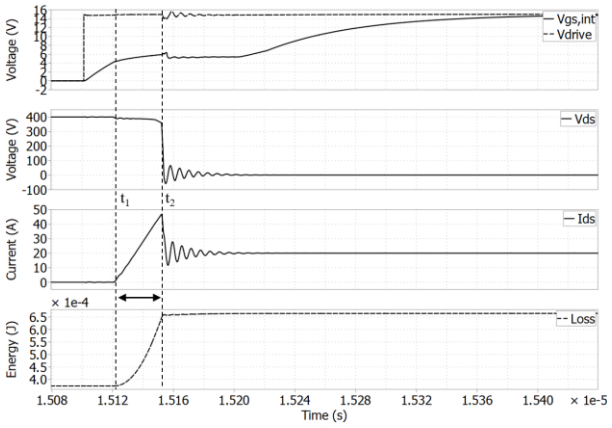


Figure 8. Current transition stage of a hard-switched turn-on with standard solution.

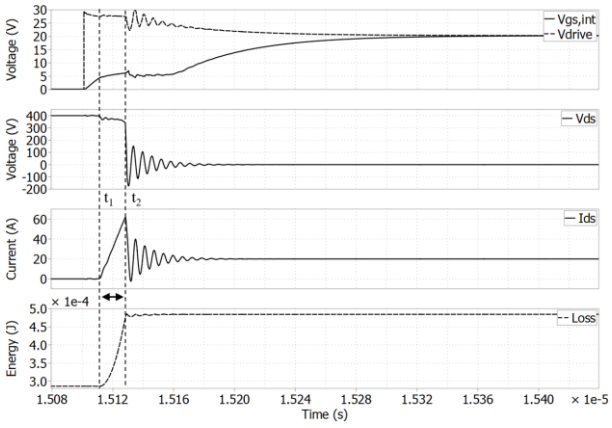


Figure 9. Current transition stage of a hard-switched turn-on with proposed solution.

2. SWITCHED CAPACITOR DRIVING SCHEME FOR POWER SEMICONDUCTORS

In the newly proposed driving circuit the standard driving structure composed by complementary switches (Q_{D1}, Q_{D2}) remains unchanged (Figure 10). The core of the proposed technique comprises an additional turn-off aid and/or additional turn-on aid realized by a switched capacitor charge pump scheme.

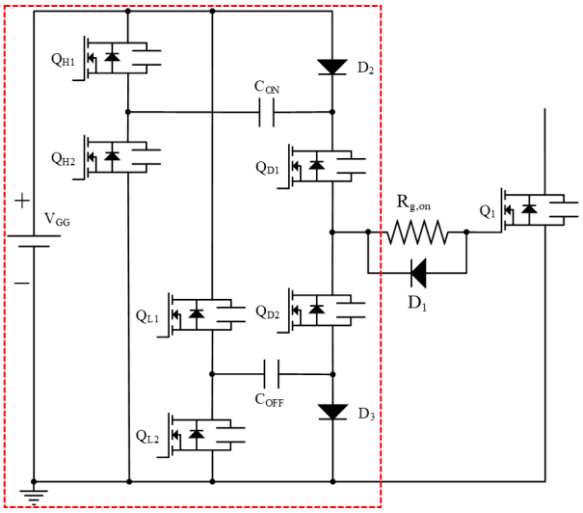


Figure 10. Proposed turn-on and turn-off aid circuit.

2.1. TURN-OFF AID

The source of the power MOSFET switch, which is the reference rail of the driver, is decoupled from the driver output stage turn-off path (or negative rail) by a diode D_3. A capacitor (C_{OFF}) is placed in parallel to the diode connected also to Q_{D2} and to two additional complementary push-pull circuits for the charging and discharging of C_{OFF}.

C_{OFF} is charged through Q_{L1} and D_3 while Q_{D2} and Q_{L2} are in off state (Figure 11). Before or while Q_{D2} turns-on, Q_{L1} becomes off and Q_{L2} becomes on. At this point D_3 blocks C_{OFF} voltage. The anode of D_3 becomes negative in reference to the source potential right at the start of the power MOSFET transition (Figure 12). Depending on the ratio of C_{OFF} to the MOSFET gate capacitance (and other external additional capacitances) C_{OFF} could be totally discharged. In that case D_3 will continue conducting till the end of the power MOSFET turn-off transition (Figure 13).

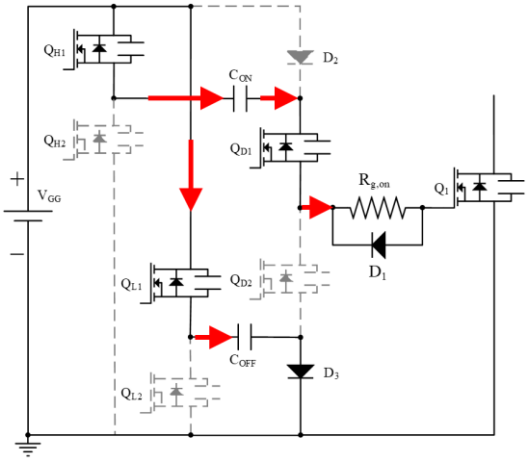


Figure 11. C_{OFF} is charged up while the output of the driver is in on state.

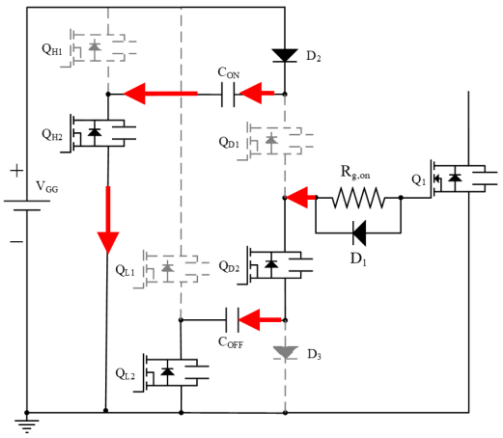


Figure 12. Charge balance of C_{OFF} and C_{gs} during the turn-off transition.

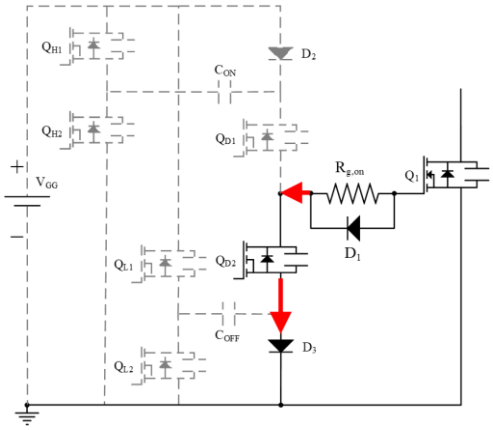


Figure 13. If C_{OFF} gets discharged during the negative driving pulse D_3 will conduct till the end of the turn-off transition.

In the following analysis the ohmic losses during the charging and discharging of C_{OFF} as well as other parasitics of the circuit whit a minor influence in the working principles of the circuit will be ignored. At the start of the turn-off transition, C_{gs} and any other external capacitance appears in parallel to C_{OFF}. The charge stored in both capacitors will balance to a voltage equilibrium. If C_{OFF} is big enough in relation to C_{gs} the final voltage of C_{OFF} will be bigger than zero ($V_0 \leq 0V$) (1-2).

$$C_{gs}(V_{GG} - V_0) = C_{OFF}(V_{OFF} - V_F) + C_{OFF}V_0 \tag{1}$$

$$V_0 = \frac{-C_{OFF}(V_{GG}-V_F)+C_{gs}V_{GG}}{C_{OFF}+C_{gs}} \tag{2}$$

C_{OFF} should be big enough not to be discharged fully during the voltage balance transition for a negative voltage charge of C_{gs} at the end of the transition ($V_0 \leq 0V$). The minimum required value of C_{OFF} is given by the relation (3-4).

$$C_{gs}V_{GG} = C_{OFF}(V_{GG} - V_F) \tag{3}$$

$$C_{OFF} = \frac{C_{gs}V_{GG}}{V_{GG}-V_F} \tag{4}$$

The charge up of C_{gd} during the dv/dt stage of the turn-off transition will provide extra charge to both equivalent parallel capacitances C_{gs} and C_{OFF}. Due to C_{gd} appearing in series to the paralleling of C_{gd} with C_{OFF}, same amount of charge injected in C_{gd} will be injected in the parallel equivalent capacitance comprised by C_{gs} and C_{OFF} (5).

$$C_{gd}(V_{bus} + V_{GG} + V_0) = \Delta V_{miller}(C_{OFF} + C_{gs}) \tag{5}$$

To simplify, because V_0 would be much smaller than V_{bus} (power switch high voltage rail), we can rewrite the previous equation as (6-7).

$$C_{gd}(V_{bus} + V_{GG}) = \Delta V_{miller}(C_{OFF} + C_{gs}) \tag{6}$$

$$\Delta V_{miller} = \frac{C_{gd}(V_{bus}+V_{GG})}{C_{OFF}+C_{gs}} \tag{7}$$

The final voltage of the gate would depend on the two relations above: voltage balance of the parallel capacitors and series charge of the Miller capacitance (8).

$$V_{gs} = \Delta V_{miller} + V_0 = \frac{C_{gd}(V_{bus}+V_{GG})}{C_{OFF}+C_{gs}} - \frac{C_{OFF}(V_{GG}-V_F)-C_{gs}V_{GG}}{C_{OFF}+C_{gs}} \tag{8}$$

2.2. TURN-OFF AID CAPACITOR DIMENSIONING

The value of C_{OFF} could be selected to achieve different behaviors of the circuit:

- Have negative bias voltage driving the MOSFET during the whole off gate pulse. This would be the case when C_{OFF} is chosen to be big enough not to be fully discharged (9-11).

$$V_0 < 0 \; And \; V_0 < \Delta V_{miller} \tag{9}$$

$$V_{gs} < 0 \tag{10}$$

$$C_{OFF} > \frac{C_{gd}V_{bus}+C_{gd}V_{GG}+C_{gs}V_{GG}}{V_{GG}-V_F} \tag{11}$$

- Speed up whole turn-off transition of the power MOSFET (Figure 14). This would be the case when V_{gs} is zero at the end of the transition (12-14).

$$V_{gs} = 0 = \Delta V_{miller} + V_0 \tag{12}$$

$$\frac{C_{gd}(V_{bus}+V_{GG})}{C_{OFF}+C_{gs}} = \frac{C_{OFF}(V_{GG}-V_F)-C_{gs}V_{GG}}{C_{OFF}+C_{gs}} \tag{13}$$

$$C_{OFF} = \frac{C_{gd}V_{bus}+C_{gd}V_{GG}-C_{gs}V_{GG}}{(V_{GG}-V_F)} \tag{14}$$

- Speed up only the *dv/dt* stage of the power MOSFET turn-off transition (Figure 15). This would be the case when C_{OFF} is fully discharged at the end of the miller plateau (15-16).

$$V_0 = \frac{C_{OFF}(V_{GG}-V_F)-C_{gs}(V_{GG}-V_{miller})}{C_{OFF}+C_{gs}} = \Delta V_{miller} = \frac{C_{gd}(V_{bus}+V_{GG})}{C_{OFF}+C_{gs}} \tag{15}$$

$$C_{OFF} = \frac{C_{gd}V_{bus}+C_{gd}V_{GG}+C_{gs}V_{GG}-C_{gs}V_{miller}}{(V_{GG}-V_F)} \tag{16}$$

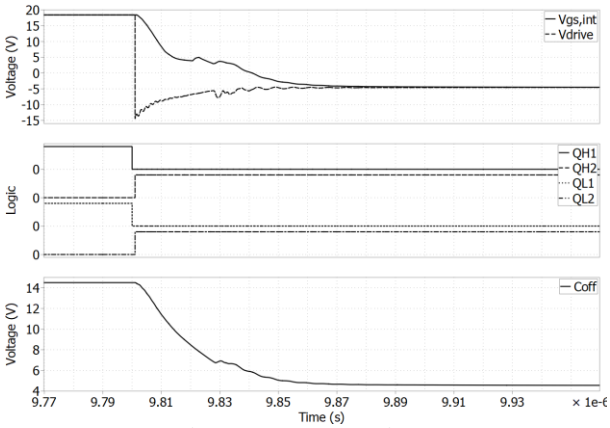


Figure 14. Example of alternative selection of C_{OFF} value in proposed circuit. C_{OFF} is not totally discharged and V_{gs} becomes lower than the source voltage during the whole off pulse.

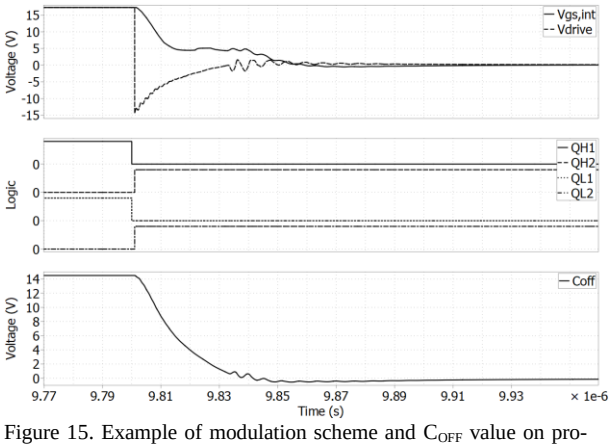


Figure 15. Example of modulation scheme and C_{OFF} value on proposed circuit. Speed up of the *dv/dt* stage.

2.3. TURN-ON AID

The positive voltage rail of the driving stage (V_{GG}) is decoupled from Q_{D1} by a diode D_2. A capacitor (C_{ON}) is placed in parallel to the diode and connected also to Q_{D1} and to two additional complementary switches (Q_{H1} and Q_{H2}) for the charging and discharging of C_{ON}.

C_{ON} is charged through Q_{H2} and D_2 while Q_{D1} and Q_{H1} are in off state (Figure 16). Before or while Q_{D1} turns-on, Q_{H2} becomes off and Q_{H1} becomes on. At this point D_2 will block C_{ON} voltage. The anode of D_2 becomes positive above V_{GG} at the start of the power MOSFET turn-on transition (Figure 17).

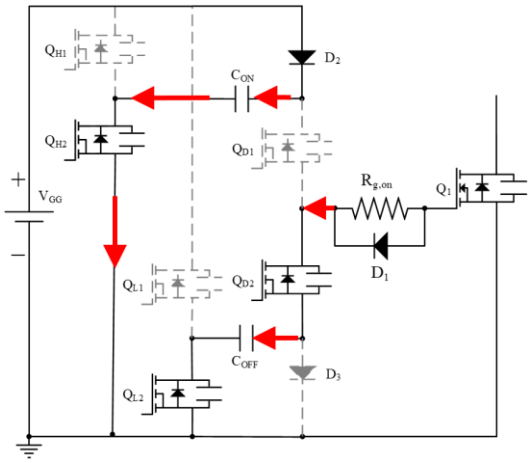


Figure 16. C_{ON} is charged up while the output of the driver is in off state.

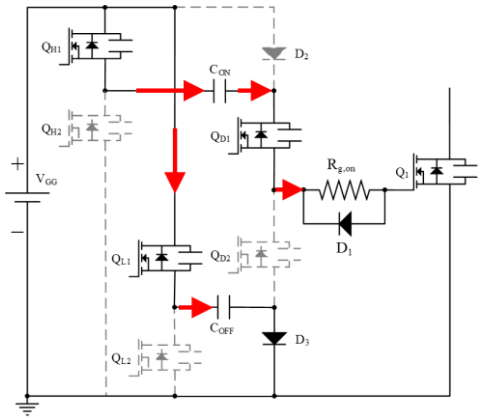


Figure 17. Charge balance of C_{ON} and C_{gs} during the turn-on transition.

Depending on the ratio C_{ON} to the MOSFET gate capacitance (and other possible external additional capacitances) C_{ON} voltage may discharge totally. In that case D_2 will continue conducting till the end of the power MOSFET turning-on transition (Figure 18).

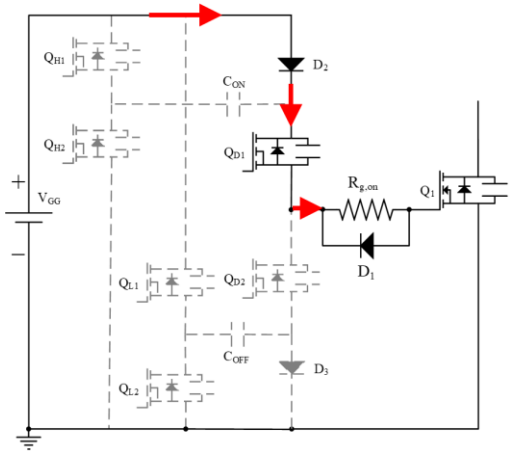


Figure 18. If C_{ON} gets discharged during the positive driving pulse, D_2 will conduct and keep the driving voltage high.

In the following analysis the ohmic losses during the charging and discharging of C_{ON} as well as other parasitics of the circuit whit a minor influence in the working principles of the circuit will be ignored. At the start of the turn-off transition, C_{gs} and any other external capacitance appears in parallel to C_{ON}. The charge stored in the parallel capacitances will balance to a voltage equilibrium. Due to C_{ON} being stacked over the driving supply voltage V_{GG} at the start of the transition, we can simplify assuming $2V_{GG}$ as the starting voltage. Because the turn-off aid might be used in combination with the turn-on aid, the starting voltage could be different from zero. V_0 is the initial voltage in C_{gs}. The final voltage in C_{gs} would be V_0 plus the variation ΔV (17-18).

$$C_{gs}(\Delta V - V_0) = C_{ON} * (2V_{GG} - V_F) - C_{ON}\Delta V \tag{17}$$

$$\Delta V = \frac{C_{ON}(2V_{GG} - V_F) + C_{gs}V_0}{C_{ON} + C_{gs}} \tag{18}$$

C_{ON} should be bigger enough not to be discharged fully during the voltage balance transition for a positive (higher than V_{GG}) voltage charge in C_{gs} at the end of the transition The minimum required value of C_{ON} is given by the relation in (19-20).

$$C_{gs}(V_{GG} - V_0) = C_{ON}(2V_{GG} - V_F) \tag{19}$$

$$C_{ON} = \frac{C_{gs}(V_{GG}-V_0)}{(2V_{GG}-V_F)} \tag{20}$$

The discharge of C_{gd} will provide extra charge to both C_{gs} and C_{ON}. Because C_{gd} appears in series to the paralleling of C_{gd} and C_{ON}, the same amount of charge injected into C_{gd} will be injected into the parallel equivalent capacitance comprised by C_{gs} and C_{ON} (21-22).

$$C_{gd}(V_{bus} + V_{GG} + V_0) = \Delta V_{miller}(C_{ON} + C_{gs}) \tag{21}$$

$$\Delta V_{miller} = \frac{C_{gd}(V_{bus}+V_{GG}+V_0)}{C_{ON}+C_{gs}} \tag{22}$$

The final voltage in the gate would depend on the result of the two phenomena above, voltage balance of the parallel capacitors and series charge of the Miller capacitance (23).

$$V_{gs} = \Delta V + V_0 - \Delta V_{miller} = \frac{C_{ON}(2V_{GG}-V_F)+C_{gs}V_0}{C_{ON}+C_{gs}} + V_0 - \frac{C_{gd}(V_{bus}+V_{GG}+V_0)}{C_{ON}+C_{gs}} \tag{23}$$

2.4. TURN-ON AID CAPACITOR DIMENSIONING

The value of C_{ON} could be selected for achieving different behaviors of the circuit:

- Set higher gate voltage than V_{GG} during the whole turn-on gate pulse (Figure 19). The external capacitor C_{ON} is not fully discharged at the end of the transition (24-26).

$$\Delta V > (V_{GG} + (V_0 - \Delta V_{miller})) \tag{24}$$

$$V_{gs} > V_{GG} \tag{25}$$

$$C_{ON} > \frac{C_{gd}V_0 - 2C_{gs}V_0 + C_{gd}V_{bus} + C_{gd}V_{GG} + C_{gs}V_{GG}}{V_0 - V_F + V_{GG}} \tag{26}$$

- Speed up whole turn-on transition of the power MOSFET (Figure 20). The external capacitor is fully discharged right at the end of the turn-on transition (27-28).

$$V_{gs} = V_{GG} \tag{27}$$

$$C_{ON} = \frac{C_{gd}V_0 - 2C_{gs}V_0 + C_{gd}V_{bus} + C_{gd}V_{GG} + C_{gs}V_{GG}}{V_0 - V_F + V_{GG}} \tag{28}$$

- Speed up only the *di/dt* stage of the power MOSFET turn-on transition. The external capacitor C_{ON} is fully discharged at the start of the Miller plateau.

$$C_{gs}(V_{miller} - V_0) = C_{ON}(2V_{GG} - V_F) \tag{29}$$

$$C_{ON} = \frac{C_{gs}(V_{miller}-V_0)}{2V_{GG}-V_F} \tag{30}$$

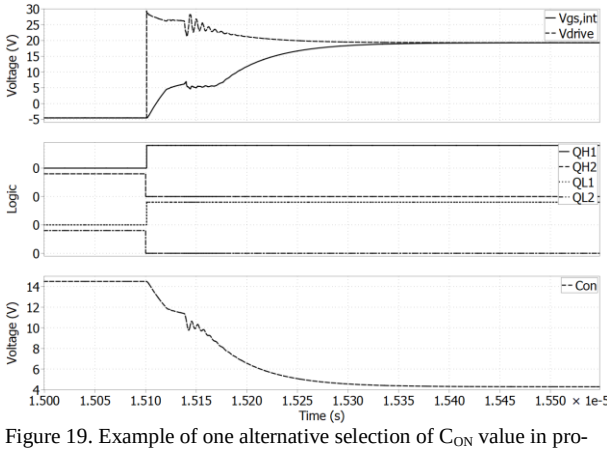


Figure 19. Example of one alternative selection of C_{ON} value in proposed circuit. C_{ON} is not totally discharged and V_{gs} becomes higher than V_{GG} (15V).

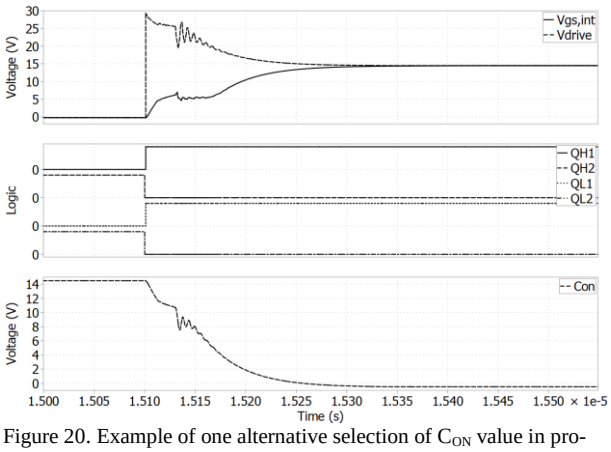


Figure 20. Example of one alternative selection of C_{ON} value in proposed circuit. Speed up of the turn-on transition.

3. PRACTICAL IMPLEMENTATION

3.1. BOOTSTRAPPING

The proposed circuit can be used to drive the high-side devices in a half-bridge configuration with standard bootstrapping techniques (Figure 21). The low side driving supply charges a bootstrapping capacitor C_{BSTRP} through the bootstrapping diode while the middle point of the half bridge (between power semiconductors Q_1 and Q_2) is grounded (at GND potential or the potential of the low side MOSFET source). For simplicity we show in the following figures only the turn-off aid, but what is stated in this section applies for any of the possible configurations proposed before.

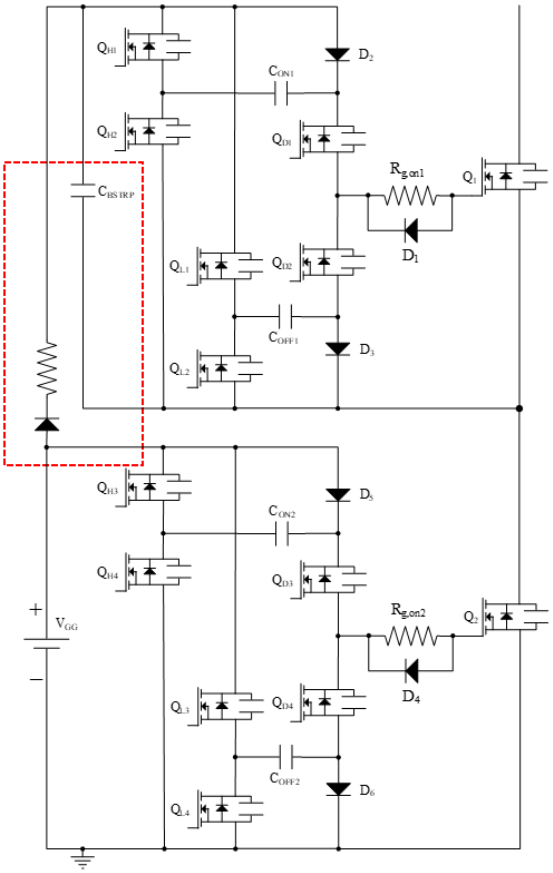


Figure 21.Half bridge configuration with bootstrapping circuitry to supply the high side driving circuitry.

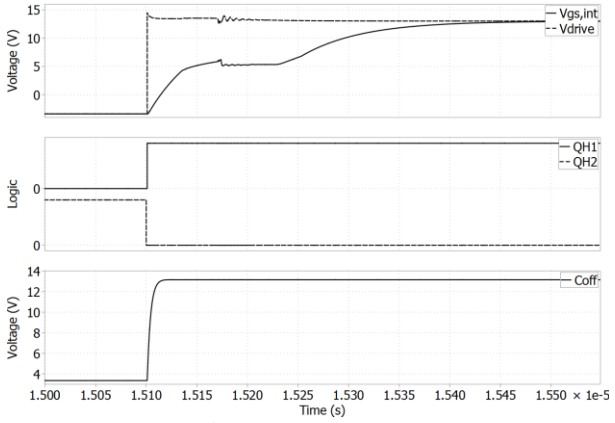


Figure 22. Example of high side turn-on signals with proposed scheme and bootstrapping supply from the low side V_{GG} (12 V).

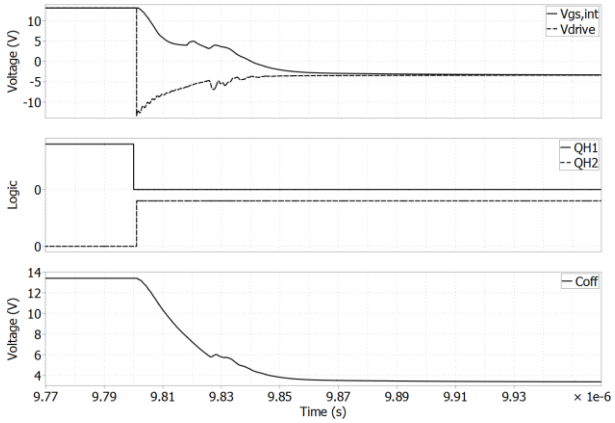


Figure 23. Example of high side turn-off signals with proposed scheme and bootstrapping supply from the low side V_{GG} (12 V).

Both the turn-on and the turn-off behavior of the low side behaves as stated in the previous sections (Figure 22 and Figure 23). However, the voltage in C_{BSTRP} will be lower than V_{GG} (low side driving supply) because of the voltage drop in the bootstrapping diode.

3.2. BIASING OF DRIVER OUTPUT STAGE

The voltage between the rails of the output stage of the driver (V_{bias} in Figure 24) may have some transients during the turn-on and the turn-off charge and discharge of the power MOSFET gate capacitance (Figure 25 and Figure 26).

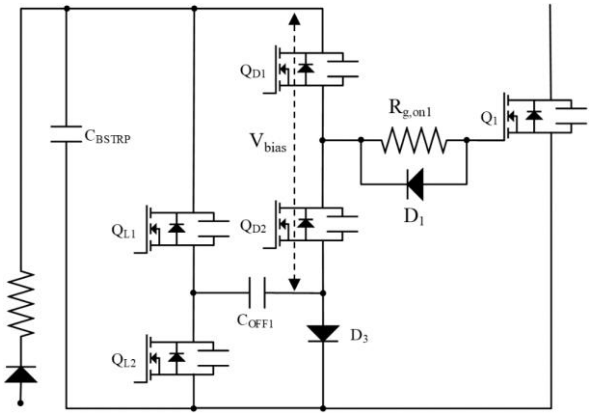


Figure 24. Point of measurement of the voltage between the rails of the output stage of the driving circuit (V_{bias}).

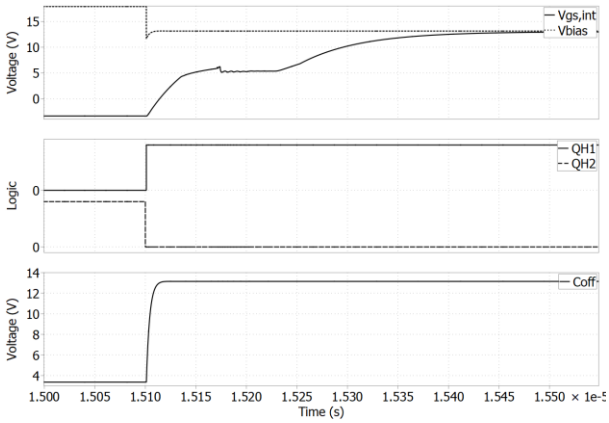


Figure 25. Example of high side turn-on signals and voltage at the rails of the output of the driving stage.

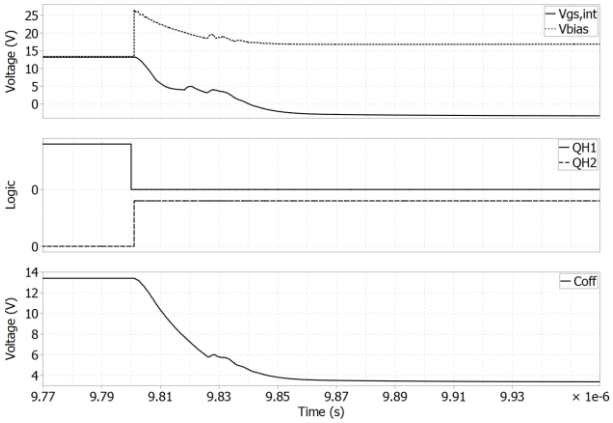


Figure 26. Example of high side turn-off signals and voltage at the rails of the output of the driving stage.

Adding a capacitor in parallel to the output stage of the driver (C_{BIAS} in Figure 27) and an extra diode in the switched capacitor charging stage (D_3) the circuit can provide a stable voltage for Q_{D1} and Q_{D2}. This may help in the implementation of the driving stage for Q_{D1} and Q_{D2}. In comparison to the previous configuration (Figure 25 and Figure 26), the output driver stage voltage has less of a variation during the switching on and off (Figure 28 and Figure 29).

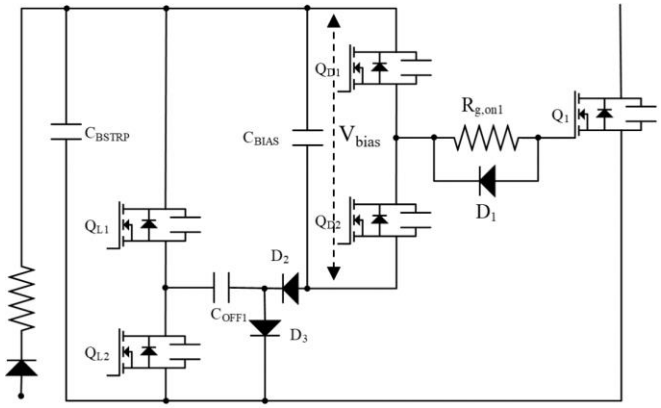


Figure 27. Point of measurement of the voltage between the rails of the driving circuit output stage (V_{bias}).

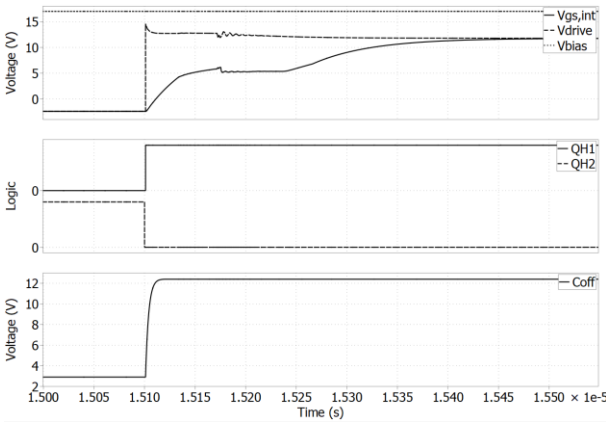


Figure 28. Example of high side turn-on signals and voltage at the rails of the output of the driving stage.

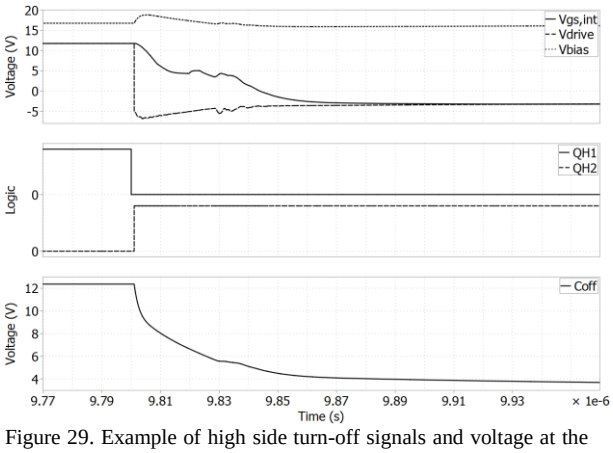


Figure 29. Example of high side turn-off signals and voltage at the rails of the output of the driving stage.

3.3. IMPLEMENTATION WITH AVAILABLE COMMERCIAL DRIVER ICS

The proposed solution could be implemented with standard driver integrated circuits (ICs) plus additional external diodes and capacitors, like it is shown in the simplified circuit in Figure 30.

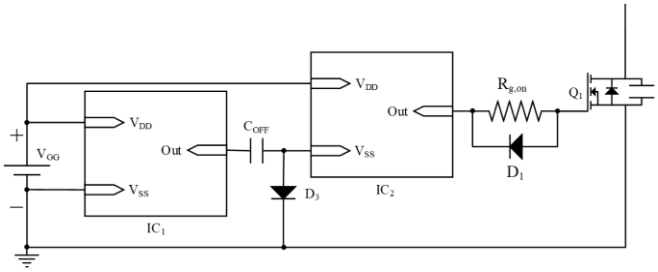


Figure 30. Example of implementation with commercial available driver ICs.

4. SIMULATION RESULTS

The standard and the proposed solution have been simulated for the most common topologies and their basic switching configurations (Figure 31 and Figure 32).

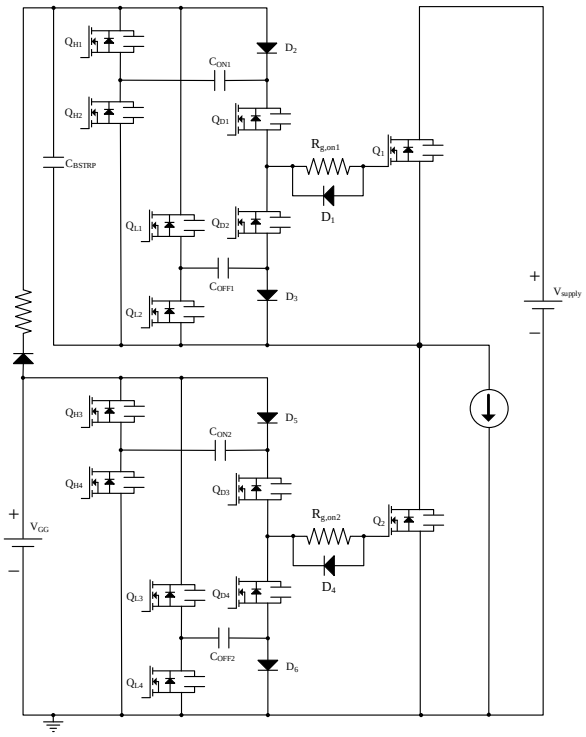


Figure 31. Half bridge configuration. Switching loss estimation of hard and soft-switched topologies.

Figure 33, Figure 34 and Figure 35 represent the simulation results of the switching losses for a device model of CFD7 TO-247 with 3 pin in three different scenarios: single device against a SiC diode, half-bridge hard-switched turn-on, and half-bridge soft-switched turn-on respectively. It can be observed that in all the cases the proposed driving circuit reduces considerably the switching losses. Moreover, it can be observed that the difference in losses increases as the switched current rises.

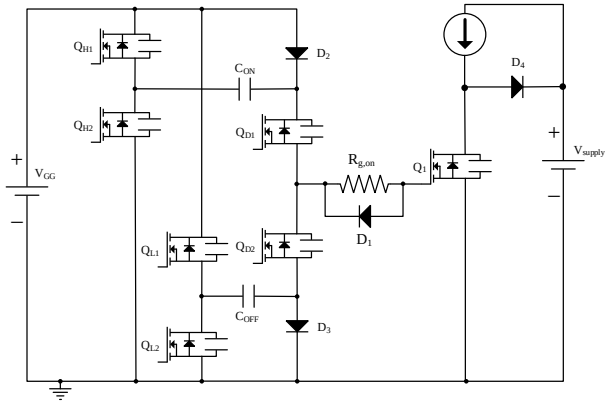


Figure 32. Boost converter, switch against diode configuration.

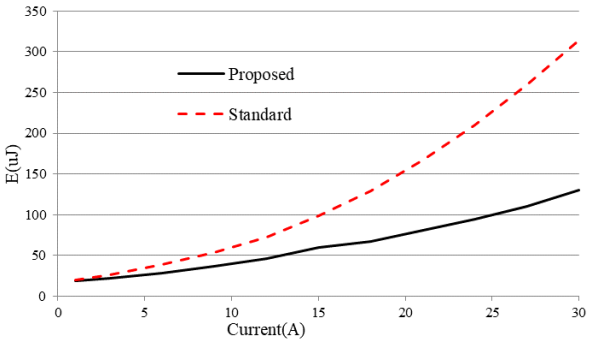


Figure 33. Switching loss of CFD7 TO-247 3 pin model with proposed circuit against standard solution in a boost converter. The energy E includes the witching energies E_{ON} plus E_{OFF}, with 15 Ω $R_{g,on}$ at different switched currents The complementary diode in the simulation is a SiC device, IDH20G65C6, with negligible Q_{rr} losses.

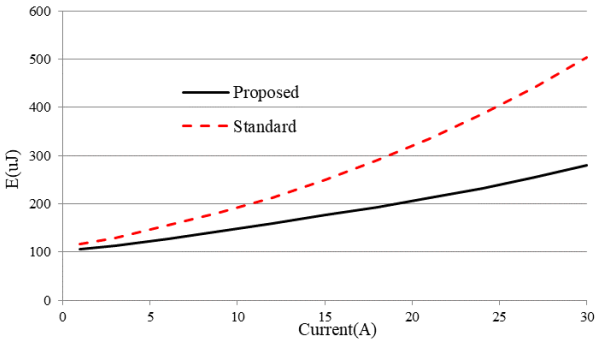


Figure 34. Switching loss of CFD7 TO-247 3 pin model with proposed circuit against standard solution in a half-bridge hard switched converter (TTF like). The energy E includes the switching energies E_{ON} plus E_{OFF}, with 15 Ω $R_{g,on}$ at different switched currents.

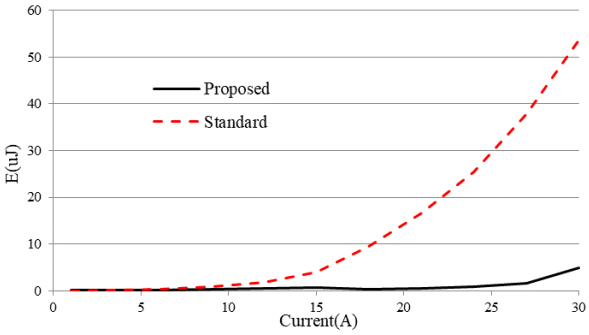


Figure 35. Switching loss of CFD7 TO-247 3 pin model with the proposed circuit against a standard solution in a half-bridge soft switched converter (LLC like). The energy E includes the switching energies E_{ON} plus E_{OFF}, with 75 Ω $R_{g,on}$ at different switched currents.

5. CONCLUSIONS

In this chapter a novel driving circuit for power semiconductors based on a switched capacitor charge pump circuit is proposed. The proposed technique could be applied to aid the turn-on transition or to provide higher positive driving voltage during the full turn-on pulse, to aid the turn-off transition or to provide lower negative driving voltage during the full turn-off pulse. The proposed turn-on aid and the turn-off aid can be used separately or combined together.

The proposed solution behaves differently and offers different advantages depending on the dimensioning of the external capacitors, and depending on their size ratio to the gate capacitance of the power semiconductor. A detailed analysis and design rules have been given in this chapter.

The proposed solution brings benefits to power semiconductor devices in all topology scenarios, reducing switching losses and allowing their usage in higher current applications with standard packages. It offers advantages both in hard-switched and soft-switched applications: lower switching losses, better clamping capabilities, and dual supply generation from a single source.

The proposed driving techniques in this chapter are patent pending, and the application has been already published [3].

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[2] E. Locorotondo, L. Pugi, F. Corti, L. Becchi and F. Grasso, "Analytical Model of Power MOSFET Switching Losses due to Parasitic Components," *2019 IEEE 5th International forum on Research and Technology for Society and Industry (RTSI)*, Florence, Italy, 2019, pp. 331-336

[3] M. Escudero, M. Kutschak, inventors; Infineon Technologies Austria AG, assignee. Switched capacitor driving circuits for power semiconductors. United States patent application 16/444,384. June 18, 2019

CHAPTER 15. MODULATION SCHEME FOR THE COLD START-UP OF THE ISOLATED BOOST CONVERTER

1. INTRODUCTION

The current-fed isolated boost converter, also referred in the literature as bidirectional PSFB (Figure 1), has the limitation of requiring of auxiliary circuitry for the so-called cold start-up [1]-[2]. The large signal gain of the converter is equal or greater than one, like any other boost converter. In cold start-up conditions (with the output capacitor discharged), it suffers of great overshoots in the secondary side devices and the current in the boost inductor (L_o) raises uncontrollably.

In [2] an auxiliary external circuitry is suggested for the pre-charge of the bulk voltage prior to the converter starting up in the current-fed isolated boost mode (Figure 2). In [3] a second ACDC stage pre-charges the bulk capacitance from the grid prior to the bidirectional PSFB starts-up and provides energy back from the LV supply. After the bidirectional converter has started-up, the ACDC changes mode and becomes and inverter feeding energy back to the grid.

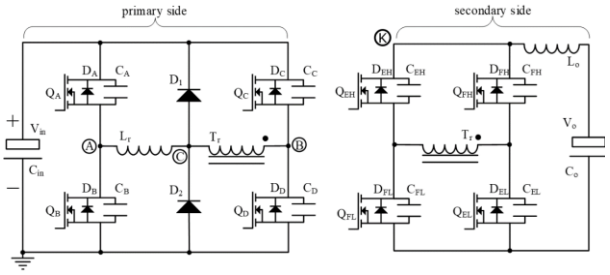

Figure 1. Simplified schematic of a bidirectional Phase Shifted Full Bridge.

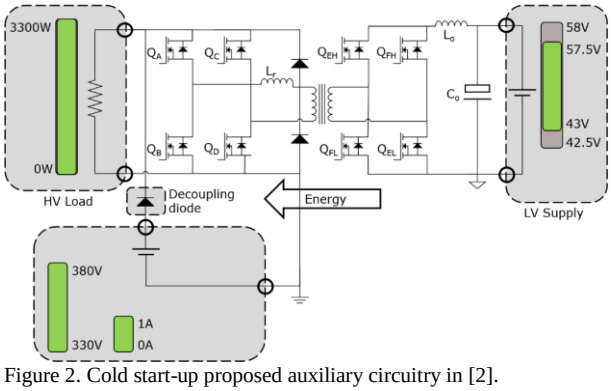

Figure 2. Cold start-up proposed auxiliary circuitry in [2].

In this chapter a novel modulation scheme is proposed enabling the cold start-up of the bidirectional PSFB (current-fed isolated boost) without additional circuitry or the availability of a second ACDC stage with bidirectional capability, which would enable as well its use in e.g. islanding grid applications. The basis of the proposed modulation is the transfer of energy in a limited manner, maintaining under control the current in the output inductor (L_o) and keeping the overshoot of the synchronous rectifiers under their rated limit.

2. MODULATION SCHEME FOR THE COLD START-UP OF THE ISOLATED BOOST CONVERTER

The principle of operation of the proposed modulation consist in enabling one of the synchronous rectification branches (LV side) during a limited time (Figure 3). During this time the current through the inductor L_o increases and at the same time a proportional current is being transferred to the primary (HV side) through the transformer. At a defined peak of current the synchronous rectification branch is turned-off. All the energy, which has been stored in the inductor L_o, will resonate against the output capacitance of the synchronous rectifiers (Figure 4, Figure 6 and Figure 5). After the current through the inductor L_o reaches zero again, a new cycle can be started (t_4 in Figure 3).

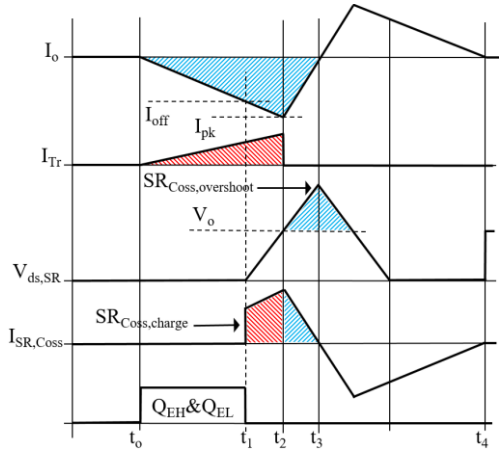

Figure 3. Simplified waveforms of the proposed modulation.

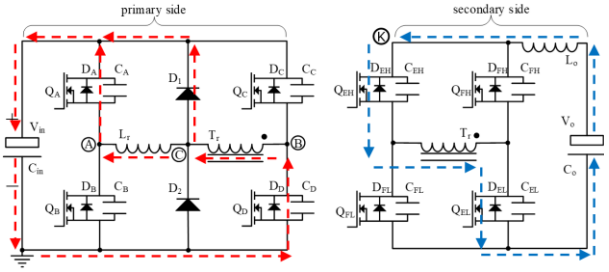

Figure 4. Simplified flow of currents in the proposed modulation during the interval [t_0,t_1].

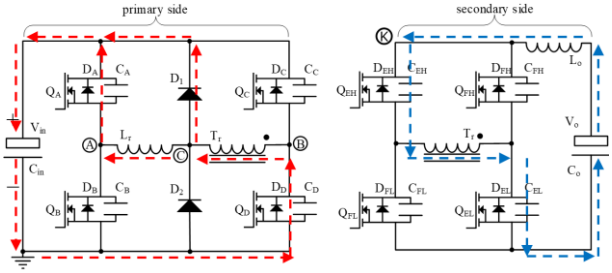

Figure 6. Simplified flow of currents in the proposed modulation during the interval [t_1,t_2].

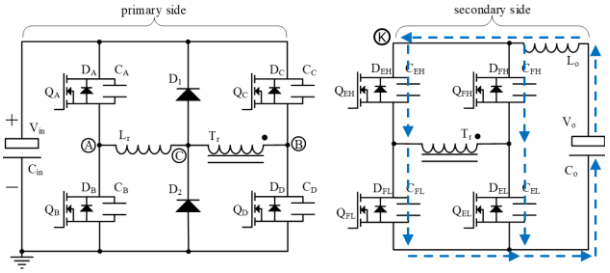

Figure 5. Simplified flow of currents in the proposed modulation during the interval [t_2,t_3].

In the following, the validity of the proposed modulation is analyzed and demonstrated mathematically. The charge that is being transferred into the input capacitor C_{in} is equal to the integral of the primary transformer current i_{Tr} during the interval [t_0, t_2] and can be estimated with (1-2), whereas the increase in voltage of the input capacitor can be estimated by (3).

$$\Delta Q_{Cin} = \int_{t0}^{t2} i_{Tr} dt \cong \frac{I_{pk,ref} \cdot (t_2 - t_0)}{2} \tag{1}$$

$$I_{pk,ref} = \frac{N_{sec}}{N_{pri}} \cdot I_{pk} \tag{2}$$

$$\Delta V_{Cin} \cong \frac{I_{pk,ref} \cdot (t_2 - t_0)}{2 \cdot C_{in}} \tag{3}$$

The peak current I_{off} can be estimated from the output and input voltages and the value of the output inductance L_o (4-5).

$$I_{off} = \frac{V_o - V_{in,ref}}{L_o} \cdot (t_1 - t_0) \tag{4}$$

$$V_{in,ref} = \frac{N_{sec}}{N_{pri}} \cdot V_{in} \tag{5}$$

From the previous equations it is possible to estimate how much time it is required to maintain the switches Q_{EH} and Q_{EL} (or alternatively Q_{FH} and Q_{FL}) in their conducting state. However, after the synchronous rectifiers are switched off, the current will continue increasing up to I_{pk} due to the charge of the output capacitance of the synchronous rectifying branches. The additional increase of current can be calculated by the amount of energy

being stored into the capacitors, which will be stored in an equal amount in the inductor during the transition (6-9).

$$\Delta E_{Lo} = 2 \cdot E_{oss}, t_1 < t < t_2 \tag{6}$$

$$E_{Lo,max} = \frac{{I_{off}}^2 \cdot L_o}{2} + 2 \cdot E_{oss,SR}(V_o) + 2 \cdot \left(E_{oss,SR}(V_o) - E_{oss,SR}(V_{in,ref})\right), t = t_2 \tag{7}$$

$$E_{Lo,max} \approx \frac{{I_{off}}^2 \cdot L_o}{2} + 2 \cdot E_{oss,SR}(V_o) + 2 \cdot E_{oss,SR}(V_o - V_{in,ref}), t = t_2 \tag{8}$$

$$I_{pk} = \sqrt{\frac{2 \cdot E_{Lo,max}}{L_O}} = \sqrt{{I_{off}}^2 + \frac{\left(4 \cdot E_{oss,SR}(V_o) + 4 \cdot E_{oss,SR}(V_o - V_{in,ref})\right)}{L_O}} \tag{9}$$

On the other hand, the energy which has been stored in the inductor during the interval [t_0, t_2] will continue to be dumped into the output capacitance of all of the synchronous rectifiers, until the V_{ds} achieves its peak at [t_3]. However, because all the synchronous rectifiers are in blocking state the actual V_{ds} of each of the switches in the stacked half-bridges is half of the apparent blocking voltage of the full rectification stage (10-12). Notice that in center-tapped configuration, although a single device blocks the resonance, the devices are rated for twice the blocking voltage.

$$\Delta E_{SR} = E_{Lo,max}, t_2 < t < t_3 \tag{10}$$

$$E_{SR,max} = \frac{{I_{off}}^2 \cdot L_o}{2} + 2 \cdot E_{oss,SR}(V_o) + 2 \cdot E_{oss,SR}(V_o - V_{in,ref}) + 4 \cdot E_{oss,SR}(V_o), t = t_3 \tag{11}$$

$$V_{K,max} = \sqrt{\frac{2 \cdot E_{SR,max}}{4 \cdot C_{oss,SR}}} = \sqrt{\frac{{I_{off}}^2 \cdot L_o + 12 \cdot E_{oss,SR}(V_o) + 4 \cdot E_{oss,SR}(V_o - V_{in,ref})}{4 \cdot C_{oss,SR}}} \tag{12}$$

It is desirable to maintain the maximum V_{ds} overshoot of the synchronous rectifiers under a specified limit, commonly 80% of their rated breakdown voltage. That would limit the maximum energy that could be transferred in each of the switching cycles and how long it would take to achieve the nominal V_{in} voltage depending on the size of the input capacitor C_{in} (13-15).

$$I_{off,max} = \sqrt{\frac{{V_{K,max}}^2 \cdot 4 \cdot C_{oss,SR} - 12 \cdot E_{oss,SR}(V_o) - 4 \cdot E_{oss,SR}(V_o - V_{in,ref})}{L_o}} \tag{13}$$

$$(t_2 - t_0) \cong \frac{I_{pk} \cdot L_o}{(V_o - V_{in,ref})} \tag{14}$$

$$\Delta V_{Cin,max} \cong \frac{{I_{pk,max}}^2 \cdot L_o}{2 \cdot C_{in} \cdot (V_o - V_{in,ref})} = \frac{{I_{off,max}}^2 \cdot L_o + 4 \cdot E_{oss,SR}(V_o) + 4 \cdot E_{oss,SR}(V_o - V_{in,ref})}{2 \cdot C_{in} \cdot (V_o - V_{in,ref})} \tag{15}$$

$$(t_4 - t_2) \cong \frac{2 \cdot \pi \cdot \sqrt{L_o \cdot 4 \cdot C_{oss,SR}}}{2} \tag{16}$$

From the previous formulas it is obvious that $I_{off,max}$ it is nearly independent of the charging state of C_{in} (V_{in}). The duty cycle would have however to adapt to compensate for the increase in V_{in} and the reduction in the slope of the current through L_o (13). From (14) it is obvious that the increase in voltage in C_{in} is only possible while V_o is bigger than the reflected voltage in the transformer. This modulation scheme can only provide buck gain. Once the V_{in} equals the reflected output voltage, the proposed modulation scheme in [1] can be used to achieve boost gain and finish the start-up sequence.

It interesting to point out as well that the closer $V_{in,ref}$ is to the final voltage the more energy can be transferred to the input capacitor per switching cycle. This is due to the proportional increase in the time it takes to reach I_{pk} in the inductor (13). During that longer time, current flows proportionally more into the primary side capacitor. Nevertheless, the saturation limit of the transformer has still to be observed.

3. PRACTICAL IMPLEMENTATION

There are two possible implementations of the proposed novel modulation scheme:

- A fixed switching frequency control. The converter operates in Discontinuous Conduction Mode (DCM) for the small duty and in boundary mode once the duty is limited by the switching frequency.
- A variable switching frequency control. The converter operates in boundary mode only limited in the lower frequency range by the saturation of the transformer.

Both variants can be implemented in a programmable controller like the XMC from Infineon as an extension of the currently available bidirectional PSFB controller in [1].

4. SIMULATION RESULTS

In an implementation of the proposed modulation with constant switching frequency, the maximum duty that could be applied is equal to the period minus the resonance time (16). Substituting the values in the previous formulas we can solve numerically the charging time for the cold start-up of a converter with C_{in} = 440 µF, V_o = 54 V, $C_{oss,SR}$ = 4·604 pF, $E_{oss,SR}(Vo)$ = 0.88 µJ, L_o = 6 µH, $V_{ds,SR,max}$ = 120 V, N_{pri} = 21 and N_{sec} = 4. The $I_{off,max}$ for the given parameters would be equal to $I_{off,max}$ = 3.71 A. The corresponding $I_{pk,max}$ would be equal to 4.30 A. The resonance time would be approximately 378 ns.

For a fixed frequency scheme the maximum possible duty at 200 kHz switching frequency would be approximately 4.24 µs. The maximum V_{in} at which we could apply the $I_{off,max}$ at 200 kHz would be $V_{in,DCM}$ = 251 V. Therefore, under $V_{in,DCM}$ the converter operates in DCM (Figure 7 and Figure 8), above $V_{in,DCM}$ and until $V_{in,max}$ = 283 V the converter operates in boundary mode (Figure 9).

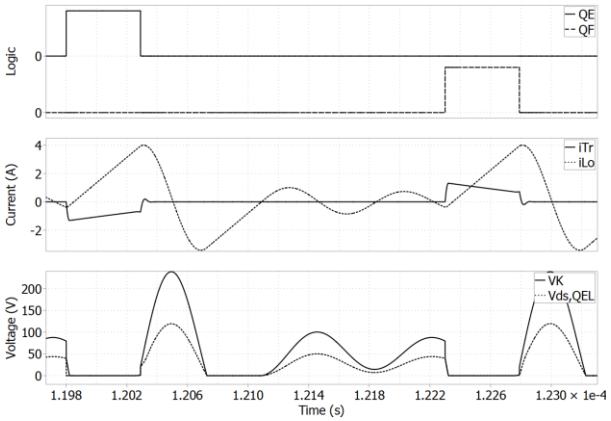

Figure 7. Simulation of fixed frequency cold-start-up with the proposed modulation.

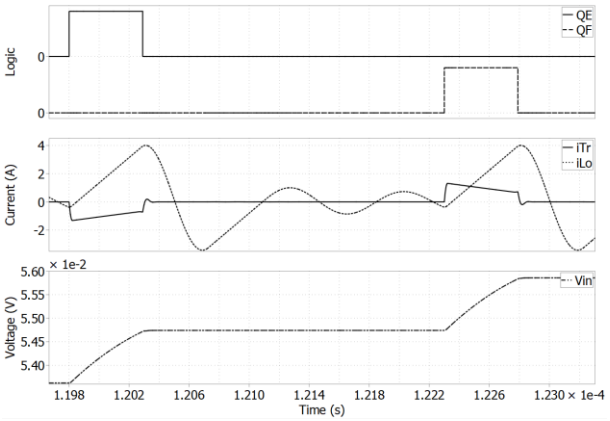

Figure 8. Simulation of fixed frequency cold-start-up with the proposed modulation.

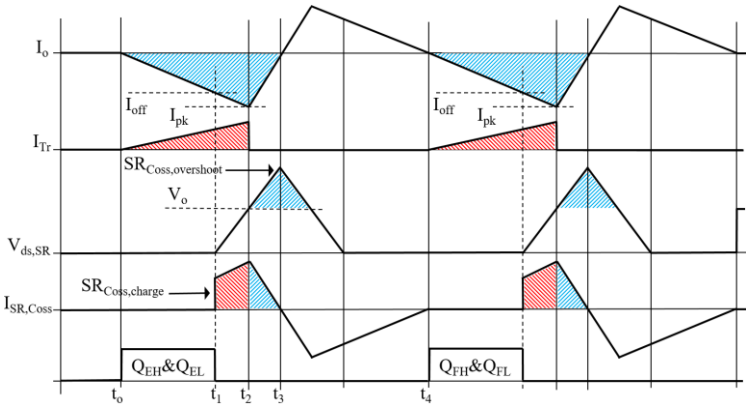

Figure 9. Simplified waveforms of the proposed modulation in boundary mode.

In a fixed frequency cold-start-up scheme the start-up takes relatively long time, a minimum of 360 ms for the previous example parameters (Figure 10). In a variable frequency scheme the converter operates in boundary mode always, limited only by the maximum $I_{off,max}$ (Figure 11 and Figure 12). In this mode the charging time from V_{in} = 0 until $V_{in,max}$ = 283 V can be calculated also numerically. In this mode of operation the start-up requires less time, a minimum of 146 ms (Figure 13).

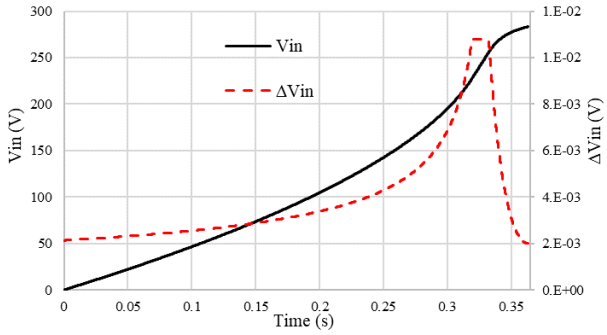

Figure 10. Cold start-up with a fixed frequency scheme (DCM). Approximately 360 ms.

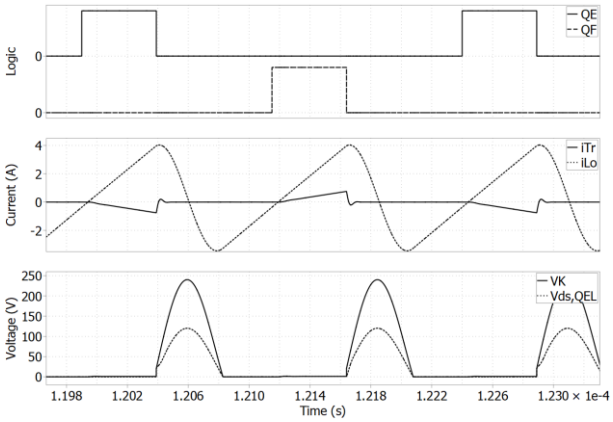

Figure 11. Simulation of variable frequency cold-start-up (boundary mode) with the proposed modulation.

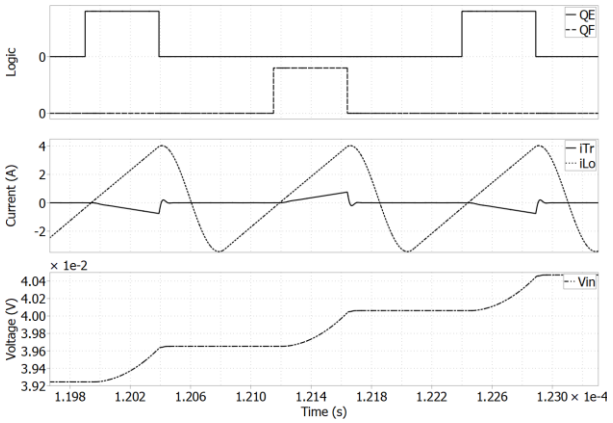

Figure 12. Simulation of variable frequency cold-start-up (boundary mode) with the proposed modulation.

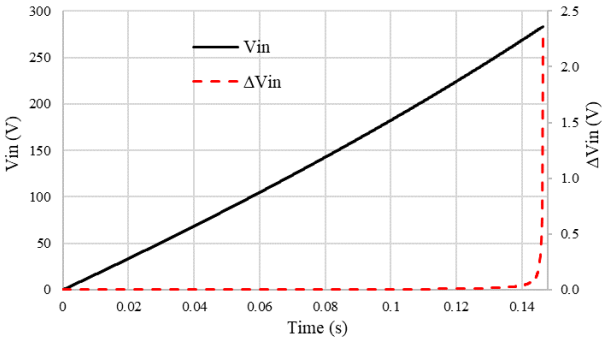

Figure 13. Cold start-up with a variable frequency scheme (boundary mode). Approximately 146 ms.

5. CONCLUSIONS

In this chapter a new modulation scheme for the cold start-up of current-fed isolated boost converters and bidirectional Phase Shifted Full Bridge converters has been proposed. The proposed modulation scheme allows using PSFB topology as part of a bidirectional converter with cold start-up requirements, common in electric vehicles DCDC converters, UPS, or islanding grid applications among others. The proposed control technique enables the PSFB DCDC converter as an alternative to bidirectional converters with buck-boost capabilities like DAB or CLLC.

Two alternative implementations of the modulation scheme have been proposed. In a fixed frequency implementation the converter operates in Discontinuous Conduction Mode and in boundary mode limited by the fixed period. In a variable frequency implementation the converter operates in boundary mode only limited in the lower frequency range by the saturation of the transformer.

Finally the proposed modulation scheme has been demonstrated mathematically and in simulations.

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CHAPTER 16. MODULATION SCHEME FOR THE GAIN RANGE EXTENSION AND BIDIRECTIONAL OPERATION OF LLC CONVERTERS

1. INTRODUCTION

The LLC resonant converter working in the forward direction (Figure 1) has a large signal gain that depends on the switching frequency: the gain decreases above the series resonant frequency (buck operation) and increases under the series resonant frequency (boost operation) (Figure 2). Additionally, the gain also varies depending on the load of the converter:

- For heavy loads the boost capability decreases.
- For light loads the buck capability reduces. The phenomenon is aggravated by the effects of additional circuit parasitics that may cause the gain to become non-monotonic and to actually increase as the switching frequency goes up [1].

In consequence, the design of a wide output and/or wide input range LLC converter requires of special design considerations (increase of the magnetizing current, with the consequent decrease in overall efficiency) and/or control techniques (e.g. burst mode), especially at light load or at the minimum output voltage. A good summary of solutions for the light load regulation of LLC converters is covered in [1]-[5]. It is noteworthy that in [5] a delayed turn-off is applied to the SRs to decrease the gain of the converter while operating under resonance and in forward mode. However, the most common solution, when possible, is burst mode operation.

It is acknowledged that the LLC converter can operate as a bidirectional converter (Figure 3). However, when operating in reverse direction the maximum possible gain is lower than or equal to one (Figure 4). The converter operates as series resonant converter in this mode (the equivalent resonant tank is comprised of only two resonant elements, LC). This limits the applicability of the reverse operation of the LLC [4], often replaced by CLLC or other symmetrical topologies like Dual Active Bridge (DAB) when bidirectional capability is a requirement [6].

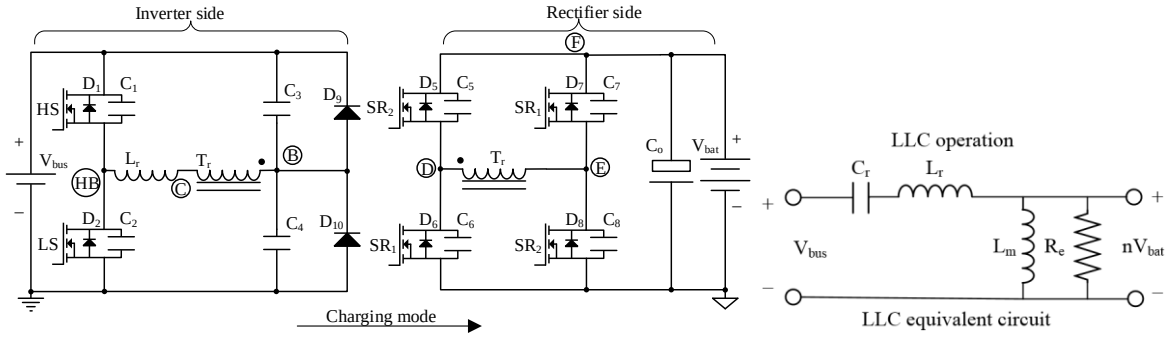


Figure 1. LLC converter operating in forward direction and its equivalent circuit.

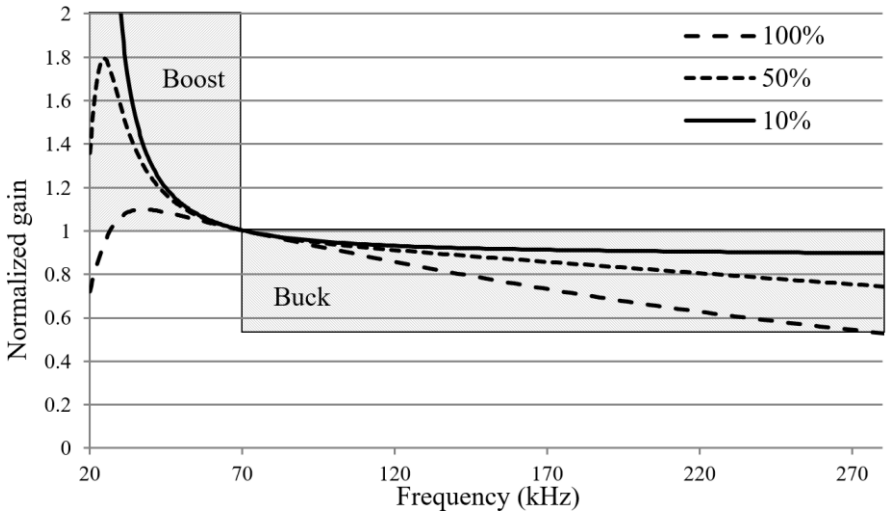


Figure 2. LLC converter frequency to gain curves at different loads. Buck operation above the series resonance (70 kHz) and boost operation under the series resonance.

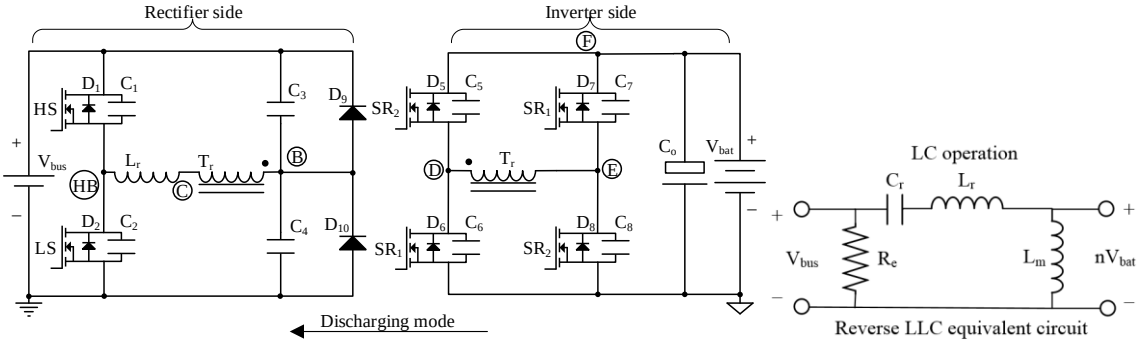


Figure 3. LLC converter operating in reverse direction and its equivalent circuit.

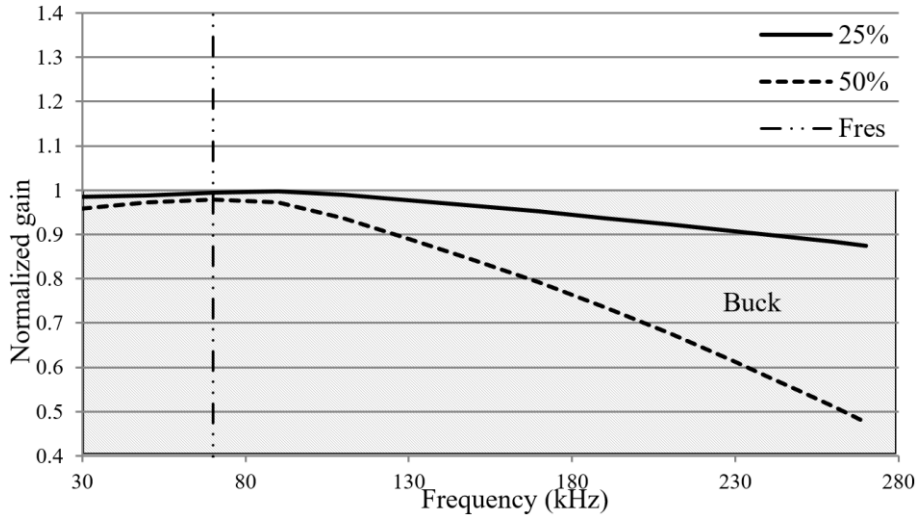


Figure 4. Reverse operating LLC converter frequency to gain curves at different loads. Gain is always lower than or equal to one.

In this chapter a new modulation scheme is proposed which provides boosting gain for the series resonant converter. Moreover, the proposed control scheme works both in forward and reverse operation of the LLC and addresses both the problems listed above: light load regulation in forward mode and boost gain in reverse mode. The novel modulation scheme controls the large signal gain of the LLC converter adjusting the synchronous rectifier's conduction time without any additional circuitry. For the proposed modulation scheme the only requirement is the operation of the LLC above the resonant frequency.

2. MODULATION SCHEME FOR THE GAIN RANGE EXTENSION AND BIDIRECTIONAL OPERATION OF LLC CONVERTERS

2.1. INCREASE OF GAIN

The gain of the converter can be increased by delaying the turn-off of the synchronous rectifiers (Figure 5). The delayed turn-off increases the initial current at the start of the next power transfer and the total amount of energy transferred (enclosed area between iL_r and the magnetizing current, which corresponds to the secondary side reflected current (Figure 5)).

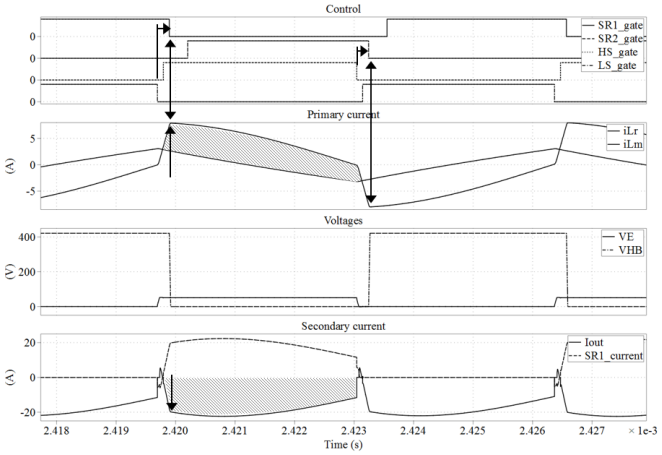


Figure 5. Proposed increase of gain of the LLC by delayed turn-off of the SRs.

2.2. DECREASE OF GAIN

The gain of the converter can be decreased by advancing the turn-on of the synchronous rectifiers (Figure 6). The early turn-on decreases the initial current at the start of the next power transfer and the total amount of energy transferred (enclosed area between iL_r and the magnetizing current, which corresponds to the secondary side reflected current (Figure 6)).

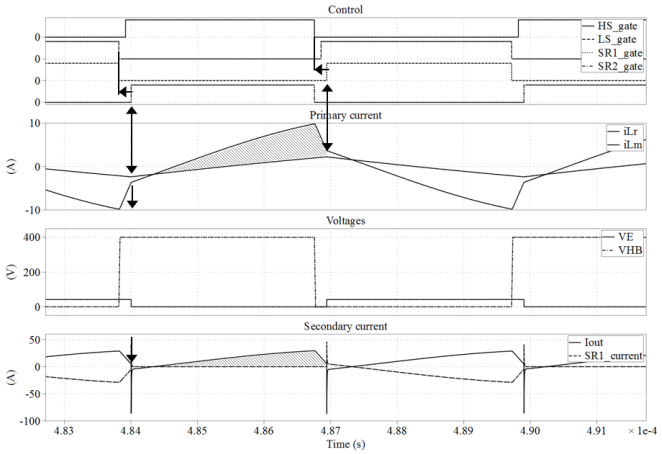


Figure 6. Proposed decrease of gain of the LLC by early turn-on of the SRs.

3. SIMULATION RESULTS

3.1. BIDIRECTIONAL OPERATION, INCREASE OF GAIN

The LLC converter in Figure 3 was simulated both with a standard modulation and applying different turn-off delays to the SRs. The resulting gains of the converter plotted in Figure 7 and Figure 8 demonstrate the effect of the proposed modulation scheme. Furthermore, the graphs in Figure 7 highlight the fact that the proposed modulation scheme only works above the resonant frequency of the converter.

Figure 9 and Figure 10 emphasize the influence of the working point on the circulating currents through the converter. Nearly the same increase in gain can be achieve in D and H, C and G, B and F but the latest points E to H are more practical since the resulting *rms* currents are much lower.

On the other hand, it is noteworthy to mention that while the HV side is always soft switched in all working points A to G, the LV side is soft-switched in A, E and F but it is partially hard-switched in G and F, and hard-commutated in B, C and D.

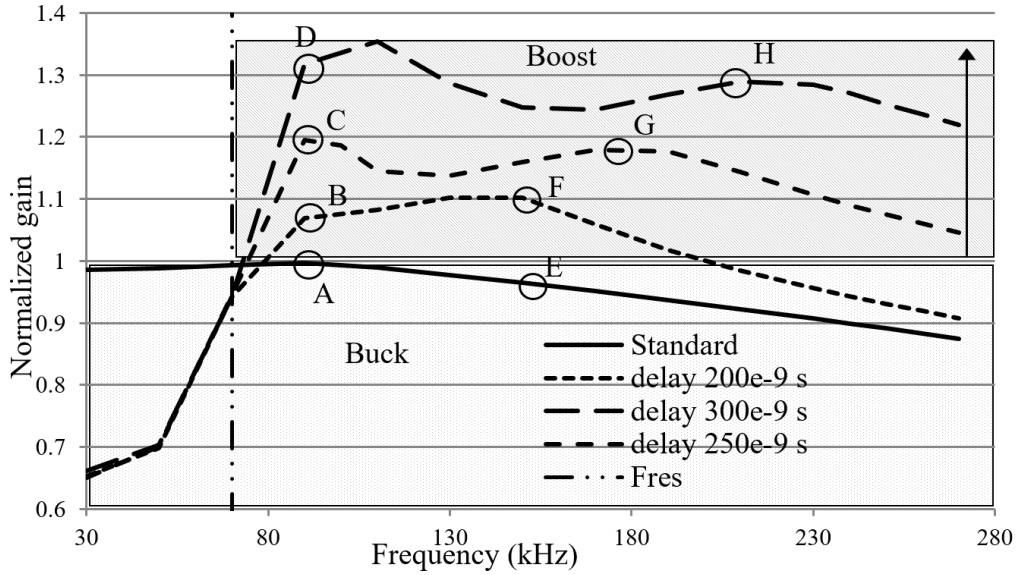
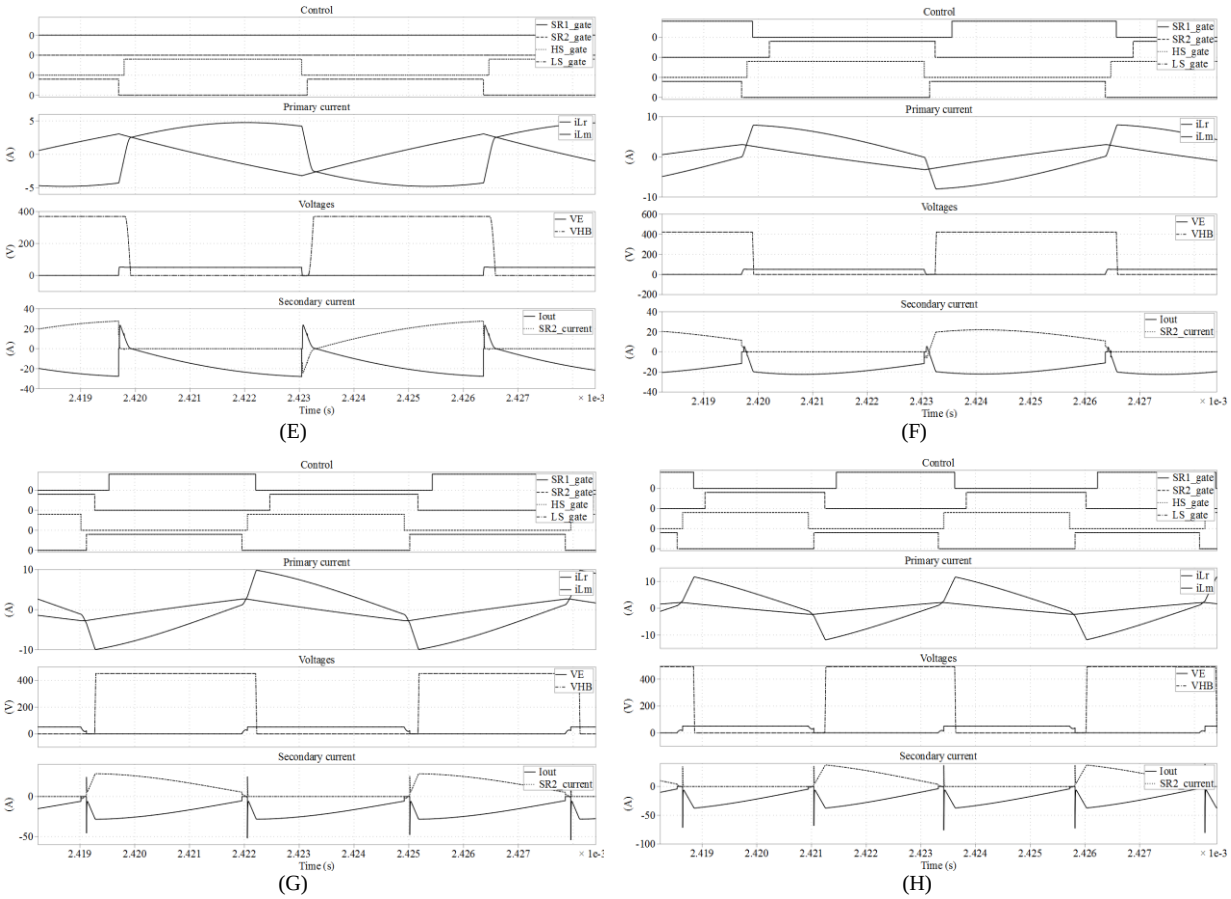


Figure 7. Reverse operating LLC converter frequency to gain curves with the proposed modulation and applying different turn-off delays to the SRs. Includes four examples of possible boost operating points close to the resonance and four examples of possible boost operating points at high frequencies in relation to the series resonance.



(E) (F)

(G) (H)

Figure 8. Simulated waveforms of the standard and the proposed modulation scheme for the points E to H in Figure 7.

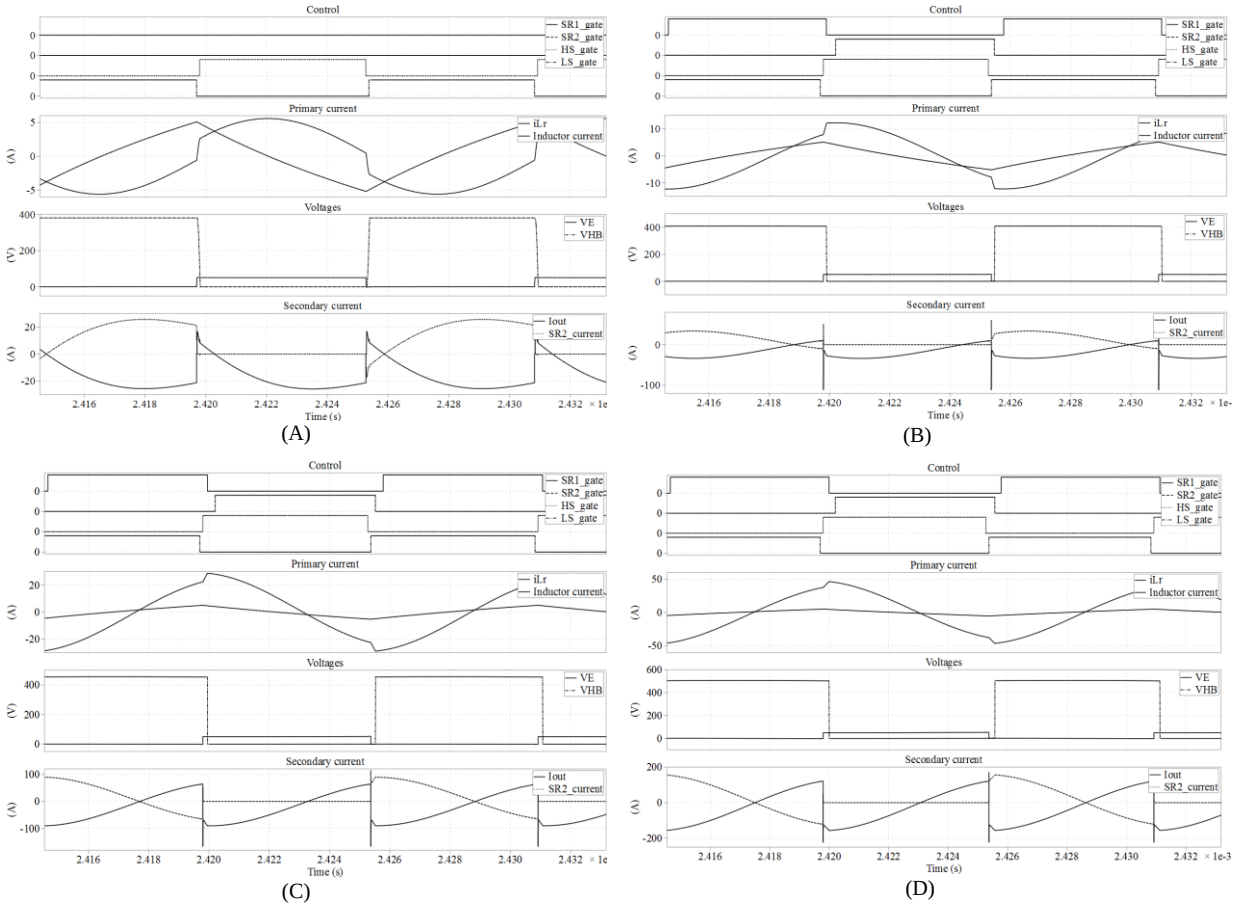


Figure 9. Simulated waveforms of standard and proposed modulation scheme for the points A to D in Figure 7. The *rms* currents are higher than in the operating points E to H in Figure 7.

3.2. DECREASE OF GAIN

The LLC converter in Figure 1 was simulated with a standard modulation and applying different turn-on delays to the synchronous rectifiers. The resulting gains of the converter plotted in Figure 10 demonstrate the effect of the proposed modulation scheme. The graph in Figure 10 highlights the fact that the proposed modulation scheme only works above the resonant frequency of the converter.

On the other hand, Figure 11 emphasizes the increase in *rms* currents for the proposed modulation scheme while reducing the gain. Moreover, it is noteworthy to mention that while the HV side is soft-switched in L-I, the LV side is hard-commutated in K-I.

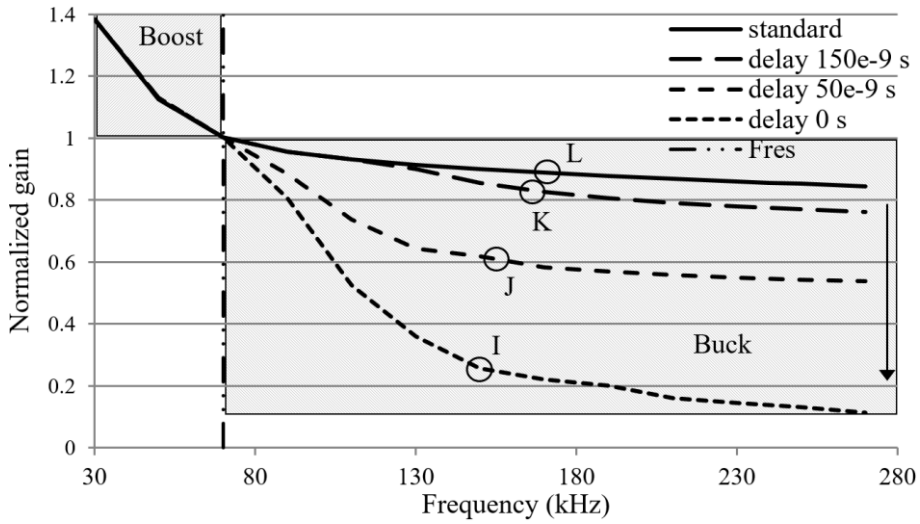


Figure 10. Forward operation of the LLC converter. Frequency to gain curves with the proposed modulation applying different turn-on delays to the SRs. Includes four example working points at high frequencies in relation to the series resonance.

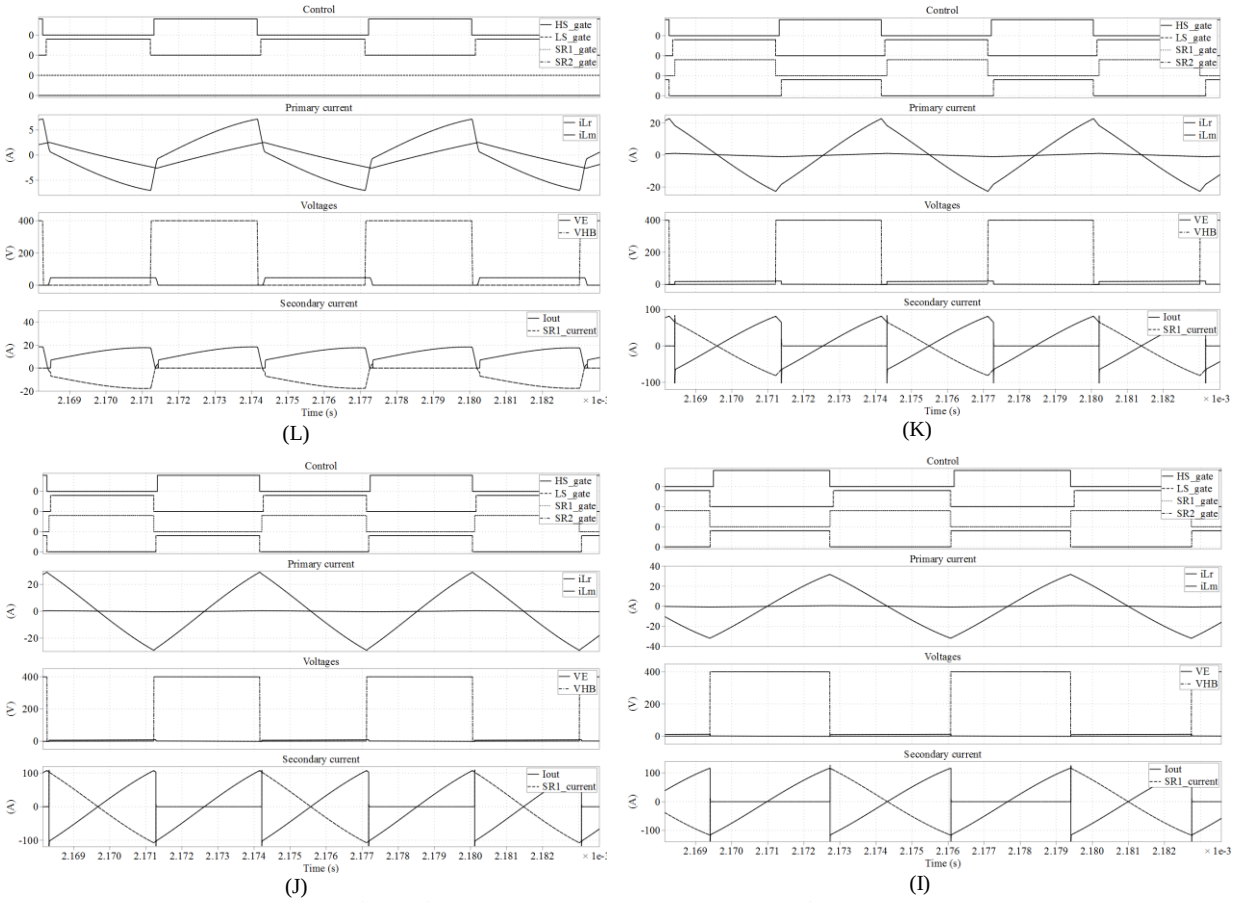


Figure 11. Simulated waveforms of standard and proposed modulation scheme for the points I to L in Figure 10.

4. CONCLUSIONS

In this chapter a new modulation scheme for LLC converters is proposed, which increases or decreases the large signal gain of the converter by delaying or advancing the synchronous rectifiers gating signals. The proposed modulation scheme does not require of any hardware modification of the power stage. The control can be applied to a standard LLC which controller allows delaying and/or advancing the synchronous rectifiers (SR) gating signals. The preferred implementation would be a digital controller with multimode operation where the frequency control and SR delay control can be integrated.

The solution presented enables the LLC as a bidirectional converter in applications where the efficiency in the reverse boost operation mode is not important. For example, it is a requirement in On Board Chargers (OBC) to charge up the bus capacitors prior to the battery switch closes and connects the high voltage (HV) battery to the bus. However, most of the time the OBC works in the forward direction. The solution presented in this chapter enables a more efficient and cost effective solution than the CLLC or the DAB alternatives.

The proposed control techniques in this chapter are patent pending, and the application has been already published [7].

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SECTION IV. CONCLUSION

CHAPTER 17. RESULTS AND CONCLUSIONS

1. MAIN RESULTS

For the currently available semiconductor power switching devices the resonant and quasi-resonant converters are the most attractive options for achieving high efficiency, high power density or a combination of both at a reasonable cost. The key advantage of the resonant and quasi-resonant converters is the reduction of the switching losses. The switching losses can be reduced achieving ZVS for the turn-on transition and ZCS for the turn-off transition.

Among the isolated, resonant and quasi-resonant DCDC converter topologies, the most common ones in medium-high power and high-voltage applications are the LLC, the PSFB and the DAB due to their simplicity and high efficiencies. Among those topologies each one has its own advantages and disadvantages, which makes each of them best suited for different applications, power and voltage ranges.

This thesis is focused in the study of the LLC and the PSFB. Both of this topologies are very promising and well suited for any of the available power switching semiconductor technologies in the market, specifically for Si SJ MOSFETs, which are currently the most mature devices and the most competitive in cost now and in the foreseeable future. The objective of this thesis is the optimization, improved reliability and functionality of the LLC and the PSFB maintaining as much as possible the simplicity of the standard circuit configuration.

Therefore, the main contribution of this thesis is the design and construction of two converters with similar specifications and similar magnetic structure to study the achievable performance of the two main topologies objective of this work: LLC and PSFB. It has been found that, although PSFB can achieve higher efficiencies than is commonly expected thanks to the newest devices and the newly proposed control techniques, the LLC is still potentially superior and capable of still higher efficiencies with less components at a lesser cost. However, in bidirectional applications the large signal gain range of the PSFB makes it still superior to the LLC.

Chapter 4 introduces a complete system solution for a 3300 W bidirectional PSFB DCDC converter from 400 V to 54 V which achieves 98 % efficiency in forward or buck mode and 97% in reverse or boost mode. The achieved power density is in the range of 4.34 W/cm³ (71.19 W/in³), which is enabled by the use of SMD packages, the innovative stacked magnetic construction and the innovative cooling solution. This DCDC converter proves the feasibility of PSFB topology as a high efficiency topology at the level of fully resonant topologies when combined with the latest SJ MOSFET technologies. This DCDC converter proves as well that the PSFB topology can be used as a bidirectional DCDC stage without changes in the standard design or construction of a traditional and well known topology through innovations in control techniques powered by digital control.

Chapter 5 introduces a complete system solution for a 3300 W LLC DCDC converter from 400 V to 51.5 V achieving 98.1 % peak of efficiency. The achieved power density is in the range of 4 W/cm³ (66 W/in³) which is enabled by the use of SMD packages, the innovative stacked magnetic construction and the innovative cooling solution. The optimized layout and an optimized driving circuitry achieves benchmark performance with minimum stress in the devices, enabled also by the innovative cooling concepts presented in this board. This DCDC converter proves the feasibility of the half-bridge LLC as a high-efficiency topology for a 3300 W converter, at the level of full-bridge LLC or a dual stage LLC. This DCDC converter also proves that digital control, powered by XMC™ Infineon general purpose microcontrollers, is not only capable of controlling the LLC topology but the most effective way to overcome its difficulties and pitfalls. Moreover, the included protections mechanisms and control schemes further boost the reliability and performance of the converter achieving the best possible efficiency.

2. CONCLUSIONS

2.1. PHASE SHIFT FULL BRIDGE CONVERTER DESIGN

Since the server power supplies consume an enormous amount of power, the most critical issue is high efficiency. In order to implement a high efficiency and high power density server PSU, PSFB converter with SRs MOSFETs, external resonant inductor and clamping diodes is the perfect topology for the DCDC stage. Its main characteristic is the wide ZVS operation range from mid to full load, nearly suppressing switching losses. Moreover, the constant switching frequency allows a simple control and EMI design. One of the major advantages of PSFB over other resonant soft-switching topologies is the comparatively lower *rms* currents through the secondary side of the converter thanks to the output filter inductance. However, hold-up time regulation requirement makes PSFB converter not to be operated with its maximum effective duty in nominal conditions and causes long freewheeling time and large circulating currents in the primary side of the converter.

The design of a high efficiency PSFB converter is a complex problem with many degrees of freedom which requires of a sufficiently accurate modeling of the losses of the converter and of efficient design criteria. In the published paper in Chapter 9 a losses model of the converter has been proposed as well as design guidelines for

the efficiency optimization of the PSFB converter. The losses model and the criteria have been tested with the redesign of an existing reference PSFB DCDC converter for server applications that achieved 95.85 % of efficiency at 50 % of load. The new converter was designed following the same specifications as the reference: 1400 W of maximum power; 400 V nominal input voltage; hold-up regulation down to 360 V input voltage; and 12 V output. The new optimized prototype of PSFB converter was built and tested achieving a peak efficiency of 96.68 % at 50 % of load, notably exceeding the performance of the reference converter in all load range and operating conditions.

The main differences between both designs are related to the magnetics construction, with an improved balance of core and conduction losses along the load range of the converter. Furthermore, the transformer turns ratio and the dimensioning of the external resonant inductance enabled lower $R_{ds,on}$ in the primary side HV devices and lower voltage class (and consequently also lower $R_{ds,on}$) in the secondary side LV devices. Moreover, all semiconductors in the new optimized design are SMD, which together with the high efficiency at full load enables a power density in the range of 3.70 W/cm³ (60.78 W/in³).

Chapter 3 further describes the new optimized PSFB DCDC converter for server applications which was introduced in the published paper in Chapter 9. This DCDC converter proves the feasibility of PSFB topology as high efficiency topology at the level of fully resonant topologies when combined with the latest SJ MOSFETs devices. This DCDC converter proves as well that digital control, powered by XMC™ Infineon general purpose microcontrollers, is not only capable of controlling PSFB topology but also to overcome its drawbacks and to enable the usage of the latest SJ MOSFET devices and the lowest possible voltage class devices, both in the HV and in the LV side, to achieve the best possible performance.

2.1.1. PSFB PRIMARY SIDE CIRCULATING CURRENTS

The primary side *rms* current in PSFB DCDC converters is larger than in other quasi-resonant or fully resonant converters (DAB or LLC). During the freewheeling phase the current recirculates in the primary side of the converter without effective power transfer to the secondary side. There are techniques described in the literature for resetting the primary circulating currents but always with additional circuitry in the primary or in the secondary side of the converter.

Chapter 12 has proposed a new modulation technique which decreases the switching frequency of the PSFB DCDC converter to compensate for the loss of duty cycle due to the drop in the input voltage (e.g. during hold-up time). The proposed control scheme allows the design of PSFB for its optimal performance at the nominal operating conditions while fulfilling the specifications for hold-up time. Alternatively, the proposed control scheme allows increasing the input voltage regulation range and/or the output voltage regulation range.

Chapter 13 has proposed a new modulation scheme for resetting the primary side circulating currents in PSFB DCDC converters without additional circuitry. The proposed control scheme reduces the primary side conduction losses in PSFB topology for highly efficient DCDC converters. Moreover, the proposed modulation scheme is especially advantageous in designs with Wide Band Gap devices or similar in the primary side of the converter. The lower reverse recovery charges (Q_{rr}) and output charge (Q_{oss}) of the devices further helps reducing the circulating currents and the additional switching losses in this newly proposed modulation scheme.

2.1.2. PSFB SYNCHRONOUS RECTIFIERS VOLTAGE CLASS

One of the major disadvantages of the PSFB topology in comparison to other resonant topologies is the higher blocking voltage required for the SRs. This is especially detrimental in wide range operation converters and further aggravated by the SRs drain voltage overshoot. Unlike other resonant topologies, the inductor at the output of the PSFB effectively decouples the capacitor bank from the rectification stage, which otherwise becomes a strong lossless snubber.

In the published paper included in Chapter 8 the main causes for the secondary side rectifiers drain voltage overshoot in PWM converters, specifically in PSFB converters, have been analyzed. Design guidelines and solutions for each of the scenarios, including a novel modulation scheme for the operation of PSFB with the output filter operating in DCM have been proposed. Traditionally the main criterion for the selection of the external resonant inductance has been the available energy for the ZVS of the HV primary side devices and the loss of duty cycle at full load. However, the analysis in this work demonstrates that, from the point of view of the overall performance of the system, the impact on the secondary side drain voltage overshoot and the reduction of the secondary side switching losses has to be taken into account for the dimensioning of the transformer's turns ratio *n* and the external inductance L_r.

The proposed strategies enable the design of DCDC PSFB converters targeting high efficiency without penalties in reliability, complexity or cost. Lower blocking voltage requirements for the rectification devices improve their Figure of Merit, potentially reducing their related losses and increasing the overall efficiency of the converter.

The feasibility of the proposed solutions have been tested in the two PSFB DCDC converters in this thesis, a 1400 W PSFB converter for server application in Chapter 3 and Chapter 8, and a 3300 W PSFB converter for

telecom and battery charging applications in Chapter 4 and Chapter 7. The drain voltage overshoot has been proven to remain well within standard rated limits in all working conditions of these converters.

2.1.3. BIDIRECTIONAL PSFB DCDC CONVERTER

In the published paper included in Chapter 7 a modulation scheme for the operation of the PSFB as a bidirectional DC/DC converter has been proposed to overcome well-known problems on isolated boost converters: high drain voltage overshoot on the secondary or current-fed side devices, and the lack of ZVS capability on the primary or voltage-fed side devices. Furthermore, these issues are addressed without penalties in complexity, cost or performance: the design optimization procedure (selection of the output inductor, leakage or magnetizing inductance among other parameters) is not constrained by the proposed bidirectional operation of the converter.

The main issues and the solutions given by the proposed control techniques have been analyzed in detail. The proposed modulation allows boost operation with minimized drain voltage overshoot equalizing the currents through the boost inductor and other inductances of the converter (L_r, L_{lkg} and stray) prior to a power transfer. Moreover, it enables the usage of primary side clamping diodes, with their advantages in forward or buck operation.

With the proposed modulation the primary side devices achieve full or nearly full ZVS along all load range of the converter in both forward and reverse operation. In addition, a method for extending ZVS range of the lagging leg while operating in boost mode with the proposed modulation has been introduced: precharging the inductances above the minimum required for reducing the overshoot.

In the proposed boost mode operation the secondary side devices are turned-on in hard switching conditions, whereas they are soft switched in buck operation mode. The conduction loss of the primary side clamping diodes is also relatively higher in the boost mode. Those additional contributions to losses, which are the main drawbacks of the modulation presented in this paper, decrease the overall system efficiency of the converter when working in reverse or boost mode in comparison to the forward or buck mode.

A high efficiency prototype of bidirectional 3300 W PSFB was designed and built to demonstrate the feasibility of the proposed solution. The experimental results confirm the analysis introduced in this paper. The prototype achieves a peak efficiency of 98 % in the buck mode and 97.5 % in the boost mode at nominal conditions and 50 % load points. Overall, this work demonstrates that the PSFB is a competitive alternative when building highly efficient and cost-competitive bidirectional DC/DC converters.

In Chapter 15 a new modulation scheme for the cold start-up of current-fed isolated boost converters and bidirectional Phase Shifted Full Bridge converters is proposed. The proposed modulation scheme allows using PSFB topology as part of a bidirectional converter with cold start-up requirements, common in electric vehicles DCDC converters, UPS, or islanding grid applications among others. The proposed control technique enables the PSFB DCDC converter as an alternative to bidirectional converters with buck-boost capabilities like DAB or CLLC.

Two alternative implementations of the start-up modulation scheme are proposed. In a fixed frequency implementation the converter operates in Discontinuous Conduction Mode and in boundary mode limited by the fixed period. In a variable frequency implementation the converter operates in boundary mode only limited in the lower frequency range by the saturation of the transformer. Finally the proposed modulation scheme has been analyzed mathematically and demonstrated in simulations.

2.2. BIDIRECTIONAL LLC DCDC CONVERTER

In Chapter 16 a new modulation scheme for LLC converters has been proposed that increases or decreases the nominal large signal gain of the converter by delaying or advancing the synchronous rectifiers gating signals. The proposed modulation scheme does not require of any hardware modification of the power stage. The control can be applied to a standard LLC whose controller allows delaying and/or advancing the synchronous rectifiers (SR) gating signals. The preferred implementation would be a digital controller with multimode operation where the frequency control and SR delay control can be integrated.

The solution presented enables the LLC as a bidirectional converter in applications where the efficiency in the reverse boost operation mode is not important. For example, it is a requirement in On Board Chargers (OBC) to charge up the bus capacitors prior to the battery switch closes and connects the high voltage (HV) battery to the bus. However, most of the time the OBC works in the forward direction. The solution presented in this chapter enables a more efficient and cost effective solution than the CLLC or the DAB alternatives.

2.3. SI SJ MOSFETS IN RESONANT AND QUASI-RESONANT CONVERTERS

In the published paper included in Chapter 10 the impact of the non-linear distribution of charge in the output capacitance of modern Si devices on the performance and requirements for the design of resonant ZVS converters has been analyzed. Furthermore, the non-linear capacitance of Si has been compared to the quasi-linear capacitance of a SiC device of equivalent time related output capacitance $C_{oss(tr)}$, and compared to the quasi-linear capacitance of a GaN device of similar energy related output capacitance $C_{oss(er)}$. The advantages and disadvantages

of each of the alternatives have been analyzed for single device and half-bridge based topologies, as well as in full ZVS and partial or full hard-switching operating conditions.

In half-bridge topologies the required energy to achieve full ZVS depends exclusively on the total output stored charge $Q_{oss}(V_{DC})$ and the supply voltage V_{DC}, whereas in single device topologies the required energy is further increased by a relatively smaller $E_{oss}(V_{DC})$. In summary, in the full ZVS scenario, the equivalent SiC and the GaN devices are superior to the Si device in single device and half bridge topologies.

In partial hard-switching turn-on, within certain hard-switching turn-on voltage, the losses of the Si device could be lower than the switching losses of the equivalent $C_{oss(tr)}$ SiC or the equivalent $C_{oss(er)}$ GaN device. However, for a certain energy in the resonant inductor the switching voltage of the SiC or the GaN devices is much lower. Moreover, the Si advantage window dramatically diminishes when is compared to equivalent $R_{ds,on}$ SiC or GaN devices.

Overall, this work demonstrates that a meaningful one-to-one replacement of devices without a redesign of the converter would be among devices with an equivalent $C_{oss(tr)}$. Moreover, to fully unleash the potential improvement in the overall performance of the converter while replacing a Si device by an equivalent $R_{ds,on}$ SiC or GaN device requires the redesign of the resonant ZVS converter accounting for the reduced ZVS energy requirements. Finally, a highly efficient 3300 W DCDC LLC resonant converter prototype was designed and built to demonstrate the validity of the analysis.

2.3.1. DRIVING SCHEME FOR POWER SEMICONDUCTORS

In Chapter 14 a novel driving circuit for power semiconductors based on a switched capacitor charge pump circuit is proposed. The proposed technique could be applied to aid the turn-on transition or to provide higher positive driving voltage during the full turn-on pulse, to aid the turn-off transition or to provide lower negative driving voltage during the full turn-off pulse. The proposed turn-on aid and the turn-off aid can be used separately or combined together.

The proposed solution behaves differently and offers different advantages depending on the dimensioning of the external capacitors, and depending on their size ratio to the gate capacitance of the power semiconductor.

The proposed solution brings benefits to power semiconductor devices in all topology scenarios, reducing switching losses and allowing their usage in higher current applications with standard packages. It offers advantages both in hard-switched and soft-switched applications: lower switching losses, better clamping capabilities, and dual supply generation.

Finally, the proposed solution can be used together with any type of power semiconductor devices reducing losses in any topology and providing a dual supply bias from a single supply source when required.

2.4. MAGNETICS CONSTRUCTION

Reducing the switching and conduction losses of the semiconductor switches is not enough [1]. The key of an efficient and reliable isolated DCDC converter is in the magnetics design, more specifically the transformer. The main transformer has two main contributions to the losses: core loss and conduction loss. The core loss is proportional to the switching frequency and the flux density. The conduction loss in the transformer becomes increasingly complicated to estimate as the switching frequency increases (skin, proximity and fringing effects). The same principles apply to other magnetics in the converter like the series resonant chokes or the output inductors. This is the reason why so many studies focus in improving the magnetics: reducing the flux density, or improving their construction to alleviate the effects of the high frequency in the conductors.

In Chapter 6 and Chapter 11 a complete PSU with high efficiency requirements and constrained dimensions is presented. Due to the outer dimension limits, a planar transformer with reduced height and volume is preferred. In the proposed construction, the main transformer and the parallel resonant inductor have been integrated into the same structure. One of the main advantages of the discrete implementation of the parallel resonant inductor and the main transformer is the improved coupling of the transformer. The magnetizing inductance of the main transformer can be made arbitrarily high. Therefore, the magnetizing current becomes neglectably small. On the one hand, this reduces the proximity losses, especially important in planar windings. On the other hand, the gap of the main transformer is virtually zero, therefore, reducing the effect of the stray fields, also very harmful in planar windings.

With the proposed construction technique it is possible to achieve high efficiency at reasonable cost and power density in isolated DCDC converters.

3. FUTURE WORKS

3.1. NARROW RANGE DAB CONVERTER WITH SI SJ MOSFETS

The DAB is a fully symmetric converter in which the large signal gain is controlled by the overlap or phase shift between the primary side and the secondary side duty and the direction of the power flow is controlled by

the sign of the phase shift between the primary and the secondary side duty. In its most simple modulation scheme the primary and the secondary side devices are controlled by a fixed frequency 50% duty signal. Other more advanced modulation schemes are possible in which the duty of the primary, the secondary or both sides can vary.

Whereas the most advanced modulation schemes bring the advantage of an extended ZVS range, and lower *rms* currents through the converter in part of the operation range, the control complexity greatly increases. Moreover, the simple 50 % duty modulation allows the implementation of a DAB converter with a half-bridge in the primary and center tapped rectification in the secondary, which greatly reduces the circuit complexity of the circuit and has a total component count at the level of LLC converters. Furthermore, the efficiency levels that can be achieved in this configuration are potentially near the level of an LLC with similar specifications.

Finally, it is commonly acknowledged that the DAB converter is not well suited for wide range applications with Si SJ MOSFETs. The ZVS operation range is limited at light loads. Moreover, the primary side or the secondary side can become hard-commutated depending on the load, the input and output voltages. However, the issue can be alleviated increasing the primary side magnetizing currents, at the expense of the additional circulating currents and conduction losses. This approach can be effective in narrow range output converters.

3.2. WIDE BAND GAP DEVICES IN PSFB, LLC AND DAB CONVERTERS

Whereas the Si MOSFETs and more specifically the Si SJ MOSFETs are currently the most mature and cost effective power semiconductor switches in modern SMPS, other alternative superior technologies, like SiC and GaN devices, are becoming increasingly common. Moreover, it is to be expected that thanks to their general adoption their cost will progressively decrease and become a very competitive option in the near future.

Wide Band Gap devices (SiC and GaN) with their most notable intrinsic characteristics (very low Q_{oss} and Q_{rr}) enable alternative design rules for the presented converters in this thesis. For SiC and GaN devices hard-switching and hard-commutation are not as much of a performance or reliability issue as they are for Si devices. Moreover, the driving and switching losses allow the increase in the switching frequency without a major impact in the overall efficiency but with a potential improvement of the maximum achievable power density of the converter.

3.3. PLANAR MAGNETICS

Most of the main transformers in the converters included in this thesis have been realized with a semi-planar construction technique combining Litz wire with planar copper plates. Thanks to the semi-planar arrangement it is possible to interleave in multiple sections the primary and secondary windings, which greatly improves the proximity losses, decreases the leakage inductance and achieves a high window utilization of the transformer.

However, the construction of this type of transformers is still mostly not automated. Therefore it requires of extra assembly effort and cost. Moreover, due to the manual assembly the parameter values and the overall quality has a larger variability than fully automated solutions.

Fully planar magnetics are manufactured with one or several Printed Circuit Boards (PCBs). This alternative construction technique offers several advantages to more traditional arrangements, among them: low profile magnetics, very repeatable and automatable production. Moreover, thanks to the improvements in the PCB manufacturing it is possible to achieve as well very high window utilization. However, although it is possible to interleave primary and secondary windings in many sections, like in the semi-planar arrangement, the fully planar windings are more susceptible than Litz wire to the effect of the stray magnetics fields caused by the gaps or the magnetizing current.

Therefore, it remains a challenge to replace the semi-planar transformers in this thesis with fully planar assemblies achieving equal or better performance in a similar or smaller space.

4. OPENED WORK FOR FUTURE LINES

4.1. CONVERTER DESIGN TOOLS

During the development of the prototypes in this thesis a set of design tools have been created to estimate or predict the efficiency of the converters prior to their construction. During and after the testing, the tools have been continually adjusted to further improve the accuracy and further include observed losses phenomena within the converters.

Some of this tools have been based on analythical closed form expresions for the losses estimation of the different topologies, whereas other of the tools have been based on time domain simulations. Whichever is the approach, it has been observed that achieving the highest efficiency targets requires of accurate modelling and an iterative design process. Moreover, it has been observed that the models have to be proofed within real experimental converters, especially due to sometimes unexpected or unkown losses mechanisms.

Works like the published article in chapter 9 have proben to be very popular and highly accessed by practicing engineers and scholars. In that publication a detailed loss analysis of the PSFB converter and design rules were

given. It is therefore of high interest to continue the development of design tools and the publication of works including detailed loss analysis and design rules for other topologies.

4.2. HIGH FREQUENCY CONVERTERS

Since the power requirements of applications like server, datacenter, telecommunications, adapters, etc. continue to increase, and due to the cost of the infrastructure space or simply due to the convenience of smaller size electronics, the requirements for power density of power supplies also increase continuously.

Achieving higher power densities requires of higher efficiencies. On the one hand, the heat dissipation capabilities of some components is limited by their exposed surfaces and by the cooling system capabilities. On the other hand, the sources of heat are closely packed together, therefore rising the ambient temperature at the power supply level, or at a larger scale, of the infrastructure itself.

Finally, achieving higher power densities requires of higher switching frequencies, which can decrease the volume of the magnetic and/or capacitive energy storage components in the SMPS. However, building a high-frequency and high-efficiency power supply is a great challenge which will continue to be a field of study in the ongoing years, especially due to the adavnces in new semiconductor and magnetic material technologies.

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