Source-to-Drain Tunneling Analysis in FDSOI, DGSOI and FinFET Devices by Means of Multi-Subband Ensemble Monte Carlo

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***Abstract*—The inclusion of quantum effects in the transport direction plays an important role in the extensive research of ultrascaled electronic devices. In this context, it is necessary to study how these phenomena affect different technological architectures in order to conclude which one can be the best candidate to replace standard technology. This work presents the implementation of direct Source-to-Drain Tunneling effect (S/D tunneling) in a Multi-Subband Ensemble Monte Carlo (MS-EMC) simulator showing its influence in different structures such as FDSOI, DGSOI and FinFET devices. The differences in the potential profile and the electron distribution in the subbands for these architectures modify the number of electrons affected by this quantum mechanism and, therefore, their short channel behavior.**

***Index Terms*—direct Source-to-Drain tunneling, Multi–Subband Ensemble Monte Carlo, FDSOI, DGSOI, FinFET.**

I. Introduction

EXTENSIVE research of different technologies and materials has been devoted in the last years to replace the conventional technology and to extend the end of the Roadmap. In the simulation framework, there are two main trends to assess the potential alternatives: first, novel structures are considered to create new transistor architectures [1], [2]; and second, the inclusion of new quantum effects in conventional devices at nanometric scale is required to understand their performance.

Different technological architectures are proposed to overcome the limitations of conventional planar devices. Fully-Depleted Silicon-On-Insulator (FDSOI) devices have been recognized as an alternative to bulk devices. Nonetheless, the utilization of multiple gates surrounding the channel increases the electrostatic confinement and reduces the short-channel effects (SCEs) [3]. If we focus on double gate devices, their gates can be parallel to the standard wafer surface, like the Double-Gate Silicon-On-Insulator (DGSOI); or perpendicular, like the FinFET, as depicted in Figure 1. It should be highlighted that the FinFET is a 3D structure whereas our Multi-Subband Ensemble Monte Carlo (MS-EMC) simulator makes use of a 2D description. However, it was demonstrated that FinFETs with a sufficiently high aspect ratio show similar behavior in all transport regimes when 2DMS-EMC (considering infinite fin height) and other 3D codes are used [4].

Furthermore, in order to improve scalability, quantum effects in the transport direction must be included due to the reduced channel length of current and future devices. In particular, direct Source-to-Drain tunneling (S/D tunneling) has been presented as a scaling limiting effect in ballistic non-equilibrium Green's Function (NEGF) approaches [5]. In addition, it is expected that the MOSFET operation would be distorted at channel lengths around 3nm [6]. When electrons with energy below the injection barrier tunnel, they increase the OFF current with respect to pure thermionic emission. Then, these carriers change the shape of the potential profile, and this in turn reduces again the current, making it closer to the classical limit. This effect is of special interest when the operation regime is near-threshold because the leakage current increases and the threshold voltage (V_{th}) decreases [7].

This work presents a meticulous comparison among FDSOI, DGSOI and FinFET when S/D tunneling is included by means of a MS-EMC simulator. This study is very relevant to determine the impact of this quantum effect on these architectures. It will be shown that the addition of multiple gates combined with their orientation has different influence on the S/D tunneling and, consequently, on the device characteristics.

The structure of this work is organized as follows. Section II gives a detailed overview of the simulator developed to carry out our research. First, introducing the starting point of the simulation framework, and later on, providing an in-depth description of the S/D tunneling algorithm to explain the transmission probability and the motion of an electron experiencing this effect. Results and discussions are detailed in Section III. Finally, in Section IV, the main conclusions are drawn.

II. Simulation Set-up

The fundamentals of the MS-EMC simulator, in which the S/D tunneling effect has been modeled, are based on the mode-space approach of quantum transport [8]. The device structure is divided into slices along the confinement direction where the 1D Schrödinger equation is solved, whereas the 2D Bolzmann Transport Equation (BTE) is computed in the transport plane as shown in Figure 1. Both equations are coupled with the 2D Poisson Equation to keep the self-consistency of the

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solution. This code has already demonstrated its capabilities studying a large range of nanodevices [9], [10], where scattering mechanisms and quantum effects are taken into account. Nevertheless, this tool allows a reasonable computational time thanks to an efficient parallel implementation.

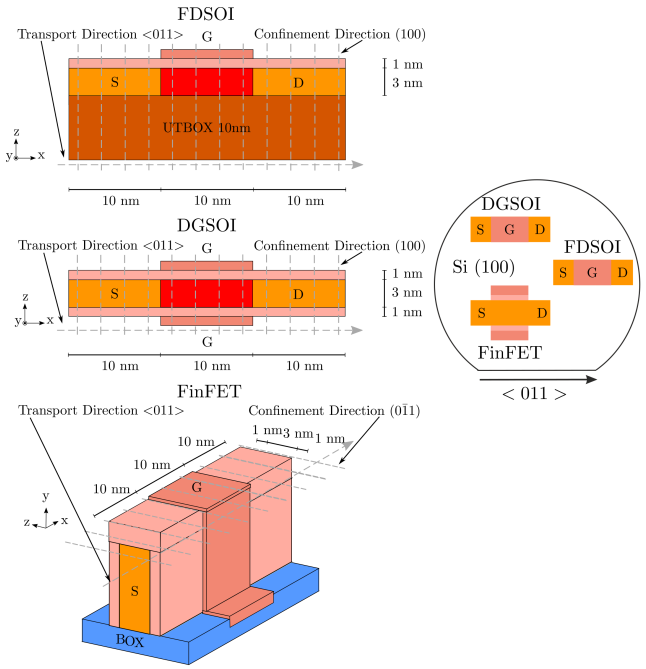

Fig. 1. FDSOI, DGSOI and FinFET structures analyzed in this work with L_G=10nm. 1D Schrödinger equation is solved for each grid point in the transport direction and BTE is solved by the MC method in the transport plane.

A. Description of simulated devices

The performance of FDSOI, DGSOI and FinFET devices is herein analyzed when S/D tunneling is included in order to determine its impact on them. The considered confinement direction of these devices on standard wafers changes from (100) for both planar FDSOI and DGSOI to (0$\bar{1}$1) for FinFET, whereas the transport direction <011> is the same for all of them, as depicted in Figure 1. The difference in the confinement direction modifies the electron distribution in the subbands, and, consequently, the electrostatic potential profile. In addition, the carrier transport effective mass is also modified [11]. Table I summarizes the values of the masses for each device where m_x and m_z are the transport and confinement masses, respectively, and m_y is the one in the direction normal to transport. The subindex of Δ represents the corresponding degeneration factor associated to the different silicon conduction band valleys. Notice that in silicon, $m_l = 0.916m_0$ and $m_t = 0.198m_0$ are the longitudinal and traverse effective masses, respectively, $\frac{2m_l m_t}{m_l+m_t} = 0.326m_0$, $\frac{m_l+m_t}{2} = 0.557m_0$, and m_0 is the electron-free mass.

These devices have been parametrized for gate lengths ranging from 5nm to 20nm. The rest of the technological parameters remains constant, i.e., channel thickness T_{Si}=3nm, Equivalent Oxide Thickness (EOT) of the gate oxide 1nm, and metal gate work function of 4.385eV. A Back-Plane with an

Device	Valley	m_x	m_y	m_z
FDSOI & DGSOI	Δ_2	m_t	m_t	m_l
(100)<011>	Δ_4	$\frac{2m_l m_t}{m_l+m_t}$	$\frac{m_l+m_t}{2}$	m_t
FinFET	Δ_2	m_t	m_l	m_t
(0$\bar{1}$1)<011>	Δ_4	$\frac{m_l+m_t}{2}$	m_t	$\frac{2m_l m_t}{m_l+m_t}$

TABLE I
EFFECTIVE MASSES IN SILICON FOR THE FDSOI, DGSOI AND FINFET DEVICES HEREIN STUDIED WHERE m_x AND m_z ARE THE TRANSPORT AND CONFINEMENT MASSES, RESPECTIVELY, AND m_y IS THE MASS IN THE DIRECTION NORMAL TO TRANSPORT.

UTBOX of 10nm, Back-Bias (BB) polarization of $V_{BB} = 0V$, and Back-Plane (BP) work function of 5.17eV have been chosen for the FDSOI device since a higher BP work function improves the electrostatic control of the channel [12].

B. Description of the model

The standard implementation of the free-flight of an electron in Monte Carlo algorithms establish that its motion finishes due to the random choice of a scattering event. After each flight, the new position of the electron is calculated. If the total energy of an electron is higher than the potential barrier at this new position (Figure 2(a)), the electron goes from source to drain by thermionic emission. On the other hand, if the electron energy is lower than the maximum of the potential barrier (Figure 2(a)), it would either rebound suffering a backscattering, or traverse the potential barrier via S/D tunneling.

The probability of tunneling through the barrier (Figure 2(b)) is equivalent to the transmission coefficient: it determines the fraction of electrons experiencing S/D tunneling at a given energy lower than the top of the potential barrier. The tunneling probability of the electron T_{dt} is calculated using the WKB approximation [13]:

$$T_{dt}(E) = \exp\left\{-\frac{2}{\hbar}\int_a^b \sqrt{2m^*_{tr}(E_i(x) - E_x)}\,dx\right\} \quad (1)$$

where *a* and *b* are the starting and ending points; E_x is the total energy in the transport plane considering only the component of the kinetic energy in the direction that faces the potential barrier; m^*_{tr} is the transport effective mass of the electron; and $E_i(x)$ is the energy of the *i-th* subband. This approximation has already been used to study S/D tunneling in other electronic devices [14].

Once the tunneling probability is known, a rejection criterion is used to determine whether the electron will tunnel or not. A uniformly distributed random number r_{dt} between 0 and 1 is generated and compared to T_{dt} (Figure 2(b)). If $r_{dt} > T_{dt}$, the electron will turn back with $v_{\leftarrow}(x) = -v_{\rightarrow}(x)$ suffering a backscattering (Figure 2(c)). Otherwise, if $r_{dt} \leq T_{dt}$, the electron will go through the barrier and the particle will be marked to indicate that it experiences S/D tunneling (Figure 2(d)).

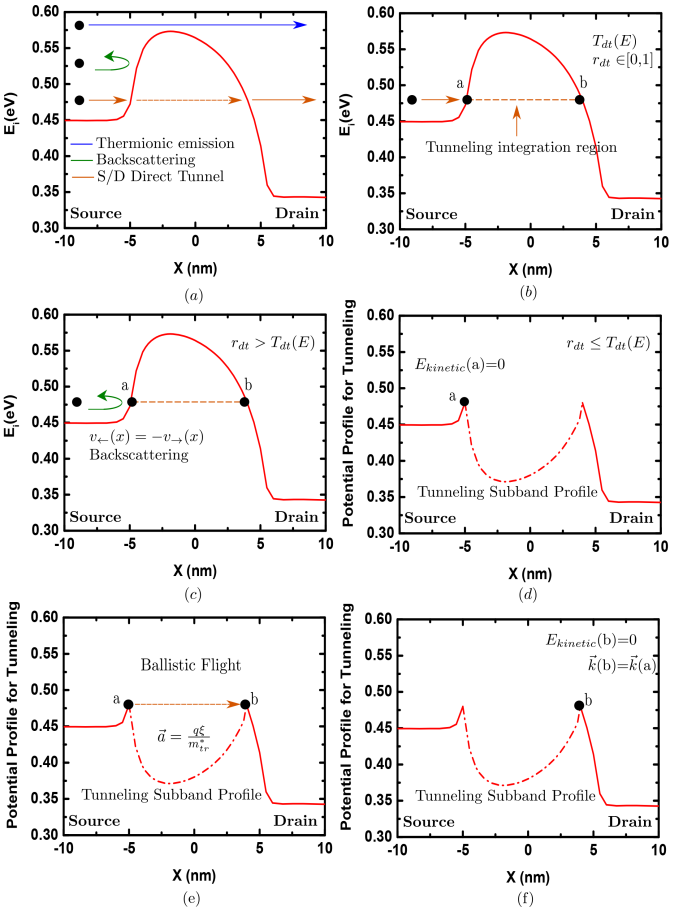

Fig. 2. Representation of the tunneling model. If the total energy of an electron used for tunneling, which corresponds to the total energy in the transport plane considering only the component of the kinetic energy in the direction that faces the potential barrier, is higher than the potential barrier at this new position, the electron goes from source to drain by thermionic emission (a). Otherwise, it would either traverse the potential barrier via S/D tunneling (b), or rebound from it suffering a backscattering (c). In order to choose between these last two phenomena ((b) and (c)), a uniformly distributed random number r_{dt} between 0 and 1 is generated and compared to T_{dt} (b). If $r_{dt} > T_{dt}$, the particle rebounds. If $r_{dt} < T_{dt}$, it undergoes S/D tunneling. For this last scenario, the potential barrier is inverted, the particle is placed at the starting point *a* (d), and it follows a classical path obeying Newton's second law of motion (e) until it reaches the ending point *b* (f).

Several assumptions have been made in the aforementioned method to improve the calculation of T_{dt}. First, the exact starting and ending points through which the electron crosses the barrier are calculated in order to reduce the rounding errors coming from the discretization. Second, a maximum tunneling rejection length is also introduced (L_{max}) to avoid computing a large number of negligible probabilities. In our work, L_{max} has been chosen to match the channel length dimensions. Third, the comparison between r_{dt} and T_{dt} has been included after each integration step in order to decrease the computational effort.

Let us now describe the process for the tunneling path estimation. The first step is to provide a realistic model for the motion of the particle. To do so, two assumptions can be made, leading to two different scenarios. The first one establishes that the electron goes directly from the starting point to the ending point within the same time step. Therefore the electron will not stay inside the potential barrier. This instantaneous tunneling (IT) model is unrealistic and non self-consistent because it assumes negligible tunneling time; whereas steady-state full-quantum simulations show some charge inside the barrier. Nevertheless, this IT model has been considered here as a limit of the S/D tunneling. For this reason, a more realistic second assumption called ballistic tunneling (BT) model is used in this work considering that electrons fly through the potential barrier during a certain period of time. This last idea has been employed in several works allowing the possibility of electrons flying into forbidden regions [15]. For this second approach, and assuming that electrons reach the potential barrier perpendicularly to it, they will be regarded as moving according to Newton's Mechanics in an inverted potential profile $V(\vec{r}) \rightarrow -V(\vec{r})$, Figure 2(d).

This foregoing BT model has been chosen because it mimics the motion of an electron in a forbidden region with imaginary $\vec{k}$. In particular, it is an extension of the non-local band-to-band tunneling algorithm (BTBT) described in [16]. The main advantage of this choice is that, once it has been implemented in the simulator, it can be extended to our S/D tunneling since both mechanisms rely on the same principles.

Regarding the motion inside the barrier, the electron is considered as drifted in a conservative field. As a consequence, the angle, which determines the k_x-k_y relationship, is maintained at the starting point *a* before entering inside the potential barrier.

This classical trajectory is determined as follows [7], [17]. First, a hypothetical particle is placed at the starting point *a* with zero kinetic energy (Figure 2(d)). Then, it accelerates according to Newton's second law of motion, where ξ is the electric field (Figure 2(e)), and without any scattering. Finally, it reaches the ending point *b* with zero kinetic energy (Figure 2(f)) and continues flying with the same dynamics that it previously had outside the barrier.

In order to assess the accuracy of the aforementioned approach, the simulation results have been compared to those obtained with 2D NEGF simulation of ultrathin DGSOI devices considering ballistic transport [18]. They showed a good agreement especially for the degradation in the subthreshold region.

III. Results and Discussion

This section has been divided into two stages: first, we perform a meticulous study of how the two different assumptions of the electron motion inside the potential barrier can substantially modify the device performance and, second, we study the influence of S/D tunneling in the three devices under consideration: FDSOI, DGSOI and FinFET.

Figure 3 shows the difference in the subband profile of the lowest energy subband in a FinFET when IT and BT are considered in contrast with a simulation without S/D tunneling. The potential barrier increases its height when the electrons fly inside the forbidden region, contrary to what happens for the IT.

As derived from Equation 1, either longer tunneling paths, higher potential barriers or larger m^*_{tr} values, produce smaller

tunneling probabilities. Accordingly, a narrower potential barrier obtained when the IT model is considered, provides a larger T_{dt} due to the resulting shorter tunneling path. Therefore, the percentage of electrons near the potential barrier affected by S/D tunneling (Figure 4) is much higher compared to the BT model.

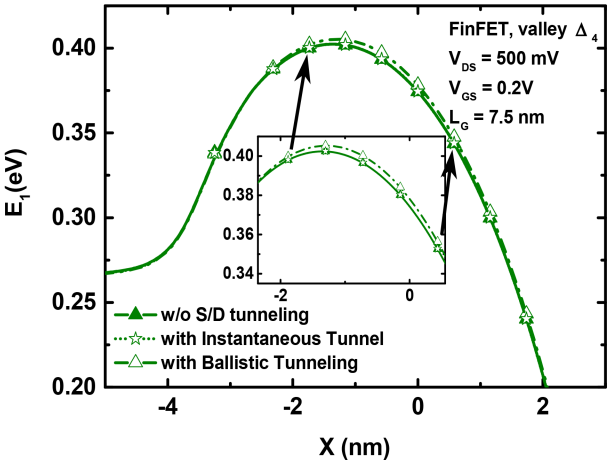

Fig. 3. Energy profile of the lowest energy subband in the 7.5nm device for a FinFET (valley Δ_4) with instantaneous tunnel, with ballistic tunneling model (considering the motion of the electrons inside the potential barrier) and w/o S/D tunneling. $V_{GS} = 0.2V$ and $V_{DS} = 500mV$.

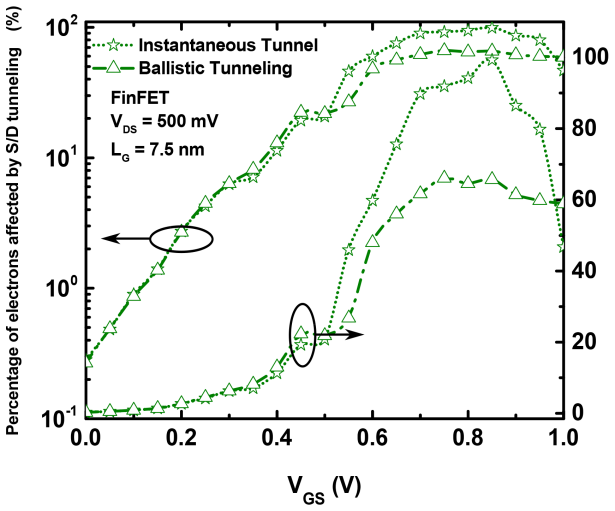

Fig. 4. Percentage of electrons affected by S/D tunneling near the potential barrier as a function of V_{GS} in a FinFET with L_G=7.5nm at $V_{DS} = 500mV$ for both the instantaneous and the ballistic tunneling.

This quantum effect produces a modification of the $I_D - V_{GS}$ characteristics (Figure 5) obtained from both IT and BT criteria. In general, the drain current in Monte Carlo simulators is calculated by the spatial average of the electron current along the channel. Consequently, the number of electrons located inside the potential barrier due to the BT model will contribute in Monte Carlo to the total current increasing it. The differences between curves, observable at low and high V_{GS} regimes, have different explanations as detailed in what follows. In the subthreshold regime, S/D tunneling implies an increase of the drain current because thermionic emission is low. On the other hand, when thermionic emission dominates the current, the fraction of particles that undergo this quantum effect proves to be negligible. For this last reason, and for high gate bias, although IT shows a larger percentage of electrons affected by S/D tunneling, the existence of charge inside the barrier (because the BT percentage is also appreciable) leads to a small increase of the current when computed by the Monte Carlo simulator. Therefore, this phenomena is more relevant at subthreshold regime.

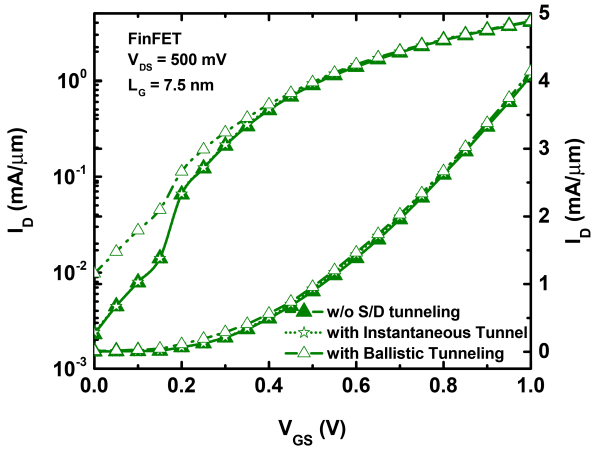

Fig. 5. I_D vs. V_{GS} in the 7.5nm device for a FinFET at $V_{DS} = 500mV$ for both the instantaneous and the ballistic tunneling.

From now on, and due to the differences in the curves, suggesting that the IT model is not an adequate approximation, we will hereafter focus on the more realistic BT model. Figure 6 depicts the energy profiles of the lowest energy subband for a simulation considering S/D tunneling in FDSOI, DGSOI, and FinFET devices, as well as the electron distribution from the fundamental subband as a function of the total energy.

Notice that the lowest energy subband changes from Δ_2 in both FDSOI and DGSOI transistors to Δ_4 in the FinFET. The difference in the device orientation also alters the average effective transport mass of the electrons, labeled m_x in Table I, being higher for the FinFET than for both the FDSOI and the DGSOI. This statement can be extended for the less populated valleys: Δ_2 in FinFET and Δ_4 in FDSOI and DGSOI devices.

A comparison between FDSOI and DGSOI devices with the same confinement direction and the same m^*_{tr}, shows that the higher and larger energy profile of the DGSOI (Figure 6) decreases T_{dt}. For this reason, a larger number of electrons rebounds at the potential barrier for the DGSOI compared to the FDSOI. In spite of the similar energy profile between the DGSOI and the FinFET (Figure 6), which means similar tunneling length at a given starting point *a*, the higher potential barrier for the DGSOI makes T_{dt} lower. However, the larger m^*_{tr} (Table I) for the FinFET orientation significantly reduces the tunneling probability. As a consequence, the number of particles affected by S/D tunneling is lower in the FinFET compared to the DGSOI due to the higher relevance of m^*_{tr} in the computation of T_{dt}.

The percentage of electrons near the potential barrier affected by S/D tunneling as a function of the gate length is

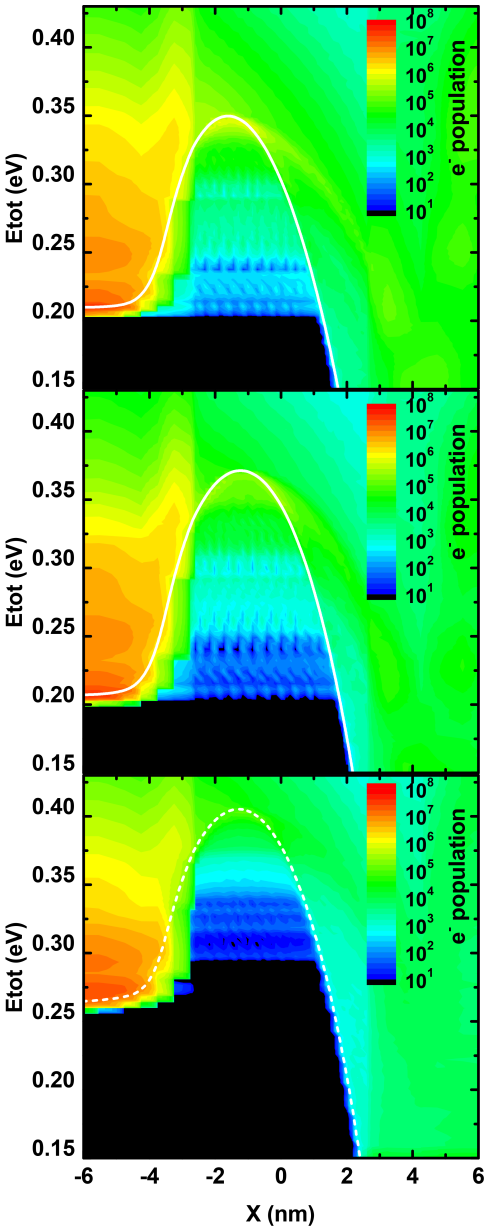

Fig. 6. Electron distribution in arbitrary units in the lowest energy subband of the valley Δ_2 (solid) and of the valley Δ_4 (dashed) as a function of total energy in the 7.5nm device including S/D tunneling for FDSOI (top), DGSOI (middle), and FinFET (bottom) with $V_{GS} = 0.2V$ and $V_{DS} = 500mV$.

shown in Figure 7 at $V_{GS} = 0.2V$ due to the importance of this phenomenon in the sub-threshold regime. Note that Figure 7 shows the percentage of electrons affected by S/D tunneling near the potential barrier and not their total value. This means that the number of electrons experiencing this phenomenon is compared to the electrons rebounding from the potential barrier and to those with higher energy than that of the potential barrier. In general terms, the percentage is larger at saturation regime due to the reduction of the potential profile. In this scenario, the larger m^*_{tr} of the FinFET reduces the importance of S/D tunneling compared to both the FDSOI and the DGSOI at any drain bias and any L_G. Moreover, it is almost negligible in the case of the FinFET with L_G >7.5nm.

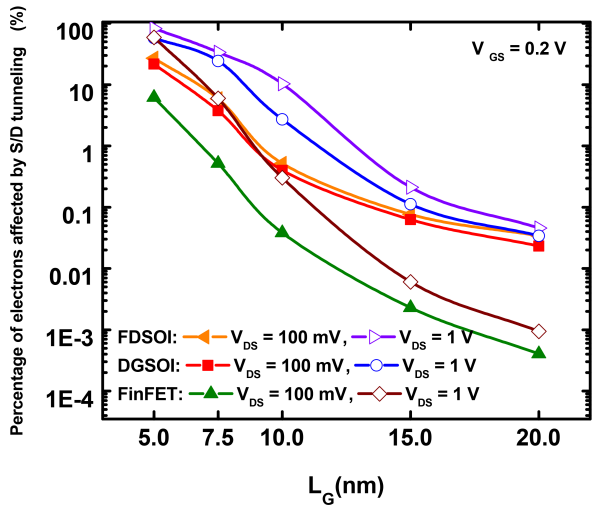

Fig. 7. Percentage of electrons affected by S/D tunneling near the potential barrier as a function of L_G for FDSOI, DGSOI, and FinFET at low drain bias and saturation conditions with $V_{GS} = 0.2V$.

The impact of S/D tunneling on the threshold voltage variation (ΔV_{th}) can be observed in Figure 8. V_{th} has been calculated in this work according to the constant drain current method [19]. The percentage of electrons affected by S/D tunneling near the threshold voltage is higher for V_{DS}=1V than for low drain bias owing to electrostatic variations when the drain bias is increased. Thus, the reduction of V_{th} when this type of tunneling is taken into account is intensified for higher V_{DS}. This effect becomes more relevant when the device size is reduced. However, the influence of this quantum effect is lower in the DGSOI and the FinFET due to the better control on the SCEs.

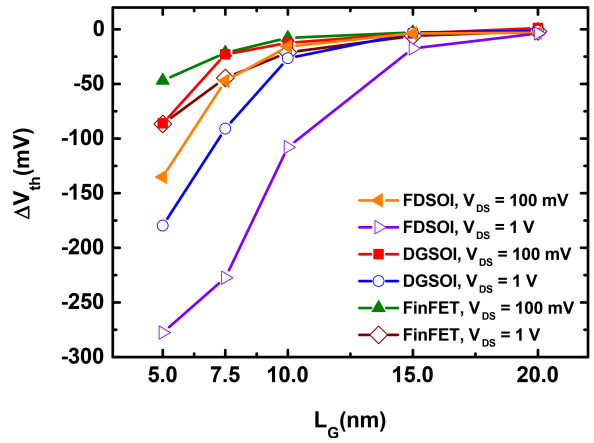

Fig. 8. Difference between the threshold voltage (ΔV_{th}) of a simulation considering S/D tunneling and w/o it as a function of L_G for FDSOI, DGSOI, and FinFET at low drain bias and saturation conditions.

The Drain Induced Barrier Lowering (DIBL) is one of the main parameters used to determine the impact of SCEs when devices are scaled down. Figure 9 shows the DIBL dependence on the channel length when S/D tunneling is considered in the simulations. Observe that this inclusion entails a higher DIBL in the three devices especially for lower gate lengths.

The difference between V_{th} with and without S/D tunneling is more pronounced for higher drain biases (Figure 8) and, therefore, this produces a DIBL increase when S/D tunneling is considered. Lower DIBL means that the degradation caused by the drain voltage is lower. This effect can affect negatively the device performance when its dimensions are scaled down, especially for applications where an increase of I_{OFF} can be very harmful.

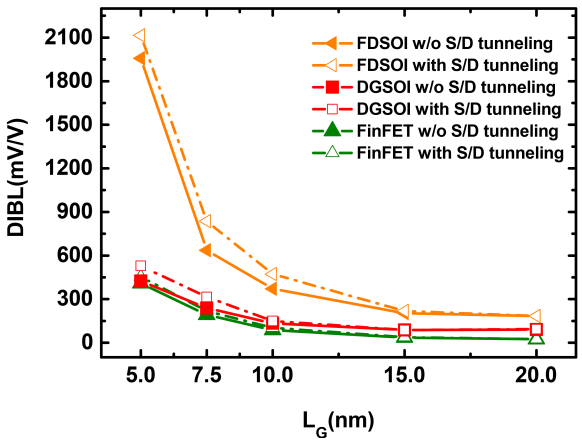

Fig. 9. DIBL as a function of L_G considering both simulations with and w/o S/D tunneling for FDSOI, DGSOI, and FinFET.

Another important parameter that provides information about the device performance is the $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio, where I_{ON} and I_{OFF} are the highest and lowest attainable currents of the devices, respectively ($I_{\mathrm{ON}} = I_D$ when $V_{GS} = V_{DS} = 1V$; $I_{\mathrm{OFF}} = I_D$ when $V_{GS} = 0V$ and $V_{DS} = 100mV$). Ideally, the best device would be the one with the highest $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio. This parameter is depicted in Figure 10 as a function of the channel length for both situations. Notice how the FinFET features a much higher ratio than the other devices. The main difference in the $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio between the three devices lies in the very low I_{OFF} for the FinFET in comparison to the FDSOI and the DGSOI. The change in the confinement direction modifies the device characteristics such as the subband profile or the scattering rates. These changes increase the number of particles with high energy, which implies higher velocities in the channel for very low V_{GS} in the FDSOI and DGSOI. Therefore, as the drain current is estimated in Monte Carlo simulators by multiplying the average number of particles by their velocity, the total current for both SOI devices turns out to be higher.

As a result of the increasing number of particles flowing from source to drain at low gate bias with S/D tunneling enabled, I_{OFF} increases. However, at higher gate bias, the number of electrons near the potential barrier with low energy is reduced and thus there is almost no difference in the I_{ON} current between the simulations with and w/o S/D tunneling. The result is that the $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio decreases when this quantum phenomenon is incorporated, being the FinFET structure the one featuring the higher difference between both scenarios as it is clearly shown in Figure 10.

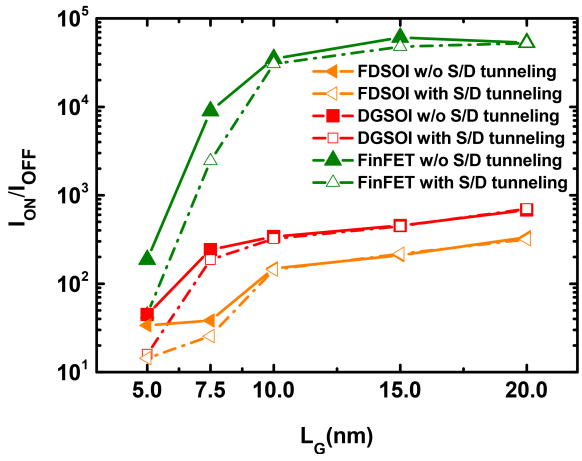

Fig. 10. $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ as a function of L_G considering both simulations with and w/o S/D tunneling for FDSOI, DGSOI, and FinFET.

IV. Conclusions

This work implements S/D tunneling in an existing MS-EMC tool considering two different criteria for the particle motion accounting for it. Our calculations show that the model including the flight of the electrons inside the forbidden region increases the potential barrier compared to the instantaneous tunneling model. Therefore, this last model produces a higher T_{dt} compared to the ballistic one, and overestimates the number of particles suffering it. A comparison of S/D tunneling impact on FDSOI, DGSOI and FinFET devices has been performed. The difference in the energy profiles and the change in the confinement directions among them modify the tunneling probabilities, decreasing them for higher potential barriers and larger transport masses, which are the cases for the DGSOI and the FinFET, respectively. In conclusion, the number of particles experiencing S/D tunneling is lower in FinFET and very similar for both FDSOI and DGSOI devices. The FinFET shows less degradation than the others at any bias regime enabling a better control of the SCEs.

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