electronics

MDPI

Review

Memcapacitor and Meminductor Circuit Emulators: A Review

Francisco J. Romero [1,2,*], Akiko Ohata [3], Alejandro Toral-Lopez [1,2], Andres Godoy [1,2], Diego P. Morales [1,4] and Noel Rodriguez [1,2,*]

1 Department of Electronics and Computer Technology, Faculty of Sciences, University of Granada, 18071 Granada, Spain; atoral@ugr.es (A.T.-L.); agodoy@ugr.es (A.G.); diegopm@ugr.es (D.P.M.)
2 Pervasive Electronics Advanced Research Laboratory, University of Granada, 18071 Granada, Spain
3 Institute of Space and Astronautical Science, Japan Aerospace Exploration Agency, Kanagawa 252-5210, Japan; ohata@post.kek.jp
4 Biochemistry and Electronics as Sensing Technologies Group, University of Granada, 18071 Granada, Spain
* Correspondence: franromero@ugr.es (F.J.R.); noel@ugr.es (N.R.)

Abstract: In 1971, Prof. L. Chua theoretically introduced a new circuit element, which exhibited a different behavior from that displayed by any of the three known passive elements: the resistor, the capacitor or the inductor. This element was called memristor, since its behavior corresponded to a resistor with memory. Four decades later, the concept of mem-elements was extended to the other two circuit elements by the definition of the constitutive equations of both memcapacitors and meminductors. Since then, the non-linear and non-volatile properties of these devices have attracted the interest of many researches trying to develop a wide range of applications. However, the lack of solid-state implementations of memcapacitors and meminductors make it necessary to rely on circuit emulators for the use and investigation of these elements in practical implementations. On this basis, this review gathers the current main alternatives presented in the literature for the emulation of both memcapacitors and meminductors. Different circuit emulators have been thoroughly analyzed and compared in detail, providing a wide range of approaches that could be considered for the implementation of these devices in future designs.

Keywords: emulator; gyrator; memcapacitor; meminductor; memristor

Citation: Romero, F.J.; Ohata, A.; Toral-Lopez, A.; Godoy, A.; Morales, D.P.; Rodriguez, N. Memcapacitor and Meminductor Circuit Emulators: A Review. *Electronics* **2021**, *10*, 1225. https://doi.org/10.3390/electronics10111225

Academic Editors: Chun Sing Lai, Zhekang Dong and Donglian Qi

Received: 15 April 2021
Accepted: 18 May 2021
Published: 21 May 2021

1. Introduction

Prof. Leon L. Chua presented in 1971 the theoretical definition of the two terminal device which defined the relation between the time-integral of its input voltage (ϕ, flux) and its electric charge (q) [1]. This element was called *memristor* given that its behavior corresponds to a nonlinear resistor in which the current through its terminals at an instant t_1 depends not only on the input voltage at t_1, but also on the input voltage from $t = -\infty$ to $t = t_1$ (i.e., a resistor whose resistance depends on the history of its input). It was also demonstrated that this element was passive and that, contrary to capacitors and inductors, it cannot store energy. Therefore, as a manifestation of these characteristics, the current of the memristor is zero whenever the input voltage is zero and, for a periodic current input, the memristive systems show a "closed pinched hysteretic loop" in their *i-v* characteristic [2].

However, until 2008 the investigation into the memristor concept was very limited due to the lack of a solid-state implementation of this device [3–6]. However, it was in 2008 that a group of researchers of Hewlett Packard Labs announced the first solid-state device fulfilling the theoretical definition of the memristor [7], which constituted a turning point in the research of memristors and its applications. Since then, thanks to its non-volatility and non-linear behavior, the memristor is expected to play a disruptive role in diverse fields, such as neuromorphic circuits and neural networks [8–12], analog programmable circuits and arithmetic circuits [13–16], logic gates [17], crossbar classifiers [18–20], adaptive filters [21], chaotic circuits [22,23] and non-volatile memories [24–26]. This had led to

intensive studies of the memristive behavior in a wide range of materials, such as transition metal oxides (e.g., NiO and TaO_x) [27,28], polymers [29], 2D materials [30] or graphene oxide [31–33], among others. The success of the memristor led Di Ventra, Pershin and Chua to extended the concept of the memory circuit elements to capacitive and inductive systems, thus defining the memcapacitor and the meminductor, respectively [34]. In this way, together with the memristor, they established the electrical relations between the time-integral of the charge (σ) and the flux (ϕ) with the memcapacitor; and between the time-integral of the flux (ρ) and the charge (q) with the meminductor (see Figure 1).

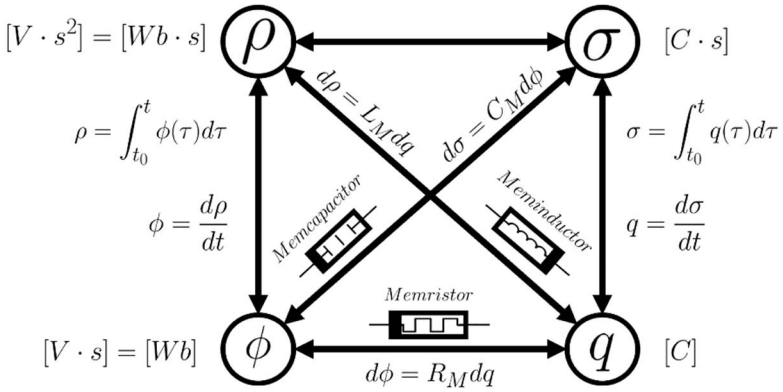

Figure 1. Mem-elements definition on the basis of their fundamental physical magnitudes (units are presented in brackets). Memristor: relation between the charge (q) and the time-integral of the voltage (ϕ); memcapacitor: relation between time-integral of the charge (σ) and the time-integral of the voltage (ϕ); meminductor: relation between time-integral of the flux (ρ) and the charge (q) [35].

As in the case of memristors, memcapacitors and meminductors also present a memory ability manifested through a closed pinched hysteresis loop in the characteristic of their two constitutive variables; with the additional advantage of being capable of storing energy in capacitive and inductive forms, respectively [36]. These devices are expected to be the key for the emergence of a new form of computation called neuromorphic computing, since their essential properties are envisaged to allow them to mimic biological computing. Thanks to their ability to both store and process information simultaneously, computers based on these mem-elements would offer capabilities and power consumption comparable to those of the human brain [37–39]. However, the lack of solid-state implementations of memcapacitors and meminductors hinders the exploitation of the prominent features of these devices in practical implementations. Due to this, in recent years there has been an emerging line of research dedicated to the development of emulators of these devices, i.e., circuits that satisfy the constitutive equations of the emulated mem-element.

In this context, this work reviews the different models and practical memcapacitor and meminductor emulators presented in the literature. Thus, the different approaches followed for the emulation of the memory effect and nonlinear behavior of these devices have been analyzed in detail and in a comparative way. The manuscript is structured as follows: after this introduction, Section 2 presents the concept of memcapacitance as well as the different approaches proposed for the emulation of memcapacitors. Similarly, Section 3 introduces the concept of meminductive system and the different alternatives adopted for the emulation of meminductors. Moreover, those circuits that based on the same design are able to emulate either a memcapacitor or a meminductor with minimal changes in their design have been grouped in Section 4. Finally, the main conclusions of the different emulation approaches are drawn in Section 5.

2. Memcapacitor Emulators

The general memcapacitance (C_M) is defined as the nth-order system that establishes a nonlinear relation between the charge of the device (q) and its input voltage (v) [34]. It can be either voltage-controlled or charge-controlled depending on its constitutive input

variable. Therefore, an *n*th-order voltage-controlled memcapacitive system can be defined by Equation (1):

$$q(t) = C_M\left(\vec{x_N}, v, t\right)\cdot v(t) \tag{1}$$

whereas the *n*th-order charge-controlled memcapacitance systems are defined by Equation (2):

$$v(t) = C_M^{-1}\left(\vec{x_N}, q, t\right)\cdot q(t) \tag{2}$$

being $\vec{x_N}$ a vector that represents the n internal state variables of the system.

The memcapacitor is a particular case of memcapacitive system with one single state variable; the voltage in the case of voltage-controlled memcapacitors, Equation (3), or the charge in the case of charge-controlled memcapacitors, Equation (4).

$$q(t) = C_M\left[\int_{t_0}^{t} v(\tau)d\tau\right]\cdot v(t) \tag{3}$$

$$v(t) = C_M^{-1}\left[\int_{t_0}^{t} q(\tau)d\tau\right]\cdot q(t) \tag{4}$$

In the previous equations, the initial instant of time, t_0, may be selected to ensure that $\int_{-\infty}^{t_0} v(\tau)d\tau = 0$ and $\int_{-\infty}^{t_0} q(\tau)d\tau = 0$, respectively.

Therefore, the memcapacitors are nothing but capacitors whose capacitance depends on the history of the constitutive variable that acts as input (either charge or voltage) and whose q-v characteristic presents a closed-pinched hysteresis loop in which $v = 0$ whenever $q = 0$ (and vice versa) for bipolar sine wave-like excitations. In this way, the memcapacitor emulators must be able to monitor the control variable (q or v) and then change its input capacitance according to the history of this variable. Therefore, the memcapacitor emulators can also be either voltage- or charge-controlled.

An example of charge-controlled memcapacitor emulator is the one proposed by Fouda and Radwan in Ref. [40], and shown in Figure 2. This circuit is based on the mathematical model of charge-controlled memcapacitance introduced by Biolek et al. [41], which is given by Equation (5):

$$\frac{1}{C_M(t)} = \frac{1}{C_0} + k'\int_0^t q(\tau)\tau \tag{5}$$

where C_0 corresponds to the initial capacitance and k' is the mobility factor.

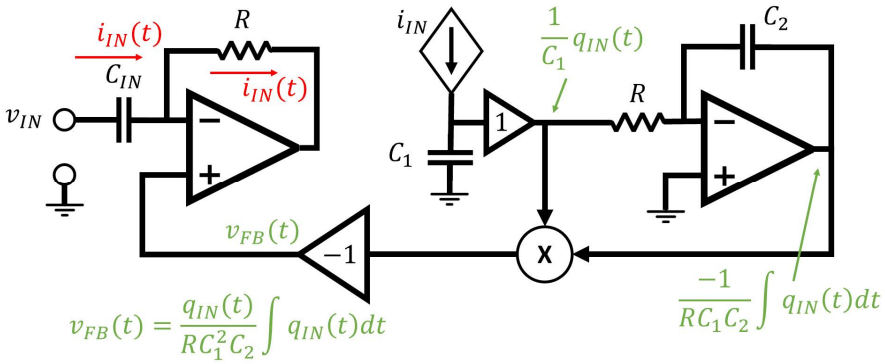

Figure 2. Memcapacitor emulator circuit proposed by Fouda and Radwan [40].

This emulator is designed to achieve the behavior indicated in Equation (5) from the input current of the circuit, then:

$$\begin{aligned} v_{IN}(t) = \frac{1}{C_{IN}} \int i_{IN}(t)dt + v_{FB}(t) = \frac{q(t)}{C_{IN}} + v_{FB}(t) = \frac{q(t)}{C_{IN}} + k'q(t) \int_0^t q(\tau)d\tau \\ = \frac{q(t)}{C_{IN}} + \frac{q(t)}{RC_2C_1^2} \int_0^t q(\tau)d\tau \end{aligned} \quad (6)$$

Note that this circuit requires implementing a copy of the injected current in order to obtain the input charge and its integration; besides, it is limited for the emulation of grounded memcapacitors. The circuit of Figure 2 was simulated using SPICE, demonstrating that it certainly behaves as a charge-controlled memcapacitor for a frequency of 10 Hz resulting in a good agreement with the mathematical derivation. However, there is a lack of physical implementation of this design demonstrating its actual performance.

A similar approach, but without the drawback of requiring a copy of the input current, was proposed by Sah et al. in Ref. [42] and it is presented in the circuit of Figure 3 which, following the same principle than the previous design, can be modelled as follows:

$$\begin{aligned} v_{IN}(t) = \frac{1}{C_1} \int i_{IN}(t)dt - v_{FB}(t) = \frac{q(t)}{C_1} - v_{FB}(t) = \frac{q(t)}{C_1} - k'q(t) \int_0^t q(\tau)d\tau \\ = \frac{q(t)}{C_1} + \frac{q(t)}{RC_2C_1^2} \int_0^t q(\tau)d\tau \end{aligned} \quad (7)$$

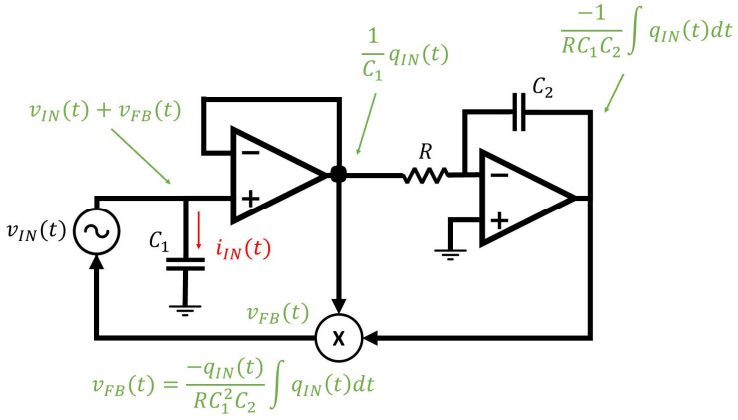

Figure 3. Memcapacitor emulator circuit proposed by Sah et al. [42].

Their authors validated this proposal through both SPICE simulations and experimental results, demonstrating that this model is able to emulate a charge-controlled memcapacitor at input frequencies ranging from 0.1 Hz to 25 Hz. Hence, this circuit was able to provide a similar behavior to the previous one with a simplified design.

Another alternative to emulate grounded memcapacitors was proposed by Romero et al. in Ref. [43], although in this case for voltage-controlled memcapacitors. This emulator was implemented by relating the memcapacitance concept with the Miller effect, which accounts for the amplification of the feedback capacitance in inverting voltage amplifiers Equation (8).

$$Z_{IN} = \frac{\boldsymbol{V}_{IN}}{\boldsymbol{I}_{IN}} = \frac{\boldsymbol{V}_{IN}}{\mathrm{j}\omega C_1(\boldsymbol{V}_{IN} - \boldsymbol{V}_{OUT})} = \frac{1}{\mathrm{j}\omega C_1(1+A)} = \frac{1}{\mathrm{j}\omega C_{IN}} \quad (8)$$

On the basis of Equation (8), the authors proposed a gain, A, which depends on the time-integral of the input voltage (i.e., the flux). To do so, they used a voltage-controlled resistor, as shown in Figure 4a, to change the amplifier's voltage gain according to the

flux, hence satisfying the definition of the voltage-controlled memcapacitor, as derived in Equation (9).

$$\begin{aligned} \frac{d\sigma_{IN}}{dt} = \boldsymbol{q_{IN}(t)} &= \int i_{IN}(t)dt \\ &= \int C_1 \frac{dv_{C1}(t)}{dt}dt = C_1(v_{IN}(t) - v_{out}(t)) = C_1(1 + A(\phi))v_{in}(t) \\ &= \boldsymbol{C_M(\Phi)v_{IN}(t)} \end{aligned} \tag{9}$$

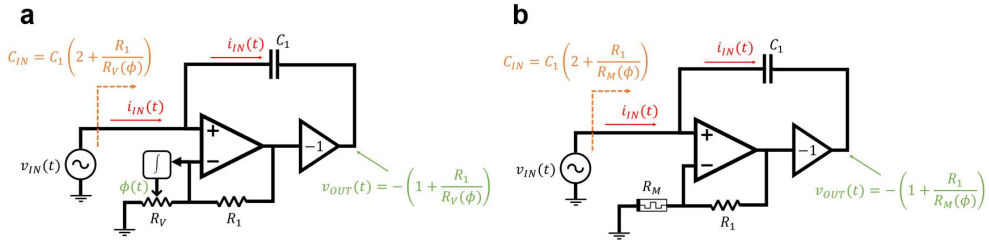

Figure 4. Memcapacitor emulator circuit proposed by Romero et al. [43] implemented with a voltage-controlled resistor (**a**) and with a voltage-controlled memristor (**b**).

In the case of the implementation shown in Figure 4a, the resulting memcapacitance is given by:

$$C_M(\phi) = C_1\left(2 + \frac{R_1}{R_V(\phi)}\right) \tag{10}$$

Additionally, having a voltage-controlled resistor whose value changes according to the input flux (which is actually the time-integral of its input) makes also feasible the implementation of this circuit by means of a memristor, as depicted in Figure 4b. In this case, the memcapacitance could be expressed as indicated in Equation (11). Circuits such as this one are considered as electrical mutators since, according to Equation (9) and Equation (11), they transform the constitutive equation of the memristor ($R_M = \frac{d\phi}{dq}$) into a memcapacitor with its own constitutive relation ($C_M = \frac{d\sigma}{d\phi}$).

$$C_M(\phi) = C_1\left(2 + \frac{R_1}{R_M(\phi)}\right) \tag{11}$$

The feasibility of this implementation was demonstrated by SPICE simulations for different input waveforms at a frequency of 50 Hz, as well as by means of its physical implementation in a field-programmable analog array (FPAA) using a controlled-gain amplifier.

Actually, the use of mutators is a common approach for the implementation of memcapacitor emulators. Another example of this kind is the design proposed by Wang et al. in Ref. [44] to emulate voltage-controlled memcapacitors. In this work, the authors relied on the use of two commercially available second-generation current conveyors (CCII) AD844 in combination with a memristor, as shown in Figure 5a.

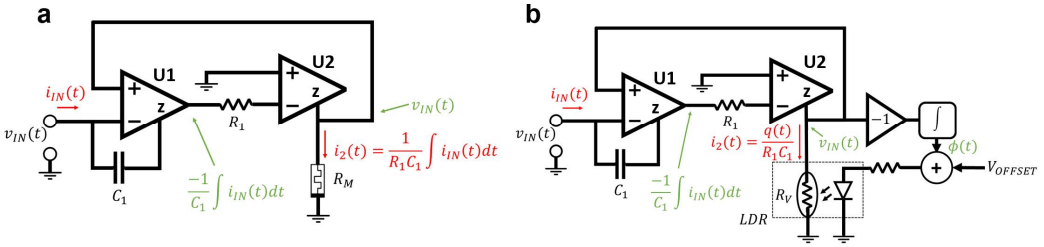

Figure 5. (**a**) Memcapacitor emulator circuit proposed by Wang et al. [44] implemented with a voltage-controlled memristor. (**b**) Memcapacitor emulator schematic using a memristor emulator based on a LED optically coupled to a LDR (light-dependent resistor).

In this circuit, the capacitor C_1 and the first CCII are used to obtain a voltage proportional to the integration of the input current (i.e., proportional to the charge). After that, the second CCII allows to convert that voltage to current, given that $I_Z = -I_-$ and $V_- = V_+$:

$$i_2(t) = I_{Z_2} = \frac{-v_{out_1}}{R_1} = \frac{1}{R_1 C_1}\int_{t_0}^{t} i_{IN}(\tau)d\tau = \frac{q(t)}{R_1 C_1} \tag{12}$$

Therefore, the relation between the current and the voltage across the memristor can be expressed as follows:

$$R_M(\phi) = \frac{v_{IN}(t)}{i_2} = \frac{v_{IN}(t)R_1 C_1}{q(t)} \tag{13}$$

As seen, from the constitutive equation of the memristor we can get the equivalent memcapacitance of this circuit, which is given by Equation (14).

$$C_M(\phi) = \frac{R_1 C_1}{R_M(\phi)} \tag{14}$$

Moreover, the authors presented in this work a novel approach for dealing with both voltage-dependent resistors and/or voltage-controlled memristors (see Figure 5b). This approach is based on a LED optically coupled with a LDR (light-dependent resistor) and, as it will be shown later, it has been adopted for other authors for the implementation of their emulators. However, it is important to highlight that this approach limits the upper frequency of the emulator, since the LDRs usually suffer from a slow time-response.

The use of current conveyors to implement mutators was theoretically introduced by Pershin and Di Ventra in Ref. [45], and since then it has been adopted by many authors in the literature. One of the benefits of using current conveyors relies on the possibility to implement floating memcapacitors, as shown in Figure 6.

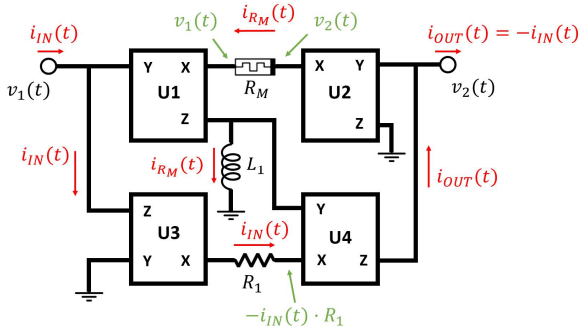

Figure 6. Memcapacitor emulator circuit proposed by Pershin and Di Ventra [45].

In the circuit of Figure 6, the current through the memristor corresponds to the current through the inductor L_1, and therefore:

$$v_{L1}(t) = -i_{IN}(t)\cdot R_1 = L_1 \cdot \frac{d\left(i_{R_M}(t)\right)}{dt} = \frac{L_1}{R_M(\phi)} \cdot \frac{d(v_2(t) - v_1(t))}{dt} = \frac{-L_1}{R_M(\phi)} \cdot \frac{d(v_{IN}(t))}{dt} \tag{15}$$

which indicates that this circuit emulates a voltage-controlled memcapacitor whose memcapacitance is given by Equation (16).

$$C_M(\phi) = \frac{L_1}{R_1 R_M(\phi)} \tag{16}$$

A similar approach to the one proposed in this work was followed by Yu et al. for the implementation of a practical emulator based on this model [46]. However, their proposal presents the drawback of requiring the use of a custom implementation of memristor emulator, which does not guarantee the equality between the input and output current of its two terminals.

There are additional works that also make use of current conveyors for the practical implementation of emulators without the requirement of including any memristor or memristor emulator. This is the case of the grounded memcapacitor emulator presented by Yesil and Babacan in Ref. [47] and schematized in Figure 7.

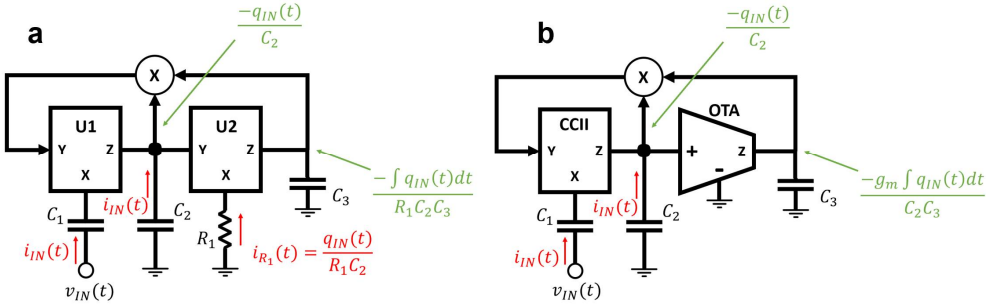

Figure 7. Memcapacitor emulator circuit proposed by Yesil and Babacan [47]. (**a**) Implementation based on only CCII, (**b**) implementation based on a CCII-OTA combination.

In this emulator, the memcapacitance can be derived from the input current, which can be expressed as:

$$i_{IN}(t) = C_1 \frac{d\left(v_{IN}(t) - \frac{q(t)}{R_1C_2^2C_3}\int q(t)dt\right)}{dt} \tag{17}$$

and, therefore, the equivalent charge-controlled memcapacitance corresponds to the following expression (see Equation (5)):

$$\frac{1}{C_M(q)} = \frac{1}{C_1} + \frac{1}{R_1C_2^2C_3}\int_{t_0}^{t} q(t)dt \tag{18}$$

Moreover, this emulator could also be implemented by replacing the second CCII with an operational transconductance amplifier (OTA), as shown in Figure 7b. In that case, the resulting memcapacitance would be given by:

$$\frac{1}{C_M(q)} = \frac{1}{C_1} + \frac{g_m}{C_2^2C_3}\int_{t_0}^{t} q(t)dt \tag{19}$$

where g_m is the OTA's transconductance gain.

The experimental results obtained using off-the-shelf components demonstrated that the circuits of Figure 7 was able to emulate a grounded charge-controlled memcapacitor at frequencies up to 48 Hz.

The emulation of mem-elements using OTAs-based circuits is also common in the literature. For instance, in Ref. [48] Vista and Ranjan presented a memcapacitor emulator using a dual X current conveyor differential input transconductance amplifier (DXCCDITA).

Their emulator is based on a DXCCDITA modeled as indicated in Figure 8.

On this basis, the memcapacitance can be derived from the voltage at the three different passive elements, R_1, C_1 and C_2 as:

$$\begin{cases} v_{C_1} = v_{Z_-} = \frac{1}{C_1}\int_{t_0}^{t} i_{C_1}(t)dt = \frac{1}{C_1}\int_{t_0}^{t} i_{Z_-}(t)dt = \frac{\alpha}{C_1}\int_{t_0}^{t} i_{X_-}(t)dt = \frac{\alpha q_{IN}(t)}{C_1} \\ v_{C_2}(t) = V_{O_+}(t) = V_{B_{O_-}}(t) = \frac{1}{C_2}\int_{t_0}^{t} i_{O_+}(t)dt = \frac{g_m}{C_1}\int_{t_0}^{t} V_{Z_-}(t)dt = \frac{\alpha g_m}{C_2C_1}\int_{t_0}^{t} q_{IN}(t)dt \\ V_Y(t) = \frac{V_{X_+}(t)}{\beta} = \frac{-V_{X_-}(t)}{\beta} = V_{O_-}(t) = I_{O_-}(t)R_1 = -g_mV_{Z_-}(t)R_1 = \frac{-g_m\alpha q_{IN}(t)R_1}{C_1} \end{cases} \tag{20}$$

being α and β the current transfer gain and voltage transfer gain, respectively. On the other hand, the transconductance (g_m) can be expressed as $g_m = K\left(V_{B_{O_-}} + V_{DD} - V_t\right)$, where

V_{DD} is the positive supply voltage and both V_t and K are parameters that depend on the CMOS technology used.

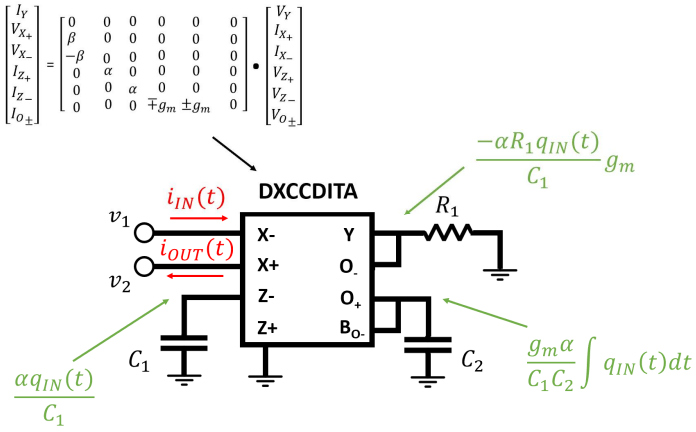

Figure 8. Memcapacitor emulator circuit proposed by Vista and Ranjan [48] based on a DXCCDITA.

Therefore, the constitutive equation of this charge-controlled memcapacitor can be obtained as:

$$v_{in}(t) = V_{X_-}(t) - V_{X_+}(t) = -2\beta V_Y = \frac{2\alpha\beta K R_1}{C_1} \cdot q(t) \cdot \left(V_{DD} - V_T + \frac{\alpha g_m}{C_1 C_2} \int_{t_0}^{t} q_{IN}(t) dt \right) \quad (21)$$

Hence, the charge-controlled memcapacitance is given by:

$$\frac{1}{C_M(q)} = \frac{2\alpha\beta K R_1}{C_1} \cdot \left(V_{DD} - V_T + \frac{\alpha g_m}{C_1 C_2} \int_{t_0}^{t} q_{IN}(t) dt \right) \quad (22)$$

The feasibility of this floating charge-controlled memcapacitor model has been verified by means of SPICE simulation, and additionally, the practicability of this model is examined in an adaptative neuromorphic structure [48].

Finally, a brief comparison of the different memcapacitor emulators presented in this section is summarized in Table 1. The comparison has been carried out in terms of their key components and mode of operation (grounded or floating), among other parameters.

Table 1. Comparison of the different memcapacitor emulators presented in this review.

Reference	Mutator	Configuration	Control Variable	Key Components	Experimental
Fouda and Radwan [40]	No	Grounded	Charge	Op amps Analog multiplier Copy of the input current	No
Sah et al. [42]	No	Grounded	Charge	Op amps Analog multiplier	Yes
Romero et al. [43]	Yes	Grounded	Voltage	Op amps Memristor [1]	Yes
Wang et al. [44]	Yes	Grounded	Voltage	Current conveyors Memristor [1]	Yes
Pershin and Di Ventra [45]	Yes	Floating	Voltage	Current conveyors Inductor Memristor	No
Yesil and Babacan [47]	No	Grounded	Charge	Current conveyor OTA Analog multiplier	Yes
Vista and Ranjan [48]	No	Floating	Charge	Custom DXCCDITA	No

[1] Or memristor emulator (applicable in all cases).

3. Meminductor Emulators

The meminductance (L_M) is defined as the nth-order system that establishes a non-linear relation between the current across the terminal of the device (I) and its input flux (ϕ) [34]. It can be either current-controlled or flux-controlled depending on its constitutive input variable. Therefore, the nth-order current-controlled meminductive systems are defined by Equation (23), whereas the flux-controlled ones are defined by Equation (24).

$$\phi(t) = L_M\left(\vec{x_N},\ I, t\right)\cdot I(t) \tag{23}$$

$$I(t) = L_M^{-1}\left(\vec{x_N},\ \phi, t\right)\cdot \phi(t) \tag{24}$$

being $\vec{x_N}$ a vector which represents the n internal state variables of the system.

The meminductor is a particular case of meminductive system with one single state variable; the current in the case of current-controlled meminductors (Equation (25)) or the flux in the case of flux-controlled meminductors (Equation (26)):

$$\phi(t) = L_M\left[\int_{t_0}^{t} I(\tau)d\tau\right]\cdot I(t) \tag{25}$$

$$I(t) = L_M^{-1}\left[\int_{t_0}^{t} \phi(\tau)d\tau\right]\cdot \phi(t) \tag{26}$$

where the initial instant of time, t_0, may be selected to ensure that $\int_{-\infty}^{t_0} I(\tau)d\tau = 0$ and $\int_{-\infty}^{t_0} \phi(\tau)d\tau = 0$, respectively.

Therefore, the meminductance of meminductors depends on either the current or the flux depending on whether they are current-controlled or flux-controlled, respectively. In addition, their i-ϕ characteristic presents a closed-pinched hysteresis loop in which $i = 0$ whenever $\phi = 0$ (and vice versa) for bipolar sine wave-like excitations. The usual approaches followed to implement meminductors emulators are quite similar to those used to emulate memcapacitors. One of these common approaches employs mutators in order to transform memristors into meminductors in both grounded and floating configurations. This is the case of the grounded meminductor shown in Figure 9, which was proposed by Wang in Ref. [49].

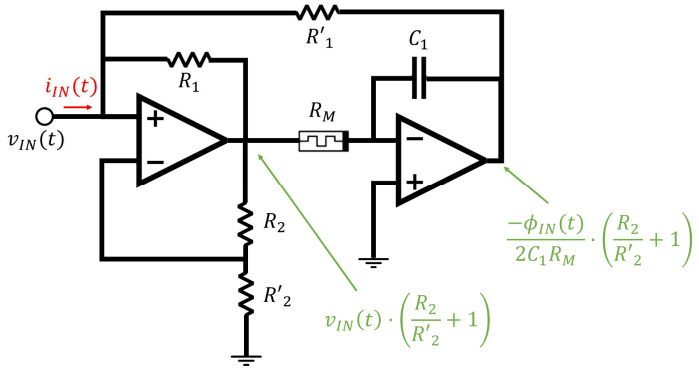

Figure 9. Meminductor emulator circuit proposed by Wang [49].

In this circuit, the input current can be expressed as follows:

$$i_{IN}(t) = i_{R_1} + i_{R'_1} = v_{IN}(t)\cdot\left(\frac{1}{R'_1} - \frac{R_2}{R_1 R'_2}\right) + \frac{\phi_{IN}(t)}{2R_2 R_M(\phi)C_1}\cdot\left(\frac{R_2}{R'_2} + 1\right) \tag{27}$$

As seen, Equation (27) can be directly related to the constitutive equation of a flux-controlled meminductor with the condition of cancelling the term associated with the input voltage, i.e., with $R'_1 = R_1$ and $R'_2 = R_2$. In that case, the resulting input current can

be expressed as indicated in Equation (28) and, therefore, the circuit would emulate the behavior of a flux-controlled meminductance modelled by Equation (29).

$$i_{IN}(t) = \frac{\phi_{IN}(t)}{R_2 R_M(\phi) C_1} \tag{28}$$

$$L_M(\phi) = R_2 R_M(\phi) C_1 \tag{29}$$

This simple model was verified by means of simulations; however, it was studied neither in the frequency-domain nor with an experimental implementation.

Another example of mutator, based on a gyrator, was presented by Romero et al. upon the design of the Antoniou's circuit, as depicted in Figure 10 [35].

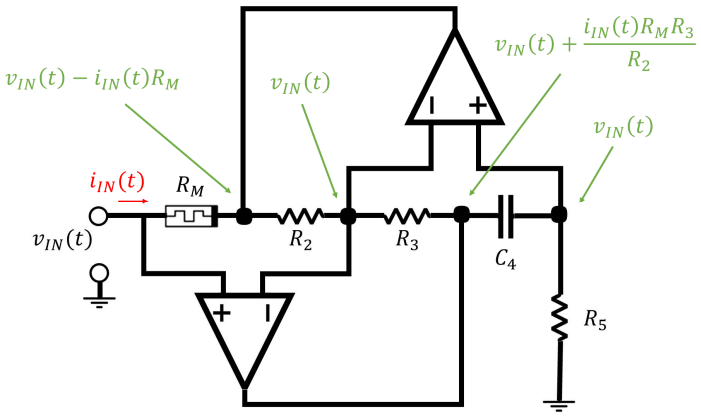

Figure 10. Grounded meminductor emulator circuit proposed by Romero et al. [35].

In this case, the meminductance can be derived from the current through R_5, given that $i_{R_5} = i_{C_4}$. Therefore:

$$\frac{v_{IN(t)}}{R_5} = \frac{C_4 R_M R_3}{R_2} \cdot \frac{d(i_t(t))}{dt} \rightarrow i_{IN}(t) = \phi_{IN}(t) \cdot \frac{R_2}{R_M(\phi) R_3 R_5 C_4} \tag{30}$$

which indicates that the circuit behaves as a flux-controlled meminductor whose value is given by Equation (31).

$$L_M(\phi) = \frac{R_M(\phi) R_3 R_5 C_4}{R_2} \tag{31}$$

This circuit was validated using SPICE simulations for various input signals and frequencies. For the simulations, the memristor was implemented by means of a LDR, as shown in previous implementations. In addition, the practicability of the meminductor model was also exhibited with a long-term potentiation (LTP) and long-term depression (LTD) example [35]. However, this circuit also presents the disadvantage of being restricted to grounded configurations.

Following the same approach, Romero et al. also presented a floating meminductor emulator based on the Riordan gyrator. In this case, the meminductor emulator is based on the schematic shown in Figure 11.

In order to emulate a floating meminductor, the input current at the first terminal must be equal to the output current of terminal two, therefore:

$$\boldsymbol{I}_{IN} = -\boldsymbol{I}_{OUT} = \boldsymbol{V}_{IN} \cdot \frac{Z_2 Z_4}{Z_5 Z_M Z_1} = -\boldsymbol{V}_{IN} \cdot \left(\frac{Z_7}{Z_8 Z_6} + \frac{Z_2 Z_4 Z_7}{Z_M Z_5 Z_6 Z_8} - \frac{1}{Z_5} \right) \tag{32}$$

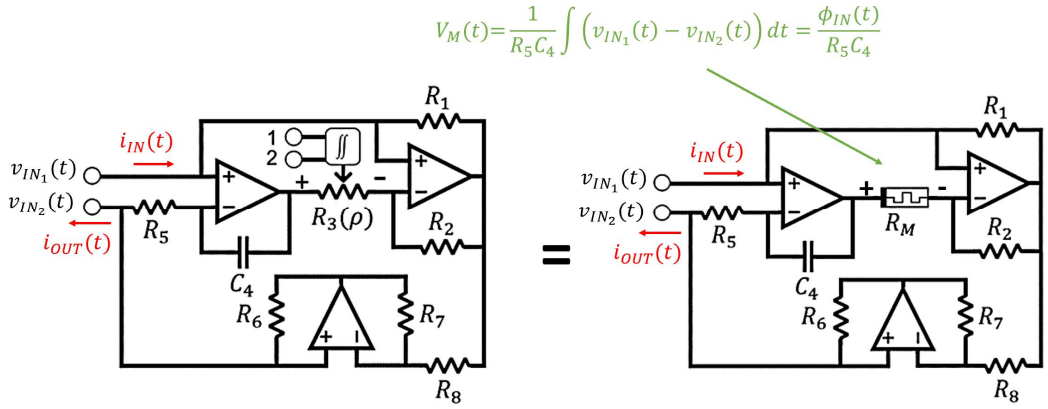

Figure 11. Floating meminductor emulator circuit proposed by Romero et al. [50].

Thus, the circuit of Figure 11 needs to fulfill the following condition:

$$\frac{1}{Z_5}=\frac{1}{Z_1}=\frac{Z_7}{Z_6Z_8} \tag{33}$$

where Z_i represents the impedance of the passive element i. On this basis, considering $R_1 = R_2 = R_5 = R_7 = R_6 = R_8 = R$, Equation (32) can be expressed as given in Equation (34).

$$\boldsymbol{I}_{IN}=\frac{\boldsymbol{V}_{IN}}{s}\cdot\frac{1}{RC_4R_M(\phi(s))} \tag{34}$$

Finally, the constitutive equation of this floating meminductor emulator can be obtained by transforming Equation (34) to the time domain:

$$i_{IN}(t)=\phi_{IN}(t)\cdot\frac{1}{RC_4R_M(\phi)}=\phi_{IN}(t)\cdot\frac{1}{L_M(\phi)} \tag{35}$$

Therefore, with this implementation we can avoid the drawback of being subject to grounded configurations when implementing a meminductor emulator. The feasibility of this circuit was proved by a practical implementation, besides, an example of application in which the emulator is used in an adaptative low-pass filter was also shown.

As in the case of memcapacitor emulators, some authors also rely on the use of current conveyors for the implementation of their emulators. An example of this practice is the model proposed by Sah et al. in Ref. [51], whose schematic is shown in Figure 12.

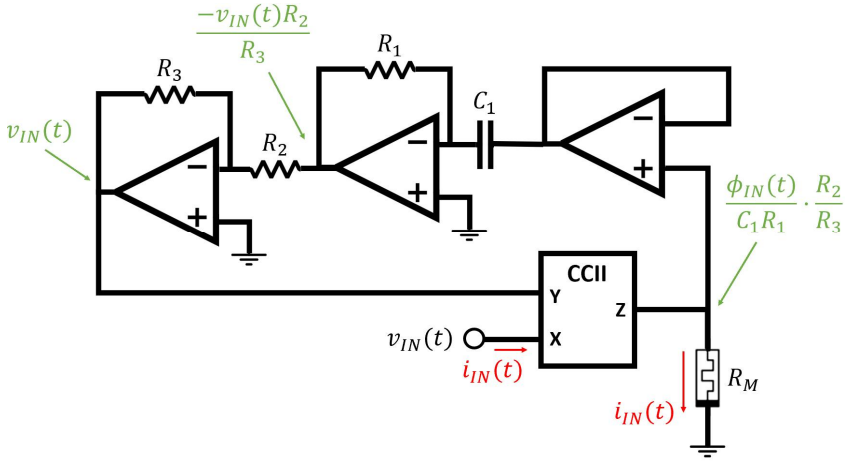

Figure 12. Meminductor emulator circuit proposed by Sah et al. [51].

In this circuit, the current relations $i_{C_1} = i_{R_1}$ and $i_{R_2} = i_{R3}$ allow extracting the constitutive equation of the equivalent flux-controlled meminductor:

$$i_{IN}(t) = \phi_{IN}(t) \cdot \frac{R_2}{C_1 R_1 R_3 R_M(\phi)} \tag{36}$$

which results in the following meminductance:

$$L_M(\phi) = \frac{C_1 R_1 R_3 R_M(\phi)}{R_2} \tag{37}$$

as it was demonstrated by means of both SPICE and experimental results for different input frequencies. Alternatively, in Ref [52] the same authors presented an equivalent circuit based on two current conveyors (see Figure 13).

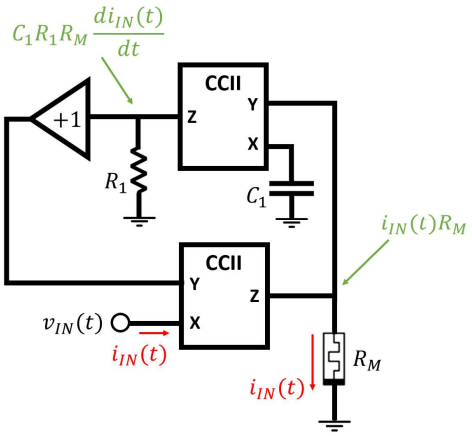

Figure 13. Meminductor emulator circuit based on current conveyors proposed by Sah et al. [52].

In this emulator, the meminductance can be derived from the relation between the current passing through the different passive elements, resistor, capacitor and memristor:

$$i_{C_1} = i_{R_1} = C_1 R_M \frac{di_{IN}(t)}{dt} = \frac{v_{IN}(t)}{R_1} \tag{38}$$

Therefore, the flux-controlled meminductance is given by Equation (39), as demonstrated experimentally by the authors.

$$i_{IN}(t) = \frac{\phi_{IN}(t)}{R_1 R_M(\phi) C_1} = \frac{\phi_{IN}(t)}{L_M(\phi)} \tag{39}$$

Another example of mutator based on current conveyors was the circuit proposed by Liang et al. [36] to emulate floating flux-controlled meminductors (Figure 14).

As it is shown, the equivalent input meminductance of this mutator can be extracted from the current through the memristor:

$$i_{R_M}(t) = i_{R_2}(t) = \frac{\phi_{IN}(t)}{R_1 C_1 R_M} = \frac{i_{IN}(t) R_3}{R_2} \tag{40}$$

Thus, the flux-controlled meminductance can be calculated as:

$$L_M(\phi) = \frac{R_2}{R_1 C_1 R_3 R_M(\phi)} \tag{41}$$

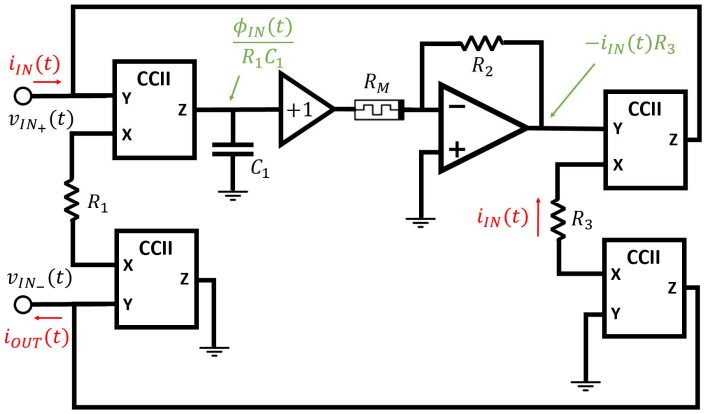

Figure 14. Floating meminductor emulator circuit based on current conveyors proposed by Liang et al. [36].

Contrary to others practical mutators, in this work, the authors opted for the use of an analog multiplier rather than a LDR for the implementation of the memristor with the goal of achieving a better control over its memristance. Their proposed circuit was validated experimentally using a sinusoidal input voltage for two different frequencies, 28.3 Hz and 36.9 Hz. A similar approach to the followed in this latter work was presented in Ref. [53] by the same authors, and by Sozen and Cam in Ref. [54], although in this latter case the authors made use of an OTA instead of a current conveyor to obtain the input flux.

All the meminductor emulators presented so far require the use of either a memristor or a memristor emulator for their practical implementations. An alternative also based on current conveyors, but without the need of implementing a memristor, can be found in Ref. [55], in which Fouda and Radwan proposed the circuit depicted in Figure 15 to emulate grounded current-controlled meminductors.

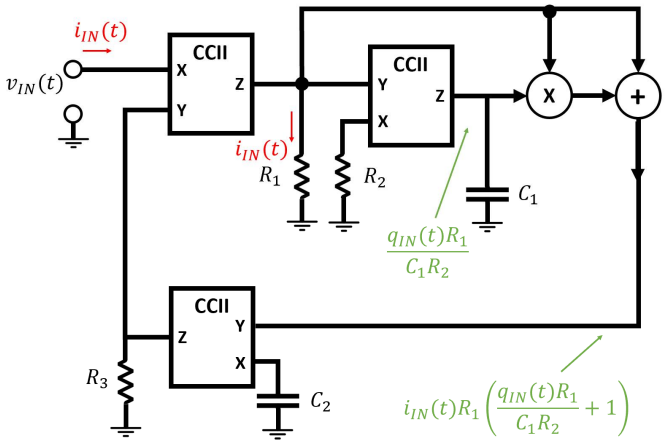

Figure 15. Meminductor emulator circuit based on current conveyors proposed by Fouda and Radwan [55].

This circuit is designed to fulfill the constitutive equation of the current-controlled meminductors as defined in Equation (25) [56]:

$$\phi(t) = (L_0 + kq(t)) \cdot i(t) \tag{42}$$

being L_0 the initial inductance and k the mobility factor.

Therefore, considering that $i_{R_3} = i_{C_2}$, we can obtain:

$$\phi_{IN}(t) = \left(R_1R_3C_2 + \frac{R_1^2R_3C_2}{C_1R_2} q_{IN}(t) \right) \cdot i_{IN}(t) \tag{43}$$

By comparing the two previous equations, the current-controlled meminductance can be expressed as indicated in Equation (44), which was demonstrated by SPICE simulations and a circuit implementation at a frequency of 10 Hz.

$$L_M(q) = L_0 + kq_{IN}(t) = R_1R_3C_2 + \frac{R_1^2R_3C_2}{C_1R_2}q_{IN}(t) \tag{44}$$

Moreover, as in the case of the memcapacitors emulators, some authors resorted to the use of custom CMOS-based circuits to implement memristor-less meminductor emulators. Some examples of these circuits are the works presented by Konal and Kacar in Ref. [57], where the authors proposed a CMOS realization of multi-output OTAs for the emulation of grounded meminductors; or the work presented by Vistan and Ranjan in Ref. [58], where a voltage difference transconductance amplifier (VDTA) implemented with CMOS technology is revealed to be also used for the emulation of grounded meminductors.

Finally, a brief comparison of the different meminductor emulators presented in this section is given in Table 2. The comparison has been carried out in terms of their key components and mode of operation (grounded or floating), among other parameters.

Table 2. Comparison of the different meminductor emulators presented in this work.

Reference	Mutator	Configuration	Control Variable	Key Components	Experimental
Wang [49]	Yes	Grounded	Flux	Op amps, Memristor [1]	No
Romero et al. [35]	Yes	Grounded	Flux	Op amps, Memristor	No
Romero et al. [50]	Yes	Floating	Flux	Op amps, Memristor	Yes
Sah et al. [51]	Yes	Grounded	Flux	Current conveyor, Op amps, Memristor [1]	Yes
Sha et al. [52]	Yes	Grounded	Flux	Current conveyors, Memristor	No
Liang et al. [36]	Yes	Floating	Flux	Current conveyor, Op amps, Memristor	Yes
Fouda and Radwan [55]	No	Grounded	Current	Current conveyor, Analog multiplier, Adder	No

[1] Or memristor emulator (applicable in all cases).

4. Universal Emulators: Memcapacitors and Meminductor

In this section, we select some of the remarkable circuits available in the literature that are able to emulate either a memcapacitor or a meminductor by minor changes in their structure or by a proper configuration of their passive elements. For instance, the circuits shown in Figure 16a,b were proposed by Babacan for the emulation of memcapacitors and meminductors, respectively [59]. In the first case, the memcapacitance behavior is achieved by the feedback provided by the capacitors connected to the outputs of the OTA:

$$i_{IN}(t) = C_1\frac{d\left(v_{IN}(t) - \frac{q_{IN}(t)\int q_{IN}(t)dt}{C_2^2}\right)}{dt} \tag{45}$$

and therefore, the equivalent input charge-controlled memcapacitance can be derived as:

$$C_M(q) = \frac{1}{C_1} + \frac{\int_{t_0}^{t} q_{IN}(\tau)d\tau}{C_2^2} \tag{46}$$

Similarly, in the circuit depicted in Figure 16b, the feedback provided in the negative input of the OTA and the combination of the voltage in both R_1 and C_1 allows to express the input voltage as follows:

$$v_{IN}(t) = L_1 \frac{di_{IN}(t)}{dt} + \frac{R_1}{C_1} \cdot \frac{d(i_{IN}(t) \cdot q_{IN}(t))}{dt} \tag{47}$$

and therefore, according to Equation (25), the current-controlled equivalent input meminductance of this circuit corresponds to Equation (48).

$$\phi_{IN}(t) = \left(L_1 + \frac{R_1}{C_1} q_{IN}(t) \right) i_{IN}(t) = L_M(q) i_{IN}(t) \tag{48}$$

The mutation of memristive systems into universal memcapacitive and meminductive emulators have also been considered by some authors, as the case of Taşkiran et al. [60]. In this work, the authors proposed a simple current backward transconductance amplifier (CBTA) to implement a universal mutator based on the scheme exhibited in Figure 17a, whose equivalent input impedance in the Laplace domain can be expressed as:

$$Z_{IN}(s) = \frac{\boldsymbol{V}_{IN}}{\boldsymbol{I}_{IN}} = \frac{Z_W}{Z_Z} \cdot \frac{1}{\mu_W g_m \alpha} \tag{49}$$

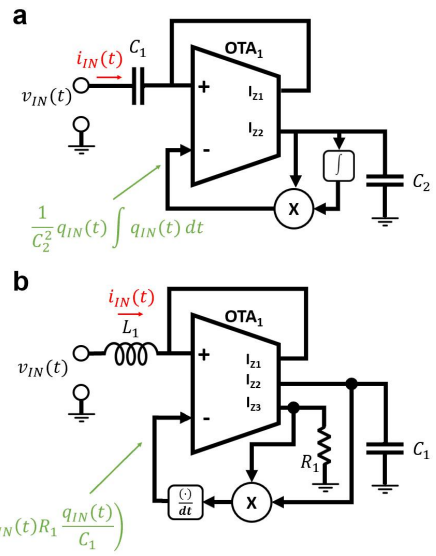

Figure 16. Memcapacitor (**a**) and meminductor emulator (**b**) circuits proposed by Babacan [59].

Thus, by means of the substitutions shown in Figure 17b,c, the circuit of Figure 17a can be used to emulate either a memcapacitor or a meminductor, respectively. In that case, the equivalent input memcapacitance and meminductance can be derived as follows:

$$Z_{IN_{MC}}(s) = \frac{1}{R_M(\phi(s)) C_1 s} \cdot \frac{1}{\mu_W g_m \alpha} \rightarrow C_M(\phi) = R_M(\phi) C_1 \mu_W g_m \alpha \tag{50}$$

$$Z_{IN_{MI}}(s) = \frac{R_M(\phi(s)) C_1 s}{\mu_W g_m \alpha} \rightarrow L_M(\phi) = \frac{R_M(\phi) C_1}{\mu_W g_m \alpha} \tag{51}$$

where g_m, μ_W, and α are the transconductance gain and both voltage and current gains, respectively.

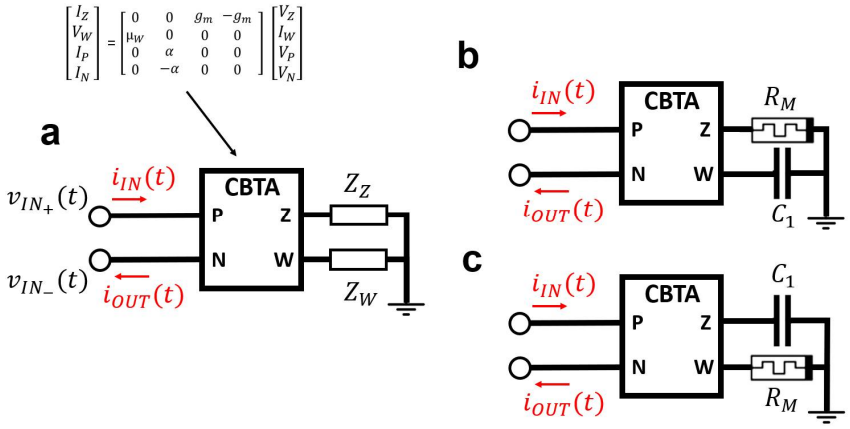

Figure 17. (**a**) CBTA-based circuit for the emulation of floating memcapacitors and meminductors devices proposed by Taşkiran et al. [60]. (**b**) Mutator for the emulation of memcapacitors, (**c**) mutator for the emulation of meminductors.

Similarly, Yu et al. [61] proposed an universal mutator based on commercial current conveyors for emulating grounded mem-elements (Figure 18a). As in the case of the circuit proposed by in Ref. [60], this mutator can be used to achieve a straightforward transformation between a memristor and either a memcapacitor or a meminductor by just modifying the combination of its different impedances. In both cases, either the memcapacitor (Figure 18b) or the meminductor (Figure 18c), the constitutive equation of the emulated device can be derived from the relation between the current and the voltage in Z_1. Thus, for the memcapacitive ciruit:

$$q_{IN}(t) = \frac{C_1}{R_2R_3R_4R_M(\phi)} v_{IN}(t) = C_M(\phi) \cdot v_{IN}(t) \tag{52}$$

whereas for the meminductive circuit:

$$i_{IN}(t) = \frac{R_4}{R_1R_2R_M(\phi)C_3} \phi_{IN}(t) = L_M^{-1}(\phi) \cdot \phi_{IN}(t) \tag{53}$$

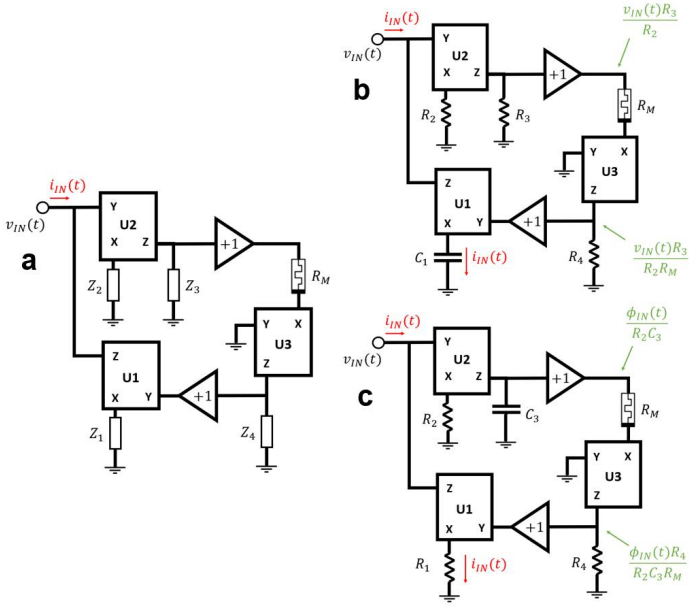

Figure 18. (**a**) Universal circuit for the emulation of grounded mem-elements proposed by Yu et al. [61]. (**b**) Mutator for the emulation of memcapacitors, (**c**) mutator for the emulation of meminductors.

Recently, Yu et al. [62] revisited this circuit aiming to emulate not only grounded mem-elements but also their floating configurations, with the additional advantage of avoiding the inclusion of a memristor (or its emulator) for its implementation. The behavior of these circuits is derived from the relation between the current through the resistor R_2 and the varactor diode C_{VD}, given that $i_{R_2} = i_{C_{VD}}$. On this basis, the memcapacitance of the circuit displayed in Figure 19a can be extracted as:

$$\begin{gathered} i_{R_2}(t) = \frac{q_{IN}(t)}{C_1 R_2} = C_{VD}(\phi)\frac{d\left(\frac{\phi_{IN}(t)}{R_1 C_2} - V_{OFFSET}\right)}{dt} = C_{VD}(\phi)\frac{v_{IN}(t)}{R_1 C_2} \\ \rightarrow \; C_M(\phi) = \frac{C_1 R_2 C_{VD}(\phi)}{R_1 C_2} \end{gathered} \tag{54}$$

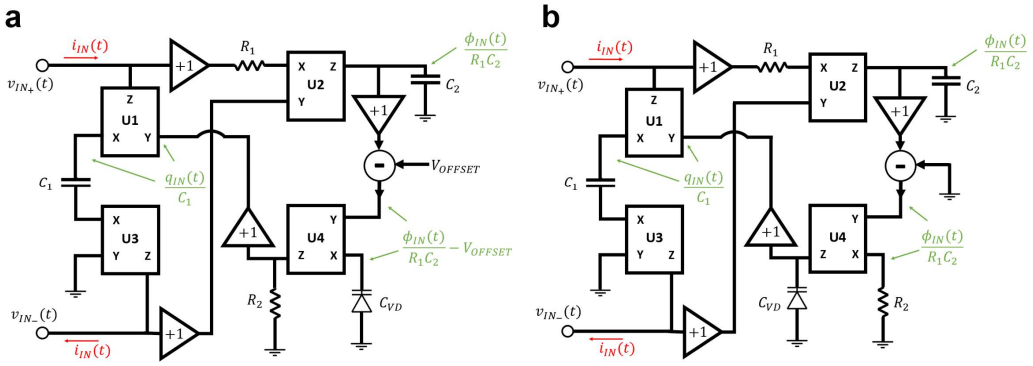

Figure 19. Universal circuit proposed by Yu et al. [62] for the emulation of floating memcapacitors (**a**), and floating meminductor (**b**).

In the same way, the equivalent meminductance of the circuit shown in Figure 19b can be expressed as:

$$\begin{gathered} i_{VD}(t) = \frac{C_{VD}(q)}{C_1}\cdot\frac{dq_{IN}(t)}{dt} = \frac{C_{VD}(q)}{C_1} i_{IN}(t) = \frac{\phi_{IN}(t)}{R_1 R_2 C_2} \\ \rightarrow \; L_M(q) = \frac{R_1 R_2 C_2 C_{VD}(q)}{C_1} \end{gathered} \tag{55}$$

The feasibility of these circuits has been proved by means of experimental results for sinusoidal input signals and in a wide range of frequencies (up to 22 kHz).

A similar circuit was proposed recently by Zhao et al. [63] as an alternative of this latter emulator. The circuit presented by Zhao et al., shown in Figure 20, makes use of an additional current conveyor and an analog multiplier in order to avoid the inclusion of a varactor diode, thus also escaping from the necessity of an external offset voltage. In both cases, memcapacitor emulator (Figure 20a) and meminductor emulator (Figure 20b), the constitutive equations can be extracted relating the voltage at the output terminal Z of both current conveyors, U3 and U4. Therefore, for the memcapacitor emulator we can write:

$$v_{IN}(t) = v_{IN+} - v_{IN-} = q_{IN}(t)\cdot\left(\frac{R_4}{C_0 R_5} - \frac{R_2}{C_0 R_3} + \frac{R_2}{C_0^2 C_1 R_1 R_3}\int_{t_0}^{t} q(\tau)d\tau\right) \tag{56}$$

while for the meminductor emulator:

$$\phi_{IN}(t) = \phi_{IN+} - \phi_{IN-} = i_{IN}(t)\cdot\left(R_0 R_4 C_2 - R_0 R_2 C_0 + \frac{R_0^2 R_2 C_0}{R_1 C_1} q_{IN}(t)\right) \tag{57}$$

Therefore, the equivalent charge-controlled memcapacitance and the current-controlled meminductance of these circuits can be expressed as indicated in Equation (58) and Equation (59), respectively.

$$C_M^{-1}(q) = \frac{R_4}{C_0 R_5} - \frac{R_2}{C_0 R_3} + \frac{R_2}{C_0^2 C_1 R_1 R_3} \int_{t_0}^{t} q(\tau) d\tau \tag{58}$$

$$L_M(q) = R_0 R_4 C_2 - R_0 R_2 C_0 + \frac{R_0^2 R_2 C_0}{R_1 C_1} q_{IN}(t) \tag{59}$$

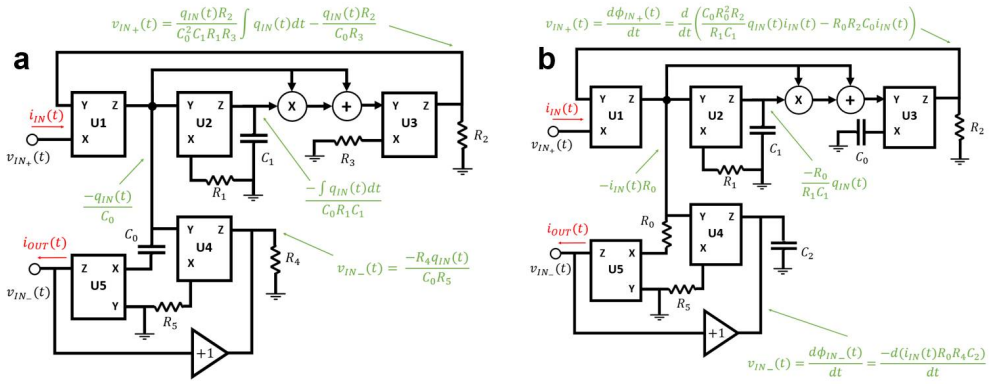

Figure 20. Universal circuit proposed by Zhao et al. [63] for the emulation of floating memcapacitors (**a**), and floating meminductors (**b**).

To sum up, Table 3 presents a brief comparison of the main features of the emulators presented in this section for both memcapacitor and meminductor configurations.

Table 3. Comparison among of the different universal emulators cited in this review.

Reference	Emulator	Mutator	Conf.	Control Variable	Key Components	Experimental
Babacan [59]	Memcap. / Memind.	No	Grounded	Charge / Current	OTA Integrator Differentiator Multiplier	No
Taşkiran et al. [60]	Memcap. / Memind.	Yes	Floating	Voltage / Flux	Custom CBTA Memristor [1]	No
Yu et al. [61]	Memcap. / Memind.	Yes	Grounded	Voltage / Flux	Current Conveyor Memristor	Yes
Yu et al. [62]	Memcap. / Memind.	No	Floating	Voltage / Flux	Current Conveyor Varactor diode Subtractor	Yes
Zhao et al. [63]	Memcap. / Memind.	No	Floating	Charge / Current	Current Conveyor Multiplier Adder	Yes

[1] Or memristor emulator (applicable in all cases).

5. Conclusions

In this work, different approaches proposed in the literature for the emulation of memcapacitors and meminductors are reviewed in detail. The selected emulator circuits have been theoretically analyzed to infer their constitutive equations and their equivalent memcapacitance or meminductance. It has been reported that most of the emulators presented in the literature are based on mutators, i.e., circuits that transform the constitutive equation of memristors into the corresponding constitutive equation of the emulated device.

Moreover, there are also a set of emulators that does not require the use of a memristor (or its emulator) for their implementation, providing a reliable and simpler alternative to emulate mem-elements. The main features of the analyzed mem-elements emulators have been gathered in three tables to offer a complete overview of the technological options. So that, we firmly consider that this study provides a useful guide for those researchers trying to choose the appropriate emulator restricted by the requirements and constraints of their practical implementations.

Author Contributions: Conceptualization, F.J.R., A.O., A.G., D.P.M. and N.R.; methodology, A.O., D.P.M. and N.R.; formal analysis, F.J.R. and A.O.; investigation, F.J.R. and A.T.-L.; writing—original draft preparation, F.J.R., A.O. and N.R.; writing—review and editing, A.T.-L., A.G. and D.P.M.; funding acquisition, A.O., D.P.M. and N.R. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the Japanese KAKENHI through Grant Number JP18k04275 and Spanish Ministry of Education, Culture, and Sport (MECD), through Project TEC2017-89955-P and Grant Numbers: FPU16/01451 and FPU16/04043.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Chua, L. Memristor-The Missing Circuit Element. *IEEE Trans. Circuit Theory* **1971**, *18*, 507–519. [CrossRef]
2. Chua, L.O.; Kang, S.M. Memristive Devices and Systems. *Proc. IEEE* **1976**, *64*, 209–223. [CrossRef]
3. Chua, L.O.; Kocarev, L.; Eckert, K.; Itoh, M. Experimental Chaos Synchronization in Chua's Circuit. *Int. J. Bifurc. Chaos* **1992**, *2*, 705–708. [CrossRef]
4. Chua, L.O. State Space Theory of Nonlinear Two- Terminal Higher-Order Elements. *J. Frankl. Inst.* **1983**, *316*, 1–50. [CrossRef]
5. Chua, L.O. Chua's Circuit: An Overview Ten Years Later. *J. Circuits Syst. Comput.* **1994**, *4*, 117–159. [CrossRef]
6. Süsse, R.; Domhardt, A.; Reinhard, M. Calculation of Electrical Circuits with Fractional Characteristics of Construction Elements. *Forsch. Ing.* **2005**, *69*, 230–235. [CrossRef]
7. Strukov, D.B.; Snider, G.S.; Stewart, D.R.; Williams, R.S. The Missing Memristor Found. *Nature* **2008**, *453*, 80–83. [CrossRef]
8. Jo, S.H.; Chang, T.; Ebong, I.; Bhadviya, B.B.; Mazumder, P.; Lu, W. Nanoscale Memristor Device as Synapse in Neuromorphic Systems. *Nano Lett.* **2010**, *10*, 1297–1301. [CrossRef] [PubMed]
9. Pershin, Y.V.; Di Ventra, M. Experimental Demonstration of Associative Memory with Memristive Neural Networks. *Neural Netw.* **2010**, *23*, 881–886. [CrossRef]
10. Azghadi, M.R.; Linares-Barranco, B.; Abbott, D.; Leong, P.H.W. A Hybrid CMOS-Memristor Neuromorphic Synapse. *IEEE Trans. Biomed. Circuits Syst.* **2017**, *11*, 434–445. [CrossRef]
11. Prezioso, M.; Merrikh-Bayat, F.; Hoskins, B.D.; Adam, G.C.; Likharev, K.K.; Strukov, D.B. Training and Operation of an Integrated Neuromorphic Network Based on Metal-Oxide Memristors. *Nature* **2015**, *521*, 61–64. [CrossRef] [PubMed]
12. Kozma, R.; Pino, R.E.; Pazienza, G.E. (Eds.) *Advances in Neuromorphic Memristor Science and Applications*; Springer: Dordrecht, The Netherlands, 2012; ISBN 978-94-007-4490-5.
13. Shin, S.; Kim, K.; Kang, S. Memristor Applications for Programmable Analog ICs. *IEEE Trans. Nanotechnol.* **2011**, *10*, 266–274. [CrossRef]
14. Merrikh-Bayat, F.; Shouraki, S.B. Memristor-Based Circuits for Performing Basic Arithmetic Operations. *Procedia Comput. Sci.* **2011**, *3*, 128–132. [CrossRef]
15. Pershin, Y.V.; Ventra, M.D. Practical Approach to Programmable Analog Circuits With Memristors. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2010**, *57*, 1857–1864. [CrossRef]
16. Pershin, Y.V.; Sazonov, E.; Di Ventra, M. Analogue-to-Digital and Digital-to-Analogue Conversion with Memristive Devices. *Electron. Lett.* **2012**, *48*, 73. [CrossRef]
17. Vourkas, I.; Sirakoulis, G.C. Emerging Memristor-Based Logic Circuit Design Approaches: A Review. *IEEE Circuits Syst. Mag.* **2016**, *16*, 15–30. [CrossRef]
18. Chen, S.; Mahmoodi, M.R.; Shi, Y.; Mahata, C.; Yuan, B.; Liang, X.; Wen, C.; Hui, F.; Akinwande, D.; Strukov, D.B.; et al. Wafer-Scale Integration of Two-Dimensional Materials in High-Density Memristive Crossbar Arrays for Artificial Neural Networks. *Nat. Electron.* **2020**, *3*, 638–645. [CrossRef]
19. Yuan, B.; Liang, X.; Zhong, L.; Shi, Y.; Palumbo, F.; Chen, S.; Hui, F.; Jing, X.; Villena, M.A.; Jiang, L.; et al. 150 Nm × 200 Nm Cross-Point Hexagonal Boron Nitride-Based Memristors. *Adv. Electron. Mater.* **2020**, *6*, 1900115. [CrossRef]
20. Zhu, K.; Liang, X.; Yuan, B.; Villena, M.A.; Wen, C.; Wang, T.; Chen, S.; Hui, F.; Shi, Y.; Lanza, M. Graphene–Boron Nitride–Graphene Cross-Point Memristors with Three Stable Resistive States. *ACS Appl. Mater. Interfaces* **2019**, *11*, 37999–38005. [CrossRef]
21. Driscoll, T.; Quinn, J.; Klein, S.; Kim, H.T.; Kim, B.J.; Pershin, Y.V.; Di Ventra, M.; Basov, D.N. Memristive Adaptive Filters. *Appl. Phys. Lett.* **2010**, *97*, 093502. [CrossRef]

22. Buscarino, A.; Fortuna, L.; Frasca, M.; Valentina Gambuzza, L. A Chaotic Circuit Based on Hewlett-Packard Memristor. *Chaos* **2012**, *22*, 023136. [CrossRef] [PubMed]
23. Muthuswamy, B.; Kokate, P.P. Memristor-Based Chaotic Circuits. *IETE Tech. Rev.* **2009**, *26*, 417–429. [CrossRef]
24. Xu, C.; Dong, X.; Jouppi, N.P.; Xie, Y. Design Implications of Memristor-Based RRAM Cross-Point Structures. In Proceedings of the 2011 Design, Automation Test in Europe, Grenoble, France, 14–18 March 2011; pp. 1–6.
25. Secco, J.; Corinto, F.; Sebastian, A. Flux–Charge Memristor Model for Phase Change Memory. *IEEE Trans. Circuits Syst. II Express Briefs* **2018**, *65*, 111–114. [CrossRef]
26. Almurib, H.A.F.; Kumar, T.N.; Lombardi, F. Design and Evaluation of a Memristor-Based Look-up Table for Non-Volatile Field Programmable Gate Arrays. *IET Circuits Devices Syst.* **2016**, *10*, 292–300. [CrossRef]
27. Ting, Y.-H.; Chen, J.-Y.; Huang, C.-W.; Huang, T.-K.; Hsieh, C.-Y.; Wu, W.-W. Observation of Resistive Switching Behavior in Crossbar Core–Shell Ni/NiO Nanowires Memristor. *Small* **2018**, *14*, 1703153. [CrossRef] [PubMed]
28. Miao, F.; Yi, W.; Goldfarb, I.; Yang, J.J.; Zhang, M.-X.; Pickett, M.D.; Strachan, J.P.; Medeiros-Ribeiro, G.; Williams, R.S. Continuous Electrical Tuning of the Chemical Composition of TaOx-Based Memristors. *ACS Nano* **2012**, *6*, 2312–2318. [CrossRef] [PubMed]
29. Chen, Y.; Liu, G.; Wang, C.; Zhang, W.; Li, R.-W.; Wang, L. Polymer Memristor for Information Storage and Neuromorphic Applications. *Mater. Horiz.* **2014**, *1*, 489–506. [CrossRef]
30. Zhang, L.; Gong, T.; Wang, H.; Guo, Z.; Zhang, H. Memristive Devices Based on Emerging Two-Dimensional Materials beyond Graphene. *Nanoscale* **2019**, *11*, 12413–12435. [CrossRef]
31. Romero, F.J.; Toral, A.; Medina-Rull, A.; Moraila-Martinez, C.L.; Morales, D.P.; Ohata, A.; Godoy, A.; Ruiz, F.G.; Rodriguez, N. Resistive Switching in Graphene Oxide. *Front. Mater.* **2020**, *7*. [CrossRef]
32. Romero, F.J.; Toral-Lopez, A.; Ohata, A.; Morales, D.P.; Ruiz, F.G.; Godoy, A.; Rodriguez, N. Laser-Fabricated Reduced Graphene Oxide Memristors. *Nanomaterials* **2019**, *9*, 897. [CrossRef]
33. Sahu, D.P.; Jetty, P.; Jammalamadaka, S.N. Graphene Oxide Based Synaptic Memristor Device for Neuromorphic Computing. *Nanotechnology* **2021**, *32*, 155701. [CrossRef] [PubMed]
34. Ventra, M.D.; Pershin, Y.V.; Chua, L.O. Circuit Elements With Memory: Memristors, Memcapacitors, and Meminductors. *Proc. IEEE* **2009**, *97*, 1717–1724. [CrossRef]
35. Romero, F.J.; Escudero, M.; Medina-Garcia, A.; Morales, D.P.; Rodriguez, N. Meminductor Emulator Based on a Modified Antoniou's Gyrator Circuit. *Electronics* **2020**, *9*, 1407. [CrossRef]
36. Liang, Y.; Chen, H.; Yu, D.S. A Practical Implementation of a Floating Memristor-Less Meminductor Emulator. *IEEE Trans. Circuits Syst. II Express Briefs* **2014**, *61*, 299–303. [CrossRef]
37. The Computer That Stores and Processes Information at the Same Time. Available online: https://www.technologyreview.com/2012/11/21/181520/the-computer-that-stores-and-processes-information-at-the-same-time/ (accessed on 15 May 2021).
38. Pershin, Y.V.; Di Ventra, M. Memcomputing: A Computing Paradigm to Store and Process Information on the Same Physical Platform. In Proceedings of the 2014 International Workshop on Computational Electronics (IWCE), Paris, France, 3–6 June 2014; pp. 1–2.
39. Di Ventra, M.; Pershin, Y.V. The Parallel Approach. *Nat. Phys.* **2013**, *9*, 200–202. [CrossRef]
40. Fouda, M.E.; Radwan, A.G. Charge Controlled Memristor-Less Memcapacitor Emulator. *Electron. Lett.* **2012**, *48*, 1454–1455. [CrossRef]
41. Biolek, D.; Biolek, Z.; Biolkova, V. SPICE Modelling of Memcapacitor. *Electron. Lett.* **2010**, *46*, 520–522. [CrossRef]
42. Sah, M.P.; Yang, C.; Budhathoki, R.K.; Kim, H.; Yoo, H.J. Implementation of a Memcapacitor Emulator with Off-the-Shelf Devices. *Elektron. Elektrotechnika* **2013**, *19*, 54–58. [CrossRef]
43. Romero, F.J.; Morales, D.P.; Godoy, A.; Ruiz, F.G.; Tienda-Luna, I.M.; Ohata, A.; Rodriguez, N. Memcapacitor Emulator Based on the Miller Effect. *Int. J. Circuit Theory Appl.* **2019**, *47*, 572–579. [CrossRef]
44. Wang, X.Y.; Fitch, A.L.; Iu, H.H.C.; Qi, W.G. Design of a Memcapacitor Emulator Based on a Memristor. *Phys. Lett. A* **2012**, *376*, 394–399. [CrossRef]
45. Pershin, Y.V.; Ventra, M.D. Emulation of Floating Memcapacitors and Meminductors Using Current Conveyors. *Electron. Lett.* **2011**, *47*, 243–244. [CrossRef]
46. Yu, D.S.; Liang, Y.; Chen, H.; Iu, H.H.C. Design of a Practical Memcapacitor Emulator Without Grounded Restriction. *IEEE Trans. Circuits Syst. II Express Briefs* **2013**, *60*, 207–211. [CrossRef]
47. Yesil, A.; Babacan, Y. Electronically Controllable Memcapacitor Circuit with Experimental Results. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, *68*, 1443–1447. [CrossRef]
48. Vista, J.; Ranjan, A. Simple Charge Controlled Floating Memcapacitor Emulator Using DXCCDITA. *Analog. Integr. Circuits Signal Process.* **2020**, *104*, 37–46. [CrossRef]
49. Wang, S.-F. The Gyrator for Transforming Nano Memristor into Meminductor. *Circuit World* **2016**, *42*, 197–200. [CrossRef]
50. Romero, F.J.; Medina-Garcia, A.; Escudero, M.; Morales, D.P.; Rodriguez, N. Design and Implementation of a Floating Meminductor Emulator upon Riordan Gyrator. *AEU Int. J. Electron. Commun.* **2021**, *133*, 153671. [CrossRef]
51. Sah, M.P.; Budhathoki, R.K.; Yang, C.; Kim, H. Mutator-Based Meminductor Emulator for Circuit Applications. *Circuits Syst. Signal Process.* **2014**, *33*, 2363–2383. [CrossRef]
52. Sah, M.P.; Budhathoki, R.K.; Yang, C.; Kim, H. A Mutator-Based Meminductor Emulator Circuit. In Proceedings of the 2014 IEEE International Symposium on Circuits and Systems (ISCAS), Melbourne, VIC, Australia, 1–5 June 2014; pp. 2249–2252.

53. Liang, Y.; Ying, S.; Bingmeng, H.; Lu, C.; Jing, S. Design and Characteristic Analysis of Floating Flux-Controlled Meminductor Emulator. *J. Syst. Simul.* **2018**, *30*, 1337. [CrossRef]
54. Sozen, H.; Cam, U. A Novel Floating/Grounded Meminductor Emulator. *J. Circuits Syst. Comput.* **2020**, *29*, 2050247. [CrossRef]
55. Fouda, M.E.; Radwan, A.G. Memristor-Less Current- and Voltage-Controlled Meminductor Emulators. In Proceedings of the 2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS), Marseille, France, 7–10 December 2014; pp. 279–282.
56. Elwakil, A.S.; Fouda, M.E.; Radwan, A.G. A Simple Model of Double-Loop Hysteresis Behavior in Memristive Elements. *IEEE Trans. Circuits Syst. II Express Briefs* **2013**, *60*, 487–491. [CrossRef]
57. Konal, M.; Kacar, F. Electronically Tunable Meminductor Based on OTA. *AEU Int. J. Electron. Commun.* **2020**, *126*, 153391. [CrossRef]
58. Vista, J.; Ranjan, A. High Frequency Meminductor Emulator Employing VDTA and Its Application. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **2020**, *39*, 2020–2028. [CrossRef]
59. Babacan, Y. An Operational Transconductance Amplifier-Based Memcapacitor and Meminductor. *Istanb. Univ. J. Electr. Electron. Eng.* **2018**, *18*, 36–38. [CrossRef]
60. Çam Taşkıran, Z.G.; Sağbaş, M.; Ayten, U.E.; Sedef, H. A New Universal Mutator Circuit for Memcapacitor and Meminductor Elements. *AEU Int. J. Electron. Commun.* **2020**, *119*, 153180. [CrossRef]
61. Yu, D.; Liang, Y.; Iu, H.H.C.; Chua, L.O. A Universal Mutator for Transformations Among Memristor, Memcapacitor, and Meminductor. *IEEE Trans. Circuits Syst. II Express Briefs* **2014**, *61*, 758–762. [CrossRef]
62. Yu, D.; Zhao, X.; Sun, T.; Iu, H.H.C.; Fernando, T. A Simple Floating Mutator for Emulating Memristor, Memcapacitor, and Meminductor. *IEEE Trans. Circuits Syst. II Express Briefs* **2020**, *67*, 1334–1338. [CrossRef]
63. Zhao, Q.; Wang, C.; Zhang, X. A Universal Emulator for Memristor, Memcapacitor, and Meminductor and Its Chaotic Circuit. *Chaos* **2019**, *29*, 013141. [CrossRef]