Back-Gate Biasing Influence on the Electron Mobility and the Threshold Voltage of Ultra Thin Box Multigate MOSFETs

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Abstract

This work studies the influence of the back-gate bias on the threshold voltage (V_T) and the electron mobility of silicon trigate devices over ultra-thin-box. The analysis allows us to confirm the possibility of achieving body factors higher than γ=0.1 as long as the width is increased and the height is reduced as much as possible. Also, we have demonstrated the impact of the back-gate biasing on the electron mobility using state-of-the-art scattering models for 2D confined devices.

Introduction

Control of the V_T seems mandatory to reduce stand-by power while keeping high I_{on}. One potential solution is the back-gate biasing that modifies V_T due to the body effect. Few works deal with this effect on multi-gate MOSFETs [1-4]. Moreover, most of them are focused on the body factor (γ) but they do not include the implications on the transport properties, which may be non-negligible [5]. In this paper, we analyze the behavior of Ultra-Thin Box trigate devices including back-biasing as a function of the device dimensions.

Results

For this work we consider silicon trigate structures (see Fig. 1) with the following characteristics: SiO_2 as insulator and a thickness of 1.2nm for the gate insulator (T_{ox}) and 10nm for the buried oxide (T_{box}). A midgap metal with Φ_m=4.61eV as gate contact. The channel is oriented along the [011] crystallographic direction, being the top and bottom Si-insulator interfaces (100)-oriented, and the lateral ones (011)-oriented. Back-gate bias (V_{bg}) is applied beneath the buried oxide, as shown in the figure. The simulation results are achieved by self-consistently solving the 2D Schrödinger and Poisson equations in a cross-section of the structure, under the effective mass approach, including appropriate modifications on the effective mass tensor to account for the channel orientation and non-parabolicity corrections [6,7].

A. Electrostatic behavior

We first present the resulting inversion charge (N_i) *vs.* front gate voltage (V_{fg}) curves as a function of the device geometry and back-gate bias. Figure 3 depicts the linear charge curve for a device with W_{Si}=H_{Si}=5nm at different back-gate biases: as expected, the threshold voltage is reduced (increased) for positive (negative) back-gate bias, and as a consequence the curves are horizontally shifted in the figure. In the ideal conditions of these simulations, there are no significant variations on the gate capacitance ($C_G=dN_i/dV_{fg}$) achieved with different V_{bg}. However, the electron density is altered due to the variation in the potential distribution inside the semiconductor, as depicted in Fig. 4. This fact can influence the mobility behavior of the device, as will be shown later. When different device widths are considered for a fixed H_{Si}=5nm (see Fig. 5), the behavior gets more complicated. At negative V_{bg} values, V_T slightly increases with the device width, while for positive values of V_{bg}, the reduction of V_T as a function of W_{Si} is remarkable. The complete picture is shown in Fig. 6, where V_T is depicted for the whole range of applied V_{bg}. The role of the device height has been studied in Fig. 7 that presents V_T as a function of H_{Si} and the applied back bias. As already reported in [1], both the increase of W_{Si} and the decrease of H_{Si} are useful to increase the body factor $\gamma=|V_T/V_{bg}|$, which has been depicted in Fig. 8. As can be seen, for the values of T_{ox} and T_{box} considered in this work, γ higher than 0.1 can be achieved.

B. Electron mobility

The electron mobility has been estimated by means of the Kubo-Greenwood formula [8]. The total momentum relaxation time is calculated using the Mathiessen's rule at each energy value. Optical (OP) and acoustic (AP) phonons, surface-roughness (SR) and Coulomb (CO) scattering mechanisms have been included in the simulations. Both SR and CO scattering mechanisms have been implemented taking into account the tensorial dielectric screening [7]. The equations regarding the mobility calculation and the necessary parameters are listed in Fig. 2. The surface charge (N_{it}) is similar to that used in [9], where such a high value is needed to fit experimental results. The total mobility versus V_{bg} is depicted in Fig. 9 for a W_{Si} x H_{Si} =10nm x 5nm trigate: the electron mobility decreases for negative values of the back-gate bias since V_{bg} provokes a displacement of the charge towards the top region of the device even at sub-threshold voltages. On the other hand, positive values of V_{bg} shifts the charge towards the bottom interface, also separating it from the lateral sides and therefore reducing the SR influence due to those interfaces. In Fig. 10, both the phonon (μ_{PH}) and SR (μ_{SR}) components of the mobility are calculated for V_{bg}=±2V. As can be seen, the mobility values are higher for V_{bg}=2V, and in particular a very large increase of μ_{SR} is found. The decrease of μ_{PH} with V_{bg}= −2V can be explained by the increase of the overlap integral, originated from the confinement of the carriers in the top interface of the device. Finally, the influence of the CO mechanism has been studied comparing the total mobility achieved in the absence of interfacial charges (only SR, AP and OP) and that achieved when the interface charge is placed only in the Si/BOX interface or in the Si/OX interfaces (Fig. 11). The Si/BOX charge has a very little influence when V_{bg}=−2V, as the inversion charge is close to the top interface. For V_{bg}=2V, the charge is close to the bottom interface in the sub-threshold regime and thus, the mobility is degraded.

Conclusion

We have shown that large body factor values (γ>0.1) are possible for trigate SOI MOSFETs, and therefore dynamic power control is possible. The γ value strongly depends on the device's geometry. Moreover, back-gate bias is also a powerful tool to increase the electron mobility when positive values of V_{bg} are applied, due to the reduction of both SR and phonon scattering mechanisms.

Acknowledgment

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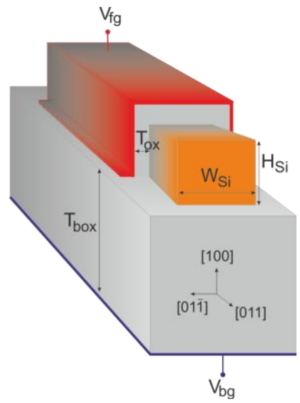

Fig. 1. Geometry of the trigate device: W_{Si} and H_{Si} are the silicon width and height, T_{ox} and T_{box} the oxide and buried oxide thickness.

$$\mu_i = \frac{g_i e}{n_i 2\pi k_B T}\int_{-\infty}^{\infty} dk\, v_i^2(k)\tau_i^m(k) f(E)\left(1-f(E)\right)$$

$$\frac{1}{\tau_i^m(k)} = \sum_{\text{mec}} \frac{1}{\tau_i^{m,\text{mec}}(k)} \qquad \mu = \frac{\sum_i n_i \mu_i}{\sum_i n_i}$$

SR: Δ_m = 0.5nm, L_{sr}=1.5nm
AP: Ξ_{ac} = 12eV, v_s=9 x 10^5 cm/s, ρ=2.329 x 10^{-3} kg/cm^3
OP: D_tK_j and ω_l parameters extracted from [11].
CO: N_{it} = 4 x 10^{12} cm^{-2} [9].

Fig. 2 Mobility calculation and scattering mechanisms modeling. $\tau_i^m(k)$, $v_i(k)$, g_i and n_i are the momentum relaxation time, velocity, valley degeneracy and electron density of subband *i*, respectively. *f* (E) is the Fermi distribution function. Scattering mechanisms are introduced as described in [7], but for the SR, which is calculated as in [10]: the corresponding parameters are listed above.

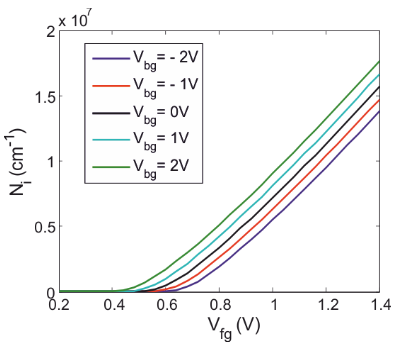

Fig. 3. N_i vs. V_{fg} in a device with W_{Si} = H_{Si} = 5nm, as a function of V_{bg} (ranging from –2V to 2V).

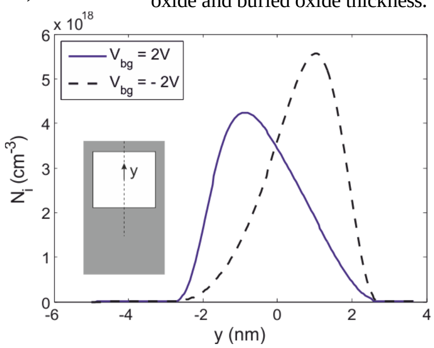

Fig. 4. Electron distribution at the threshold voltage of a 5nm x 5nm trigate with V_{bg} = 2V (solid line) and V_{bg} = –2V (dashed line).

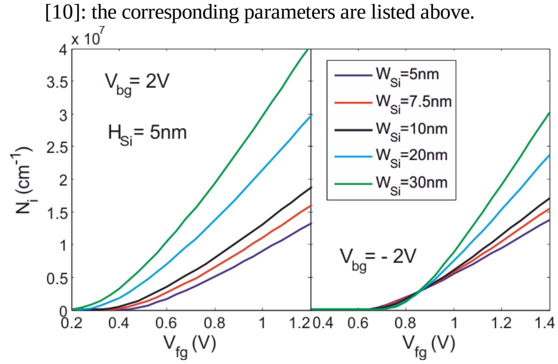

Fig. 5. N_i vs. V_{fg} in a device with H_{Si} = 5nm and variable silicon width: V_{bg}=2V (left), V_{bg} = –2V (right).

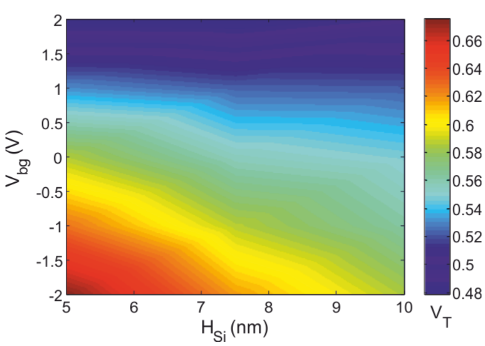

Fig. 6. V_T vs. the device height and the back-gate bias, for W_{Si} = 5nm devices.

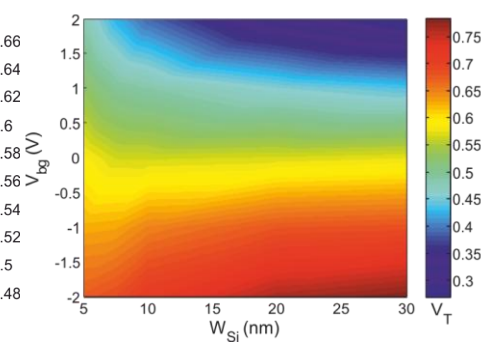

Fig. 7. V_T vs. the device width and the back-gate bias, for H_{Si} =5nm devices.

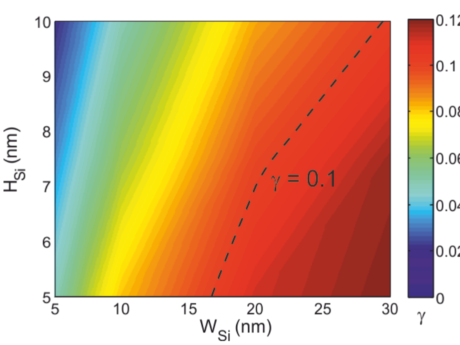

Fig. 8. Body factor (γ) as a function of W_{Si} and H_{Si}. The dashed line indicates the γ=0.1.

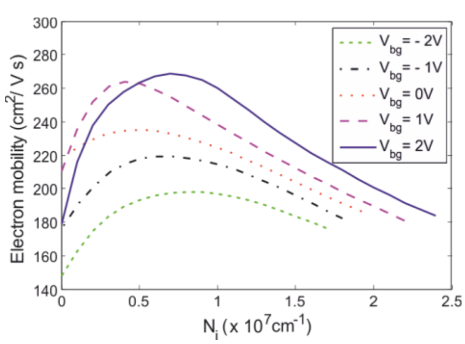

Fig. 9. Electron mobility vs. inversion charge as a function of the back-gate bias for a 10nm x 5nm trigate device.

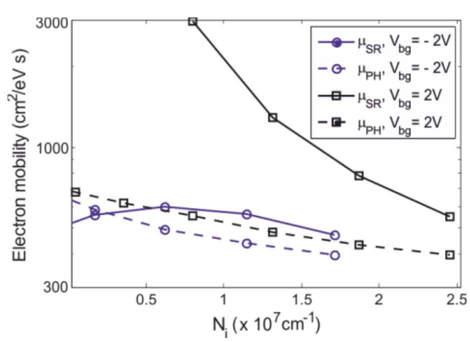

Fig. 10. SR-limited (solid lines) and phonon-limited (dashed-lines) mobility with V_{bg} = 2V (squares) and V_{bg} = - 2V (circles).

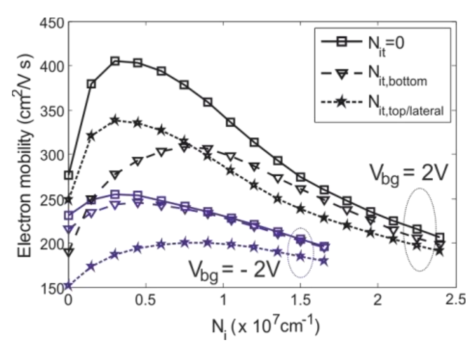

Fig. 11. Influence of the N_{it} on the total mobility (Vbg=±2V): No N_{it} (squares), N_{it} at the Si/BOX interface (triangles) and N_{it} only at the Si/OX regions (stars) are compared.