3D TCAD Study of the Implications of Channel Width and Interface States on FD-SOI Z^2-FETs

C. Navarro, S. Navarro, C. Marquez, J.L Padilla, P. Galy and F. Gamiz

***Abstract*—3D numerical TCAD simulations, based on experimental results, are performed to study the origin of the large Z^2-FET DRAM memory cell-to-cell variability on FD-SOI technology. The body width, cross-section shape and the passivation-induced lateral and top interface state density impacts on the device dynamic memory operation are investigated at room temperature. The width and body shape arise as marginal metrics not strongly inducing fluctuations in the device triggering conditions. However, the interface state (D_{it}) control, especially at the top of the ungated section, emerges as the main challenge since traps significantly increase the ON voltage variability threatening the capacitor-less DRAM operation.**

***Keywords*—3D, Capacitor-less, DRAM, Fully Depleted, Interface states, Memory, Silicon, SOI, Trap, variability, Z2-FET, 1T-DRAM.**

I. Z^2-FET INTRODUCTION AND BASICS

The Z^2-FET device [1], [2] is gaining momentum nowadays [3]. This double gated SOI (Silicon-on-Insulator) p-i-n diode is currently being extensively investigated via advanced TCAD simulations [4], [5] and through experiments [6], [7], as a possible DRAM replacement for embedded memory applications. As other single-transistor cells [8], [9], the Z^2-FET main advantage favoring its adoption is the possibility of getting rid of the external capacitor. This saving potentially reduces both the footprint and production complexity making them suitable for embedded applications.

The operation principles are based on a transient modulation of the stored charge underneath the gate thanks to the floating-body effect (FBE) [10]. Appropriate gates biasing is required: the front/back-gate terminals, $V_{FG/BG}$, are complementary biased (positive and negative, respectively) to induce additional energy barriers along the intrinsic body region. As a result, a new reverse virtual p-n junction arises (p-*i*-n→p-*n*-*p*-n) and two distinct logic levels can be obtained (Fig. 1): i) a high electron concentration below the top gate reduces the anode-gated region energy barrier (avoiding the deep depletion regime as in a MOS capacitor [11]), the inner section behaves again as intrinsic and the device presents the diode p-i-n current ($I_1 \equiv$ '1'-state); ii) a limited electron concentration in contrast reinforces the reverse mid n-p junction barrier blocking the current flow ($I_0 \equiv$ '0'-state). By adjusting the inner body carrier population, transitory shifts in the triggering anode voltage, V_{ON}, can be achieved enabling the memory operation [12].

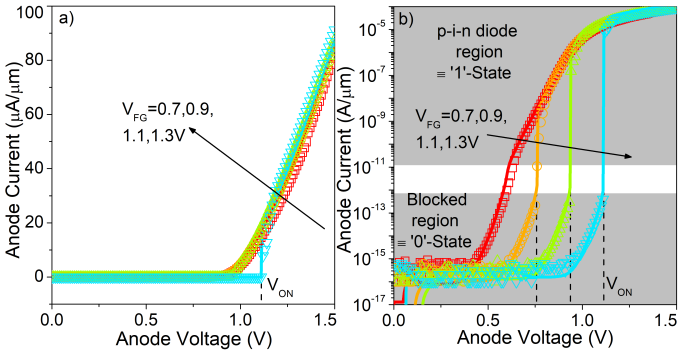

Fig. 1. DC $I_A(V_A)$ Z^2-FET switching characteristics comparison between 2D TCAD simulations (solid lines) and experimental results (symbols) in a) linear and b) logarithmic scales for distinct V_{FG}. $V_{BG} = -1$ V, $V_K = 0$ V. $t_{Si} \simeq 7$ nm, $t_{Epi} \simeq 15$ nm, $L_G = L_{In} = 200$ nm and $W = 100$ μm.

The Z^2-FET variability is reported to increase for narrow and short devices [13]. In this work we focus on the influence of the cell body geometry (width and cross-section) and silicon/passivation layer interface trap density on this variability. The origin might be the lateral shallow trench isolation (STI). As a result of etching and polishing fabrication steps, STI may be responsible of simultaneously inducing defects at the interfaces and non-completely vertical sidewalls. The traps presence is especially hard to mitigate since the crystal orientation is not perfectly controlled in volume production. Furthermore, the STI process induces mechanical stress at the edges due to trench fabrication or thermal processes increasing the number of traps through lattice distortion and/or dislocation formation [14], [15].

II. STRUCTURE DETAILS AND SIMULATION SETUP

The simulated Z^2-FET structure mimics a double-gate p-i-n diode manufactured on 28 nm FD (Fully Depleted) SOI technology [16] at STMicroelectronics. A sufficiently long diode, with $L \simeq 400$ nm (with gated region of $L_G = 200$ nm), is initially selected to limit short-channel effects (SCE) from affecting the electrostatics [17]. The body thickness is $t_{Si} \simeq 7$ nm under the gate stack while along the ungated region it increases up to $t_{Si} + t_{Epi} \simeq 22$ nm. The silicon active layer (p-type $N_{SOI} = 10^{16}$ cm^{-3}) lies above a buried SiO_2 sheet with $t_{BOX} \simeq 25$ nm and underneath, a p-type doped ($N_{Sub} \approx 10^{18}$ cm^{-3}) region as ground-plane (GP/BG) is present. The front-gate (FG) insulator comprises a high-k

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multi-layer stack with a final thickness of $t_{Ox} \approx 3$ nm. The top-gate features a close to mid-gap work-function of 4.7 eV. The back-gate terminal work-function is irrelevant and only the substrate doping impact on the electrostatic as shown later. The lateral terminals, anode (A) and cathode (K), are highly p/n-type doped, respectively ($N_K \approx N_A > 10^{21}$ cm^{-3}). The gate width, W, remains as a non-fixed parameter. The Z^2-FET default 3D structure is depicted in Fig. 2a.

Concerning the simulation, the Poisson's, charge continuity and density gradient (to implement the spatial quantization in the ultra-thin Si film) equations were considered for electrons and holes. Included models and parameters are room temperature (300 K), SRH (Shockley-Read-Hall) recombination/generation, surface recombination, band-to-band tunneling (BtBT) and several mobility models (doping dependence, high field velocity saturation, transverse electric field with remote-Coulomb scattering, and thin-layer) [18]. Additional details regarding the Z^2-FET architecture and simulation features can be found in [12].

Typical DC $I_A(V_A)$ switching characteristics were experimentally characterized from significantly wide devices. DC results were used to fit a 2D simulation deck [12], [17] from which the final 3D structure was built. Figure 1 illustrates, on the one hand, the characteristic Z^2-FET sharp current onset at $V_A = V_{ON}$ and, on the other hand, the curve fitting with the experimental results demonstrating an excellent agreement. The carrier lifetime ($\tau_n = 2.5 \cdot 10^{-8}$ s and $\tau_p = 10^{-8}$ s) and access resistance ($R_{SD} = 400\ \Omega/\mu m$) were fixed to fit the DC characteristics. Note that, fixing the carrier lifetime prevents its potential impact on the device variability.

Different cross-section body configurations were accounted in the 3D deck. They reflect the lateral Si_3N_4 isolation process impact on the architecture that induces non-perfectly vertical sidewalls. The top and bottom bases are always parallel while the two lateral sidewalls have the same length (isosceles trapezoids). Since the body thicknesses are fixed, each trapezoid is fully defined by α, a shape factor representing the angle between the top base and the sidewalls, Fig. 2c. Positive angles ($\alpha > 0°$) yield wider bodies at the bottom whereas negatives ($\alpha < 0°$) provide narrower bottom bases.

Similarly, the impact of the interface density of states (D_{it}), in-between the passivation Si_3N_4 layer and the silicon-body, is analyzed for different trap nature and distributions. Both acceptor (they have the charge of one electron when fully occupied) and donor (positively charged when occupied) traps are accounted. All trap distributions are randomly generated (the pseudo random number generator uses known seeds so that results can be reproduced if required) and correspond to Gaussian-like profiles with variable average concentration per unit area. Four locations are considered: exclusively at the gated (blue traps in Fig. 2b) or ungated (red traps in Fig. 2c) region sidewalls, at the ungated top interface (green traps in Fig. 2c,d) or in all three regions simultaneously.

III. Z^2-FET CROSS-SECTION GEOMETRY IMPACT

This section is devoted to analyze the effect when shrinking down the Z^2-FET width for several silicon-body geometries (no side or top Si_3N_4/Si interface D_{it} are included).

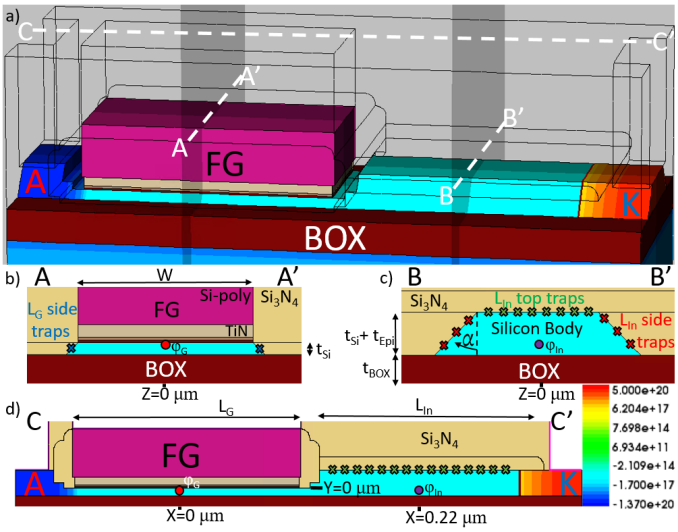

Fig. 2. a) Simulated 3D Z^2-FET structure with the net silicon-body doping concentration (cm^{-3}). Transverse cutting planes at the b) gated (A-A', showing the L_G sidewall traps) and c) ungated (B-B', depicting the L_{In} top and side traps) regions, respectively. d) Longitudinal plane (C-C', illustrating the L_{In} top traps) along the carriers propagation direction between anode (A) and cathode (K). Subfigures b,c and d indicate where the traps might be located at the Si_3N_4/Si interface: top of the ungated intrinsic region and the sidewalls (both along the gated and/or ungated regions). $W = 100$ nm, $\alpha = +45°$.

A. Current onset and electrostatic control

Figure 3a shows the $I_A(V_A)$ characteristics for several Z^2-FET widths where the currents have not been normalized to enhance data discrimination. The ON voltage arises later as the width is downscaled from 500 to 100 nm (minimum targeted width). This trend reflects the inner body potential decrease. Figure 3b depicts the electrostatic potential along the A/K direction at mid-channel. The previously mentioned virtual mid p-n junction is evidenced thanks to the gate biasing scheme. Two points can be highlighted: φ_G close to the front-gate dielectric at mid channel (Fig. 2b,d, $X = Z = 0$ and $Y \simeq 0$ μm) and φ_{In} equivalently in the ungated region (Fig. 2c,d, $X = 0.22$, $Y \simeq 0$ and $Z = 0$ μm). The potential is gradually reduced by these width-channel effects that enlarge the cathode-body barrier. In analogy with SCE, width-channel effects are those mechanisms degrading the top and bottom gates electrostatic control as the width is reduced. This degradation is more accentuated in the ungated region due to the worse electrostatic control induced by the thicker Si-film and insulator (BOX layer with respect to the front-gate stack). Indeed, if the width channel effects were visible in the gated region (φ_G reduction), the $V_{ON}(W)$ trend would have been the opposite since the anode-body barrier is the main responsible of driving the carrier injection and device triggering [12]. Width channel effects are much less evident and dramatic than SCE [17] but still measurable: the ON voltage variation from $W = 500$ nm to $W = 100$ nm, ΔV_{ON}, is only 20 mV (see inset in Fig. 3a) even when the corresponding shift in the electrostatic cathode-body barrier height is much larger. The

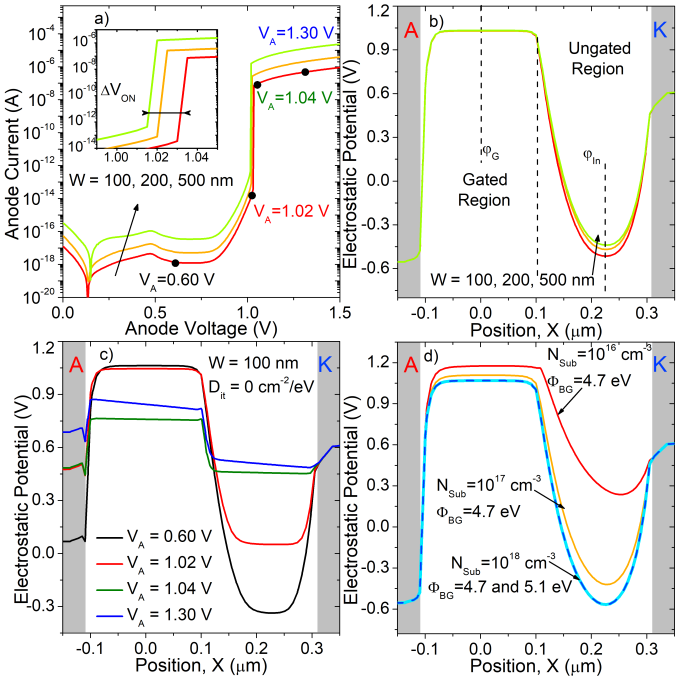

Fig. 3. a) 3D TCAD $I_A(V_A)$ DC curves for different widths. b) Electrostatic potential along the A/K X-axis at mid-channel ($Y \simeq 0$ and $Z = 0$ μm) comparison for several widths at $V_A = 0$ V. c) Electrostatic potential at distinct biasing conditions (from Fig. 3a $W = 100$ nm) to observe the Z^2-FET triggering via barrier collapse with the anode biasing, V_A, for $W = 100$ nm. d) Impact of back-gate work-function (Φ_{BG}) and ground-plane doping (N_{Sub}) on the electrostatic ($W = 100$ nm). $V_{FG} = 1.2$ V, $V_{BG} = -1$ V, $V_K = 0$ V, $L_G = L_{In} = 200$ nm and $\alpha = 0°$. No top or side D_{it}.

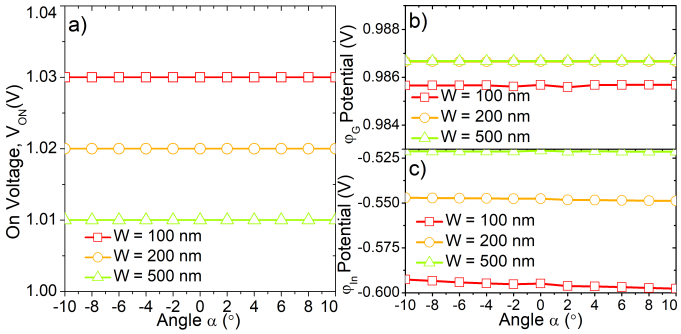

Fig. 4. 3D TCAD simulated a) V_{ON} for different trapezoidal body geometries depending on the α angle. Corresponding b) φ_G and c) φ_{In} to investigate the impact on the electrostatics at $V_A = 0$ V. $V_{FG} = 1.2$ V, $V_{BG} = -1$ V, $V_K = 0$ V and $L_G = L_{In} = 200$ nm. No top or side D_{it}.

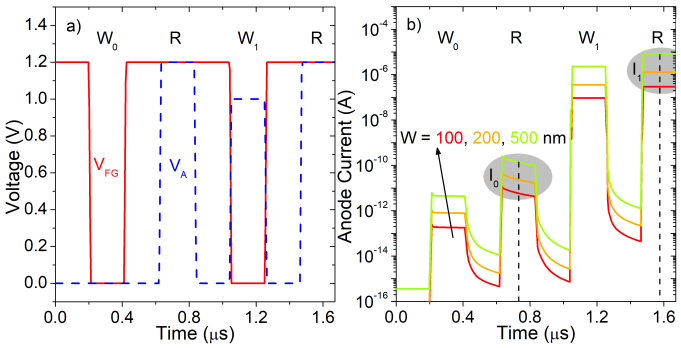

Fig. 5. 3D TCAD simulated a) bias pattern containing the W$_0$-R-W$_1$-R sequence. b) Current readout for different widths as in Fig. 3. $V_{BG} = -1$ V, $V_K = 0$ V and $L_G = L_{In} = 200$ nm. $\alpha = 0°$. No top or side D_{it}.

energy barrier evolution demonstrating the device triggering thanks to the energy barrier collapse can be analyzed in Fig. 3c (extracted for $W = 100$ nm in Fig. 3a). Finally, Fig. 3d depicts the negligible impact the back-gate terminal (located underneath the doped substrate) work-function has on the SOI film electrostatic compared to the ground-plane doping.

The impact of the trapezoidal body shape is depicted in Fig. 4. The ON voltage is represented as a function of α for several widths, Fig. 4a. The corresponding φ_G and φ_{In} are also plotted in Fig. 4b,c, respectively. Due to the ultra-thin Si film and large width, the body geometry (through the parameter α) does not deeply affect the gated region potential and it remains essentially fixed ($\simeq$1 mV range) for any width. Nevertheless, it is expected that narrower devices will experience a larger α impact. The effect along the ungated region is more evident but the impact in this region is much less important on the Z^2-FET triggering. In conclusion, for relatively wide devices the potential slightly depends on the width and is almost constant with the sidewalls tilt, proving its limited influence on the Z^2-FET characteristics.

B. Memory operation

The memory operation is verified by applying a bias pattern consisting on a W$_0$-R-W$_1$-R sequence, Fig. 5a. The current readout, shown in Fig. 5b, validates the memory behavior without any width-induced perturbation: I_1 (read, R, current after programming '1'-state, W$_1$) is much higher than I_0 (read current after writing '0'-state, W$_0$). Note that the biasing conditions have not been extensively optimized in this work.

IV. Interface States Distributions Influence

This section accounts for different trap densities located at the passivation/silicon interface affecting the Z^2-FET operation. An initial overview of the influence in DC variability (ON voltage) is first studied. Later the impact of the traps location is investigated for narrow and short devices (those more severely impacted) and finally worse trap profiles are selected to analyze their influence on DRAM operation. Different trap nature (acceptor and donor) as well as concentrations ($D_{it} = 10^{11}$, 5×10^{11} and 10^{12} cm^{-2}/eV) are investigated. Randomly-generated trap profiles, following Gaussian-like spatial distributions are initially contemplated. The trap energy profile is centered at the intrinsic level, E_i (see inset in Fig. 7b): it represents a pessimistic memory scenario since it improves the SRH generation/recombination mechanism [19]. Other trap energy distributions (centered at $E_i \pm 0.28$ eV for acceptor/donor, respectively [20]) were simulated with no significant difference in the V_{ON} statistics (not shown). It is worth remarking that, since trap spatial distributions are

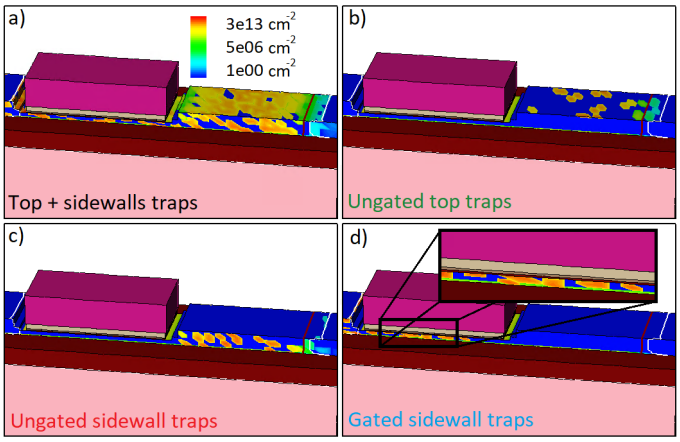

Fig. 6. 3D TCAD structure comparison between distinct random donor Gaussian trap profile locations and concentrations. a) top + sidewalls ($D_{it} = 10^{12}$ cm^{-2}/eV), b) ungated top ($D_{it} = 10^{11}$ cm^{-2}/eV), c) ungated sidewalls ($D_{it} = 5 \times 10^{11}$ cm^{-2}/eV) and d) gated sidewalls ($D_{it} = 10^{12}$ cm^{-2}/eV) interface trap distributions. $L_G = L_{In} = 200$ nm, $W = 100$ nm and $\alpha = 0°$.

not truly random these simulations only serve to evaluate pessimistic profiles and analyze their impact on the memory operation afterward. Finally, no serious impact is expected if the passivation silicon nitride (Si_3N_4), surrounding the Z^2-FET, is changed to other material as SiO_2. Depending on the new material permittivity the impact will be marginally diluted or strengthened.

Figure 7a-b shows the anode current curves for different trap concentrations and nature. As the trap density increases, the ON voltage grows either for donor or acceptor concentrations, reflecting a weakening of the carrier injection (barriers are enhanced). It can be observed that, even with identical D_{it} concentration, a different spatial trap distribution in the device yield significant V_{ON} variations. The mean and standard deviation for fixed D_{it} densities are plotted in Fig. 7c,d and summarized in Table I. The statistical error from simulations is taken as the standard deviation (σ) from the mean (μ). Since the dispersion is reduced, the number of repetitions for different D_{it} random profiles is limited to 6 iterations unless specified otherwise.

TABLE I. ON VOLTAGE STATISTICS WHEN TRAPS ARE LOCATED AT SIDEWALLS AND UNGATED TOP SECTION. $L_G = L_{In} = 200\ nm$, $\alpha = 0°$.

Donor						
D_{it} (cm^{-2}/eV)	10^{11}		5×10^{11}		10^{12}	
W (nm)	μ (V)	σ (V)	μ (V)	σ (V)	μ (V)	σ (V)
100	1.123	0.026	1.218	0.008	1.255	0.006
200	1.093	0.019	1.203	0.008	1.236	0.005
500	1.100	0.012	1.183	0.003	1.217	0.005
Acceptor						
D_{it} (cm^{-2}/eV)	10^{11}		5×10^{11}		10^{12}	
W (nm)	μ (V)	σ (V)	μ (V)	σ (V)	μ (V)	σ (V)
100	1.118	0.023	1.184	0.019	1.235	0.009
200	1.087	0.024	1.183	0.004	1.224	0.004
500	1.097	0.011	1.173	0.006	1.218	0.005

The standard deviation is drastically reduced when moving to broad Z^2-FETs. Wider devices are less sensitive to trap

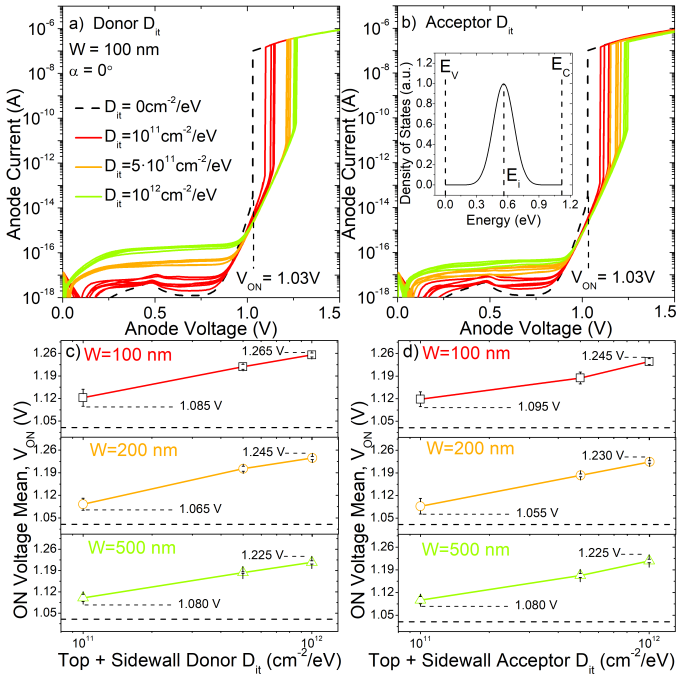

Fig. 7. 3D TCAD simulated a-b) $I_A(V_A)$ curves (6 iterations with $W = 100$ nm) and c-d) statistics for a-c) donor and b-d) acceptor D_{it} concentrations and several widths. $\alpha = 0°$. Inset in b) shows the donor/acceptor energy trap distribution. The interface density of states is located both at the sidewalls and the top ungated regions, see Fig. 2. Horizontal dashed lines indicate the ON voltage without D_{it}. $V_{FG} = 1.2$ V, $V_{BG} = -1$ V, $V_K = 0$ V and $L_G = L_{In} = 200$ nm.

distribution randomness as if the influence were diluted with the surface. For instance, the $W = 1$ μm width Z^2-FET systematically presents $\sigma \leq 5$ mV (not shown). Nevertheless, the D_{it} concentration still affects wide devices. Although the maximum and minimum ON voltage is the same at $W = 0.5$ μm regardless of the trap type, the ON voltage distribution is not identical. Note as well that increasing the interface defects density reduces the dispersion since the surface becomes more homogeneous (as observed in Fig. 6). The variability increase motivates a detailed study exclusively focused on narrow Z^2-FETs, which are as well the most interesting from the scaling and integration point of view. The discrimination of each trap-profile location impact on the performance is now analyzed splitting the traps into three distinct positions according to Fig. 2 and 6. Results are illustrated in Fig. 8 and detailed in Table II.

As occurred with wider devices, increasing the interface state density typically yields larger V_{ON} shifts but lower variability. The reduced randomness found at the gated sidewall region for low D_{it} can be explained by the small surface and limited concentration of traps (overall insignificant trap density) together with the enhanced top-gate induced electrostatic control. Interestingly, in contrast to traps at the ungated region, donor gated sidewall traps impact on the V_{ON} is barely noticeable with only 20 mV V_{ON} shift. However, donor traps along the ungated top region systematically induce the

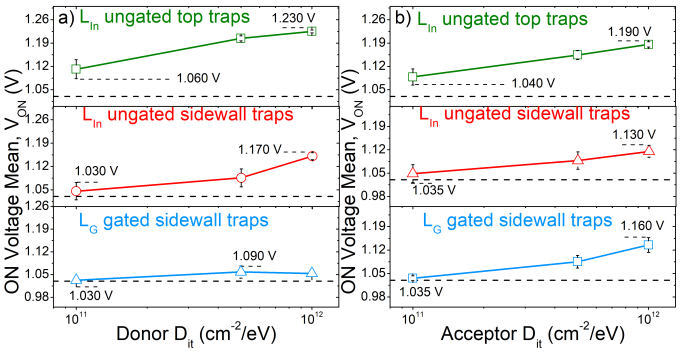

Fig. 8. 3D TCAD simulated V_{ON} statistics (6 iterations) for a) donor and b) acceptor D_{it} concentrations at different locations according to Fig. 2 and 6. Horizontal dashed lines indicate the ON voltage without D_{it} (1.03 V). $W = 100$ nm and $\alpha = 0°$, $V_{FG} = 1.2$ V, $V_{BG} = -1$ V, $V_K = 0$ V and $L_G = L_{In} = 200$ nm.

TABLE II. ON VOLTAGE STATISTICS AT DISTINCT TRAP LOCATIONS. $L_G = L_{In} = 200\,nm$, $W = 100\,nm$ AND $\alpha = 0°$.

Donor						
D_{it} (cm^{-2}/eV)	10^{11}		5×10^{11}		10^{12}	
Traps location	μ (V)	σ (V)	μ (V)	σ (V)	μ (V)	σ (V)
Ungated top	1.112	0.029	1.204	0.007	1.225	0.004
Ungated sidewalls	1.046	0.026	1.086	0.027	1.151	0.010
Gated sidewalls	1.033	0.004	1.059	0.023	1.053	0.009
Acceptor						
D_{it} (cm^{-2}/eV)	10^{11}		5×10^{11}		10^{12}	
Traps location	μ (V)	σ (V)	μ (V)	σ (V)	μ (V)	σ (V)
Ungated top	1.088	0.024	1.154	0.016	1.186	0.008
Ungated sidewalls	1.048	0.027	1.088	0.026	1.115	0.017
Gated sidewalls	1.036	0.007	1.085	0.019	1.135	0.022

larger ON voltage shifts compared to any other trap type and location. Following with the observed trend, a larger variability is expected for even narrower cells ($W < 100$ nm).

Gate length influence

The D_{it} impact when shortening the gate or the intrinsic lengths is summarized in Table III. The typical ON voltage dependence with the length is observed: shorter Z^2-FETs reduce the triggering point due to the short channel effects [12]. It is worth noting that if L_{In} is too short the energy barriers are weak, the ON voltage drops and the device loses the sharp switching and memory operation [17]. However, since the triggering voltage increases with the D_{it} (Fig. 7a-b), the V_{ON} can be recovered. This is interesting since it enables a more aggressive cell downscaling with reduced randomness. As with the width, the device-to-device variability increases when reducing the length, especially for low D_{it} as the impact cannot be averaged along the whole surface. If the D_{it} is large, the V_{ON} distribution follows the same trend as for longer devices and it gets much narrower.

V. IMPACT ON 1T-DRAM MEMORY PERFORMANCE

The extreme trap distribution profiles (for $W = 100$ nm and $L_G = L_{In} = 200$ nm) are now used to analyze the impact on the memory performance: distributions with the lowest and highest V_{ON} are selected. They correspond to a

TABLE III. ON VOLTAGE STATISTICS WHEN SCALING THE Z^2-FET (SIDEWALLS AND TOP TRAPS). $W = 100\,nm$ AND $\alpha = 0°$.

Donor						
D_{it} (cm^{-2}/eV)	10^{11}		5×10^{11}		10^{12}	
$L_{In} = 200$ **nm**	μ (V)	σ (V)	μ (V)	σ (V)	μ (V)	σ (V)
$L_G = 150$ **nm**	1.068	0.031	1.199	0.005	1.233	0.005
$L_G = 100$ **nm**	1.101	0.012	1.166	0.011	1.198	0.014
$L_G = 50$ **nm**	1.019	0.027	1.089	0.010	1.113	0.016
D_{it} (cm^{-2}/eV)	10^{11}		5×10^{11}		10^{12}	
$L_G = 200$ **nm**	μ (V)	σ (V)	μ (V)	σ (V)	μ (V)	σ (V)
$L_{In} = 150$ **nm**	1.071	0.043	1.173	0.011	1.205	0.014
Acceptor						
D_{it} (cm^{-2}/eV)	10^{11}		5×10^{11}		10^{12}	
$L_{In} = 200$ **nm**	μ (V)	σ (V)	μ (V)	σ (V)	μ (V)	σ (V)
$L_G = 150$ **nm**	1.036	0.028	1.154	0.019	1.197	0.009
$L_G = 100$ **nm**	1.099	0.012	1.159	0.007	1.202	0.005
$L_G = 50$ **nm**	1.004	0.042	1.058	0.015	1.081	0.012
D_{it} (cm^{-2}/eV)	10^{11}		5×10^{11}		10^{12}	
$L_G = 200$ **nm**	μ (V)	σ (V)	μ (V)	σ (V)	μ (V)	σ (V)
$L_{In} = 150$ **nm**	1.058	0.048	1.166	0.020	1.212	0.006
$L_{In} = 100$ **nm**	No V_{ON}		1.115	0.012	1.199	0.012

donor $D_{it} = 10^{12}$ cm^{-2}/eV at all interfaces ($V_{ON} = 1.265$ V in Fig. 7c) and a low donor $D_{it} = 10^{11}$ cm^{-2}/eV concentration at the gated sidewall ($V_{ON} = 1.030$ V in Fig. 8a). The ON voltage shift is $\Delta V_{ON} = 0.235$ V which explains the high variability observed in experimental samples [13]. Two sets of parameters are investigated, the current levels (I_1 and I_0) and the normalized (to the non D_{it} scenario) retention time.

A. Current levels and ratio

Figure 9a compares the anode current readout from several D_{it} scenarios (solid lines) and the default structure without traps (dashed line). When the D_{it} is high, the logic '1'-state is lost due to the significant V_{ON} increase (see V_{ON} increase with D_{it} in Fig. 7a-b): the carrier injection is not high enough to trigger the Z^2-FET. Analogous results have been found at high temperature with 360 K (Fig, 9b). A value up to $D_{it} = 3 \times 10^{11}$ cm^{-2}/eV still allows proper memory operation (for the considered structure, biasing and timing conditions). Above this level, the '1'-state is lost due to the increase in the V_{ON} (larger energy barriers) as can be observed in Fig. 7c,d and 8. Such a high D_{it} presence (10^{12} cm^{-2}/eV) threats the memory operation also for other biasing conditions, either different V_{FG} (Fig. 9c) or V_A (Fig. 9d) present problems for the high current logic state. No success has been observed when using the back-gate bias, from -5 to +5 V, to try to mitigate the degradation and recover the memory operation (not shown).

B. Retention time

The retention time, t_{ret}, is obtained by gradually increasing the holding time (H_t) after programming in the H-W$_{1/0}$-H$_t$-R sequence. Figure 10a schematically illustrates the extraction process. Figure 10b shows the normalized retention as a function of the trap density concentration (donor top + sidewalls) for several surface recombination velocities (inversely proportional to the carrier lifetime) [18]. Larger trap densities notably degrade the retention time by over 50%. This retention degradation with interface states has been also

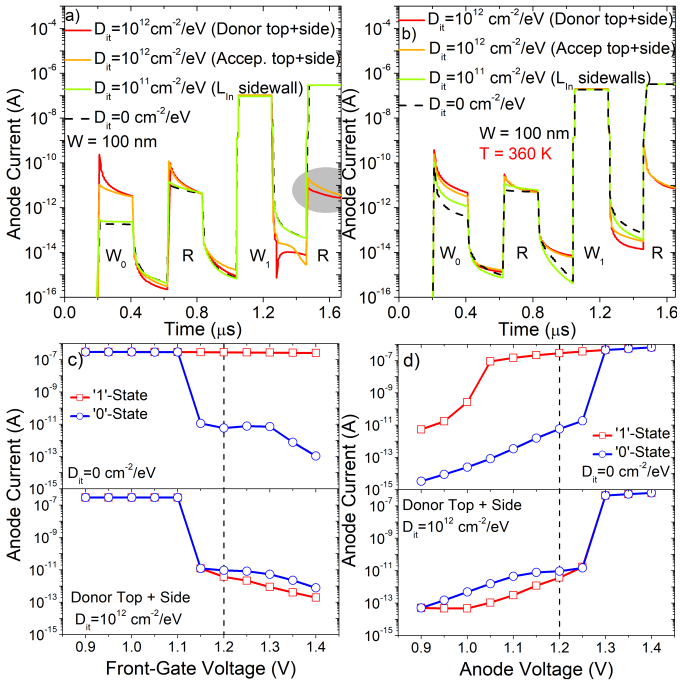

Fig. 9. Cell current readout for different trap distributions corresponding to extreme DC V_{ON} scenarios at a) room (300 K) and b) high (360 K) temperatures. The anode reading voltage at 360 K is reduced from 1.20 V to 1.15 V to prevent undesired '1'-state triggering. c) V_{FG} (with $V_A = 1.2$ V) and d) V_A (with $V_{FG} = 1.2$ V) logic states bias dependence for extreme D_{it} scenarios. $W = 100$ nm and $\alpha = 0°$, $V_{BG} = -1$ V, $V_K = 0$ V and $L_G = L_{In} = 200$ nm.

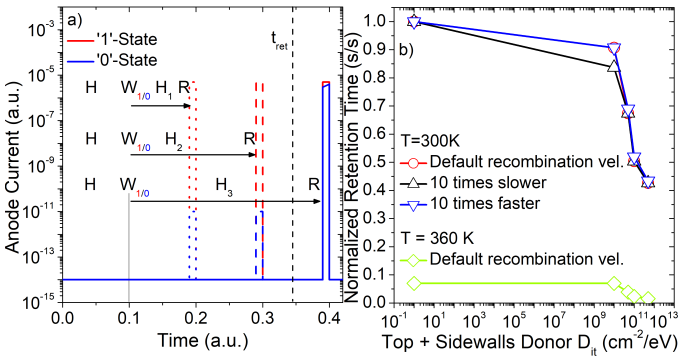

Fig. 10. a) Retention time extraction schematic with three H-$W_{1/0}$-H_t-R sequences. In the example the retention would be calculated as the average between the H_2 and H_3 holding times when the '0'-state flips into a '1'-state. b) Normalized (to the non-D_{it} scenario) retention time as a function of the interface trap density. Uncalibrated retention time is about 0.34 s for $D_{it} = 0$ cm^{-2}/eV at room temperature. The retention at high temperature (360 K) is calculated using a reading $V_A = 1.05$ V and the default recombination velocity. $W = 100$ nm and $\alpha = 0°$, $V_{BG} = -1$ V, $V_K = 0$ V and $L_G = L_{In} = 200$ nm.

observed experimentally [21]. More important is that interface states are strongly related, via the trap capture cross-section (σ) dependence with the trap energy [22], with the wide retention time variability observed in capacitorless cells [23], [24]. Since retention time in long Z^2-FETs is driven by the SRH generation at the anode-body junction [4], reducing the surface recombination velocity negatively impacts this figure of merit. On the other hand, faster recombination rates slightly enhance the retention time. Finally, by increasing the temperature the typical $\simeq$1 order of magnitude retention drop already observed in other 1T-DRAM cells [24] is obtained due to the enhanced generation/recombination processes.

Conclusion

The width or the body cross-section does not severely affect the Z^2-FET static and transient behavior down to W = 100 nm (minimum targeted width) thanks to the ultra-thin SOI film benefits. However, the presence of interface defects, especially at the top ungated region, actively degrades the 1T-DRAM operation enhancing the variability and explaining the ON voltage randomness from experiments. Wide Z^2-FETs are sensitive to the trap density while the trap distribution influence is diluted. On the other hand, narrow and short devices are affected by both the trap location profile and its concentration. Even when neglecting other variability sources, D_{it} might still induce DRAM operation failure. Nevertheless, high D_{it} densities could be deliberately sought at the expense of larger operating voltages and reduced retention times.

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