Experimental Demonstration of Operational Z^2-FET Memory Matrix

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***Abstract*—In this work, a functional Z^2-FET DRAM memory matrix is experimentally demonstrated for the first time. Word-level operation with simultaneous reading and programming accesses is successfully proved. Disturbance is also explored, and the results demonstrate bitline disturbance immunity. Furthermore, the fabricated memory matrix, which includes only one selector per word-line, facilitates the scalability of the memory for increasing array dimensions.**

***Index Terms*—Array, diode, DRAM, matrix, PIN, Silicon on Insulator, Z^2-FET.**

I. Introduction

DYNAMIC random access memories (DRAM) have been traditionally based on the 1T-1C (1 transistor, 1 capacitor) cell architecture [1], being the major drawback the CMOS process incompatibility and the scaling of the capacitor [2]. SOI-based capacitor-less DRAM cells [3]–[6] arise as a solution for embedded memory based devices. Z^2-FET 1T-DRAM is one of the most promising low-power solutions for the Internet of Things (IoT).

This Letter reports the performance of a functional Z^2-FET memory matrix. The structure has been fabricated in 28 nm FDSOI technology at STMicroelectronics [7], Fig.1a. The 2x2 array is addressed with common bitlines (columns) and wordlines (rows). In order to enable isolated word reading/programming and to avoid sneaky current paths, an N-type MOSFET is located at the wordline output as a selector device. Despite the larger Z^2-FET cell size ($\simeq$0.2 μm^2) with respect to a 6T-SRAM in 28FDSOI technology [8] ($\simeq$0.125 μm^2), TCAD simulations prove the cell is functional for reduced dimensions [9], drastically reducing its footprint.

II. Cell Characterization

For the electrical characterization of each memory cell and the memory matrix, two Agilent B1500A semiconductor analyzers were employed. They were responsible for driving the transient signals: bitline (BL), wordline (WL) and selector (M) terminals (Fig.1a) applied through arbitrary waveform generators (B1530). The simultaneous control of more than two lines required the development of custom software to remotely manage the semiconductor analyzer through a computer. The characterization at wafer-level was possible by employing a Suss Microtec PA300 PS-MA semiautomatic probe station. Due to equipment limitations and capacitance parasitics (cables, connectors and equipment), memory pulses were limited down to the μs range in order to ensure stable current levels for the later characterization. Nevertheless, TCAD simulations indicate that much faster Z^2-FET memory operation is feasible [10].

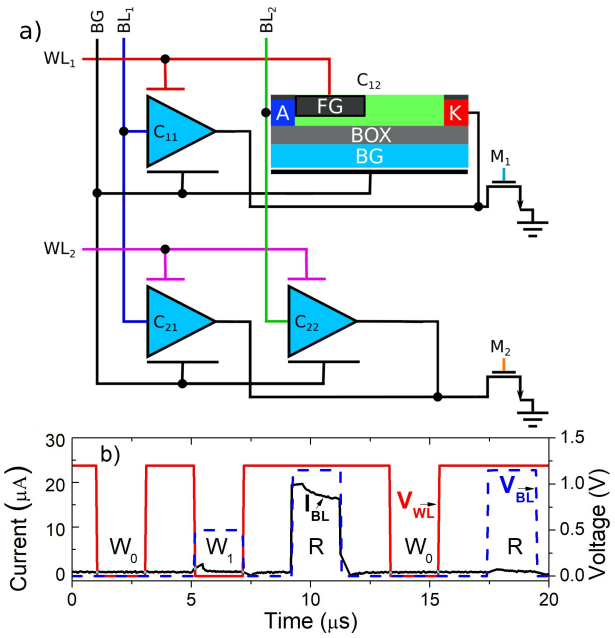

Fig. 1. a) Z^2-FET matrix diagram and cell device structure. Wordline (WL), bitline (BL), front gate (FG), back gate (BG), anode (A), cathode (K), selector (M). Each Z^2-FET cell (C_{XY}) features: $L_G = L_{in} = 200$ nm (gated/ungated region length), $W = 0.4$ μm, $EOT \simeq 1.5$ nm, $t_{Si} \simeq 7$ nm, $t_{Epi} \simeq 15$ nm (ungated epitaxy thickness) and $t_{BOX} \simeq 25$ nm. $N_{body} \simeq 10^{16}$ cm^{-3}, $N_{BG} > 10^{18}$ cm^{-3} and $N_{A/K} > 10^{21}$ cm^{-3}. b) Experimental demonstration of C_{11} Z^2-FET memory operation for a W_0-W_1-R-W_0-R sequence. Initial W_0 prior to W_1 guarantees worst '1'-state programming scenario.

The Z^2-FET cell structure (cell C_{12} in Fig.1a) resembles a conventional PIN diode with four terminals: anode (A), cathode (K) and front and back gates (FG/BG). The intrinsic region comprises a gated region covered by the top gate (L_G) adjacent to the anode, and an ungated region (L_{in}) adjacent to the cathode, while the ground plane (acting as BG) lies below the whole device. Default positive front-gate bias is

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employed to induce a potential barrier along the gated region. Similarly, a negative voltage is applied to the ground plane to build a complementary barrier in the ungated section. The barriers height modulation, by altering the inner carrier density (especially electrons below the front gate), yields different Z^2-FET conductance values and thus distinct logic states. To drive all device terminals, specific bias patterns were designed for each experimental test. Proper single-cell operation was initially verified by applying the W_0-W_1-R-W_0-R sequence to cell C_{11}, Fig. 1b. The initial '0'-state writing (W_0) forced the worst possible scenario to store the '1'-state (W_1). To program the Z^2-FET, the top gate is grounded to suppress the lateral body-anode barrier, allowing carriers to be injected or evacuated. Otherwise, the top gate voltage remains always positive. For the '1'-state writing (W_1), carriers are introduced by pulsing the anode potential forward biasing the Z^2-FET as a PIN diode. Contrarily, to program the '0'-state, the anode is grounded and the body becomes depleted thanks to capacitive coupling. An increase in the anode bias, with positive front-gate biasing leading to higher injection barriers, is used for reading (R). The reading anode voltage should (not) be high enough to inject carriers and trigger a cell storing the '1' ('0') -state. In case the cell is not accessed, it remains on hold (H) state by default (grounded anode while gate-induced barriers prevent carrier injection or evacuation). Therefore, the previously stored logic state is preserved. Table I summarizes the applied voltages at each terminal for all memory operations. The bitline current in Fig. 1b validates the memory behavior: high current margin between logic states and very low current during programming which reduces power consumption [11]. The anode current can be modulated to enhance the current level margin and ratio by increasing the anode voltage (the front-gate bias would probably need to be adjusted as well). As a consequence, the power consumption could be compromised. Scaling the cell might also improve the current logic '1' level due to the reduction in the series resistance and the lateral electric field increment. Exhaustive Z^2-FET details, operating as isolated memory cell, are found in [10], [12].

TABLE I
BIASING CONDITIONS FOR MEMORY OPERATION. PULSES FEATURE $t_{r/f} = 50\ ns$ (RISE/FALL TIMES) WITH $t_w = 2\ \mu s$ (PULSE WIDTH). * THE CATHODE TERMINAL IS DRIVEN THROUGH THE SELECTOR TRANSISTOR.

Z^2-FET Cell	Matrix	W_0	W_1	R	H	D
Anode	Bitline	0	0.5	1.15	0	1.15
Cathode*	-	$\simeq 0$	$\simeq 0$	$\simeq 0$	High-Z	High-Z
Front gate	Wordline	0	0	1.2	1.2	1.2
Back gate	Back Gate	-1	-1	-1	-1	-1
-	Selector	1.2	1.2	1.2	0	0

III. MATRIX CHARACTERIZATION

A. Word-level operation

One of the major advantages of the Z^2-FET resides in the simultaneous word reading and programming functionality. The concurrent access drastically increases the memory speed with respect to the individual access scenario. This property

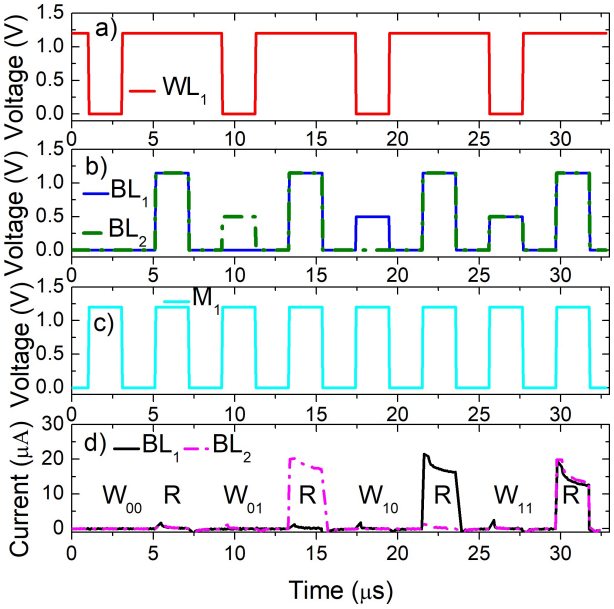

Fig. 2. a) Wordline (WL_1), b) bitline (BL_1 and BL_2) and c) selector (M_1) bias pattern to test the memory response at word level. The sequence corresponds to W_{00}-R-W_{01}-R-W_{10}-R-W_{11}-R operations. d) Bitline current readouts demonstrating the simultaneous word reading and programming. The output selector, M_1, is pulsed for every word access (reading or programming).

is possible due to: *i)* the output transistors (M_X) that allow to independently select the accessed word (avoiding the operation of other matrix rows) and *ii)* the wordline bias which does not depend on the programming/reading logic value. Consequently, only one memory cycle is necessary to modify or discriminate the word content. In fact, individual cell writing is not possible: while programming one cell, undesired '0'-state store operations would be carried out in all other cells within the same word (not shown). In case the desired word length does not match the array word size, the matrix would suffer an area efficiency penalty.

To characterize the word-level operation, the sequence of logic-values '00'-'01'-'10'-'11' was written, one by one, to both cells (C_{11} and C_{12}) and then read, Fig.2a,b. Only when the row is being accessed, the M_1 selector signal is pulsed (Fig.2c) grounding the cathodes and enabling efficient reading/programming operations. The bitline currents (Fig.2d) demonstrate that the written logic word is successfully recovered later for any case.

B. Bitline disturbance immunity

Disturbance tests (D in Table I) assess whether the cell state is perturbed when accessing other cells sharing the same bitline. Wordline disturbances are not possible due to the simultaneous word programming and reading. The state degradation test is performed as follows: i) C_{11} and C_{12} are programmed (Fig.3a,b) while pulsing M_1 (Fig.3c) at the same time; ii) the word is then read to verify its content; iii) after reading, M_1 is left grounded to isolate the C_{11} and C_{12} word; iv) BL_1 and BL_2 are pulsed afterward to emulate accessing C_{21} and C_{22}, potentially disturbing the C_{11} and C_{12} state; v) C_{11} and C_{12} are finally read back to check their

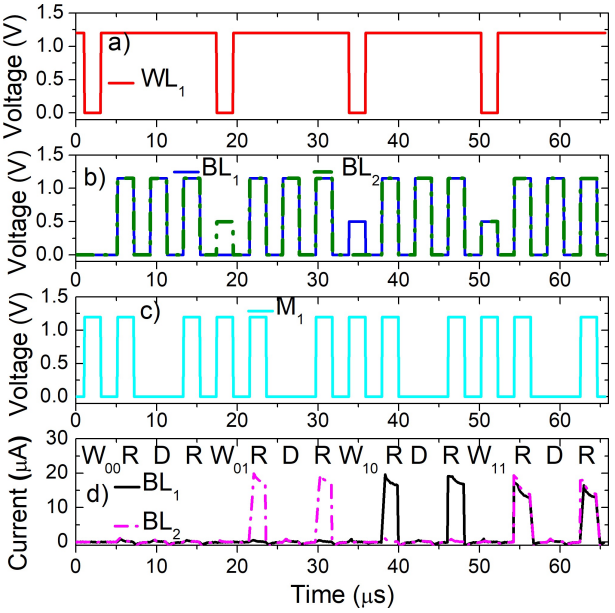

Fig. 3. a) Wordline (WL_1), b) bitline (BL_1 and BL_2) and c) selector (M_1) bias pattern (W_{00}-R-D-R-W_{01}-R-D-R-W_{10}-R-D-R-W_{11}-R-D-R) to test the word operation under bitline disturbances (D). During perturbations, the output selector M_1 is in cut-off regime to isolate the word content. d) Bitline current readout showing the bitline disturbance immunity.

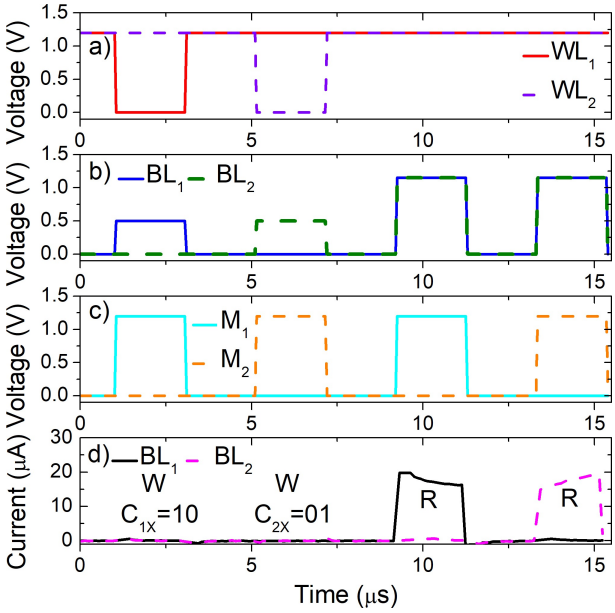

Fig. 4. a) Wordline (WL_1 and WL_2), b) bitline (BL_1 and BL_2) and c) selector (M_1 and M_2) bias pattern to test the entire memory operation. The sequence corresponds to W_{10}(into C_{1X})-W_{01}(into C_{2X})-R(C_{1X})-R(C_{2X}) operations, with C_{nX} being the nth matrix row cells. d) Bitline current readout illustrating the recovered logic states for all the cells.

bitline disturbance resilience. The process is then repeated for other logic state combinations. Fig.3d shows the bitline current readouts when the following logic words are written into the test row: '00', '01', '10' and '11'. Notice that the bitline current readouts before and after applying disturbance coincide for all cases, proving the correct behavior and immunity to other words access. In real applications, not only one but multiple disturbance pulses could impact each cell possibly leading to reading failures afterward. However, the expected memory operation speed (ns range) is much faster than the applied pulses. Therefore, the degradation in Fig.3 can be seen as many disturbance pulses in a row. Nevertheless, the disturbance immunity can be enhanced by rising the wordline (front-gate) voltage to further prevent carrier injection from the anode.

C. Integral operation

Finally, the entire matrix operation was verified by programming and reading the two available words with the same pattern. Due to the simultaneous writing and reading, only four access cycles are required to store and discriminate all cells logic state in the array. Fig.4 illustrates an example of bias patterns and the bitline current readouts. The pattern consisted in: the '10'-logic word was written in the first row (C_{11} and C_{12}, Fig.4a,b) while only M_1 output selector was pulsed (M_2 remained off, Fig.4c). Then, the '01'-logic word was written in the second row (C_{21} and C_{22}) while the output selector signals were inverted. Lastly, the two words were consecutively read. Figure 4d demonstrates adequate logic states extraction.

Despite the fact that the proposed memory matrix represents the smallest case, it can be easily up-scaled to larger array dimension designs. By simply including Z^2-FET cells in the row, the word size is extended maintaining a single selector transistor. Similarly, the matrix storage capacity can be enhanced by including additional words (rows) without degrading the expected memory performance.

IV. Conclusion

A Z^2-FET memory matrix has been experimentally evaluated. Single-cell and by-word memory access operation point out the correct behavior of the fabricated matrix. Disturbance tests also show the matrix does not exhibit any degradation of the logic states. Finally, all the matrix cells have been fully accessed emulating real operation, reporting promising results and proving the proposed array design as easy to scale.

REFERENCES

[1] "Field-effect transistor memory," Jun. 4 1968, US Patent 3,387,286.

[2] E. Gerritsen, N. Emonet, C. Caillat, N. Jourdan, M. Piazza, D. Fraboulet, B. Boeck, A. Berthelot, S. Smith, and P. Mazoyer, "Evolution of materials technology for stacked-capacitors in 65nm embedded-DRAM," *Solid-State Electronics*, vol. 49, no. 11, pp. 1767 – 1775, 2005. DOI: 10.1016/j.sse.2005.10.024

[3] S. Okhonin, M. Nagoga, J. M. Sallese, and P. Fazan, "A SOI capacitorless 1T-DRAM concept," in *2001 IEEE International SOI Conference. Proceedings*, Oct 2001, pp. 153–154. DOI: 10.1109/SOIC.2001.958032

[4] M. Bawedin, S. Cristoloveanu, and D. Flandre, "A Capacitorless 1T-DRAM on SOI Based on Dynamic Coupling and Double-Gate Operation," *IEEE Electron Device Letters*, vol. 29, no. 7, pp. 795–798, July 2008. DOI: 10.1109/LED.2008.2000601

[5] N. Rodriguez, F. Gamiz, C. Navarro, C. Marquez, F. Andrieu, O. Faynot, and S. Cristoloveanu, "Experimental developments of A2RAM memory cells on SOI and bulk substrates," *Solid-State Electronics*, vol. 103, pp. 7–14, jan 2015. DOI: 10.1016/j.sse.2014.09.001

[6] N. Rodriguez, F. Gamiz, and S. Cristoloveanu, "A-RAM Memory Cell: Concept and Operation," *IEEE Electron Device Letters*, vol. 31, no. 9, pp. 972–974, sep 2010. DOI: 10.1109/LED.2010.2055531

[7] N. Planes, O. Weber, V. Barral, S. Haendler, D. Noblet, D. Croain, M. Bocat, P. O. Sassoulas, X. Federspiel, A. Cros, A. Bajolet, E. Richard, B. Dumont, P. Perreau, D. Petit, D. Golanski, C. Fenouillet-Branger, N. Guillot, M. Rafik, V. Huard, S. Puget, X. Montagner, M. A. Jaud, O. Rozeau, O. Saxod, F. Wacquant, F. Monsieur, D. Barge, L. Pinzelli, M. Mellier, F. Boeuf, F. Arnaud, and M. Haond, "28nm FDSOI technology platform for high-speed low-voltage digital applications," in *2012 Symposium on VLSI Technology (VLSIT)*. IEEE, 2012, pp. 133–134. DOI: 10.1109/VLSIT.2012.6242497

[8] V. Joshi, H. Ramamurthy, S. Balasubramanian, S. Seo, H. Yoon, X. Zou, N. Chan, J. Yun, T. Klick, E. Smith, J. Schmid, R. vanBentum, J. Faul, and C. Weintraub, "Low-variation sram bitcells in 22nm fdsoi technology," in *2017 Symposium on VLSI Technology*. IEEE, 2017, pp. T222–T223. DOI: 10.23919/VLSIT.2017.7998179

[9] C. Navarro, M. Duan, M. S. Parihar, F. Adamu-Lema, S. Coseman, J. Lacord, K. Lee, C. Sampedro, B. Cheng, H. E. Dirani, J.-C. Barbe, P. Fonteneau, S.-I. Kim, S. Cristoloveanu, M. Bawedin, C. Millar, P. Galy, C. L. Royer, S. Karg, H. Riel, P. Wells, Y.-T. Kim, A. Asenov, and F. Gamiz, "Z^2-FET as Capacitor-Less eDRAM Cell For High-Density Integration," *IEEE Transactions on Electron Devices*, vol. 64, no. 12, pp. 4904–4909, 2017.

[10] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "A compact capacitor-less high-speed DRAM using field effect-controlled charge regeneration," *IEEE Electron Device Letters*, vol. 33, no. 2, pp. 179–181, 2012. DOI: 10.1109/LED.2011.2176908

[11] M. S. Parihar, K. H. Lee, H. E. Dirani, C. Navarro, J. Lacord, S. Martinie, J. C. Barbe, P. Fonteneau, P. Galy, C. L. Royer, X. Mescot, F. Gamiz, B. Cheng, A. Asenov, Y. Taur, M. Bawedin, and S. Cristoloveanu, "Low-Power Z^2-FET Capacitorless 1T-DRAM," in *2017 IEEE International Memory Workshop (IMW)*. IEEE, 2017, pp. 1–4. DOI: 10.1109/IMW.2017.7939093

[12] C. Navarro, J. Lacord, M. S. Parihar, F. Adamu-Lema, M. Duan, N. Rodriguez, B. Cheng, H. E. Dirani, J. C. Barbe, P. Fonteneau, M. Bawedin, C. Millar, P. Galy, C. L. Royer, S. Karg, P. Wells, Y. T. Kim, A. Asenov, S. Cristoloveanu, and F. Gamiz, "Extended Analysis of the Z^2 -FET: Operation as Capacitorless eDRAM," *IEEE Transactions on Electron Devices*, vol. 64, no. 11, pp. 4486–4491, Nov 2017. DOI: 10.1109/TED.2017.2751141