A thorough study of Si nanowire FETs with 3D Multi-Subband Ensemble Monte Carlo simulations

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Abstract

In this paper, the DC electrical behavior of n-MOS transistors based on Si nanowires with ⟨100⟩ and ⟨110⟩ channel orientations is thoroughly compared by means of Multi-Subband Ensemble Monte Carlo simulations. We find that the drain current depends on the nanowire diameter and it is slightly, but consistently, larger for ⟨100⟩ than for ⟨110⟩ nanowires. The observed differences in mobility, velocity and spatial charge distribution are interpreted in terms of the effective masses and populations of the different Si conduction band valleys, whose six-fold degeneracy is lifted by quantum confinement in narrow nanowires. Finally, we study the scaling behavior for channel lengths down to 8 nm, concluding that the differences observed between both orientations are minimal.

Keywords: Gate-all-around MOSFET, Monte Carlo simulation, multi-subband, short-channel effects, nanowire orientation.

1. Introduction

Scaling the channel length of Field-Effect Transistors (FETs) in the nanometer range is not trivial if we strive to keep short channel effects under control. To achieve this goal, a strong electrostatic control of the gate electrode over the channel charge is required. The best possible electrostatic control is obtained when the channel is completely surrounded by the gate, as in the Gate-All-Around (GAA) devices [1]. In this

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paper, we consider GAA transistors based on cylindrical Si nanowires with different crystal orientations and sub-10 nm diameter. When different nanowire orientations are considered, it is found that ⟨100⟩ oriented devices show larger electron mobility [2] and higher ballistic conductance [3]. However, the performance of very short channel devices cannot be predicted only based on these parameters as a comprehensive device description is needed, especially to assess the scaling perspective and the short channel effects. The comparison between ⟨100⟩ and ⟨110⟩ nanowires is especially relevant: a potentially better performance of the former configuration with respect to the latter would pose a fabrication challenge to integrate nanowire-based transistors with traditional bulk FETs or FinFETs with ⟨110⟩ channel orientation.

To perform such a study, we employ an in-house developed 3D Multi-Subband Ensemble Monte Carlo simulator [4], which takes into account the quantum effects of 2D confinement, thanks to the solution of the 2D Schrödinger equation in several cross sections of the device, and employs Monte Carlo (MC) method, able to model non-equilibrium transport and compute the $I - V$ characteristics. The simulator has already proved its capabilities for the analysis of 3D devices where 2D confinement is important, such as Si nanowires [4] and FinFETs with small cross section [5].

The outline of this paper is as follows: in section 2 we briefly describe the simulator, in section 3 we define the structure of the devices under study and discuss the results and, finally, in section 4 we draw the main conclusions.

2. Simulation setup

The 3D simulation tool employed in this work is based on the space-mode approach and has been described in detail in previous publications [4, 5]. Its main feature with respect to classical or quantum-corrected MC simulators is that quantum confinement in the plane perpendicular to electron transport is fully taken into account, by solving the 2D Schrödinger equation in several cross sections along the device. For transport, the simulator solves the 1D Boltzmann equation through the Ensemble MC method, taking the solutions of the Schrödinger equation as inputs: subband energy profiles determine the drift field and wave-functions are employed to compute the scattering

rates. Finally, self consistency is achieved by coupling this procedure in a loop with the solution of the 3D Poisson equation.

The structure of the device under study is described employing a 3D finite element mesh with tetrahedral elements. As we need to solve the Schrödinger equation in different cross sections of the device, this 3D mesh is constructed by extruding a 2D triangular mesh. The choice of finite elements allows a good representation of complex geometries and is particularly appropriate for the modeling of rounded devices such as the cylindrical nanowires studied in the present work. Electronic band structure is described employing the effective mass model with anisotropic valleys and non-parabolic corrections [6]. For very narrow nanowires, this description is not as accurate as the one that could be obtained employing multiple-band $\boldsymbol{k} \cdot \boldsymbol{p}$ models or atomistic ones such as those based on the Density Functional Theory or Tight Binding approach. However, the effective mass model can provide reliable results [7, 8] employing bulk values of the effective masses for Si nanowires down to a diameter of 5 nm and even below, if these values are correctly fitted [8]. The 1D MC simulation includes carrier scattering by acoustic and optical phonons [9], taking into account Pauli exclusion principle [10]. A variance reduction technique based on non-uniform super-particle weight [11] is employed in order to improve the MC statistics, reducing the statistical noise in the sub-threshold regime: the weight of a simulation super-particle is computed according to its total energy [4]. To improve the performance of the simulator, a high level of parallelism is employed in the MC simulation and in the solution of Poisson and Schrödinger equations.

The same simulator also allows the calculation of carrier mobility. In this case only the channel of the device is considered, where a uniform electric field, F_z, is applied in the longitudinal direction, z, and the average electron velocity, v_z, is computed. Electron mobility is then extracted by fitting the curve of v_z vs. F_z in the limit of small field.

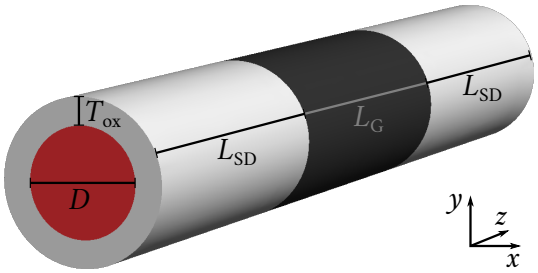

Figure 1: Structure of the devices simulated in this work. Device cross sections are parallel to the *xy* plane, transport is along *z* axis. The total length of the simulation domain in the *z* direction is $L_z = L_G + 2L_{SD}$.

3. Results and discussion

The devices considered in this paper are GAA n-MOSFETs based on cylindrical Si nanowires with channel along either the ⟨100⟩ or ⟨110⟩ directions. Three different nanowire diameters are employed in this work: $D = 4$ nm, 6 nm and 8 nm. When not explicitly stated otherwise, the channel length is $L_G = 14$ nm and in the final scaling study L_G is reduced down to 8 nm. The thickness of the SiO_2 gate oxide is $T_{ox} = 1$ nm, the channel is considered undoped and a midgap metal is employed as gate material. The doping density in source and drain regions is set to $N_{SD} = 1 \times 10^{20}$ cm^{-3}, with an underlap of $\Delta_{SD} = 2$ nm from the gate edges and a Gaussian distribution with $\sigma_{SD} = 0.8$ nm. The simulation domain includes source and drain regions for a length of $L_{SD} = 14$ nm each. The complete structure is depicted in Figure 1.

We first compute the transfer characteristics for the devices with the three values of the diameter and the two channel orientations, shown in Figure 2 for both low ($V_D = 50$ mV) and high ($V_D = 0.5$ V) values of drain bias. Before analyzing the results, we can observe that the statistical noise intrinsic to the MC procedure is evident only for values of I_D lower than 1 nA, thanks to the implementation of a variance reduction technique as previously mentioned. The trends we can observe in Figure 2 are the same for both values of V_D. First, I_D decreases as the nanowires diameter is reduced. This is the result of two cumulative effects: *i)* narrower devices have higher threshold voltage, V_{th}, because of stronger confinement which increases the subband energy levels, including the fundamental one; *ii)* narrower devices have smaller gate oxide capacitance per unit

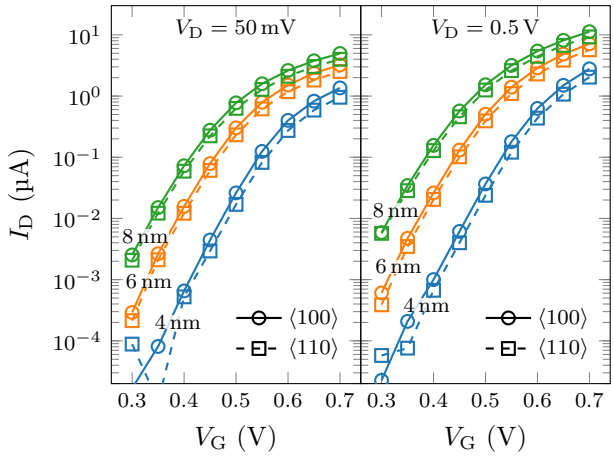

Figure 2: Transfer characteristics of ⟨100⟩ and ⟨110⟩ devices with different diameters, for $V_D = 50\,mV$ (left) and $V_D = 0.5\,V$ (right).

length and therefore lower carrier density for the same gate overdrive voltage. Second, comparing the curves corresponding to different channel orientations, we observe that ⟨100⟩ devices show a systematic larger current: the difference is not substantial, but it is noticeable in the whole range of gate bias and consistent for different values of the drain bias and nanowire diameter.

To check whether the difference between ⟨100⟩ and ⟨110⟩ devices is due to electrostatics or to transport properties, we first consider the inversion charge under the gate, which is shown in Figure 3, as a function of V_G for $V_D = 50\,mV$ for all devices. Here we can notice the same dependence on D as observed before for the current, but now the difference between both channel orientations has essentially disappeared. As another check, we compare the $I_D - V_G$ curves by factoring out the electrostatic effects. To do that, we rescale the drain current to take into account the device geometry. For planar devices, this would simply mean dividing I_D by the channel width W. Instead, for 3D devices, the correct normalization involves the gate capacitance per unit length that, for cylindrical nanowires, is given by [12]:

$$\frac{C_{ox}(D)}{L} = \frac{2\pi\kappa\epsilon_0}{\log(1 + 2T_{ox}/D)}$$

where κ is the dielectric constant of the oxide material and ϵ_0 is the permittivity of

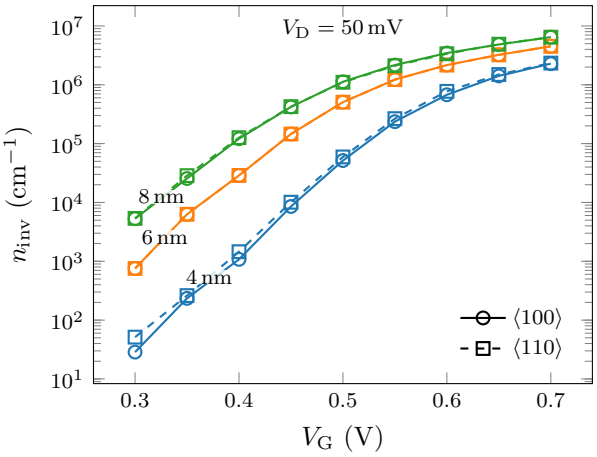

Figure 3: Linear inversion charge in the center of the devices with ⟨100⟩ and ⟨110⟩ and different diameters, for $V_D = 50\,mV$.

free space. Thus, we rescale the drain currents of the devices with different D as if they all corresponded to a nanowire with $D = 4\,nm$, obtaining the scaled current $I_{D,s} = I_D \cdot (C_{ox}(4\,nm)/C_{ox}(D))$. Then, $I_{D,s}$ is plotted against the gate overdrive voltage, that is $V_G - V_{th}$. The threshold voltage, V_{th}, is extracted employing a fixed value of the normalized current, $I_{D,s} = 0.02\,\mu A$. Figure 4 shows the resulting scaled transfer characteristics for $V_D = 50\,mV$: all the curves are essentially superposed in the sub-threshold regime indicating that electrostatic effects have been correctly factored out. On the other hand, a larger current can still be observed for ⟨100⟩ devices for large overdrive voltage. Therefore, we cannot ascribe such difference to electrostatics and we turn to the analysis of transport quantities, such as velocity and mobility.

The average electron velocity in the transport direction, v_z, is shown in Figure 5 as a function of position, z, along the channel, for a fixed overdrive voltage $V_G - V_{th} = 0.3\,V$, with both small ($V_D = 50\,mV$) and large ($V_D = 0.5\,V$) drain bias. It should be noticed that, for all considered nanowire diameters and drain biases, velocity is larger in ⟨100⟩ than in ⟨110⟩ channels. Now, we look separately at the results obtained for the two values of V_D. For low drain bias the longitudinal field is relatively small: transport is near equilibrium. In this case, we can observe that the velocity inside the channel gets higher for wider nanowires and the position of the peak velocity moves from the drain

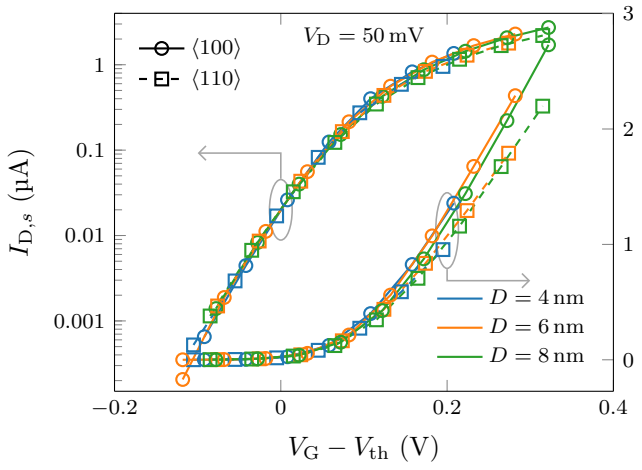

Figure 4: Normalized drain current $I_{D,s}$ versus overdrive voltage for ⟨100⟩ and ⟨110⟩ devices with different diameters. All curves are computed for $V_D = 50\,mV$.

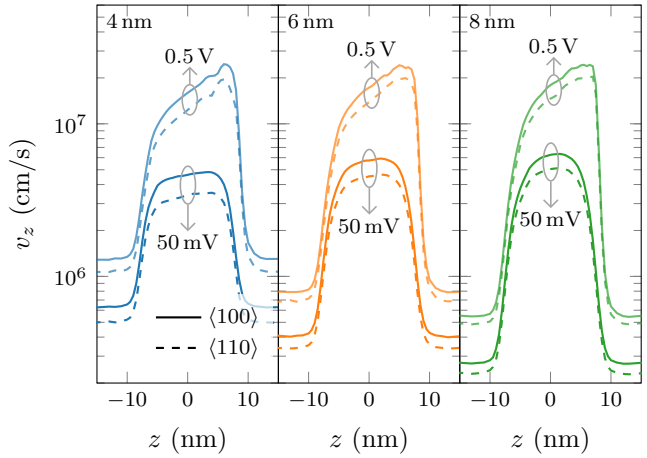

Figure 5: Ensemble average of the longitudinal electron velocity as a function of position z along the channel for the different diameters. The voltages indicated by arrows are the corresponding values of V_D.

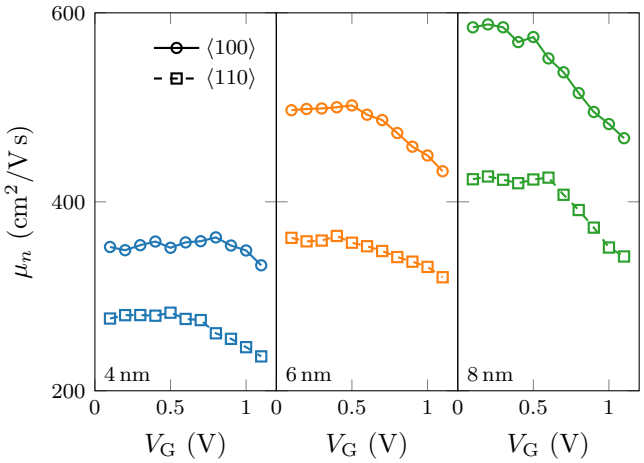

Figure 6: Electron mobility as a function of gate bias for the different orientations and nanowire diameters.

end of the channel towards its center. On the contrary, for high drain bias, transport is strongly out of equilibrium: now the shape and height of the velocity peaks in the channel is very similar for all considered values of D.

Next, we turn out attention to the electron mobility μ_n, computed for the same channel structures but now assuming infinite channel length in the limit of small longitudinal electric field. In Figure 6 we can observe that μ_n always decreases as the gate bias increases due to stronger carrier confinement: phonon scattering is larger when the electron wave-functions are localized in smaller regions [13]. However, such dependence is weaker in the case of the narrowest nanowire with $D = 4\,\text{nm}$, because confinement in this case is essentially generated by the silicon/oxide barriers and only weakly modified by the gate field. The increased geometrical confinement is the reason for the reduction of μ_n for narrower nanowires. In any case, consistently with [2], mobility in ⟨100⟩ channels is significantly larger than in ⟨110⟩ channels for all considered nanowire sizes, with up to 40% difference. These observations are consistent with the conclusions we drew in the analysis of velocity for low V_D: in both cases transport is near equilibrium. Summing up, we can conclude that transport properties of ⟨100⟩ nanowires are better than those of ⟨110⟩ nanowires, both in near equilibrium and with a strong longitudinal field.

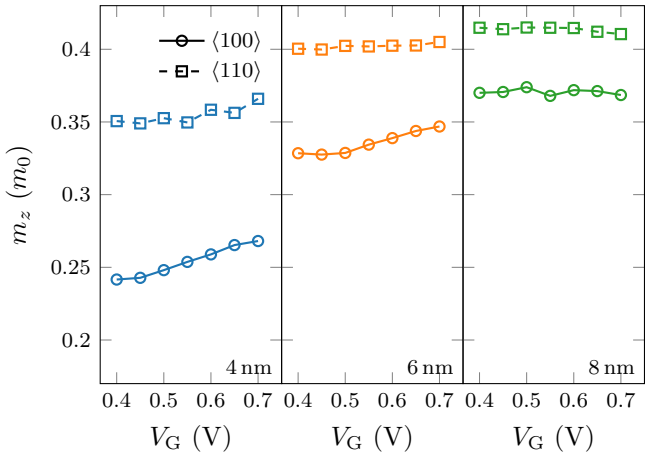

Figure 7: Average of electron effective transport mass in the middle of the channel as a function of gate bias for the different orientations and nanowire diameters.

This conclusion can be explained by analyzing the average of the effective transport mass, m_z, in the middle of the channel. This is computed as the average of the effective transport mass of each valley, weighted by the corresponding population. shown in Figure 7. Indeed, m_z is smaller in nanowires with ⟨100⟩ orientation that in those with ⟨110⟩ channel. The larger mass of wider nanowires does not translate into a lower velocity or mobility because larger D also imply a decrease of the scattering rates, as we already mentioned. The difference in effective mass for the two orientations stems from the different splitting of the six conduction bands of silicon (equivalent in the bulk semiconductor) due to quantum confinement. In ⟨100⟩ nanowires, there is a set of four valleys with the longitudinal mass, $m_l = 0.916\, m_0$, perpendicular to the nanowire axis and $m_z = m_t = 0.19\, m_0$: two valleys, Δ_x, with m_l along [100] and two valleys, Δ_y, with m_l along [010]. The other two valleys, Δ_z, have $m_z = m_l$ along [001] direction and an isotropic confinement mass equal to m_t in the nanowire cross section, as shown in Figure 8. The different confinement effective masses give rise to lower subband energies for Δ_x and Δ_y with respect to Δ_z valleys. As a consequence of this and of the larger multiplicity, valleys with low transport mass $m_z = 0.19\, m_0$ are overall more populated than those with $m_z = 0.916\, m_0$, as shown in the left part of Figure 8 for $V_G = 0.5$ V (other values of V_G give similar results). Therefore, ⟨100⟩ devices present

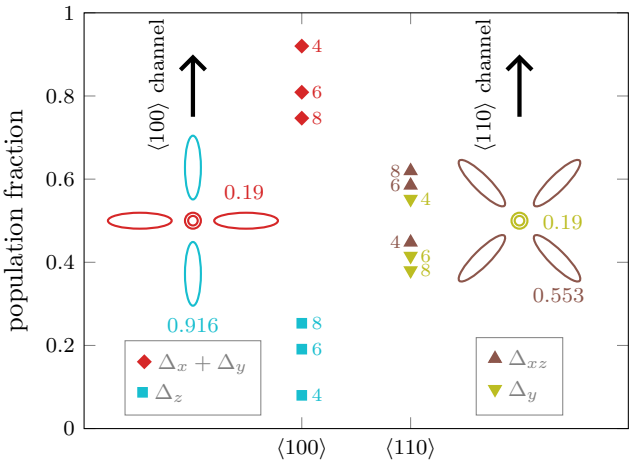

Figure 8: Schematic representation of the six conduction band valleys with respect to channel direction in ⟨100⟩ and ⟨110⟩ nanowires; the values near the ellipses are the transport masses of each set of valleys in units of m_0. Also shown is the total population of the different sets of valleys in the center of the device for nanowires with different diameters and $V_G = 0.5\,V$, $V_D = 50\,mV$; here the number besides each symbol denotes the nanowire diameter in nm.

a relatively low average value of m_z.

On the other hand, for ⟨110⟩ nanowires, quantum confinement splits the six degenerate valleys into a set of four-fold degenerate Δ_{xz} valleys with m_l forming an angle of 45° with the z axis (the transport direction) and two-fold degenerate Δ_y valleys with m_l in the confinement plane. In this case, the fundamental subbands correspond to Δ_y valleys because of their larger in-plane mass. However, the larger population in each of those Δ_y valleys do not always generate an overall larger population given the larger multiplicity of Δ_{xz} valleys. Indeed, in Figure 8 we can see that the overall population of Δ_y valleys is smaller than that of Δ_{xz} valleys for nanowires with $D = 6\,nm$ and $D = 8\,nm$ and only larger for the narrowest device with $D = 4\,nm$, where confinement is stronger and the subband energy difference prevails. For different bias conditions, the exact values of the valley population differ from those in Figure 8, but the weighted average of m_z is always larger than the one obtained for ⟨100⟩ devices, as shown in Figure 7.

We now turn to the spatial charge distribution in a cross section in the middle of

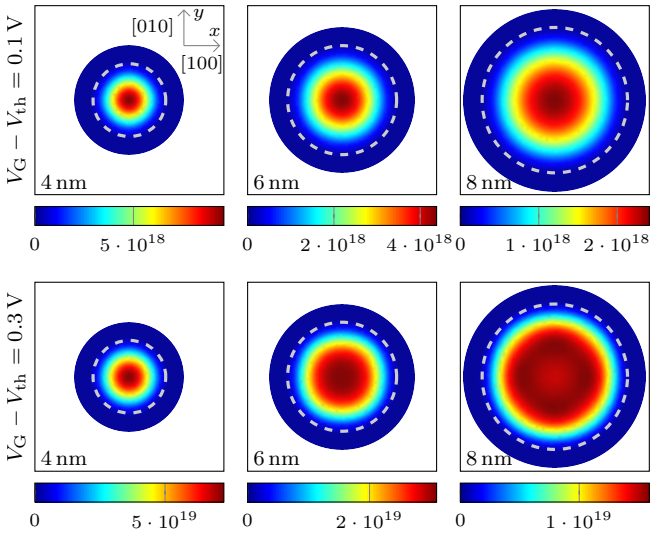

Figure 9: Inversion charge distribution in ⟨100⟩ devices with either $V_G - V_{th} = 0.1$ V or $V_G - V_{th} = 0.3$ V and $V_D = 50$ mV. The dashed line indicates the Si/SiO_2 interface. Units of electron density are cm^{-3}.

the channel. To perform a fair comparison, we plot the electron distribution in different devices with the same values of overdrive voltage $V_G - V_{th}$. These are shown in Figures 9 and 10 for ⟨100⟩ and ⟨110⟩ orientations, respectively. We can see that in ⟨100⟩ devices the inversion charge is distributed symmetrically. The peak of the distribution corresponds to the geometrical center of the cross section in most of the depicted cases. Only for the larger values of V_G and the widest D, the inversion charge moves towards the surrounding gate insulator and four peaks appear along [100] and [010] directions, as can be seen in the bottom right of Figure 9 for $V_G - V_{th} = 0.3$ V and $D = 8$ nm. On the contrary, Figure 10 shows in-plane asymmetry for ⟨110⟩ devices. In the nanowire with $D = 4$ nm (Fig. 10, left), charge distribution extends slightly more in the $[10\bar{1}]$ direction (horizontal in the figure) than in the [010] direction (vertical), while for larger diameters this shape is reversed. As in the case of ⟨100⟩ channel, there is a single peak of charge located at the center of the cross section except for the widest device, $D = 8$ nm, and for large overdrive voltage, $V_g - V_{th} = 0.3$ V (Fig. 10, bottom right), when two main peaks in the [010] direction appear.

The previously observed asymmetry can be quantified by computing the variance

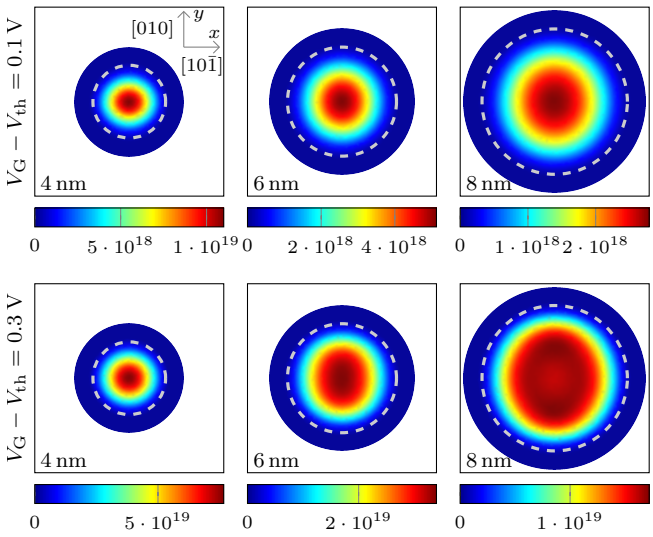

Figure 10: Inversion charge distribution in ⟨110⟩ devices with either $V_G - V_{th} = 0.1$ V or $V_G - V_{th} = 0.3$ V and $V_D = 50$ mV. The dashed line indicates the Si/SiO_2 interface. Units of electron density are cm^{-3}.

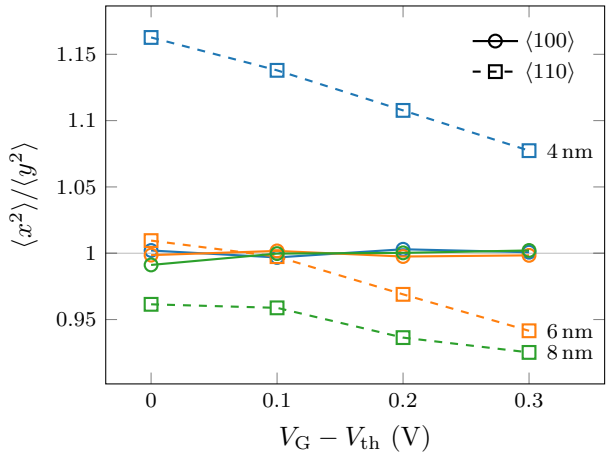

Figure 11: Ratio between the weighted average of x^2 and the weighted average of y^2, where the weight is given by the 2D charge distribution. The x direction is ([100] for ⟨100⟩ channel and [10$\bar{1}$] for ⟨110⟩ channel; the y direction is [010] for both channel orientations.

of the charge distribution in the horizontal, x, direction ([100] for $\langle 100 \rangle$ channels and $[10\bar{1}]$ for $\langle 110 \rangle$ channels) and the vertical, y, direction ([010] for both channel orientations). The ratio of these quantities, $\langle x^2 \rangle / \langle y^2 \rangle$, is shown in Fig. 11. Such ratio is equal to one, up to the numerical accuracy, for $\langle 100 \rangle$ devices. Turning to $\langle 110 \rangle$ devices, we can observe that the ratio is larger than unity for $D = 4\,\mathrm{nm}$, indicating a greater extension in the horizontal direction, while it is smaller than unity for $D = 6\,\mathrm{nm}$ and $D = 8\,\mathrm{nm}$, indicating a greater extension in the vertical direction.

The shape of the electron distribution in the different devices can be explained by taking into account the splitting of the six conduction band valleys. For $\langle 100 \rangle$ devices, the Δ_x and Δ_y valleys give rise to subbands with the same energy; the corresponding wave-functions are equivalent but rotated by 90 degrees in the cross section plane. The other valleys, Δ_z, possess an in-plane isotropic mass: therefore, the corresponding charge distribution is also isotropic. Thus, the cumulative charge density is symmetric for rotations of 90 degrees in the plane, because the contribution of Δ_z is isotropic and those of Δ_x and Δ_y are symmetrically placed. On the other hand, for $\langle 110 \rangle$ nanowires both Δ_y and Δ_{xz} valleys present an asymmetric charge distribution with different shapes: the former elongated along the horizontal direction ($[10\bar{1}]$) and the latter more extended in the vertical direction ([010]). Therefore, the total charge distribution will depend on the relative population of the different valleys, as shown in Fig. 8. For $D = 4\,\mathrm{nm}$, the doubly degenerate Δ_y valleys are the most populated ones, and the total charge distribution presents an horizontal shape. For $D = 6\,\mathrm{nm}$ and $D = 8\,\mathrm{nm}$, instead, the fourfold degenerate Δ_{xz} valleys represent the larger contribution and the total charge distribution is elongated along the vertical axis.

While the charge distribution depends on channel orientation, the average distance of carriers from the nanowire axis is essentially the same, as depicted in Fig. 12. Here we represent the results of the average radius $r_{\mathrm{avg}} = \sqrt{\langle r^2 \rangle} = \sqrt{\langle x^2 \rangle + \langle y^2 \rangle}$ weighted by the local 2D charge density as shown in Figures 9 and 10. It can be observed that r_{avg} depends slightly on the applied bias and notably on the nanowire diameter, but not on its orientation. It means that, for a given diameter, the average distance between the charge and the Si/SiO_2 interface does not depend on the nanowire orientation and therefore we can assume that the component of the capacitance due to the spatial distribution

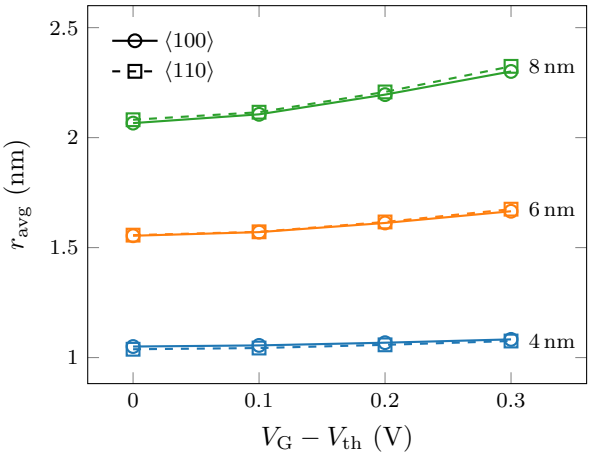

Figure 12: Average distance of the charge from the center of the cross section, measured as the square root of the weighted average of $x^2 + y^2$ where the weight is given by the 2D charge distribution, as a function of overdrive voltage.

of the inversion charge is the same for ⟨100⟩ and ⟨110⟩ devices. This result explains the behavior depicted in Figure 3, the linear inversion charge in the channel does not depend on the nanowire orientation.

Finally, we look at the scaling behavior of the GAA FETs, and especially its dependence on channel orientation. To do that, we consider nanowires with the same diameter as before but with the channel length, L_{G} reduced down to 8 nm. For all devices, we computed the transfer characteristics at low and high drain voltages ($V_{\mathrm{D}} = 50\,\mathrm{mV}$ and $V_{\mathrm{D}} = 0.5\,\mathrm{V}$, respectively) and we extracted the threshold voltages, shown in Figure 13 as a function of L_{G}. For both ⟨100⟩ and ⟨110⟩ orientations the results are quite similar: as the nanowire diameter is decreased, V_{th} increases due to the quantum confinement effect, both for low and high drain bias. At the same time, V_{th} roll-off is observed, *i. e.* the threshold voltage decreases for shorter values of L_{G}. Narrower devices are more immune to such roll-off: for example, considering $V_{\mathrm{D}} = 50\,\mathrm{mV}$, for $D = 4\,\mathrm{nm}$ a variation of the threshold voltage lower than 10 mV is observed between $L_{\mathrm{G}} = 8\,\mathrm{nm}$ and $L_{\mathrm{G}} = 14\,\mathrm{nm}$, while for $D = 8\,\mathrm{nm}$ a value of $\Delta V_{\mathrm{th}} \sim 65\,\mathrm{mV}$ can be estimated in the same L_{G} range. In any case, the behavior of ⟨100⟩ and ⟨110⟩ devices is very similar, with slightly larger values of V_{th} for ⟨110⟩ nanowires.

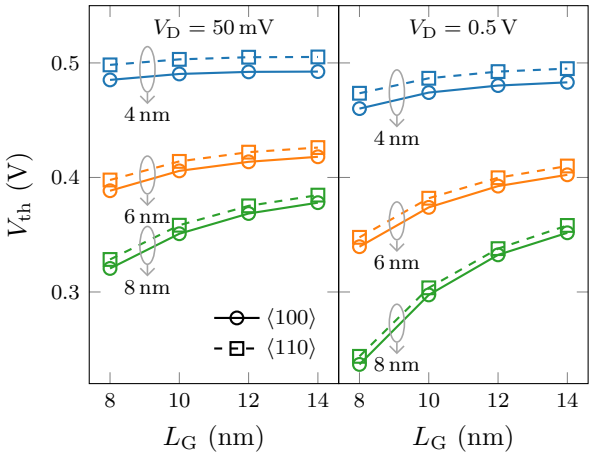

Figure 13: Threshold voltage, computed for different nanowire diameters and orientations, for low and high drain biases, as a function of gate length L_G.

Next, for each device we compute the Drain Induced Barrier Lowering (DIBL) as $(V_{th,1} - V_{th,2})/(V_{D,2} - V_{D,1})$, where $V_{th,1}$ and $V_{th,2}$ are the previously computed values of threshold voltage corresponding to drain voltages $V_{D,1} = 50\,mV$ and $V_{D,2} = 0.5\,V$, respectively. The values of DIBL, shown in Fig. 14, are again slightly larger in the case of ⟨110⟩ devices with respect to ⟨100⟩ ones, but only by a negligible amount. In both cases, if we choose a reference value of 100 mV/V for the DIBL, at $L_G = 10\,nm$ the devices with $D = 4\,nm$ and $D = 6\,nm$ are within the chosen limit, while at $L_G = 8\,nm$ only the ones with $D = 4\,nm$ fulfill the requirement.

4. Conclusions

We compared, through simulations, the performance of GAA n-MOSFETs where the channel is constituted by a cylindrical Si nanowire in either ⟨100⟩ or ⟨110⟩ orientation. The calculations were carried out using our Multi-Subband Ensemble Monte Carlo simulator, which fully captures the quantum properties in the confinement direction including the different valley orientations. Our main conclusion is that ⟨100⟩ devices possess better transport properties: velocity inside the channel, electron mobility and, consequently, drain current are consistently larger than for ⟨110⟩ channels,

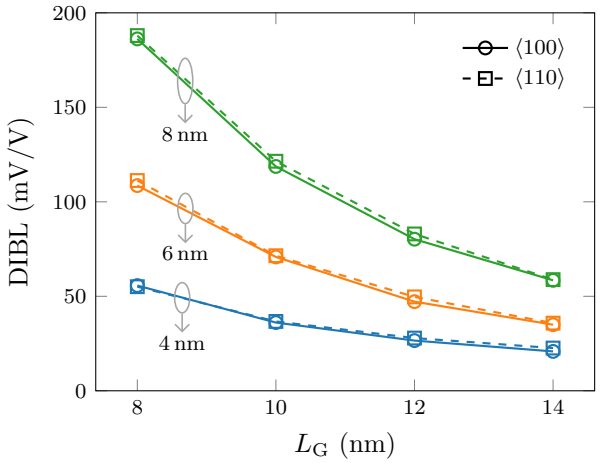

Figure 14: DIBL computed for different nanowire diameters and orientations, as a function of gate length L_G.

although not by a large amount. On the contrary, electrostatic behavior is essentially the same for both orientations. This fact is supported by several results: the linear charge density in the middle of the channel, the average radius of electron distribution in the cross section and the scaling behavior only present negligible differences.

We can conclude that narrow GAA FETs with ⟨100⟩ channel can provide larger currents and improved performance. However, if co-integration with bulk devices or FinFET is required so that ⟨110⟩ direction is preferred, the performance loss is moderate and the scaling behavior is essentially the same.

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