Simulation of 2D semiconductor based MOSFETs

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1. Abstract

In this work we address the simulation of 2D materials based Field Effect Transistors advancing a simple method to take into account the Density of States of arbitrary materials in a Drift-Diffusion transport scheme.

2. Introduction

Two-dimensional materials (2DM) have awakened a noticeable interest in the field of nanoelectronics, as they exhibit auspicious properties to overcome the problems associated with the continuous downscaling of MOSFET devices [1, 2]. Many experimental works have already demonstrated working 2DM based FETs (2DMFETs); however, the theoretical support is needed to select the best options amongst the extensive range of materials. In this context, modeling and simulation are fundamental to quantitatively asses their operation. In the diffusive regime where, given the current experimental dimensions, these devices are operating, there is a lack of simulation studies and most of research works consist of simplified compact models [3, 4]. This work is intended to contribute to fill the gap of numerical simulation of 2DM-based devices in the diffusive regime.

3. Methods

A semi-classical approach has been adopted for the simulation of 2DMFETs. The electrostatics are governed by the 2D Poisson equation that determines the potential in the structure, V:

$$\nabla(\varepsilon\,(\nabla V)) = -\rho \qquad (1)$$

where ε is the dielectric constant and ρ the charge density. The value of ρ in the semiconductor is obtained using the 1D Drift-Diffusion transport model:

$$J_n = \mu n \frac{dV}{dx} - D_n \frac{dn}{dx}, \quad \nabla J_n = 0 \qquad (2)$$

where k_B is the Boltzmann constant, T the temperature in Kelvins, q the electron charge, μ the carrier mobility, D_n the diffusion coefficient which is connected to the mobility through Einstein's relation and n the electron concentration. In equilibrium conditions, the charge density is evaluated using the general expression where the material DoS is included:

$$n(V) = \int_0^{\infty} d\tilde{E}\; D(\tilde{E}) \left(1 + exp\left(\frac{\tilde{E} - qV}{k_B T}\right)\right)^{-1} \qquad (3)$$

where $\tilde{E} = E - E_C$ and the potential is defined as $V = (E_F - E_C)/q$. Out of equilibrium the Drift-Diffusion transport equation is used and the charge boundary conditions are defined by Eq. (3). Once the longitudinal charge profile is obtained, it is distributed in the layer thickness using a fixed sinusoidal profile with a maximum at the centre of the thin semiconductor region.

4. Results

This scheme was used to simulate a Double Gate (DG) monolayer MoS_2 MOSFET. The structure is depicted in Fig.1 and the parameters used to characterize it are gathered in Table 1. The source and drain are doped with donors, fixing the carrier injection into the channel to n-type. The transfer and output characteristics of the device are depicted in Fig.2 and Fig.3 respectively. The effect of the emulated contact resistances is observed in the longitudinal potential profile (Fig.4). Since the doping concentration at the source and drain is not high enough, the gate voltages compete for the charge control, and contrary to a conventional bulk scenario the bands at these regions are no longer flat (V_{GS}=1V). The cross section potential in the centre of the channel is shown in Fig.5. Note the change in the potential distribution in the semiconductor region when the conducting channel is formed: the charge screens the gate field lines and the potential at the centre of the channel does not varies linearly with the gate voltage. The channel generation can be better observed in Fig.6. For V_{FG}=0.2V the channel is not created and the potential roughly changes in the channel region. When V_{FG} is increased to 0.6V the channel has been created and the potential is modified in the region where the semiconductor is located. The channel generation is reproduced correctly, even the pinch-off that causes the reduction of the charge density near the drain region.

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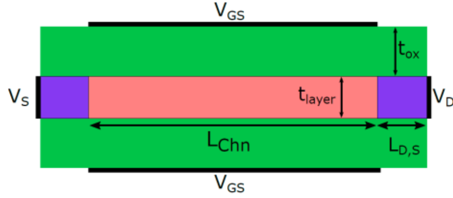

Fig.1. Structure of the monolayer DG simulated. Geometrical and material parameters are gathered in Table 1

Parameter	Value
L_{Chn} / $L_{D,S}$	500 nm / 200nm
t_{layer} / t_{Ox}	0.65 nm / 1nm
$N_{d,\,Chn}$	$3.5\cdot10^{11}$ cm^{-2}
$N_{d,\,D,S}$	$6.5\cdot10^{12}$ cm^{-2}
ε_{MoS_2}	$4.8\varepsilon_0$
μ_{MoS_2}	50 cm^2/Vs
χ_{MoS_2}	4.3 eV
ϕ_{Gate} / $\phi_{D,S}$	4.75eV / 4.3eV

Table 1. Parameters used in the simulation of the double gate MoS_2 MOSFET device.

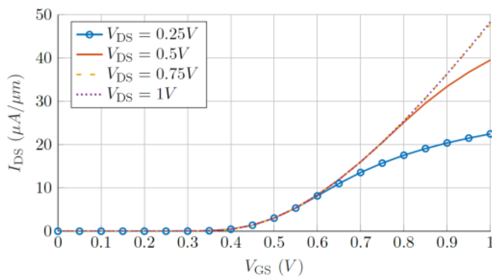

Fig.2. Transference response of the device for different V_{DS} values. Note the saturated trend of the curve for $V_{DS} = 0.25V$ due to the doped regions added in the sides of the channel.

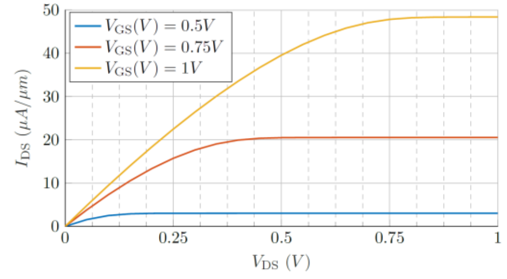

Fig.3. Output response of the device for different gate biases.

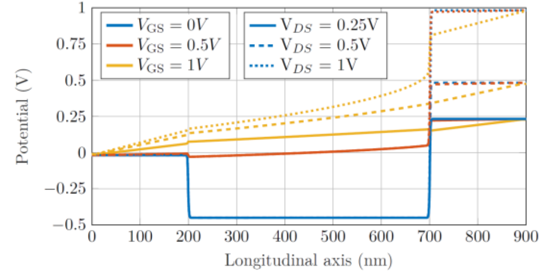

Fig.4. Longitudinal potential profile in the center of the semiconductor layer (from source to drain) for different gate bias.

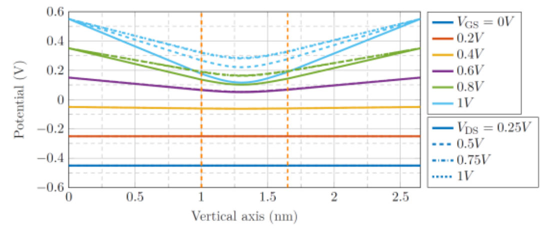

Fig.5. Cross section potential profile in the center of the channel as a function of the position.

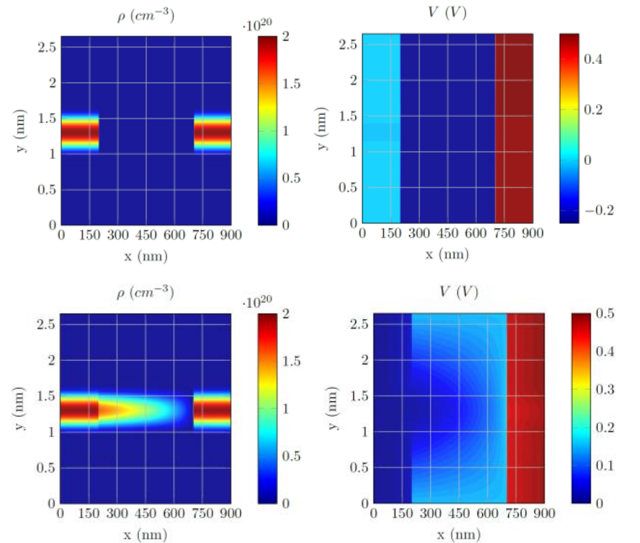

Fig.6. 2D plot of the charge density (left) and potential (right) in the device for $V_{GS} = 0.2V$ (up) and $V_{GS} = 0.6V$ (down). In both cases $V_{DS} = 0.5V$.