UNIVERSITY OF GRANADA

DOCTORAL THESIS

Distributed control systems based on high accurate timing synchronization

Author:
Miguel Jiménez López

Supervisor:
Dr. Antonio Javier Díaz Alonso

A thesis submitted in fulfillment of the requirements for the PhD Degree in the

PhD Program in Information and Communication Technologies of the University of Granada

Department of Computer Architecture and Technology

UNIVERSIDAD DE GRANADA

December 19, 2018

Editor: Universidad de Granada. Tesis Doctorales
Autor: Miguel Jiménez López
ISBN: 978-84-1306-114-6
URI: http://hdl.handle.net/10481/54816

Resumen

Esta tesis se centra en las tecnologías de sincronización de alta precisión y su utilización en diferentes tipos de aplicaciones desde las instalaciones científicas hasta las infraestructuras industriales. Este trabajo describe el desarrollo de sistemas que incluyen dispositivos System-on-Chip (SoC) de nueva generación que combinan capacidades de alto ancho de banda con protocolos de sincronización de alta precisión sobre la misma red.

En las secciones iniciales, se presenta una revisión completa del estado del arte en relación con las técnicas de sincronización temporal considerando sus ventajas y desventajas. Algunas de ellas están basadas en señales de referencia de tiempo como las señales de ondas cuadradas o sinusoidales de 10 MHz o las de 1 pulso por segundo (PPS). Otras alternativas despliegan un sistema global de navegación por satélite (GNSS) con múltiples receptores sincronizando los elementos de la red a los relojes atómicos de los satélites (en este caso utilizando señales de baja energía por enlaces inalámbricos). En contraste con las soluciones que incluyen señales de referencia de tiempo, existen protocolos basados en paquetes estándares como el protocolo de tiempo en red (NTP) o el protocolo de tiempo preciso (PTP) que se utilizan de forma habitual para distribución de tiempo y sincronización en redes con tecnología Ethernet. Sin embargo, la precisión de estas soluciones está limitada a la escala de los milisegundos y microsegundos respectivamente. Adicionalmente, existen soluciones metrológicas que pueden proporcionar precisiones de hasta unos pocos picosegundos, pero estas requieren equipos muy específicos y caros y no pueden ser fácilmente adaptadas para su uso en muchas aplicaciones. En este contexto, se ha propuesto una nueva solución estándar basada en paquetes para mejorar significativamente la precisión de la sincronización en la aproximación basada en paquetes: La tecnología White Rabbit (WR). Esta se basa en la segunda versión del PTP e incluye algunas mejoras para alcanzar una precisión en la sincronización temporal sub-nanosegundo con una estabilidad de pocos picosegundos.

Posteriormente, se ha realizado el diseño y desarrollo de una nueva familia de dispositivos para sistemas WR basados en dispositivos SoC programables de nueva generación en un marco de estrecha colaboración con la industria. Esta plataforma implementa un nodo WR mejorado aprovechando la precisión de sincronización que aporta WR y, al mismo tiempo, ofreciendo características software avanzadas. Debido a la bondad de esta solución, ha sido propuesta para ser utilizada en la Matriz de Telescopios de Kilómetro Cuadrado (SKA), concretamente para su sistema de distribución de PPS. Además del desarrollo, se han realizado algunas pruebas para caracterizar el sistema en términos de precisión de la sincronización, escalabilidad y los efectos en el mismo debido a las variaciones de temperatura. Dichos resultados garantizan que el sistema propuesto cumple las necesidades de SKA.

Además del tema relacionado con la sincronización temporal, se han estudiado las redes de alto ancho de banda de datos y, especialmente, su aplicación a sistemas de adquisición de datos (DACQ). Estos están normalmente compuestos de muchos sensores distribuidos que generan datos que son generalmente procesados en un servidor central. En consecuencia, se deben implementar mecanismos de agregación de datos para unir distintas conexiones de red provenientes de los sensores en un solo canal para alcanzar el servidor central. Por otra parte, los sistemas de DACQ también requieren un canal de comunicación completamente configurable y flexible entre el servidor central y los sensores para tareas de control y monitorización. Estos requisitos son muy específicos para las redes convencionales de alto ancho de banda que no pueden ser utilizadas de forma satisfactoria para muchos de los sistemas de

DACQ. En este contexto, se ha propuesto una nueva y genérica arquitectura de red asimétrica para solventar este problema proporcionando capacidades de agregación y enrutado. Gracias a la flexibilidad y el diseño optimizado de esta solución, ha sido seleccionada para su utilización en la infraestructura de Matriz de telescopios Cherenkov (CTA), concretamente en la cámara compacta de alta energía (CHEC). En este contexto, se han realizado distintas pruebas para verificar que esta solución cumple los requisitos de CTA obteniendo unos resultados que los satisfacen de manera holgada. Además, la solución propuesta ha sido integrada satisfactoriamente en la CHEC en el Sincrotón de Electrones Alemán (DESY) en un marco colaborativo con una entidad participante en el proyecto CTA.

En colaboración con la industria, otra contribución importante de la tesis ha consistido en la actualización de la tecnología WR para trabajar con redes de alto ancho de banda como las basadas en 10 Gigabit Ethernet (10G). Este desarrollo es necesario para solventar las limitaciones de WR en relación con el ancho de banda de datos y la interoperabilidad, permitiendo su utilización en otras aplicaciones en las que hasta ahora no era una opción posible como sistema de sincronización temporal. A este respecto, se ha desarrollado una solución completamente modular teniendo en cuenta los conceptos aprendidos de los desarrollos basados en dispositivos SoC y el diseño basado en redes asimétricas dando como resultado una arquitectura unificada para datos y sincronización. Esta es capaz de proporcionar sincronización temporal de alta precisión junto con servicios de transferencia de datos de alto ancho de banda. Además, esta solución se ha validado obteniendo una precisión temporal comparable o incluso mejor en algunos aspectos que la presentada por los dispositivos estándar de WR. Adicionalmente, se ha realizado una caracterización del sistema midiendo el ancho de banda, la latencia y la interoperabilidad con dispositivos comerciales basados en 10G obteniendo resultados satisfactorios.

Finalmente es importante remarcar que por primera vez en la literatura, se ha presentado un sistema capaz de proporcionar unos mecanismos de sincronización de alta precisión y una distribución de datos 10G, evitando el despliegue de diferentes redes separadas para sincronización y transferencia de datos.

Abstract

This thesis is focused on high accurate timing synchronization technologies and their utilization in different kind of applications from scientific facilities to industrial infrastructures. The work describes the development of systems which include new generation System-on-Chip (SoC) devices combining high data bandwidth capabilities together with high accuracy timing synchronization protocols over the same network.

In the first sections, a full revision of the state of the art is presented in regards of timing synchronization technologies taking into consideration their advantages and drawbacks. Some of them are based on timing references as 10 MHz square/sine signals or 1 Pulse Per Second (PPS) ones. Other alternatives deploy a Global Navigation Satellite System (GNSS) with many receivers synchronizing elements in the network to the atomic clocks of the satellites (in this case using low energy satellite signals via wireless links). In contrast to those timing signal solutions, there are standard packet-based protocols as Network Time Protocol (NTP) or Precise Time Protocol (PTP) that are widely used for time transfer and synchronization through Ethernet-based networks. However, synchronization accuracy of these are limited to millisecond and microsecond scale respectively. Additionally, there are alternate metrology solutions, that can provide accuracies up to few picoseconds, but they require very specific and expensive equipment and they are not easily adapted to be used in many applications. Under this context, a new standard packet-based solution has been proposed to significantly improve time synchronization performance of the packet based approach: White Rabbit (WR) technology. It is based on Precise Time Protocol version 2 (PTPv2) but includes some enhancements to reach a time synchronization accuracy in the sub-nanosecond scale with a precision of picoseconds.

Then, the design and development of a new family of devices for WR systems based on new generation programmable SoC devices have been accomplished in partnership with industrial partners. This new platform implements an enhanced WR node taking advantage of WR synchronization performance and, at the same time, offering advanced software capabilities. These features have motivated its proposal as reference timing platform for Square Kilometer Array (SKA), concretely for the PPS distribution system. In addition to the development, some tests have been performed for characterizing the system in terms of timing performance, scalability and the effects derived from temperature variations. Such results guarantee that the proposed system fulfills the SKA needs.

Apart from the timing synchronization topic, high data bandwidth networks have been studied and, specially, its application in Data ACQuisition (DACQ) systems. They are usually composed of many distributed sensors which generate data that are typically processed by a central server. Consequently, data aggregation mechanisms must be implemented to join several network connections from sensors to a single channel in order to reach the central server. On the other hand, DACQ systems also require a fully configurable and flexible routing communication channel between the central server and sensors for control/monitor tasks. These requirements are very specific for conventional high data bandwidth networks that can not be applied successfully for many DACQ systems. In this regard, a novel and generic asymmetric network architecture has been proposed to overcome this issue providing aggregation and routing capabilities. Due to the flexiblity and optimized design of this solution, it has been selected to be used in the Cherenkov Telescope Array (CTA) infrastructure, concretely inside the Compact High Energy

Camera (CHEC). In this scenario, several tests have been performed to verify that this solution fulfills the CTA requirements obtaining results that outperform them. Furthermore, the proposed solution has been integrated properly in the CHEC at Deutsches Elektronen-Synchrotron (DESY) in a collaborative framework with a CTA partner.

In collaboration with an industrial partner, other important thesis contribution has consisted on the update of the WR technology to work with high data bandwidth networks as 10 Gigabit Ethernet (10G) ones. This development is required in order to overcome WR limitations in terms of data bandwidth and interoperability, enabling its utilization in other applications in which it has not been a feasible option for the timing synchronization system up to now. In this regard, a fully modular solution has been developed taking into consideration the learned concepts from the SoC developments and the asymmetric network design given as a result an unified architecture for data and synchronization purposes. This is able to provide high accurate timing synchronization together with high data bandwidth transfer services. Moreover, this solution has been validated obtaining a timing performance comparable or even better in some aspects than standard WR devices. Additionally, a system characterization has been performed measuring the data bandwidth, latency and the interoperability with commercial 10G devices obtaining satisfactory results.

Finally, it is important to remark that for first time in the literature, a system able to provide high accurate timing synchronization and 10G data distribution has been presented, avoiding the deployment of different separated networks for data transfer and synchronization purposes.

Agradecimientos

Parece ayer cuando empecé la tesis cargado de ilusiones y ganas; con el afán de aprender y mejorar a cada paso, de formarme como ingeniero que siempre fue mi pasión y desde hace unos años, mi profesión. Esta aventura no ha sido fácil pero eso solo la ha hecho más interesante y divertida; con ratos frustrantes y otros estimulantes. Me gustaría empezar estos agradecimientos dando las gracias a mi familia por apoyarme durante todo este proceso y por nunca dejar de creer en mi. A Nuria por ser la mejor persona que se podría desear, mi mujer, aquella a la que amo. A mis padres por siempre creer en mí y nunca darme por perdido. A mi hermano por apoyarme en momentos complicados.

Gracias también a mis compañeros de laboratorio, por las tertulias, los cafés y los ratos pasados. En especial a José, Paco y Felipe por apoyarme siempre que lo he necesitado y contribuir todos juntos para hacer buena ciencia en forma de artículos.

No quiero olvidarme tampoco de mis amigos en la empresa de Seven Solutions, con una mención especial a Rafa que siempre apostó por mí. También quiero agradecer su ayuda a Emilio, Fidel, Benoit, Jorge Machado... y un sin fin de nombres. Gracias a todos.

Finalmente, a vosotros, mi director Javier Díaz, mi tutor Eduardo Ros y al profesor de mi grupo de investigación Manuel Rodríguez. Os agradezco la gran oportunidad que me habéis dado. Todo este proceso me ha hecho crecer como ingeniero y científico pero, sin duda, también como persona.

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Acronyms

100G 100 Gigabit Ethernet.

10G 10 Gigabit Ethernet.

25G 25 Gigabit Ethernet.

3G Third Generation.

40G 40 Gigabit Ethernet.

5G Fifth Generation.

ADC Analog-to-Digital Converter.

ADEV Allan DEViation.

ALICE A Large Ion Collider Experiment.

AMBA Advanced Reduced Instruction Set Computer Machines Advanced Microcontroller Bus Architecture.

AMIGA Analysis of the interstellar Medium of Isolated GAlaxies.

AMIGA5 Analysis of the interstellar Medium of Isolated GAlaxies 5.

AMIGA6 Analysis of the interstellar Medium of Isolated GAlaxies 6.

ARM Advanced Reduced Instruction Set Computer Machines.

ASIC Application Specific Circuit.

ASKAP Australian Square Kilometer Array Pathfinder.

ASTERICS Astronomy European Strategy Forum on Research Infrastructures & Research Infrastructure Cluster.

ATLAS A Toroidal Large Hadron Collider ApparatuS.

AVAR Allan VARiance.

AXI Advanced Extensible Interface.

AXIS Advanced Extensible Interface-Stream.

BC Boundary Clock.

BCD Binary-Coded Decimal.

BMC Best Master Clock.

BRAM Block Random Access Memory.

CAM Content Addressable Memory.

CERN European Organization for Nuclear Research.

CHEC Compact High Energy Camera.

CIEMAT Research Center for Energy, Environment and Technology.

CLK CLocK.

CLONETS CLOck NETwork Services.

CMS Compact Muon Solenoid.

CPU Central Processing Unit.

CRTT Cable Round Trip Time.

CSMA/CD Carrier-Sensing Multiple-Access with Collision Detection.

CSP Central Signal Processor.

CTA Cherenkov Telescope Array.

CTAO Cherenkov Telescope Array Observatory.

DAC Digital-to-Analog Converter.

DACQ Data ACQuisition.

DDMTD Digital Dual Mixer Time Difference.

DDR Double Data Rate.

DE DElaware.

DEMO DEMOnstration fusion reactor.

DESY Deutsches Elektronen-Synchrotron.

DIO Digital Input-Output.

DMA Direct Memory Access.

DMTD Dual Mixer Time Difference.

DONES DEMOnstration fusion reactor Oriented Neutron Source.

DTP Datacenter Time Protocol.

DUT Device Under Test.

EGNOS European Geostationary Navigation Overlay Service.

ELT Extremely Large Telescope.

ESFRI European Strategy Forum on Research Infrastructures.

EU European Union.

EVEDA Engineering Validation and Engineering Design Activities.

EVN European Very Long Baseline Interferometry Network.

FAIR Facility for Antiproton and Ion Research.

FEE Front-end Electronic.

FF Flip Flop.

FIFO First In-First Out.

FMC Field Programmable Gate Array Mezzanine Card.

FPGA Field Programmable Gate Array.

GbE Gigabit Ethernet.

GCT Gamma-ray Cherenkov Telescope.

GLONASS Global'naya Navigatsionnaya Sputnikovaya Sistema.

GM Grand-master.

GNSS Global Navigation Satellite System.

GPS Global Positioning System.

GSI Helmholtz Centre for Heavy Ion Research.

GT Gigabit Transceiver.

H2020 Horizon 2020.

HAL Hardware Abstraction Layer.

HDL Hardware Description Language.

HEP High-Energy Physics.

HESS High Energy Stereoscopic System.

HFT High Frequency Trading.

I2C Inter-Integrated Circuit.

IACT Imaging Atmospheric Cherenkov Technique.

ICAO International Civil Aviation Organization.

IDE Integrated Development Environment.

IEEE Institute of Electrical and Electronics Engineers.

IFMIF International Fusion Material Irradiation Facility.

IIoT Industrial Internet of Things.

ILA Integrated Logic Analyzer.

INRIM National Institute of Metrological Research.

IoT Internet of Things.

IP Intellectual Property.

IRIG Inter-Range Instrumentation Group.

IRIG-B Inter-Range Instrumentation Group time code B.

IT Information Technology.

ITER International Thermonuclear Experimental Reactor.

ITU International Telecommunication Union.

ITU-T International Telecommunication Union Telecommunication Standardization Sector.

JIVE Joint Institute for Very Long Baseline Interferometry in Europe.

JTAG Joint Test Action Group.

KM3Net Kilometre Cube Neutrino Telescope.

L1 Layer 1.

LAN Local Area Network.

LED Light-Emitting Diode.

LHAASO Large High Altitude Air Shower Observatory.

LHC Large Hadron Collider.

LHCb Large Hadron Collider beauty.

LLC Logical Link Control.

LM32 LatticeMico32.

LNE-SYRTE National Laboratory of Metrology and Testing.

LOFAR Low Frequency ARray.

LST Large Size Telescope.

LTE Long Term Evolution.

LTE-A Long Term Evolution Advanced.

LUT Look-up Table.

LUTRAM Look-up Table as Random Access Memory.

M2M Machine-to-Machine.

MAC Medium Access Control.

MAN Metropolitan Area Network.

MDEV Modified Allan DEViation.

MeerKAT Karoo Array Telescope.

MMCM Mixed-Mode Clock Manager.

MST Medium Size Telescope.

MTIE Maximum Time Interval Error.

NIC Network Interface Core.

NIKHEF Dutch National Institute for Subatomic Physics.

NIST National Institute of Standards and Technology.

NLP National Physical Laboratory.

NTP Network Time Protocol.

OC Ordinary Clock.

OCXO Oven-Controlled Crystal Oscillator.

OHWR Open HardWare Repository.

OS Operating System.

PC Personal Computer.

PCI Peripheral Component Interconnect.

PCIe Peripheral Component Interconnect Express.

PCS Physical Coding Sublayer.

PHY PHYsical.

PI Proportional Integral.

PLL Phase-Locked Loop.

PM Phase Modulation.

PMA Physical Medium Attachment.

PMD Physical Medium Dependent.

PMR Professional Mobile Radio.

PMU Phasor Measurement Unit.

PPS Pulse Per Second.

PRC Primary Reference Clock.

PTP Precise Time Protocol.

PTPv2 Precise Time Protocol version 2.

RAM Random Access Memory.

RISC Reduced Instruction Set Computer.

RJ45 Registered Jack-45.

RMS Root Mean Square.

RS Reconciliation Sublayer.

RTL Register Transfer Level.

RTS Real Time Subsystem.

RTU Routing Table Unit.

SaDT Signal and Data Transport.

SAT Synchronization and Timing.

SDH Synchronous Digital Hierarchy.

SerDes Serializer-Deserializer.

SFP Small Form-factor Pluggable transceptor.

SKA Square Kilometer Array.

SMA SubMiniature version A.

SME Small and Medium-sized Enterprises.

SoA State-of-the-Art.

SoC System-on-Chip.

SONET Synchronous Optical NETwork.

SPEC Simple Peripheral Component Interconnect Express Field Programmable Gate Array Mezzanine Card carrier.

SPI Serial Peripheral Interface.

SSM Synchronization Status Message.

SST Small Size Telescope.

SVM Support Vector Machine.

SyncE Synchronous Ethernet.

TAI International Atomic Time.

TARGET TeV Array Readout Electronics with GSa/s sampling and Event Trigger.

TC Transparent Clock.

TDEV Time DEViation.

TLV Type, Length, Value.

ToD Time of Day.

TSN Time Sensitive Network.

TSU TimeStamping Unit.

TWSTFT Two-Way Satellite Time and Frequency Transfer.

TxTSU Transmission TimeStamping Unit.

UART Universal Asynchronous Receiver-Transmitter.

UAV Unmanned Aerial Vehicle.

UCTS Uniform Clock and Trigger time Stamping.

UDP User Datagram Protocol.

UGR University of Granada.

USA United States of America.

USB Universal Serial Bus.

UTC Coordinated Universal Time.

UVA University of Amsterdam.

VHDL Very High Speed Integrated Circuit Hardware Description Language.

VHSIC Very High Speed Integrated Circuit.

VLBI Very Long Baseline Interferometry.

VLT Very Large Telescope.

VSL Dutch National Metrology.

VTT MIKES National Metrology Institute of Finland.

WAN Wide Area Network.

WB WishBone.

WIS Wide Area Network Interface Sublayer.

WR White Rabbit.

WR-LEN White Rabbit Lite Embedded Node.

WR-PTP White Rabbit Precise Time Protocol.

WR-Z16 White Rabbit Zynq 16 ports.

WR-ZEN White Rabbit Zynq Embedded Node.

WRITE Precision Time for Industry.

WRPC White Rabbit Precise Time Protocol Core.

WRPC-2p White Rabbit Precise Time Protocol Core Dual Port.

WRS White Rabbit Switch.

WWDM Wide-Wavelength Division Multiplexing.

XDACQ eXtended Data ACQuisition.

Dedicado a mi familia, gracias por nunca dejar de creer en mí. . .

Chapter 1

Introduction

"Engineers like to solve problems. If there are no problems handily available, they will create their own problems."

– Scott Adams

Introduction (Spanish and English versions)

1.1 Introducción

El primer capítulo está dedicado a proporcionar una visión global del ámbito y el marco de proyectos para esta tesis.

Este capítulo se organiza en seis secciones. La sección 1.1.1 presenta el contexto general del tema principal abordado en la tesis: la sincronización temporal. La sección 1.1.2 describe las necesidades actuales para muchas aplicaciones en relación a la sincronización temporal. Además, introduce la tecnología White Rabbit (WR) teniendo en cuenta su motivación, las aplicaciones objetivo, el estado presente y sus perspectivas futuras. La sección 1.1.3 enumera los diferentes objetivos científicos propuestos para la tesis. La sección 1.1.4 define los proyectos nacionales e internacionales en los que se ha contribuido a través del trabajo de la tesis. La sección 1.1.5 expone los métodos y herramientas utilizados durante el periodo de la tesis. Finalmente, la sección 1.1.6 describe la organización en capítulos de la presente tesis.

1.1.1 Vista general

Hasta la última parte del siglo XVIII, el tiempo se determinaba normalmente en cada ciudad gracias a un reloj de sol local, lo que daba como resultado que cada ciudad tuviera su propio concepto de tiempo. Con la llegada y la expansión del sistema de tren en el siglo XIX, surgió una creciente necesidad de gestionar los horarios de los trenes. Se implementaron zonas horarias estandarizadas, así como medios para sincronizar la hora en estas zonas a través del sistema del telégrafo. Ya en el siglo XXI se produjo un avance rápido a la era moderna de la tecnología de la información: el protocolo de tiempo en red (NTP). Éste fue desarrollado para tener medios estandarizados de sincronización temporal entre dispositivos de red a través de redes locales y de área amplia con una precisión inferior al milisegundo. Para cuando las aplicaciones requerían un mejor rendimiento de sincronización, se desarrolló el protocolo de tiempo preciso (PTP) que consiguió reducirlo al microsegundo. El desarrollo de protocolos de sincronización temporal y la implementación del sistema global de navegación por satélite (GNSS) ha impulsado un mercado global de 1,2 billones de euros para soluciones de distribución de tiempo en 2016 [1], incluido el sistema global de posicionamiento (GPS) para transportar y transferir señales de tiempo a dispositivos y aplicaciones dispares que requieran una gran precisión temporal.

En este contexto, la sincronización temporal es uno de los factores más importantes en muchas aplicaciones donde varios dispositivos deben cooperar entre sí para cumplir un objetivo específico. Algunos ejemplos importantes se pueden encontrar en infraestructuras científicas como aceleradores de partículas, p.e. el Gran Collisonador de Hadrones (LHC) en la Organización Europea para la Investigación Nuclear (CERN) y la Instalación para la Investigación de Antiprotones e Iones (FAIR) en el Centro Helmholtz para la Investigación de Iones Pesados (GSI) y las instalaciones de astrofísica como la Matriz de Telescopios de Kilómetro Cuadrado (SKA) o la Matriz de telescopios Cherenkov (CTA). Además las aplicaciones industriales como redes de telecomunicaciones, redes eléctricas inteligentes, infraestructuras financieras o sistemas del internet de las cosas (IoT) también tienen requisitos de tiempo estrictos que solo pueden cumplirse mediante técnicas avanzadas de sincronización temporal. En todos estos sistemas, cada dispositivo tiene su propio reloj con una noción de tiempo concreta y posiblemente diferente. Un reloj está compuesto por un oscilador y un contador. El primero produce una señal específica con una frecuencia concreta y determina la granularidad del reloj porque el intervalo de tiempo mínimo que se puede medir es el período del oscilador. El segundo almacena el número de transiciones del oscilador desde un instante o época específica. Debido a la existencia de muchos relojes en el sistema, el primer paso es ajustarlos para que coincidan con la misma frecuencia en diferentes ubicaciones. Se conoce como sincronización de frecuencia o simplemente sintonización y garantiza que cada dispositivo cuente el tiempo con la misma frecuencia. Además, diferentes osciladores pueden funcionar a la misma frecuencia pero con una diferencia de fase específica que debe corregirse utilizando técnicas de alineamiento de fase. Para realizar una sincronización de tiempo completa, se requiere un ajuste adicional para que todos los contadores asociados a los relojes coincidan. En caso de no utilizar un método de sincronización temporal para el sistema, los relojes comenzarán a diferir después de un período de tiempo debido a la desviación del reloj.

En la actualidad existen diferentes mecanismos para proporcionar sincronización

temporal cada uno con sus propias características. Algunos utilizan señales de temporización, mientras que otros implementan redes donde se utilizan protocolos estándares basados en paquetes. Normalmente, en el enfoque basado en la red, se implementan diferentes redes con fines de sincronización y distribución de datos. Con esta configuración, el coste del sistema se incrementa al mismo tiempo que los recursos de hardware requeridos: fibras ópticas, transceptores ópto-eléctricos (SFPs), tarjetas de interfaz de red, etc. En este escenario, la tesis tiene como objetivo principal estudiar las tecnologías de sincronización y redes de alto ancho de banda con el fin de elaborar una solución de red unificada donde la información de sincronización y los datos puedan viajar usando el mismo medio.

El primer paso consiste en revisar las técnicas de sincronización para seleccionar la más adecuada, considerando el rendimiento de la tecnología de sincronización como factor clave. Durante este proceso, se han revisado muchas alternativas, incluyendo protocolos estándar basados en paquetes como NTP, PTP o WR. WR es un protocolo de sincronización temporal de alta precisión basado en la tecnología de Gigabit Ethernet (GbE) que puede alcanzar una precisión por debajo del nanosegundo con una estabilidad en el rango de los picosegundos. Sin embargo, la tecnología WR presenta algunas limitaciones que impiden su uso en algunas aplicaciones, como las redes de telecomunicaciones. Estos están relacionados con los requisitos de ancho de banda de datos, tecnología de la capa física, robustez, redundancia y escalabilidad en largas distancias de enlace. Los dos primeros problemas se refieren al hecho de que WR ha sido diseñado para funcionar en redes 1 GbE. Estas no pueden proporcionar suficiente ancho de banda de datos para muchas aplicaciones y su tecnología de capa física difiere de las alternativas de mayor ancho de banda como las basadas en 10 Gigabit Ethernet (10G). Por lo tanto, esta tesis incluye algunos desarrollos en esta línea con el fin de mejorar la tecnología WR habilitando su integración en las aplicaciones actuales y futuras que permiten la transferencia de tecnología del mundo científico a las soluciones industriales. Para este arduo trabajo, hemos utilizado técnicas de co-diseño hardware/software para el diseño digital y hemos trabajado con la última tecnología System-on-Chip (SoC) aprovechando su arquitectura híbrida compuesta por un dispositivo basado en una matriz de puertas programables (FPGA) y una unidad central de procesamiento (CPU). Estos dispositivos SoC de última tecnología han permitido la actualización de los dispositivos WR dotándoles de un mayor número de características. Al mismo tiempo, los han habilitado para poder utilizarse en aplicaciones en las que los antiguos diseños no cumplían los requisitos. Como prueba de concepto del nuevo diseño, se ha desarrollado el sistema de sincronización temporal para el proyecto SKA con resultados sorprendentes (consulte el capítulo 3). Además, se ha diseñado e implementado una nueva arquitectura de red asimétrica genérica para adquisición de datos (DACQ) que permite la utilización de enlaces de alto ancho de banda de datos como 10G (consulte el capítulo 4). Esta arquitectura de red asimétrica se ha evaluado en el proyecto CTA, lo que demuestra que la solución propuesta no solo muestra un buen rendimiento en términos de ancho de banda de datos, sino también una flexibilidad para integrarse en diferentes aplicaciones que requieren un sistema de DACQ. Finalmente, la capa física WR se ha adaptado para permitir su integración en las infraestructuras actuales con enlaces 10G. En esta línea, se ha diseñado una arquitectura unificada totalmente modular utilizando la implementación de red asimétrica para sistemas de DACQ y el nuevo desarrollo de WR con capacidades 10G (consulte el capítulo 5).

En resumen, el objetivo de la tesis es proporcionar una solución común para las redes de sincronización y de datos utilizando la tecnología WR. La hipótesis principal de esta tesis consiste en suponer que es posible enviar a través de la misma

red datos y patrones de sincronización de muy alta precisión de forma escalable, interoperable y confiable.

1.1.2 Motivación

WR es una tecnología de sincronización de alta precisión desarrollada por el CERN en colaboración con otros centros de investigación prestigiosos como GSI e importantes empresas como Siemens AG y National Instruments. WR se ha presentado en un marco de proyecto de código abierto con un repositorio público central conocido como repositorio de hardware abierto (OHWR). Con respecto al diseño de la tecnología WR, ha sido concebida para ser una plataforma modular y escalable que se re-configura automáticamente permitiendo mecanismos de monitorización/control entre miles de nodos con distancias de enlace de hasta decenas de kilómetros. Una característica importante de WR es su comportamiento determinista en la entrega de paquetes junto con su baja latencia. También puede incluir métodos proactivos para intercambiar mensajes importantes de manera robusta, teniendo en cuenta condiciones con fallos excepcionales. La tecnología WR se ha implementado como una extensión de la segunda versión del protocolo de tiempo preciso (PTPv2). PTPv2 define varias extensiones o perfiles que están orientados a ciertos sectores estratégicos, como la energía, las telecomunicaciones, la distribución de videos, etc. Permiten desarrollar una solución específica para cada aplicación centrada en sus requisitos. Actualmente, WR se está adaptando para convertirse en el nuevo perfil de alta precisión temporal de PTP. De esta forma, la estandarización de WR conlleva una gran ventaja para su integración en muchas aplicaciones industriales. La principal conclusión de este estudio es que la tecnología WR proporciona un rendimiento de sincronización en el rango por debajo del nanosegundo. Si bien es cierto que algunas tecnologías de sincronización temporal ad-hoc presentan un mejor rendimiento que WR, no son estándar y no pueden integrarse fácilmente en muchos sistemas. A la luz de todos los puntos establecidos anteriormente, WR es la mejor opción para el protocolo de sincronización temporal.

1.1.3 Objetivos científicos

Los objetivos científicos de la tesis se presentan a continuación:

[Obj-1] Diseño y desarrollo de una nueva familia de dispositivos junto a una metodología de diseño de sistemas WR basados en componentes SoC programables de última generación.

[Obj-2] Desarrollo de topologías de red eficientes y optimizadas para sistemas de DACQ capaces de operar en redes de alto ancho de banda.

[Obj-3] Actualización de la tecnología WR a nuevos estándares Ethernet de alto ancho de banda como 10G.

[Obj-4] Validación de interoperabilidad con otros dispositivos 10G. Optimización del bucle de control proporcional integrador (PI) y calibración del enlace en redes 10G.

[Obj-5] Desarrollo de nuevas aplicaciones para la red de sincronización basada en WR.

1.1.4 Proyectos relacionados

En este apartado, se describen los diferentes proyectos que se encuentran dentro del contexto de la presente tesis y en los que se han colaborado activamente. Los ejemplos más importantes se centran en infraestructuras de física de alta energía (HEP) e instalaciones de astrofísica. Además, hay otras aplicaciones importantes en el sector industrial que se comentan someramente. En las siguientes secciones, se presenta una breve descripción de cada proyecto.

Física de alta energía

En esta sección, se describen brevemente las instalaciones, proyectos y repositorios de HEP más relevantes:

- **OHWR [2]:** Es un proyecto abierto fundado por el CERN cuyo principal objetivo es proporcionar una plataforma donde los ingenieros puedan desarrollar soluciones hardware de una forma colaborativa y siguiendo los mismos principios del open software. Actualmente, alberga más de 100 proyectos abiertos.
- **LHC [3]:** Es el acelerador de partículas más grande del mundo ubicado en el CERN cerca de Ginebra, Suiza. Su propósito consiste en hacer colisionar partículas sub-atómicas en lugares específicos donde se sitúan detectores como el Aparato Toroidal para el Gran Collisonador de Hadrones (ATLAS), el Solenoide Compacto de Muones (CMS), el Experimento del quark fondo para el Gran Collisonador de Hadrones (LHCb) y el Gran Colisionador de Iones (ALICE). Estos son responsables de observar las partículas resultantes de las colisiones y así entender los elementos que componen la materia.
- **Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas (CIEMAT):** Es un centro de investigación español principalmente dedicado a la energía y el medio ambiente junto con sus aspectos tecnológicos. La Universidad de Granada (UGR) está colaborando activamente con el CIEMAT en algunos proyectos de investigación científica internacionales como la Instalación Internacional para la Irradiación de Materiales de Fusión (IFMIF). El propósito principal de este proyecto es estudiar diversos materiales para determinar la idoneidad de los mismos para su uso en un reactor de fusión. En esta infraestructura, una fuente de neutrones es la encargada de generar un gran flujo de neutrones bajo condiciones similares a las que habría en un reactor de fusión. Nuestra colaboración en IFMIF está especialmente centrada en los proyectos denominados como Actividades de Validación y Diseño de Ingeniería (EVEDA) y Fuente de Neutrones Orientada para el Reactor de Fusión de Demostración (DONES) [4]. El primero tiene como objetivo demostrar la viabilidad técnica de IFMIF [5] y el segundo es responsable de construir la infraestructura que proporcionara la fuente de neutrones con suficiente energía para estudiar los materiales candidatos para el reactor de fusión [6].

Astrofísica

En esta sección, se describen brevemente los proyectos e infraestructuras asociados al Foro de Estrategia Europea sobre Infraestructuras de Investigación (ESFRI) más relevantes en el campo de la astrofísica:

- **SKA [7]:** Es un proyecto internacional que se centra en la construcción del radio telescopio más grande del mundo. SKA desplegará miles de discos y hasta un millón de antenas de baja frecuencia sobre un área de un kilómetro cuadrado en dos localizaciones distintas: Sudáfrica y Australia. La configuración de SKA permite la realización de observaciones superando la calidad en resolución de imágenes del telescopio espacial Hubble. En este contexto, hay dos proyectos adicionales llamados Análisis del Medio Interestelar para Galaxias aisladas (AMIGA) [8] concretamente AMIGA5 y AMIGA6 cuyo objetivo principal es proporcionar una contribución española al proyecto SKA.
- **CTA [9]:** Será el telescopio terrestre de rayos gamma más avanzado mejorando en un factor de diez la sensibilidad de las infraestructuras actuales. CTA ha sido diseñado para detectar rayos gamma usando más de 100 telescopios distribuidos en los dos hemisferios de la Tierra: Paranal (Chile) y La Palma (España).
- **Foro de Estrategia Europea sobre Infraestructuras de Investigación para Astronomía y Clúster para la Infrastructura de Investigación (ASTERICS) [10]:** Es un proyecto internacional incluido en el marco de trabajo Horizon 2020 (H2020) de la Unión Europea (EU). Su objetivo principal es crear un equipo multidisciplinario compuesto de investigadores, científicos, ingenieros, especialistas de hardware y software para astronomía, astrofísicos, y físicos de astropartículas. Este equipo es responsable de desarrollar nuevos instrumentos y acelerar el desarrollo de las soluciones actuales que posibilitan el estudio de los eventos de interés. Además, ASTERICS se centra en el desarrollo de 4 instrumentos ESFRI: SKA, CTA, el Telescopio Extremadamente Grande (ELT) y el Telescopio de Neutrinos de Kilómetro Cuadrado (KM3Net). También está colaborando con centros de investigación como la Matriz de Baja Frecuencia (LOFAR), sistemas Interferometría de Base Muy Larga (VLBI) como la Red europea para la Interferometría de Base Muy Larga (EVN), el Sistema Estereoscópico de Alta Energía (HESS) y el Telescopio Muy Grande (VLT) que están operativos en la actualidad.

Proyectos con la industria

En esta sección, se comentan los proyectos más relevantes en el sector industrial:

- **Servicios de red de reloj (CLONETS) [11]:** Es un proyecto internacional focalizado en la transferencia del conocimiento sobre sincronización temporal de alta precisión en enlaces de fibra óptica a la industria y, al mismo tiempo, preparar el desarrollo de una red para las infraestructuras de investigación europeas. La creación de esta red ofrece una alternativa o, al menos, una solución complementaria para los sistemas actuales basados en tecnologías GNSS y sus bien conocidas vulnerabilidades. Además, se espera que la red europea sea compatible con las redes de telecomunicaciones actuales y de esa forma, habilitar varios servicios de tiempo junto con aplicaciones convencionales.
- **Tiempo preciso para industria (WRITE) [12]:** Desarrollará métodos y dispositivos para WR considerando características para la resiliencia que garanticen la distribución de tiempo y frecuencia a diferentes elementos y redes. Además, se deberán implementar mecanismos de calibración mejorados y escalables para WR y, al mismo tiempo, implementar técnicas de validación para la distribución de tiempo resiliente y redundante hacia usuarios que desplieguen

aplicaciones industriales. Como resultado, muchas aplicaciones industriales que requieren de sincronización de alta precisión podrán beneficiarse de la tecnología WR.

- **Instrumentos para Pequeñas y Medianas Empresas (SME):** Es un programa del marco de trabajo EU H2020 cuyo principal objetivo es acelerar el crecimiento rápido de las empresas y proporcionar nuevas oportunidades de mercado a través de actividades de innovación [13]. Nuestra contribución ha sido realizada al proyecto cuyo número de referencia del acuerdo es 725490.

1.1.5 Métodos y herramientas

La metodología seguida por la tesis ha sido principalmente experimental, aunque se requirió un primer paso de análisis teórico que incluye la revisión del estado del arte. Esto fue necesario para explorar las diferentes alternativas de sincronización temporal. Posteriormente, se utilizó para dividir la tecnología WR y resolver los problemas que podrían afectar su integración para otras aplicaciones. Además, permitió obtener los parámetros clave para el determinismo de la sincronización. La fase teórica fue necesaria no solo para realizar una exhaustiva revisión de la literatura o del estado del arte, sino también para establecer las condiciones y configuraciones adecuadas para los experimentos. También reveló los aspectos más significativos con respecto a las topologías de red, el procedimiento de medición y el modelado de los experimentos planificados.

En una segunda fase, se tuvieron que desarrollar algunos diseños en plataformas concretas para demostrar que los modelos teóricos funcionaban como se esperaba. Para esto, hemos utilizado varios lenguajes de programación para realizar diferentes tareas. Por un lado, hemos implementado diseños específicos para los dispositivos FPGA y SoC con entornos de desarrollo integrado (IDEs) como las herramientas de Xilinx Vivado [14] e ISE [15]. Estas permiten desarrollar sistemas utilizando lenguajes convencionales en el nivel de transferencia de registros (RTL) como el lenguaje de descripción hardware para circuitos integrados de muy alta velocidad (VHDL) o Verilog. También incluyen simuladores y características de analizador de lógica integrado (ILA) para validar la solución en diferentes etapas del proceso. Además, Vivado permite la creación de un proyecto basado en bloques propiedad intelectual (IP) con capacidades de síntesis de alto nivel. Este enfoque favorece el proceso de desarrollo porque incluye características avanzadas para usar las técnicas de co-diseño de hardware/software [16, 17] y, a la vez, permite la re-utilización de componentes de terceros de forma rápida. Por otro lado, hemos realizado algunas tareas de desarrollo de software utilizando principalmente lenguajes de programación C, C++, Bash script y Python para procesadores físicos como Máquinas avanzadas tipo conjunto de instrucciones de máquina reducido (ARM) [18] y procesadores dentro de FPGA como LatticeMico32 (LM32) [19]. Para lograr esto, se han utilizado varios kits de herramientas como los relativos al LM32 y la herramienta Buildroot que permite crear un sistema operativo (OS) integrado basado en Linux para muchas arquitecturas de procesadores diferentes.

En relación con los equipos físicos, hemos requerido multímetros de uso general, osciloscopios, medidores de frecuencia y analizadores digitales para fines de instrumentación. Además, otros elementos básicos para la tesis fueron una estación de trabajo personal con el OS denominado Ubuntu, cables de Grupo unificado de acción de pruebas (JTAG), relojes de alta estabilidad, fibras ópticas, SFPs, cables de Jack-45 (RJ45), cables de bus serie universal (USB), etc.

Las principales plataformas de hardware utilizadas para realizar los trabajos de tesis para diferentes proyectos presentados anteriormente (sección 1.2.4) fueron el Nodo White Rabbit embebido basado en Zynq (WR-ZEN), el Dispositivo White Rabbit de 16 puertos basado en Zynq (WR-Z16), el Nodo White Rabbit embebido ligero (WR-LEN), el Nodo simple White Rabbit basado en la versión express de la interconexión de componentes periféricos con conector para tarjeta de expansión para matriz de puertas programables (SPEC), el Switch White Rabbit (WRS) y la tarjeta para adquisición de datos extendida (XDACQ).

1.1.6 Organización de la tesis

La presente tesis está organizada en diferentes capítulos que se describen a continuación:

- **Capítulo 1, Introducción**: Presenta el trabajo de la tesis describiendo su contexto y los proyectos relacionados.
- **Capítulo 2, Estado del arte**: Contiene una revisión de la literatura sobre los mecanismos de sincronización temporal. También abarca la tecnología WR y el marco teórico necesario para la compresión de la solución expuesta en la tesis.
- **Capítulo 3, Desarrollo de un nuevo sistema WR basado en dispositivos SoC: Caso de uso de SKA**: Presenta una nueva y escalable arquitectura para los dispositivos WR basada en SoC con tecnología de nueva generación. Además, se presenta un caso de uso científico: La WR-ZEN para el telescopio SKA
- **Capítulo 4, Arquitectura de red asimétrica para infraestructuras científicas: Caso de uso de CTA**: Abarca la implementación de una arquitectura de red asimétrica que cumple los requisitos típicos de un sistema de adquisición de datos. Además, se presenta otro caso de uso científico: La XDACQ para el telescopio CTA.
- **Capítulo 5, Enlaces WR de alto rendimiento para interfaces 10G**: Expone el desarrollo realizado para la actualización de la tecnología WR para funcionar correctamente sobre redes 10G. Este desarrollo conlleva una mejora en la interoperabilidad de las soluciones WR y abre la puerta para nuevas aplicaciones.
- **Capítulo 6, Conclusión**: Enumera los resultados más relevantes extraídos de la tesis junto con las líneas de trabajo futuras más prometedoras y las principales contribuciones científicas.

1.2 Introduction

The first chapter is dedicated to providing a general overview of the scope and projects framework of this thesis.

This chapter is organized in six sections. Section 1.2.1 presents a general context for the main topic of the thesis: time synchronization. Section 1.2.2 describes the current needs for many applications in terms of time synchronization. It also introduces the White Rabbit (WR) technology considering its motivation, target applications, current status and future perspectives. Section 1.2.3 enumerates the different scientific objectives for the thesis. Section 1.2.4 establishes the main national and international projects in which the thesis works have contributed. Section 1.2.5 exposes the methods and tools used during the thesis time period. Finally, section 1.2.6 describes the chapters organization of the present thesis.

1.2.1 Overview

Until the latter part of the 18th century, time was normally determined in each town by a local sundial, resulting in every town having its own concept of current time. With the advent and expansion of the railway system in the 19th century, there was a growing need for managing train schedules. Standardized time zones, as well as means to synchronize time across these zones via the telegraph system, were implemented. Fast forward to the modern age of information technology in the 21st century: Network Time Protocol (NTP) was developed to have standardized means of synchronizing time between network devices across local and wide-area networks with sub-millisecond accuracy. By the time applications required greater precision, Precise Time Protocol (PTP) was developed to provide sub-microsecond accuracy. The development of time synchronization protocols and the deployment of the Global Navigation Satellite System (GNSS) has led to a €1.2B global market for solutions that provide time in 2016 [1], including Global Positioning System (GPS) receivers and equipment to transport and hand off timing signals to disparate devices and applications in need of accurate time.

Under this context, time synchronization is one of most important factors in many applications where several devices must cooperate together in order to fulfill a specific goal. Some important examples can be found at scientific infrastructures such as particle accelerators e.g. Large Hadron Collider (LHC) at European Organization for Nuclear Research (CERN) and Facility for Antiproton and Ion Research (FAIR) at Helmholtz Centre for Heavy Ion Research (GSI) and astrophysics facilities as Square Kilometer Array (SKA) or Cherenkov Telescope Array (CTA). Furthermore, industrial applications as telecommunication networks, Smart Grids facilities, financial infrastructures or Internet of Things (IoT) systems also have strict timing requirements that can only be fulfilled by means of advanced time synchronization techniques. In all these systems, each device has its own clock with a concrete and possibly different time notion. A clock is composed of an oscillator and a counter. The former produces a specific signal with a concrete frequency and it determines the clock granularity because the minimum time slot that can be measured is the oscillator period. The latter stores the number of oscillator transitions since an specific time instant or epoch. Due to the existence of many clocks in the system, the first step is to adjust them in order to match the same frequency at different locations. It is known as frequency synchronization or simply syntonization and ensures that every device counts time with the same rate. Moreover, different oscillators can work at the same frequency but with a specific phase offset that must be corrected using

phase alignment techniques. To perform a complete time synchronization, an additional adjustment is required for all counters associated to the clocks to match. If no time synchronization method is used for the system, clocks will start differing after some amount of time due to clock drift.

Currently, there are different mechanisms to provide timing synchronization, each one with its own features. Some of them uses timing signals whilst other ones deploy networks where packet-based protocols are used. Typically, in the network-based approach, different networks are deployed for synchronization and data delivery purposes. With this configuration, the system cost is increased at the same time than the required hardware resources: optical fibers, Small Form-factor Pluggable transceptors (SFPs), network interface cards, etc. In this scenario, the thesis has as main goal to study the synchronization technologies and the high bandwidth networks to elaborate an unified network solution where the synchronization and data information can travel using the same media.

The first step consists on reviewing the synchronization techniques to select the most appropriate one considering the time synchronization performance as key factor. During this process, many alternatives have been review, some of them were standard packet-based protocols as NTP, PTP or WR. The WR is a high accuracy synchronization protocol based on Gigabit Ethernet (GbE) technology that can reach the sub-nanosecond scale with a picoseconds range precision. However, WR technology presents some limitations that prevent to be used in some applications such as telecommunications networks. These are related to data bandwidth requirements, physical layer technology, robustness, redundancy and scalability over long link distances. The first two issues are referred to the fact that WR has been designed to work in 1 GbE networks. These can not provide enough data bandwidth for many applications and its physical layer technology differs from the higher bandwidth alternatives as 10 Gigabit Ethernet (10G) based ones. Therefore, this thesis includes some developments on this line in order to improve the WR technology to be ready for current and future applications allowing technology transfer from science world to industrial solutions. For this hard work, we have used advanced techniques for digital design known as hardware/software co-design and have worked with latest technology System-on-Chip (SoC) taking advantage of its hybrid architecture composed of a Field Programmable Gate Array (FPGA) device and a Central Processing Unit (CPU) microprocessor. These latest technology SoC devices have allowed the update of WR devices providing new interesting features. At the same time, they have been enabled to be used in applications in which the older versions were not suitable for. As a proof of concept of this new design, time synchronization system for SKA project has been developed obtaining amazing results (see chapter 3). Additionally, a new asymmetric network architecture has been designed and implemented for Data ACQuisition (DACQ) enabling the utilization of high data bandwidth links as 10G ones (see chapter 4). This asymmetric network architecture has been evaluated in the CTA project, demonstrating that the proposed solution not only exposes a good performance in terms of data bandwidth but a flexibility to be integrated into different applications that require a DACQ system. Finally, the WR physical layer has been adapted allowing its integration into current infrastructures with 10G links. In this line, an unified fully modular architecture has been designed using the asymmetric network implementation for DACQ systems and the new development of WR with 10G capabilities (see chapter 5).

To sum up, the thesis goal is to provide a common solution for synchronization and data networks using WR technology. The main hypothesis of this thesis consists on supposing that it is possible to send in the same network data and very high

precision synchronization patterns in a scalable, interoperable and reliable way.

1.2.2 Motivation

WR is a high accurate synchronization technology which has been developed by CERN in collaboration with other prestigious research centers such as GSI and important companies such as Siemens AG and National Instruments. WR has been presented in a open source project framework with a central public repository known as Open HardWare Repository (OHWR). Regarding WR technology design, it has been conceived to be a modular and scalable platform that is automatically reconfigured allowing monitoring and controlling mechanisms between thousands of nodes with link distances up to tens of kilometers. One important feature of WR is its deterministic behavior in the packet delivery alongside its low latency. It also can include pro-active methods to exchange important messages in a robust way taking into consideration exceptional failure conditions. The WR technology has been implemented as an extension of Precise Time Protocol version 2 (PTPv2). The PTPv2 defines several extensions or profiles that are oriented to certain strategic sectors such as energy, telecommunications, video distribution, etc. They allow to develop a specific solution for each applications focusing on their requirements. Nowadays, WR is being adapted to become the new high performance profile of PTP. In this vein, the standardization of WR implies a huge advantage for its integration into many industrial applications. The main conclusion of this study is WR technology provides a synchronization performance in the sub-nanosecond range. While it is true that some ad-hoc time synchronization technologies present a better performance than WR, they are not standard ones and they can not be integrated easily into many systems. In the light of all the points set out above, WR is the best choice for the time synchronization protocol.

1.2.3 Scientific Objectives

The scientific goals of the thesis are presented below:

[Obj-1] Design and development of a new family of devices and a methodology of WR systems based on the new generation programmable SoC components.

[Obj-2] Development of efficient and optimized network topologies for DACQ systems capable of operating in high bandwidth networks.

[Obj-3] Update of WR technology to new Ethernet standards with high data bandwidth features such as 10G

[Obj-4] Validation of interoperability with other 10G devices. Optimization of the Proportional Integral (PI) control system and link calibration for 10G networks.

[Obj-5] Development of new applications for the WR synchronization network.

1.2.4 Projects Framework

In this section, we describe the different projects, repositories and infrastructures that are in the context of this thesis and in which we have actively collaborated. The most important examples are focused on High-Energy Physics (HEP) and astrophysics projects. Moreover, there are other important applications in collaboration with industrial partners that are briefly commented. In the following sections, a description of each project is presented.

High-energy physics

In this section, the most relevant HEP facilities, projects and repositories are briefly described:

- **OHWR [2]:** It is an open project funded by CERN whose main goal is to provide a platform where engineers can develop hardware solutions in a collaborative way and with the same principles of the open source software philosophy. Currently, there are more than 100 open projects.
- **LHC [3]:** It is the largest particle accelerator in the world located at CERN close to Geneva, Switzerland. Its purpose consists on colliding subatomic particles at specific points where some detectors are deployed as A Toroidal Large Hadron Collider ApparatuS (ATLAS), Compact Muon Solenoid (CMS), Large Hadron Collider beauty (LHCb) and A Large Ion Collider Experiment (ALICE). These detectors are responsible for observing the particles resulting from the collisions to understand the elements that conform the matter.
- **Research Center for Energy, Environment and Technology (CIEMAT):** It is a Spanish research center mainly focused on the energy and environment together with the technological aspects in regards of these topics. The University of Granada (UGR) is collaborating actively with CIEMAT in some international scientific research program as International Fusion Material Irradiation Facility (IFMIF). Its main purpose is to test several materials in order to determinate their suitability for use in a fusion reactor. In this infrastructure, a particle accelerator neutron source is in charge of generating a large neutron flux under specific conditions similar to fusion reactor ones. Our collaboration in IFMIF is centered specifically in Engineering Validation and Engineering Design Activities (EVEDA) and DEMOnstration fusion reactor Oriented Neutron Source (DONES) projects [4]. The former aims to demonstrate the technical feasibility of IFMIF [5] and the latter is responsible for building an infrastructure which provides a neutron source with enough energy to study candidate materials for a future fusion reactor [6].

Astrophysics

In this section, the most relevant European Strategy Forum on Research Infrastructures (ESFRI) projects and infrastructures for astrophysics projects are briefly described:

- **SKA [7]:** It is an international project that focuses on building the world's largest radio telescope. SKA will deploy thousand of dishes and up to a million low-frequency antennas over a square kilometer of collecting area at two different locations: South Africa and Australia. The SKA configuration enables to perform observations exceeding the image resolution quality of the Hubble Space Telescope. Under this context, there are two additional projects entitled Analysis of the interstellar Medium of Isolated GAlaxies (AMIGA) [8] i.e. AMIGA5 and AMIGA6 whose main goal is to provide a Spanish contribution to the SKA project.
- **CTA [9]:** It will be the most advanced ground-based gamma-ray telescope improving in a factor of ten the sensitive of the current infrastructures. CTA has been designed to detect gamma rays using more than 100 telescopes located at the two earth hemispheres: Paranal (Chile) and La Palma (Spain).

- **Astronomy European Strategy Forum on Research Infrastructures & Research Infrastructure Cluster (ASTERICS) [10]:** It is an international project included in the European Union (EU) Horizon 2020 (H2020) framework. Its main goal is to create a multidisciplinary team composed of researchers, scientists, engineers, hardware and software specialists for astronomy, astrophysics and astro-particle physics. This team is responsible for developing new instruments and accelerating the development of the current solutions that enable the study of interesting events. Moreover, ASTERICS is focused on the development of four ESFRI instruments: SKA, CTA, Extremely Large Telescope (ELT) and Kilometre Cube Neutrino Telescope (KM3Net). It is also collaborating in some research infrastructures such as Low Frequency ARray (LOFAR), Very Long Baseline Interferometry (VLBI) systems as European Very Long Baseline Interferometry Network (EVN), High Energy Stereoscopic System (HESS) and Very Large Telescope (VLT) that are operating currently.

Industrial projects

In this section, the most relevant projects in collaboration with industrial partners are commented:

- **CLOck NETwork Services (CLONETS) [11]:** It is an international project focused on transferring high accurate synchronization knowledge over optical networks to industry and, at the same time, prepares the development of a pan-European network for the European research infrastructures. The creation of this network offers an alternative or, at least, a complementary solution for the current systems based on GNSS technologies and their well-known vulnerabilities. Moreover, it is expected that the pan-European network is compatible with the current telecommunications networks enabling several time services together with the conventional applications.

- **Precision Time for Industry (WRITE) [12]:** It will develop methods and devices for WR taking into consideration resilient features that guarantee the proper time and frequency dissemination to several endpoints and networks. Moreover, enhanced and scalable calibration mechanisms for WR must be developed and, at the same time, validation techniques must be implemented for redundant and resilient time transfers to industrial users. As a result, many industrial applications that require a high accurate time notion can benefit from WR technology.

- **Small and Medium-sized Enterprises (SME) Instruments:** It is a program in the EU H2020 framework whose main goal is to boost fast company growth and provides new market opportunities by means of innovation activities [13]. Our research contribution has been performed under the grant agreement number 725490 of this program.

1.2.5 Methods and Tools

The methodology followed in the thesis was mainly experimental, albeit it required a first step of theoretical analysis including the state of art revision. This was necessary to explore the different time synchronization alternatives. Then, it was used to bisect the WR technology and catch up its issues that could affect in its integration for other applications. Moreover, it allowed to figure out the key parameters for the

determinism of the synchronization. The theoretical phase was required not only to perform an exhausting literature review but also to establish the proper conditions and setups for the experiments. It also revealed the most significant aspects regarding to the network topologies, measurement procedure and modeling for the planned experiments.

In a second phase, some real implementations had to be developed to demonstrate that the theoretical models worked as expected. For this, we have used several programming languages to perform different tasks. On the one hand, we have implemented specific designs for FPGA and SoC devices with Integrated Development Environments (IDEs) as Xilinx Vivado [14] and ISE [15] tools. They allow to develop systems using Register Transfer Level (RTL) conventional languages such as Very High Speed Integrated Circuit Hardware Description Language (VHDL) or Verilog. They also includes simulators and Integrated Logic Analyzer (ILA) features to validate the solution in different stages of the process. Additionally, Vivado enables the creation of a project based on Intellectual Property (IP) cores with high-level synthesis capabilities. It boosts the development process because it includes advanced features to use hardware/software co-design techniques [16, 17] and, at the same time, it enables the re-utilization of third-party components in a fast way. On the other hand, we have performed some software development tasks using mainly C, C++, Bash script and Python programming languages for hard processors as Advanced Reduced Instruction Set Computer Machines (ARM) [18] and soft-processors inside the FPGA as LatticeMico32 (LM32) [19]. To accomplish this, several toolchain environments have been used as LM32 toolchain and Buildroot tool which creates embedded Linux Operating System (OS) for many different processor architectures.

In relation to physical equipments, we have required general purpose multimeters, oscilloscopes, frequency meters and digital analyzers for instrumentation purposes. Moreover, other basic items for the thesis were a personal work station with Ubuntu OS, Joint Test Action Group (JTAG) cables, high stability clocks, optical fibers, SFPs, Registered Jack-45 (RJ45) cables, Universal Serial Bus (USB) wires, etc.

The main hardware platforms used to perform the thesis works for different projects previously presented (section 1.2.4) were White Rabbit Zynq Embedded Node (WR-ZEN), White Rabbit Zynq 16 ports (WR-Z16), White Rabbit Lite Embedded Node (WR-LEN), Simple Peripheral Component Interconnect Express Field Programmable Gate Array Mezzanine Card carrier (SPEC), White Rabbit Switch (WRS) and eXtended Data ACQuisition (XDACQ).

1.2.6 Organization of the Thesis

The present thesis is organized in different chapters that are described below:

- **Chapter 1, Introduction**: It presents the Ph.D. thesis work describing its context and associated projects.
- **Chapter 2, State of the art**: It contains a literature review about synchronization mechanisms. It also covers the WR technology and the theoretical background needed to understand the developed solutions exposed on this thesis.
- **Chapter 3, Development of a WR system based on SoC devices: SKA use case**: It presents the new modular and scalable architecture for the WR devices based on new generation SoC technology. In addition to that, a scientific use case is described: the WR-ZEN for the SKA Telescope.

- **Chapter 4, Asymmetry network architecture for scientific facilities: CTA use case**: It covers the implementation of an asymmetric network architecture that fulfills the data acquisition system requirements. Moreover, other scientific use case is presented: the XDACQ for CTA Telescope.
- **Chapter 5, High performance WR links for 10G interfaces**: It exposes the development performed to update the WR technology to work properly over 10G networks. This enhancement improves the interoperability of the WR solutions and opens the door for new applications.
- **Chapter 6, Conclusion**: It enumerates the most important remarks extracted from the thesis together with the most promising future work lines and the main scientific contributions.

Chapter 2

State of the art

"I have not failed. I've just found 10,000 ways that won't work."

– Thomas Edison

Contents

This chapter presents the State-of-the-Art (SoA) regarding the time synchronization. It is a key factor in many systems and, specially, in distributed ones. These are composed of several nodes that are scattered and connected by network links. In order to perform system tasks, nodes must exchange information through the network in an ordered way. It also requires an homogeneous time notion in the whole network to schedule properly different tasks. However, and because of each node is an independent element, it has its own time notion which is likely different from the notion of time of other nodes. In order to coordinate the entire system, a time synchronization technology must be deployed to ensure that all nodes share the same time notion. There are several alternatives to solve this issue. Some of them rely on timing signals, standard time codes or GNSS deployments. Moreover, there are well-known standard packet-based protocols as NTP, PTP, Datacenter Time Protocol (DTP) or WR among others and purely software solutions as Huygens algorithm. In addition to this, some ad-hoc solutions have been designed to work in specific metrological infrastructures obtaining an amazing time synchronization performance.

The structure of the present chapter is organized in three different sections. Section 2.1 exposes the common definitions in the time synchronization research field. Section 2.2 depicts different approaches to implement a time synchronization system. Finally, section 2.3 shows several scientific and industrial applications where

the synchronization is an important requirement for the proper operation of the system.

2.1 General concepts

To understand the synchronization research field properly, it is necessary to establish some basic definitions:

- **Time transfer** is referred to the different techniques and mechanisms to share a precise reference time between several nodes in a network.
- **Frequency dissemination** comprises different techniques to spread the clock frequency over the network.
- **Synchronization** is a general term that implies the time alignment between different and independent clocks. The synchronization can be divided into different steps:
  - **Frequency synchronization (syntonization):** The local clock frequency is the same than the reference one.
  - **Phase synchronization:** The local clock rising/falling edges occur at the same instant than the reference ones.
  - **Time synchronization also known as Time of Day (ToD) synchronization:** The local clock time and date are the same than the reference ones. It is related to the International Atomic Time (TAI) and Coordinated Universal Time (UTC) time scales.
- **Clock drift** is the variation of the clock frequency that occurs when no correction mechanisms are applied.
- **Clock skew** is the time difference between two clocks in the network. In our research context, clock skew is usually referred as phase difference.
- **Clock jitter** is defined as short-term ($\geq$ 10 Hz) variations of the clock edges from their ideal positions in time.
- **Clock wander** is defined as long-term ($<$ 10 Hz) variations of the clock edges from their ideal positions in time. This concept is not so relevant for WR solutions because of it does not affect them. However, we put here in definitions in the sake of completeness.
- **Accuracy** and **Precision** (Fig. 2.1). The former is defined as the proximity of a measured value to a standard or known one. The latter is defined as the closeness between different measurements.
- **Measurement of synchronization performance** is a very complex task which requires advanced metrics [20, 21]. In the following lines, some of most used ones are defined:
  - **Phase noise** represents, in the frequency domain, the short-term random fluctuations in the phase of a specific signal.
  - **Time DEViation (TDEV)** shows the phase difference between a specific clock and a reference.

- **Maximum Time Interval Error (MTIE)** defines maximum wander within an observation window.
- **Allan VARiance (AVAR)** is also known as two-sample variance and it is used to measure the frequency stability in clocks.
- **Allan DEViation (ADEV)** is also known as sigma-tau and is the square root of ADEV.
- **Modified Allan DEViation (MDEV)** measures frequency variation and frequency uncertainty of clocks.

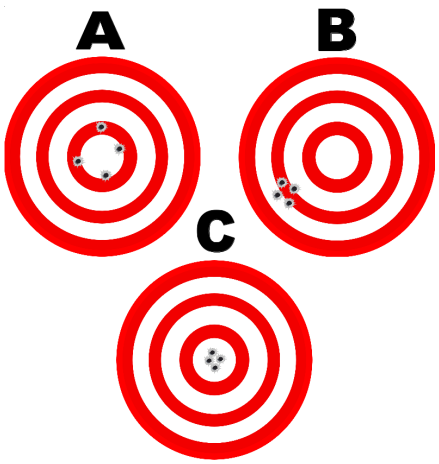

FIGURE 2.1: Accuracy (target A) indicates that values are around the known one. Precision (target B) is referred to the distance between measures is low, albeit these values are far from the expected one. Finally, target C shows a measurement with accuracy and precision.

2.2 Time synchronization technologies

This section presents several synchronization approaches focusing on their advantages and drawbacks.

2.2.1 Timing signals

The Pulse Per Second (PPS) is an electrical periodic signal with a frequency about 1 Hz. It presents a transition edge that accurately repeats each period and it can be used as timing reference for the synchronization protocols. The PPS signal provides the start of a new second so it can be used to frequency synchronization. In addition to the PPS signals, it is a very common practice to use a 10 MHz square or sine electrical signal to disseminate frequency between different devices. However, PPS and 10 MHz signals can not be used as complete time synchronization solutions because they don not provide additional timing information such a UTC.

The main issues regarding the PPS and 10 MHz signal distribution are the need of the calibration procedures to compensate the transmission delays and the signal degradation that reduces the accuracy.

2.2.2 Two-Way Satellite Time and Frequency Transfer

The Two-Way Satellite Time and Frequency Transfer (TWSTFT) [22] technique requires the utilization of two ground base stations (A and B) together with a geostationary satellite (S). The working principle is shown in Fig. 2.2. It consists on the transmission of a pseudo noise code sequence from A to S using modulated signals. Then, S re-transmits them to B. Consequently, B is able to compute the link delay and, therefore, the difference between the clock of A and the clock of B. Similarly, B also transmits pseudo noise sequences to S which re-transmits to A. Thanks to it, A is able to compute the link delay and obtain the clock difference too.

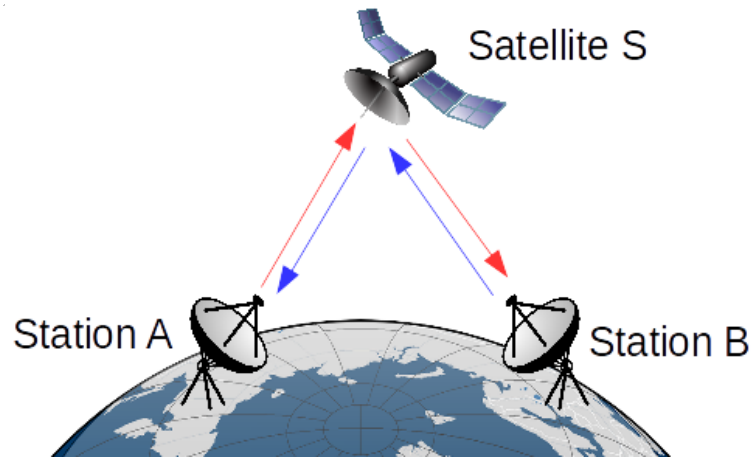

FIGURE 2.2: TWSTFT synchronization technique needs two base stations (A and B) and a satellite (S). The red and blue arrows represents the transmissions in different ways.

2.2.3 GNSS

The GNSS is a technology that allows to determine the position of a specific receiver by means of a constellation of satellites. The receiver position is given by its coordinates (latitude, longitude and height) [23] that can be obtained using the distance between the receiver and different satellites. The satellite constellation must be configured properly to guarantee that every receiver is able to establish communication with at least three satellites all the time. These three satellites are enough to calculate the coordinates because they have atomic clocks that are synchronized in the nanosecond range. However, receivers are not equipped with atomic clocks due to they are very expensive. To obtain the time information together with the position one, a fourth satellite can be used to calculate the time difference between the receiver clock and the satellite constellation one. The GNSS is able to reach a time synchronization in the order of nanoseconds, specially when it is calibrated as shown in [24]. However, these kind of systems suffer some problems such as jamming and spoofing that can degrade the overall time synchronization and, even down the entire system.

The first systems GNSS were GPS by the United States of America (USA) and Global'naya Navigatsionnaya Sputnikovaya Sistema (GLONASS) system by the Soviet Union deployed around 1990 [25]. First of all, they were used mainly for military applications but soon some commercial and consumer markets raised. In addition to the GPS and GLONASS, there is other alternatives such as Galileo by EU and Compass by China.

2.2.4 IRIG

The Inter-Range Instrumentation Group (IRIG) [26] time codes are specific formats for transferring timing information. The standard time codes are designated using an alphabetic character and some digits.

The IRIG standard codes are described in the following lines:

- **Time code A:** 10 frames per second and the index count interval is 1 millisecond.
- **Time code B:** 1 frame per second and the index count interval is 10 milliseconds.
- **Time code D:** 1 frame per hour and the index count interval is 1 minute.
- **Time code E:** 6 frames per minute and the index count interval is 100 milliseconds.
- **Time code G:** 100 frames per second and the index count interval is 0.1 milliseconds.
- **Time code H:** 1 frame per minute and the index count interval is 1 second.

The most implemented time code of the IRIG specification is the Inter-Range Instrumentation Group time code B (IRIG-B), in particular IRIG B122. There are many commercial devices that generate IRIG-B signal to allow other devices to synchronize to within 1 microsecond of accuracy. It transmits 100 pulses per second using a sine wave carrier with a frequency of 1 KHz and it encodes the information of day of the year, hours, minutes and seconds using Binary-Coded Decimal (BCD) coding scheme.

2.2.5 Ethernet time protocols

In addition to the timing signals and GNSS systems, there are other solutions based on packet protocols. In this section, some packet-based alternatives are briefly described presenting their advantages and drawbacks.

Synchronous Ethernet

Synchronous Ethernet (SyncE) is an International Telecommunication Union Telecommunication Standardization Sector (ITU-T) standard for computer networks based on Ethernet technology. This standard is composed of three recommendations:

- **Architecture (G.8261 [27]):** This recommendation defines the SyncE network architecture taking into consideration the timing synchronization aspects.
- **Clocks (G.8262 [28]):** This recommendation establishes the timing characteristics for the SyncE clocks.
- **Messaging channel (G.8264 [29]):** This recommendation defines the Synchronization Status Message (SSM) for SyncE networks. SSM is used in Synchronous Digital Hierarchy (SDH) networks to provide traceability of synchronization signals.

The main goal of SyncE is to provide mechanisms for the transferences of clock signals over the Ethernet PHYsical (PHY) layer. Consequently, transferred clock can be made traceable to the Primary Reference Clock (PRC).

SyncE defines a hierarchical structure (Fig. 2.3) in which the root node is responsible for syntonizing its local clock to a external one, usually coming from GPS or atomic clock. Then, it propagates its own clock using SyncE. Finally, the others nodes recover this clock from the network and use an internal Phase-Locked Loop (PLL) to adjust their own clocks. Thanks to it, all clocks are syntonized in the whole network.

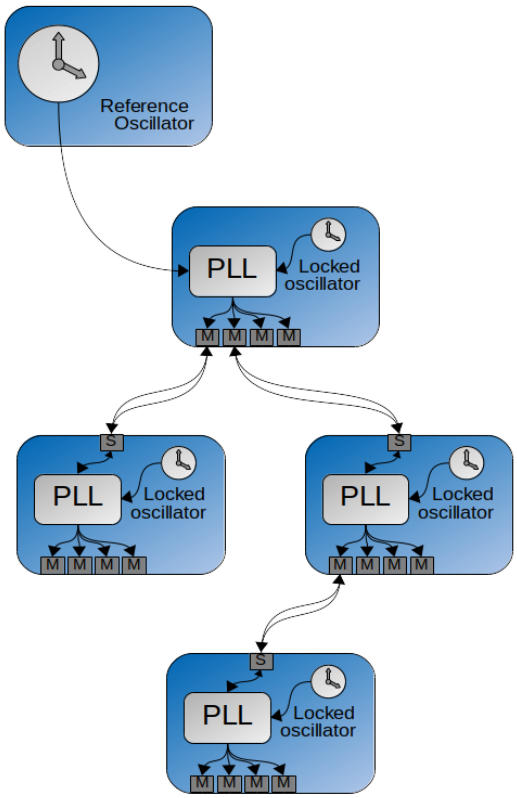

FIGURE 2.3: The Sync-E network contains a root element also known as PRC, normally a GPS or atomic clock, that disseminates its clock frequency to allow other elements in the network to syntonize. Devices placed at intermediate level of the hierarchy retrieves the reference clock from the uplink and syntonize their local clocks. Then, it encodes the transmission packets using this local locked clock and transmit them through downlinks. Finally, the leaf devices syntonize their local clocks using the reference clock from the link.

NTP

NTP [30, 31] was developed in 1981 by David L. Mills at the University of DElaware (DE), Newark, DE, USA. NTP is a packet-oriented protocol that defines several message formats using User Datagram Protocol (UDP) datagrams. Under this context, NTP protocol allows to synchronize devices connected in a Local Area Network (LAN) network or via Internet. In the NTP nomenclature is defined the client and the server. The client acts as slave node and tries continually to adapt its local clock and follow the server's one. The server replies to the client requests and provides to the client some timestamps for the delay calculation (see Fig. 2.4).

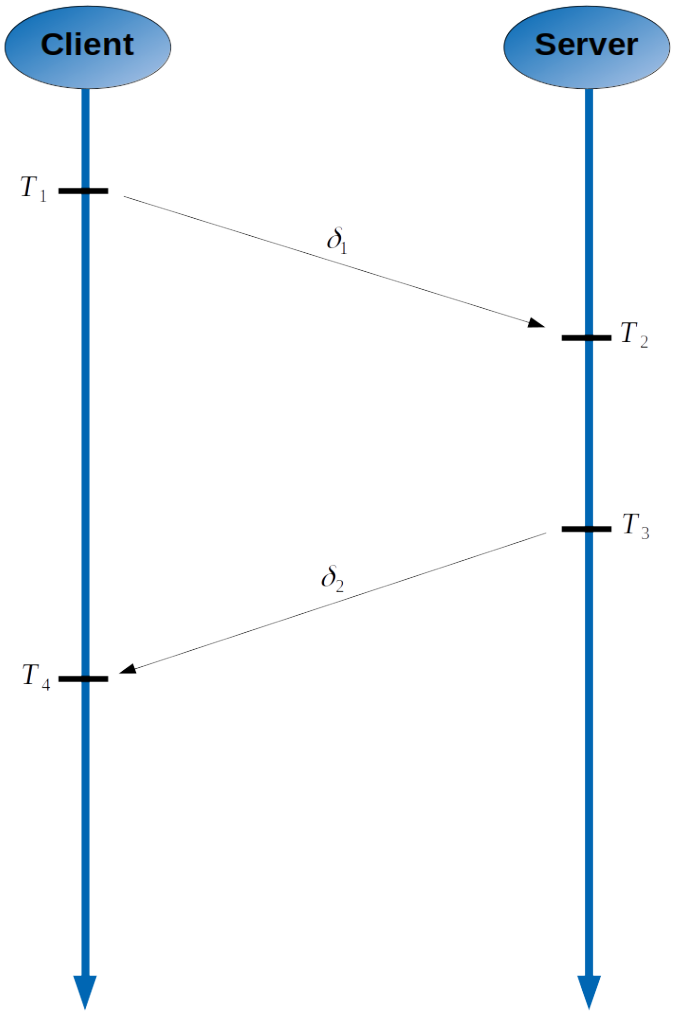

FIGURE 2.4: NTP protocol sends two packets to generate four timestamps. Thanks to these timestamps, the round-trip time can be computed and the clock can be adjusted.

Finally, NTP presents some limitations in regards of software timestamps resolution and the symmetric path assumption that avoid to get a better synchronization performance than a few milliseconds.

PTP

PTP is an Institute of Electrical and Electronics Engineers (IEEE) standard [32, 33], also known as IEEE-1588. It is a synchronization protocol that is based on message exchanging. It uses different kind of packets for the protocol and implements hardware timestamp to improve its accuracy. PTP establishes a hierarchical master-slave network topology for time synchronization. It also defines different kind of elements:

- **Ordinary Clock (OC):** This device only has a single network interface. It can be configured as slave or master.

- **Boundary Clock (BC):** This device has multiple network interfaces (≥ 2) which only one of them acts as slave meanwhile the other ones are configured as masters.
- **Transparent Clock (TC):** This device forwards PTP messages from master to slave. It introduces some time information inside each packet to compensate the forwarding process delay. In contrast to BC, it does not synchronize its local clock by means of PTP.

PTP follows the master-slave model where the slave device must perform some actions to synchronize its local clock to the master one. To perform this, PTP can use in two different methods: One-step or two-step. The first option requires that a specific hardware capable of inserting the hardware timestamp inside the packet on-the-fly. On the other hand, the two-step implementation uses an additional message to transmit the hardware timestamp related to the previous packet. In the PTP protocol shown in the Fig. 2.5, the master node starts sending an ANNOUNCE message to report its presence to the rest of the slave devices. It also starts the Best Master Clock (BMC) algorithm that is responsible for selecting the best master device for the whole network. Then, the master transmits a SYNC packet that contains the first hardware timestamp in the one-step implementation. If the two-step is used, the first hardware timestamp is sent using a FOLLOW-UP message. The second hardware timestamp is generated when the SYNC or FOLLOW-UP packet is received in the slave device in the one-step and two-step implementation respectively. The slave node transmits a DELAY_REQ message and generates the third timestamp. Finally, the master device receives the DELAY_REQ packet and responds using a DELAY_RESP message that contains the reception timestamp of the DELAY_REQ one. In addition to the previous PTP messages, it also implements signaling ones that are dedicated for non-time-critical communication topics.

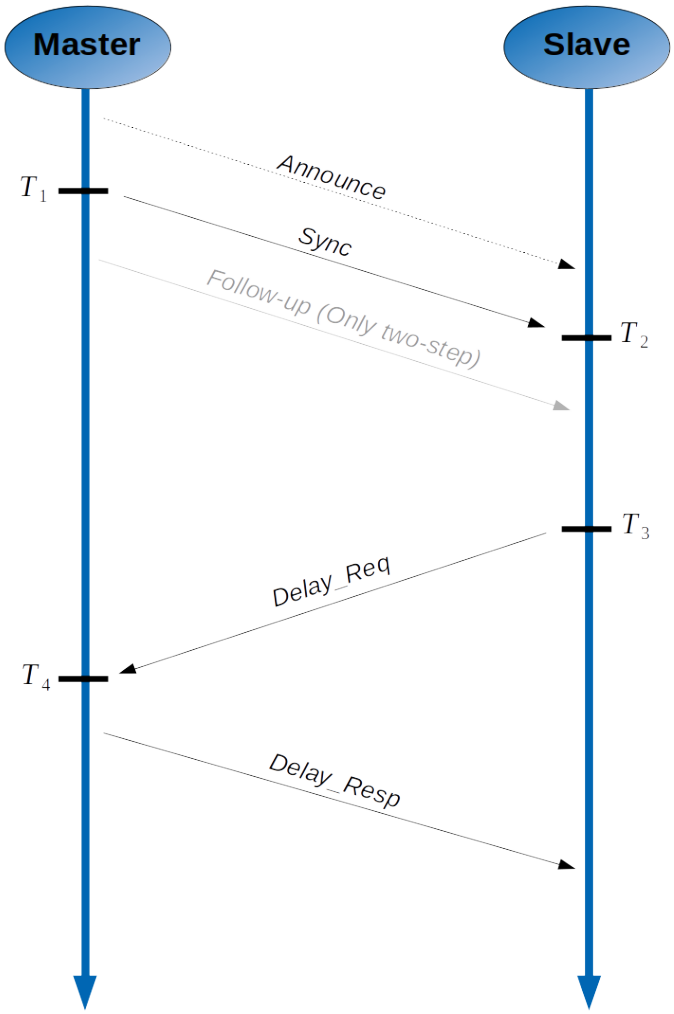

FIGURE 2.5: PTP protocol defines several messages: Announce, Sync, Follow-up, Delay Request and Relay Response. The picture shows the temporal order of these messages and the concrete timestamps that are generated on each case.

PTPv2 improves the accuracy of the previous version of PTP, however, it introduces an incompatibility issue between both of them. Moreover, PTPv2 brings new interesting capabilities that make it more suitable for several applications. They are the PTP profiles which specify a set of attribute values and optional features, conforming a specific configuration oriented to a concrete application [34]. PTPv2 profiles also can use Type, Length, Value (TLV) mechanism to extend PTP conventional packets and can implement an alternate version of the BMC algorithm. Some examples of PTPv2 profiles are focused on telecommunication networks applications such as G.8265.1, G.8275.1 and G.8275.2, other ones are dedicated to Smart Grids facilities as IEEE C37238-2011 or Time Sensitive Network (TSN) applications as IEEE 802.1 [35].

DTP

DTP [36] is a synchronization protocol used on data centers infrastructures. It defines several messages at the PHY layer of the GbE technology. The DTP exploits

the fact that the two endpoints connected by a GbE link are already synchronized. Therefore, the reception clock of one endpoint is built from the network recovered clock that drives the transmission path on the other side. Consequently, these clocks are virtually the same with some phase offset. The utilization of the PHY synchronization improves the timestamp resolution to the sub-nanosecond scale and provides a very low deterministic latency. Moreover, DTP packets are generated on the PHY layer without the software network stack intervention. It reduces significantly the overhead of the network stack and, at the same time, avoids its time uncertainty.

DTP uses idle characters of the GbE PHY layer to disseminate protocol messages. Each endpoint has associated a local counter in the PHY layer that is driven by its local clock. The DTP goal is to synchronize the local clocks of several endpoints taking into consideration the intermediate switches. The DTP algorithm is divided into two different phases:

- **INIT phase:** The one-way delay between two endpoints is measured when link is established. It is calculated by means of *INIT* and *INIT-ACK* messages and dividing the total delay by two.
- **BEACON phase:** Two endpoints sends their local counters for resynchronization.

The main limitations of the DTP are related to the PHY mechanisms utilization. Although it has several advantages described previously, the implementation of the DTP messages depends on the PHY layer specification that varies between the different network standards. Therefore, the DTP must be implemented on a different way for each network technology such as GbE, 10G and so on.

White Rabbit

Some applications require a better synchronization performance that can not be obtained using the previously described synchronization protocols. For these cases, WR technology [37, 38] could be applied. WR is an open initiative promoted by CERN and in which many important research centers and big companies are working currently. The WR-related project are hosted in OHWR which contains more than 100 open source projects. It is based on GbE networks and has been designed to be deploy using optical fiber networks with links up to 10 km each. It is able to synchronize thousands of nodes with a sub-nanosecond range accuracy and a precision in the picosecond scale.

WR uses three mechanisms for the time synchronization technology:

- **Frequency syntonization:** WR implements a dissemination of the frequency by means of a Layer 1 (L1) syntonization similar to SyncE. Moreover, it recovers the carrier frequency from the optical fiber link and adapts the local clock to follow it. In this way, the local frequency is tunned to be the same than the recovered one.
- **Enhanced PTP, also known as White Rabbit Precise Time Protocol (WR-PTP)** WR extends the two-steps PTPv2 to be suitable for high accuracy applications. It defines a new high accuracy profile of PTPv2 and currently, it has been proposed to be integrated into the official IEEE-1588 standard [39, 40] of PTP. WR-PTP includes additional signaling messages to establish a WR link properly in a first step. Then, the protocol is the same than the PTP standard one.

- **Phase measurement:** WR creates a new module based on the analog Dual Mixer Time Difference (DMTD) concept known as Digital Dual Mixer Time Difference (DDMTD). It is able to measure the phase difference between two clocks with a resolution of femtoseconds. The DDMTD is a digital implementation that consists on two low-pass filters, an interval counter and a local oscillator.

A WR network presents a tree hierarchy composed of different kind of elements: Grand-master (GM), nodes and switches. The former is in charge of synchronizing to a high accuracy timing source such as GPS or atomic clock and disseminates this reference to the rest of the network devices. The WR nodes are the leaf elements of the hierarchy and implement any user-specific applications that require high accuracy synchronization. Typically, the WR nodes implement some kind of DACQ or control system with sensors and/or actuators. On the other hand, the WRSs are the main elements in the WR network. They are responsible for switching data packets and provide WR synchronization mechanisms. The WRSs are compatible with any other Ethernet devices and they behave as a standard switches if no-WR devices are connected.

2.2.6 Software techniques: Huygens

Huygens [41] is a software clock synchronization protocol that does not require dedicated hardware and, consequently, it can be integrated easily into many applications. It is based on three key ideas: coded probes, Support Vector Machine (SVM) techniques and natural network effect. The former is used to identify network issues such as queue delays, random jitter and network interface card timestamp noise from probe data and rejects them for the synchronization algorithm. Then, it uses SVM and classification procedures to estimate accurately the one-way delay and synchronizes clocks with an upper limit of 100 ns. The latter is used to synchronize transitively the clocks over the network improving the synchronization error correction ratio.

In contrast to PTP or NTP, Huygens processes timestamps of probe packets exchanged by a pair of clocks in bulk over a 2 second intervals and simultaneously from multiple servers. Thus, Huygens is able to exploit inference techniques by means of SVM and estimates the time and frequency offset without clock period rounding issues.

The main limitation of Huygens is that is very focused on data centers infrastructures. Consequently, it is not easily applicable to other applications due to the utilization of advanced techniques such as SVM.

2.2.7 Metrological solutions

In addition to the previous described time transfer technologies, there are other alternatives that can offer a better timing and frequency performance. They use very specific devices which are not available as commercial ones and are mounted expressly for metrological infrastructures. These devices are extremely precise ones but they are also very expensive. Moreover, they require custom deployments together with complex calibration procedures. In addition to the custom devices, the metrological systems also require expensive equipment specifically designed to work in optical fiber networks such as ultra-stable lasers and expensive oscillators among others.

The metrological solutions are based on common approaches which can be classified into active and passive methods. These are briefly described in the following lines:

- **Active compensation:** It corrects the fiber fluctuations (phase or delay) by means of a feedback loop. In this approach, the signal is transmitted from one device to another via the fiber link. Furthermore, the signal is reflected to come back to the source device closing the loop. Under this scenario, the reference signal is compared to the reflected one being the feedback loop responsible for driving the error to zero. The active compensation has been used on urban networks of tens of kilometers obtaining a frequency instability below 10^{-18} s for a integration interval of 24 hours [42]. Moreover, it is able to obtain a time deviation below 1 ps from network of hundred of kilometers [43].

- **Passive compensation:** It is also known as phase conjugation technique. It uses a probe signal instead the reference one to obtain information about fiber phase fluctuations. Then, the reference signal is shifted accordingly to compensate them. This technique has been tested on a 150km urban network obtaining a frequency stability of 6 x 10^{-17} s with an averaging time of 10^4 s [44]. The main drawback of the passive compensation is that it can only be used to frequency distribution limiting the number of potential applications.

- **Two-way compensation:** It mimics the behavior of the TWSTFT applied to optical fibers. This approach demands that different endpoints connected through optical fiber have their own clocks. Moreover, time interval counter equipments must be deployed at these locations to be able to measure the difference between clocks. This approach has been used on a real fiber network of 612 km obtaining an accuracy of 2.2 ps for a 512 s averaging interval [45]. However, it can only be applied as an off-line service and not in real time.

The compensation techniques previously described are able to obtain timing and frequency performance in the picosecond or even in femtosecond range, albeit they are mostly applied to scientific infrastructures or in prototype networks. Currently, they can not be easily ported to industrial applications because of their custom networks setup requirements. Moreover, some of them require a specific network for frequency and time distribution or, at least, dedicated dark fibers/channels being difficult their adoption in some infrastructures.

2.3 Time synchronization use cases

There are many scientific infrastructures and industrial facilities that require a complex and specific system for the control tasks. These systems are composed of several nodes that are spatially scattered and connected using different network technologies. Due to their distributed nature, it is necessary to deploy synchronization mechanisms in order to coordinate the activity of each node in the system. Under this context, there are many applications that demand high accuracy synchronization mechanisms and their stringent requirements avoid to use well-known standard solutions such as NTP or PTP. In this situation, WR is a perfect candidate for these applications as synchronization solution because it can guarantee sub-nanosecond accuracy.

2.3.1 Metrological and scientific applications

There are many infrastructures that require synchronization procedure for proper operation:

- **National Time Laboratories.** Some examples are National Metrology Institute of Finland (VTT MIKES), Dutch National Metrology (VSL), National Laboratory of Metrology and Testing (LNE-SYRTE) in France, National Physical Laboratory (NLP) in United Kingdom, National Institute of Standards and Technology (NIST) in USA and National Institute of Metrological Research (INRIM) in Italy whose main goal is to distribute UTC time. To accomplish this, they have to deploy some time and frequency transfer technology to disseminate time information through the network. Normally, their networks have a root device known as GM which is in charge of providing the time reference. Then, several layers of the network are composed of switches that propagate the time information to the leaf nodes that are dedicated to specific applications. The time distribution is performed using a PPS signal together with the time specific packets.

- **Particle accelerators facilities.** They require a high accuracy synchronization technology for their control system. Remarkable infrastructures are CERN, GSI and International Thermonuclear Experimental Reactor (ITER) among others. In such applications, a time-triggered control mechanism is demanded. Under this context, a controller is responsible for sending in advance a sequence of actions together with the time information to the different devices of the network. Then, devices should execute required actions at a particular time specified by the controller. It is important to note that system latency is a critical factor for the system behavior.

- **Astrophysics applications.** These kind of systems need high accurate timestamping mechanisms for incoming events under study. It is necessary to be able to correlate information about the same event in different devices of the distributed system. CTA, SKA, Large High Altitude Air Shower Observatory (LHAASO) and KM3Net are specific examples of astrophysics infrastructures with strict time requirements.

2.3.2 Industrial applications

The most relevant industrial applications that demand high accurate time synchronization are exposed highlighting their requirements and candidate solutions:

- **Smart Grids.** The timing synchronization is one of the most important features for the Smart Grids infrastructures. It is required for several components of the system such as power plants, Phasor Measurement Units (PMUs) and voltage conversion substations to work properly. Currently, a GNSS is deployed to provide the time reference or at least by means of a local oscillator whilst IRIG-B, PTP/PTPv2 or NTP are used to time dissemination ensuring an accuracy in the range between milliseconds and microseconds. However, some Smart Grids systems are demanding an improvement on the synchronization accuracy (nanosecond scale) that is not easily covered by the current solutions.

- **Finance.** Financial services demand a high accurate synchronization technology to provide a log of events properly ordered on a chronological way. Moreover, the time information must be traceable to a well defined time references such as UTC. Under this context, the main applications in the Finance field are: banks, trading centers and stock exchanges. Bank entities are interested in knowing the causal links between different events in the systems. Therefore and due to their non-strict synchronization requirements, they use a GNSS, NTP server or a local oscillator as primary reference and disseminate time information using the NTP protocol. In the case of trading centers, a high accurate time synchronization (microsecond and even nanosecond range) is required because of interesting events are generated each microsecond. Moreover, system latency is other important feature specially for High Frequency Trading (HFT). For these finance applications, timing solutions are normally based on NTP servers, GNSS receivers or a local oscillator for the primary references and time distribution by means of timing signals or PTP. The stack exchanges also need high accuracy timestamps (1 ms in USA and 100 μs in EU) for all transactions. Under these circumstances, GNSS receivers, NTP servers or local oscillators are used as primary reference and timing information are transferred using PTP protocol.

- **Telecommunications networks.** Telecommunications applications have specific requirements related to the indoor cells that are not easily faced by GNSS systems. Moreover, Synchronous Optical NETwork (SONET) and SDH networks are becoming deprecated in favor of the packet-based protocols. In this new scenario, an accurate synchronization mechanism is required for proper operation of telecommunications infrastructures. Nowadays, current systems use GNSS receivers or a local oscillator for primary reference and deploy PTPv2 that is able to provide sub-microsecond accuracy. It is enough for the Long Term Evolution (LTE) requirements, albeit it is at the limit of what is permitted for Long Term Evolution Advanced (LTE-A) (1.5 μs). This situation represents a point of failure for the current standards. Furthermore, the incoming Fifth Generation (5G) generation networks will demand more exigent synchronization requirements that can not be accomplished with presented solutions.

- **Aerospace and defense.** Aerospace and defense systems need a fully deterministic and reliable notion of time. This capability guarantees a deterministic and coordinated behavior when an order is issued. A specific example are Unmanned Aerial Vehicles (UAVs) which require high accurate synchronization to calculate precisely their position coordinates. These systems are equipped with expensive high stable oscillators and GNSS receivers to obtain a time reference. Moreover, they disseminate the time information with different protocols such as NTP, PTPv2 or timing signals depending on specific application and its specific accuracy requirements (from milliseconds to nanoseconds).

- **Air traffic control.** In the aviation sector, GNSS is used for multiple purposes such as routing, surveillance, position calculation, movement control, etc. However, GNSS systems are not able to provide minimum requirements set by International Civil Aviation Organization (ICAO) and must be combined with European Geostationary Navigation Overlay Service (EGNOS) systems that has a 99.9% of availability by means of robust mechanisms as multi-constellation support. To sum up, in air traffic control applications, GNSS and

EGNOS systems are used to obtain a primary reference and the preferred dissemination mechanism is NTP protocol because of the required synchronization accuracy is typically on the millisecond range.

- **Industrial Internet of Things (IIoT).** Time synchronization is a fundamental feature for IIoT systems where a deterministic management of the time is required. Some examples of IIoT applications are autonomous factories, navigation systems, remote surgery, etc. Some of them have very strict requirements because the proper operation comprises human life. As common solution, these systems normally obtain the primary reference using a GNSS device and uses NTP, PTPv2 or timing signals as distribution mechanism for time dissemination with an accuracy in the microsecond range.

- **Professional Mobile Radio (PMR).** PMR devices are used as communication channel for some services as emergencies, police, coast guard and taxi companies. In these applications, a time synchronization technology in the microsecond range is mandatory to ensure a proper utilization of time slots that are dynamically assigned to different devices avoiding collisions or interferences. Currently, these systems are implemented using GNSS receivers to obtain a primary reference and generate timing signals to disseminate time information.

Chapter 3

Development of a WR system based on SoC devices: SKA use case

"We cannot solve our problems with the same thinking we used when we created them."

– Albert Einstein

Contents

This chapter presents the new design for WR nodes using high technology SoC devices. This contribution has been performed in the framework of the SKA international project. The previous design for WR nodes are pretty limited because they are based on standalone implementations or required an external Personal Computer (PC) for advanced capabilities. Under this context, Xilinx provides a very interesting alternative: the Zynq SoC. It combines a programmable logic device with a hard microprocessor inside the same chip. Thanks to this new architecture, WR nodes can implement more complex applications because of the OS utilization avoiding the development of very specific standalone applications. Moreover, many software standard components can be easily integrated into the system saving time and cost in the development phase. The WR-ZEN platform is equipped with a Zynq SoC and is offered as an enhanced alternative with regard to legacy WR devices. A flexible design has been implemented in the WR-ZEN to provide high accurate synchronization by means of WR protocol. Thanks to this contribution, the WR-ZEN platform

has been proposed as candidate for the SKA PPS distribution system. Moreover, several test scenarios have been evaluated to evidence that our proposal solution fulfills the SKA needs.

This chapter is structured as follows: Section 3.1 describes the general context for the DACQ systems and their requirements specially those regarding time synchronization. Under this context, some DACQ applications for scientific facilities and industrial infrastructures are cited. Section 3.2 presents the legacy WR solutions describing their basic architectural details and their limitations. Section 3.3 introduces SKA project and its needs. Section 3.4 performs a synchronization technology analysis taking into consideration the SKA requirements. Section 3.5 depicts the proposed SKA PPS distribution system based on the WR-ZEN platform. Section 3.6 discusses about some experimental tests and their results demonstrating that the proposed solution fulfills the SKA needs. Finally, section 3.7 exposes final conclusions and most promising future work lines.

3.1 Motivation

Nowadays, there are many scientific facilities and industrial infrastructures which require DACQ [46, 47] systems. They are composed of several nodes which are responsible for implementing different tasks. Some of them are dedicated to receive analog signals and convert them into digital information which are sent through the network toward a special node known as processing server. It is in charge of receiving, handling and extracting critical information that are always associated to important events. DACQ systems are designed to monitor some kind of events and to perform some actions consequently. However, there is an important issue related to events and the distributed nature of the system. The different nodes are connected through network links and each node extracts some analog signals independently. Then, information are sent to the processing server. Nevertheless, the latter needs some time event information in order to correlate data from several sources. Consequently, a key factor for DACQ system is the time synchronization technology.

The DACQ systems cover many different sectors such as telescope arrays e.g. LHAASO [48], SKA [7] and SKA's precursor Karoo Array Telescope (MeerKAT) [49]; particle accelerators e.g. ATLAS [50] and [51]; smart grid networks [52] and applications in health sciences [53] among others.

Under this context, the present chapter provides a revision about the DACQ system for the SKA project. It is focused on its time synchronization system which is responsible for disseminating a PPS reference signal through SKA network. In this line, our contribution is the development of the SKA PPS distribution system based on WR technology using WR-ZEN platform.

3.2 Current WR solutions

The current solutions for WR nodes are based on the White Rabbit Precise Time Protocol Core (WRPC) described in depth in [54, 37]. This core has been designed to be implemented in FPGA devices without requiring an external CPU. Therefore, it can be used in most embedded systems. The WRPC is composed of several blocks that are shown in the Fig. 3.1 and they are briefly described in the following lines:

- **LM32.** It is a soft-processor responsible for implementing the software control of the WRPC. It includes hardware drivers, WR-PTP network stack and a shell environment accessible through a serial port.
- **mini-Network Interface Core (NIC).** This module is in charge of transmitting/receiving data packets to/from the network through the Endpoint.
- **Random Access Memory (RAM).** It contains data and program code to run in the LM32 soft-processor.
- **Universal Asynchronous Receiver-Transmitter (UART).** It implements a general core to establish serial communication using a serial port, for example an USB interface.
- **Periph.** It contains several IP cores for different purposes as on-board EEPROM/Flash access, board temperature readings, etc.
- **SoftPLL.** It is a software implementation of a PLL module. Its main tasks are: clock phase measurement using DDMTD modules and external clock frequency adjustment using external Digital-to-Analog Converters (DACs).
- **1-PPS.** It contains the time counters for seconds and cycles from an specific epoch. They are adjusted by the WR-PTP software in order to synchronize their values. Moreover, this module generates a 1-PPS output signal that are aligned with the seconds counter.
- **Fabric redirector.** It is a special module that routes packets depending on some rules defined inside the Endpoint. Therefore, it forwards WR ones to the mini-NIC in order to reach the LM32 soft-processor. On the other hand, user packet traffic can be defined to be consumed by an external User IP core.
- **Endpoint.** It implements functionalities required by the Medium Access Control (MAC) and Physical Coding Sublayer (PCS) layers of the GbE technology. It also contains improved TimeStamping Units (TSUs) that generate high accuracy timestamps.

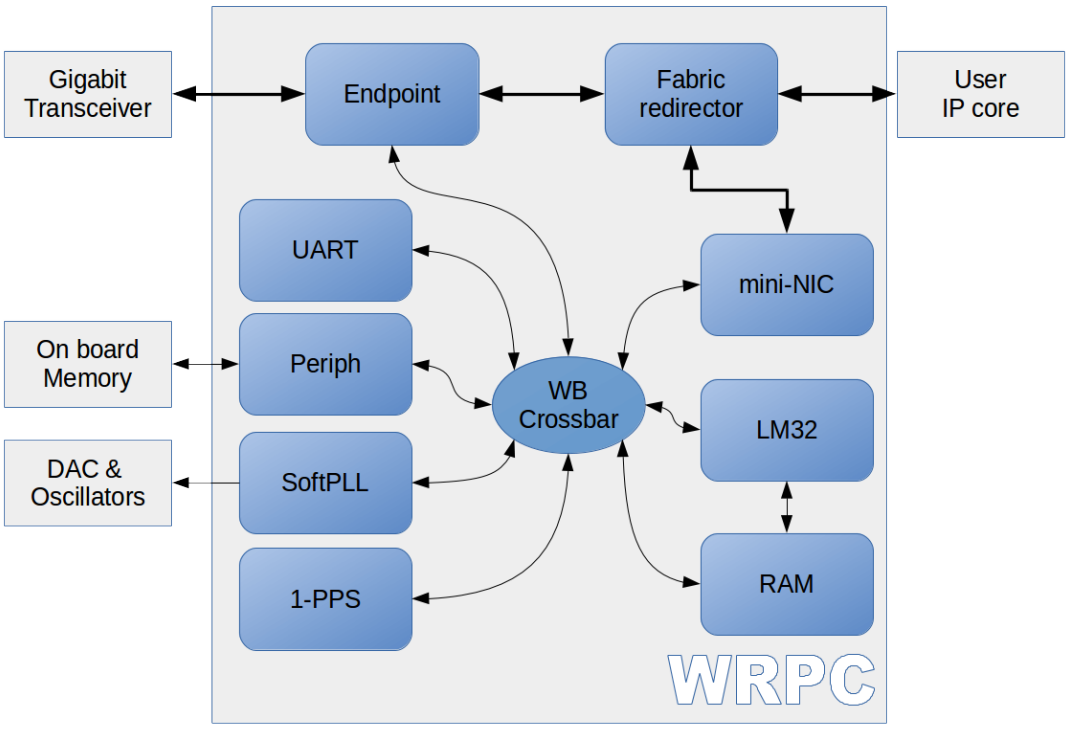

FIGURE 3.1: This picture shows the main basic elements for WR nodes. It contains a soft-microprocessor which is responsible for implementing the WR protocol. In addition, there are other important peripherals as the Endpoint for network capabilities, SoftPLL for measuring phase difference between clocks and 1-PPS which contains clock counters. This picture is inspired by Fig 1 from [54].

The WRPC can be integrated in many embedded systems which only have a single FPGA chip. However, its architecture is very limited in terms of software capabilities that can be developed. Its LM32 soft-processor has very limited resources and can not run easily typical OS such Linux ones. Then, WRPC-based devices usually require to be connected to an external PC using some bus protocol as Peripheral Component Interconnect (PCI) or Peripheral Component Interconnect Express (PCIe). Thanks to this, advanced software capabilities can be developed at the expense of consuming more resources and increasing the system costs. This drawback is not always suitable for many applications that demand compact systems optimizing resources and costs.

In this thesis, we introduce a new WR design using new generation SoC devices which overcomes these limitations. Moreover, this solution has been proposed to be integrated into SKA project in which the old WR implementations are not good candidates.

3.3 Square Kilometer Array

SKA [7] will be world's largest radio-telescope (Fig. 3.2), tens of times more sensitive and hundreds of times faster than existing infrastructures at mapping the sky. It will be located in two geographical areas: South Africa (MeerKAT [55]) and Australia/New Zealand (Australian Square Kilometer Array Pathfinder (ASKAP) [56]). The placement decision has been taken in oder to cover several frequency ranges

for the ska observations [57]. The construction of SKA has been faced in two phases: SKA1 (2018-2023) and SKA2 (2023-2033). Conceptually, SKA is a DACQ system composed of several distributed antennas connected through an optical fiber network.

FIGURE 3.2: SKA Telescope. This picture has been extracted from [7].

The Signal and Data Transport (SaDT) element [58] is responsible for designing the SKA Telescope network including hardware and software required for the information exchange between different elements of SKA. SaDT also specifies details about the provision of time which is a key factor for the interferometry. Moreover, SaDT also covers the Synchronization and Timing (SAT) that disseminates frequency and clock signals from a central ensemble to the rest of the system to guarantee the same phase information on all receptors. The phase coherence demands a short-term timing precision of around 1 ps and, in addition, an accuracy of 10 ns for 10-year periods for long-term timing pulsar requirements. However, only the accuracy requirement must be taken into consideration due to the frequency dissemination is performed through an additional network. Therefore, the PPS distribution network must deal with the accuracy requirement. Nevertheless, it is not only for the PPS distribution network and other elements consume some part of this [59]. Therefore, the PPS distribution system only has a timing constraint of 2 ns.

The PPS distribution system must deliver the timing information to the following locations:

- **SKA1-MID:** 133 dishes connected to optical fibers of 120-150 km.
- **SKA1-LOW:** 45 stations along 3 spiral arms connected to optical fibers of 70-80 km.

Depending on the frequency offset scheme applied to all SKA1-MID dishes, additional 64 endpoints may be needed in SKA1-MID. By this, the synchronization network might be increased from 182 to 246 endpoints.

There are some important factors to consider due to the location conditions. First, SKA1 uses aerial optical fibers in desert locations with large temperature excursion (more than 20°C) during operation. Second, wind conditions up to 40 km/h can influence changing the fiber length. Lastly, the Sagnac effect [60] appears for long distance links and can produce a deviation of about 350 ps as described in [61]. So far, the previous factors force to implement compensation techniques not to degrade the synchronization performance.

3.4 Synchronization technology for SKA

Regarding synchronization technology and as shown in chapter 2, GNSSs can be used to get timing information from satellites such as GPS, GLONASS [62] and Galileo [63]. Although the GPS solution is deployed successfully on many systems that require accurate synchronization [64], these technologies are exposed to jamming and spoofing issues. It is specially relevant for SKA infrastructure because its optical fiber strands are exposed to environmental conditions. Then, the time synchronization performance could be affected. Accordingly, GNSS can not be used as the only time synchronization technology in order to guarantee the proper operation of the time synchronization system. However, GNSS can be deployed as backup alternatives to provide synchronization if the primary system fails.

On the other hand, there are several synchronization solutions are based on packet protocols such as NTP [31] and PTPv2 [32, 33]. However, the standard packet protocols are not able to provide the frequency dissemination. Moreover, they are not able to provide a synchronization accuracy to meet the exigent SKA time requirements of 2 ns. As a result, NTP and PTPv2 are not suitable for implementing the time synchronization system for SKA.

Getting back to chapter 2, the only remaining synchronization technology which provides a enough accuracy performance and, at the same time, is based on well-known standard protocols is WR. Consequently, WR [65] has been proposed for the SKA PPS distribution.

3.4.1 WR devices survey for SKA

Once WR has been chosen as synchronization technology for SKA, it is necessary to select the most appropriate equipment from a suitable set of WR devices. They can be classified in two roles according to a typical WR network: BC and OC. The WRS [66] acts as BC and is a very convenient device for this role due to its 18 SFP slots. On the other hand, there are several WR platforms that can act as OC. Therefore, an analysis must be performed to chose the most promising device taking into consideration the specific requirements of SKA project. The candidate platform are presented in the following lines:

- **SPEC [67]:** It can be used in standalone mode [68], albeit it has a severe limitation regarding the computational resources. This limitation forces the utilization of a host PC to provide advanced software capabilities while the SPEC is connected to it via the PCIe interface.
- **WR-LEN [69]:** It is a standalone WR node with a good timing performance. However, this minimal design does not allow to implement advanced software capabilities easily.
- **WR-ZEN [70]:** It presents important improvement compared to the rest of WR nodes thanks to its novel architecture based on Xilinx Zynq SoC that includes a FPGA device together with a dual-core ARM microprocessor [18]. It also enhances the clock circuitry providing low-noise behavior.

Under this context, the WR-ZEN is the most suitable device for the SKA project. Currently, we are working as a partner in the SaDT [58] work package promoting WR-ZEN as the node for the SKA PPS distribution system.

3.5 SKA PPS distribution system

The SKA PPS distribution network presents a similar topology to the ITU-TG.8275.1-/Y.1369.1 standard where the SKA1 clock is the master time reference that must be disseminated through the entire network. To perform this dissemination, WR uses a master-slave configuration in a tree topology as presented in Fig. 3.3. There are two different kind of devices in the SKA PPS distribution systems:

- The WRSs [71] are multi-ports devices that are localized in the Central Signal Processors (CSPs) at each of the clock examples. For SKA1-MID, one is place halfway along each of the 3 spiral arms as repeaters to regenerate the signal for the longest links.
- The end-nodes (WR-ZEN [70]) are placed at the cores of SKA1-LOW and SKA1-SURVEY, along their spiral arms, one for each dish and CSP.

The different elements of the network are attached using a single fiber link up to 120 km and commercial SFPs. Howerver, the distances for SKA1-MID are longer and require a intermediate WRS as repeater. It introduces a penalty in the synchronization performance due to the increment of noise of each WR device. The jitter evolution in this case has been analyzed in [72] that explains the relationship between the number of hops and the timing degradation.

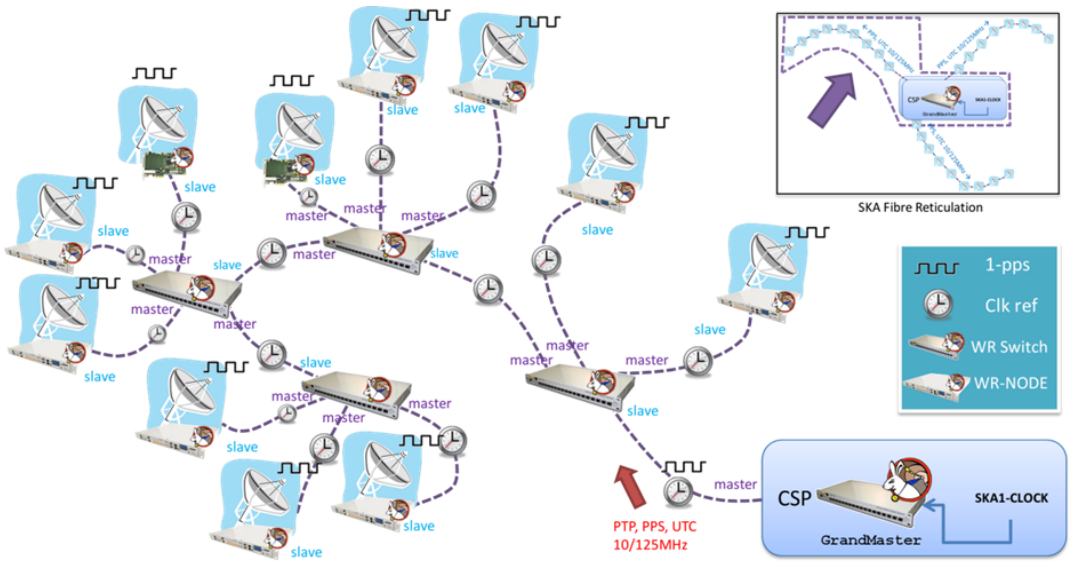

FIGURE 3.3: Network topology for PPS signal distribution based on WR switches and nodes.

An important consideration of the SKA PPS distribution system is that the WR network is used only for monitoring the absolute time of each PPS and activate an alert if PPS is not properly aligned. Under this context, the PPS signal of each node is derived from the reference frequency distributed from SKA clock instead of the WR network. In addition to this task, the WR system can alter the division ratio to bring the PPS edge back in alignment with UTC time. If this occurs, fringe finding must then be performed to restore the full calibration again.

3.5.1 WR-ZEN architecture

The WR-ZEN is a candidate for the SKA PPS distribution system node. It supports WR protocol to guarantee sub-nanosecond accuracy in the system. The first version of the WR-ZEN for SKA includes the Fine Delay Field Programmable Gate Array Mezzanine Card (FMC) card [73] that is responsible for generating the timing signals through specific channels. Nowadays, the utilization of the Fine Delay FMC is still under discussion and other version of the WR-ZEN can be presented without this module. An additional configuration has been performed using the Analog-to-Digital Converter (ADC) FMC [74] that can be used in DACQ systems to build a distributed oscilloscope. In addition to the core that controls this FMC, the WR-ZEN design includes two NICs for accessing optical fiber from OS as conventional network interfaces. A more detailed description of this configuration can be found in [75]. Due to the bandwidth limitations of the NICs, a high bandwidth version of the system has been developed in other contribution [76] obtaining a data bandwidth that cover almost the GbE link capability.

Hardware and FPGA design

The WR-ZEN hardware (Fig. 3.4) includes a Xilinx Zynq SoC and an enhanced clocking circuitry specifically designed to improve the clock stability. WR general performance is bounded by noise when the devices acts as GM locking to an external reference. A good way to reduce the noise is include external hardware PLL instead of the FPGA internal ones as discussed in [77].

FIGURE 3.4: WR-ZEN board

The FPGA firmware, also known as gateware, contains several IP cores connected on a WishBone (WB) bus through a WB crossbar. However, the communication with the ARM is provided by an Advanced Reduced Instruction Set Computer Machines Advanced Microcontroller Bus Architecture (AMBA) Advanced Extensible Interface (AXI) bus. Consequently, a specific bridge has been implemented to allow data transfers from one bus to another. An important block in its design is the White Rabbit Precise Time Protocol Core Dual Port (WRPC-2p) one. It is a natural evolution of WRPC including support for a second network port. A detailed description of this component can be found in [72], albeit a quick overview of its IP cores is shown in the Fig. 3.5.

The Fig. 3.6 presents the main components of the general FPGA gateware design:

- **WRPC-2p:** It is the main module of the design and it is responsible for providing WR synchronization mechanisms, networking capabilities and basic debug

functionalities. A more detailed description of the internal components (Fig. 3.5) can be found in [72].

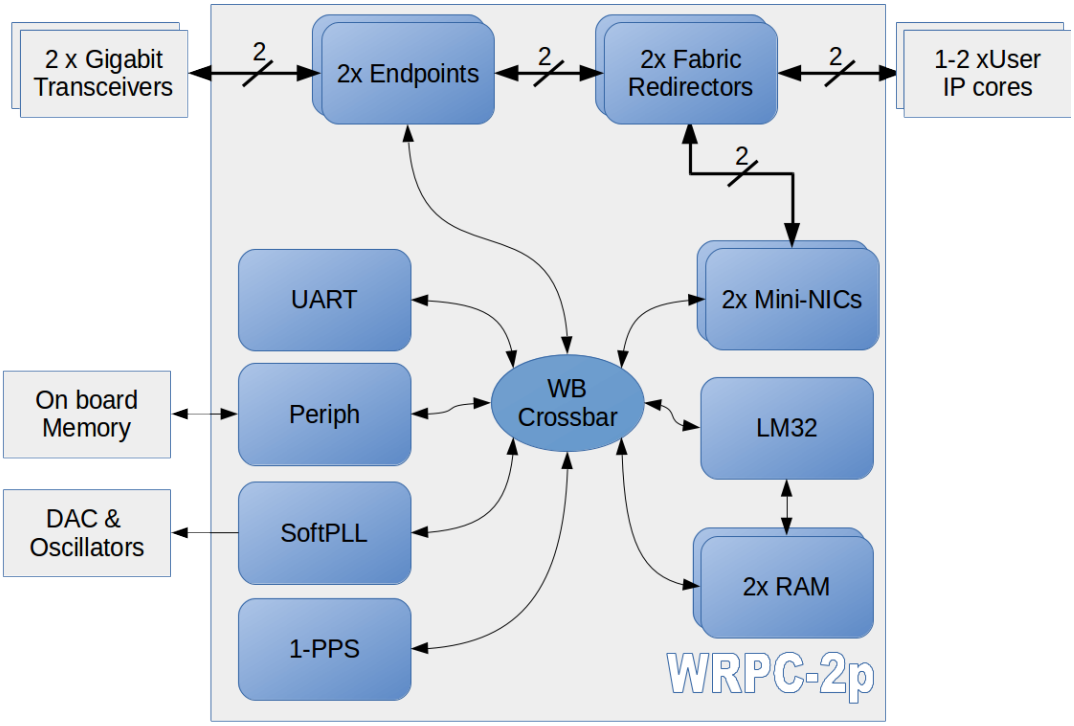

FIGURE 3.5: The architecture of the WRPC-2p is basically the same than WRPC one. The main difference is the duplication of the network blocks as Endpoints, Fabric redirectors, Mini-NICs and RAMs.

- **GTP:** It is referred to the transceiver primitive of the FPGA logic. It implements the high speed Serializer-Deserializer (SerDes) circuits and some specific logic for the physical layer of the GbE protocol.
- **NIC:** It is a module that implements the reception/transmission procedures allowing the processor access to the packets.
- **Transmission TimeStamping Unit (TxTSU):** It is a First In-First Out (FIFO) memory reserved to store the transmission timestamps temporary. It enables the processor to recover the time information for the outgoing packets.
- **Fine Delay FMC:** It is the controller for the Fine Delay FMC card if any is plugged into the FMC socket.
- **WB Inter-Integrated Circuit (I2C) arbiter:** It is a special component that allows multiple masters to access to a shared I2C bus. It is required due to the hardware configuration of the WR-ZEN.
- **AXI-WB Bridge:** It is in charge of converting AXI bus transactions into WB bus ones.

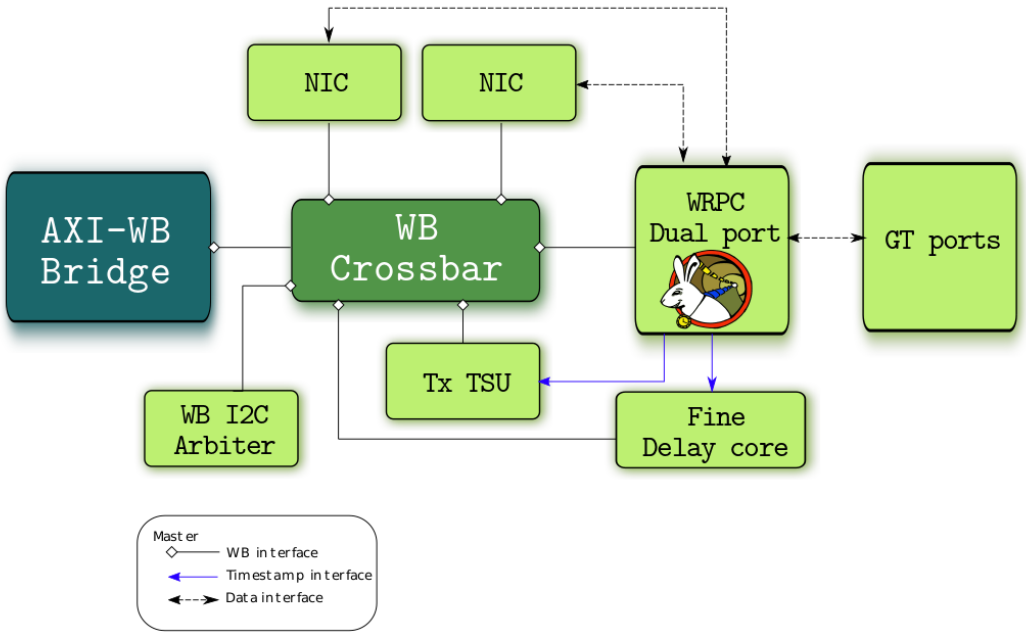

FIGURE 3.6: The WRPC-2p implements the WR protocol, the GTP primitives and NICs allow to receive/transmit Ethernet packets through the SFP interface and the Fine Delay core controls the FMC card.

Firmware and software

The firmware is related to the embedded software inside the soft-microprocessor contained in the WRPC-2p core. These main tasks are: the WR protocol implementation including the PTP stack and the servo control loop algorithm for the DACs which adjusts the local oscillator frequency to be locked to the recovered master's one.

The software (Fig. 3.7) is referred to functionalities developed on the top of an OS that are executed by the ARM. They are divided into two parts: userspace utilities and kernel support. The former implement a basic library (Zen library) and some tools (Zen tools) that are responsible for programming FPGA and access some internal IP cores such as the UART among others. On the other side, the kernel support includes some drivers to handle the entire platform.

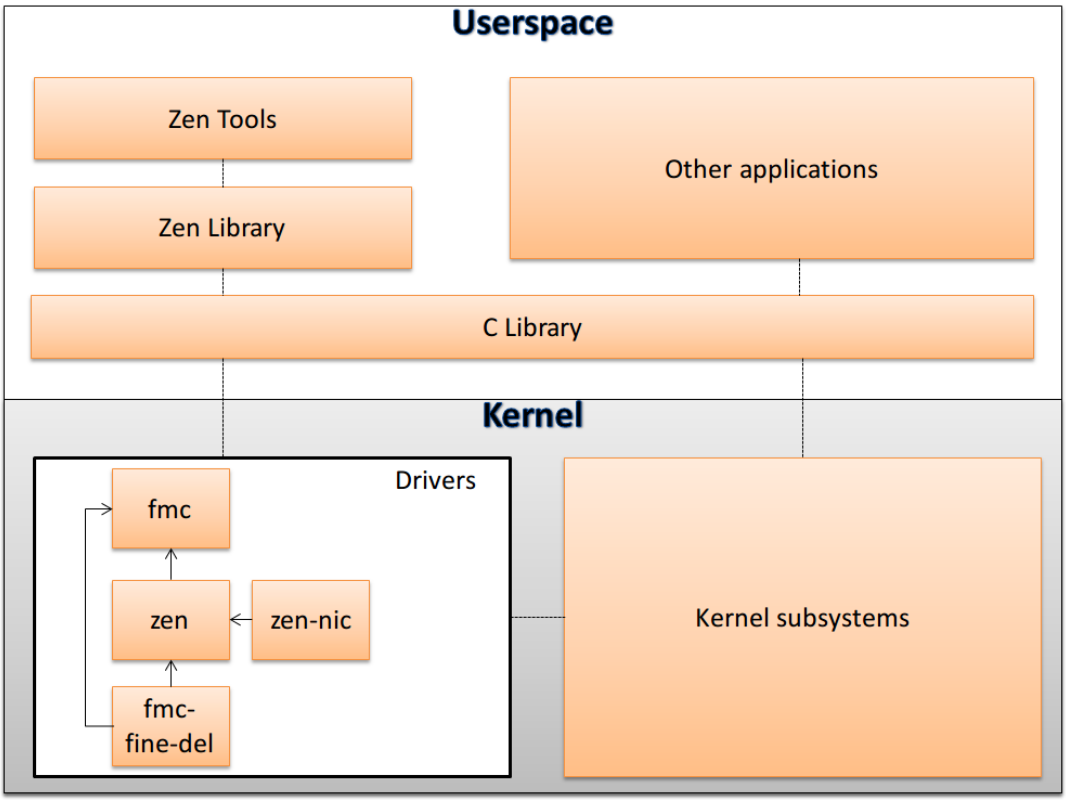

FIGURE 3.7: WR-ZEN software is composed of different components such as the Linux kernel, some specific drivers and custom userspace applications.

3.6 Experiments and results

In order to validate that the WR-ZEN design is suitable for the SKA Telescope PPS distribution system, three different experiments have been performed. The first one show a stability comparison between three different WR nodes previously presented in the section 3.4.1. The second one evaluates the scalability of the system for the SKA network. The latter covers a performance evaluation of the PPS stability under variable thermal conditions. The experiment setup is represented in the Fig. 3.8 and the principal equipment and tools used during experiments are presented in the following lines:

- 2x WRS (hardware v3.4 and firmware v5.0)
- 1x WR-LEN (hardware v1.0)
- 1x SPEC with a Digital Input-Output (DIO) FMC
- 2x WR-ZEN (hardware v3.0 and firmware v1.2)
- 1x Keysight high-resolution counter (52320A)

In addition to the devices mentioned, interconnection elements are necessary to establish the communication links such as SFPs modules (AXCEN 1310/1490 nm for short distances and GE-BX-80 1490/1550 nm for larger scenarios) and optical fiber strands (few meters, 20km and 50km). Moreover, an Oven-Controlled Crystal Oscillator (OCXO) Morion MV89 is utilized for providing the GM frequency reference.

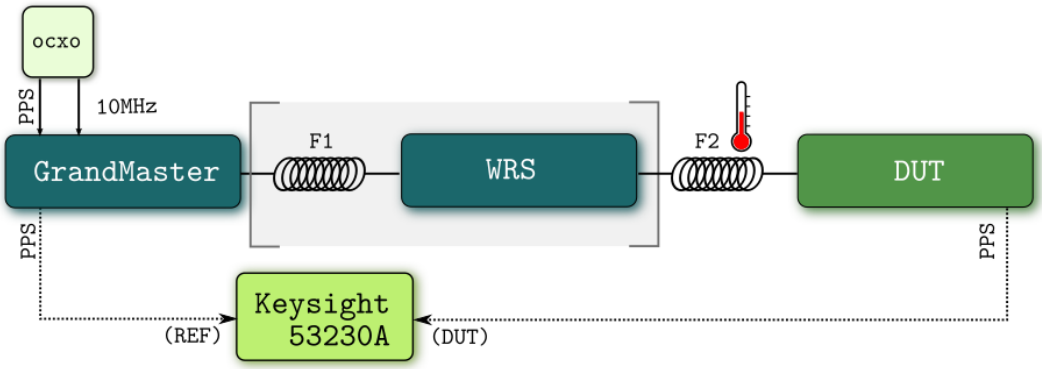

FIGURE 3.8: Block diagram of the different experiment configurations for the PPS stability, network scalability and temperature influence test using a climatic chamber.

3.6.1 PPS performance experiment

This experiment evaluates the PPS performance for the WR-ZEN, SPEC with DIO FMC and WR-LEN devices with a WRS configured as GM. The specific setup can be explained by observing the Fig 3.8. For this experiment under laboratory conditions, F1 and the second WRS are not included; F2 is a short fiber link of 0.5m and each node is attached to the WRS through a short fiber link of 0.5m. When the node is properly synchronized, we start to measure the time difference between the WRS PPS and slave node PPS during 24 hours.

The obtained TDEV statistic is shown in the Fig. 3.9. It indicates the stability of the phase between the WR master and slave versus the observation interval, τ. For a $\tau = 1$ s, the WR-ZEN has a TDEV value of 1.47e-11 s while the WR-LEN presents a value of 3.6e-12 s and 1.18e-11 s for SPEC. The lowest value is 1.0e-12 s for the WR-ZEN with differences respect to the lowest values of WR-LEN and SPEC of 6.2e-13 s and 4.6e-13 s respectively.

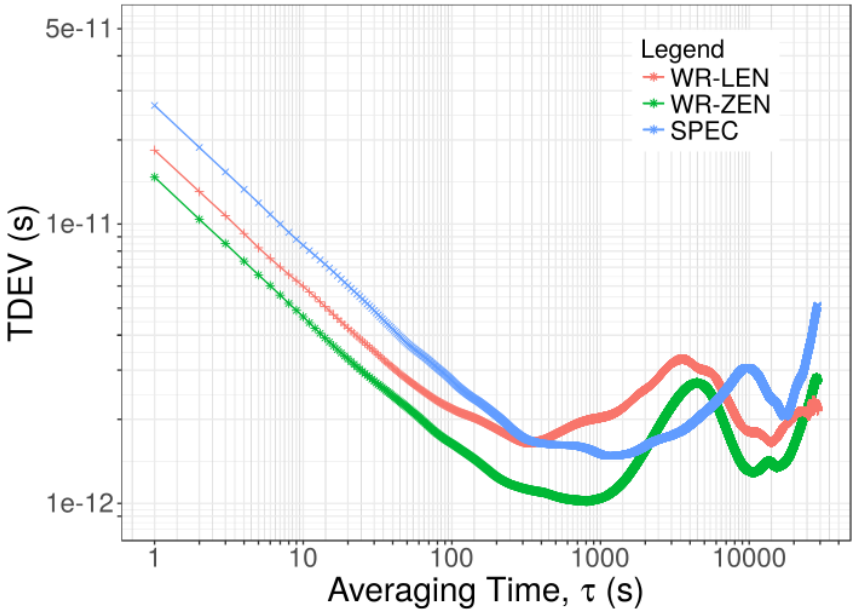

FIGURE 3.9: TDEV plot for the three analyzed WR nodes as slaves of a WRS

The MDEV results are drawn in the Fig. 3.10. Taking into consideration the TDEV (Fig. 3.9) and MDEV (Fig. 3.10) results, we realize that white Phase Modulation (PM) noise dominates from $\tau = 1$ s to few hundred seconds averaging time depending on the specific device. Thereafter, the rest is flicker PM noise.

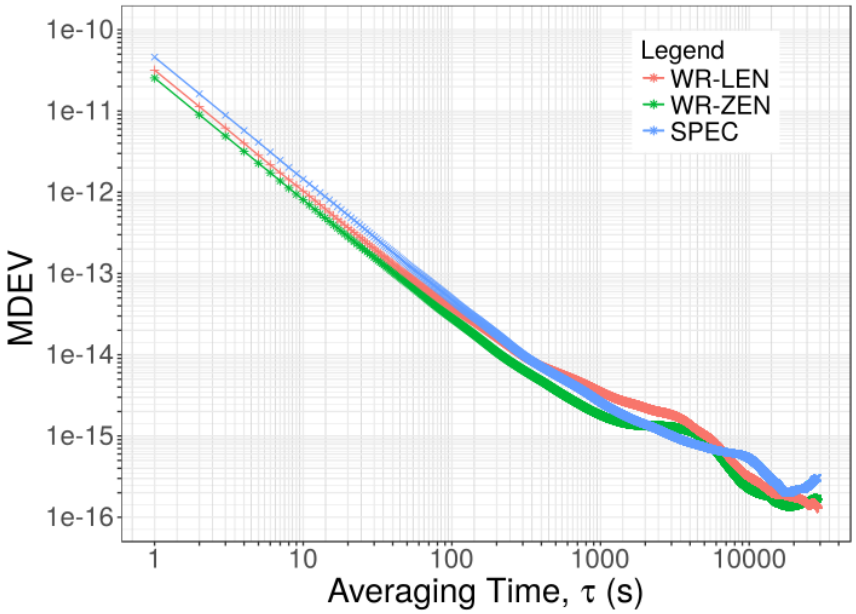

FIGURE 3.10: MDEV plot for the three analyzed WR nodes as slaves of a WRS

The worst case analysis has been performed using MTIE statistic (Fig. 3.11). The MTIE ensures that all the proposed WR devices fulfills the 2 ns synchronization requirement even for the worst conditions. For the WR-ZEN the time difference is

bounded on 1.5e-10 s. Once more, the WR-ZEN achieves the best results: 3.90e-11 s less than the WR-LEN and 1.02e-10 s less than the SPEC.

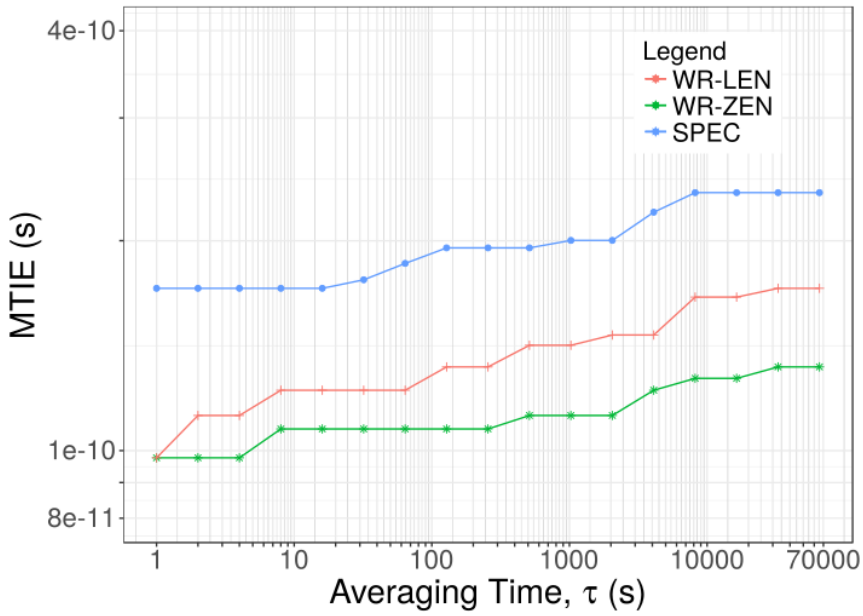

FIGURE 3.11: The MTIE plot analyzes the worst case scenario for the three WR nodes.

Finally, the tests reveal that the proposed solution fulfills the SKA Telescope PPS distribution system requirements and, in addition, improves the results obtained from other WR nodes.

3.6.2 Scalability experiment

The second experiment performs a scalability analysis of the WR solution for SKA. An estimation of 250 endpoints for the SKA network was discussed in the section 3.3. These nodes must be synchronized with an accuracy better than 2 ns. Under these circumstances, we have to demonstrate that WR solution is good enough with hundreds of nodes. For this purpose, we build a network as shown in the Fig. 3.8 (F1 and F2 are 20 km fiber spools under laboratory conditions) with two WRSs, one as GM and the other as BC and a WR-ZEN as end-node. We use SFP-GE-BX80 SFPs from FiberStore with 1490/1550 nm wavelengths and a Keysight 52320A counter to measure the PPS difference between the WR-ZEN and the WRS in GM mode during 4 hours. This test configuration allows to connect up to 306 end-nodes with only two hops and, therefore, it is a perfect setup to validate SKA requirements.

The numerical values for the TDEV and MTIE can be found in the Table 3.1 and have been calculated by octaves. For the short-term stability, TDEV is 2.32e-11 s. The minimum is reached at $\tau = 64$ s, after that, it is observed a frequency drift from $\tau = 200$ s to $\tau = 1000$ s (see Fig. 3.12). The MTIE results show that the maximum PPS error is bounded below 2e-10 s (see Fig. 3.13).

τ (s)	TDEV (s)	MTIE (s)
1	2.32e-11	1.36e-10
8	6.51e-12	1.36e-10
64	2.37e-12	1.46e-10
512	4.38e-12	1.61e-10
1024	7.27e-12	1.66e-10
2048	9.75e-12	1.75e-10
4096	7.97e-12	1.90e-10

TABLE 3.1: This table contains the TDEV and MTIE results from the scalability test.

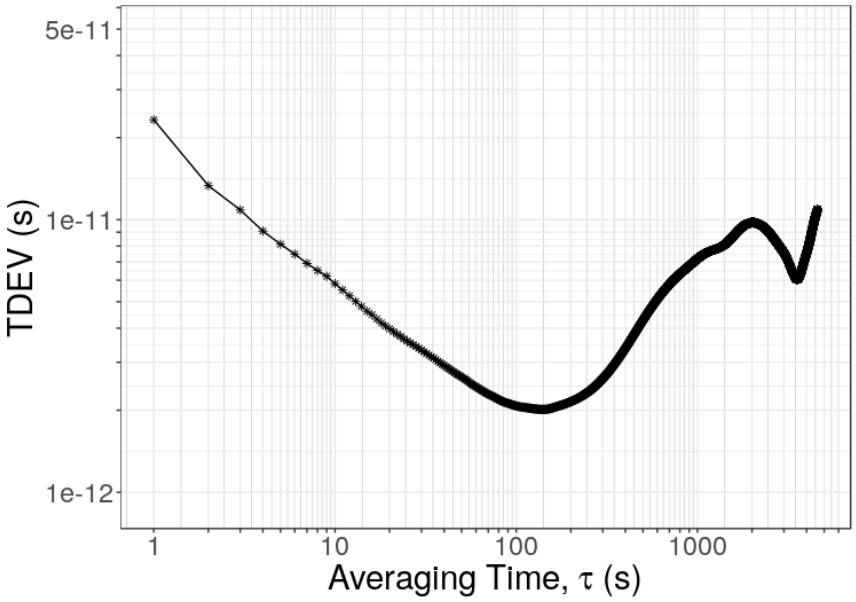

FIGURE 3.12: TDEV plot comparing the PPS signal from the end-nodes (WR-ZEN) to the GM of the network.

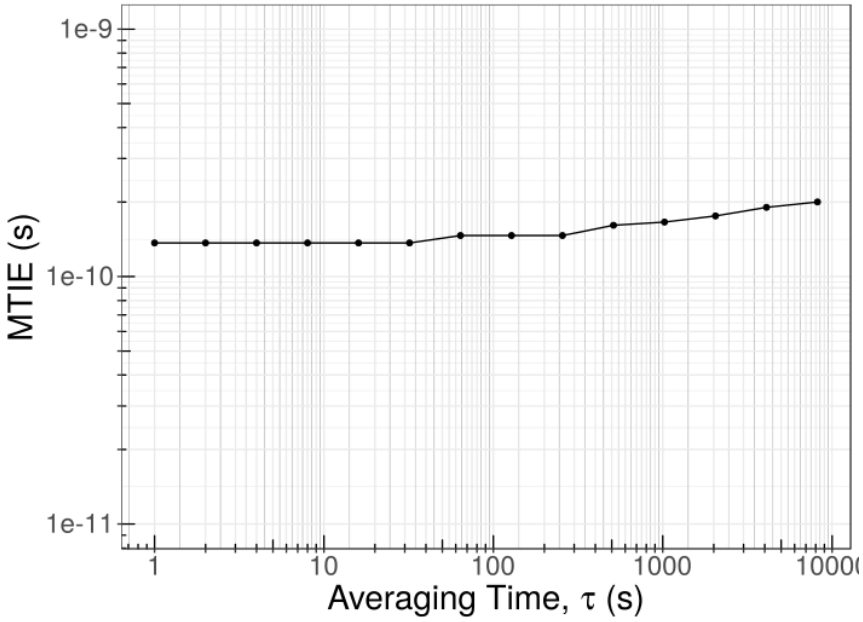

FIGURE 3.13: MTIE plot for the scalability test. The end-node (WR-ZEN) is compared to the GM of the network.

With the previous results, a WR network with two levels has been validated as synchronization provider to be used for SKA facilities. An important final remark is that some links could be divided into two WR links due to the distance between antennas. It is necessary to add an extra WR device increase the network levels. However, it does not introduce any issue related to the synchronization as discussed in [72], where a 10-hop WR network is also able to fulfill the SKA time requirement.

3.6.3 Temperature influence experiment

As commented in the section 3.3, the WR network in the SKA infrastructure will deploy long distance aerial fiber links. These optical channels are exposed to environment climate conditions and the propagation path is affected by external effects such as fiber bending, thermal expansions of materials, etc. All these factors can change the refractive index of the fiber impacting in the WR performance.

Chapter 2 explains that WR requires an accurate estimation of the one-delay between WR master and slave to calculate the time offset. Consequently, WR has to consider the fiber link as an asymmetric media where the transmission and reception path have different delay due to the wavelength-division multiplexing. It can be modeled as an asymmetry factor known as α and is assumed to be constant for the WR's link model. Nevertheless, the challenging environmental SKA conditions regarding the temperature can influence in α because of the chromatic dispersion [78].

The proposed solution has been tested by Joint Institute for Very Long Baseline Interferometry in Europe (JIVE) [79] in the SKA specific dessert zones of the South Africa and the main issues to face are described in [61]. In this thesis, we focus on the temperature effect over the Cable Round Trip Time (CRTT) and the PPS performance. For this purpose, we have performed an experiment with the setup shown in the Fig. 3.8 where F2 is a 50 km fiber spool in a climatic chamber (Fig. 3.14); F1 and WRS have not been used and using another WR-ZEN as the GM node. The CRTT and the PPS offset have been measured for a temperature range from 20^{o}C to

50ºC with 10ºC steps. We expected to bound the accuracy degradation due to a temperature change in the propagation medium. All the measurement of the dependent values, such as CRTT and PPS offset, were accomplished right after reaching the target temperature. The WR equipment was calibrated to compensate the characteristic delays of each device following the official calibration procedure [80].

FIGURE 3.14: Climatic chamber.

	RTT (ps)		PPS $offset_{SM}$ (ps)	
Spool temp (ºC)	$\overline{x}$	s	$\overline{x}$	s
20	478471695	303	193	17
30	478503719	50	203	17
40	478533492	807	150	17
50	478567050	399	110	14

TABLE 3.2: Results of the thermal characterization for an operational fiber temperature in range 20ºC to 50ºC with 10ºC steps.

The main results have been formated in the Table 3.2. On the one hand, the mean value of the CRTT and PPS offset samples. On the other hand, the standard deviation of CRTT and PPS offset. The experiment took 2 hours and acquired 7200 samples per temperature step. The amplitude of the CRTT is 96496 ps. We can easily obtain the CRTT variation in function of temperature dividing this amplitude by the temperature range. The result is 3213 ps/ºC. This variation is a huge value and can impact dramatically in the synchronization performance if no dynamic calibration mechanisms are included which is no acceptable for the SKA equipment. The peak-to-peak difference for the PPS offset is 211 ps which leaves us a 7 ps/ºC and if we divide by the total link length: $0.14 ps/ºC \cdot km$.

Lastly, the Fig. 3.15 reveals a linear dependency between the temperature and the CRTT. At the same figure, we have included the perfect fit between them with a yellow line. Comparing the fit with the experimental data, the high level of correlation between fiber temperature and CRTT is evidenced, albeit the PPS offset is not constant as we suppose in our initial hypothesis. The Fig. 3.16 suggests an inverse linear dependency between CRTT and the offset, expressed with a yellow line again. It must be considered that α is computed experimentally using fixed-point arithmetic. This computation does not introduce any penalty for short links up to few kilometers but it impacts for long distances as the ones used in our experiments. Nevertheless, the observed offset variation for a long distance link and a 30ºC temperature gradient is only 2e-10 s. This together with the results from the previous experiments make the new PPS distribution system suitable for the SKA timing system.

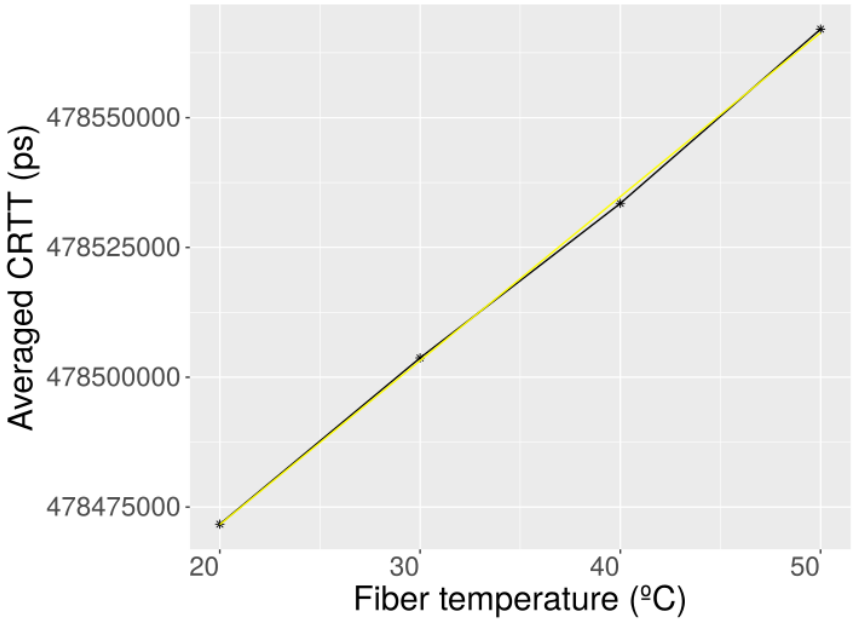

FIGURE 3.15: The figure shows the relation between the fiber temperature and the CRTT. The yellow line represents a perfect fit between both variables.

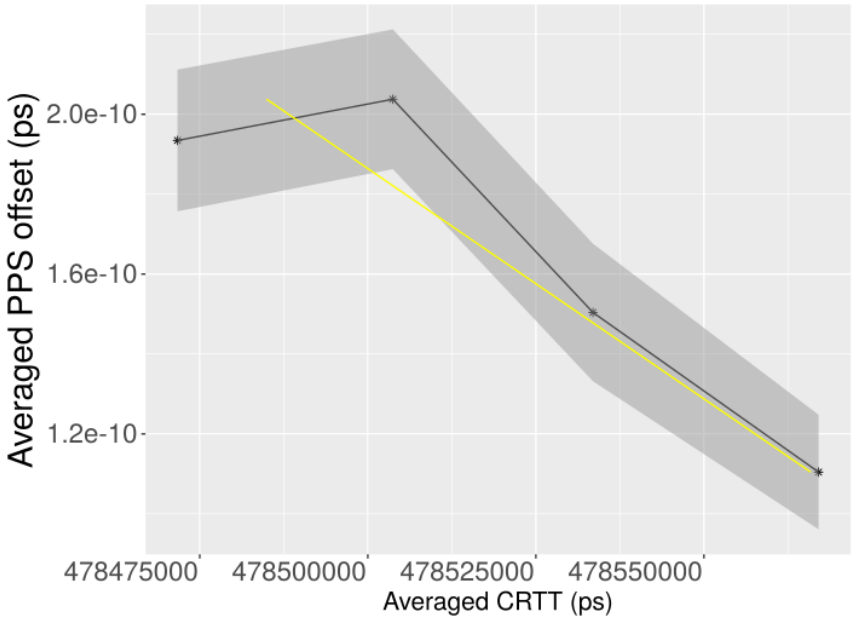

FIGURE 3.16: Evaluation of the CRTT time and the PPS offset with variable temperature conditions for the fiber link. A linear fit model is included with the yellow line.

3.7 Final remarks

This chapter presents a new implementation for WR nodes using platforms which include new generation SoC devices. For this, a new version of WRPC has been developed to work with two network interfaces. Then, a new gateware architecture has been implemented to take advantage of new SoC resources. Finally, it has been integrated successfully into the WR-ZEN platform obtaining a standalone platform with high accurate synchronization capabilities and, at the same time, advanced software features thanks to its software ecosystem based on Linux OS.

Once developed the WR-ZEN solution, it was proposed as WR candidate solution for the SKA Telescope timing system. Due to the exigent synchronization requirements of SKA, it is necessary the utilization of high performance synchronization protocol that ensure an accuracy better than 2 ns. Under this context, NTP and PTP are not suitable for integrating into SKA project. Therefore, the WR-ZEN platform is proposed because of its improvements in relation to the existing WR nodes and its ability to include advanced software functionalities. Moreover, its new gateware design is WR compliant, implements FMC support to integrate FMC cards and the enhanced clock circuitry reduces significantly its noise and can be configured to offer the best synchronization performance. WR-ZEN platform also provides a high level software environment with an Linux OS alongside to some userspace tools and drivers.

To evaluate and verify the goodness of our proposed solution, several tests have been performed. The PPS performance ones indicates that the synchronization accuracy is bounded below 200 ps that is far away from the 2 ns of SKA. Furthermore, the scalability tests show that the synchronization accuracy is maintained for hundred of nodes in network with several levels. Additionally, some experiments have been performed to simulate the SKA climatic environment conditions evaluating the thermal change influence in the fiber propagation delay and how they impact in the PPS

system performance. The experiments results evidences that the propagation delay is affected in a scale of tens of ns (96 ns) because of temperature changes. However, they also demonstrate that the PPS offset conserves its accuracy not exceeding hundreds of picoseconds (211 ps). The experimental findings guarantee that the proposed WR solution outperforms the exigent needs of SKA and is able to deal with the extreme environmental conditions of the telescope locations.

Finally, there are four key factors that must be studied in future contributions to improve the proposed system:

- The inclusion of different kind of SFPs with variable wavelengths. It could look an easy task but there are some calibration issues that must be faced.
- The realization of more environmental tests in SKA place locations to take into account more realistic atmospheric conditions.
- The enhancement of WR technology to reduce the jitter of the frequency dissemination. It enables the utilization of WR as candidate technology for the frequency dissemination network in addition to the PPS distribution one.
- The implantation of the WR proposed solution to other scientific infrastructures such as CTA [9], IFMIF-DONES [4, 81] or KM3Net [82, 83].

Chapter 4

Asymmetry network architecture for scientific facilities: CTA use case

"Perfect is the Enemy of Good."

– Voltaire

Contents

This chapter presents an asymmetric network DACQ architecture for DACQ systems. Conventional high data bandwidth networks are very complex and are not able to fulfill the very specific requirements of DACQ systems in terms of data flow features. DACQ systems are usually composed of many distributed devices which generate data to be processed by a central server. Therefore, several network connections must be joined into a single high data bandwidth link. Moreover, additional network capabilities are required due to the central server must configure and monitor different devices. Hence, a fully configurable and flexible routing mechanism must be implemented. This network architecture does not match to the high data bandwidth ones because of its asymmetric nature. Consequently, a new asymmetric network architecture has been proposed. It is able to provide high data bandwidth features and, at the same time, fully flexible routing functionalities for slow control traffic flows. It is a generic solution that can be applied for many DACQ systems.

Under this context, we have performed a DACQ design using our asymmetric network approach for CTA project. Concretely, it has been integrated into Compact High Energy Camera (CHEC), the prototype for Small Size Telescope (SST). Part of this work had been performed during a 3-month research stay in Amsterdam at Dutch National Institute for Subatomic Physics (NIKHEF) and we collaborated

actively with researchers in University of Amsterdam (UVA) that gave an important technical support. The proposed architecture is based on the XDACQ platform which includes a Zynq SoC together with two Kintex Ultrascale FPGA devices. It is the perfect tandem to implement a high data bandwidth system with advanced software capabilities. Additionally, our proposed solution has been tested intensively in several laboratory configurations to validate its functionalities along with system metrics: data bandwidth, resource utilization and latency. Moreover, this has been properly integrated into CHEC by Deutsches Elektronen-Synchrotron (DESY) staff. This integration has ensured that the proposed DACQ fulfills CTA and it is ready for the deployment.

This chapter is divided into five sections. Section 4.1 describes the motivation for the developed asymmetric DACQ architecture and sets the context in the CTA project. Section 4.2 presents CTA and its requirements. Section 4.3 explains in detail the proposed DACQ solution based on XDACQ platform. Section 4.4 shows experimental results which evidence the goodness of the solution in terms of resource utilization, data performance and latency. Finally, section 4.5 exposes final conclusions and most promising future work lines.

4.1 Motivation

As discussed in chapter 3, the DACQ systems are deployed in many applications for both scientific facilities and industrial solutions. For these systems, the synchronization is one of the most important issues to take into consideration. However, it is not the only one. DACQ systems are normally composed of many distributed sensors that generate a huge amount of data. This data must be transmitted to a central server in order to process it. Under this context, the network architecture design is an important task that must be faced carefully [84] due to the possibility of congestion problems. Although it is true that some software solutions [85] can be used, the data bandwidth is significantly reduced. It is not acceptable for all DACQ systems and some more complex solutions must be implemented using specific hardware components. Thanks to the FPGA devices, it is not necessary to design a specific hardware enabling the development of logic IP cores with the custom behavior. These required functionalities for DACQ network are: data aggregation and routing. The former is related to join different slow data streams in a fast data output interface. The main feature of this data flow is its directionality from sensors to the core network. The latter, the routing mechanism, is referred to a configurable data path for control/management packets. The source and destination of this data flow are not known in advance, therefore, switching components must be integrated into the system to allow the interconnection between any two nodes in the network. The previous described network architecture represents an asymmetric topology where a significant amount of data bandwidth is required in one direction whist in the other way a fully configuration routing path is demanded.

Under these circumstances, we have implemented a generic DACQ system considering the asymmetric network model (Fig. 4.1). This is able to aggregate several 1 GbE interfaces into a single 10G port without data bandwidth loss. In addition to that, a fully configurable and flexible routing system has been implemented to enable control/management flows from the processing server connected to the 10G interface to a device attached to a specific 1 GbE port. For the routing mechanism, a Routing Table Unit (RTU) IP core has been implemented. It is able to detect MAC

address of each packet and route it depending on its value. The RTU configuration can be performed using a software tool that has been created.

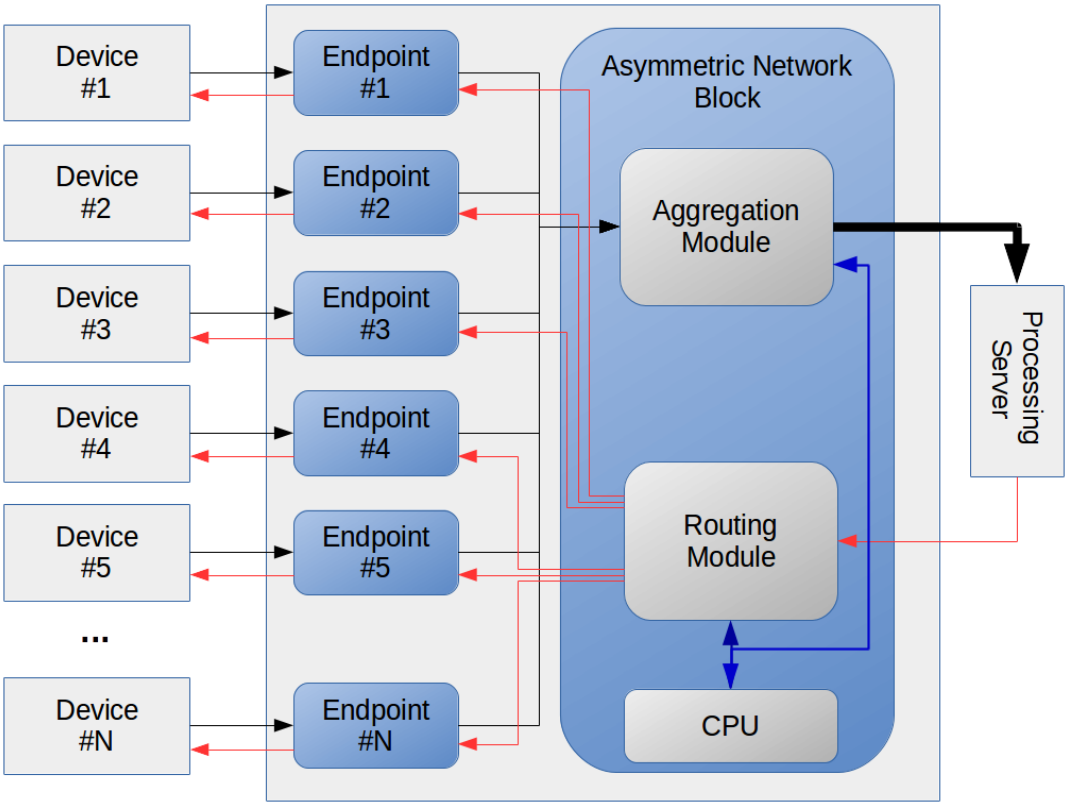

FIGURE 4.1: It shows the asymmetric network model with several devices generating data and a single processing server. The black lines represent the aggregation datapath from devices to the server. The red lines show the routing datapath for the control/management from the server to devices. Finally, the blue lines are required connections to allow the CPU to configure the behavior of aggregation and routing blocks.

In order to verify the goodness of our design, we have focused on telescope array systems as specific examples of DACQ applications. The design for these infrastructures comprises very complex tasks with many aspects to take care of [86] and where there are many key factors such as energy efficiency [87] that constraints the solution. As specific use case, we have developed a DACQ system for the CTA scientific project to be integrated into its SST concretely in its prototype known as CHEC. The CTA will be an observatory for gamma ray astronomy with more than 100 distributed telescopes. Its cameras record images of gamma rays when they penetrate the atmosphere. Each camera is composed of several photo sensor modules that are able to capture and digitize Cherenkov light. The data obtained from the sensors must be transmitted to a central server. However, the needed data bandwidth is very high because of the number of sensors. The proposed solution offers an aggregation mechanism capable of joining data from sensors to a single 10G port. The utilization of the 10G is motivated by the technological evolution of other scientific instruments [88] and the progress of the commercial wired a wireless networks with higher bandwidth every day [89]. Our proposal also considers the control and management packets that require a fully configurable routing design. To perform this, some components have been introduced to check the MAC address for each packet

and, thanks to a routing table, deliver it to the proper destination. Although these features are included in some TSN devices and high performance switches [90, 91], they are very expensive. Consequently, our solution is implemented using flexible FPGA devices that provides a cost-effective alternative.

4.2 Cherenkov Telescope Array

CTA [9] is an international project whose main goal is to explore the universe in the gamma rays energy region (20 GeV - 300 TeV). It will be an order of magnitude more sensitive than current Imaging Atmospheric Cherenkov Technique (IACT) applications [92] that operate at the same energy segment. CTA is divided into two telescopes array (Fig. 4.2) regions: Paranal (Chile) and La Palma (Spain). These locations have been evaluated using Monte Carlo simulations [93] to check the impact of different factors such as altitude, night-sky background and local geomagnetic field. Each telescope array is composed of several telescopes which are classified in three types depending on the energy range that are able to measure: Large Size Telescope (LST), Medium Size Telescope (MST) and SST.

FIGURE 4.2: CTA Telescope. This picture has been extracted from [9].

CTA uses the IACT to measure cosmic rays by capturing the few nanoseconds long Cherenkov light flashes. They are emitted in air showers when the gamma rays reach the Earth's atmosphere. The direction of the Cherenkov light cone, when recorded with multiple telescopes, allows for the detection of the origin of the primary gamma ray in the sky. On the other hand, the light intensity is a measure of the primary gamma-ray energy. IACT telescopes are equipped with large tessellated mirrors that concentrate the Cherenkov light onto the camera with several photo sensors. They are read out by fast electronics which provide nanosecond sampling. This time precision allows to distinguish gamma rays from charged cosmic rays that hit the atmosphere much more numerously, and therefore contribute most to the background measured by IACT telescopes. Cosmic-ray air showers are on average broader, less symmetric, and have more irregular timing footprints. Moreover,

precise time information result in optimum energy and direction reconstruction performance. Consequently, precise timing is mandatory for CTA and the required relative timing precision between different cameras is constrained to 2 ns on average with less than 1 ns Root Mean Square (RMS) jitter. On the other hand, the absolute timing precision must guarantee a 1 μs. Just to compare the magnitude of the synchronization requirements, in other systems such as the Hitomi satellite [94], a 35 μs is demanded for proper operation and in SKA telescope a nanosecond range synchronization is also needed [95].

The Gamma-ray Cherenkov Telescope (GCT) is a consortia whose main goal is to provide the SSTs as an in-kind contribution to the Cherenkov Telescope Array Observatory (CTAO). The prototype for the SST is called the CHEC (Fig. 4.3) that is in charge of measuring and digitizing the sky stimulus and send data to a server in order to process it. The CHEC [96] is composed of 2048 pixels distributed in 32 Front-end Electronic (FEE) modules, also known as TeV Array Readout Electronics with GSa/s sampling and Event Trigger (TARGET) modules; the Backplane board, two DACQ boards, the Uniform Clock and Trigger time Stamping (UCTS) board and auxiliary system like cooling, calibration and safety systems. Each FEE contains a pixalated photo-detector that is responsible for capturing the Cherenkov light information and transmit it to the Backplane via the front-end buffers and the Application Specific Circuits (ASICs) inside TARGET modules [97]. The backplane is a PCB board that allows the communication between the 32 FEE modules and triggers the UCTS board for absolute timestamps for the different types of camera triggers. In this contribution, the authors propose a solution to replace the two DACQ boards of CHEC with one single board, called XDACQ board. It receives serial data from the FEE modules through the backplane via two SAMTEC connectors and provides 36 GTX serial transceivers at 1 Gbps. The DACQ implements a high-bandwidth data aggregation mechanism to transfer the FEE data and trigger information from the different GbE links in the backplane to a processing server through a high speed interface based on 10G port. It also includes a routing mechanism to the control packets from the server to the FEE modules. Moreover, the XDACQ board takes into consideration redundancy issues thanks to a second 10G SFP+ connector. The 10G technology has been required to transmit the high amount of data generate at the CTA telescope, as described in other contributions such as [98] and [99].

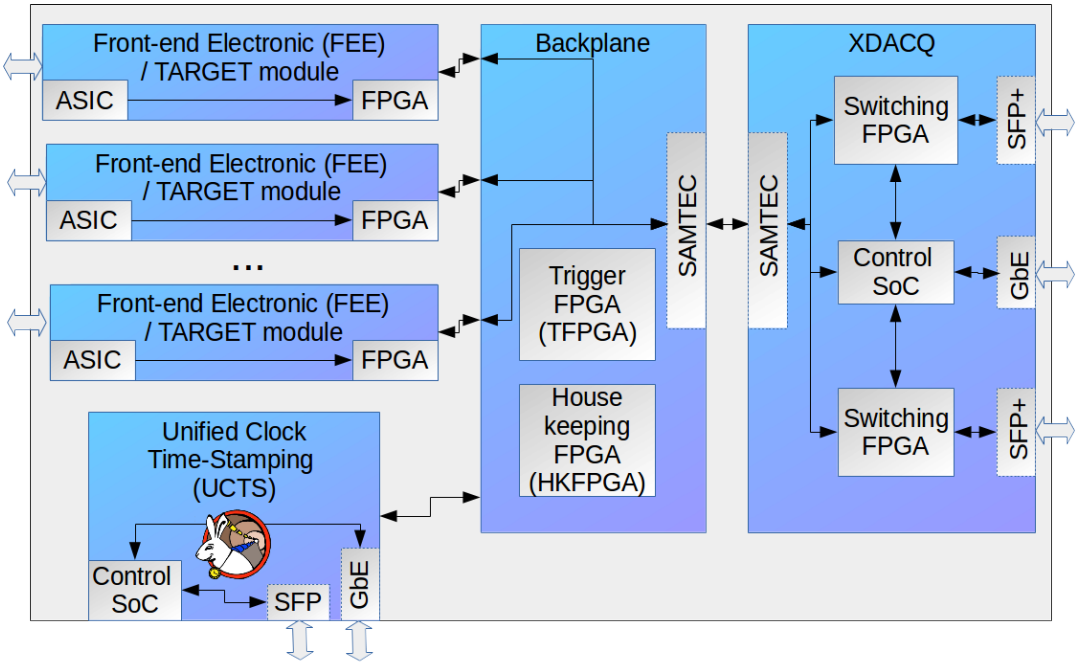

FIGURE 4.3: Schematic overview on the data path and trigger relevant components of the CHEC. It is composed of TARGET modules, the backplane board, the UCTS board and the XDACQ. The latter is the platform where the data aggregation and routing capabilities must be implemented.

4.3 Proposed DACQ system design

This section describes the implementation of the proposed DACQ system: the aggregation and routing mechanisms.

4.3.1 DACQ system requirements

The CHEC architecture demands a custom data aggregation and routing systems capable of implementing data transmission between the different 32 FEE modules and the processing server with a expected bandwidth that goes from 2.6 Gbps up to 5.1 Gbps. Under this context, it is clear that a 10G interface is able to deal with this requirement and even leave some bandwidth margin for future applications.

The input ports of the DACQ system are located at the SAMTEC connectors. Each of them is composed of several 1 GbE channels that must be aggregated to reach a single 10G interface. One important thing to note is that the aggregation path must be ready to receive high bandwidth transactions from different FEE modules at the same time. Therefore, the DACQ system should provide buffering memories to guarantee no data lost or corruption. On the other hand, the DACQ system must offer configurable routing capabilities in order to allow the processing server to control and monitor the status of the different modules of the CHEC. Moreover, it must implement redundancy mechanisms which requires the presence of a second 10G port. With this configuration, one of the 10G interfaces is active and the other is

configured in backup mode. In case of failure or user actuation, the backup interface can be converted in the active one re-establishing the communication.

Because the CHEC has specific and custom requirements such as physical interface connectors, very compact design and the asymmetric data flows, it is not an easy task to find a suitable commercial device for it. Under these circumstances, the XDACQ board has been proposed as candidate to implement the DACQ system. It has been specifically designed to be integrated in the CHEC and provides an hybrid architecture based on a Zynq SoC and two Ultrascale FPGA devices. Its hardware architecture provides a general framework to apply co-design techniques partitioning properly hardware components and software elements. The former are included as IP cores that can be synthesized inside the FPGA devices while the latter runs in the hard microprocessor inside the SoC taking advantage of the software flexibility. The data aggregation path asks for high bandwidth and buffering memory elements that can not be faced easily in software. For this reason, this part is implemented using IP cores to fulfill the CHEC requirements. Contrarily, the routing path demands fully configurable mechanisms that are not easily afforded in hardware. Then, a basic RTU IP core is implemented in the FPGA device that redirects each packet depending on its destination MAC address. However, the configuration, update and control of the RTU module is performed by software in sake of providing a flexible routing system.

4.3.2 XDACQ

In this part, the XDACQ board is described considering its hardware architecture, proposed gateware design and implemented software.

Hardware

The XDACQ (Fig. 4.4) is a new board that has been designed to be integrated into the CHEC. It is composed of one Zynq SoC (xc7z015clg485-1) and two Kintex Ultrascale FPGA devices (xcku040-ffva1156-1-c). The SoC contains an ARM Cortex-A9 dual core microprocessor and a FPGA chip with 74000 logic cells, 3.3 Mb RAM and 4 high speed transceivers. This SoC is in charge of controlling and monitoring the rest of components of the DACQ system. The Ultrascale FPGA devices are programmable devices with with 530250 logic cells, 21.1 Mb RAM and 20 high speed transceivers whose main goal is to aggregate all the traffic from the FEE modules (SAMTEC connectors) to the 10G port and provide configurable routing interconnections in the opposite direction. Moreover, the XDACQ board incorporates two 10G ports that enable the implementation of redundancy mechanisms as discussed previously. It also has two SAMTEC sockets with 18 1 GbE interfaces each, a control Serial Peripheral Interface (SPI) interface, three USB connectors for debugging the different FPGA devices and a control standard 1 GbE port for the Zynq device.

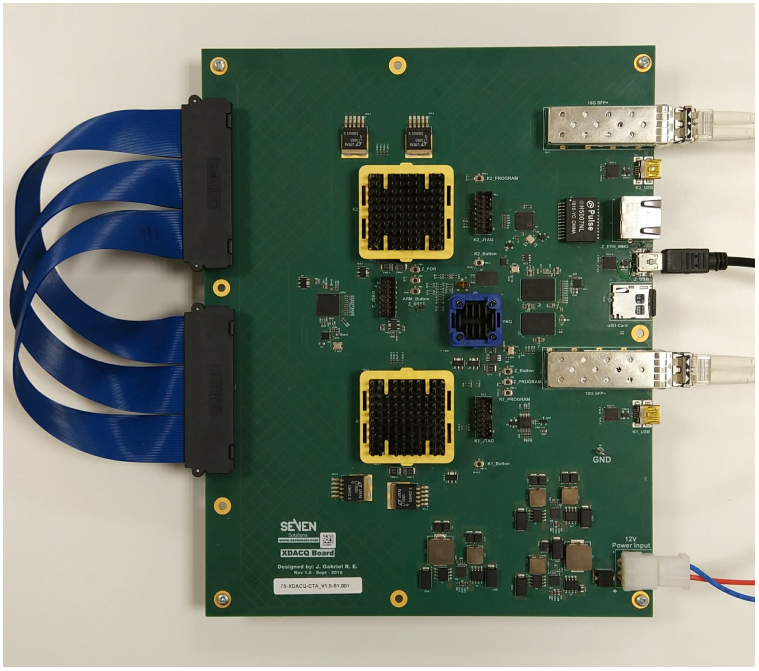

FIGURE 4.4: The XDACQ board. It contains two different kind of devices: Kintex Ultrascale FPGA chips and Zynq SoC. The former provide buffering enough memory for the data transfer mechanisms. The latter is in charge of controlling and monitoring the entire system and to route the trigger information to the Kintex Ultrascale chips. The SAMTEC connectors to the left (here interconnected for test purposes, see text) are nominally used for the downlink to the further camera electronics.

Gateware

The XDACQ FPGA firmware (gateware) is represented on a block diagram of Fig. 4.5.

The main block design is divided into two different parts: the Zynq gateware and the Kintex Ultrascale one. The former is composed by five subsystems that are handled by the ARM microprocessor inside the SoC as shown in the Fig. 4.6.

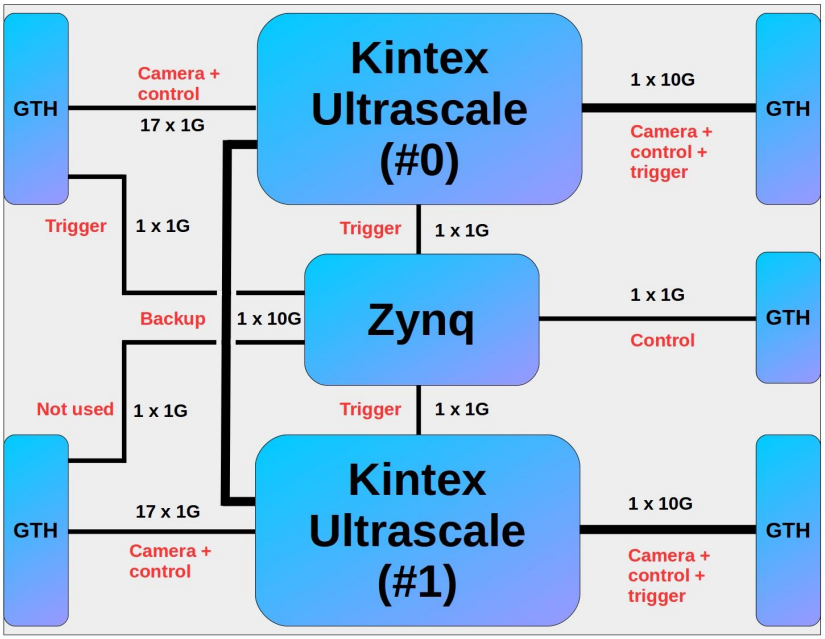

FIGURE 4.5: The XDACQ board architecture. The XDACQ is composed of two FPGA devices and a SoC. Some routing and aggregation mechanisms must be provided in order to process the different packets. Some of them come from the FEE modules and must be aggregated and re-directed to the 10G interface. In addition to that, control packets can reach the 10G port and must be routed to a specific FEE module. Moreover, the Zynq device is able to send some control packets to FEE modules. It is possible thanks to the Aurora 8b/10b protocol that allows to share a high speed link to send control packets and write directly to the Kintex Ultrascale registers using AXI commands. The XDACQ board also includes an advanced backup mechanism between the two Kintex Ultrascale FPGA devices.

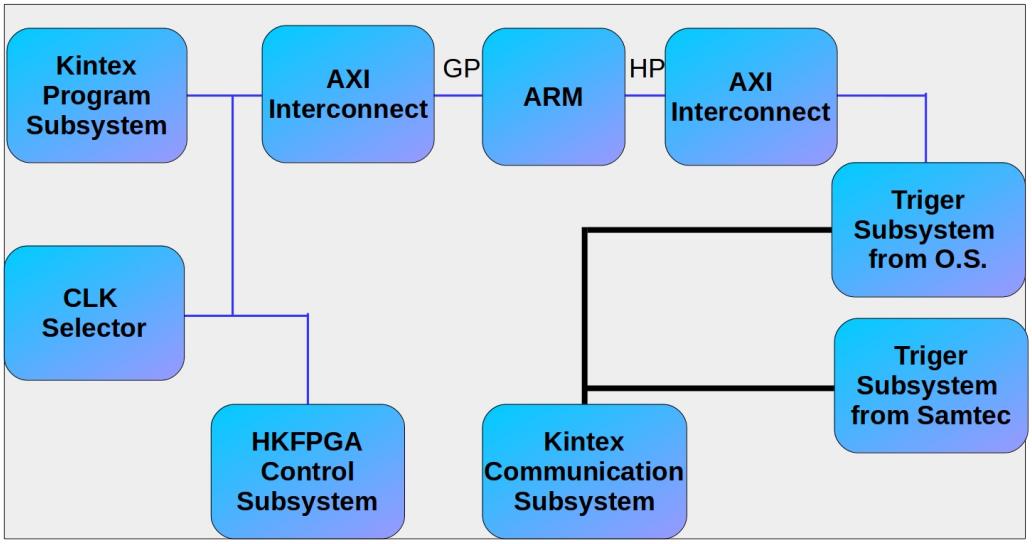

FIGURE 4.6: The Zynq gateware design. The main functionalities are the Kintex Ultrascale FPGA programing, reference clock selection mechanism, the trigger re-direction capability and the communication modules with the backplane and the Kintex Ultrascale FPGA devices.

In the following lines, main blocks of the Zynq gateware are discussed:

- The **Kintex Program Subsystem** is responsible for programming the Kintex Ultrascale FPGA chips with a specific bitstream specified by the user. The default bitstream contains all the elements required by the aggregation and routing systems.
- The **Backplane Control Subsystem** provides control mechanisms for the Backplane FPGA devices: House-Keeping and Trigger ones through a SPI interface.
- The **Kintex Communication Subsystem** implements a communication channel between the SoC and Kintex Ultrascale FPGA chips. It meets two different purposes: remote memory mapped access to configure the registers inside the Kintex Ultrascale FPGA devices and trigger packet bypassing from the SAMTEC connector to the aggregation system. Two IP cores have been implemented to establish this channel: Hub and Splitter. The former adds some headers to the data transmission in order to distinguish between control transactions and trigger packets. The Splitter core is in charge of reading the header information and route the data accordingly. The physical implementation of the channel has been performed using the Aurora 8b/10b protocol.
- The **Trigger Subsystems** receives trigger packets from OS or the SAMTEC and re-direct them to the **Kintex Communication Subsystem**.
- The **CLocK (CLK) Selector Subsystem** selects the Kintex Ultrascale FPGA chips input clock from an internal or external source.

The Kintex Ultrascale gateware accomplishes the two main tasks of the DACQ system: data aggregation and routing. These FPGA devices have 17 1 GbE links each from SAMTEC connectors. Through them, data and control packets are exchanged between the different modules of the DACQ system and the processing server. The Kintex Ultrascale gateware is composed of three subsystems:

- The **Switching Subsystem** is responsible for aggregating and routing all the data for the DACQ system.
- The **Remote Control Subsystem** is the counterpart of the **Kintex Communication Subsystem** for the Zynq gateware. It is dedicated to receive control commands to read/write registers and trigger packets from the Zynq SoC.
- The **10G Backup Subsystem** implements the functionalities regarding the backup configuration and the communication between two Kintex Ultrascale FPGA chips. Due to each Kintex Ultrascale FPGA device has one 10G port and only one of them is active at the same instant, the FPGA with the port in backup mode must bypass packets to the other Kintex Ultrascale FPGA device in order to reach the active port. In case of failure or by user demand, the backup port will become in the active one avoiding link interruption.

The detailed block diagram of the Kintex Ultrascale gateware is represented in the Fig. 4.7. It includes several 1 GbE endpoints as many as channels of the SAMTEC connectors, two 10G components for the SFP+ ports, a switching core and an Aurora 8b/10b module for communication with the Zynq SoC. The switching core is a complex component that implements the aggregation and routing paths dealing with the data and control packets. The former receives data from the 17 ports from SAMTEC

connector. Then, these packets are stored into FIFO queues until the Advanced Extensible Interface-Stream (AXIS) Switch is ready. When it is ready, packets are bypassed to the local 10G port if it is in active state or to the other Kintex Ultrascale FPGA device if it is in backup mode. The latter, routing path, receives packets from the 10G ports and store them into two FIFO memories. Then, they are transmitted to another AXIS Switch module that bypasses them to the Router core. The router core implements a RTU module that is able to catch the MAC address from each packet, search in a Content Addressable Memory (CAM) to find the proper destination and append some additional information to allow other components to route the specific packet properly.

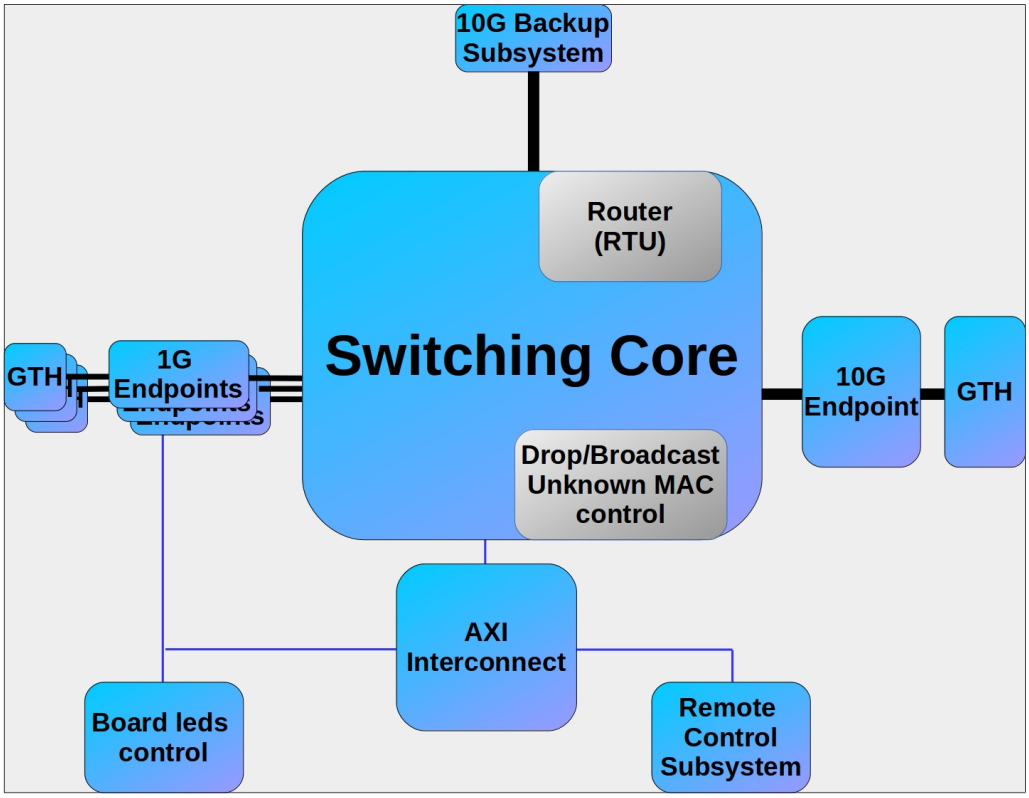

FIGURE 4.7: The Kintex Ultrascale gateware design. It contains several Endpoints for the 1 GbE links in the SAMTEC connectors, a switching core that aggregates and routes packets, two 10G endpoints (one of them for backup configuration) and some modules to control the Light-Emitting Diodes (LEDs) in the board and to receive information from the Zynq SoC.

Software

The XDACQ board requires some additional software to work properly. It has been designed to run in the ARM microprocessor inside the Zynq SoC. This processor executes a Linux environment which enables to use standard applications and, at the same time, simplifies the software development task. In the following lines, the five software elements are briefly described:

- The **Xilinx Ethernet Subsystem Configuration** configures the 1 GbE and 10G endpoints registers to enable the transmission, reception and Jumbo frames.

- The **Statistic Driver** is a Linux driver that retrieves the endpoint statistics and shows them via ifconfig shell command.
- The **RTU configuration** is responsible for initializing/updating the RTU CAM contents when the Linux OS starts up.
- The **Backup configuration** is in charge of enabling/disabling the backup function and configures its mode (automatic or manual for user intervention).
- The **Clock input configuration** configures the input clock to use an internal or external source for the Kintex Ultrascale FPGA devices.

4.4 Experiments and results

In this section, we provide some tests to demonstrate that the developed system fulfills the CHEC requirements. The first part shows the resource utilization meanwhile the second one evaluates the system performance.

4.4.1 Resource utilization

As discussed in the section 4.3, the system requires two different gatewares: one for the Kintex Ultrascale FPGA devices and another for Zynq SoC. The utilization report of Kintex FPGA chips is presented in the Fig. 4.8. As we could expect, this design requires several Block Random Access Memory (BRAM) instances dedicated to build the FIFO elements for buffering purposes in the aggregation and routing path. Moreover, all the Gigabit transceivers are used to connect all the links coming from the SAMTEC connector, SFP+ port and the Aurora 8b/10b communication channel. However, the overall utilization is not so high in terms of Look-up Table (LUT), Flip Flop (FF) and Look-up Table as Random Access Memory (LUTRAM) primitives. It means that the Kintex Ultrascale FPGA device has enough logic resources to implement future functionalities if needed.

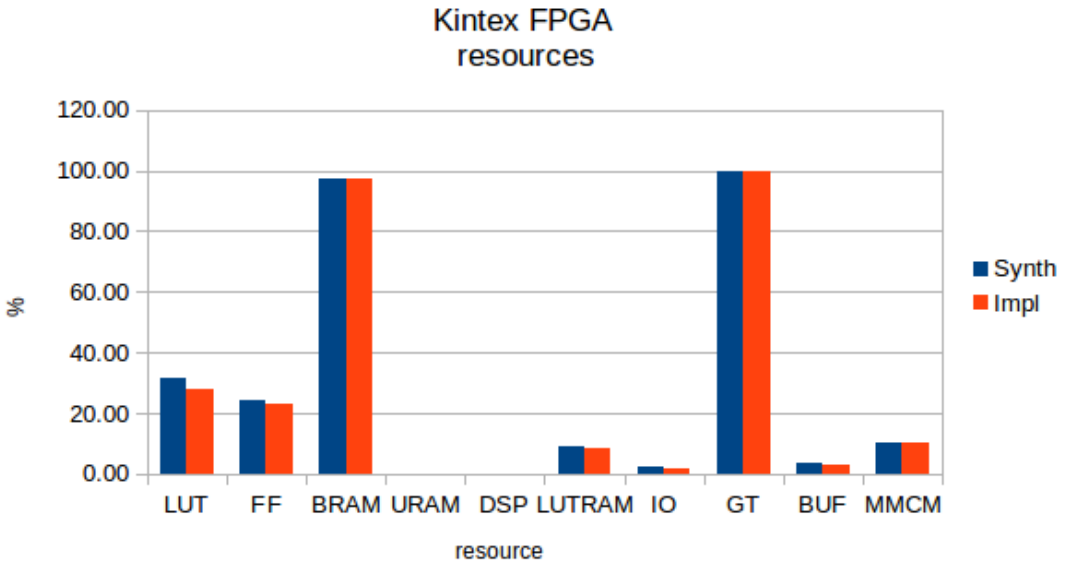

FIGURE 4.8: Kintex FPGA resource utilization report. It shows that all the Gigabit Transceivers are used and practically all the BRAM available for the FIFO components of the aggregation and routing implementation. The high utilization for the BRAM avoids the packet loss when several packets arrives at the same time from different FEE modules.

On the other hand, the utilization report of the Zynq SoC is shown in Fig. 4.9. As expected, the resource needs are different than the Kintex Ultrascale's ones. In this case, the Gigabit transceiver, the PLL or Mixed-Mode Clock Manager (MMCM) primitives and the clock buffers are the most required blocks for the current design, albeit some free logic elements are available for future developments.

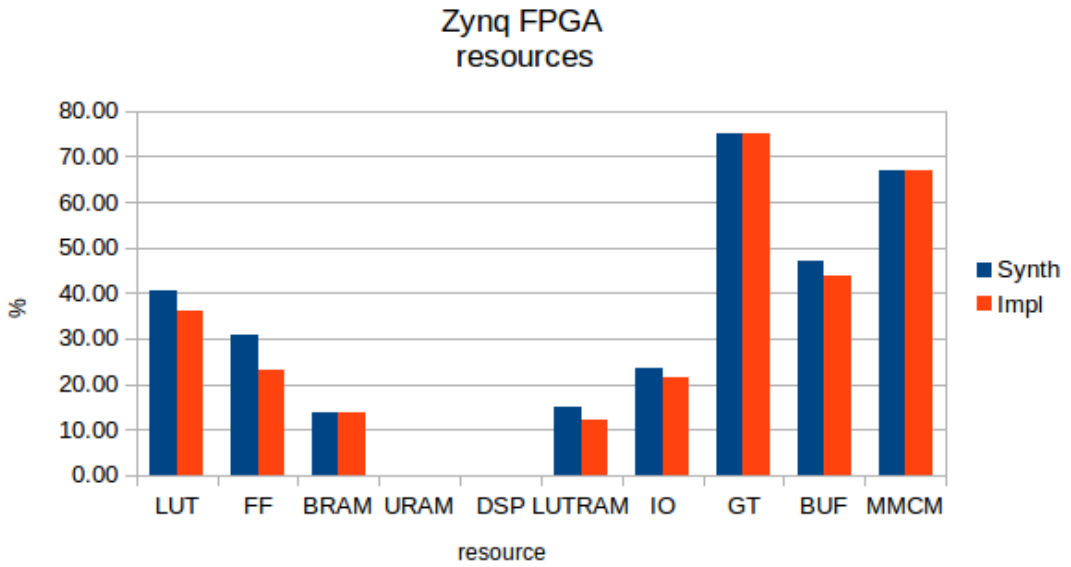

FIGURE 4.9: Zynq SoC resource utilization report. This design fits very well in the current platform and there are available resources to implement advanced features if needed.

4.4.2 Performance evaluation

The system performance evaluation is an important task to ensure that the DACQ system fulfills the specific CHEC requirements. It focuses on obtaining the DACQ system bandwidth and latency. To accomplish this, all interfaces of the XDACQ board must be tested to validate the entire design. There are several approaches to perform system tests. The first one is the utilization of a conventional computer, albeit these devices normally are limited by their number of physical interfaces. It makes hard the testing process because the high number of XDACQ ports. Other alternative is placing an advanced switch or router. However, it is very expensive due to it must fulfill the CTA interconnection requirements. To overcome the previous inconveniences, a custom solution has been developed: a traffic generator system is programmed in one of the Kintex Ultrascale FPGA devices and the other one is the Device Under Test (DUT) for experiments. The traffic generator system is fully configurable and allows to replicate the behavior of the FEE modules producing packets bursts from different interfaces at the same time. In addition to the FPGA development, a crossed SAMTEC cable is required to establish communication between the two Kintex Ultrascale FPGA chips.

The traffic generator design is based on the AXIS Traffic Generator IP [100] from Xilinx and a custom module that calculates the checksum of every packet and stores some packets statistics. This architecture is able to generate high-bandwidth packet patterns using only one AXIS Traffic Generator and an AXIS Broadcaster IP which replicates each incoming packet to reach all the 1 GbE interfaces contained on the SAMTEC socket. The Fig. 4.10 shows the basic scenario for the performance experiments. Data are received on the PC side through an Endace DAG 10X2-S Network Controller [101] and the bandwidth metrics are calculated using the nload tool [102].

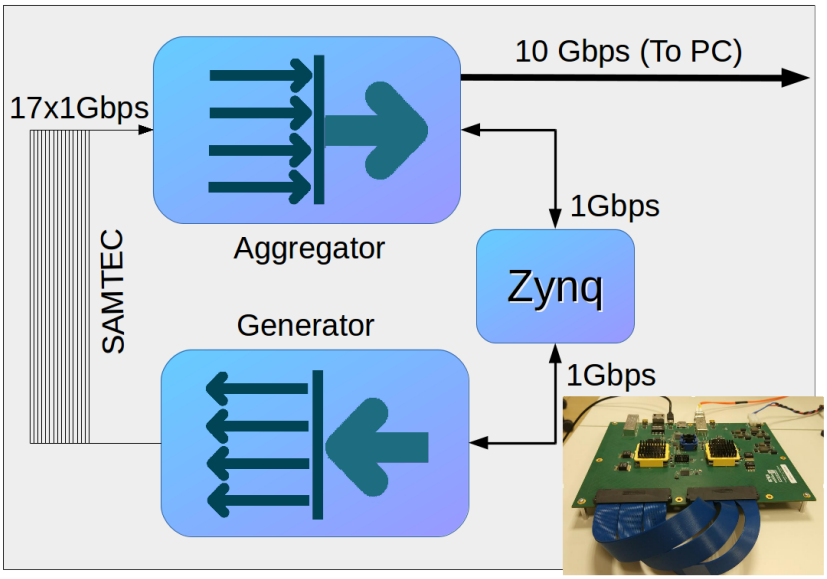

FIGURE 4.10: A Kintex FPGA device is configured to generate several packets through the SAMTEC connection. On the other side, the second Kintex FPGA device receives and pass them through the switching connector to reach the 10G port.

The XDACQ system has been evaluated on different conditions to guarantee that it is able to cope with the CHEC requirements. The first experiment exposes the

system behavior when several interfaces from SAMTEC are used at its full capacity. The obtained results are presented in the Fig. 4.11 where the independent variable is the number of active interfaces at the same time for different packet sizes: 1500, 4500 and 9000 bytes. This experiment reveals that the system is able to operate at the 92.9% of the 10G total capacity.

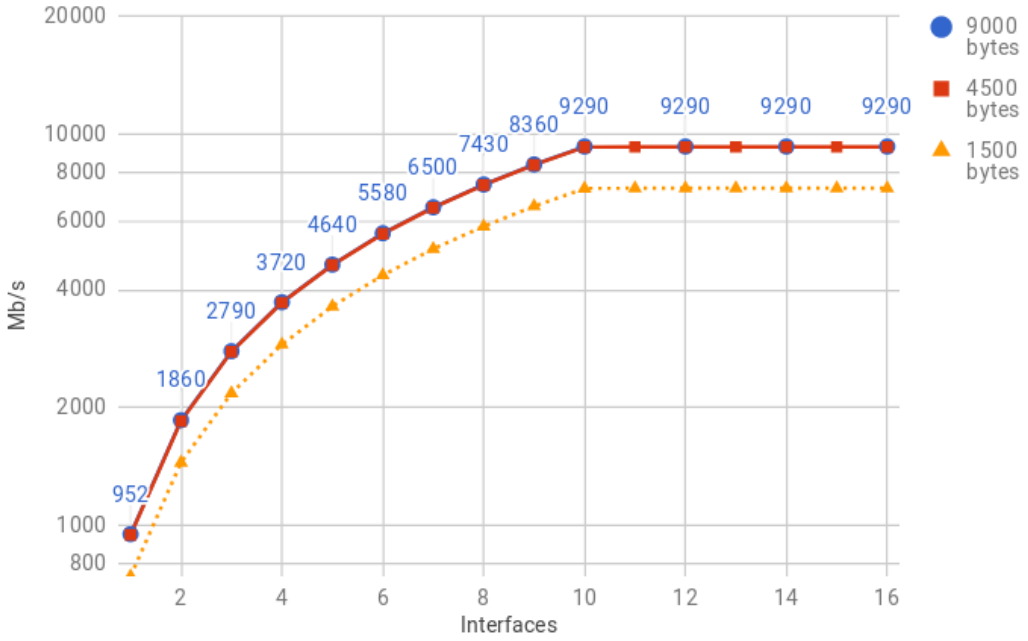

FIGURE 4.11: System bandwidth with different packet sizes and several interfaces transmitting at the same time. It shows that the system is able to cope with the maximum 10G bandwidth (10 interfaces at the same time).

The second test scenario is focused on measuring the data bandwidth limit when all the SAMTEC interfaces are activated at the same time. Under these circumstances, the independent variable is the data bandwidth per interface. The results are summarized in the Fig. 4.12 that shows a mostly perfect fit between the system performance and the theoretical one. Moreover and, as would be expected, the output interface is limited by the 10G capacity and the XDACQ system performance can be reduced dramatically if a high bandwidth condition exceeds this limitation for a long time period. To avoid this issue, the XDACQ aggregation system implements an advanced FIFO control mechanism that enables the bandwidth to remain constant even though under high demanding conditions (Fig. 4.11 and Fig. 4.12)

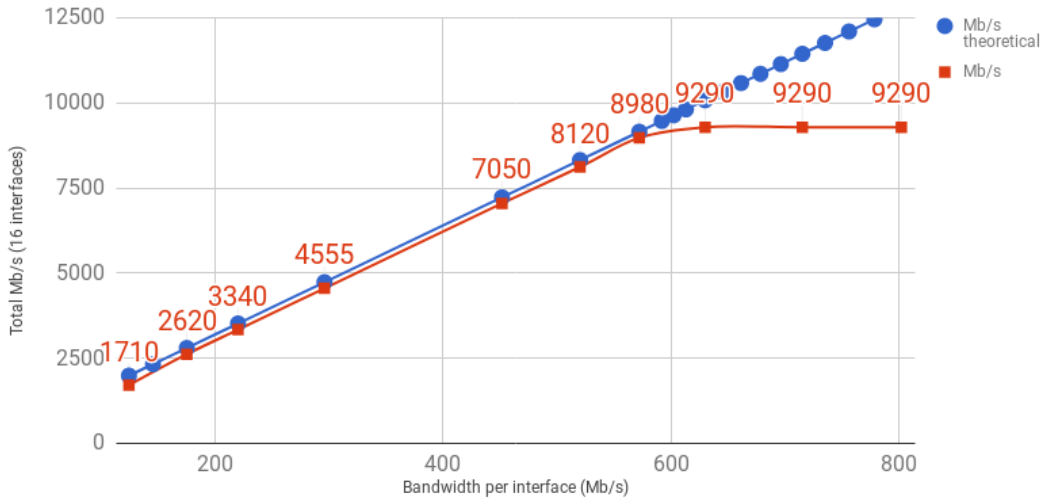

FIGURE 4.12: comparison of system performance with theoretical bandwidth expectations. For bandwidth larger than 600 Mbit/s per interface the system is able to use the 92.9% of the 10G link capacity.

Other key factor of the XDACQ system that must be characterized is the routing latency and, specially, the delay introduced by the RTU module. The RTU IP core has been evaluated on high bandwidth conditions to ensure the isolation between the control and data path. To demonstrate this, the control path latency should remain constant and should not be affected by the aggregation system activities. The first step is the RTU characterization in terms of latency. The Fig. 4.13 shows that it is deterministic and, therefore, it does not introduce any penalty in the routing path. Furthermore, the dedicated design of the RTU module does not include any memory element to hinder the packet traffic. Consequently, it can be placed at high bandwidth paths although it is not strictly required by CTA.

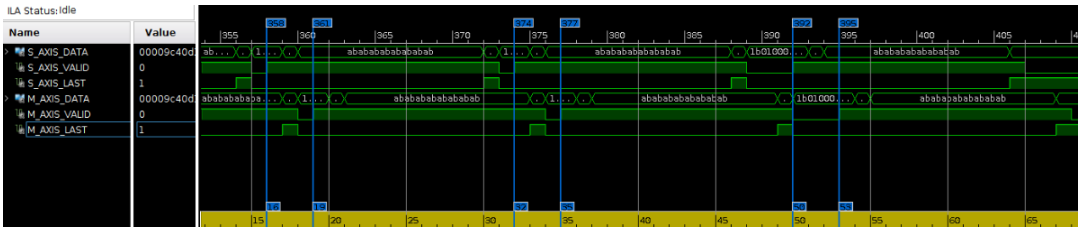

FIGURE 4.13: The information contained in this picture has been obtained using the Vivado logic analyzer IP so it represents real condition in a working system not a simulation waveform. It shows a burst of three packets and demonstrate that the RTU module always presents a fixed latency of 3 cycles thanks to its optimal design.

Once characterized the main routing component, the overall routing latency has been measured (Fig. 4.14). The results demonstrate that the routing latency does not depend by network activity and prove the isolation between the aggregation and routing paths.

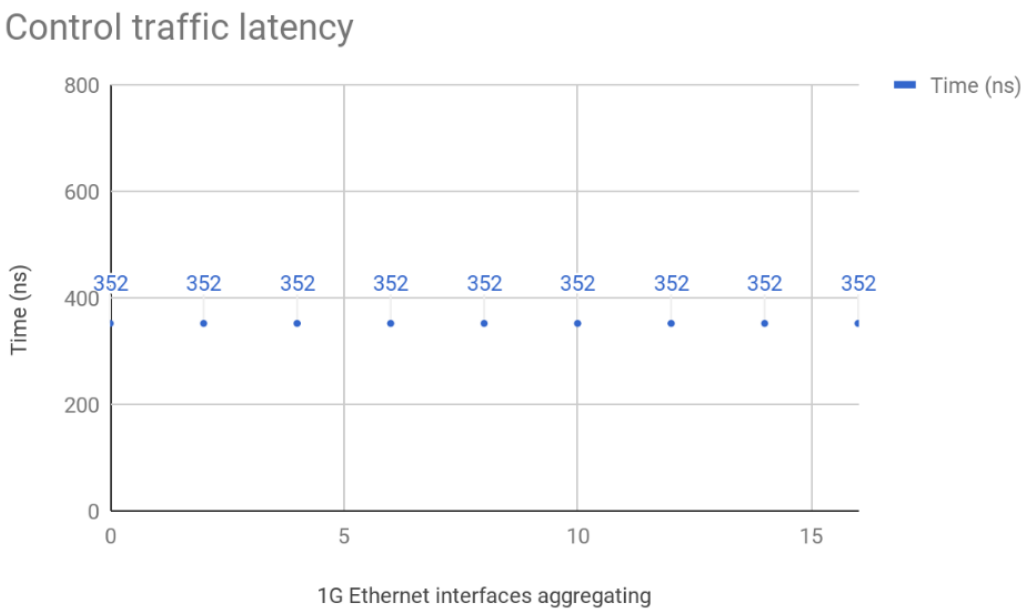

FIGURE 4.14: Latency test for the control flow through the RTU module while the aggregation mechanism is active. The figure illustrates the latency behavior for the control packets that is not affected by the aggregation logic in the system. It demonstrate that the data packet flow and the control one are properly isolated.

Lastly, the XDACQ board is currently being integrated in the CHEC camera prototype (see Fig. 4.15), and several integration tests have been already successfully performed on DESY [103].

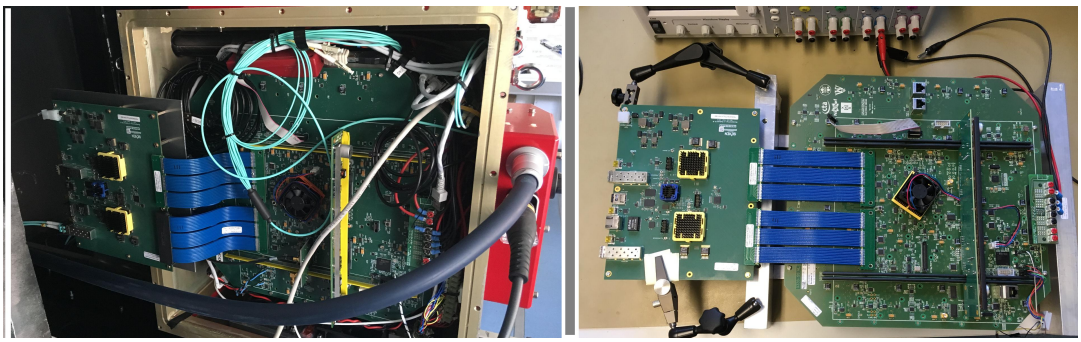

FIGURE 4.15: Integration and validation of the XDACQ board on the CHEC camera.

4.5 Final remarks

The present chapter describes an asymmetric network architecture that is suitable for being deployed as a cost-effective and flexible solution for DACQ systems. In these kind of systems, there are two different and separated traffic flows: high bandwidth data and low bandwidth management ones. The former is normally in charge of aggregating several sources into a high bandwidth output channel while the latter implements a flexible and fully programmable system that is responsible for routing incoming packets to reach different output interfaces depending on certain criteria (e.g. MAC destination address). Each traffic flow requires specific features that are

incompatible ones sometimes. Therefore, it is a hard task to find commercial devices that fit with the specific project needs.

Under this context, the proposed architecture has been integrated on the DACQ system for CTA project using the XDACQ board. This new platform has been developed specifically for CTA and its hardware is composed of two FPGA devices and a Zynq SoC interconnected by a high speed bus based on Aurora 8b/10b technology. The FPGA chips include the building basic blocks such as memory elements, high speed transceivers and LUTs for the aggregation and routing systems. On the other hand, the Zynq SoC supervises the system behavior performing control tasks such as RTU maintenance, FPGA programming and diagnostics among others. In addition, the utilization of a Linux OS running on Zynq SoC easies the development phase, while at the same time presents a friendly and standard interface to the users.

The XDACQ platform has been evaluated by means of several experiments. Some of them are dedicated to measure the system bandwidth performance. Their results demonstrate that XDACQ board is able to handle up to 9.29 Gbps and its bandwidth is not degraded under extraordinary conditions over the 10G capacity. Other experiments have been characterized the routing system latency and the properties of its main element: the RTU module. As a result, the RTU core offers a deterministic latency and its design is suitable for high bandwidth paths without introducing any penalty. Moreover, the isolation between the aggregation system activity and the control path has been demonstrated because of management packets latency is not affected by high bandwidth data network conditions. These evidences bring to light that the XDACQ system is capable of fulfilling the CTA requirements and, at the same time, is flexible enough to be deployed on others DACQ systems.

Last but not least, there are some future work lines that must be remarked to improve the current system:

- Implement advanced traffic control mechanism enhancing the existing one. It is required to detect anomalous bandwidth conditions and provide alarm signals to the software for monitoring purposes.
- Improve the Aurora 8b/10b channel to enable a full duplex communication. It allows the access to the Zynq SoC from the 10G port.
- Enhance the current asymmetric architecture to provide static routing and fully programmable aggregation services.
- Migrate the current design to higher bandwidth interfaces such as 25 Gigabit Ethernet (25G) ones.

Chapter 5

High performance WR links for 10G interfaces

"The way to succeed is to double your failure rate."

– Thomas J. Watson

Contents

The present chapter analyzes the WR drawbacks in relation to the interoperability. The main issue is that current version of WR devices only work with 1 GbE networks. This fact reduces dramatically its integration for some applications because many of them require a high data bandwidth network link with, at least, 10G capacity. Consequently, they can not benefit from the WR solution. In this chapter, we have implemented a WR design that is able to be deployed in 10G infrastructures overcoming the initial limitation. In this line, we have developed a new solution that combines the proposed SoC design presented in the section 3 with the asymmetric network DACQ system described in section 4 into an unified architecture. Consequently, it is able to provide high data bandwidth services together with high accurate synchronization mechanisms. In addition to that, we have evaluated our proposed system in regards of time synchronization and data performance. The results indicate that the new WR 10G system is able to handle high data rates close to 10G capacity and, at the same time, presents a time synchronization performance comparable to WR standard implementations in terms of time accuracy and frequency dissemination. Under this context, Seven Solutions has been actively supporting the development of the WR 10G solution.

This chapter is divided into four sections. Section 5.1 shows that there are many scientific and industrial applications with strict time requirements for which WR would be a perfect candidate respecting time synchronization performance. However, it can not be used because of an interoperability issue. They usually require network links with more data bandwidth than 1 GbE ones. Section 5.2 presents a brief review about the 10G technology. Section 5.3 describes the new WR 10G design taking into account several aspects such as hardware platform, FPGA design and developed software. Section 5.4 shows different test cases to evaluate time synchronization performance, data bandwidth and latency of the proposed solution. Finally, section 5.5 exposes final conclusions and most promising future work lines.

5.1 Motivation

As discussed in chapters 2, 3 and 4 the time synchronization is a very important topics for many application in the Information Technology (IT) age. Some examples of them are first-level scientific facilities such as particle accelerators (CERN [104] and IFMIF [4, 81]) and telescopes arrays (CTA [9] and SKA [9]) among others. The telescope arrays user cases have been covered on detail in chapters 3 and 4 for SKA and CTA respectively. On the other side, there are many industrial infrastructures in different market sectors that demand high accurate synchronization as one of their key features. The main industrial applications are focused on telecommunication, Machine-to-Machine (M2M), smart grids, finance [105], data centers, IoT and new generation networks [106].

On the smart grid systems, synchronophasor data are time sensitive and, therefore, a very accurate synchronization is required to timestamp interesting events precisely. The timing information must be transferred to the PMU using reliable mechanisms [107]. Under this context, the IEEE C37.118 standard states that a requirement of 1 μs is needed which can be obtained using GNSS sources. Nevertheless and, as stated in [108], the accuracy of the time synchronization must be improved about ten times from the original requirements in order to provide an extra time budget for other error sources. Taking into consideration the new synchronization requirements, the GNSS reference are not good enough in terms of accuracy and traceability to be deployed on smart grids networks.

The synchronization is also an important factor for Fronthaul network system in telecommunication infrastructures. Typically, the SDH is used to provide a time synchronization scheme based on time multiplexing. It creates several time slots that can be assigned to different resources. In the Third Generation (3G) and LTE current mobile network, a microsecond scale synchronization is required for the different neighboring base stations [109]. In this scenario, a GPS must be connected to each base station, meaning a very expensive solution to reach the timing accuracy. Moreover, the GPS suffers from some issues such as spoofing, jamming, reduced coverage and atmosphere influence. The coming 5G technologies demand an enhanced on the synchronization and, at the same time, require additional reliability and redundancy capabilities [109]. An analysis of the technology and standardization gaps are exposed in [110] and, as discussed on [35], the radio categories B to A+ impose synchronization requirements between 110 ns and 12.5 ns. As a result of sharing the same signal spectrum between multiple mobile operators, the inter-operator interferences must be considered. Under these circumstances, a time traceability mechanism is required which in turn needs a high accurate synchronization technology underneath.

For the data centers, the time synchronization is a crucial factor to ensure the proper behavior of the main functions such as data consistency, event ordering, tasks scheduling and resources sharing [41]. In order to deploy applications where time and delay notions are important factors such as finance, a nanosecond scale synchronization technology must be implemented in data center infrastructures. The software solutions are not able to provide needed synchronization performance [41] due to the lack of dedicated hardware components to timestamp packets precisely. One software example is the Huygens algorithm [41] that implements specific techniques based on SVM to estimate the one-way propagation time obtaining a better accuracy than standard solutions such as PTP or NTP. However, its accuracy is not enough for many high demanding applications. As discussed in chapter 2, there are other approaches based on the utilization of timing signals for the time distribution, albeit they requires dedicated hardware elements and, even though, a specific network development to avoid time imprecision due to unknown cable delays.

For all the applications previously described, it is possible to apply an uniform time synchronization technology. In chapter 2, optical fiber network was presented as a candidate solution to provide time information using recognized and traceable standards such as UTC or TAI [111]. In this way, there are some projects such as CLONETS [112] that intend to speed up the transfer of high accurate time and frequency synchronization technologies to industry. Under this context, standard packet protocols such as NTP [31] or PTP [32] have been proposed for time dissemination and have been deployed on specific applications such as China Mobile that uses PTP in hundreds of cities obtaining a $\pm 1.5\mu$s time accuracy, fulfilling 3G and LTE requirements [109]. Nevertheless, the previous presented applications demand a high accurate synchronization technology whose time requirement goes beyond the NTP or PTP performance. Typically, NTP only can guarantee a millisecond scale accuracy whist PTP can obtain a microsecond scale one [113]. Although PTP can improve its performance for specific LAN configuration obtaining an accuracy in the order of nanoseconds. Other alternative that has been exposed on chapter 2 is WR. It is a synchronization technology that provides sub-nanosecond accuracy that is able to overcome one of the most important topics on time synchronization: timestamp sampling resolution limitation [109]. Some contributions indicate that WR is emerging as a good candidate [114] for applications with high accurate synchronization requirements. However, WR presents a compatibility issue related to the fact that it only works on GbE networks. It reduces significantly the number of applications where WR can be deployed.

The current chapter faces the technology limitation of the WR protocol and presents a new fully compatible and modular version that is able to work on 10G networks. This solution includes an enhanced design of WR based on new SoC devices explained in chapter 3 and the asymmetric network DACQ concepts from chapter 4. Thanks to this, WR is ready to be used on many applications which were not suitable for up to now and, at the same time, applications that demand high data bandwidth requirements can benefit from high accuracy synchronization.

5.2 10 Gigabit Ethernet

The 10G technology [115, 116] was included in the Ethernet standard (IEEE 802.3ae [117]) in 2002. It has a speed of 10 Gbps and includes features for LANs, Metropolitan Area Networks (MANs) and Wide Area Networks (WANs). This section is focused on 10G over optical fibers, albeit there are some implementations that use

cooper links. The Fig. 5.1 shows the different layers for 10G alternatives. These differences are related to the PHY layer which some standards have been defined (Tbl. 5.1).

The Logical Link Control (LLC) and MAC are responsible for implementing the MAC capabilities. 10G shares the same Ethernet frame format, minimum and maximum frame size than lower speed Ethernet technologies. Nevertheless, 10G implements full-duplex only mechanism and, consequently, it does not require Carrier-Sensing Multiple-Access with Collision Detection (CSMA/CD) protocol as low speed standards. The Reconciliation Sublayer (RS) is in charge of converting the MAC data format into PHY layer data one.

Regarding PHY layer, it is composed of PCS, Wide Area Network Interface Sublayer (WIS), Physical Medium Attachment (PMA) and Physical Medium Dependent (PMD). The former defines the encoding scheme to be used. WIS provides WAN features by means of encapsulating Ethernet frames in SONET/SDH containers. PMA layer contains SerDes modules for converting serial data into parallel one. PMD layer implements the physical connection and signaling to the medium using optical transceivers in optical fiber networks.

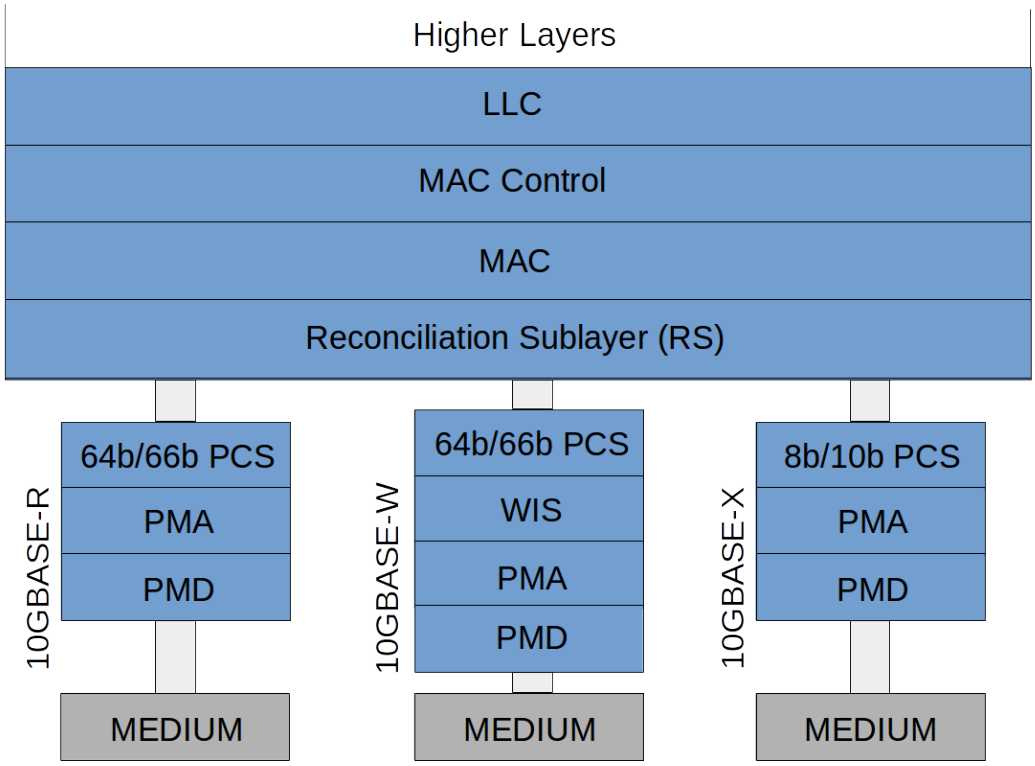

FIGURE 5.1: It shows the specific layers of the 10G technology: LLC, MAC and PHY layers. This picture has been inspired by Figure 2 from [115].

The 10G PHY layer can be classified into three different types:

- **10GBASE-R:** It uses a 64b/66b encoding scheme for the physical layer and the channel frequency is 10.3125 GHz.
- **10GBASE-W:** It uses the same physical encoding than *10GBASE-R* but also includes an additional layer known as WIS for WAN capabilities. The channel frequency for this implementation is 9.58464 GHz for compatibility reasons with the payload rate of OC-192c/SDH VC-4-64c.

- **10GBASE-X:** It uses a 8b/10b encoding scheme for the physical layer and it is composed of four independent channels using different wavelengths by means of the Wide-Wavelength Division Multiplexing (WWDM) technique. Each channel has a frequency of 3.125 GHz and the total frequency considering the four channels is 12.5 GHz. This is bigger than *10GBASE-R* and *10GBASE-W*, albeit the 8b/10b encoding scheme presents more overhead than 64b/66b one. Therefore, both of them has the same data bandwidth features.

TABLE 5.1: It shows the 10G port types for optical fibers. Most of them use 64b/66b encoding scheme and serial interfaces instead of WWDM ones.

Name	PCS	WIS	PMD	Scope	Distance
10GBASE-SR	64b/66b	No	850 nm Serial	LAN	25 - 400 m
10GBASE-SW	64b/66b	Yes	850 nm Serial	WAN	25 - 400 m
10GBASE-LX4	8b/10b	No	1310 nm WWDM	LAN	300 m - 10 km
10GBASE-LR	64b/66b	No	1310 nm Serial	LAN	10 km
10GBASE-LW	64b/66b	Yes	1310 nm Serial	WAN	10 km
10GBASE-ER	64b/66b	No	1550 nm Serial	LAN	40 km
10GBASE-EW	64b/66b	Yes	1550 nm Serial	WAN	40 km
10GBASE-ZR	64b/66b	No	1550 nm Serial	LAN	80 km
10GBASE-ZW	64b/66b	Yes	1550 nm Serial	WAN	80 km

For our 10G system, we choose the *10GBASE-R* physical implementation because of it has different alternatives depending on the specific application providing solutions for LANs, MANs and even WANs if WIS is used (*10GBASE-W*). Moreover, the *10GBASE-X* requires more hardware resources due to the utilization of four independent channels of lower speed and has more overhead because of its PCS encoding scheme.

5.3 White Rabbit solution for 10G

In this section, the WR solution for 10G network is discussed describing its hardware platform, FPGA design (gateware) and developed software.

5.3.1 Hardware platform

For the hardware platform of the WR 10G system, the WR-Z16 board (Fig. 5.2) has been chosen. It has been designed by Seven Solutions and brings a Xilinx Zynq SoC (XC7Z035) that contains an FPGA device and an ARM microprocessor inside the same chip. It converts WR-Z16 into a complete standalone platform where hardware accelerators can be implemented for critical functions and, at the same time, advanced software capabilities can be executed on a OS environment. The WR-Z16 board has 16 10G SFP+ ports, a custom clocking circuitry and some SubMiniature version A (SMA) sockets for PPS, 10 MHz input clock and 10 MHz output clock.

FIGURE 5.2: WR-Z16 board

5.3.2 FPGA design

The FPGA design or gateware presents some differences regarding the SoC-based one of chapter 3 and the WRPC one. Firstly, this architecture is fully modular and the network endpoint IP has been divided into two independent cores: MAC and PCS blocks. It easies the integration of other third-party IP cores if required. Moreover, the time synchronization related logic has been separated into a specific core known as Timing IP. It comprises the TSU modules and Timing controller. The former have been extracted from the endpoint core of the old versions. This enables a homogeneous implementation for the TSU modules whilst different network components are used.

A FPGA design overview is shown in the Fig. 5.3 and its main components are described in the following lines:

- **Processor:** It is the ARM inside the Zynq SoC. It is in charge of executing an OS and the required software tools (see section 5.3.3)
- **RAM:** It is the Double Data Rate (DDR) memory of the board. It contains the data and code needed by the processor.
- **Direct Memory Access (DMA) core:** It is responsible for handling the packet transmissions and receptions to/from the network through the 10G Endpoint and the Gigabit Transceiver (GT). This enables high data bandwidth network transactions because it performs these data operations between the endpoint and RAM without the ARM intervention.
- **10G Endpoint:** It contains the 10G MAC and PCS cores. It implements the Ethernet layer and part of the physical layer for the 10G standard.
- **GT:** It is the physical primitive that contains the SerDes and physical components for the low-level 10G physical layer.
- **Timing IP:** It contains the TSU core and the Timing controller.
  - **TSU modules:** They are able to detect the start of frame events from the SerDes data interface. It is a requirement in order to guarantee a deterministic packet latency because some network blocks (MAC and PCS) can expose variable delay. Therefore, if this effect is not considered, time synchronization performance can be degraded.

  - **Timing controller:** It is in charge of implementing the needed logic for WR protocol and is composed of similar blocks to the Real Time Subsystem (RTS) used in the FPGA gateware of the WRS.

- **Crossbar core:** It allows the processor to access the memory-mapped registers of all the components of the design.

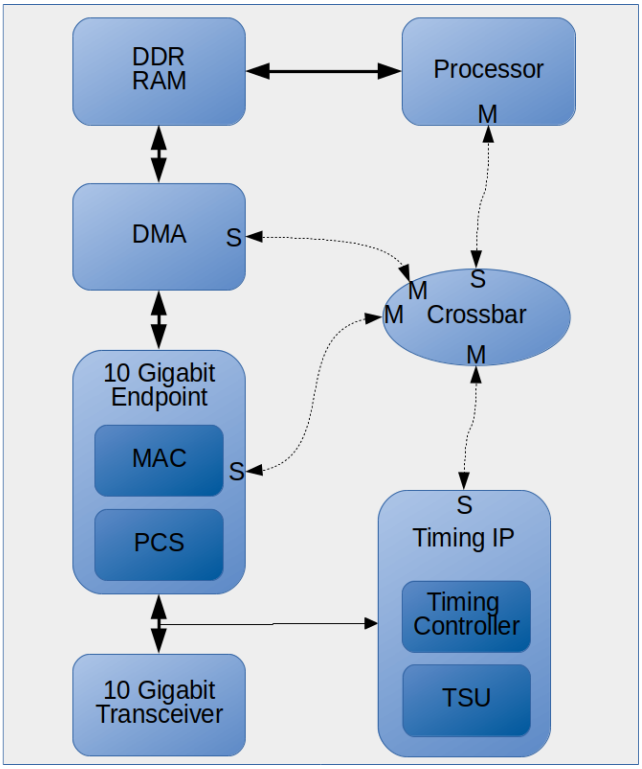

FIGURE 5.3: 10G system architecture.

In the proposed solution, the 10G MAC core [118] and 10G PCS module [119] from Xilinx are used, albeit it is flexible enough to change them in order to work with other third-party MAC and PCS cores.

5.3.3 Software

The software components are drawn in the Fig. 5.4. They are divided into different categories:

- **Userspace daemons:** They are the user applications that handle the platform by means of system calls.
  - **Hardware Abstraction Layer (HAL) daemon:** It is responsible for handing the hardware in the FPGA device and it acts as a proxy for any application that wants to access to the hardware. It introduces a performance penalty in the system but guarantees the access to the critical components of the platform.
  - **Timing daemon**: It implements the WR-PTP stack giving to the entire system a sub-nanosecond synchronization. In contrast to the WRPC/WRPC-2p-based systems, it is executed by the ARM processor and not by LM32

soft-processor. Therefore, some adaptation tasks have been performed to WR-PTP.

- **Kernel modules:** They are referred to specific source codes to be executed inside the Linux kernel. The most remarkable element is the network driver that has been adapted from the Xilinx repository to work properly with the Timing IP core and, therefore, read the high accurate timestamp for each packet.
- **Phase-control servo loop firmware:** It is an embedded software that runs in a soft-processor inside the Timing IP core. The main responsibility of this software component is the frequency adjustment by means of DACs.

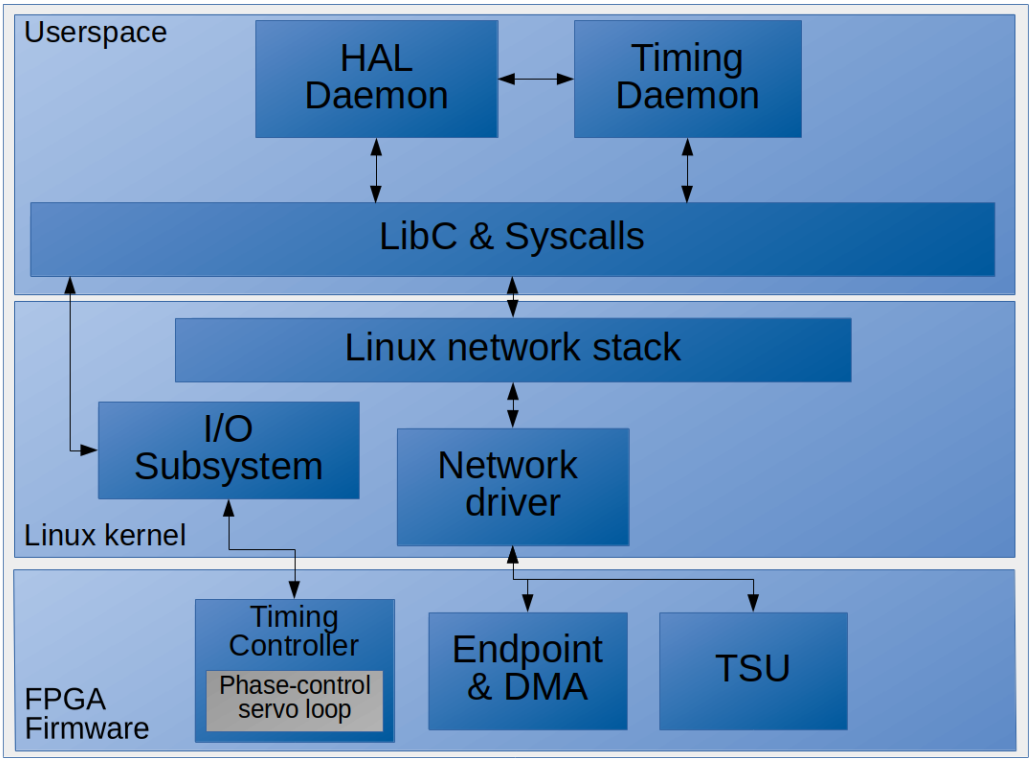

FIGURE 5.4: 10G system software components.

The proposed system has been developed from scratch taking into consideration the specifications of the WR protocol and the modifications needed by the 10G technology. This design is fully modular and its network elements such as MAC and PCS cores can be easily replaced by third-party cores. For compatibility reasons, the WR-PTP stack has been adapted to work with 10G networks instead of coding a custom one. Consequently, an industrial solution with high reliability and interoperability is achieved and, at the same time, is possible to provide this technological update to the WR community.

5.4 Experiments

Once implemented the system, some experiments must be performed in order to characterize it. The most important system features are the synchronization performance (sections 5.4.2 and 5.4.1), interoperability and a characterization in terms of data bandwidth and latency (section 5.4.3).

5.4.1 System optimization for frequency distribution

This section has been dedicated to frequency dissemination and phase noise experiments in different scenarios. The first step consists on obtaining the frequency stability of a single WR-Z16 board. To perform this, a Morion MV89 [120] oscillator is configured as GM and its 10 MHz and PPS signals are connected to WR-Z16 SMA sockets (Fig. 5.5). The 10 MHz clock is elevated to the WR-Z16 internal working frequency and uses the PPS input to track the beginning of each second. Once the internal frequencies are locked to the GM reference, the WR-Z16 generates a 10 MHz signal on a SMAs output port which is directly connected to a Microsemi 3120A [121] phase noise device. It compares the frequency reference from the Morion MV89 oscillator to the WR-Z16 10 MHz clock obtaining the frequency precision.

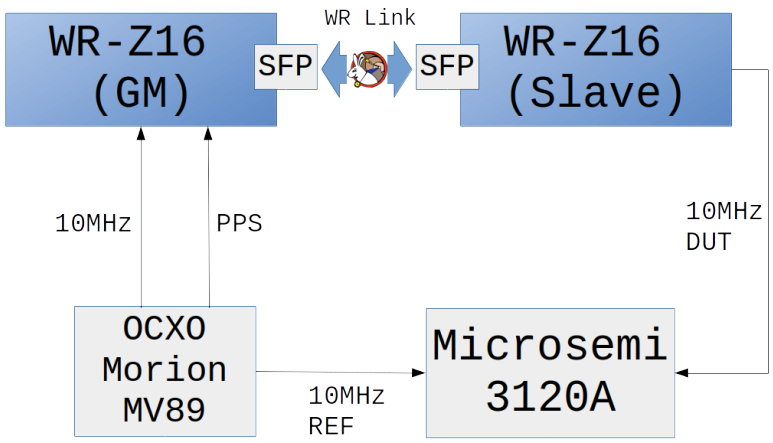

FIGURE 5.5: WR-Z16 phase noise experiment.

After this measurement, a new setup has been configured with a point-to-point link between a WR-Z16 acting as GM and a second one as slave. In this case, the 10 MHz output signal from the slave device has been connected to the phase noise device, maintaining the reference signal. Both test cases have been sampled during 60 minutes and have been performed using 1 GbE and WR 10G links for comparison purposes. For the 1 GbE configuration, WR compliant AXCEN 1310/1490 nm SFPs and a bidirectional one meter long G652D optical fiber have been used.

In these test scenarios, we have performed an optimization process regarding the PI control loop in order to find the best proportional and integrator constants. The results show in Fig. 5.6 correspond with these best values for the constants. They show that the 1 GbE and the 10G versions have different PLL bandwidth. It is because of the specific PI constants values in each version which have been modified to reduce the RMS jitter (Tbl. 5.2). The Tbl. 5.3 collects some results from [122] in regards of the phase noise values for WRS and a enhanced version of this with a low-jitter daughter board.

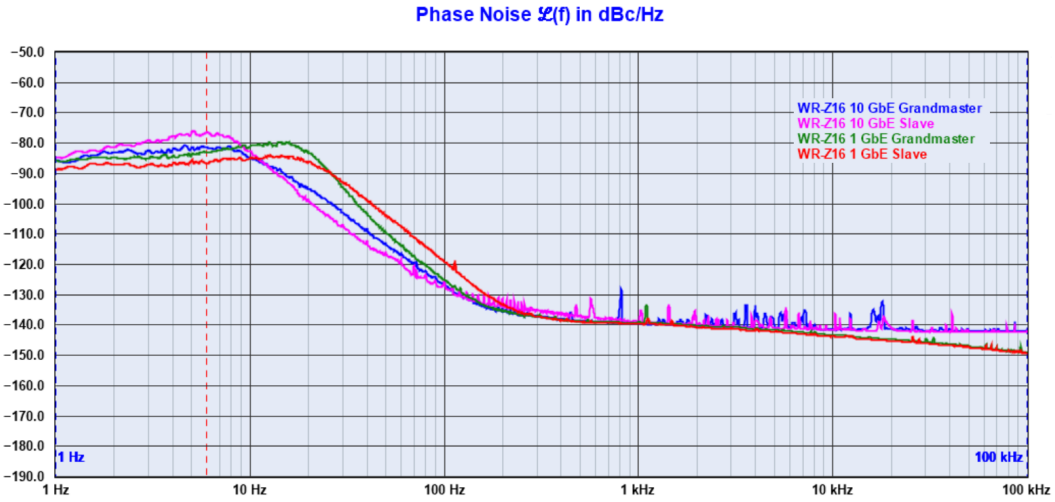

FIGURE 5.6: WR-Z16 phase noise results.

As shown in Tbl. 5.2, phase noise level in the WR-Z16 is lower, both on low and high frequencies, than the standard implementation of the WRS (Tbl. 5.3). As stated in [122], a low-jitter daughter board can be used together with the WRS to reduce significantly the phase noise.

TABLE 5.2: Integrated random RMS jitter in seconds for the WR-Z16 in different configurations.

	Bandwidth	1 Hz-100 Hz	100 Hz-100 kHz	Total
Grandmaster	1 GbE	8.3e-12	3.8e-13	8.68e-12
	10G	5.2e-12	6.3e-13	5.83e-12
Slave	1 GbE	5.6e-12	3.8e-13	5.98e-12
	10G	7.6e-12	6.0 e-13	8.2e-12

TABLE 5.3: Integrated random RMS jitter in seconds for the WRS in different configurations. These values have been extracted from [122]

	Bandwidth	1 Hz-100 Hz	100 Hz-100 kHz	Total
Grandmaster	Standard WRS	7.7e-12	2.5e-12	10.2e-12
	Enhanced WRS	6.0e-13	8.0e-13	1.4e-12
Slave	Standard WRS	11.0e-12	1.2e-12	12.2e-12
	Enhanced WRS	1.1e-12	8.0e-13	1.9e-12

The MDEV (Fig. 5.7) demonstrates that the stability is affected by a combination of white PM noise and flicker PM noise, but with an improved value at $\tau = 1$, specially in the case of the slave device. This improvement is mainly driven by the clock resources in the Zynq family used on the WR-Z16.

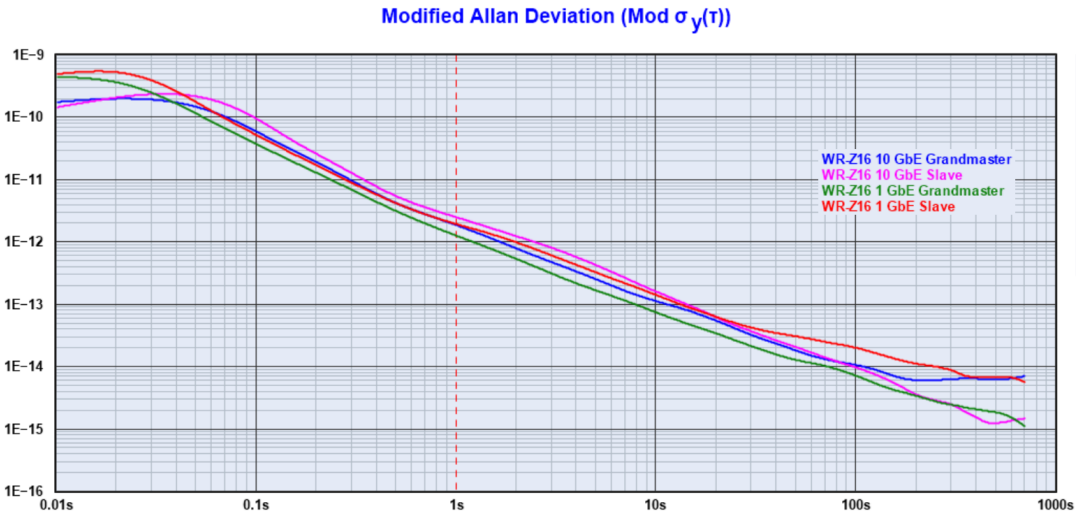

FIGURE 5.7: WR-Z16 modified Allan deviation.

5.4.2 Long term synchronization performance

This section has been dedicated to measure the long term synchronization performance of the WR-Z16 platform. The first step consists on calibrating the 10G link. The calibration procedure is required to characterized the specific hardware delays in order to compensate it. WR proposes an initial calibration method that is described in [80]. For our system, we have performed a manual calibration following the recommendations of that method.

Regarding long term synchronization performance experiments, a specific setup (shown in Fig. 5.8) has been deployed with two WR-Z16 boards connected using two parallel one meter long fibers with Avago AFBR-709SMZ SFPs attached to their optical interfaces. One of them has been configured as master device distributing its own free-running time reference to the other device configured as WR slave. Once the synchronization mechanism is completed, the PPS SMA output ports from both devices have been connected to a counter Keysight 53230A [123] to measure the synchronization accuracy between both devices for more than ninety hours.

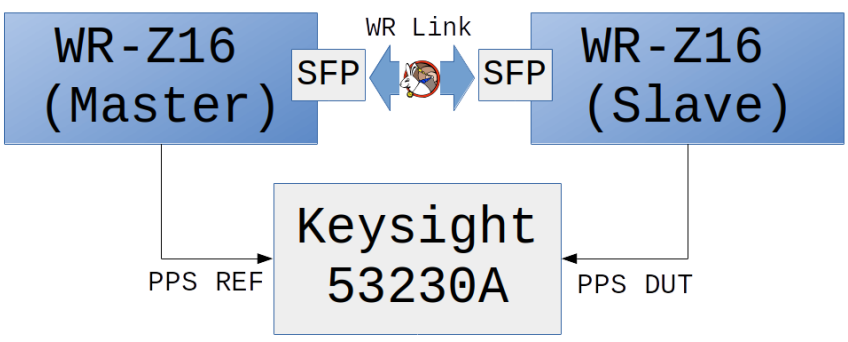

FIGURE 5.8: WR-Z16 PPS experiment.

Fig. 5.9 shows the TDEV that represents the phase difference stability between both WR-Z16 devices. In these results, the τ = 1s is below the 2e-11 s level and it decreases until a minimum value around 1e-12 s. These values are similar to previous evaluations of WR nodes [95], and even improving some of them.

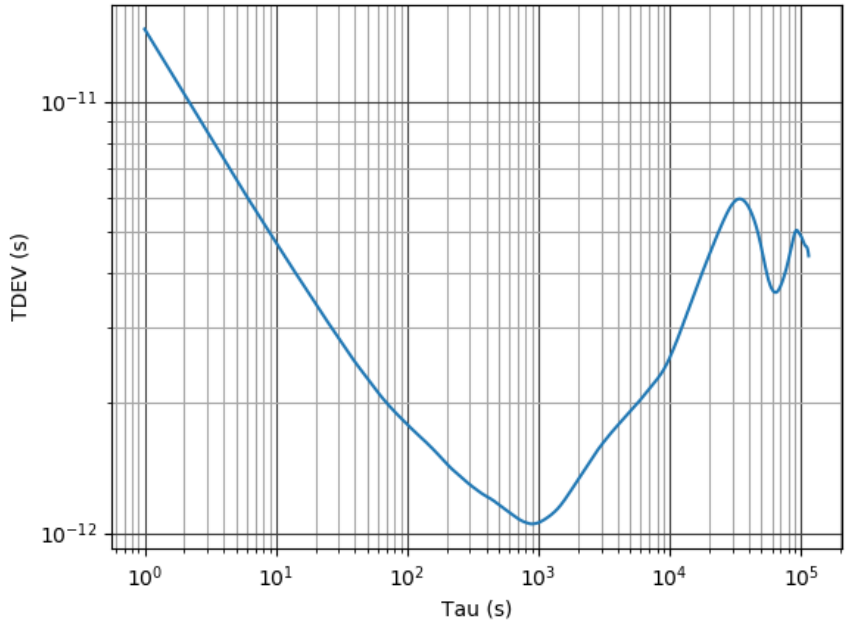

FIGURE 5.9: WR-Z16 TDEV.

Fig. 5.10 draws the MDEV which decreases linearly from τ = 1s until τ = 900s because it is mainly affected by white PM noise. Afterwards, the influence of flicker PM noise can be seen.

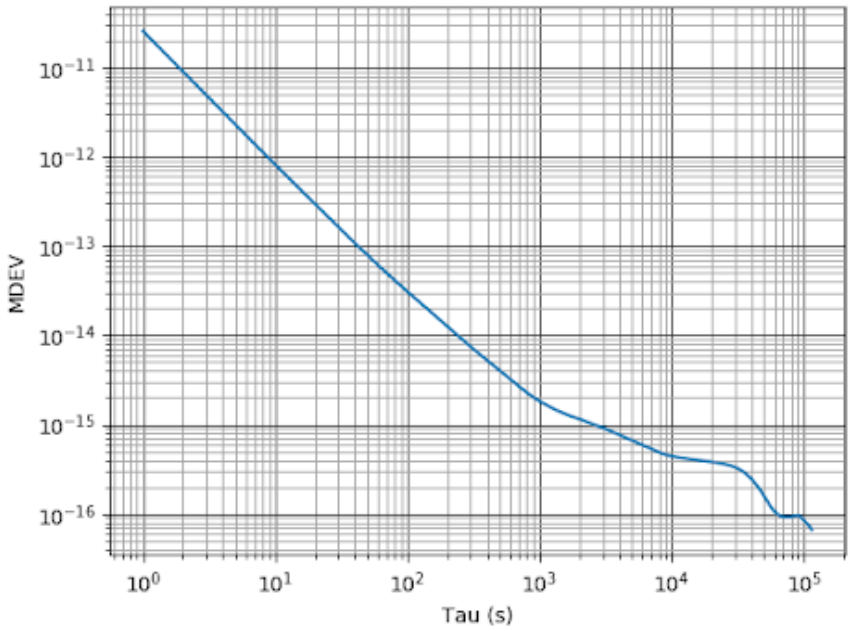

FIGURE 5.10: WR-Z16 MDEV.

The worst case analysis is shown at Fig. 5.11, where the MTIE has been represented. The MTIE values clearly fulfill the WR requirements and, consequently, the WR 10G design is suitable for high accurate synchronization just like the most standard WR nodes [95].

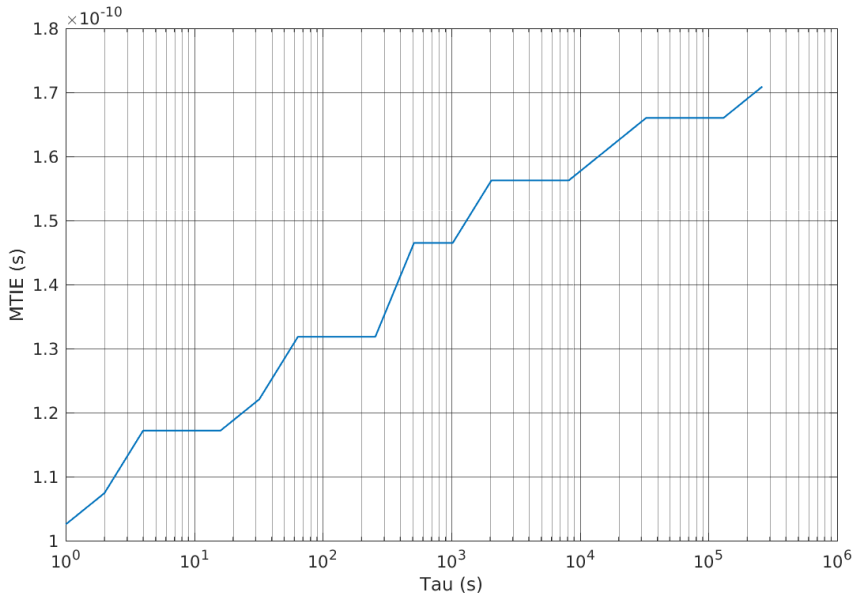

FIGURE 5.11: WR-Z16 MTIE.

5.4.3 10G interoperability and characterization

This section evaluates the interoperability of the solution and characterizes it in terms of data bandwidth and endpoint latency. The fiber strands and the SFPs for these experiments are the same than ones used in sections 5.4.1 and 5.4.2.

The first test scenarios are focused on the interoperability of our 10G solution with commercial 10G devices. We have used two external computers with 10G network interface cards and an Arista DCS-7150S-24-R [124] 10G switch. For simplicity, they are named as computer A and B. The former is equipped with an Endace DAG 10X2-S 10G card [101] whilst the latter brings a Solarflare Communications SFC9120 one [125]. The results of these experiments show that our solution can be used together with 10G standard devices.

Regarding the data bandwidth experiments, the setup configuration is shown in the Fig. 5.12 where the two computers are connected to the WR-Z16 board via an optical fiber. Then, the WR-Z16 routes the incoming packets from one interface to reach the other one. With this simple application, standard software tools such as iperf, netperf or nload can be used to measure the bandwidth performance. Under this context, nload has been chosen due to its stability compared to other alternatives.

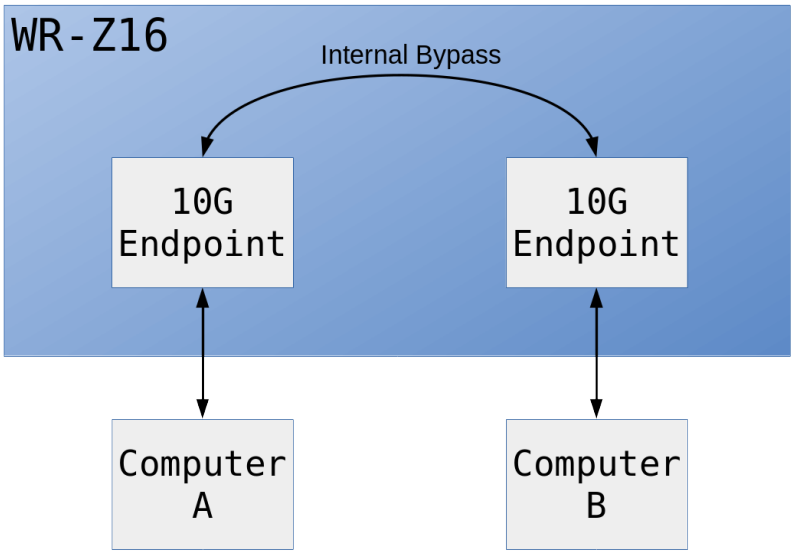

FIGURE 5.12: The two 10G endpoints are internally connected using an internal bypass technique. It allows to redirect each incoming packet to the other port establishing a communication channel between the two PCs.

In the light of the results of data bandwidth test (Fig. 5.13), it has been proved that the 10G Endpoint on the WR-Z16 board is able to cope with the 91.2% of the total capacity of the link.

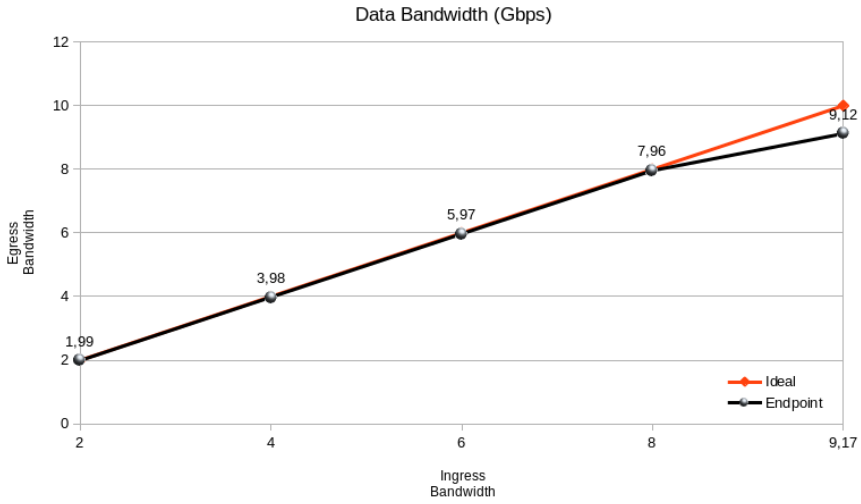

FIGURE 5.13: The X-axis represents the data traffic that is able to generate the network interface card mounted in the computer A. On the other hand, the Y-axis shows the data traffic that reaches to the computer B without any issues.

For the latency measurement, a different approach has been implemented as drawn in Fig. 5.14. On this occasion, no external computer is required to measure the endpoint latency. Instead of this, some additional IP cores have been included in the FPGA design to transmit and receive packets. They are a time baseline block that provides a common time base for the measurement and two timestamp units that are able to detect the start of frame sequence in each endpoint and store a timestamp of

that event. An important consideration about this design is that the clock reference is 156.25 MHz and it limits the timestamp resolution to 6.4 ns. Once IP modules have been inserted into the system, the latency calculation is performed subtracting the two timestamps and dividing the result by two for every single packet. However, this value also considers the fiber propagation delay, it is negligible for short links compared to the endpoint latency.

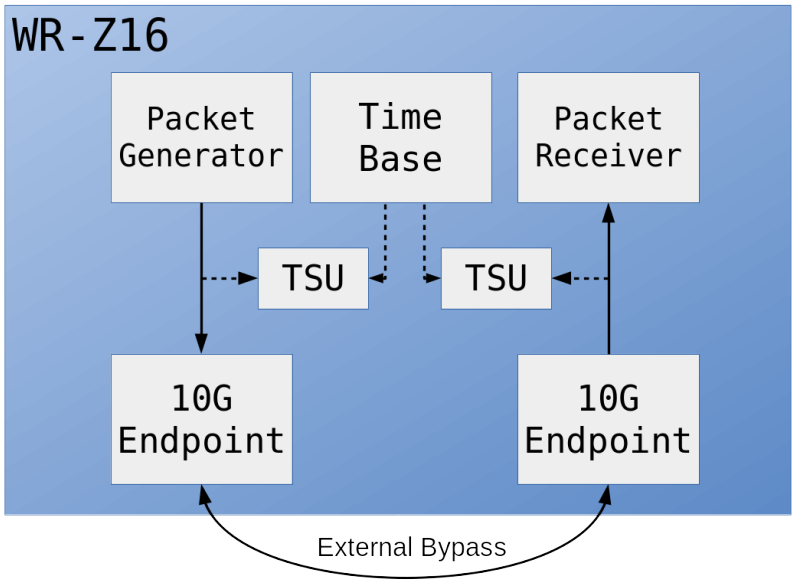

FIGURE 5.14: The two 10G endpoints are connected via an external bypass mechanism (optical fiber). The endpoints traffic is generated from a specific IP core design and is consumed by another module both inside FPGA design.

The Tbl. 5.4 condenses the results extracted from the latency experiments taking into consideration different data utilization conditions. The variation of standard deviation is below 1% of the total value and it falls within the range of the clock granularity. These results evidence that the 10G Endpoint latency is not affected by dynamic data bandwidth and it presents a value between the 198-205 ns with a deviation of 2.59 ns.

Data utilization	Metric	Total delay (ns)	Endpoint delay (ns)
No other data	Max	409.6000	204.8000
	Min	396.8000	198.4000
	Mean	407.3600	203.6800
	σ	4.2933	2.1466
$\approx$ 2 Gbps	Max	409.6000	204.8000
	Min	396.8000	198.4000
	Mean	405.94	202.9700
	σ	5.1881	2.5941
$\approx$ 4 Gbps	Max	416.0000	208.0000
	Min	396.8000	198.4000
	Mean	407.1600	203.5800
	σ	4.2819	2.1409
$\approx$ 6 Gbps	Max	409.6000	204.8000
	Min	396.8000	198.4000
	Mean	405.9400	202.9700
	σ	5.1881	2.5941
$\approx$ 8 Gbps	Max	409.6000	204.8000
	Min	396.8000	198.4000
	Mean	407.4700	203.7300
	σ	3.6950	1.8475
$\approx$ 10 Gbps	Max	403.2000	201.6000
	Min	396.8000	198.4000
	Mean	397.4100	198.7000
	σ	1.9251	0.9625

TABLE 5.4: This table shows the latency metrics retrieved from the experiments when the data utilization changes.

5.5 Final remarks

The current chapter presents a WR 10G compliant system that overcomes the technological limitations of the WR. This contribution allows WR to be used in many applications such as DACQ systems, telecommunications networks, data centers and finance infrastructures among others which require high data bandwidth network technology alongside to high accurate synchronization protocols.

The WR 10G system has been implemented using the WR-Z16 board that brings a new Xilinx Zynq SoC. Its architecture offers advantages derived from FPGA device and, at the same time, enables the deployment of software features by means of its hard-microprocessor. The gateware has been designed following a modular structure where the network IP cores such as MAC and PCS ones can be easily replaced for other versions if the specific application requires it. Moreover, some software components have been implemented to handle hardware (HAL daemon and drivers) and to perform the timing synchronization (Timing daemon). A more detailed description about the implementation of the system can be found in the section 5.3.

In addition to the system implementation, some experiments (section 5.4) have been performed to obtain its timing (sections 5.4.1 and 5.4.2) and data performance (section 5.4.3). The timing performance tests have evaluated the system in terms of

time and frequency distribution. The former demonstrate that WR 10G device has a similar synchronization performance that the most evolved WR 1 GbE nodes, with an accuracy below 200 ps. The latter evidence that the proposed system improves the precision of the standard WRS. The data performance experiments have been applied to obtain the data bandwidth and latency. The results indicate that the system is able to exploit the 91.2% of the total capacity of the 10G link whist the data latency remains in a very low value between 198-205 ns with a deviation of 2.59 ns under different data utilization conditions.

Finally, some interesting future lines have been identified to improve the current system:

- Upgrade the design to work properly in networks that use 25G technology and higher.
- Enhance the interoperability of the 10G solution to enable its integration in real scenarios.
- Increase the timing accuracy and precision of the current system including new synchronization improvements.
- Integrate the low-jitter daughter board [122] into our 10G solution to improve its phase noise.
- Create a new design for a WR compliant switch for 10G networks.

Chapter 6

Conclusions

"It is hard to fail, but it is worse never to have tried to succeed."

– Theodore Roosevelt

Conclusion (Spanish and English versions)

6.1 Conclusiones

Este capítulo se centra en la presentación de las conclusiones esenciales de la tesis junto con sus principales contribuciones, líneas de trabajo futuras y las publicaciones más relevantes.

Este capítulo se estructura de la siguiente forma: Se presentan las conclusiones generales de la tesis en la sección 6.1.1. En la sección 6.1.2 se exponen las contribuciones principales de la tesis. La sección 6.1.3 enumera las líneas de trabajo futuras más prometedoras. Además, la labor de divulgación científica del autor se discute presentando las contribuciones más relevantes a revistas de impacto en la sección 6.1.4.

6.1.1 Conclusiones generales

Esta tesis se centra en los protocolos de sincronización temporal de alta precisión en redes Ethernet y en la tecnología WR. En primer lugar, el capítulo 2 introduce el estado del arte en relación con las técnicas de sincronización considerando su rendimiento. En este contexto, se discuten algunas alternativas como las señales temporales (PPS, 10 MHz), GNSS, IRIG, soluciones software puras como Huygens,

técnicas a medida para aplicaciones metrológicas y aproximaciones basadas en paquetes como NTP, PTP, DTP y WR. Las soluciones metrológicas proporcionan las opciones más precisas pero no son fácilmente integrables en muchas aplicaciones. Por otra parte, los protocolos basados en paquetes se pueden utilizar en muchos sistemas sin problemas importantes. Sin embargo, NTP y PTP no son capaces de proporcionar la precisión en la sincronización temporal demandada por algunas aplicaciones específicas como infraestructuras para aceleradores de partículas, instalaciones para astrofísica, sistemas de telecomunicaciones, redes eléctricas inteligentes y servicios en el área de las finanzas entre otros. Como resultado de esta revisión de la literatura, podemos concluir que la solución más prometedora para una red de sincronización es WR ya que es estándar y puede proporcionar una precisión por debajo del nanosegundo con una estabilidad en el rango de los picosegundos.

En el capítulo 3, se presenta una nueva solución basada en WR que incorpora dispositivos SoC de nueva generación. La plataforma escogida para este desarrollo fue la tarjeta WR-ZEN que incluye un dispositivo SoC de Xilinx conocido como Zynq. Su nueva arquitectura permite el desarrollo de sistemas dedicados usando aceleradores hardware dentro del su chip FPGA y, al mismo tiempo, se pueden ejecutar capacidades software avanzadas en su procesador ARM. La WR-ZEN proporciona una plataforma completamente configurable y suficientemente flexible para ser desplegada como proveedor de tiempo en muchas aplicaciones. Gracias a las bondades de esta solución, se ha propuesto para ser integrada en la infraestructura de SKA. En este contexto, la instalación de SKA requiere de un sistema de DACQ con muchas antenas distribuidas conectadas a través de una red de fibra óptica. Cada elemento de la red debe estar sincronizado con una precisión por debajo de 2 ns lo que puede ser fácilmente conseguido gracias al dispositivo WR-ZEN. Además de las tareas de desarrollo, se han planteado varios escenarios de pruebas con los que se han medido los distintos parámetros del sistema. Algunos de estos experimentos se han centrado en obtener el rendimiento en la sincronización temporal utilizando la diferencia de PPS entre el dispositivo maestro y el esclavo obteniendo un valor máximo de 200 ps. Éste se encuentra por debajo de los requisitos de SKA. Además de las medidas de PPS, se han realizado otros experimentos para comprobar la escalabilidad de la solución propuesta. Dichos resultados demuestran que es posible proporcionar precisiones por debajo del nanosegundo para cientos de nodos en una red con varios niveles. Con el último experimento se ha estudiado el comportamiento del sistema WR-ZEN cuando cambian las condiciones de temperatura. Esto es necesario para asegurar la correcta operación bajo las condiciones ambientales específicas de SKA. Los resultados muestran que la temperatura impacta en el tiempo de propagación en una escala de decenas de ns (96 ns). Sin embargo, la diferencia entre las señales de PPS permanece con una precisión que cumple las necesidades de SKA (211 ps). Los experimentos presentados indican que la solución basada en la WR-ZEN es capaz de cumplir las exigentes demandas de SKA en términos de rendimiento de la sincronización y operar correctamente bajo las condiciones ambientales de las localizaciones específicas de los telescopios. A la luz de los resultados del desarrollo basado en dispositivos SoC, la solución propuesta representa una alternativa muy flexible respecto a los diseños de los antiguos nodos WR. Además, es capaz de proporcionar capacidades avanzadas de software sin necesidad de utilizar equipos externos como un PC permitiendo la integración de la tecnología WR en aplicaciones en las que soluciones embebidas básicas no pueden ser aplicadas.

En el capítulo 4, se presenta una revisión acerca de las redes de alto ancho de banda especialmente en sistemas de DACQ. En este escenario, se ha verificado que los requisitos de dichos sistemas son muy específicos para redes de alto ancho de

banda convencionales. En consecuencia, se ha diseñado una arquitectura de red asimétrica para implementar los mecanismos de agregación y enrutado de datos requeridos por dichos sistemas. Esta arquitectura es muy flexible y ha sido optimizada en términos de recursos lo que la hace perfecta para sistemas de DACQ. En este contexto, se ha implementado una versión específica utilizando la plataforma XDACQ. Posteriormente, esta fue seleccionada para ser utilizada en la infraestructura de CTA, concretamente en la CHEC. En esta cámara, se requieren mecanismos de agregación de datos para conectar varias interfaces de 1 GbE a un puerto de 10G para alcanzar el servidor central desde los sensores distribuidos. Adicionalmente, se debe implementar un sistema de enrutado avanzado, flexible y completamente configurable con propósitos de control y monitorización desde el servidor central. Además de las tareas de desarrollo, se han realizado diferentes experimentos para medir el ancho de banda de datos y la latencia del sistema. El primer conjunto de experimentos se dedicó a la medida del ancho de banda obteniendo hasta 9.29 Gbps. Por tanto, se demuestra que la XDACQ es capaz de aprovechar prácticamente todo el ancho de banda del puerto de 10G. El segundo conjunto de experimentos se ha utilizado para medir la latencia del sistema especialmente la relativa al camino de datos relacionado con el sistema de enrutado. Estos experimentos se han dividido en dos escenarios de prueba: la latencia de la RTU y el aislamiento entre los caminos de datos de agregación y enrutado. El primero demuestra que el módulo de la RTU presenta una latencia determinista por su diseño evitando cualquier penalización en el sistema de enrutado. El segundo escenario de prueba asegura que la actividad del camino de datos de agregación no interfiere en el sistema de enrutado. Esto garantiza que los paquetes de control no son afectados por las condiciones de red de alto ancho de banda en el lado de agregación. Estos resultados evidencian que el sistema basado en la XDACQ es capaz de cumplir los requisitos de CTA. Como nota final, la arquitectura de red asimétrica ha demostrado ser una solución versátil y representa una mejor alternativa para sistemas de DACQ que las redes de alto ancho de banda convencionales. Además, su diseño ha sido optimizado en términos de recursos ofreciendo rendimiento de alto ancho de banda de datos y baja latencia.

En el capítulo 5, se presenta un nuevo sistema de alto ancho de banda de datos basado en WR. Su diseño incluye los conceptos aprendidos de los nodos WR basados en dispositivos SoC y la arquitectura de red asimétrica para redes de alto ancho de banda de datos. Originalmente, WR fue diseñado para solo ser desplegado en redes con tecnología 1 GbE. Sin embargo, muchas aplicaciones industriales y científicas requieren más ancho de banda de datos y normalmente utilizan enlaces de 10G o incluso tecnologías más rápidas. Por lo tanto, una red de bajo ancho de banda independiente tiene que ser desplegada si esas aplicaciones se quieren beneficiar de las virtudes de WR lo que incrementa el coste del sistema. En este contexto, hemos actualizado la tecnología WR para trabajar con enlaces de 10G proporcionando una precisión por debajo del nanosegundo en la sincronización y habilitando la utilización de una sola red para servicios de alto ancho de banda de datos y sincronización. La nueva solución WR para redes de 10G ha sido implementada en la plataforma WR-Z16 que incluye un dispositivo SoC ofreciendo las mismas ventajas que las descritas para el diseño de la WR-ZEN. Respecto a la solución basada en la WR-Z16, la arquitectura del diseño de la FPGA ha sido concebida para ser completamente modular permitiendo el reemplazo de cualquier módulo IP de red como el MAC y el PCS por otros más adecuados para la aplicación específica. Además, se ha creado un ecosistema software para manejar el hardware e implementar el protocolo evolucionado de WR. Con el objetivo de verificar las bondades de esta solución, se han realizado un conjunto de experimentos para evaluar el rendimiento

de la sincronización temporal y del ancho de banda de datos. Por un lado, los experimentos de sincronización temporal comprenden varios casos de prueba para obtener la calidad de la sincronización temporal en relación con la distribución de tiempo y frecuencia. El experimento relativo a la distribución de tiempo está basado en medidas de PPS y revela que el sistema WR basado en enlaces de 10G tiene un rendimiento similar a los nodos WR estándar más evolucionados, con una precisión acotada superiormente por 200 ps. Las prueba de distribución de frecuencia evidencia que el sistema propuesto mejora la estabilidad del WRS estándar. Por otra parte, los experimentos relacionados con el rendimiento de datos han sido ideados para medir la capacidad del sistema en términos de ancho de banda de datos y latencia. Los resultados demuestran que el sistema es capaz de explotar el 91.2% de la capacidad total del enlace de 10G y la latencia permanece en un valor bajo entre 198-205 ns sin importar la actividad de la red. Finalmente, la solución propuesta habilita la tecnología WR para ser utilizada en muchas aplicaciones que requieren redes de 10G y, al mismo tiempo, proporciona una alternativa unificada que es capaz de usar la misma red para propósitos de sincronización de tiempo de alta precisión y de transferencia de datos de alto ancho de banda.

6.1.2 Principales contribuciones

En esta sección, se enumeran las principales contribuciones de la presente tesis.

[Res-1] Se ha realizado una revisión completa de las tecnologías de sincronización, ilustrando ejemplos de aplicaciones clave y los requisitos de las mismas.

[Res-2] Se ha presentado una solución flexible con dispositivos SoC basada en WR, mostrando una mejora en el rendimiento y la flexibilidad. Esta solución ha sido convenientemente evaluada en términos de rendimiento, precisión y capacidades adicionales. Este resultado satisface **[Obj-1]** y **[Obj-5]**.

[Res-3] La arquitectura basada en dispositivos SoC ha sido propuesta como diseño de referencia para el proyecto internacional SKA que requiere un sistema de sincronización de alta precisión para la distribución de PPS. La validación de la viabilidad de dicha solución de acuerdo a los requisitos de SKA se ha llevado a cabo realizando pruebas para comprobar los efectos de la temperatura, medidas de escalabilidad y rendimiento de la sincronización. Este resultado satisface **[Obj-1]** y **[Obj-5]**.

[Res-4] Se ha propuesto una nueva solución para la recopilación de datos y el control en redes Ethernet para aplicaciones para DACQ. Una arquitectura de red asimétrica se ha implementado para dichas aplicaciones. Su diseño tiene en cuenta los requisitos de alto ancho de banda para estos sistemas que adquieren información de múltiples sensores al mismo tiempo. Además, se debe incluir un flujo de control en el diseño para permitir la configuración del sistema y tareas de monitorización. Este resultado satisface **[Obj-1]** y **[Obj-2]**.

[Res-5] La solución de red asimétrica propuesta ha sido adoptada como diseño de referencia para la infraestructura de CTA, concretamente para CHEC. Este resultado satisface **[Obj-2]** y **[Obj-5]**.

[Res-6] Se ha desarrollado una arquitectura unificada completamente modular que incluye los conceptos referentes a los desarrollos realizados basados en dispositivos SoC, el diseño de red asimétrica para los sistemas de DACQ y una importante mejora de la tecnología WR. Este resultado satisface **[Obj-1]**, **[Obj-2]** y **[Obj-3]**.

[Res-7] Se ha presentado la evolución de la tecnología WR para redes 10G. Originalmente, la utilización de WR estaba limitada a redes de bajo ancho de banda con enlaces de 1 GbE. Sin embargo, se ha desarrollado una nueva solución que permite el despliegue de WR en redes de alto ancho de banda como las de 10G. Este resultado satisface **[Obj-1]**, **[Obj-2]** y **[Obj-3]**.

[Res-8] La solución WR para redes 10G ha sido completamente optimizada y validada asegurando su precisión por debajo del nanosegundo. En este contexto, se ha medido el rendimiento de la sincronización temporal teniendo en cuenta su precisión y su distribución de frecuencia revelando resultados comparables o incluso mejores que los obtenidos por los dispositivos estándar de WR. Además, se ha comprobado la interoperabilidad con diferentes equipos comerciales y se ha realizado una caracterización completa del ancho de banda de datos y latencia. Este resultado satisface **[Obj-3]** y **[Obj-4]**.

6.1.3 Trabajo futuro

En esta sección, se presentan brevemente y se discuten algunas líneas futuras de investigación.

El sistema WR basado en redes 10G ha sido desarrollado con una sola interfaz 10G. Sin embargo, se requiere un dispositivo multi-puerto para distribuir la información temporal hasta distintas localizaciones. En consecuencia, el diseño actual podría ser ampliado para incluir varios puertos con capacidades de enrutado similares a las propuestas en la arquitectura de red asimétrica.

Además, el sistema WR basado en redes 10G presenta un diseño modular y flexible que puede ser actualizado para incluir tecnologías de red de mayor ancho de banda como 25G, 40 Gigabit Ethernet (40G) o incluso 100 Gigabit Ethernet (100G).

La tecnología WR implementa mecanismos de distribución de datos que siguen la misma aproximación que en las redes Ethernet convencionales: el esquema best effort. Una interesante línea de trabajo futuro sería la actualización de los dispositivos WR para incluir aspectos de redes de TSN.

6.1.4 Publicaciones

Esta parte presenta publicaciones científicas como artículos, pósters y presentaciones en revistas internacionales y conferencias internacionales/nacionales.

Revistas internacionales con impacto científico

Esta sección expone los artículos publicados, presentados o en preparación para revistas internacionales con un impacto científico significativo:

- M. Jiménez-López, F. Torres-González, J. L. Gutiérrez-Rivas, M. Rodríguez-Álvarez and J. Díaz, "A Fully Programmable White-Rabbit Node for the SKA Telescope PPS Distribution System" **Publicado** en IEEE Transactions on Instrumentation and Measurement (Q1). doi: 10.1109/TIM.2018.2851658.

Disponible online: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8412745&isnumber=4407674

- M. Jiménez-López, J. Machado-Cano, M. Rodríguez-Álvarez, M. Stephan, G. Giavitto, D. Berge and J. Diaz, "Optimized framegrabber for the Cherenkov Telescope Array" **Aceptado** en Journal of Astronomical Telescopes, Instruments and Systems (Q1).

- M. Jiménez-López, F. Girela-Lopez, Emilio Marín-López, Rafael Rodríguez and J. Diaz, "10 Gigabit White Rabbit: a high bandwidth sub-nanosecond synchronization solution for data and timing distribution", **En preparación**.

- J. Sánchez-Garrido, A. Jurado, M. Jiménez-López, M. Rodríguez-Álvarez, D. Berge and J. Diaz, "A novel networked TimeStamp unit for the White Rabbit Synchronization System of CTA", **En preparación**.

Conferencias internacionales y nacionales

Esta sección enumera las publicaciones científicas que se han presentado en conferencias internacionales y nacionales:

- J. Sánchez-Garrido, A. M. López-Antequera, M. Jiménez-López and J. Díaz, "Sub-nanosecond Synchronization over 1G ethernet data links using white rabbit technologies on the WR-ZEN board", 2017 40th International Conference on Telecommunications and Signal Processing (TSP), Barcelona, 2017, pp. 688-693. doi: 10.1109/TSP.2017.8076075. Disponible online: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8076075&isnumber=8075917

- J. López-Jiménez, M. Jiménez-López, J. Díaz and J. L. Gutiérrez-Rivas, "White-rabbit-enabled data acquisition system", 2017 Joint Conference of the European Frequency and Time Forum and IEEE International Frequency Control Symposium (EFTF/IFCS), Besancon, 2017, pp. 410-416. doi: 10.1109/FCS.2017.8088907. Disponible online: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8088907&isnumber=8088780

- M. Jiménez-López, J. L. Gutiérrez-Rivas, J. Díaz, E. López-Marín and R. Rodríguez, "WR-ZEN: Ultra-accurate synchronization SoC based on Zynq technology", 2016 European Frequency and Time Forum (EFTF), York, 2016, pp. 1-4. doi: 10.1109/EFTF.2016.7477790. Disponible online: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7477790&isnumber=7477754

- M. Jiménez López, J. L. Gutiérrez Rivas and J. Díaz Alonso, "A White-Rabbit Network Interface Card for synchronized sensor networks", IEEE SENSORS, Valencia, 2014, pp. 2000-2003. doi: 10.1109/ICSENS.2014.6985426. Disponible online: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6985426&isnumber=6984913

- J.L. Gutiérrez-Rivas, M. Jiménez-López, Eduardo Ros and J. Diaz, "Spanish Participation in the SKA Synchronization and Data Transport (SKA SaDT) Consortium", Sesión de posters en SKA Spanish Day, Octubre 2014, Granada, Spain

6.2 Conclusion

This chapter is focused on presenting the essential thesis conclusions together with its main contributions, future work lines and most relevant publications.

This chapter is structured as follows: General conclusions are presented in section 6.2.1. In section 6.2.2, the main thesis contributions are exposed. Section 6.2.3 enumerates the most promising future lines. Moreover, author scientific dissemination labor are discussed enumerating most important journal contributions in section 6.2.4.

6.2.1 General conclusions

This thesis is focused on the high accuracy timing synchronization protocols based on Ethernet networks and WR technology. Firstly, chapter 2 introduces the state of the art of synchronization technologies taking into consideration their timing performance. Under this context, some alternatives have been discussed as timing signals (PPS, 10 MHz), GNSS, IRIG, pure software solutions as Huygens, custom metrological techniques and packet-based approaches as NTP, PTP, DTP and WR. The metrological solutions provide most accurate choices, albeit they are not easily integrated into many applications. On the other hand, the packet-based protocols can be used in many systems without important issues. However, NTP and PTP are not able to provide the time synchronization performance requested by specific applications such as particle accelerators facilities, astrophysics infrastructures, telecommunication systems, smart grids networks and finance services among others. As a result of this literature review, we can conclude that the most promising solution for the synchronization network is WR because of it is a standard solution that can provide sub-nanosecond accuracy with a precision in the picosecond range.

In chapter 3, a new WR solution using new generation SoC devices is presented. The chosen platform for this development was the WR-ZEN board that includes a Xilinx Zynq SoC device. Its novel architecture enables the development of dedicated systems using hardware accelerators inside the FPGA chip and, at the same time, advanced software capabilities can be executed by the ARM microprocessor. WR-ZEN provides a fully configurable platform and is flexible enough to be deployed as time provider in many applications. Due to the goodness of this solution, it has been proposed to be integrated into SKA infrastructure. Under this context, SKA facility requires a DACQ system with many distributed antennas connected using a optical fiber network. Every element in the network must be synchronized with an accuracy below 2 ns which can be easily obtained thanks to the WR-ZEN device. In addition to the development tasks, several test scenarios have been performed and specific system parameters have been measured. Some of these experiments are focused on obtaining the time synchronization performance by means of PPS difference between master and slave devices obtaining a maximum limit of 200 ps. This value for time accuracy is lower than SKA's requirements. In addition to the PPS test case, other experiments have been performed to check scalability of the proposed solution. Such results demonstrate that is possible to provide sub-nanosecond accuracy for hundred of nodes in multi-level network. The last experiment has studied the WR-ZEN system behavior when temperature conditions change. It is necessary to ensure the proper operation under SKA specific environment conditions. The outcomes show that temperature changes impact on propagation time in a scale of tens of ns (96 ns). Nevertheless, the PPS difference remains with an accuracy that fulfills SKA's needs (211 ps). The presented experiments indicate that WR-ZEN solution is

able to cover the exigent demands of SKA in terms of synchronization performance and deals properly with environmental conditions of the telescope locations. In the light of the results of the development based on SoC devices, proposed solution represents a very flexible alternative respecting to the older WR nodes. Moreover, it can provide advanced software capabilities without the necessity of external equipment as PC enabling the integration of WR technology in applications in which basic embedded solutions are not suitable for.

In chapter 4, a review about high data bandwidth networks have been accomplished specially for DACQ systems. In this scenario, it has been verified that the requirements of such systems are too specific for conventional high data bandwidth networks. Consequently, an asymmetric network architecture has been designed to implement the data aggregation and routing mechanisms required by such systems. This architecture is very flexible and has been optimized in terms of resource utilization what makes it perfect to be used in DACQ systems. Under this context, we have implemented a specific version using the XDACQ platform. Then, it has been selected to be used in CTA infrastructure, concretely in the CHEC. In this camera, data aggregation mechanisms have been required to connect several 1 GbE interfaces to a single 10G port in order to reach the processing server from distributed sensors. Additionally an advanced, flexible and fully configurable routing system must be implemented for control and monitor purposes from the processing server. In addition to the development tasks, several experiments have been performed to measure data bandwidth and system latency. The first set of experiments has been dedicated to the data bandwidth system performance obtaining up to 9.29 Gbps. Therefore, it demonstrates that XDACQ is able to cover almost the full bandwidth of 10G port. The second set of experiments has been used to measure the system latency specifically the routing datapath one. These experiments have been divided into two different test scenarios: RTU latency and isolation between the aggregation datapath and routing one. The former demonstrates that the RTU module presents a deterministic delay by its design avoiding the introduction of any penalty in the routing system. The latter ensures that aggregation datapath activity does not interfere in the routing subsystem. It guarantees that control packets are not affected by high bandwidth network conditions in the aggregation side. These results evidence that XDACQ system is capable of fulfilling the CTA requirements. As final remark, the network asymmetric architecture has demonstrated that is a versatile solution and represents a better alternative for DACQ systems than conventional high data bandwidth networks. Moreover, its design has been optimized in terms of resource utilization offering high data bandwidth performance and low latency.

In chapter 5, a new high data bandwidth system based on WR has been presented. Its design includes the learn concepts from the WR nodes based on SoC devices and the asymmetric network architecture for high data bandwidth networks. Initially, WR was designed only to be deployed over 1 GbE networks. However, many current industrial infrastructures and scientific facilities require more data bandwidth and normally use 10G links or even faster technologies. Therefore, an independent low bandwidth synchronization network must be deployed if these applications want to benefit from WR virtues what increases the cost of overall system. Under this context, we have updated the WR technology to work properly with 10G links providing sub-nanosecond synchronization and allowing the utilization of a single high bandwidth network for data and synchronization services. The new WR 10G solution has been implemented in the WR-Z16 platform that brings a new generation SoC device offering same advantages than those described for WR-ZEN design. Regarding WR-Z16 solution, the gateware architecture has been conceived to

be fully modular allowing the replacement of any network IP core such as MAC and PCS for other ones more suitable for the specific application. Furthermore, a software ecosystem has been created to handle hardware and to implement the evolved WR protocol. In order to verify the goodness of the solution, a set of experiments has been performed to evaluate the timing synchronization and data performance. On the one hand, the timing synchronization experiments comprise several test cases to obtain timing synchronization quality in terms of time and frequency distribution. The time dissemination experiment based on PPS measurements reveals that WR 10G system has a similar performance that the most evolved standard WR nodes, with an accuracy bounded by 200 ps. The frequency distribution test evidences that the proposed system improves the precision of the standard WRS. On the other hand, the data performance experiments have been devised to measure system capacity in terms of data bandwidth and latency. The results demonstrate that the system can exploit the 91.2% of the total capacity of the 10G link and data latency remains in a very low value between 198-205 ns regardless of network activity. Finally, the proposed solution enables the WR technology to be used in many applications that require 10G networks and, at the same time, provides an unified alternative that is able to use the same network for high accurate timing synchronization and high data bandwidth transfer purposes.

6.2.2 Main contributions

In this section, the main contributions of the present thesis dissertation are enumerated.

[Res-1] A complete review of synchronization technologies has been performed, illustrating key example applications and the performance requirements.

[Res-2] A flexible SoC solution based on WR has been presented, showing an enhancement on performance and flexibility. This solution has been properly evaluated in terms of performance, accuracy and additional features. This result satisfies the **[Obj-1]** and **[Obj-5]**.

[Res-3] The SoC architecture has been proposed as reference design for the SKA international project that requires a high accurate timing synchronization system for PPS distribution. The validation of the feasibility of such solution according to SKA requirements has been addressed including temperature effects, scalability measurement and synchronization performance. This result satisfies the **[Obj-1]** and **[Obj-5]**.

[Res-4] A novel solution for data gathering and control over Ethernet networks has been proposed for DACQ applications. An asymmetric network architecture has been implemented for such applications. Its design takes into account high data bandwidth requirements for these systems that acquire information from multiple sensors at the same time. Moreover, a control flow must be included in the design in order to enable system configuration and monitoring tasks. This result satisfies the **[Obj-1]** and **[Obj-2]**.

[Res-5] The proposed asymmetric network solution has been adopted as reference design for the CTA facility, concretely for the CHEC. This result satisfies the **[Obj-2]** and **[Obj-5]**.

[Res-6] A fully modular and unified architecture has been developed including the new SoC implementation concepts, the asymmetric network design for DACQ systems and an important enhancement for the WR technology. This result satisfies the **[Obj-1]**, **[Obj-2]** and **[Obj-3]**.

[Res-7] The evolution of the WR technology for 10G networks has been presented. Initially, the utilization of WR was limited to low data bandwidth network with 1 GbE links. However, a new solution has been developed to enable the deployment of WR in high data bandwidth networks such as 10G ones. This result satisfies the **[Obj-1]**, **[Obj-2]** and **[Obj-3]**.

[Res-8] The WR 10G solution has been fully optimized and tested ensuring its sub-nanosecond accuracy. Under this context, timing synchronization performance has been measured in terms of accuracy and frequency distribution exposing results comparable or even better than WR standard devices ones. Furthermore, the interoperability has been demonstrated with different commercial equipment and a full characterization of the data bandwidth and latency has been performed. This result satisfies the **[Obj-3]** and **[Obj-4]**.

6.2.3 Future work

In this section, some promising future lines of research are briefly presented and discussed.

The WR 10G system has been developed with a single 10G interface. However, a multi-port device is required in order to disseminate timing information to several locations. Consequently, the current design could be extended to have several ports with similar routing capabilities than the asymmetric network architecture ones.

Moreover, the WR 10G system presents a modular and flexible design which can be updated to use higher bandwidth network technologies as 25G, 40 Gigabit Ethernet (40G) or even 100 Gigabit Ethernet (100G).

WR technology implements data delivery mechanisms which follow the same approach as in conventional Ethernet networks: best effort one. An interesting future work line would be to update WR devices including TSN networks aspects.

6.2.4 Publications

This part introduces scientific publications such as articles, posters and presentations on international journal and international/national conferences.

International journals with scientific impact

This section exposes articles published, submitted or in progress for international journals with significantly scientific impact:

- M. Jiménez-López, F. Torres-González, J. L. Gutiérrez-Rivas, M. Rodríguez-Álvarez and J. Díaz, "A Fully Programmable White-Rabbit Node for the SKA Telescope PPS Distribution System" **Published** in IEEE Transactions on Instrumentation and Measurement (Q1). doi: 10.1109/TIM.2018.2851658. Available online: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8412745&isnumber=4407674

- M. Jiménez-López, J. Machado-Cano, M. Rodríguez-Álvarez, M. Stephan, G. Giavitto, D. Berge and J. Diaz, "Optimized framegrabber for the Cherenkov

Telescope Array" **Accepted** in Journal of Astronomical Telescopes, Instruments and Systems (Q1).

- M. Jiménez-López, F. Girela-Lopez, Emilio Marín-López, Rafael Rodríguez and J. Diaz, "10 Gigabit White Rabbit: a high bandwidth sub-nanosecond synchronization solution for data and timing distribution", **Work in progress**.

- J. Sánchez-Garrido, A. Jurado, M. Jiménez-López, M. Rodríguez-Álvarez, D. Berge and J. Diaz, "A novel networked TimeStamp unit for the White Rabbit Synchronization System of CTA", **Work in progress**.

International and national conferences

This section enumerates scientific publications that have been presented on international and national conferences:

- J. Sánchez-Garrido, A. M. López-Antequera, M. Jiménez-López and J. Díaz, "Sub-nanosecond Synchronization over 1G ethernet data links using white rabbit technologies on the WR-ZEN board", 2017 40th International Conference on Telecommunications and Signal Processing (TSP), Barcelona, 2017, pp. 688-693. doi: 10.1109/TSP.2017.8076075. Available online: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8076075&isnumber=8075917

- J. López-Jiménez, M. Jiménez-López, J. Díaz and J. L. Gutiérrez-Rivas, "White-rabbit-enabled data acquisition system", 2017 Joint Conference of the European Frequency and Time Forum and IEEE International Frequency Control Symposium (EFTF/IFCS), Besancon, 2017, pp. 410-416. doi: 10.1109/FCS.2017.8088907. Available online: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8088907&isnumber=8088780

- M. Jiménez-López, J. L. Gutiérrez-Rivas, J. Díaz, E. López-Marín and R. Rodríguez, "WR-ZEN: Ultra-accurate synchronization SoC based on Zynq technology", 2016 European Frequency and Time Forum (EFTF), York, 2016, pp. 1-4. doi: 10.1109/EFTF.2016.7477790. Available online: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7477790&isnumber=7477754

- M. Jiménez López, J. L. Gutiérrez Rivas and J. Díaz Alonso, "A White-Rabbit Network Interface Card for synchronized sensor networks", IEEE SENSORS, Valencia, 2014, pp. 2000-2003. doi: 10.1109/ICSENS.2014.6985426. Available online: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6985426&isnumber=6984913

- J.L. Gutiérrez-Rivas, M. Jiménez-López, Eduardo Ros and J. Diaz, "Spanish Participation in the SKA Synchronization and Data Transport (SKA SaDT) Consortium", Poster session at SKA Spanish Day, October 2014, Granada, Spain

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