MENTORED RESEARCH PROJECT [MTAF] "ANALITICAL MODELING FOR SQUARE GATE-ALL-AROUND MOSFETs"'

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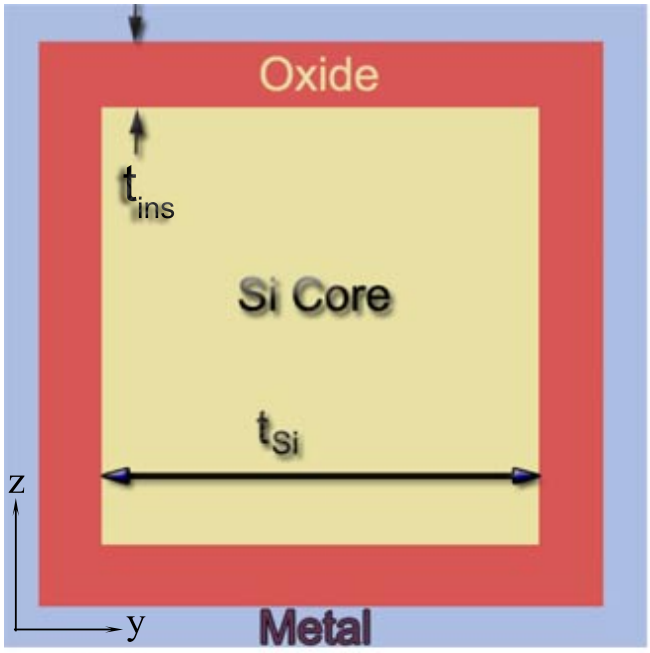

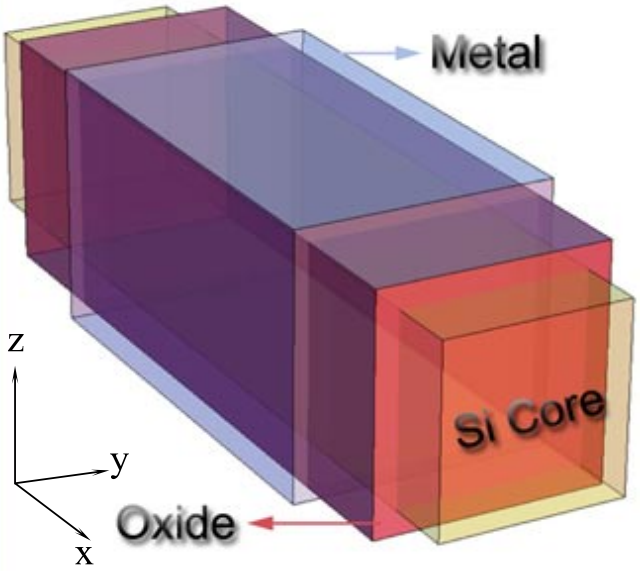

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in memory of my cousin
Ángel Moreno *(1972-04),*
a devoted motorcycle rider
and a lovely man, who was
taken from us much too soon.

Contents

1 Abstract

Two analytical models for square Gate All Around (GAA) MOSFETs has been introduced. The first part of this report include a quantum viewpoint and this first work has been published [1], while the second part approach a classical developed.
With the model developed in the first part, it is possible to provide an analytical description of the 2D inversion charge distribution function (ICDF) in square GAA MOSFETs of different sizes and for all the operational regimes. The accuracy of the model is verified by comparing the data with that obtained by means of a 2D numerical simulator that self-consistently solves the Poisson and Schrödinger equations. The expressions presented here are useful to achieve a good description of the physics of these transistors; in particular, of the quantization effects on the inversion charge. The analytical ICDF obtained is used to calculate important parameters from the device compact modeling viewpoint, such as the inversion charge centroid and the gate-to-channel capacitance, which are modeled for different device geometries and biases. The model presented accurately reproduces the simulation results for the devices under study and for different operational regimes.
Anyway the second part of this report is focus on square GAA MOSFETs with a classical view point, which have not been analytically described in depth due to their particular geometrical complexity. The analytical description of cylindrical GAA MOSFETs is simpler since the symmetry of the structure around the rotation angle allows a 1D description, accounting just for the radial component [2–5]. In the case of square GAA MOSFETs other modeling strategies are necessary, as will be shown below.
Firstly, a technique to obtain analytical functions which are solutions of the 2D Poisson equation where the charge density in the silicon channel has been calculated, and the total inversion charge is introduced. Among all these functions a simple one for the electric potential in the silicon core of the square GAA MOSFETs was proposed. Secondly, the model introduced has been used to calculate the total inversion charge making use of Gauss's Law. The models obtained are finally validated with simulations data obtained with a 2D simulator developed in our group for Multiple-gate MOSFETs. This second part is organized as follows: in section 7 the electric potential modeling is introduced. The calculation and modeling of the inversion charge is presented in section 8. Finally, the main conclusions are given in section 9.

2 Introduction

Multiple-gate MOSFETs are considered a serious alternative for keeping up with the continuous reduction in device dimensions imposed by Moore's law. These structures show promising possibilities in relation to the control of short channel effects (SCEs) and the achievement of ideal subthreshold swing values [6–8].
Both square and cylindrical GAA MOSFETs are currently under intense study from the simulation and modeling viewpoint [**?**,2–5,8,9,11–13]. One key area in these structures is the study of quantum mechanical effects (QMEs), since both structural and electrical confinement (produced by a square gate in the quadruple-gate device and by a circular gate in the cylindrical one) make these devices (nanowires FETs) quasi-1D transistors, where transport occurs in a set of loosely coupled propagating modes.
Making use of technologies based on these new geometries, channel lengths could be shrunk to below 22nm accordingly to the latest edition of ITRS [6]. In this respect, their capacity to reduce SCEs and

the possibility of using undoped channels are essential features for the achievement of this goal. The latter, in particular, is critical since random impurity effects are by no means negligible in nanometric devices [14, 15]. These effects produce a dispersion of fundamental parameters such as the threshold voltage and the sub-threshold slope [14–17].
GAA MOSFETs are part of the Silicon-On-Insulator (SOI) transistor family, which demonstrates unique features that look promising for future mainstream CMOS technologies [16, 17]. The use of ultra-thin-body (UTB) SOI structures allows the fabrication of fully-depleted devices that offer not only extremely good control of SCEs but also a very good behaviour with respect to drain-induced barrier-height lowering (DIBL), threshold voltage roll-off, and off-state leakage [16, 17].
In first part of this work the study is focus on square GAA MOSFETs with a cuantum viewpoint. To the best of our knowledge, these devices have not previously been analytically described in any depth due to their particular geometrical complexities. The concentration of inversion charge close to the corners of the silicon body makes a bi-dimensional description of the inversion charge distribution and other important magnitudes imperative from the compact modeling viewpoint. The analytical description of cylindrical GAA MOSFETs is simpler since the symmetry of the structure around the rotation angle allows a 1D description, accounting for just the radial component [2–5]. In the case of square GAA MOSFETs, other modeling strategies are necessary.
First, an analytical function $f(y, z)$ that accurately reproduces the inversion charge distribution function (ICDF) for square GAA MOSFETs of different sizes and for different biases have been introduced. The ICDF is related to the inversion charge density as $n(y, z) = N_{\text{inv}} \mid f(y, z) \mid^2$, N_{inv} (cm^{-1}) being the value of the total electron density integrated over the square area of the silicon channel. Second, The inversion charge centroid (ICC) and the gate-to-channel capacitance (C_{GC}), making use of the proposed analytical ICDF have been successfully modeled. The geometry of these devices makes the definition and modeling of the ICC a tough issue. To deal with this, I have presented a definition that correctly characterises the spatial distribution of the inversion charge in the silicon channel.

In second part of this report, a technique to obtain analytical functions to model the electric potential will be introduced. These functions are solutions of the 2D Poisson equation where the charge density in the silicon channel includes the inversion charge. In this respect, the approach I'm following is much accurated than others presented previously that do not take the inversion charge into account for the calculation of the charge density (these calculations were thought to analyze the potential distribution for threshold voltage modeling purposes, at the onset of the inversion operation region, where the inversion charge can be neglected reasonably). The inclusion of the inversion charge in my calculations make feasible the modeling of the most important operation regions (from the sub-threshold regime to strong inversion). Several functions to model the electric potential of a square GAA MOSFETs were proposed. The use of these functions is faced with the usual compact modeling trade-off: complexity versus accuracy. In this respect I will discuss the pros and cons of the functions I make use of. I will also calculate the inversion charge (by means of Gauss' Law) and compare the results with simulation data obtained with a 2D simulator developed in my group for Multiple-gate MOSFETs.
Inversion charge modeling is the starting point for drain current and capacitance models necessary for the development of a compact models for circuit simulation purposes. The accurate geometrical description of the charge is also a very interesting feature for mobility modeling, since coulomb and surface roughness scattering mechanisms strongly depend on the interaction of the inversion charge with semicoductor-oxide interfaces.
The second part of the report is organized as follows: in section 7 the electric potential modeling is introduced, and the calculation and modeling of the inversion charge as well as some discussions is presented in section 8. Finally, the main conclusions are given in section 9.

3 Simulator description

The simulation data presented in this work have been obtained by using a simulator developed within the research group of department of electronics and computers technology of Granada University [9, 11]. The geometry and cross-section of the GAA MOSFET studied is shown in figure 1, where t_{ins} and t_{Si} are the insulator thickness and the silicon body thickness, respectively. It can be seen that the gate completely surrounds the square silicon channel where conduction takes place. To reach a fast convergence, the 2D Poisson and Schrödinger equations, the latter solved for each energy valley, have been self-consistently solved using the predictor-corrector scheme proposed by Trellakis et al. [18] including the energy valley degeneration of the silicon conduction band. The simulator achieves accurate results for different structures, materials and gate voltages if the number of energy levels and their corresponding wave functions employed in the calculation is high enough to capture all the occupied levels.

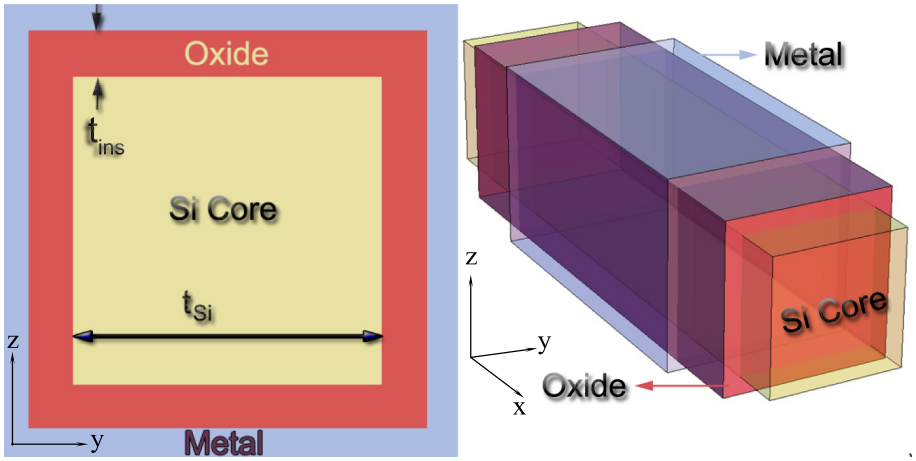


Figure 1: Cross-section and 3D geometry of the square GAA MOSFETs under study.

The geometry of the device shown in figure 1 confines the electrons in the plane perpendicular to the transport direction, which means that I am dealing with a 1D electron gas. The quantum charge density is therefore obtained by evaluating the following expression [9, 18]:

$$\rho(y,z) = \frac{q}{\pi}\left(\frac{2mk_{\mathrm{B}}T}{\hbar^2}\right)^{\frac{1}{2}} \sum_n \Psi_{\mathrm{n}}^2(y,z)\Im_{-\frac{1}{2}}\left(\frac{E_{\mathrm{F}}-E_{\mathrm{n}}}{k_{\mathrm{B}}T}\right) \qquad \left[\frac{C}{cm^3}\right] \tag{1}$$

where q is the electron charge, E_{F} is the Fermi level, Ψ_{n} is the wave function belonging to energy level E_{n}, $\Im_{-1/2}$ the complete Fermi-Dirac integral of order -1/2 and the remaining symbols have their usual meaning.

The simulator uses finite elements for the discretization of the equations. More details of the code can be found in the following references [3, 9, 19]. In all the simulated devices, an undoped substrate ($N_{\mathrm{A}} = 10^{14}$ cm^{-3}), a metal gate with a work-function of 4.61eV and an insulator thickness of 1.5 nm have been considered. The t_{Si} values considered in my work were 10, 15 and 20 nm.

Part I
An analytical model for square GAA MOSFETs including quantum effects

4 Inversion charge modeling

In this section an analytical model to describe the ICDF of square GAA MOSFETs is proposed. As starting point, the approach followed by Ge et al. for the symmetrical Double Gate MOSFETs (DGMOSFETs) [20] was used. Thus, I tried to obtain a 2D analytical model for the ICDF by generalising the 1D eigenfunctions proposed there (equation (4) in Reference [20]). I adapted the quantum mechanical variational calculation employed in [20] for the square geometry corresponding to the GAA MOSFETs considered in this report, in this way linking the analytical expression of the eigenfunctions to the inversion charge for each gate voltage and device size.

The model obtained with this procedure was compared with the simulation results but it did not fit well for certain gate voltage values and device sizes. The main explanation for this behavior could be the following: the boundary conditions chosen for the electric potential calculation were of Dirichlet kind, using a constant potential value at the semiconductor-insulator interfaces, following the approach presented in [20]. This approximation was good for DGMOSFETs devices because of the one-dimensionality of the structure; however, for a 2D square GAA MOSFETs this is not the case outside the flat band operation regime [9]. More complex boundary conditions would render more realistic results although they would increase the complexity of the analytical models. This extra complexity would make the approach useless from the compact modeling point of view.

Thus, in order to obtain a model analytically simple and accurate enough to reproduce the simulation results for different gates voltages and device sizes, I had to use a different approach. I proceeded to do so by using several trial functions. I found the best results were achieved by making use of the following inversion charge distribution function:

$$\mathrm{f(y,z)} = \mathrm{A'}\left[\sin\left(\frac{\pi \mathrm{y}}{\mathrm{t_{Si}}}\right)\right]^{\frac{1}{2}}\left[\sin\left(\frac{\pi \mathrm{z}}{\mathrm{t_{Si}}}\right)\right]^{\frac{1}{2}}\left(\mathrm{e}^{\frac{-\mathrm{b}(\mathrm{t_{Si}}-\mathrm{y})}{\mathrm{t_{Si}}}}+\mathrm{e}^{\frac{-\mathrm{by}}{\mathrm{t_{Si}}}}\right)\left(\mathrm{e}^{\frac{-\mathrm{b}(\mathrm{t_{Si}}-\mathrm{z})}{\mathrm{t_{Si}}}}+\mathrm{e}^{\frac{-\mathrm{bz}}{\mathrm{t_{Si}}}}\right) \tag{2}$$

where the normalization of (2) leads to:

$$A' = \frac{\left(1+\frac{b}{\pi}\right)^2 \mathrm{e}^{\mathrm{b}}}{t_{\mathrm{Si}}\left(b+\frac{b^2}{\pi^2}+\frac{\mathrm{e}^{\mathrm{b}}}{2b}\right)} \tag{3}$$

In this way, the electron density can be obtained as $n(y,z) = N_{\mathrm{inv}} \mid f(y,z) \mid^2$. A heuristic algorithm was developed to determine the value of the b coefficients (i.e., to obtain the dependencies of the b coefficients on the inversion charge and the device size $b(N_{\mathrm{inv}}, t_{\mathrm{Si}})$). To do this, I calculated and minimized the root mean square error (RMSE) of the simulated and modeled data for the inversion charge distribution function for all the grid nodes used in my calculations. The b coefficients obtained are given in figure 2 (shown as NA, numerical algorithm). I also developed an empirical analytical expression (4) to reproduce these b coefficients for compact modelling purposes (plotted as FF, fitting function, in figure 2). As shown, a good fit is achieved.

$$b = v(t_{\mathrm{Si}}) + g(t_{\mathrm{Si}})\,(N_{\mathrm{inv}})^{h(t_{\mathrm{Si}})} \tag{4}$$

where:

$$v(t_{\mathrm{Si}}) = -1.388 \cdot 10^{12} t_{\mathrm{Si}}^2 + 5.481 \cdot 10^6 t_{\mathrm{Si}} - 3.248$$
$$g(t_{\mathrm{Si}}) = 2.053 \cdot 10^9 t_{\mathrm{Si}}^2 - 7418.12 t_{\mathrm{Si}} + 0.0069$$
$$h(t_{\mathrm{Si}}) = -9.353 \cdot 10^{10} t_{\mathrm{Si}}^2 + 376995.66 t_{\mathrm{Si}} + 0.1696$$

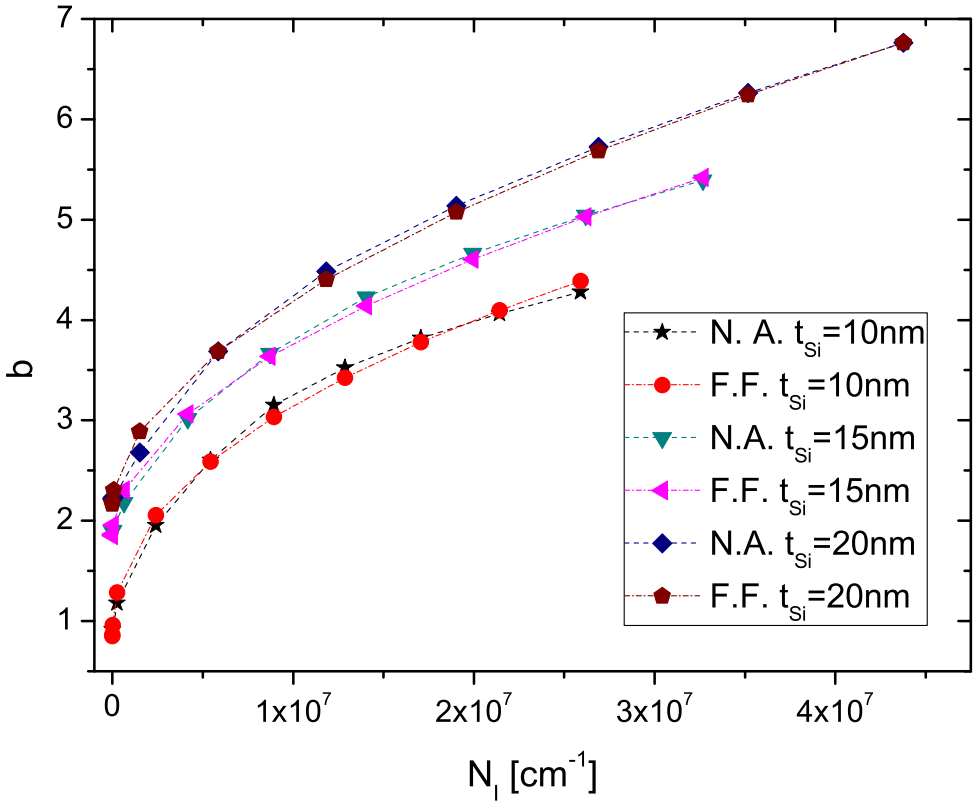


Figure 2: b coefficients versus inversion charge for different square GAA MOSFETs (t_{Si} =10 nm, t_{Si} =15 nm,t_{Si} =20 nm). The b coefficients correspond to the model proposed in (2). Numerical Algorithm (NA) and fitting fuction (FF) results are shown.

As can be seen in figures 3, 4 and 5, the new model, despite its relative simplicity, reproduces the simulation data reasonably well. The three dimensional comparison of the simulated and modelled ICDF (the latter obtained with (2)) shows a good fit in figure 3. I also analysed the accuracy of the model in depth by plotting different ICDF cross sections for several device sizes and gate voltages. In figure 4, the t_{Si}=10nm device has been chosen and some cross sections of the ICDF are depicted along the y axis for several z values, both in weak and strong inversion. In figure 5, ICDF cross sections are plotted along the y axis for several gate voltages and different device sizes. To obtain the most representative ICDF values (maxima and minima), the selected z positions generally depended on the device size. The fit is good for all the gate voltages considered, as shown in figures 4 and 5.

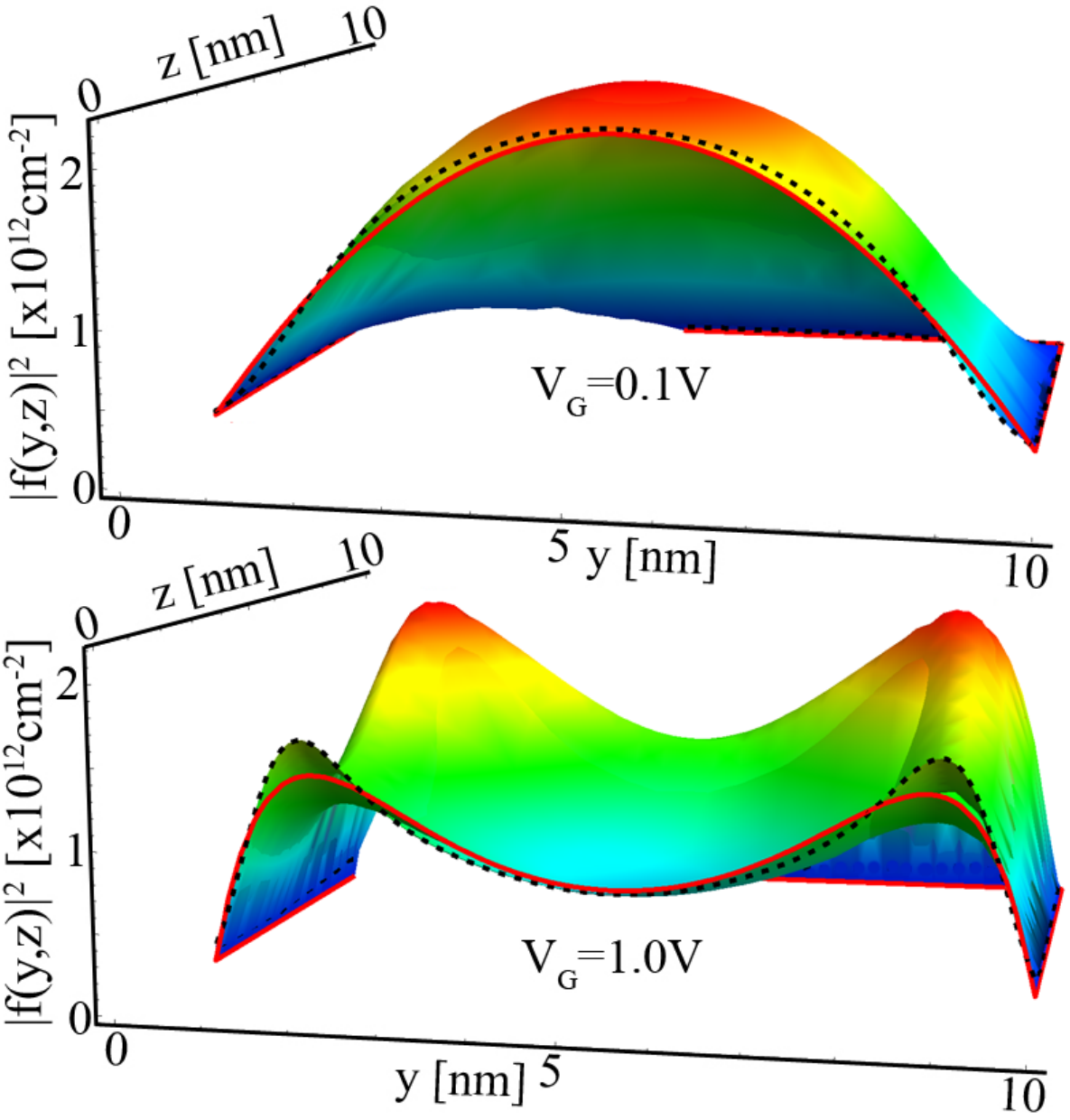
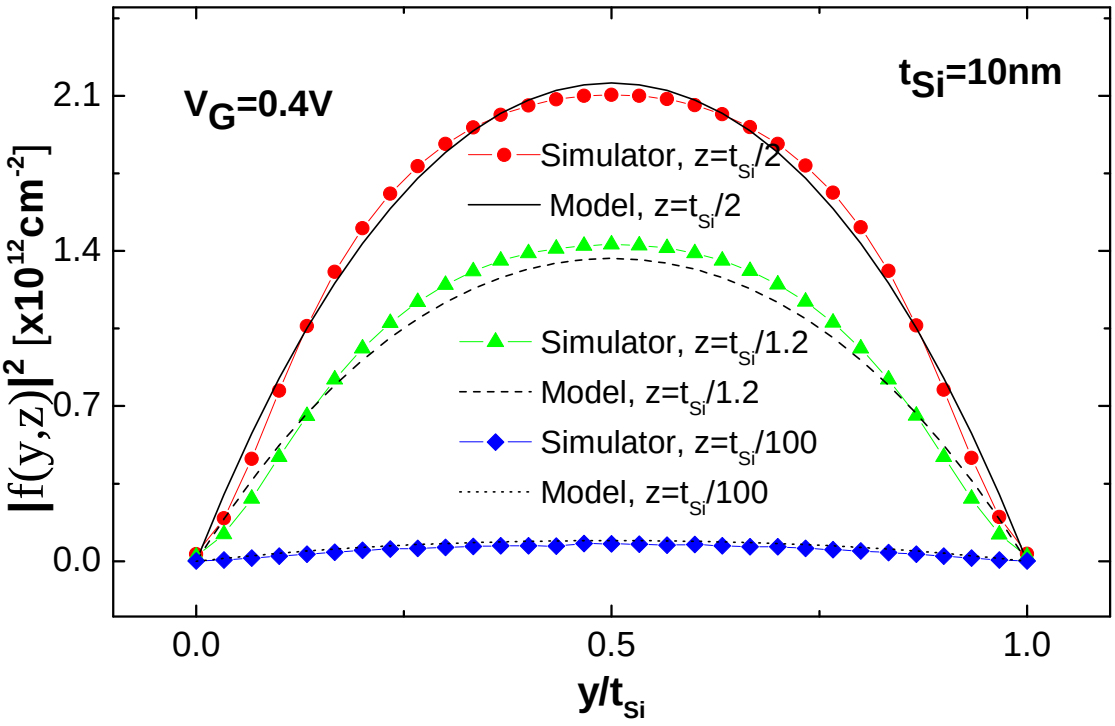
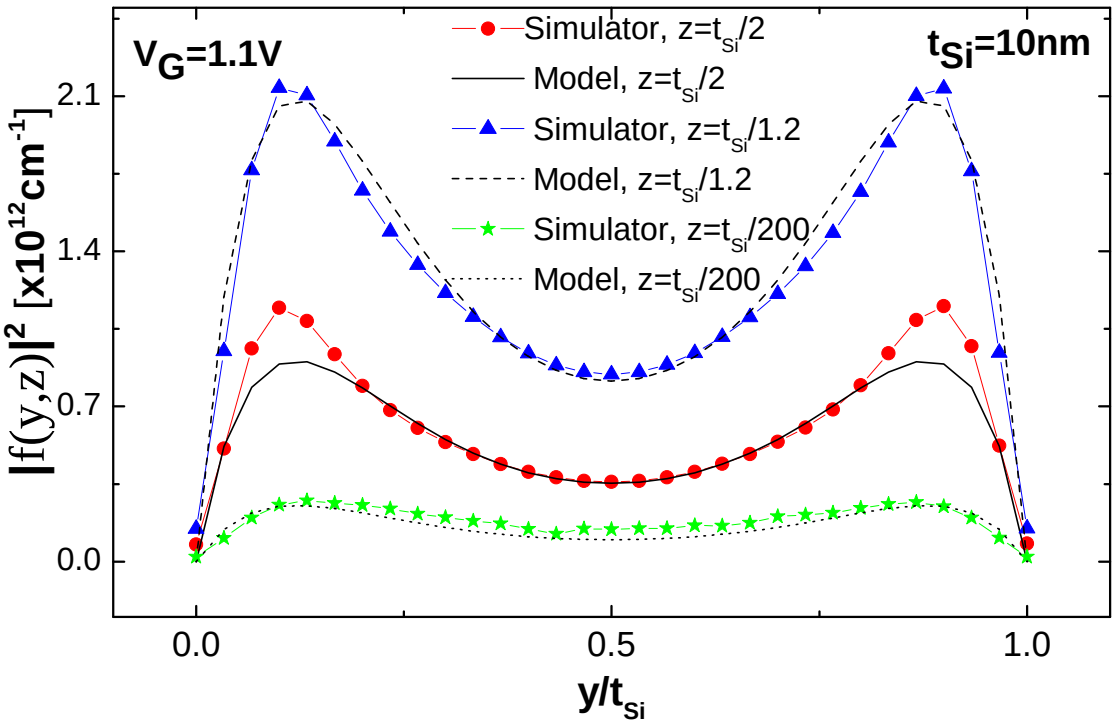


Figure 3: Three-dimensional view of the inversion charge distribution function for a square GAA MOSFET. The technological parameters used were the following: $t_{\mathrm{Si}} = 10$ nm, $t_{\mathrm{ins}} = 1.5$ nm, $N_A = 10^{14}$ cm^{-3}, qϕ_{m}=4.61 eV. The modelled (simulated) data are represented by the surface with solid (dashed) borders.
a) V_{G}=0.1V
b) V_{G}=1.1V

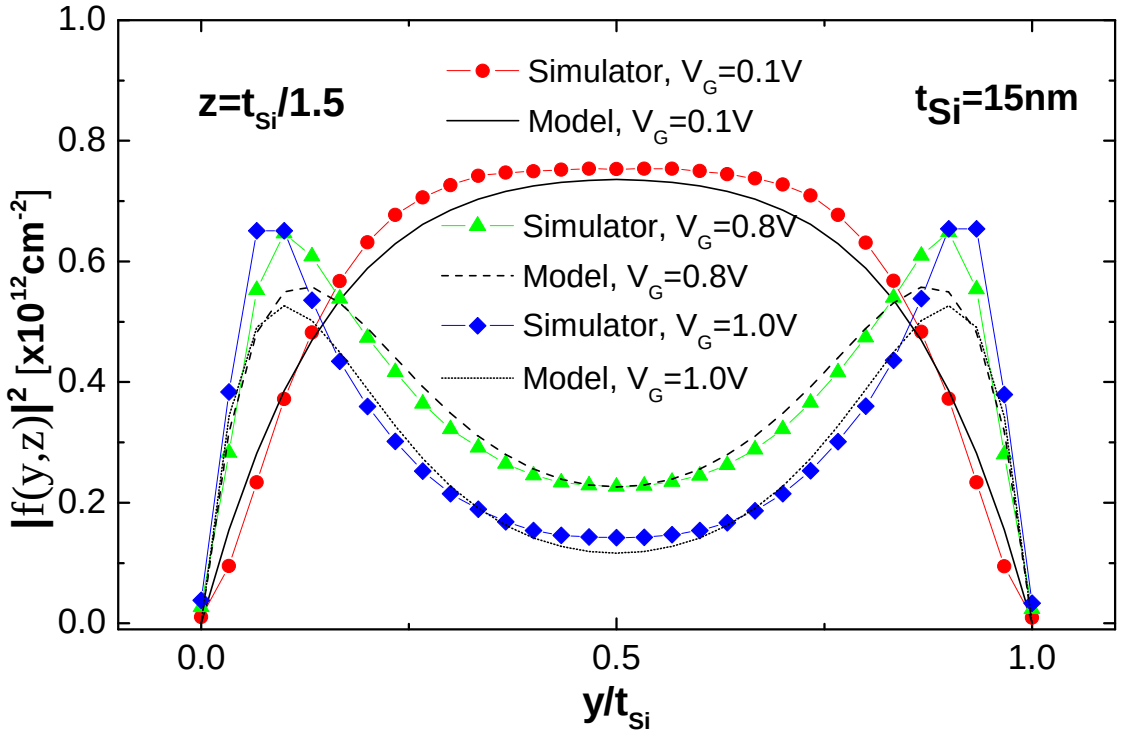


(a)

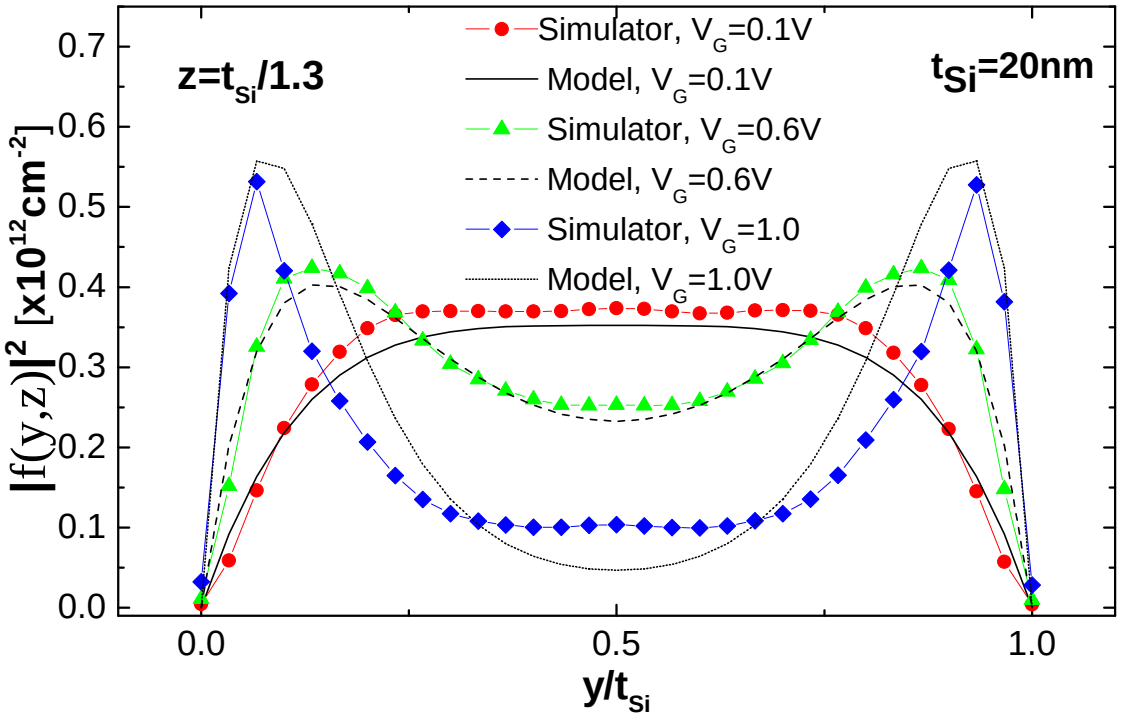


(b)

Figure 4: Inversion charge distribution function cross sections along the y axis for several z values for a square GAA MOSFET with $t_{\mathrm{Si}} = 10nm$. a) V_{G}=0.4V, b) V_{G}=1.1V



(a)



(b)

Figure 5: Inversion charge distribution function cross sections along the y axis for several gate voltages for square GAA MOSFETs.
a) $z = \frac{t_{\mathrm{Si}}}{1.5}$ and $t_{\mathrm{Si}} = 15nm$.
b) $z = \frac{t_{\mathrm{Si}}}{1.3}$ and $t_{\mathrm{Si}} = 20nm$.

In the following sections, I will use equation (2) to approximate the square GAA MOSFET ICDF in order to deal with the ICC and the C_{GC} modelling. As will be shown, the use of more complex models (e. g., a linear combination of eigenfunctions) for the ICDF would make the calculation of the ICC extremely time-consuming.

5 Inversion charge centroid calculation

The ICC in conventional bulk MOSFETs is defined as the first momentum of the inversion charge distribution (the semiconductor-insulator interface is chosen as the origin for this calculation) [**?**, 21, 22]. This parameter is essential in modelling current MOSFETs since when compared to the physical gate insulator thickness, it represents the influence of quantum mechanical effects (QMEs) on the inversion charge spatial distribution. The 1D definition of the ICC is intuitive, as reported in [**?**, 21, 22], and its modelling was carried out in bulk, double-gate and surrounding gate MOSFETs [**?**, 3, 21, 22] (note that cylindrical 2D devices can be analysed as 1D by means of an appropriate choice of coordinate system [3]). However, the definition of a useful ICC for square GAA MOSFETs is not simple. Some attempts towards this definition have been made previously [24, 25]. Here, I have followed [25] and dealt with this issue by defining an ideal square (depicted in dashed lines in figure 6) with its sides parallel to the semiconductor-insulator interfaces. The sides of the square represent the zones where, on average, most of the inversion charge is placed for a particular gate voltage.

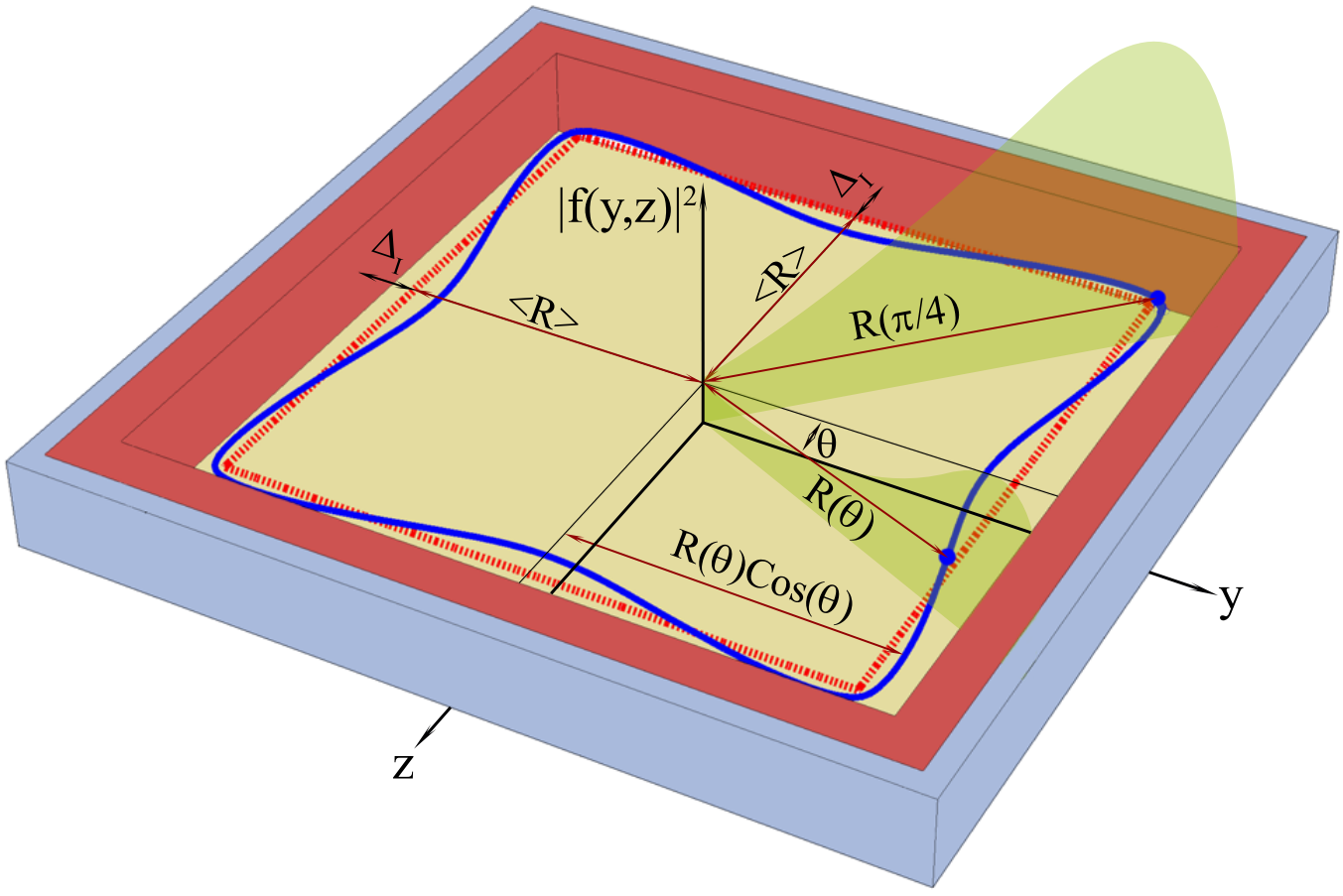


Figure 6: Representation of the $R(\theta)$ and $\langle R \rangle$ parameters needed for the inversion charge centroid definition of square GAA MOSFETs.

To determine the square that best represents the ICDF, its first momentum $R(\theta)$ has been calculated (here, θ is the angular coordinate of the polar coordinate system with its origin located at the centre of the square silicon body, see figure 6). The mathematical expression for the $R(\theta)$ calculation is the following:

$$R(\theta) = \frac{\int_0^{\frac{t_{\mathrm{Si}}}{2\cos(\theta)}} r\, n(r\cos(\theta), r\sin(\theta))dr}{\int_0^{\frac{t_{\mathrm{Si}}}{2\cos(\theta)}} n(r\cos(\theta), r\sin(\theta))dr} \tag{5}$$

where $\frac{t_{\mathrm{Si}}}{2\cos(\theta)}$ is the distance from the centre of the silicon core to the semiconductor-insulator interface for each θ value (note that due to the device symmetry, only $0 \leq \theta \leq \frac{\pi}{4}$ has to be considered in the calculation of $R(\theta)$).

Figure 6 shows $R(\theta)$ in solid lines for a square GAA MOSFET. I calculated $R(\theta)$ making use of the ICDF model introduced in the previous section ($n(r,\theta) = N_{\mathrm{inv}}\left|f(r\cos(\theta), r\sin(\theta))\right|^2$) and compared it with the results achieved using simulated data for all the GAA MOSFETs sizes and gate voltages considered in this part of the work (see figure 7). I tried to establish how accurately my ICDF model reproduced the $R(\theta)$ data obtained with simulated data. To do this, I defined an error function, $E_{rr}(\theta)$, as the relative difference between the $R(\theta)$ values obtained with the simulator and with the model:

$$E_{rr}(\theta) = \frac{\Delta R(\theta)}{R_{\max}} \times 100(\%) = \frac{\left|R_{\mathrm{Analytical}}(\theta) - R_{\mathrm{Simulator}}(\theta)\right|}{\frac{t_{\mathrm{Si}}}{2\cos(\theta)}} \times 100(\%) \tag{6}$$

For each applied gate voltage, I calculated the maximum $E_{rr}(\theta)$ by solving $\left.\frac{\mathrm{dE_{rr}}(\theta)}{\mathrm{d}\theta}\right|_{\theta=\theta_{max}} = 0$, and then selected the highest value achieved for each device size. The results are summarized in table 1. As can be seen, the model also works well (in relation to the calculation of $R(\theta)$) for all the devices under study and for the whole bias voltage range considered.

Table 1: Maximum value of the $E_{rr}(\theta)$ function for the GAA MOSFETs studied.

t_{Si}	$10nm$	$15nm$	$20nm$
E_{rr}^{MAX}	1.6%	3.5%	4.6%

To calculate the size of the ideal square that models the inversion charge position (see figure 6), the geometric average of the $R(\theta)$ projection at the Y axis was estimated as:

$$\langle R\rangle = R_{\mathrm{I}} = \left(\prod_{k=0}^{N}\left[R\left(\frac{k\pi}{4N}\right)\cos\left(\frac{k\pi}{4N}\right)\right]\right)^{\frac{1}{N+1}} \tag{7}$$

Finally, the average inversion charge centroid, Δ_I, was calculated as is usual in 1D MOSFETs, i. e., by considering the origin to be at the semiconductor-insulator interface. This definition (see the equation below), which makes use of R_{I}, allows the inclusion of QMEs in the gate capacitance model as will be shown in the next section.

$$\Delta_{\mathrm{I}} = \frac{t_{\mathrm{Si}}}{2} - R_{\mathrm{I}} \tag{8}$$

The Δ_{I} data are plotted in figure 8. It can be seen that the ICC values obtained with the simulation results correctly reproduce those calculated using the ICDF model (2).

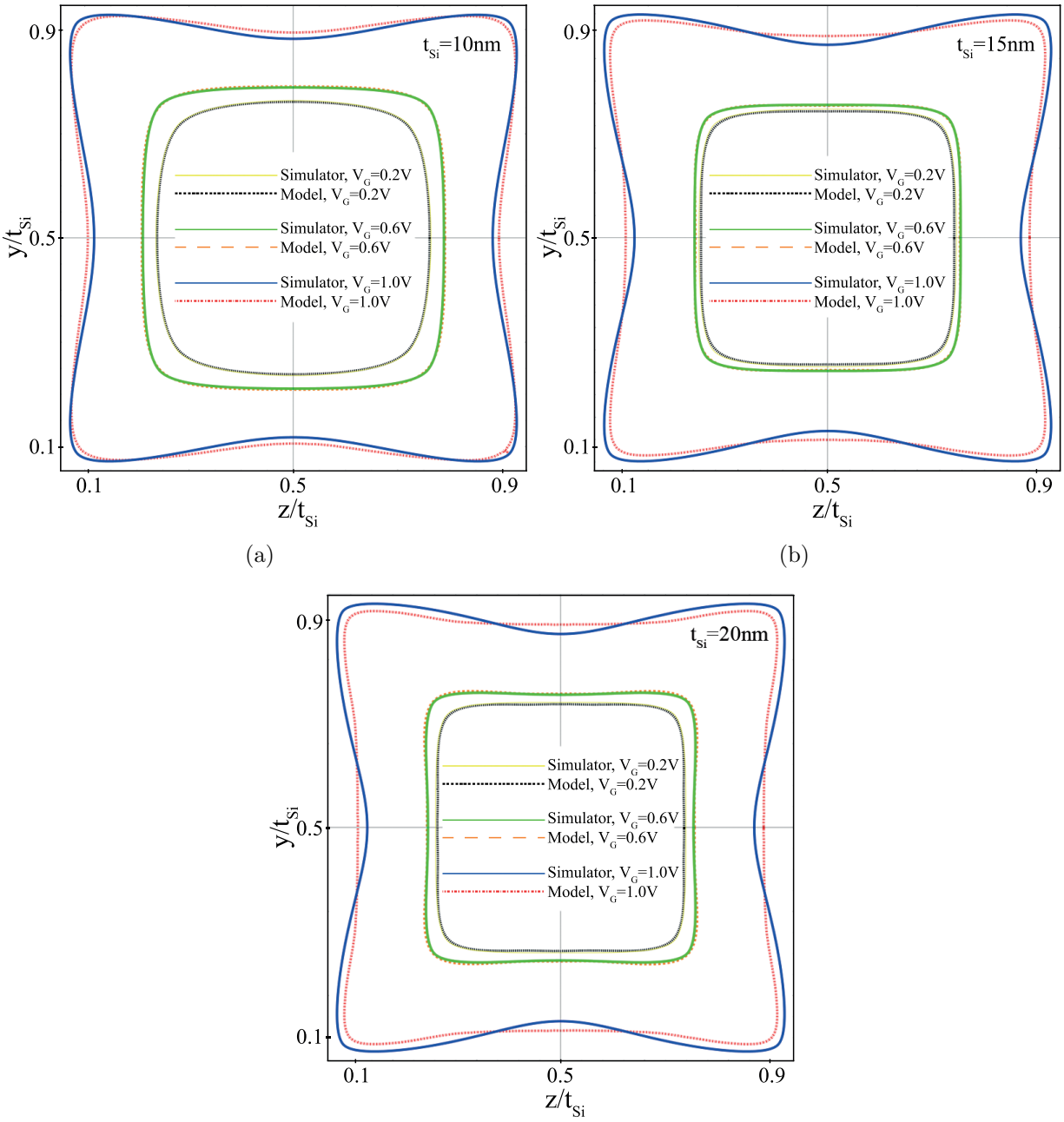


Figure 7: $R(\theta)$ polar plots for square GAA MOSFETs. The inversion charge centroid is calculated with modelled and simulated data for several V_{G} voltages.
a) $t_{\mathrm{Si}} = 10nm$.
b) $t_{\mathrm{Si}} = 15nm$.
c) $t_{\mathrm{Si}} = 20nm$.

6 Gate-to-channel capacitance modelling

The gate-to-channel capacitance, C_{GC}, is an essential MOSFET parameter since it determines the transconductance of the transistor [4, 7]. In 1D devices, C_{GC} can be calculated as the series combination of the gate insulator capacitance C_{ins} and the channel capacitance C_{ch} [26–28]:

$$C_{\mathrm{GC}} = \left(\frac{1}{C_{\mathrm{ins}}} + \frac{1}{C_{\mathrm{ch}}} \right)^{-1} \tag{9}$$

However, in the case of square GAA MOSFETs, several approximations are needed to achieve my goal of developing a simple analytical expression for C_{GC}. First, the semiconductor-insulator interface is not isopotential, making equation (9) an approximate expression [9, 19, 25]. Moreover, there are no closed analytical expressions either for C_{ins} or for C_{ch}. For the insulator capacitance term, an empirical expression previously obtained by curve-fitting was used [29]:

$$C_{\mathrm{ins}} = \frac{5\epsilon_{\mathrm{ins}}}{\ln\left(1 + \frac{5t_{\mathrm{ins}}}{4t_{\mathrm{Si}}}\right)} \tag{10}$$

It can be seen that for low values of the $t_{\mathrm{ins}}/t_{\mathrm{Si}}$ ratio (within the limit $t_{\mathrm{Si}} >> t_{\mathrm{ins}}$), the C_{ins} value of a conventional bulk MOSFET is obtained, as should be the case.

Regarding the channel capacitance, an approximate expression can be achieved, using the expression corresponding to DG MOSFETs, which can be calculated as:

$$C_{\mathrm{ch}}^{-1} = \frac{\mathrm{d}\phi_{\mathrm{s}}}{\mathrm{dQ_{inv}}} = \frac{\mathrm{d}\left(\phi_{\mathrm{s}} - \phi_{\mathrm{c}}\right)}{\mathrm{dQ_{inv}}} + \frac{\mathrm{d}\phi_{\mathrm{c}}}{\mathrm{dQ_{inv}}} \tag{11}$$

ϕ_{s} and ϕ_{c} being the electrostatic potential at the surface and the centre of the silicon body, respectively, and Q_{inv} the inversion charge per unit length ($Q_{\mathrm{inv}} = qN_{\mathrm{inv}}$). The former equation can be rewritten as [30]:

$$C_{\mathrm{ch}}^{-1} = \frac{x_{\mathrm{i}}}{W\varepsilon_{\mathrm{Si}}} + \frac{Q_{\mathrm{inv}}}{W\varepsilon_{\mathrm{Si}}}\frac{\mathrm{dx_i}}{\mathrm{dQ_{inv}}} + \frac{\mathrm{d}\phi_{\mathrm{c}}}{\mathrm{dQ_{inv}}} = \frac{1}{C_{\mathrm{inv}}} + \frac{1}{C_{\mathrm{c}}} \tag{12}$$

where x_{i} is the charge centroid position, defined in [22], and W is the transistor width (necessary to calculate the capacitance per unit length).

In order to model the gate capacitance of square GAA MOSFETs, a term equivalent to each of (12) is needed. First, a model of the electric potential within the silicon body is needed to calculate C_{c}. Due to the lack of symmetry of this kind of device, an alternative option is to make use of the similarities found between the potential behaviour in cylindrical and square GAA devices [31]. An example of these similarities is found in figure 9, where $\mathrm{d}\phi_{\mathrm{c}}/\mathrm{dQ_{inv}}$ is compared for cylindrical and square GAA MOSFETs. As can be seen, the results for the two devices are found to be almost identical. Analytical models for the electrostatic potential of cylindrical GAA devices are available in the literature [**?**, 32, 33], and here I have modelled the potential at the centre of a square GAA MOSFET making use of the expression proposed in [**?**]. Thus, the C_{c} term can be calculated as:

$$C_{\mathrm{c}} = \frac{Q_0 k_{\mathrm{B}} T}{qQ_{\mathrm{inv}}\left(Q_0 + Q_{\mathrm{inv}}\right)} \tag{13}$$

where $Q_0 = (k\mathrm{B}T/q)8\pi\varepsilon_{\mathrm{Si}}$ and the remaining parameters keep their usual meaning.

To calculate the inversion capacitance term in (12), C_{inv}, the DG centroid definition was first replaced by the one introduced in this work for the square GAA device. Then, the planar capacitance formula $W\varepsilon_{\mathrm{Si}}/x_{\mathrm{i}}$ was replaced by its square quadruple-gate counterpart (found from (10) where t_{ins} and t_{Si} are replaced by Δ_{I} and $t_{\mathrm{Si}} - 2\Delta_{\mathrm{I}}$, respectively). Finally a fitting parameter F replaced the

channel width W in the second part of the $C_{\rm inv}$ term, to appropriately take into account the 2D confinement effect. The resulting expression for square GAA MOSFETs $C_{\rm inv}$ is:

$$C_{\rm inv}^{-1} = \left(\frac{5\varepsilon_{\rm Si}}{\ln\left(1 + \frac{5}{8}\frac{\Delta_{\rm I}}{R_{\rm I}}\right)} \right)^{-1} + \frac{Q_i}{F\varepsilon_{\rm Si}} \frac{{\rm d}\Delta_{\rm I}}{{\rm dQ}_{\rm inv}} \tag{14}$$

For the sake of compactness, an empirical expression to obtain the values needed for the F parameter as a function of $t_{\rm Si}$ (here, both $t_{\rm Si}$ and F are given in centimetres) have been developed:

$$F = 2.9 \cdot 10^{-6}({\rm cm}) - 4.45 t_{\rm Si} + 2.9 \cdot 10^{6}({\rm cm}^{-1}) t_{\rm Si}^2 \tag{15}$$

Figure 10 shows the overall gate capacitance obtained from the simulation of a square GAA MOSFET with $t_{\rm Si} = 10$nm, and each one of its components (i.e., $C_{\rm ins}$, $C_{\rm inv}$ and $C_{\rm c}$), calculated used the models developed. As can be seen, the $C_{\rm c}$ term controls the behaviour of the device in the weak inversion regime, while $C_{\rm inv}$ is responsible for the gate capacitance degradation with respect to the ideal limit value $C_{\rm ins}$. A very good agreement between the model and the simulated data is achieved.

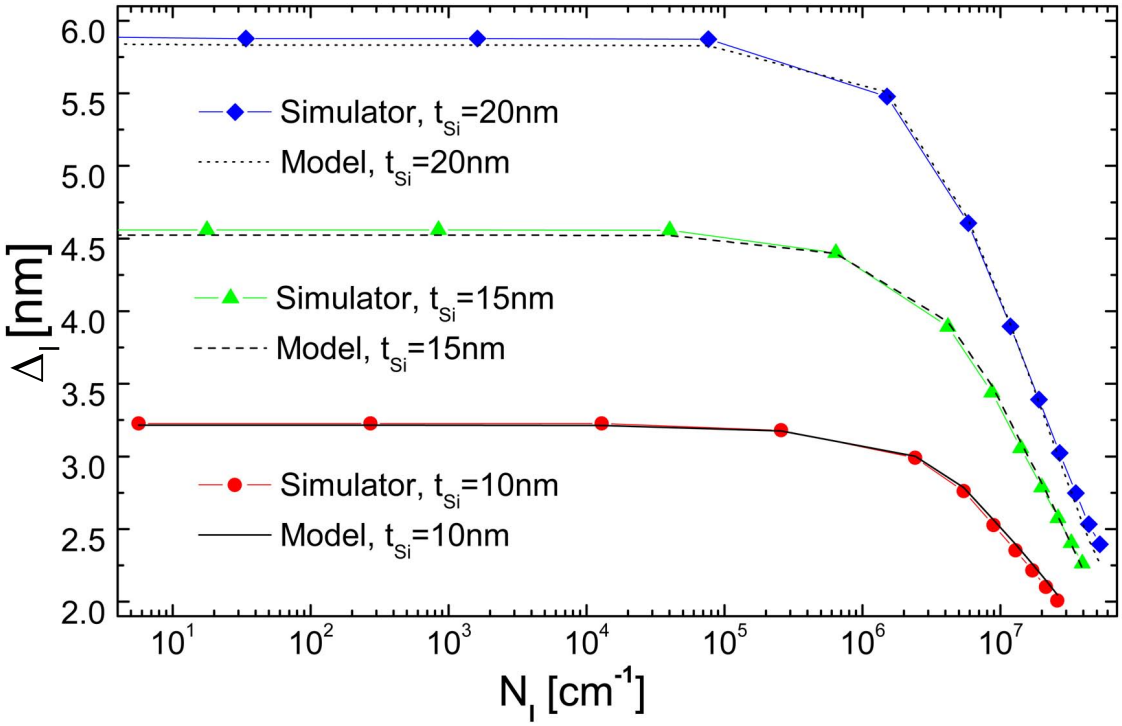


Figure 8: Average inversion charge centroid versus inversion charge for square GAA MOSFETs of different sizes.

I have compared the simulated gate-to-channel capacitance values with those obtained with (9) for various device sizes and the results are plotted in figure 11. As can be seen, quite a good fit is achieved in both the weak and strong inversion regimes. It should be highlighted that the different capacitances obtained with (9), plotted in symbols, were calculated through a fully analytical approach, which involved the calculation, using (2), of the ICDF for each device size and gate voltage, and the subsequent estimation of $\Delta_{\rm I}$ making use of (8). Therefore, the model introduced in this work reproduces reasonably well the simulation data obtained for the inversion charge distribution, the charge centroid and the gate-to-channel capacitance for different device sizes and bias voltages.

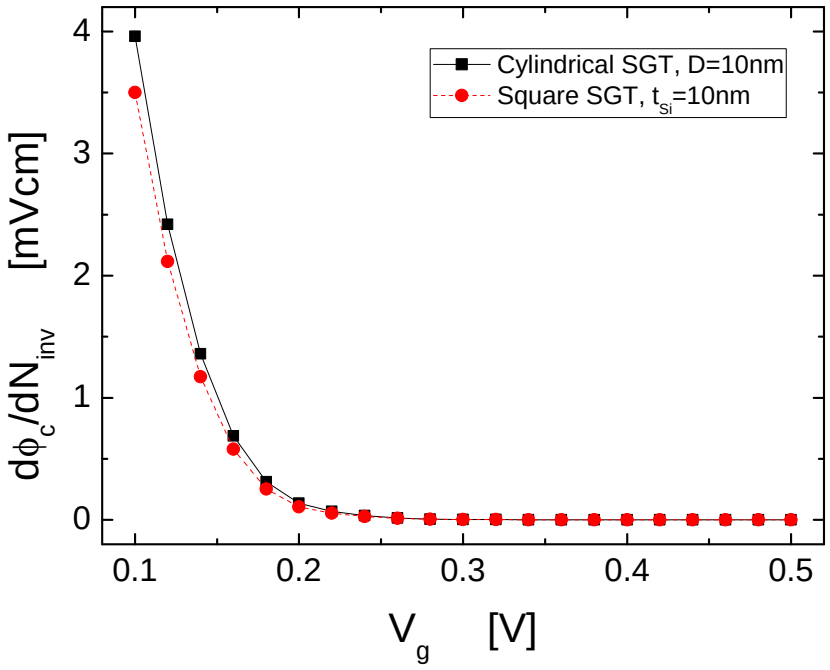


Figure 9: Comparison of $d\phi_{\rm c}/dN_{\rm inv}$ for cylindrical and square GAAs with $t_{\rm Si}$ = 10nm and D = 10nm, respectively.

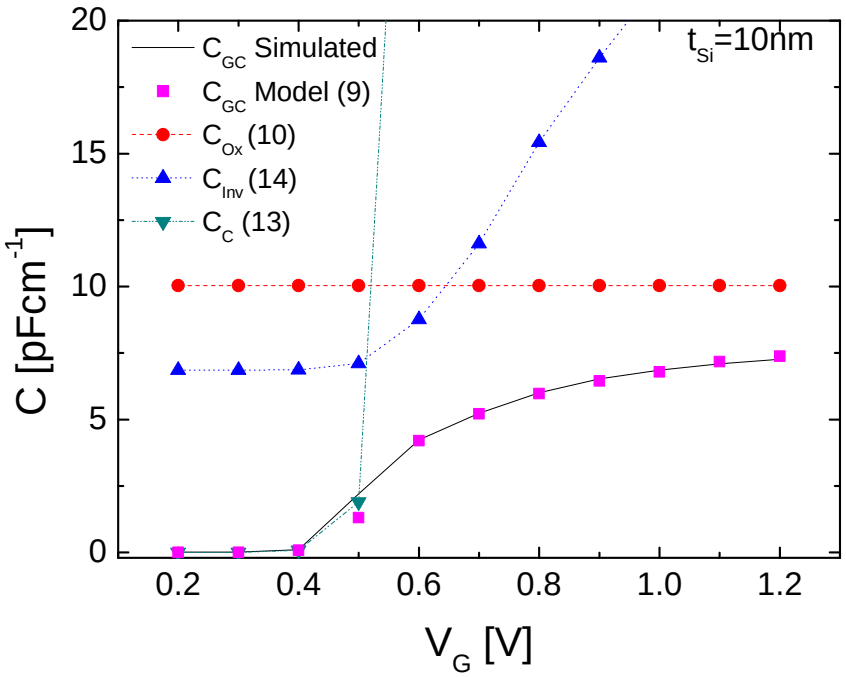


Figure 10: Decomposition of $C_{\rm GC}$ versus $V_{\rm G}$ for a GAA MOSFET with $t_{\rm Si}$ = 10nm into its three components: $C_{\rm ins}$, $C_{\rm inv}$ and $C_{\rm c}$.

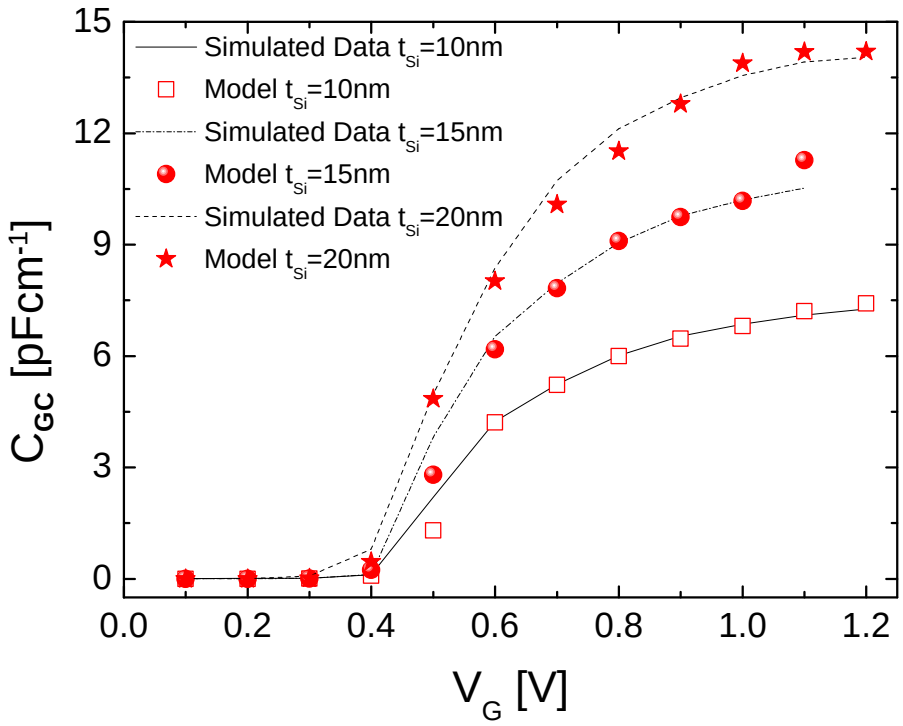


Figure 11: C_{GC} versus V_{G} for GAA MOSFETs of different sizes: results for t_{Si}=10nm, t_{Si}=15nm and t_{Si}=20nm are included. The simulated (modelled) data for the capacitance are shown in solid lines (symbols).

Part II

An analytical model of the potential and charge in square GAA MOSFETs

7 Electric potential modeling

The electric potential in the silicon channel of the device shown in figure 1 has been obtained by solving Poisson's equation making use of the coordinate system sketched in the figure. I have only accounted for electron charge in my calculations (holes are neglected considering that $\frac{q\psi}{kT} > 1$ as well as the depletion charge because of the use of an undoped or lightly doped silicon core, it is supposed that $N_A, N_D << n$). For the calculation of electric potential Poisson's equation holds.

$$\frac{\partial^2\psi(x,y)}{\partial x^2} + \frac{\partial^2\psi(x,y)}{\partial y^2} = \frac{-\rho(x,y)}{\epsilon_{Si}} = \frac{qn(x,y)}{\epsilon_{Si}} = \frac{q}{\epsilon_{Si}} n_i e^{\frac{q\psi(x,y)}{KT}} \tag{16}$$

where q is the electronic charge, ϵ_{Si} is the silicon permittivity, K is Boltzmann's constant, T stands for the temperature and n_i for intrinsic electron density. Poisson's equation solutions can be built by using equation 17 (see the Appendix A).

$$\psi(x,y) = \frac{1}{\beta} Ln\left(\frac{8\phi'(z)\phi'^*(z)}{\alpha\beta\left(1-\phi(z)\phi^*(z)\right)^2}\right) \tag{17}$$

It is important to highlight that the complex function $\phi(z)$, can be described as $\phi(z) = u(x,y) + iu(x,y)$; therefore, the electric potential can be written as $\psi(x,y)$. In order to determine completely the expression of the electric potential I considered the boundary conditions along the perimeter of the silicon channel, at the silicon-insulator interface. These boundary conditions can be expressed as follows:

$$\vec{\nabla}\psi \cdot \hat{r_i}\Big]_{P_{i,Boundary}} = \Omega \frac{V_G - \Delta\phi_{MS} - \psi(P_{i,Boundary})}{\frac{t_{Ox}}{cos\theta}} \tag{18}$$

where $\hat{r_i}$ are unitary vectors with their initial point at the center of the silicon channel and their direction sweeping different points, $P_{i,Boundary}$, at the insulator-semiconductor interface, $\theta = arctg\left(\frac{|r_{iy}|}{|r_{ix}|}\right)$, $\Omega = \frac{\epsilon_{Ox}}{\epsilon_{Si}}$ is the ratio between the silicon and oxide permittivities, $\Delta\phi_{MS}$ is the difference between the metal and semiconductor work-functions, V_G is the gate voltage and $\psi(P_{i,Boundary})$ is the value of electric potential at $P_{i,Boundary}$. The evaluation of Equation 18 at two representative points of the silicon-insulator interface (placed in the middle of the silicon channel side $P_{Half-Side} = \left(\frac{t_{Si}}{2}, 0\right)$ and at the corner $P_{Corner} = \left(\frac{t_{Si}}{2}, \frac{t_{Si}}{2}\right)$).

$$\vec{\nabla}\psi \cdot \hat{i}\Big]_{P_{Half-Side}} = \Omega \frac{V_G - \Delta\phi_{MS} - \psi(P_{Half-Side})}{t_{Ox}} \tag{19}$$

$$\vec{\nabla}\psi \cdot \left(\frac{\hat{i}}{\sqrt{2}} + \frac{\hat{j}}{\sqrt{2}}\right)\Bigg]_{P_{Corner}} = \Omega \frac{V_G - \Delta\phi_{MS} - \psi(P_{Corner})}{\sqrt{2}t_{Ox}} \tag{20}$$

Several holomorphic functions, $\phi(z) = u(x,y) + iu(x,y)$, in equation 17 to generate different analytic expressions for the electric potential, $\psi(x,y)$, can be used. One of the simplest could be $\phi_1(z) = mz$, where $m \in \mathbb{R}$ and $z \in \mathbb{C}$.
By rewriting the previous holomorphic function as $\phi_1(z) = mz = u_1(x,y) + iv_1(x,y)$ we can conclude that $u_1(x,y) = mx$ and $v_1(x,y) = my$. Hence, $\phi_1'(z)\phi_1'^*(z) = \left(\frac{\partial u_1}{\partial x}\right)^2 + \left(\frac{\partial v_1}{\partial x}\right)^2 = m^2$ and $\phi_1(z)\phi_1^*(z) = u_1^2 + v_1^2 = m^2(x^2+y^2)$ are obtained. Puting all these results together in equation 17 an analytical solution for the electric potential is obtained:

$$\psi_1(x,y) = \frac{1}{\beta} Ln\left(\frac{8m^2}{\alpha\beta(1-m^2(x^2+y^2))^2}\right) \tag{21}$$

$\psi_1(x,y)$ fulfils equation 16. This function, $\psi_1(x,y)$, was compared with an analytical expression proposed previously (it is given below) as the electric potential for a cylindrical Surrounding Gate Transistors (SGTs) (see reference [2]).

$$\psi(r) = \frac{KT}{q} Ln\left(\frac{-8B}{\delta(1+Br^2)}\right) \tag{22}$$

After changing the Cartesian coordinate system to a cylindrical coordinate system ($x^2+y^2=r^2$), and transforming a few constants ($B=-m^2$, $\delta=\alpha\beta$ and $\beta=\frac{q}{KT}$) it is easy to conclude that equations 21 and 22 are just the same expression. The electric potential shown in 22 worked well in developing an inversion charge model for cylindrical SGTs as explained in reference [2]. Nevertheless, as it will be shown below, the square GAA MOSFET inversion charge model based on $\psi_1(x,y)$ works well only in the subthreshold operation region.
The boundary conditions sketched above can be simplified in this case. So, making use of equation 20 the following equation is obtained.

$$\left(\left.\frac{\partial\psi_1}{\partial x}\right]_{\left(\frac{t_{Si}}{2},\frac{t_{Si}}{2}\right)}\hat{i} + \left.\frac{\partial\psi_1}{\partial y}\right]_{\left(\frac{t_{Si}}{2},\frac{t_{Si}}{2}\right)}\hat{j}\right)\left(\frac{\hat{i}}{\sqrt{2}}+\frac{\hat{j}}{\sqrt{2}}\right) = \Omega\frac{V_G - \Delta\phi_{MS} - \psi_1\left(\frac{t_{Si}}{2},\frac{t_{Si}}{2}\right)}{\sqrt{2}t_{Ox}} \tag{23}$$

Introducing $\psi_1(x,y)$ in the previous expression the following equation is obtained.

$$-\frac{4m^2(x+y)}{\beta\left(m^2\left(x^2+y^2\right)-1\right)} = \frac{\Omega\left(V_G - \Delta\phi_{MS} - \frac{\ln\left(\frac{8m^2}{\alpha\beta\left(\frac{1}{2}m^2t_{\mathrm{Si}}^2-1\right)^2}\right)}{\beta}\right)}{t_{\mathrm{Ox}}} \tag{24}$$

The parameter m can be obtained by solving Equation 24 for different gate voltages V_G.

It is important to assess the appropriateness of the potential proposed by analyzing the inversion charge distribution of the devices under study. Figure 12 shows the simulated inversion charge corresponding to a $t_{Si} = 20nm$ square GAA MOSFET. At high gate voltages (figure 12(a) $V_G > V_t$, where V_t stands for the threshold voltage) the inversion charge is close to the silicon insulator interface, as expected in a MOSFET device. The corners are obviously more inverted since the potential well there is deeper. It can be seen that for an inversion charge model to work well in the strong inversion operation region it is essential to model reasonably well the electric field in the silicon channel square perimeter (to do so it is necessary to develop a model that shows a square shape at high gate voltages). In addition, for gate voltages below the threshold voltage the variation of the electric potential at the semiconductor-insulator interface is not so high. In this case the inversion

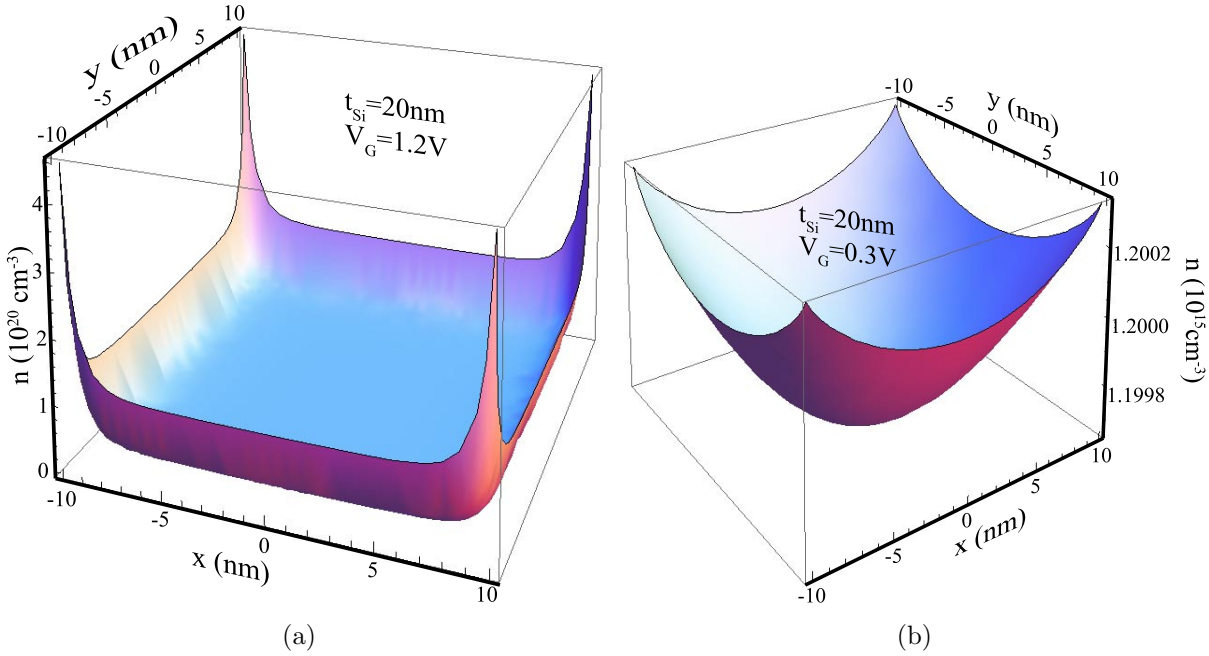


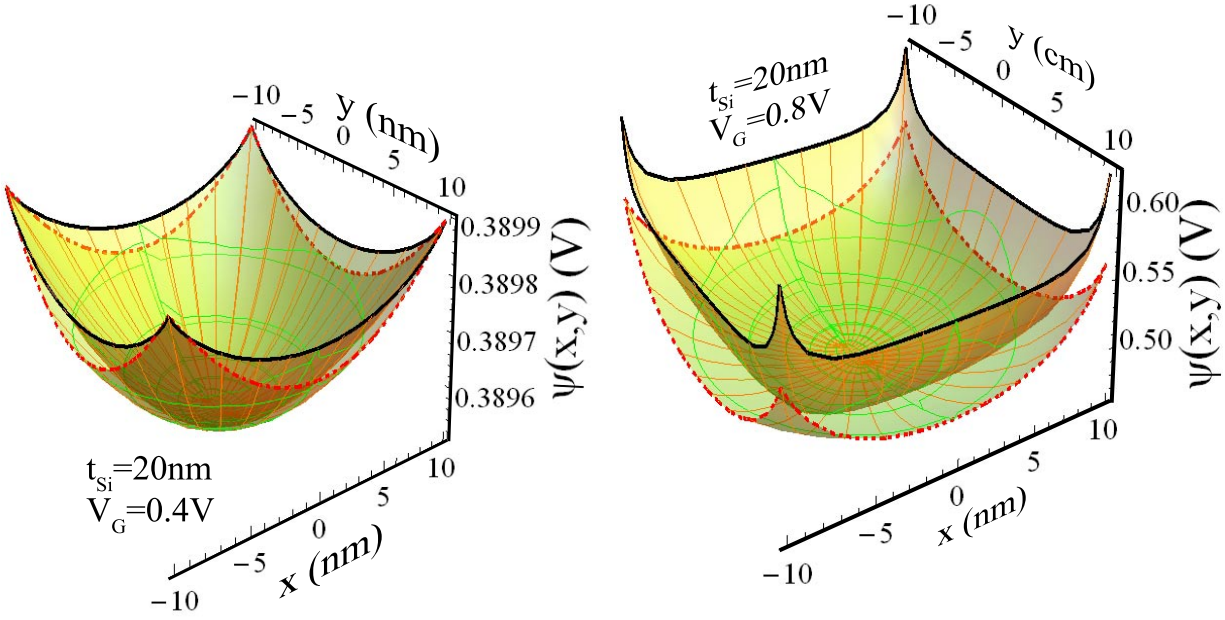
Figure 12: Three-dimensional view of the simulated inversion charge density for a square GAA MOSFET. The device technological parameters were the following: t_{Si} = 20nm, t_{Ox} = 1.5nm, $N_A = 10^{14} cm^{-3}$, $q\phi_m$=4.63 eV. a) $V_G = 1.2V$ and b) $V_G = 0.4V$

charge is mainly placed at the center of the silicon core (volume inversion). It can be seen that the charge has approximately a "cylindrical shape" (if the contribution of the corners is neglected, which is a reasonable approximation). In strong inversion when the inversion charge is placed at the semiconductor-insulator interface, showing a square shape (the inversion charge in the corners is important) a potential such us $\psi_1(x, y)$ (which shows cylindrical symmetry) is not expected to do well. Nevertheless, for the subthreshold operation region $\psi_1(x, y)$ works well as we will show below. In this respect, the lower the t_{Si} value the better this model works since the role played by the corners is less important (volume inversion effects are enhanced).

In order to shed light on this issue, the electric potential calculated with Equation 21 and the simulation data for square GAA MOSFETs are shown for two gate voltages 13(a) below and 13(b) above threshold. The accuracy of the model is strongly reduced in strong inversion (figure 13(b)), as expected. For low gate voltages the electric potential at the corners is well reproduced taking into consideration the slight variation in absolute terms of the potential.
It is clear that in order to reproduce the electric potential in all the operation regions a more complex function has to be used. To do so other holomorphic functions have been studied. Among them was the following:

$$\phi_2(z) = mz + n\left(\frac{1}{(z - \imath a)} + \frac{1}{(z + \imath a)} - \frac{1}{(z + a)} - \frac{1}{(z - a)}\right) \tag{25}$$

$\phi_2(z)$ can be written as follows: $\phi_2(x, y) = u_2(x, y) + v_2(x, y)$, where $u_2(x, y)$ and $v_2(x, y)$ are given below:



(a) (b)

Figure 13: Three-dimensional view of the electric potential for a square GAA MOSFET. The technological parameters were the following: t_{Si} = 20nm, t_{Ox} = 1.5nm, $N_A = 10^{14} cm^{-3}$, $q\phi_m$=4.63 eV. The modeled (simulated) data are represented by the surface with dashes (continuous) borders. a) V_G=0.4V, b) V_G=0.8V.

$$
\begin{aligned}
u_2(x,y) &= n\left(\frac{x}{(y-a)^2+x^2}+\frac{x}{(a+y)^2+x^2}-\frac{x-a}{(x-a)^2+y^2}-\frac{a+x}{(a+x)^2+y^2}\right)+mx \\
v_2(x,y) &= n\left(-\frac{y-a}{(y-a)^2+x^2}-\frac{a+y}{(a+y)^2+x^2}+\frac{y}{(x-a)^2+y^2}+\frac{y}{(a+x)^2+y^2}\right)+my
\end{aligned}
$$

A procedure similar to one followed for $\phi_1(z)$, gives the expression below (equation 17):

$$
\psi_2(x,y) = \beta^{-1} Ln\left(\frac{8\left(m^2+\frac{\eta(x,y)+\varphi(x,y)}{(\omega(x,y))^2}\right)}{\alpha\beta\left(1-\frac{\xi(x,y)}{\omega(x,y)}\right)^2}\right) \tag{26}
$$

where,

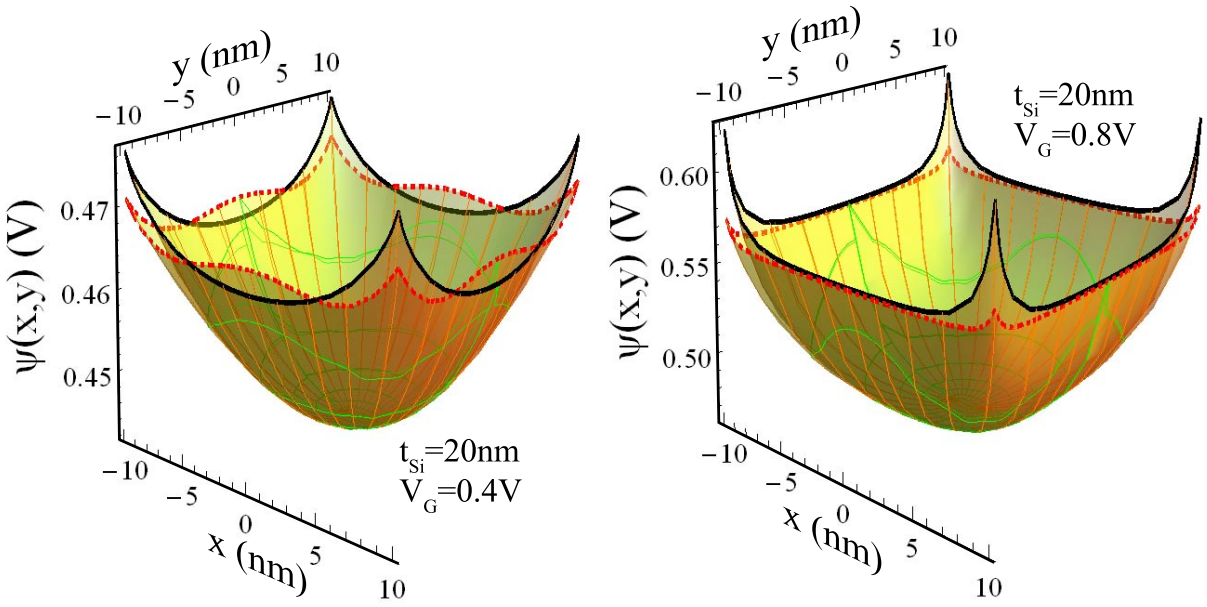
$$
\begin{aligned}
\omega(x,y) &= a^8-2a^4\left(x^4-6x^2y^2+y^4\right)+\left(x^2+y^2\right)^4 \\
\eta(x,y) &= 16a^4n^2\left(a^8+6a^4\left(x^4-6x^2y^2+y^4\right)+9\left(x^2+y^2\right)^4\right) \\
\varphi(x,y) &= 8a^2mn\left(a^{12}+a^8\left(x^4-6x^2y^2+y^4\right)-a^4\left(5x^8+52x^6y^2-34x^4y^4+52x^2y^6+5y^8\right)+\right. \\
&+ \left. 3\left(x^2+y^2\right)^4\left(x^4-6x^2y^2+y^4\right)\right) \\
\xi(x,y) &= \left(x^2+y^2\right)\left(a^8m^2+8a^6mn-2a^4\left(m^2\left(x^4\right.\right.\right. \\
&- \left.\left.\left. 6x^2y^2+y^4\right)-8n^2\right)-8a^2mn\left(x^4-6x^2y^2+y^4\right)+m^2\left(x^2+y^2\right)^4\right)
\end{aligned}
$$

Because of the symmetry of the device under study, it can be deduced that the electric potential satisfies, $\frac{\partial \psi}{\partial x}\Big]_{(0,0)} = \frac{\partial \psi}{\partial y}\Big]_{(0,0)} = 0$, at the center point, $P_{Center} = (0,0)$, as indicated in Figure 1. The m, n parameters have to be determined making use of the boundary conditions 19 and 20. In addition, the **a** parameter was chosen to make function $\psi_2(x,y)$ fit the geometrical restrictions of the potential for different device sizes, and most important (as it will be explained in the next section) to reproduce the inversion charge simulation data. An empirical expression was obtained for **a** parameter in doing so: $a = \frac{t_{Si}}{2} + \delta(V_G, t_{Si})$.

where,

$$\delta(V_G, t_{Si}) = R(t_{Si})(6 - V_G) \tag{27}$$

and $R(t_{Si}) = 0.01998 t_{Si}^2 + 0.27873 t_{Si} + 8.53015$.



(a) (b)

Figure 14: Three-dimensional view of the electric potential for a square GAA MOSFET. The technological parameters were the following: t_{Si} = 20nm, t_{Ox} = 1.5nm, $N_A = 10^{14} cm^{-3}$, $q\phi_m$=4.63 eV. The modeled (simulated) data are represented by the surface with dashes (continuous) borders. a) V_G=0.4V, b) V_G=.2V.

As can be seen in figure 14, $\psi_2(x,y)$ reproduces reasonably well the simulated electric potential even for gate voltages above threshold. It will be showed in the next section that this accuracy is enough to reproduce the inversion charge (calculated by means of Gauss's law) for all the operation regions.

Other electric potential functions could be generated by means of different holomorphic functions. We have also used $\psi_3(x,y)$, generated by $\phi_3(z)$ and given below. In this case, the analytic complexity of the electric potential is higher than the two previous cases although the accuracy of the model is improved.

$$\Phi_3(z) = mz + n\left(\frac{1}{(z-a)^2} - \frac{1}{(z+a)^2} + \frac{i}{(z+ia)^2} - \frac{i}{(z-ia)^2}\right),\ a, n, m \in \mathbb{R},$$

8 Inversion charge calculation

I have made use of Gauss's law to obtain the inversion charge of square GAA MOSFETs. The total inversion charge per unit of length Q_{INV} was calculated by integrating the charge density in the silicon channel.

$$Q_{INV} = \int_{-\frac{t_{Si}}{2}}^{\frac{t_{Si}}{2}} \int_{-\frac{t_{Si}}{2}}^{\frac{t_{Si}}{2}} \rho(x,y)dxdy = 8\epsilon_{Si} \int_{0}^{\frac{t_{Si}}{2}} -\frac{\partial\psi(x,y')}{\partial x}\Big]_{x=\frac{t_{Si}}{2}} dy' \tag{28}$$

the symmetry of the device under study was used in the right-and part of equation 28, where the integral of the electric field along the GAA MOSFET silicon-insulator interface was calculated. Making use of $\psi_1(x,y)$), the electric field can be calculated as follows: $\frac{\partial\psi_1}{\partial x}\Big]_{x=\frac{t_{Si}}{2}} = -\frac{2m^2 t_{\mathrm{Si}}}{\beta\left(m^2\left(\frac{t_{\mathrm{Si}}^2}{4}+y^2\right)-1\right)}$.

Therefore, the expression for the inversion charge per unit of length in this case was given by:

$$Q_{INV} = -\frac{32\cdot 10^7 m t_{\mathrm{Si}}\epsilon_{\mathrm{Si}} Arctan\left(\frac{mt_{\mathrm{Si}}}{\sqrt{m^2 t_{\mathrm{Si}}^2-4}}\right)}{\beta\sqrt{m^2 t_{\mathrm{Si}}^2-4}} \tag{29}$$

The inversion charge calculated through Equation 29 was compared with simulated data (Figure 15) for GAA MOSFETs with different silicon channel thicknesses. It can be seen that this model reproduces accurately the inversion charge in the subthreshold operation region. However, it does not fit the simulation data in the strong inversion regime, as expected.

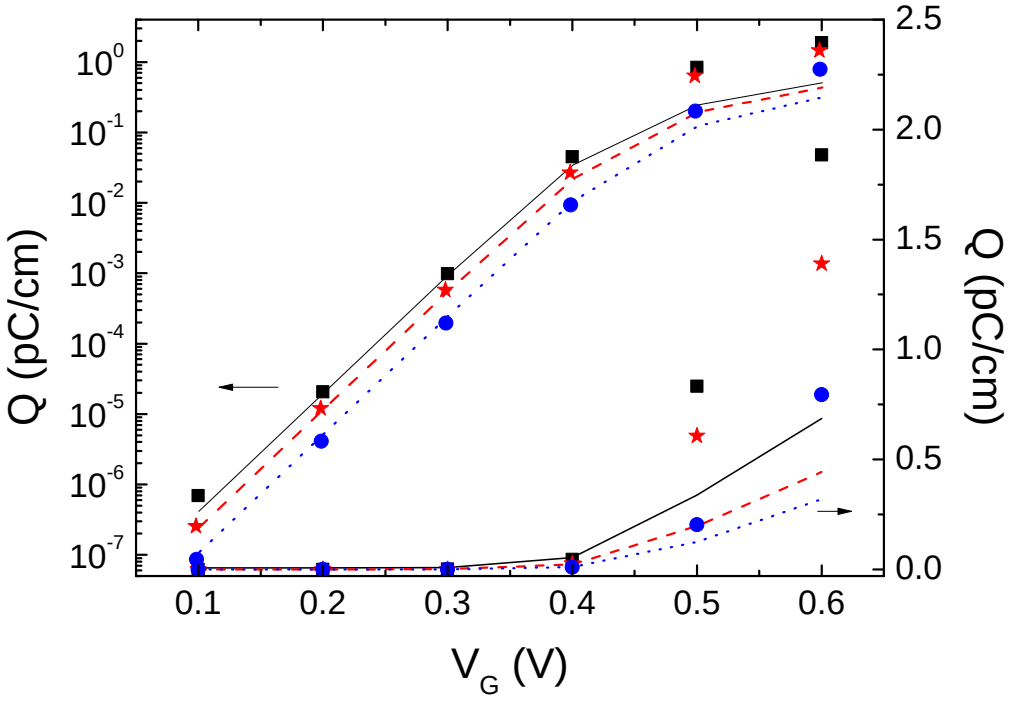


Figure 15: Inversion charge versus gate voltage for a square GAA MOSFETs with different t_{Si} values. Simulation data are shown in symbols and modeled data (for $\psi_1(x,y)$) are plotted in lines.

I have also used $\psi_2(x,y)$ to calculate the inversion charge by means of Equation 28. Figure 16 shows the modeled inversion charge data comparing with simulations. In this case, a good fit is

obtained for all the gate voltages considered in this work. Parameter **a** was tunned to improve the fitting, and an empirical expression (equation given in the previous section) was used to reproduce the values obtained. It can be seen that the fitting of the subthreshold operation region is good for all the silicon layer thicknesses considered.

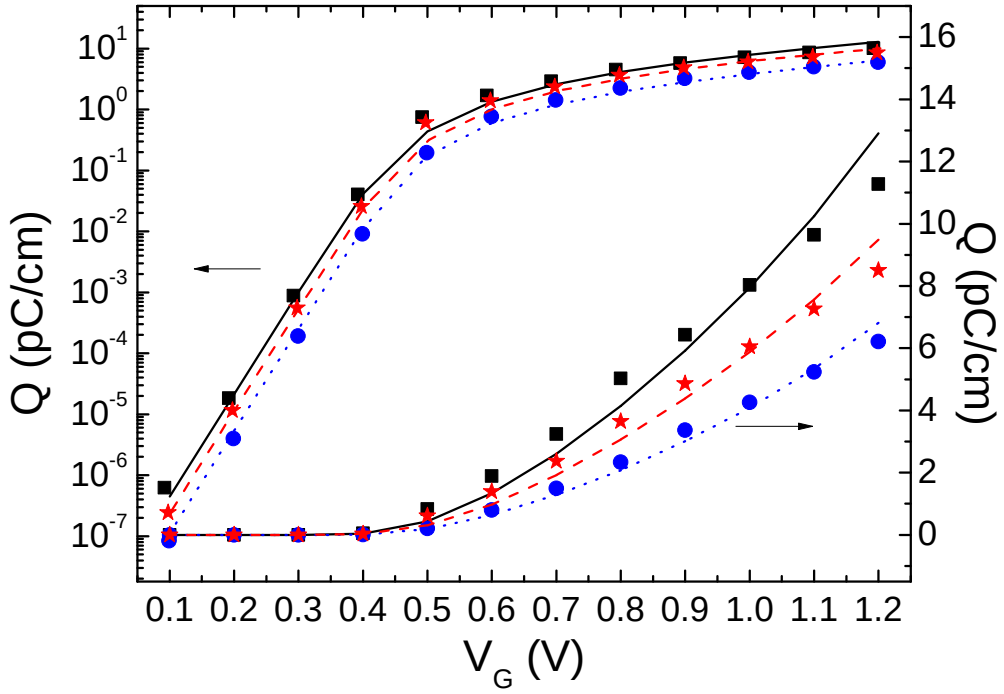


Figure 16: Inversion charge versus gate voltage for a square GAA MOSFETs with different t_{Si} values. Simulation data are shown in symbols and modeled (for $\psi_2(x, y)$) data are plotted in lines.

9 Conclusions

In this first part, an analytical model for the inversion charge distribution function of GAA MOSFETs where quantum effects have been taken into account has been introduced. The model has been tested by means of a comparison with simulation data obtained by self-consistently solving the 2D Schrödinger and Poisson equations for a wide variety of device sizes and bias ranges.
I have also calculated the inversion charge centroid and gate-to-channel capacitance by using the inversion charge distribution function developed previously. A very good agreement between the simulated and modelled data was achieved both for the ICC and the $C_{\rm GC}$ for different sizes and for all the operational regimes.
In the second part, Poisson's equation 16 is solved A, and it has allowed to obtain the electric potential in the silicon channel of square GAA MOSFETs. This potential has been used to calculate the total inversion charge per unit of length Q_{INV} by using Gauss's law for several device sizes and all operative range of voltages.
The simplicity and accuracy of the models presented are very promising from the compact modelling point of view since GAA MOSFETs are considered good candidates for future sub-22nm integrated circuit technologies.

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A Appendix

Equation 16 can be rewritten as follows for simplicity:

$$\Delta\psi(x,y) = \alpha e^{\beta\psi(x,y)} \tag{30}$$

where $\alpha = \frac{q}{\epsilon_{Si}} n_i$ and $\beta = \frac{q}{KT}$.

In order to find an analytic function $\psi(x,y)$, solution of the differential equation 30, a general function to find electric potential analytical expressions $\psi(x,y)$ that fulfill equation 30 has been deduced. It can be seen that equation 30 is a particular case of equation 31):

$$\Delta\psi(x,y) = \epsilon f(x,y) e^{\beta\psi(x,y)} \tag{31}$$

I. Sabitov [34] found the following general solution for equation 31:

$$\psi(x,y) = \frac{-2}{\beta} Ln\left(\frac{|\beta|\,|F(z)|\,(1 - 2\epsilon\beta^{-1}\phi(z)\phi^*(z))}{4\,|\phi'(z)|}\right) \tag{32}$$

where $|F(z)|^2 = f(x,y)$, $\epsilon = \pm 1$ and $\phi(z)$ an arbitrary holomorphic [1] [2] function.
We have obtained a more appropriate general function and proved that solutions for equation 31 can be built as given in the following equation (see reference [36]):

$$\psi\,(x,y) = -\frac{2}{\beta} \ln \frac{\sqrt{\frac{|\beta|}{2}}\,|F\,(z)|\,(1 - \varepsilon \operatorname{sgn}\beta\ \phi\,(z)\,\phi^*\,(z))}{2\,|\phi'\,(z)|}. \tag{33}$$

It can be shown that equations 32 and 33 are equivalent. It can also be seen that equation 30 can be obtained from 31 if $\epsilon = +1$ and $f(x,y) = \alpha > 0$. Therefore, a general solution for equation 30 could be given by the following expression:

$$\psi\,(x,y) = -\frac{2}{\beta} \ln \frac{\sqrt{\frac{\alpha\beta}{2}}\,(1 - \phi\,(z)\,\phi^*\,(z))}{2\,|\phi'\,(z)|} = \frac{1}{\beta} Ln\left(\frac{8\phi'(z)\phi'^*(z)}{\alpha\beta\,(1 - \phi(z)\phi^*(z))^2}\right) \tag{34}$$

[1] An holomorphic function is a complex-valued function of one or more complex variables that is complex-differentiable in a neighborhood of every point in its domain. The phrase "holomorphic at a point z_0" means not just differentiable at z_0, but differentiable everywhere within some neighbourhood of z_0 in the complex plane. If U is an open subset of the complex plane, $\mathbb{C}$, then a function $\phi : U \to \mathbb{C}$ is holomorphic and its derivative is everywhere non-zero on U if and only if it is conformal (or angle-preserving) at u_0 and if it preserves oriented angles between curves through u_0 with respect to their orientation [35].

[2] If a complex function $\phi(z) = u(x,y) + \imath\, v(x,y)$ (where $z = x + \imath\, y \in \mathbb{C}$) is holomorphic, then u(x,y) and v(x,y) first partial derivatives with respect to x and y exist and satisfy the CauchyRiemann equations $\frac{\partial u}{\partial x} = \frac{\partial v}{\partial y}$ and $\frac{\partial u}{\partial y} = -\frac{\partial v}{\partial x}$. [35]

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