# Study of the Gate Capacitance of GaAs, InAs and InGaAs Nanowires

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## ABSTRACT

In this work, a simulation-based study of the gate capacitance of III-V nanowires is performed by using a 2D Schrödinger-Poisson solver. The effective mass approximation, including non-parabolic corrections, is used to model the semiconductor conduction band. Also, wave-function penetration into the gate dielectric is considered. We assess the impact of parameters such as the gate-insulator effective mass and the satellite conduction band valleys energy offsets.

## 1. INTRODUCTION

The combination of both, nanowire (NW) architectures and III-V semiconductor materials are among the most promising candidates for future technology nodes. The reduction of the Short-Channel Effects (SCEs) provided by NWs and the higher electron mobility achieved with III-V compounds may allow a further integration density while increasing the device performance [1]. However, the low conduction effective mass (m*) of III-V semiconductors (particularly that associated to their Γ valley), which is the reason of the higher electron mobility, is also related to one of the main limitations of these III-V-based devices: the decrease of the inversion-layer capacitance [2]. In this work, the gate capacitance ($C_G$) of NWs with GaAs, InAs and $In_xGa_{1-x}As$ compounds is studied by means of numerical simulations. In the following, x=0.53 is employed for the ternary semiconductor, InGaAs.

## 2. SIMULATOR AND DEVICES DESCRIPTION

The electrostatic behavior of long-channel NWs is calculated by solving the 2D Schrödinger-Poisson equations in a cross-section, which provides us with the subband structure of the conduction band (CB). The effective mass approximation (EMA) is used to model the three kinds of valleys (Γ, X and Λ) of the CB. Table I shows the parameters used in this work, achieved from [3] and [4], to model each valley. Due to the high value of the non-parabolic parameters, especially for the Γ valley $\alpha_\Gamma \approx 1eV^{-1}$, the inclusion of non-parabolic corrections is needed to achieve accurate results [5]. To do so, we have followed the method proposed in [6]. Finally, wave-function ($\Psi$) penetration into the gate-insulator is allowed by introducing as additional boundary conditions the continuity of $\Psi$ and $M^{-1}\nabla\Psi$ at the semiconductor-insulator interface, where $M$ is the effective mass tensor in the confinement plane. The second boundary condition needs the effective mass of the gate-insulator, for which uneven values are found in the literature [7,8].

| | GaAs [3]/[4] | InGaAs [3]/[4] | InAs [3]/[4] |
|---|---|---|---|
| $E_\Gamma$ (eV) | 1.518 / 1.519 | 0.730 / 0.830 | 0.416 / 0.417 |
| $E_L$ (eV) | 2.003 / 1.981 | 1.480 / 1.182 | 1.140 / 1.133 |
| $E_X$ (eV) | 1.812 / 1.815 | 1.980 / 1.563 | 1.477 / 1.433 |
| $m_\Gamma$ ($m_0$) | 0.082 / 0.067 | 0.045 / 0.052 | 0.026 / 0.026 |
| $m_{Ll}$ ($m_0$) | 1.610 / 1.900 | 1.232 / 1.661 | 1.707 / 0.640 |
| $m_{Lt}$ ($m_0$) | 0.126 / 0.075 | 0.061 / 0.115 | 0.106 / 0.050 |
| $m_{Xl}$ ($m_0$) | 1.705 / 1.300 | 1.209 / 4.553 | 7.079 / 1.130 |
| $m_{Xt}$ ($m_0$) | 0.236 / 0.230 | 0.193 / 0.233 | 0.232 / 0.160 |

Table I. III-V semiconductor parameters.

## 3. RESULTS

Cylindrical NWs oriented along the [100] direction have been simulated. Semiconductor diameters range from 5nm to 15nm. $Al_2O_3$ is considered as gate insulator (dielectric constant $\varepsilon_r = 9\varepsilon_0$), with a constant insulator thickness of $T_{ins}$=2nm. A metallic gate with work function $\Phi_m$=5.05eV is used. No interface charge is included in the simulations.

First, the influence of simulation conditions is studied. InGaAs NWs have been simulated with the two different sets of parameters shown in Table I. The resulting $C_G$-$V_G$ curve is shown in Fig. 1, including $V_{T\Gamma}$, $V_{TL}$ and $V_{TX}$, defined as the Γ, L and X valleys threshold voltage, respectively. The lower the gap of a valley, the lower its threshold voltage: thus, $V_{T\Gamma}$ coincides with the device threshold voltage ($V_T$). The $C_G$ values achieved for both sets of parameters are quite similar in the range between $V_{T\Gamma}$ and $V_{TL}$. However, for $V_G > V_{TL}$ the population of the satellite valleys increases and, due to their higher m*, their contribution to $C_G$ becomes more and more significant. Therefore, the considered value for the Γ-L valleys gap clearly influences the $C_G$ curve, as shown in Fig. 1, where a hump is observed where the satellite valleys are activated. When the parameters from [4] are considered, a shoulder is observed near $V_{TL}$ ($V_G \approx 0.7V$), which is associated to an increase of the L valley population. On the other hand, when the second set of parameters is taken into account (from ref. [3]), the shoulder appears at higher gate voltages ($V_G \approx 1.5V$ for d=15nm, $V_G \approx 1.2V$ for d=5nm), as expected from the larger difference between $E_{g\Gamma}$ and $E_{gL}$. In the following, parameters from [3] will be used.

A second simulation-related effect that can modify the calculated $C_G$ behavior is the inclusion of wave function penetration into the gate insulator (see Fig. 2). Assuming an infinite potential barrier in the insulator, the minimum energy of the Γ valley subbands is raised, increasing $V_{T\Gamma}$. Moreover, the infinite barrier potential approximation underestimates $C_G$: the charge density is pushed away from the gate insulator, increasing the inversion layer centroid and thus reducing the inversion capacitance [9].

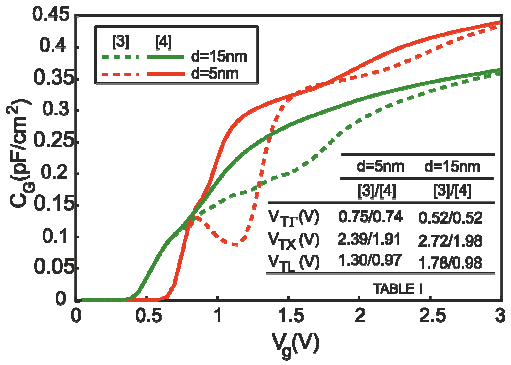


Fig. 1. $C_G$ for 5nm and 15nm diameter InGaAs NWs. Two sets of material parameters, achieved from [3] and [4], are used.

An additional consideration to take into account when allowing the wave function penetration into the gate dielectric is the effective mass of the insulator. Fig. 2 includes a comparison for two different values of $m_{ox}$ [7,8]: the larger $m_{ox}$, the lower $V_{T\Gamma}$, and the higher the difference with the infinite potential barrier. These effects are more noticeable for smaller NWs.

When comparing the $C_G$ of InAs, InGaAs and GaAs NWs, there are several effects that determine their behavior:

i. A reduction of the threshold voltage can be expected when the In molar fraction in the $In_xGa_{1-x}As$ compound increases, due to the grow of the semiconductor electron affinity ($\chi_s$).
ii. The lower the confinement effective mass for the Γ valley, the higher the energy separation from the conduction band minimum. Again, as shown in Table I, a higher In content in the $In_xGa_{1-x}As$ compound implies a lower Γ valley effective mass.
iii. The wave function penetration into the gate insulator is especially relevant for large $m_{ox}$–$m_s$ discontinuities. Therefore, it has a greater impact on smaller effective mass semiconductors (i.e., InAs), adding up to the previous effects.

Figure 3 shows the electron density per unit length ($N_t$) as a function of $V_G$ for NWs with the three semiconductors considered and 5nm and 15nm diameters. In the $V_G$ range between $V_{T\Gamma}$ and $V_{TL}$, the conduction effective mass coincides with the Γ valley mass, thus providing its well-known beneficial effects on the transport properties (high mobility). Moreover, InGaAs devices achieve the highest separation between $V_{T\Gamma}$ and $V_{TL}$ for the two device sizes considered. However, and despite the larger value of $E_L$–$E_\Gamma$ of InAs, $V_{TL}$–$V_{T\Gamma}$ is not as large as it could be expected for this material. The reason may be found in the higher energy separation from the conduction band minimum, due to the lower effective mass. In all the cases, the shrinking of the device sizes reduces $V_{TL}$–$V_{T\Gamma}$, due to the increase on $V_{T\Gamma}$.

As a drawback, in the same $V_G$ range where the higher mobility is expected, the so-called density of states bottleneck appears, limiting the gate capacitance (see Fig. 4). The gate capacitance is increased to acceptable values when L valleys get populated, and devices with smaller $V_{TL}$–$V_{T\Gamma}$ (GaAs) present better $C_G$–$V_G$ curves.

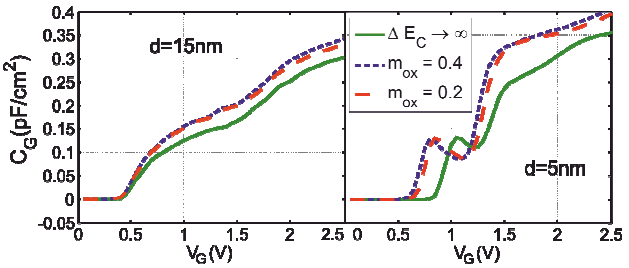


Fig. 2. $C_G$ for InGaAs NWs with 15nm (left) and 5nm (right) diameter, with and without wave function penetration into the insulator.

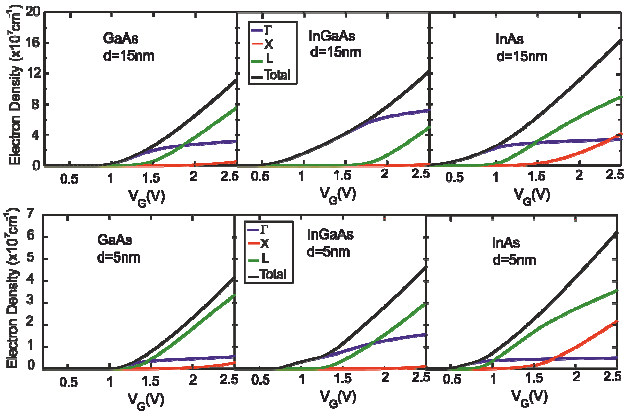


Fig. 3. Electron density per unit length corresponding to 15nm (first row) and 5nm (second row) NWs with GaAs, InGaAs and InAs (left, center and right columns, respectively). Black, blue, green and red lines stand for the total electron density and Γ, L and X valleys, respectively.

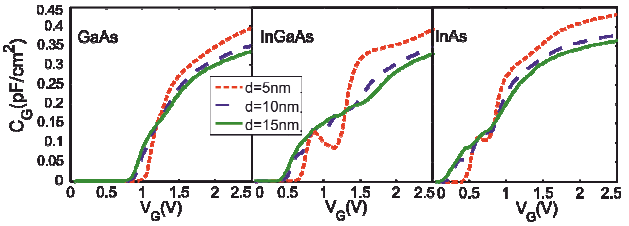


Fig. 4. $C_G$ vs $V_G$ for GaAs (left), InGaAs (center) and InAs (right), for 5nm, 10nm and 15nm diameter nanowires.

## 5. ACKNOWLEDGMENT

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