UNIVERSIDAD DE GRANADA

Universidad de Granada

Doctoral Thesis

STUDY OF ALGAN/GAN HEMTS WITH ADVANCED PROCESS STEPS FOR KA-BAND APPLICATIONS

Author:

Ming-Wen Lee

Advisors:

Dr. Edward Yi Chang

Dr. Francisco Jesús Gámiz Pérez

A thesis submitted in fulfillment of the requirements
to obtain the Dual Doctor Degree as part of the
Programa de Doctorado en Technología de la Informacíon y la Comunicación
at the Nanoelectronics Research Group, CITIC-UGR, with the
International College of Semiconductor Technology,
National Yang Ming Chiao Tung University, Taiwan
Department of Electronics and Computer Technology

Granada, 25th July, 2024

應用於 Ka-Band 頻段之氮化鋁鎵/氮化鎵高電子遷移率電晶體先進製程研究

Study of AlGaN/GaN HEMTs with Advanced Process Steps for Ka-Band Applications

研 究 生：李明文　　Student：Ming-Wen Lee

指導教授：張翼 教授　　Advisor：Prof. Edward Yi Chang

指導教授:Francisco Gamiz教授　Advisor: Prof. Francisco Gamiz

國立陽明交通大學 國際半導體產業學院

博士論文

A Dissertation
Submitted to International College of Semiconductor Technology of
National Yang Ming Chiao Tung University
in partial Fulfillment of the Requirements
for the Degree of Doctor of science in Semiconductor Technology
and Submitted to the Dual Doctoral Program in Information and
Communication Technologies (B25.56.1) of the
University of Granada, Spain.

Universidad de Granada

CITIC-UGR

July 2024
Taiwan, Republic of China

中華民國 一一三年七月

Editor: Universidad de Granada. Tesis Doctorales
Autor: Ming-Wen Lee
ISBN: 978-84-1195-557-7
URI: https://hdl.handle.net/10481/97429

誌謝

Acknowledgements

謝謝我的指導教授 張翼教授在博士論文期間給予如此多的資源和信任。謝謝我的實驗室組長 林岳欽博士，在我研究的時候細心且不厭其煩的提攜我，並且在專業領域上鞭策我成長。感謝實驗室的學長和學弟們:果然翁、賴冠銜、莊正緯與我一同完成論文發表。感謝西班牙的 Francisco Gamiz 教授以及 Carlos Marquez 教授提供 TCAD 教導以及雙聯學位的指導，使我能順利完成雙聯博士學位。感謝我的媽媽，無條件地支持我讀研究所。感謝女友陪伴著我的研究生活。感謝上帝，賜給我健康的身體和心靈可以完成學業。

應用於 Ka-Band 頻段之氮化鋁鎵/氮化鎵高電子遷移率電晶體先進製程研究

博士生：李明文　　指導教授：張　翼　教授

國立陽明交通大學

國際半導體產業學院博士班

摘要

隨著物聯網、無人機以及 AI 的應用越加廣泛，使用者端對於 5G 以及 B5G 通訊技術的需求與日俱增，現有頻段的通訊技術亦面臨傳輸頻段訊號壅塞，造成訊號傳輸速度變慢、效率降低、能量損耗增加等問題。因此，極需要提升通訊元件的操作頻率來擴增可使用的頻段。

此篇論文將藉由開發先進的元件製程技術來提升氮化鎵元件在高頻 Ka-Band 通訊環境的特性表現。首先，藉由使用步進式曝光機，開發二階段式的曝光技術，取代傳統電子束曝光機，在四吋晶圓上製作具高均勻性的小線寬元件，不僅能大幅降低製程時間、製作成本，也提升元件良率。此篇論文也成功使用二階段式的曝光技術製作 100 奈米閘極小線寬，藉以使 2×25 微米的元件輸出超過 10 瓦的功率密度。

為了進一步提升高頻元件的高頻線性度，也使用 TCAD 模擬技術輔助開發閘極鰭式蝕刻結構，用以平坦化高頻元件轉導曲線以及降低高

頻三階項的訊號，降低對主頻訊號的干擾。此篇研究中，一共探討了四種蝕刻閘極結構，分別是平坦閘極、兩片鰭式閘極、五片鰭式閘極以及十片鰭式閘極。本小訊號實驗結果顯示五片鰭式閘及元件具有最高的截止頻率以及最大震盪頻率。同樣的，五片鰭式閘極元件也具有在 V_{GS} 為 0.5 V 、0.25 I_{DSS} 以及 V_{DS} 為 20 V 時擁有最好的功率增益、OIP3-P1dB、IMD3。整體而言，鰭式閘極元件都較平坦閘極元件具有更高的功率和線性度表現。

同時，氮化鎵高電子遷移率元件的截止頻率、最大增益頻率以及高頻功率表現也取決於源極以及汲極接觸電阻。透過開發以及製作圖形化蝕刻歐姆區域氮化鎵元件，可以有效降低接觸電阻並提升直流和高頻特性。此篇研究具有四種歐姆蝕刻圖型，分別是直徑一微米的圓洞、直徑三微米的圓洞、寬度為一微米的長方形凹槽以及寬度為三微米的長方形凹槽。在此四種元件當中，擁有寬度為一微米的長方形凹槽的元件具有最低的接觸電阻(0.154 Ω·mm)以及接觸電阻率(4.04×10^{-7})，並在高頻和雜訊表現中最具 Ka Band 應用潛力。

最後，為了避免氮化鎵元件在高頻環境中的集膚效應且有效降低製程成本，此篇論文也探討使用厚銅金屬連接線技術，降低源極以及汲極電阻，且在提升高頻功率特性的同時，維持元件在高溫和高壓操作環境

中的可靠度。此篇研究使用四微米的厚銅金屬薄膜，並分析阻障層在高溫環境和高壓測試下的穩定度以及可靠度表現。結合此厚銅技術，研究中的元件可達到功率密度 6.6 瓦的功率表現，以及功率轉換效益高達 45.6 %，顯示出厚銅連接線在高頻應用的優異表現。

關鍵詞：氮化鎵高電子遷移率電晶體、高頻、小線寬、鰭式閘極、厚銅連接線、歐姆區域圖形蝕刻、TCAD 模擬。

Estudio de HEMT de AlGaN/GaN con procesos avanzados para aplicaciones en banda Ka

Doctorando: Lee, Ming-Wen / pasaporte: 352266013

Advisor：Prof. Edward Yi Chang

Co-Advisor: Prof. Francisco Gamiz

Resumen

Con el rápido crecimiento de las aplicaciones de Internet de las cosas, vehículos aéreos no tripulados e inteligencia artificial, la necesidad de tecnología de electrónica de consumo 5G y más allá de 5G (B5G) ha crecido rápidamente, y los anchos de banda de frecuencia actuales para la transmisión de datos se enfrentan a la congestión.

Como resultado, la capacidad de transmisión depende del desarrollo de transistores de mayor frecuencia para aumentar la operatividad de los amplificadores de potencia y los amplificadores de bajo ruido y ampliar el ancho de banda de frecuencia para una mayor velocidad de transmisión de datos con interferencias de señal reducidas.

Esta tesis abarca el desarrollo y la fabricación de transistores de alta movilidad electrónica AlGaN/GaN de banda Ka, utilizando cuatro pasos de procesos avanzados, como el proceso fotolitográfico en dos pasos, la simulación TCAD de HEMT y su fabricación mediante grabados en trinchera, los HEMT con patrón de grabado óhmico y el desarrollo de una interconexión de metalización gruesa de cobre.

En primer lugar, se utiliza el proceso fotolitográfico de 2 pasos con la litografía paso a paso (stepper) para superar las limitaciones de escalado de puerta y aumentar la rentabilidad con una alta uniformidad en oblea de 4 pulgadas. El dispositivo HEMT de GaN de pequeña longitud de puerta (con una longitud de puerta de 100 nm) se fabrica con éxito mediante este método. También se midió una alta densidad de potencia de más de 10 W/mm para los dispositivos fabricados de 2×25 μm. Además, se midió la uniformidad de la oblea fabricada con respecto a I_{DSS}, transconductancia extrínseca (G_m) y voltaje umbral (V_{th}). En general, los resultados de demostraron una alta uniformidad de la oblea fabricada adecuada para la producción en masa.

En segundo lugar, el estudio analiza la simulación TCAD y la fabricación de HEMT mediante grabados en trinchera para mejorar la planaridad de la curva de transconductanza (G_m) y reducir la intermodulación de tercer orden para aumentar el rendimiento de linealidad en alta frecuencia del dispositivo. En este estudio se diseñaron cuatro estructuras de puerta *finfet* diferentes: la planar, la de 2 *fins* (grabado de un *fin*), la de 5 fins (grabado de 4 fins) y la de 10 aletas (grabado de 9 fins). Los resultados de pequeña señal mostraron que los dispositivos con 5 *fins* tienen los valores de frecuencias f_T y f_{max} más altos, superando a los dispositivos de 10 *fins*. Por otro lado, los dispositivos de 5 *fins* mostraron los mejores valores de ganancia de potencia, OIP3-P_{1dB} e IMD3 sobre las otras tres estructuras diseñadas a V_{GS} de 0.5 y 0.25 I_{DSS} y V_{DS} de 20 V. Todos los dispositivos con puerta en forma de *fin* muestran un mayor rendimiento lineal en comparación con los dispositivos planares con respecto a los valores G_m, OIP3-P_{1dB} e IMD3.

En tercer lugar, los patrones de grabado óhmico de este estudio se han aplicado a dispositivos HEMT de AlGaN/GaN que funcionan a la frecuencia de la banda Ka con una resistencia de contacto reducida para mejorar el rendimiento en corriente continua (CC) y radiofrecuencia (RF). En este estudio se fabricaron cuatro diseños de patrones de grabado óhmico: líneas de 1 μm, líneas de 3 μm, agujeros de 1 μm y agujeros de 3 μm. Los dispositivos con el patrón de líneas de 1 μm mostraron la resistencia de contacto más baja de 0.154 Ω-mm y una resistividad de contacto de 4.04×10^{-7} entre los cuatro dispositivos diseñados. Los dispositivos con patrones de líneas de 1 μm muestran los resultados más prometedores entre los cuatro dispositivos diseñados aptos para aplicaciones en banda Ka.

Por último, el estudio muestra el desarrollo de una interconexión metálica de gran espesor de cobre para mejorar la resistencia de la fuente y el drenador del dispositivo y mitigar el efecto *Skin* en alta frecuencia con un bajo coste de fabricación y una alta fiabilidad. Las interconexiones metálicas de cobre se fabricaron en los dispositivos HEMT una vez definida la estructura del dispositivo. En este estudio también se realizaron pruebas térmicas y de estrés para los HEMT metalizados con el fin de demostrar la estabilidad de la barrera diseñada. También se midió una alta densidad de potencia de salida de 6.6 W/mm con una PAE del 45.6% para los dispositivos HEMT metalizados con cobre, lo que demuestra un gran potencial para aplicaciones de alta potencia en banda Ka.

Palabras clave: gallium nitride, high-electron-mobility transistor, longitud de puerta pequeña, puerta grabada en zanja, metalización de cobre grueso, patrones de grabado óhmico, simulación TCAD.

Study of AlGaN/GaN HEMTs with Advanced Process Steps for Ka-Band Applications

Doctorate Student：Lee, Ming-Wen Advisor：Prof. Edward Yi Chang

Advisor：Prof. Francisco Gamiz

International College of Semiconductor Technology

National Yang Ming Chiao Tung University

Abstract

With the rapid growth of Internet of Things, Unmanned Aerial Vehicle, and Artificial Intelligence applications, the need for 5G and Beyond 5G (B5G) consumer electronics technology has grown rapidly, and the current frequency bandwidths for data transmission face congestion.

As a result, the transmission capability relies on the development of higher frequency transistors to increase operational frequency of Power Amplifiers and Low Noise Amplifiers and to broaden the frequency bandwidth for higher data transmission speed with reduced signal interferences.

This thesis covers over the development and fabrication of Ka-Band AlGaN/GaN High-Electron-Mobility Transistors, using four advanced process steps, such as the 2-Step Photolithography Process, the TCAD simulated and fabricated Trench-Etched HEMTs, the Ohmic-Etching Pattern HEMTs, and the development of thick copper metallization interconnect.

First, the 2-Step Photolithography Process done with the Stepper Lithography is used to overcome the gate-scaling limitations of Steppers and

increase cost effectiveness with a high 4-inch wafer uniformity. The small gate length GaN HEMT device with a gate length of 100 nm is successfully fabricated with this method. High power density of more than 10 W/mm were also measured for the fabricated 2×25 μm devices. The wafer uniformity of the fabricated wafer was also measured with respect to I_{DSS}, G_m, and threshold voltage (V_{th}). Overall, the uniformity results demonstrated high wafer uniformity of the fabricated wafer suitable for mass production.

Second, the study discusses TCAD simulated and fabricated Trench-Etched HEMTs for extrinsic transconductance (G_m) curve flatness improvement and 3rd order intermodulation reduction to increase device high frequency linearity performance. Four different fin-gate structure were designed in this study: the planar, the 2 fins (1 etched fin), the 5 fins (4 etched fins), and the 10 fins (9 etched fins) devices. The small signal results showed that the devices with 5 fins have the highest f_T and f_{max} values, performing over the 10 fins devices. The 5 fins devices exhibited the best power gain, OIP3-P1dB, and IMD3 values over the three other designed structures at the V_{GS} of 0.5 and 0.25 I_{DSS} and V_{DS} of 20 V. The fin-shaped gate devices all show increased linearity performance compared to the planar devices with respect to the G_m values, OIP3-P1dB, and IMD3 values.

Third, this study ohmic etching patterns has been applied to AlGaN/GaN HEMT devices that operate at the frequency of Ka Band with decreased contact resistance for Direct Current (DC) and Radio Frequency (RF) performance improvement. Four designs of the ohmic etching patterns were fabricated in this study as 1 μm lines, 3 μm lines, 1 μm holes, and 3 μm holes. The devices with the pattern of 1 μm lines exhibited the lowest contact

resistance of 0.154 Ω·mm and a contact resistivity of 4.04×10^{-7} among the four designed devices. The devices with 1 μm line patterns show the most promising results among the four designed devices suitable for Ka-band applications.

Last, the study shows the development of thick copper metallization interconnect to improve device source and drain resistance and mitigate high frequency Skin Effect with low fabrication cost and high reliability. The thick copper-metallized interconnects were fabricated on the HEMT devices after the definition of the device structure. Thermal and stress tests were also done for the copper-metallized HEMTs in this study to demonstrate the stability for the designed barrier layer. High output power density of 6.6 W/mm with a PAE of 45.6 % were also measured for the copper metallized HEMT devices, demonstrating strong potential for high power applications at Ka Band.

Keywords: gallium nitride, high-electron-mobility transistor, small gate length, trench-etched gate, thick-copper metallization, ohmic-etching patterns, TCAD simulation.

Contents

List of Figures

1 trench, (3) 4 trenches, and (4) 9 trenches, respectively.

Figure 5-2. The measured I_{DS}-V_{GS} and G_m-V_{GS} curves of the devices with planar, 1 trench, 4 trenches, and 9 trenches, respectively.

Figure 5-3. The measured current gain and MAG/MSG versus frequency graphs of the fabricated devices with the planar, 1 trench, 4 trenches, and 9 trenches, respectively.

Figure 5-4. The block schematic diagram of the 2-tone large signal measurement setup.

Figure 5-5. The measured (a) 2-tone load pull power results of the devices with the (1) planar, (2) 1 trench, (3) 4 trenches, and (4) 9 trenches, respectively, and (b) IMD3 – (power backed off from P_{1dB}) graph of the four fabricated devices with $I_{DS} = 0.5\ I_{DSS}$.

Figure 5-6. The measured (a) 2-tone load pull power results of the devices with the (1) planar, (2) 1 trench, (3) 4 trenches, and (4) 9 trenches, respectively, and (b) IMD3 – (power backed off from P_{1dB}) graph of the four fabricated devices with $I_{DS} = 0.375\ I_{DSS}$.

Figure 5-7. The measured (a) 2-tone load pull power results of the devices with the (1) planar, (2) 1 trench, (3) 4 trenches, and (4) 9 trenches, respectively, and (b) IMD3 – (power backed off from P_{1dB}) graph of the four fabricated devices with $I_{DS} = 0.25\ I_{DSS}$.

Figure 5-8. The measured (a) 2-tone load pull power results of the devices with the (1) planar, (2) 1 trench, (3) 4 trenches, and (4) 9 trenches, respectively, and (b) IMD3 – (power backed off from P_{1dB}) graph of the four fabricated devices with $I_{DS} = 0.125\ I_{DSS}$.

Figure 5-9. The measured I_{DS}-V_{GS} and G_m-V_{GS} graphs of the fabricated

Figure 7-12. The measured G_m-V_{GS} results of the fabricated 2×50 μm devices (L_{SD}= 3.0 μm) after various stress tests at 150 °C.

Figure 7-13. The large signal power results of the fabricated 2×50 μm devices with thick copper interconnect (L_{SD}= 3.0 μm) before and after the 10-hour stress test at 150 °C.

Figure 7-14. The measured (a) I_{DS}-V_{DS} and (b) I_{DS}-V_{GS} & G_m-V_{GS} of the fabricated 2×50 μm device with thick copper interconnect (L_{SD}= 2.5 μm) before and after being annealed at 300 °C for 30 minutes.

Figure 7-15. The measured large signal power results of the fabricated 2×50 μm device with thick copper interconnect (L_{SD}= 2.5 μm) before and after being annealed at 300 °C for 30 minutes.

List of Tables

Chapter 1
Introduction

As the need for consumer electronics related to the Internet of Things (IoT), 5th Generation System (5G), and Beyond 5th Generation System (B5G) increases rapidly during the past decade, the current frequency bands face signal congestion. Therefore, the development of higher frequency band systems has become urgent and necessary to increase bandwidth, suitable for high speed and high transmission rate applications. Within the transceiver Integrated Circuit (IC), the Power Amplifier (PA) plays a crucial role in amplifying signals and require large power controllability as well as high efficiency. Among high frequency PAs, the transistors are expected to perform high current gain and high Power-Added-Efficiency (PAE) for signal amplification [1]. Research studies have shown that semiconductor transistors such as III-V High-Electron-Mobility-Transistors (HEMTs) could provide higher current gain, power density, PAE, and current density [2], [3], [4], [5], [6], [7], [8]. GaN-based HEMTs have also exhibit higher drain voltage, saturation current, and PAE over GaAs-based HEMTs due to the higher breakdown voltage and the higher saturation current material properties of Gallium Nitride. In order to increase the operation frequency of GaN-based HEMTs with high power density, it is important to fabricate the GaN HEMT with small gate length, high gate controllability, high device linearity, low contact resistance (R_c), and low source and drain contact resistance (R_s and R_d). Small gate length has been fabricated with the E-beam Lithography System (E-Beam) for device scaling [9], [10], [11]. However, the use of E-Beam requires large production time and precision, increasing

manufacturing cost and complexity. The Stepper Lithography System (Stepper) has been utilized in the fabrication of small gate length GaN HEMTs and introduced in this thesis, demonstrating the use of 2-Step Photolithography Process for large scale wafer fabrication with a high uniformity and an outstanding Radio Frequency (RF) power performance [12]. Improved gate controllability with improved device linearity are also demonstrated in this thesis with the use of Fins and Trenches along the gate width [13]. Sentaurus 2D and 3D Technology Computer Aided Design (TCAD) models are also used to simulate electrical characteristics of the Trench GaN-based HEMT devices linearity optimization[13]. To further improve RF performance, the R_c is improved with the Ohmic Etching Patterns (OEP) due to the increase in contact area and current paths, increasing Source-to-Drain Saturation Current Density (I_{DSS}), transconductance (G_m), small signal performance, and large signal performance [14]. After the decrease of R_c, the R_s and R_d are further reduced with the deposition of a 4 μm thick Copper (Cu) metal film, increasing current density and RF power performance [15].

1.1 Objectives

The main objective is to fabricate a HEMT device suitable for Ka-Band applications through the scaling of gate length dimensions, the increased gate control and device linearity, the improvement in ohmic metal contact resistance, and the reduction of source and drain parasitic resistance.

The advanced process steps are developed for the improvement of DC and RF characteristics, such as I_{DSS}, G_m, small signal performance, and large signal performance. The specific objectives are listed as follow:

Objective 1. The research and development of the 2-step photolithography using the Stepper, and to fabricate high uniformity small gate length HEMT devices with high RF performances, such as high f_T, f_{max}, and high-power density.

Objective 2. The research and development of the fin-gate structure to increase gate controllability and device DC and RF linearity, such as OIP3, IMD3, and P1dB. The results are also validated with the TCAD simulation software to analyze the electrostatic potential influences of different fin gate structures for design optimization.

Objective 3. The research and development of the different ohmic etching patterns for ohmic contact resistivity improvement for HEMT devices. The improvement in ohmic contact resistance increases the small signal and large signal performances as well as noise figure.

Lower contact resistivity results are expected to be achieved through the increased contact area between the metal and semiconductor, increased fringing effects, and tunneling effects.

Objective 4. The research and development of the thick copper metallization

technology is used to reduce the source and drain parasitic resistances of HEMT devices during high frequency applications to mitigate the skin effect. The deposition of the copper metal on top of the contact pads requires a strong barrier layer of Pt to prevent copper interdiffusion.

1.2 Methodology

In order to achieve the objectives above, we have used the following methodology to research on the development of AlGaN/GaN HEMTs for Ka-band applications.

First of all, I performed bibliographic surveys and deep analysis of the state of the art of the AlGaN/GaN HEMTs with high power density RF performance using the Stepper lithography, the AlGaN/GaN HEMTs with enhanced gate controllability and device linearity using the fin-gate structure, the AlGaN/GaN HEMTs with ohmic etching patterns that improves the contact resistivity and power performances, and the AlGaN/GaN HEMTs with thick copper interconnect that enhances power performance during high frequency operation.

Secondly, we carefully design the experiments and structures that we should fabricate and simulate in order to fulfill the Objectives listed in Section 1.1.

Thirdly, to fulfill the four specific objectives mentioned in Section 1.1, the wafers of each process basically follow the same process line of wafer cleaning, ohmic metal formation, ion implantation isolation, 2-step photolithography gate formation, and the final device passivation, as shown among Section 3.1.1 to 3.1.4.

Fourthly, the specific advanced process steps are then further developed and processed for RF performance improvements, such as the 2-step photolithography process, the fin-gate structures, the ohmic etching patterns, and the thick copper interconnects, which are mentioned among Section 3.2 to 3.5.

Lastly, there are also four data measurement technology that are used for data

curation and characterization throughout the thesis, such as the transmission line measurement, DC characteristic analysis, scattering parameters characterization, and the load pull measurement, which are shown among Section 2.1 to 2.4.

Chapter 2

Device Characteristics Measurement and Analysis

2.1 Transmission Line Measurement (TLM)

The Transmission Line Measurement Method is used to characterize the Rc and contact resistivity (ρ_c) of the GaN-based HEMT device through a set of designed TLM patterns. The patterns are designed with a set of metal pads, with a spacing of 3, 5, 10, 20, 36 μm. The analysis of TLM method utilizes the measurement of the current from TLM pads using the Keysight B1505A Power Device Analyzer / Curve Tracer. The measured I_{DS}-V_{DS} curves of the TLM pads are used for resistance extraction. After extrapolation of the resistance values and normalizing the pad widths, the R_c and the ρ_c of the GaN HEMT device could be calculated.

2.2 DC Characteristics

DC characteristics are measured using the Keysight B1505A Power Device Analyzer / Curve Tracer to obtain the I_{DS}-V_{DS}, I_{DS}-V_{GS}, G_m-V_{GS}, and stress tests curves. Power sweeps of V_{GS} from −5 V to 0 V and V_{DS} of 0 V to 25 V are used for measurement of the Depletion-mode HEMT device in this study. The DC results were further plotted with the Origin Pro Software and Microsoft Excel to compare and demonstrate the HEMT device performance.

2.3 Scattering Parameters Characterization

To set up the measure environment, the E8361C PNA network analyzer and the 4142B DC supplier were used for on-wafer S parameter extraction.

Utilizing a two-port network with a reference impedance Z_0, the signal waves are transmitted and matched to obtain S parameters of the measured HEMT devices. The measurement of the S parameters is calibrated with a Short-Open-Load-Through (SOLT) method with an accuracy of less than ±0.01 dB for both the S21 and S12 values and less than −45 dB for both the S11 and S22 values with a frequency range sweep of 100 MHz to 67 GHz. After the extraction of the S parameters, the H21 value to frequency curves and the Maximum Stable Gain (MSG)/Maximum Available Gain (MAG) to frequency curves were calculated and plotted with the Microwave Office 2000 Software for the extrapolation of the Maximum Oscillation Frequency (f_{max}) and the Cut-Off Frequency (f_T).

2.4 Load-Pull Measurement

The on-wafer load-pull measurement system used for 1-tone and 2-tone measurement was set up by the Taiwan Semiconductor Research Institute (TSRI) in Hsinchu, Taiwan. The equipment used for the load-pull measurement includes the Agilent N5227B network analyzer, HP 4142 DC source, bias-T, Keysight N5295AX52 Millimeter-wave VNA Extender, driver amplifier (DA), isolator, Exodus AMP3132A power amplifier, and Focus Delta M120280 harmonic tuner, as shown in shown in Figure 3.4.1. The software for analysis is the Focus Load Pull Explorer, measuring the DUT of two port devices and circuits. The measured load-pull parameters include the PAE, the 1 dB Compression Point (P_{1dB}), Power gain, the 3rd Order Output Intercept Point (OIP3), and the 1st and 3rd Order Intermodulation (IM1 and IM3). The operation frequency of the load-pull

system includes 28 GHz for 1-tone measurement and 30 GHz for 2-tone measurement with a 10 MHz frequency span, which is among the Ka-band range. The power sweep done by the 1-tone load-pull measurement was used to measure the HEMT power characteristics after impedance matching, which matches the maximum transducer gain at the Source Pull and maximum power at the Load Pull under a reflection coefficient of 0.8. The 2-tone load-pull measurement was impedance matched as the 1-tone load pull measurement but with two Signal Generators (SGs) to generate inter-modulated signals for the measurement of the Fundamental Power (F1) and the 3rd Order Intermodulation Power (2F1−F2), and further extrapolate the two power curves to obtain the OIP3.

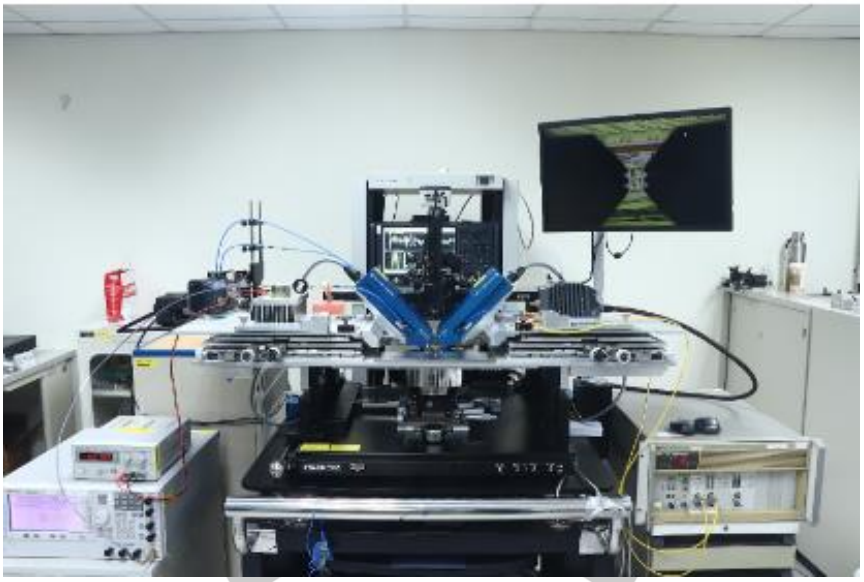


Figure 2.4-1. TSRI load-pull system for 1-tone and 2-tone measurement.

2.5 Noise Figure Measurement

The noise figure of the HEMT device was measured with the Auriga Noise Parameter Measurement System, provided by the TSRI laboratory, with the frequency ranging from 18 GHz to 41 GHz. The equipment used in the noise figure measurement includes the Agilent E8361A PNA, the Agilent N8975A Noise Figure Meter, the HP 83630B Signal Generator, the Focus Model 67260 Tuner, the Auriga AU3310 Pre-Amp, the Auriga AU3309 Down Converter, and the Auriga AU3101 PNS Controller. After the impedance-matched and on-wafer measurement, noise parameters of NF_{min}, R_n, and Γ_{opt} could be obtained for noise figure analysis.

Chapter 3

Fabrication of High Electron Mobility Transistors

3.1 Introduction of the baseline HEMT process

3.1.1 Wafer Cleaning

The epitaxial wafers are immersed in the Acetone and Isopropyl Alcohol for the removal of surface water molecules and organic particles. The cleaning of the wafer also includes the use of ultrasonic cleaning to remove particles adhesion due to van der Waals force and the capillary force.

3.1.2 Ohmic Contact Formation

The definition of an ohmic metal pad is required to fabricate all the source and drain regions for the GaN HEMTs in this study. The wafer was first spin-coated with the stepper photoresist. Afterwards, a metal stack of Ti/Al/Ni/Au of 200/1200/250/1000 Å was deposited on the wafer and the wafer was annealed with the Rapid Thermal Annealing System at around 850℃ for 30 seconds to form the ohmic contact. The ohmic contact was fabricated successfully due to a formation of TiN_X layers at the metal to semiconductor interface after the rapid thermal annealing, creating N-vacancies and lowering the Schottky barrier height. The Al metal layer acts an alloy layer mainly used to form Al-Au alloys, the Ni metal in the metal stack acts as a barrier layer to prevent Au interdiffusion, and the Au metal stack is used to lower contact resistance and prevent oxidation.

3.1.3 Ion-Implanted Isolation

The ion-implantation process is used to isolate the source and drain region of the HEMT device. The device was first spin-coated with a photoresist and then implanted with Boron ions with an ionized energy of 190 keV.

3.1.4 SiN_X Passivation

The SiN_X passivation process is to protect the fabricated device from moisture, oxidation, and contamination. The deposition of the SiN_X passivation layer is done with the Plasma Enhanced Chemical Vapor Deposition (PECVD) to deposit a thin film passivation of 100 nm. After the passivation process, via holes are opened for further thick metallization at the contact pads.

3.2 Two-Step Photolithography HEMT Process

3.2.1 Γ-Gate Definition

The two-step photolithography HEMT process using the Stepper photolithography is used in all the devices discussed in this thesis. The two-step photolithography HEMT process technology with its uniformity have been published in the IEEE Journal of Electron Device Society, vol. 11, pp. 311-318, 2023, as an article “Over 10W/mm High Power Density AlGaN/GaN HEMTs With Small Gate Length by the Stepper Lithography for Ka-Band Applications”. The Γ-Gate is fabricated on a four-inch wafer using a stepper for the first and second lithography step. After the first lithography step, the gate region of the HEMT device is left with an opening for dry etching. The dry etching process removes the exposed SiN_X layer,

followed by a second lithography step, which then creates an overlap with the first lithography step using a shifted lithography mask. The opening and the overlap created by the second lithography is then used to define the Γ-Gate after a deposition of the gate metal (Ni/Au).

3.3 Trench-Etched Gate HEMT Process

3.3.1 Trench-Etched Gate Etching

The trench-etched gate etching process is used in the fabrication of the four designed Fin-HEMT devices, which was published in the Micromachines 2023, 14(5), 931, as an article "Improvement of AlGaN/GaN HEMTs Linearity Using Etched-Fin Gate Structure for Ka Band Applications" for linearity improvement. The four devices were fabricated with fin-shaped gates, which were etched with the ICP-RIE system with Cl_2 gases. The four designed trench-etched gate devices each have an etched trench number of 0, 1, 4, and 9. Therefore, devices with 1 fin, 2 fins, 5 fins, and 10 fins were fabricated accordingly. The adoption of fin-shaped gate contributes to the increase of gate controllability and device linearity for high-power applications at Ka Band.

3.4 Ohmic Etching Patterned (OEP) HEMT Process

3.4.1 Ohmic Patterning

The Patterned Ohmic Recessing process is used in the experiment of fabricating patterned ohmic recessing GaN HEMTs, which was published in the Micromachines 2024, 15(1), 81, as an article "Improvement of AlGaN/GaN High-Electron-Mobility Transistor Radio Frequency

Performance Using Ohmic Etching Patterns for Ka-Band Applications" for the improvement of ohmic contact resistance. In order to define the patterns for the etching of the ohmic region, the wafer is spin-coated with the stepper photoresist and exposed by the stepper to define the alignment marks. The patterns are further defined by the stepper with four different ohmic etching patterns, which are patterns of 1 μm holes, 3 μm holes, 1 μm lines, and 3 μm lines. The patterns are then dry-etched with the Inductively Coupled Plasma – Reactive Ion Etching (ICP-RIE) system to half the thickness of the AlGaN barrier layer, with 10 nm barrier thickness remaining, to increase the contact area between the metal and the AlGaN layer while leaving enough AlGaN layer to create a higher electron density in the 2DEG channel.

3.5 Thick Metallization Process

3.5.1 Thick Metal Interconnect Deposition

The thick metal interconnect deposition process is done with the use of the lithography process and the Physical Vapor Deposition (PVD) system. The wafer is first spin-coated with the AZ5214E photoresist and exposed with the I-line lithography system. After defining the thick metallization deposotion area on the wafer, a 2 um thick metal stack of Ti/Au/Ti is deposited and a lift-off process is done to form the thick metal interconnect.

3.5.2 Thick Copper-Metallized Interconnect

A thick copper metallization process has been developed for the purpose of reducing fabrication costs and increasing compatibility with the Complementary Metal–Oxide–Semiconductor (CMOS) process line. The

thick copper metallization process of a GaN HEMT device has been developed and published in Phys. Status Solidi A, 220: 2200536, as an research article “Study of AlGaN/GaN High-Electron-Mobility Transistors on Si Substrate with Thick Copper-Metallized Interconnects for Ka-Band Applications”.

Chapter 4

Over 10W/mm High Power Density AlGaN/GaN HEMTs With Small Gate Length by the Stepper Lithography for Ka-Band Applications

4.1 Introduction

With the bandwidth used for consumer electronics becomes highly congested, it is crucial to develop GaN HEMT devices that could operate at higher frequency band with high a power density. In order to fabricate GaN HEMT devices with higher G_m and power gain, smaller gate length is required. Traditionally, small gate length has been fabricated using the electon-beam lithography system, however, it is time consuming and leads to high production costs. The use of the stepper photolithography system with a 2-step exposure process has been introduced in this study to reduce production costs and increase wafer uniformity, while being able to define small gate lengths for GaN HEMT devices. A high-power density of over 10 W/mm has also been measured for the GaN HEMT devices in this study, showing the potential of stepper lithography for device fabrication at Ka band. Uniformity analysis has also been made for the fabricated 4 inch wafer, demonstrating the potential for mass production.

4.2 Results and Discussion

AlGaN/GaN HEMT devices were fabricated using the stepper lithography system with a 2-step photolithography process, as shown in Figure 4-1. After the ohmic formation process, the wafer was deposited with thin film SiN_X and ready for the 1st gate photolithography step, after the first

developing process, the wafer is etched with ICP-RIE to remove the exposed SiN_X. Afterwards, the wafer is then spin-coated with a second photoresist for the 2nd gate photolithography step, and the developing of the second photoresist is followed by the deposition of the gate metal stack through physical vapor deposition. The small gate length GaN HEMT device with a gate length of 100 nm is successfully fabricated as shown in Figure 4-2, with DC curves shown in Figure 4-3 (a). Drain Induced Barrier Lowering (DIBL) curves and pulsed IV curves were both measured to investigate the small gate length devices, as shown in Figure 4-3 (b) and (c). Small-signal and large-signal characteristics were also measured for the small gate length devices for high power applications. The f_T and f_{max} of 63 GHz and 171 GHz, respectively, were measured for the 2×50 μm devices, as shown in Figure 4-8. The f_T and f_{max} of 43 GHz and 200 GHz for the 8×50 μm AlGaN/GaN HEMT with the 2-Step Photolithography Process are also shown in Figure 4-11. High power density of more than 10 W/mm were also measured for the fabricated 2×25 μm devices, as shown in Figure 4-6. Output power performances of 1.85 W and 2.25 W for the devices with larger gate widths of 8×50 μm and 8×75 μm, respectively, were also measured and shown in Figure 4-7. The wafer uniformity of the fabricated wafer was also measured with respect to I_{DSS}, G_m, and threshold voltage (V_{th}), as shown in Figure 4-5. The uniformity results demonstrated high wafer uniformity of the fabricated wafer suitable for mass production. Breakdown and TLM characteristics were measured and shown in Figure 4-4 and 4-10. Benchmark results of the power performance of the small gate length devices are also measured and

shown in Figure 4-9. The results were published in the IEEE Journal of Electron Device Society (JEDS) in May, 2023.

4.3 Conclusion

The 2-step photolithography process shown in this study demonstrates the potential for stepper lithography systems to replace traditional E-beam systems for cost reduction and increased wafer uniformity. High output power results were also measured with the devices fabricated in this study, showing the capability of the stepper to scale the device gate lengths for high frequency power applications with high wafer uniformity.

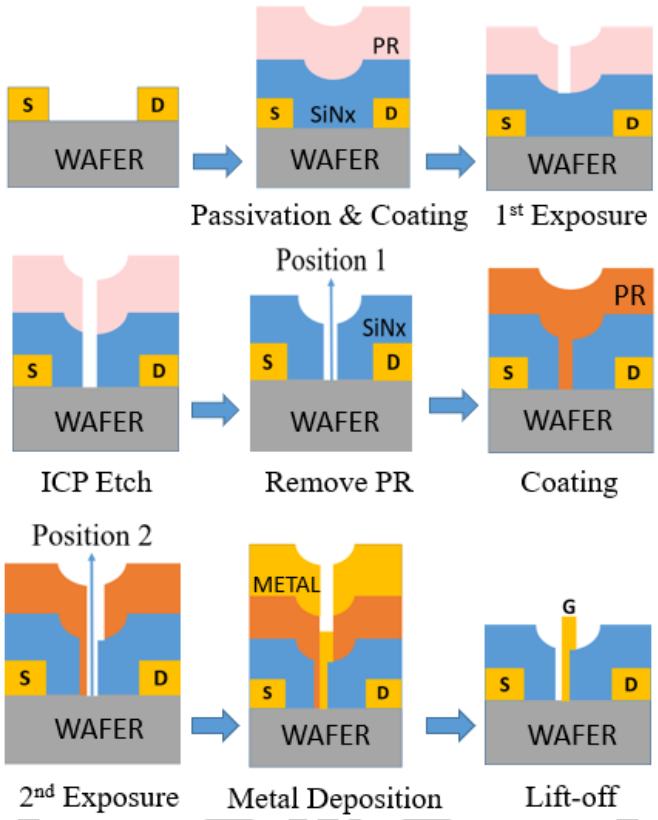


Figure 4-1. The process schematic diagram showing the 2-step photolithography technique.

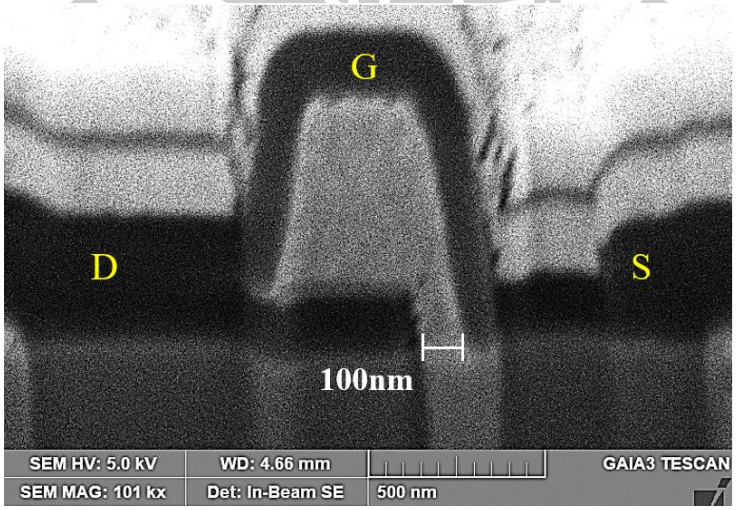


Figure 4-2. The gate cross section taken from the SEM showing the 100 nm gate length.

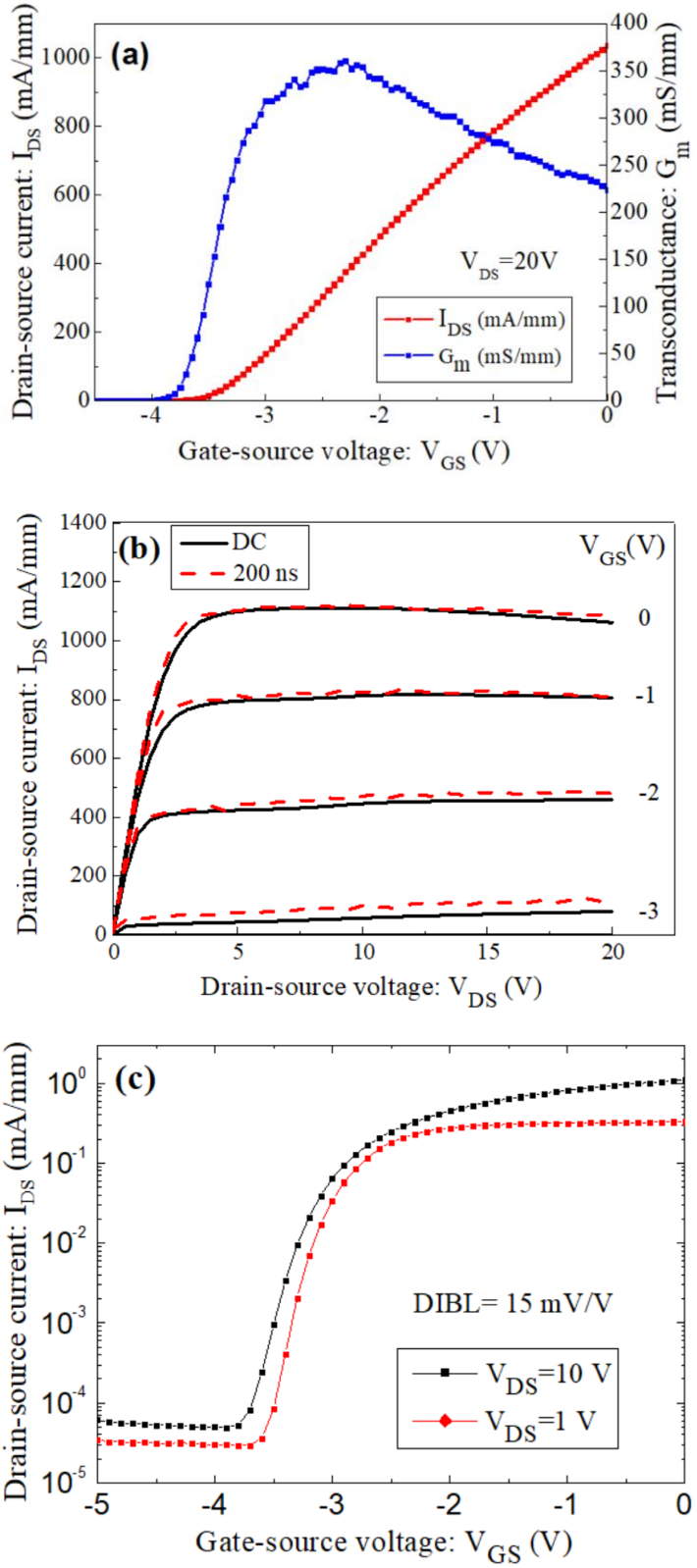


Figure 4-3. The measured (a) I_{DS}-V_{GS} curves (b) I_{DS}-V_{DS} with pulsed I_{DS}-V_{DS} curves, and the (c) transfer characteristics showing DIBL.

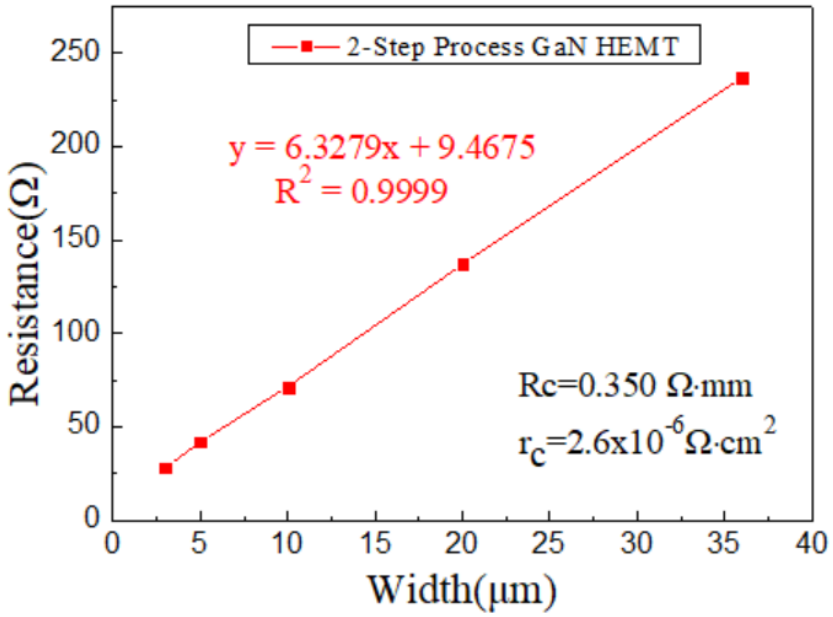


Figure 4-4. The contact resistance results that were measured for the fabricated TLM devices using the 2-step photolithography process.

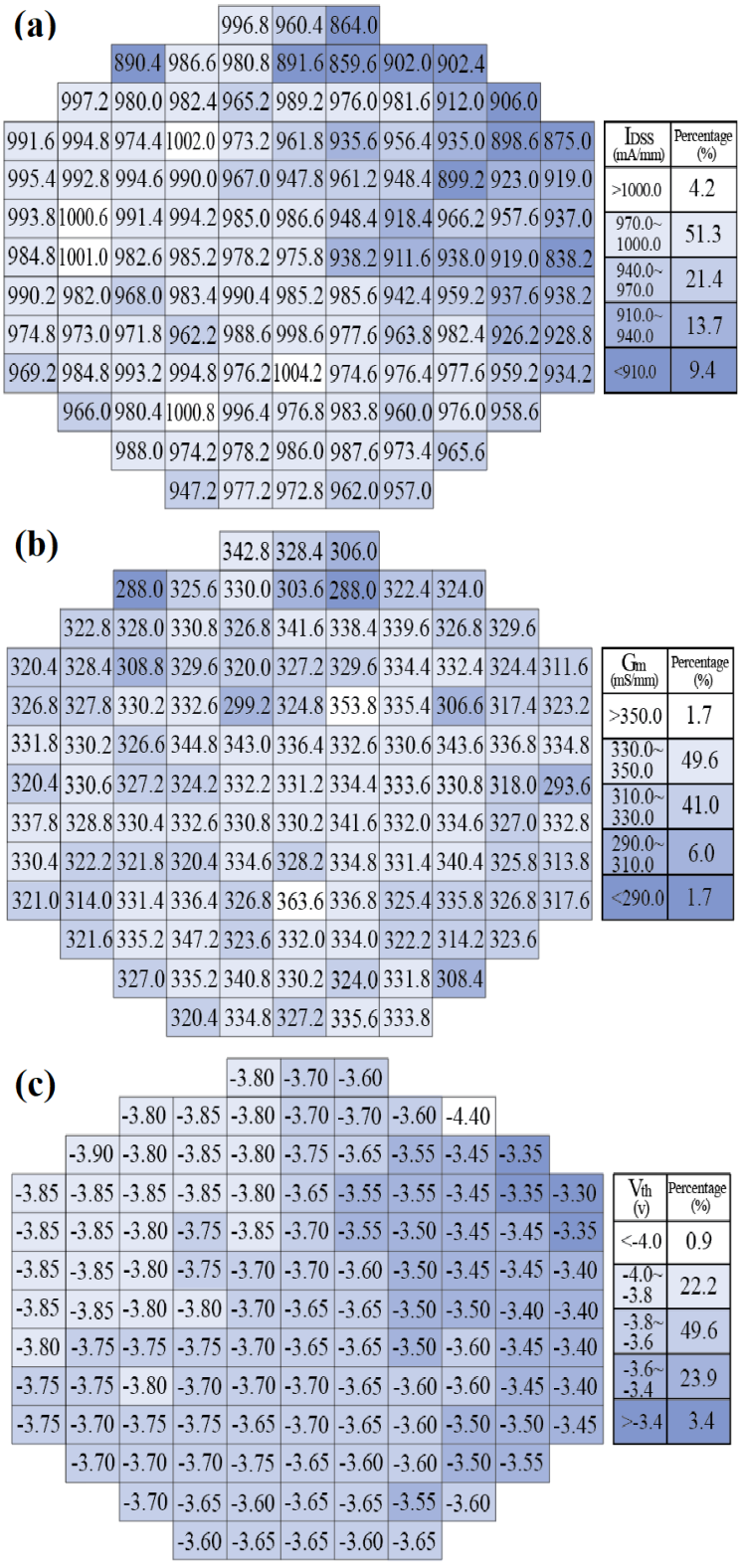


Figure 4-5. The measured uniformity regarding the (a) I_{DSS} value, (b) G_m value and (c) V_{th} value of the fabricated devices on a 4-inch wafer.

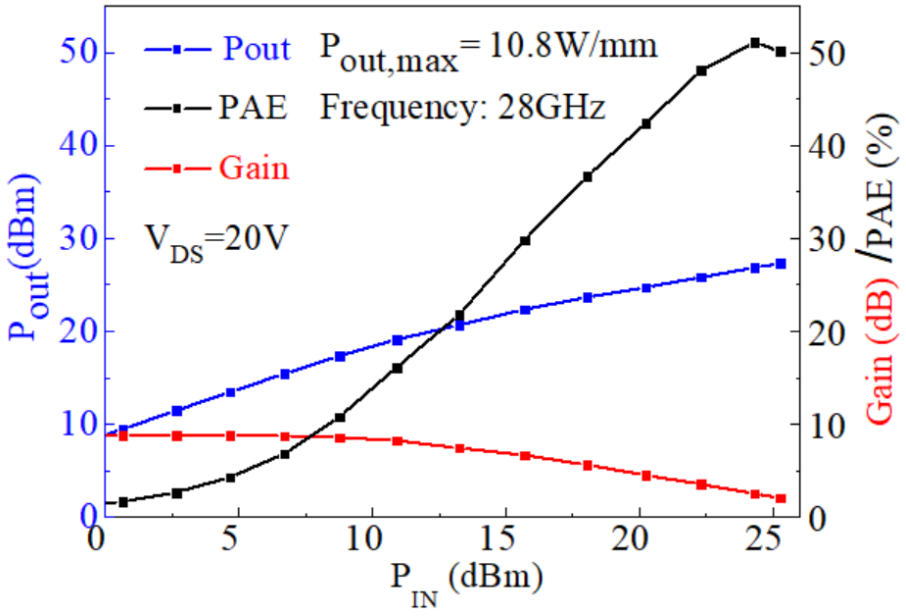


Figure 4-6. The measured load-pull power results of the 2×25 μm device using the 2-step process.

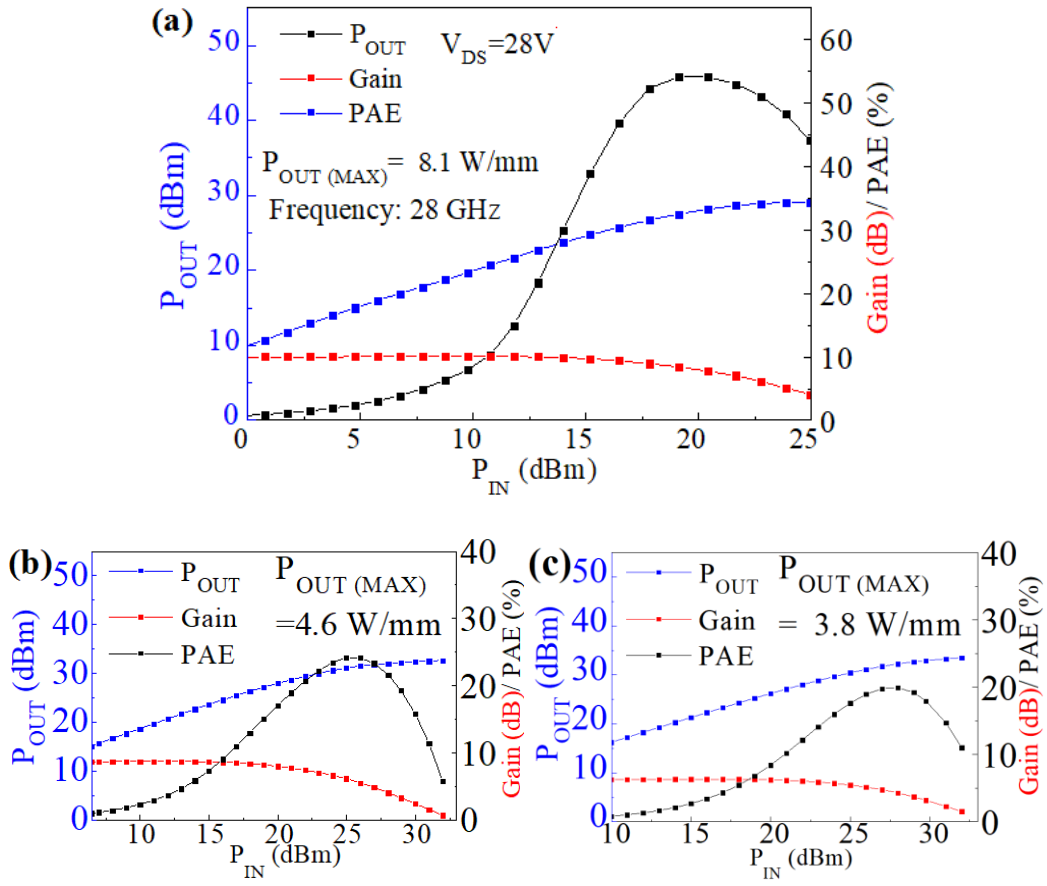


Figure 4-7. The load-pull power results of the (a) 2×50 μm, (b) 8×50 μm, (c) 8×75 μm fabricated devices using the 2-step process.

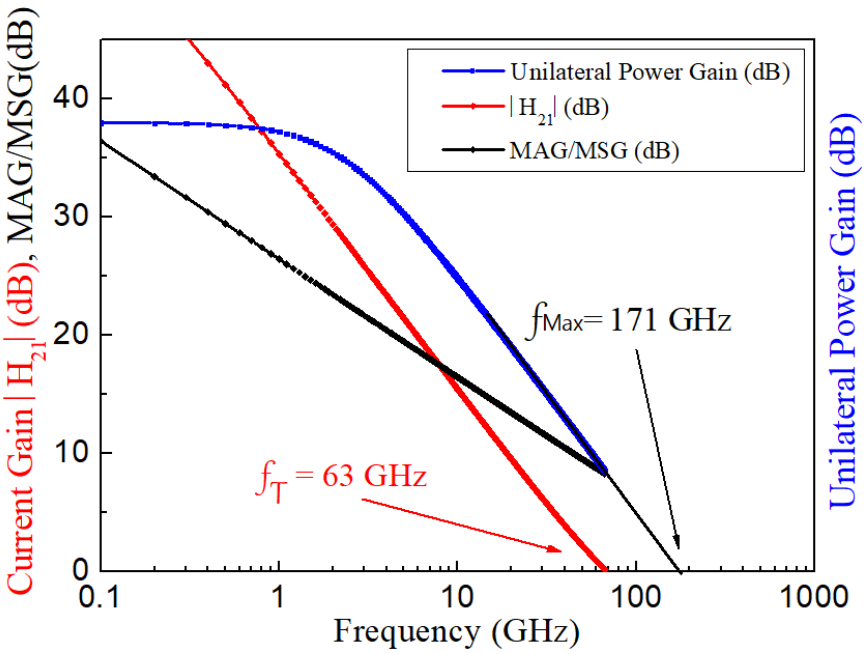


Figure 4-8. The measured $|H_{21}|$, U, and MAG/MSG versus Frequency graph for the 2×50 μm fabricated device using the 2-step process.

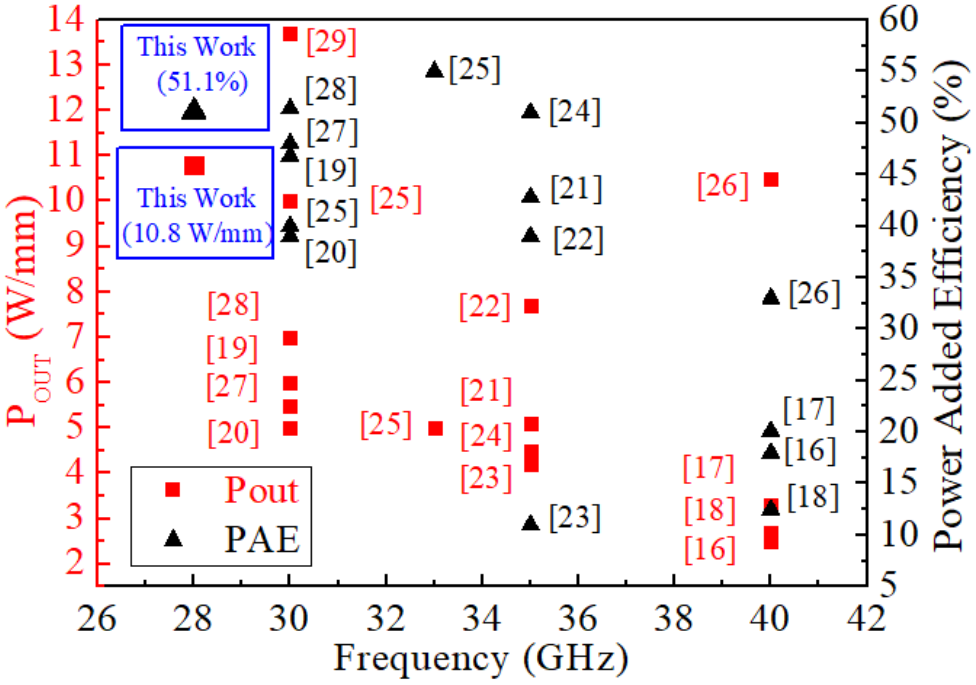


Figure 4-9. The comparison benchmark of the 2×25 μm device using the 2-step process.

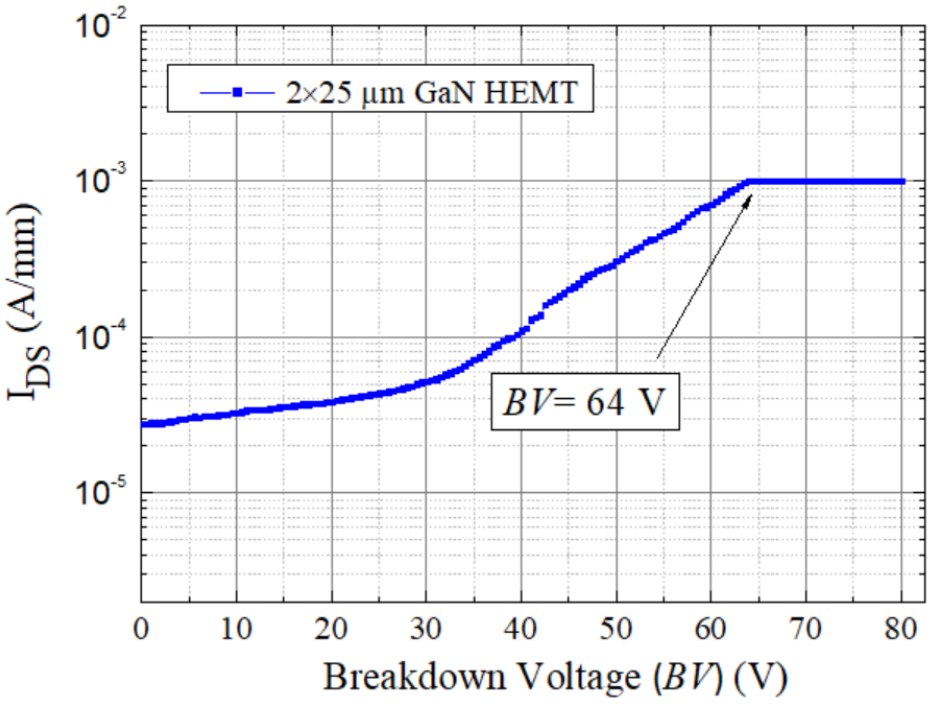


Figure 4-10. The measured breakdown results of the 2×25 μm device.

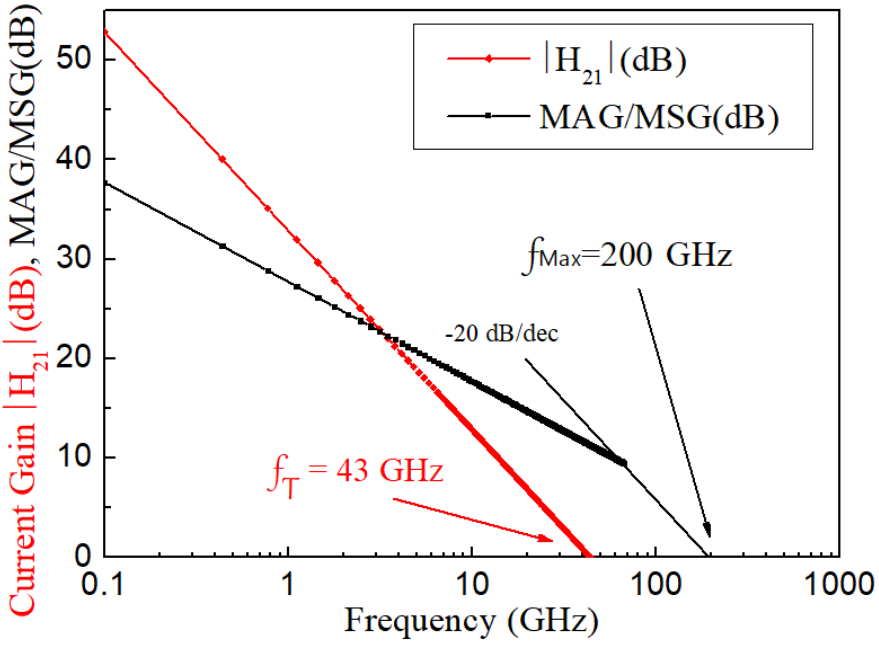


Figure 4-11. The measured $|H_{21}|$ and MAG/MSG versus Frequency results for the fabricated 8×50 μm device using the 2-step process.

Chapter 5

Improvement of AlGaN/GaN HEMTs Linearity Using Etched-Fin Gate Structure for Ka Band Applications

5.1 Introduction

The increasing demand for high-quality wireless communication systems brings about the need to increase the device linearity and to lower signal distortion. This study demonstrates the improvement of AlGaN/GaN HEMTs linearity using a fin-shaped gate structure during Ka-band power applications. There are four different fin-gate structure designs in this study: the planar, the 2 fins (1 etched fin), the 5 fins (4 etched fins), and the 10 fins (9 etched fins) devices. The separation widths between the fins are all 500 nm and the depths of the separation width are also around 500 nm. The total gate width of the devices are all 4×50 μm. The main strategy is to measure and evaluate the DC and RF performance of the four devices with respect to the device linearity. The DC linearity performance was evaluated using the I_{DS}-V_{GS} curves and the G_m-V_{GS} curves. The two-tone load pull measurement was used for RF linearity measurement, providing the linearity figure of merits such as 3rd order output power intercept point (OIP3), the 3rd order intermodulation power (IMD3), and the output power at 1dB compression point (P_{1dB}). TCAD simulation results for the fin-shaped gates have also been performed in cooperation with the CITIC-UGR research lab in the University of Granada, Spain. The final results have been published in the international journal of Micromachines in 2023, demonstrating that the fin-shaped gate structure could be used in AlGaN/GaN HEMTs to increase DC and RF

device linearity performance for Ka-band applications.

5.2 Results and Discussion

The DC and RF characteristics of the four designed devices were measured and evaluated, with the structure and design of the devices shown in Figure 5-1 (a) and (b). The I_{DS}-V_{GS} and G_m-V_{GS} curves show that the 5 fins devices have the highest Gm value among the three other designed fin-gate devices, as shown in Figure 5-2. The device linearity could also be evaluated using polynomial curve fitting to compare the linearity of the I_{DS}-V_{DG} curves. The 3rd and 5th coefficients of the polynomial fitted curves decreases with increased fin numbers, showing that the device DC linearity increases with increased fin numbers, as shown in Table 5-1. The increase in DC linearity could be due to the increased gate control over the gate width after increasing the fin numbers. The RF linearity performance was evaluated with small-signal and large-signal measurements. The small signal results showed that the devices with 5 fins have the highest f_T and f_{max} values, performing over the 10 fins devices, as shown in Figure 5-3. This may be due to the lower G_m and the higher parasitic capacitances resulting from the double fin numbers of the 10 fins devices compared to the 5 fins devices. The large-signal results measured by the two-tone load pull system, as shown in Figure 5-4, at 30 GHz with a frequency span of 10 MHz demonstrates the effectiveness of increased fin numbers on the device RF linearity, as shown in Figure 5-5, 5-6, 5-7, and 5-8. The 5 fins devices exhibited the best power gain, OIP3-P1dB, and IMD3 values over the three other designed structures at the V_{GS} of 0.5 and 0.25 I_{DSS} and V_{DS} of 20 V. However, the results obtained

from the bias point of V_{GS}=0.125 I_{DSS} and V_{DS}=20 V does not follow the same trend, which may be due to the deviated operation gate biases from around the G_m peaks and the right-shifted threshold voltages for the fin-shaped gate devices. With the obtained results, the best operating gate bias of 0.5 and 0.25 I_{DSS} for the designed fin-shaped devices were found. Moreover, the bias points of V_{DS}=10/15/25 V have also been applied to the four designed HEMTs and similar trends could be found, as shown in Figure 5-9 and 5-10. The fin-shaped gate devices all show increased linearity performance compared to the planar devices with respect to the G_m values, OIP3-P1dB, and IMD3 values. As a whole, the linearity performances increase with increased fin numbers, but decrease for the 10 fins devices, as shown in Table 5-2. The physical mechanism has been investigated with the help of the Sentaurus TCAD simulation. Simulated gate cross sections show that as the fin width narrows down from 10 μm to 5 μm, the gate electrostatic potential from the fin-gate sidewalls interfere with and repel each other more severely, and thus reduces the controllability and G_m of the fin-shaped gates, as shown in Figure 5-11 and 5-12.

5.3 Conclusion

AlGaN/GaN fin-shaped gate HEMT devices have been fabricated to increase DC and RF linearity for Ka-band applications. The devices with 5 fins exhibited the best G_m, OIP3-P1dB, power gain, and IMD3 values for the main operation bias point of 0.5 I_{DSS} and 0.25 I_{DSS}. TCAD results were also simulated for the fin-shaped gate structures to demonstrate an increased interference of the fin-gate sidewall electrostatic potential for shorter fin

widths. The results shown in this study demonstrates that the adoption of the fin-shaped gate structures increases the linearity of the devices with an optimized fin number among the four designed fin-gate structures and is suitable for Ka-band applications.

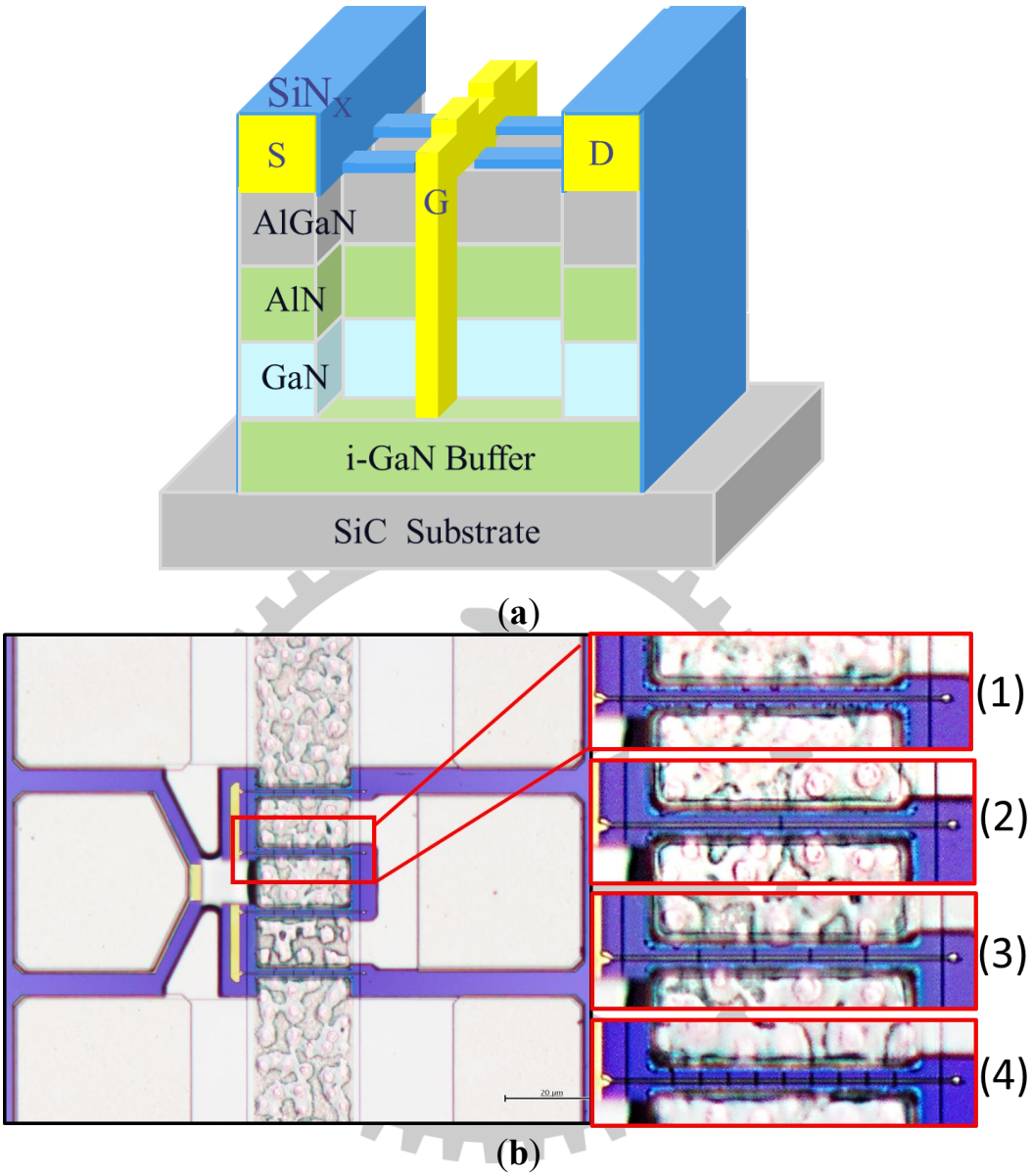


Figure 5-1. (a) The schematic diagram of the HEMT with one gate and one etched trench, and (b) the taken optical graphs of the devices with (1) planar, (2) 1 trench, (3) 4 trenches, and (4) 9 trenches, respectively.

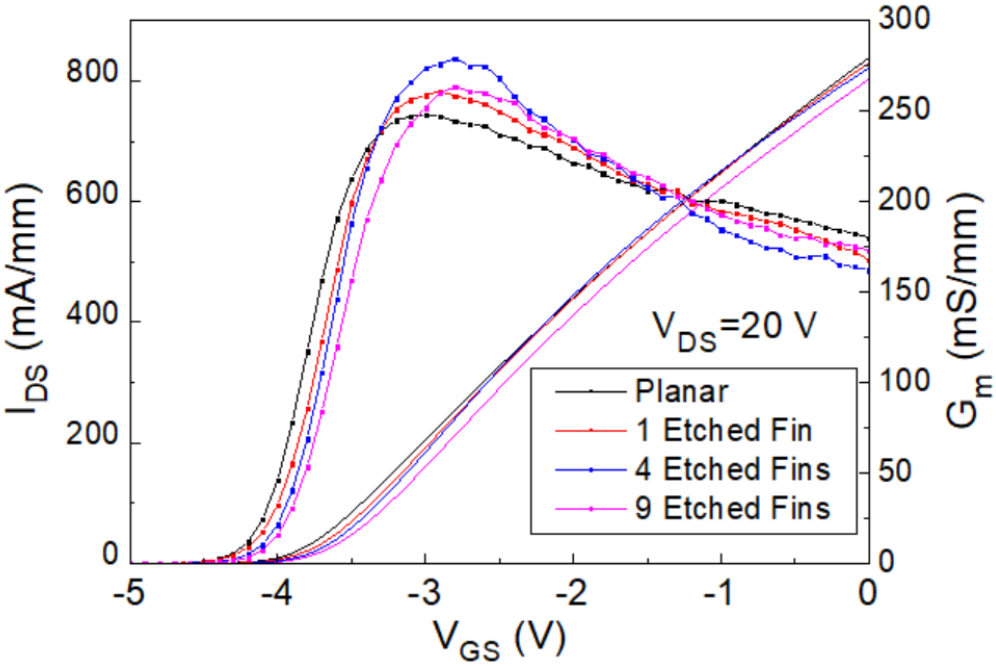


Figure 5-2. The measured I_{DS}-V_{GS} and G_m-V_{GS} curves of the devices with planar, 1 trench, 4 trenches, and 9 trenches, respectively.

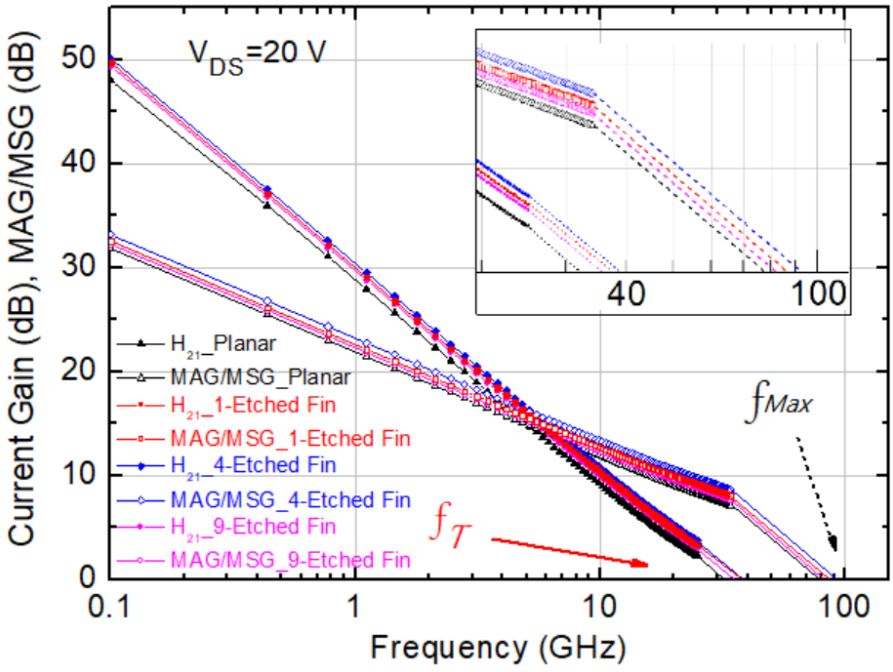


Figure 5-3. The measured current gain and MAG/MSG versus frequency graphs of the fabricated devices with the planar, 1 trench, 4 trenches, and 9 trenches, respectively.

Table 5-1. The DC results comparison of the four fabricated devices.

	Planar	**1-Etched-Fin**	**4-Etched-Fin**	**9-Etched-Fin**
I_{DSS} (I_{DS} at V_{GS} = 0 V, mA/mm)	839	830	822	803
$G_{m,\,max}$ (mS/mm)	247	261	279	264
Threshold Voltage (V)	−4.3	−4.29	−4.20	−4.05
I_{DS}-V_{GS} polynomial 1st-order coefficient (a_1)	−0.12585	0.80071	1.06891	0.36060
I_{DS}-V_{GS} polynomial 3rd-order coefficient (a_3)	−0.07354	0.19897	0.25904	0.06249
a_3/a_1	0.58435	0.24849	0.24234	0.17329
I_{DS}-V_{GS} polynomial 5th-order coefficient (a_5)	−0.00137	0.00226	0.00285	0.00023
a_5/a_1	0.01089	0.00282	0.00267	0.00064

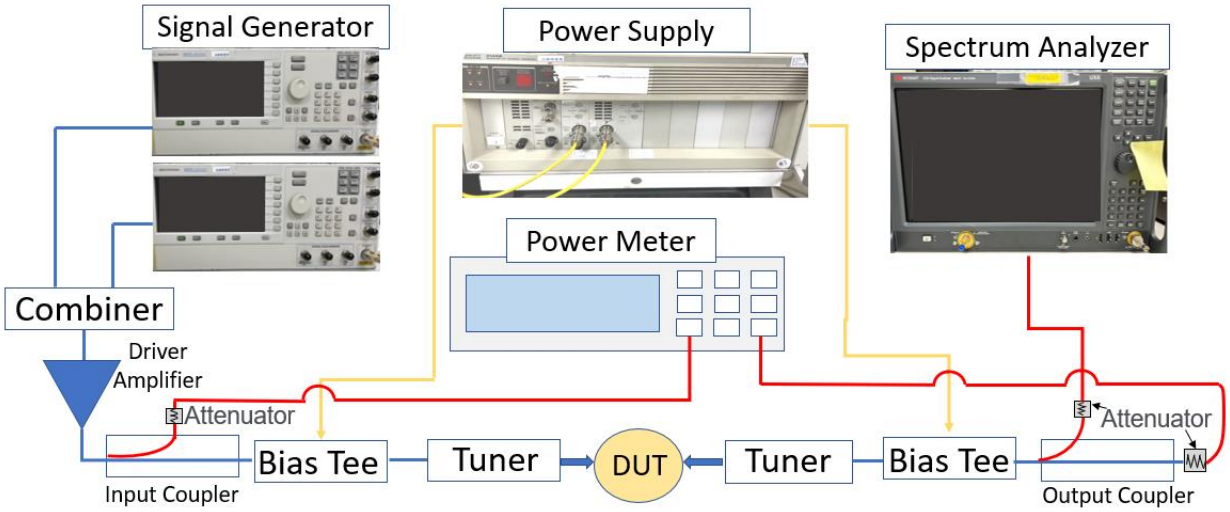
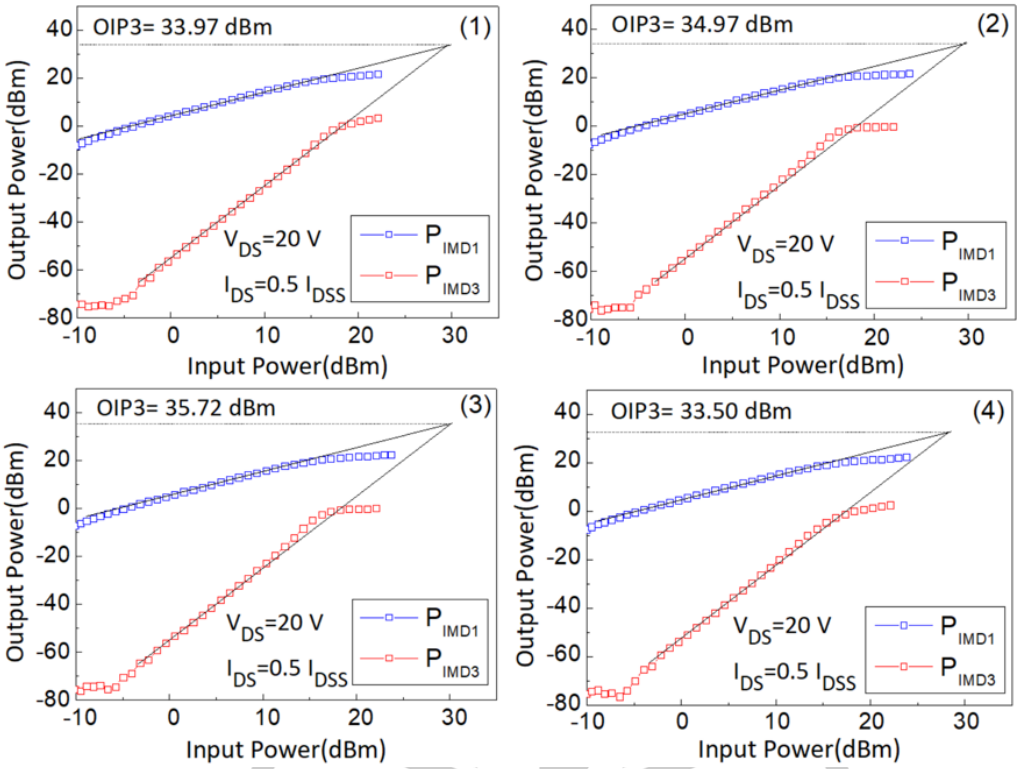
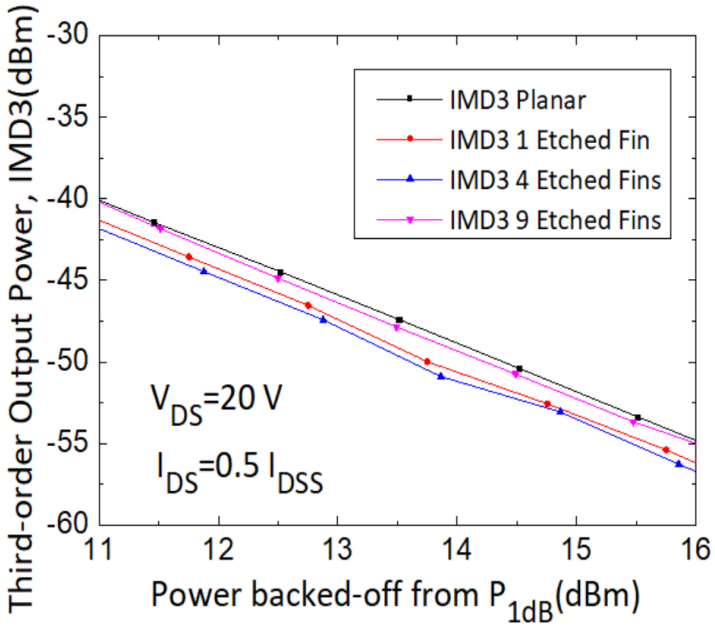


Figure 5-4. The block schematic diagram of the 2-tone large signal measurement setup.

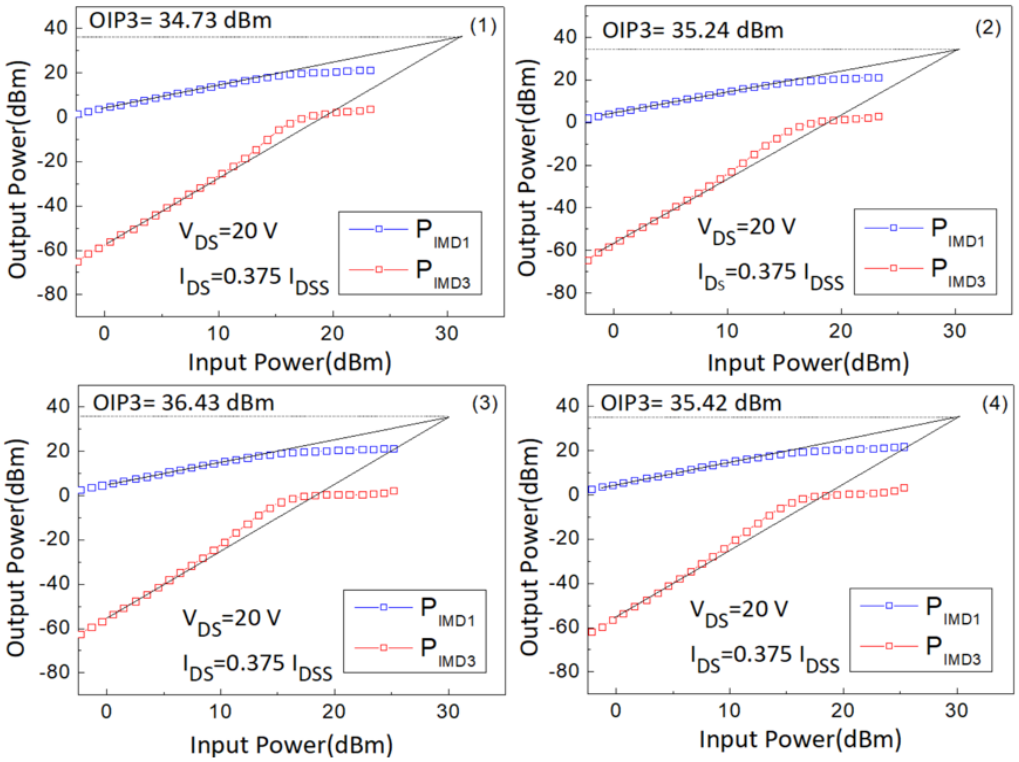


(a)

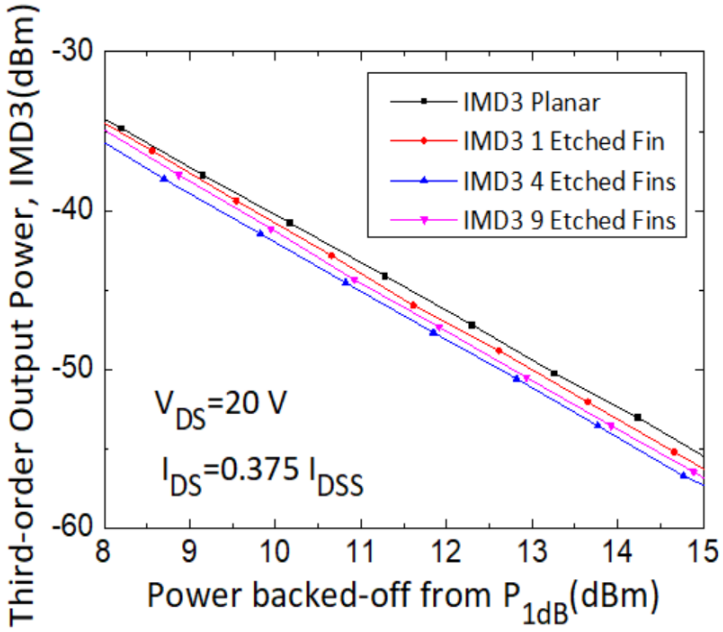


(b)

Figure 5-5. The measured (a) 2-tone load pull power results of the devices with the (1) planar, (2) 1 trench, (3) 4 trenches, and (4) 9 trenches, respectively, and (b) IMD3 – (power backed off from P_{1dB}) graph of the four fabricated devices with $I_{DS} = 0.5\ I_{DSS}$.

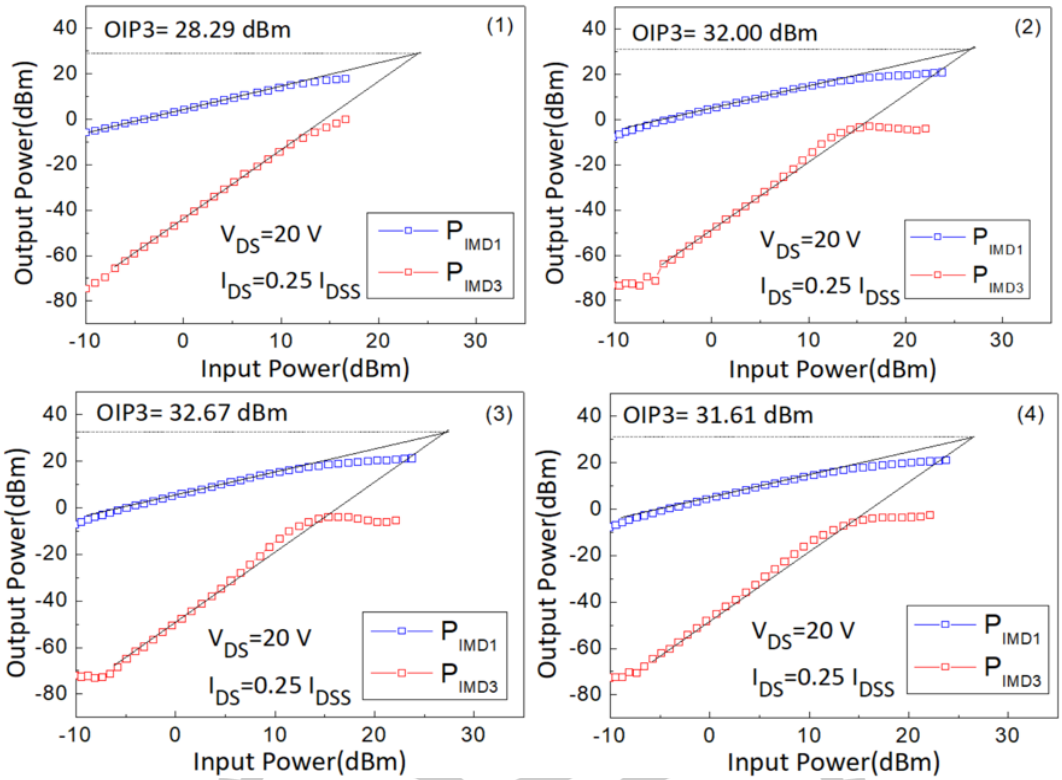


(a)

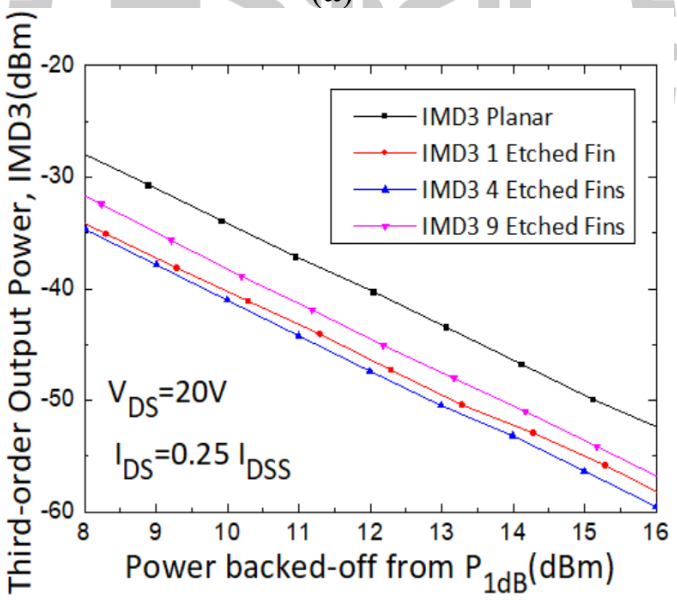


(b)

Figure 5-6. The measured (a) 2-tone load pull power results of the devices with the (1) planar, (2) 1 trench, (3) 4 trenches, and (4) 9 trenches, respectively, and (b) IMD3 – (power backed off from P_{1dB}) graph of the four fabricated devices with I_{DS} = 0.375 I_{DSS}.

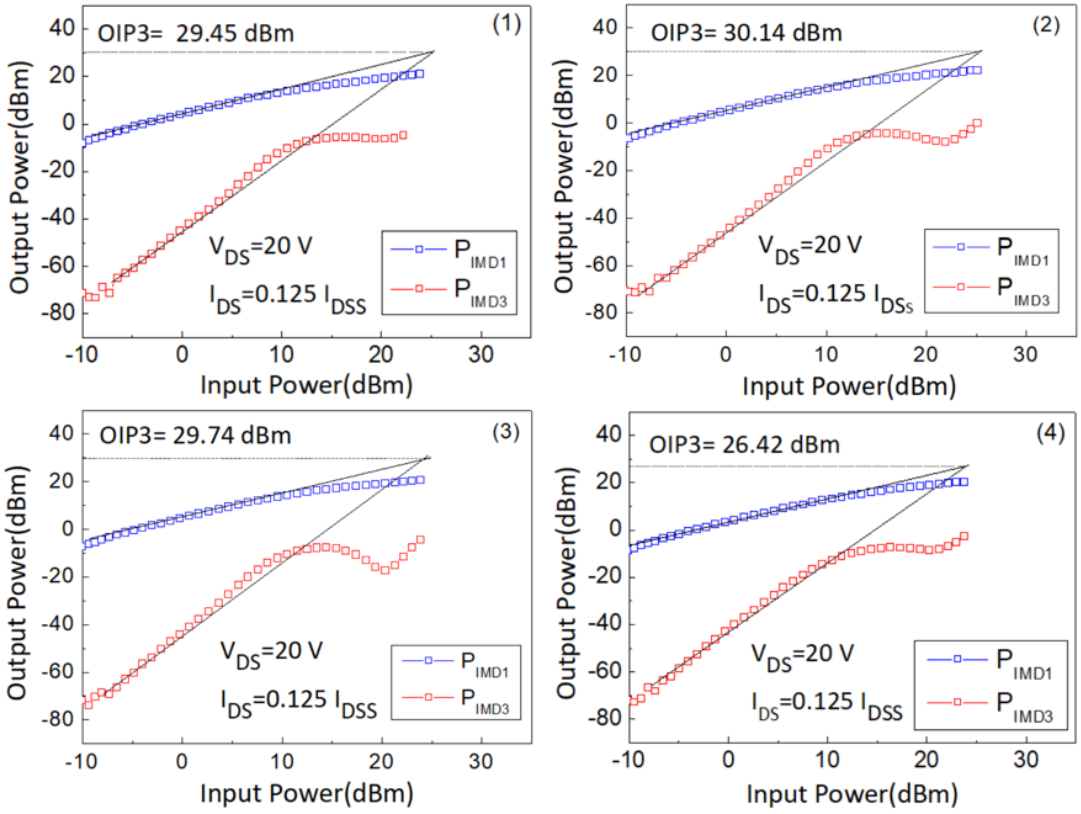


(a)

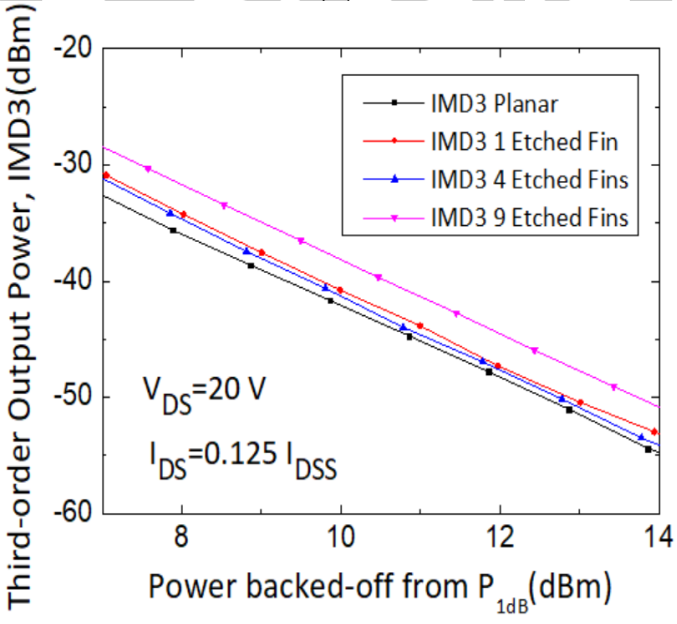


(b)

Figure 5-7. The measured (a) 2-tone load pull power results of the devices with the (1) planar, (2) 1 trench, (3) 4 trenches, and (4) 9 trenches, respectively, and (b) IMD3 – (power backed off from P_{1dB}) graph of the four fabricated devices with $I_{DS} = 0.25\ I_{DSS}$.



(a)



(b)

Figure 5-8. The measured (a) 2-tone load pull power results of the devices with the (1) planar, (2) 1 trench, (3) 4 trenches, and (4) 9 trenches, respectively, and (b) IMD3 – (power backed off from P_{1dB}) graph of the four fabricated devices with $I_{DS} = 0.125\ I_{DSS}$.

Table 5-2. The listed RF results of the four fabricated devices with different RF gate bias point.

Device Type (4 × 50 μm)	DC Bias Point: V_{DS} = 20 V, Operation Frequency: 30 GHz						
	RF Bias	I_{DS} (mA)	PIMD3 Level at 16 dB Back-Off from P_{1dB} (dBm)	OIP3 (dBm)	P_{1dB} (dBm)	Δ(OIP3-P_{1dB}) (dB)	Gain (dB)
Planar	0.5 I_{DSS}	83.90	−54.82	33.97	24.73	9.24	7.38
1 trench		83.00	−56.21	34.97	24.13	10.84	7.88
4 trenches		82.20	−56.72	35.72	24.46	11.26	8.12
9 trenches		80.30	−55.00	33.50	23.74	9.76	7.79
Planar	0.375 I_{DSS}	62.93	−55.49	34.73	24.13	10.60	7.49
1 trench		62.25	−56.27	35.24	23.72	11.52	7.84
4 trenches		61.65	−57.30	36.43	23.54	12.89	8.38
9 trenches		60.23	−56.86	35.42	23.56	11.86	8.25
Planar	0.25 I_{DSS}	41.95	−52.36	28.29	21.56	6.73	7.54
1 trench		41.50	−58.17	32.00	21.43	10.57	8.08
4 trenches		41.10	−59.54	32.67	21.45	11.22	8.28
9 trenches		40.15	−56.77	30.62	21.02	9.60	7.67
Planar	0.125 I_{DSS}	20.98	−54.73	29.45	18.36	11.09	7.39
1 trench		20.75	−53.15	30.14	19.24	10.90	7.63
4 trenches		20.55	−54.11	29.74	18.76	10.98	7.84
9 trenches		20.08	−50.83	26.42	18.46	7.96	7.00

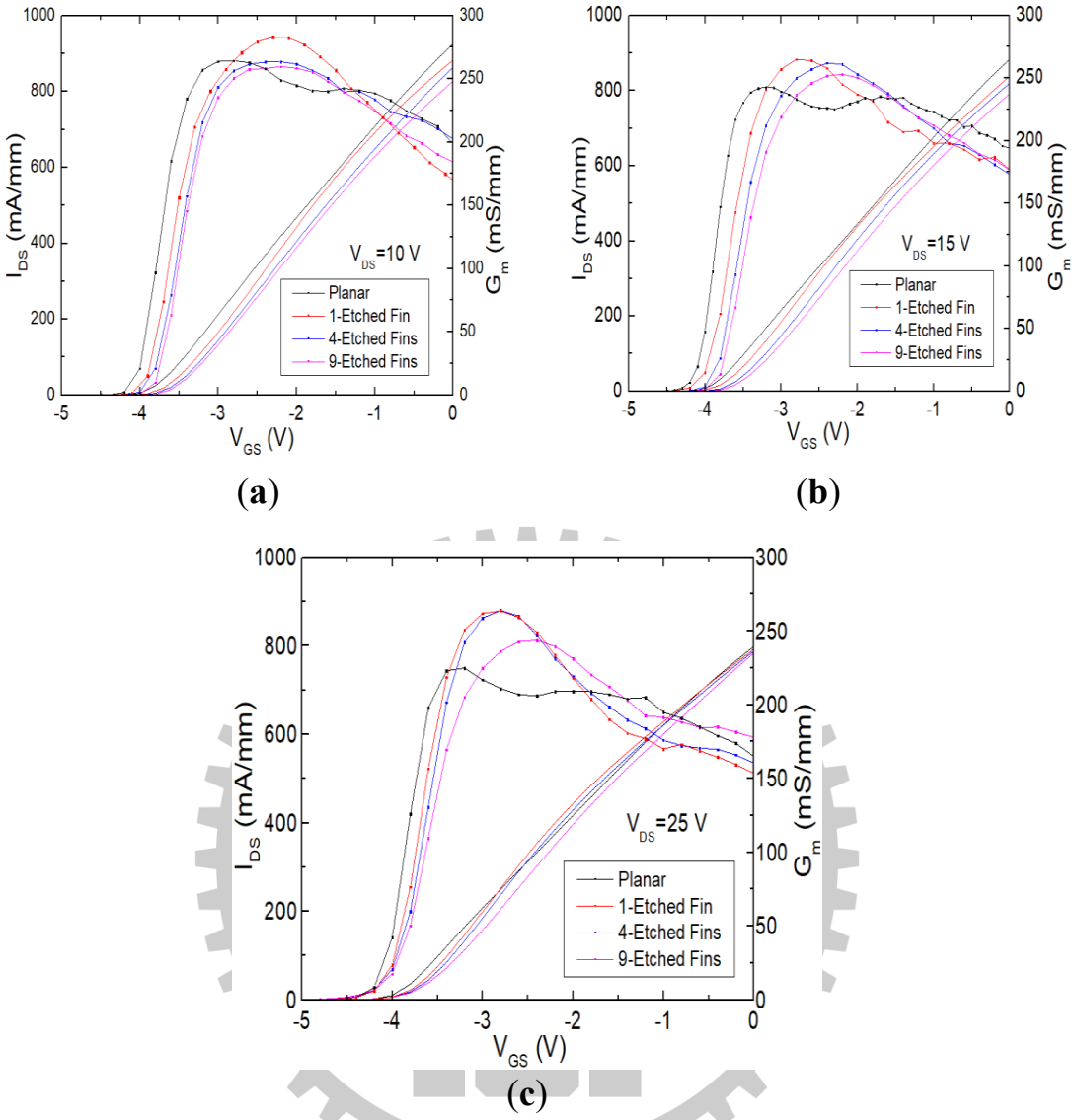


Figure 5-9. The measured I_{DS}-V_{GS} and G_m-V_{GS} graphs of the fabricated devices with the planar, 1 trench, 4 trenches, and 9 trenches, respectively, at V_{DS} of (a) 10 V, (b) 15 V, and (c) 25 V.

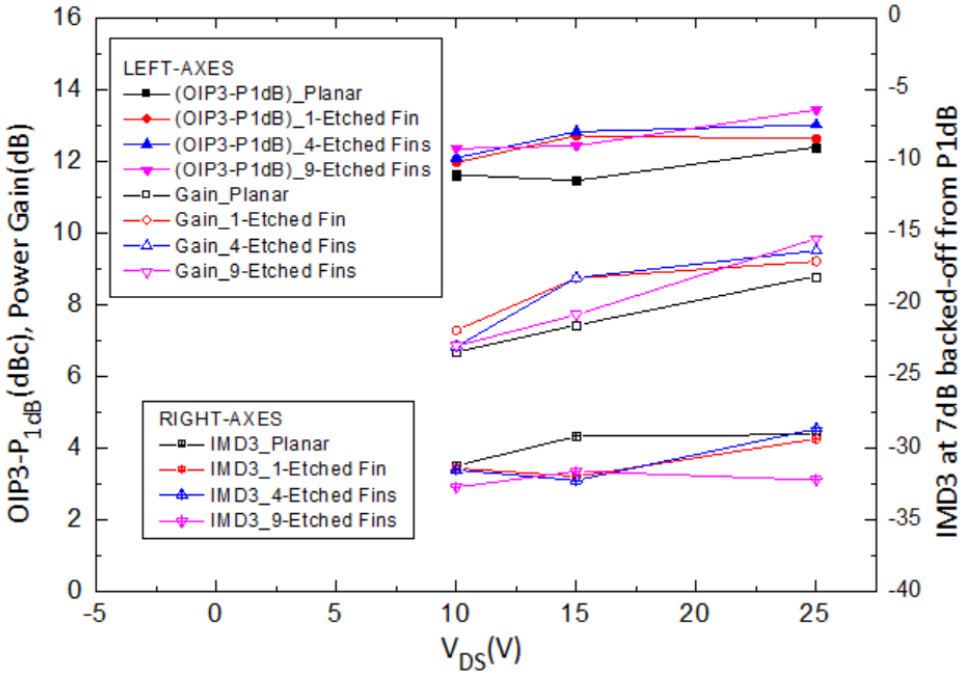
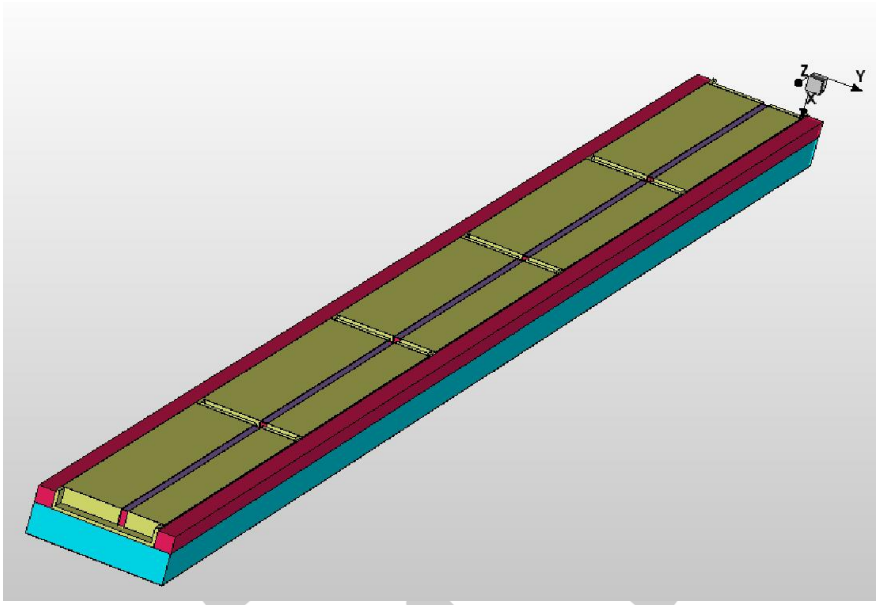
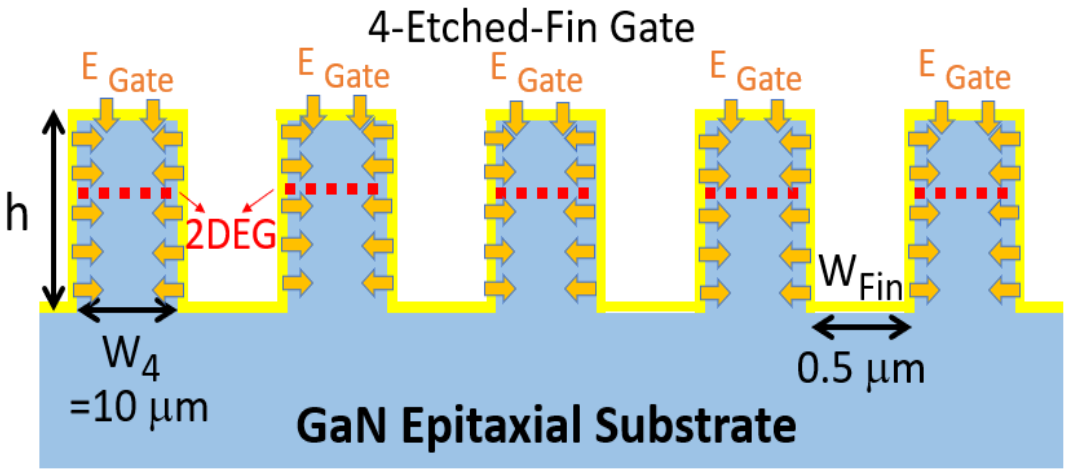


Figure 5-10. The measured Δ(OIP3-P1dB), power gain, and IMD3 at various drain biases of the fabricated devices with the planar, 1 trench, 4 trenches, and 9 trenches, respectively, at an $I_{DS} = 0.25\ I_{DSS}$ bias point.

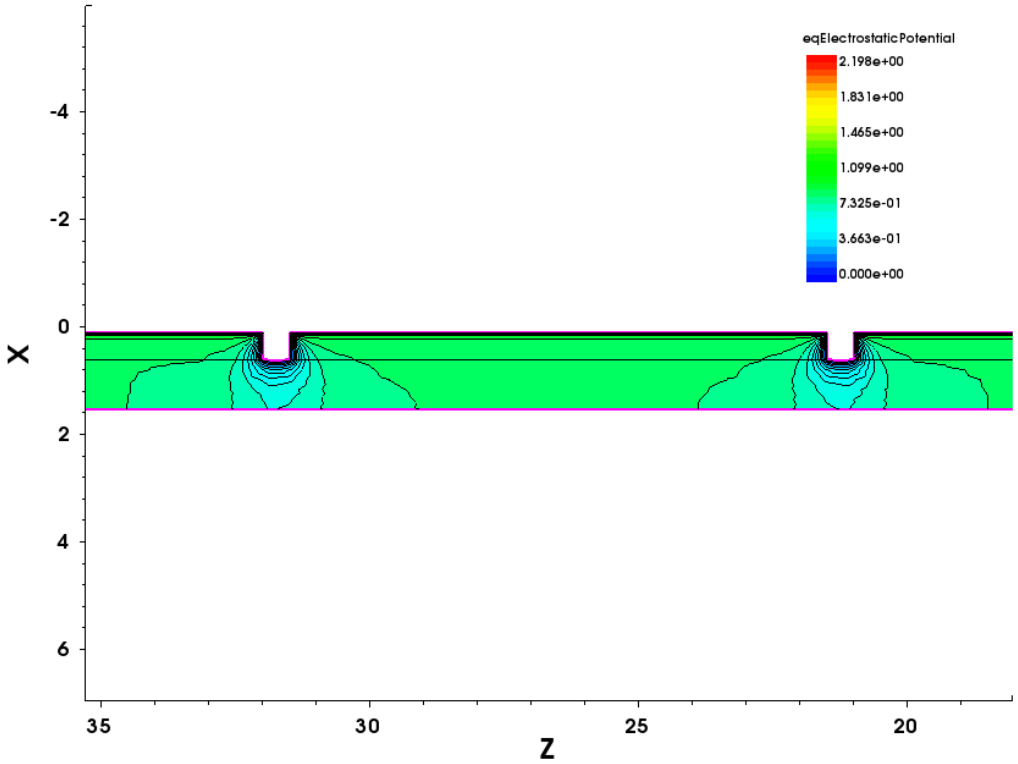


(a)

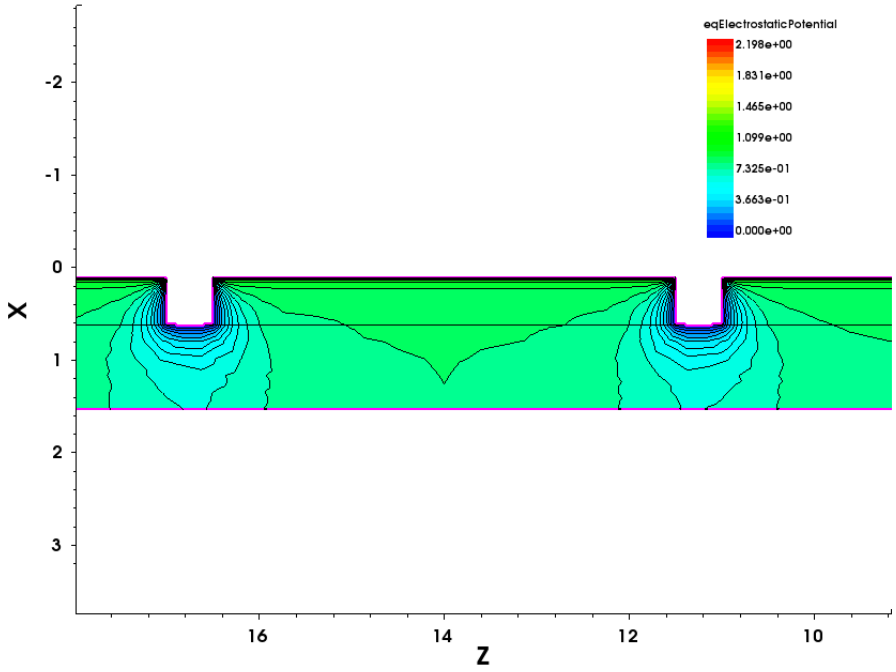


(b)

Figure 5-11. The simulated model for the (a) 4 trenched gate device with one gate and the (b) schematic diagram of the electrostatic potential effect for the simulated device.



(a)



(b)

Figure 5-12. The simulated electrostatic potential results of the device with (a) 4 trenches and (b) 9 trenches.

Chapter 6

Improvement of AlGaN/GaN High-Electron-Mobility Transistor Radio Frequency Performance Using Ohmic Etching Patterns for Ka-Band Applications

6.1 Introduction

As the need for high frequency and high-power devices begin to strive, researchers have been finding ways to improve the high frequency performance of GaN HEMTs through the improvement of high frequency figure of merits, such as f_T and f_{max}. Among the many ways to improve f_T and f_{max}, the reduction of ohmic contact stands out as one of the most popular technique. A few years ago, the use of ohmic etching patterns has been introduced and simulated by various groups to improve contact resistivity and contact resistance of ohmic contacts for GaN HEMTs. In this study, ohmic etching patterns has been applied to AlGaN/GaN HEMT devices that operate at the frequency of Ka Band, as shown in Figure 6-1. The four designs of the ohmic etching patterns in this study are 1 μm lines, 3 μm lines, 1 μm holes, and 3 μm holes, respectively, as shown in Figure 6-2 (a), (b), (c), and (d). The patterns were all etched to around 10 nm depth within the ohmic region, followed by the deposition of ohmic metal stacks and an annealing temperature of 850 °C. The devices in this study have a gate width of 2×25 μm and a gate length of 150 nm. DC and RF characteristics were measured for the designed devices, including the noise performance, small-signal performance, and large-signal performance.

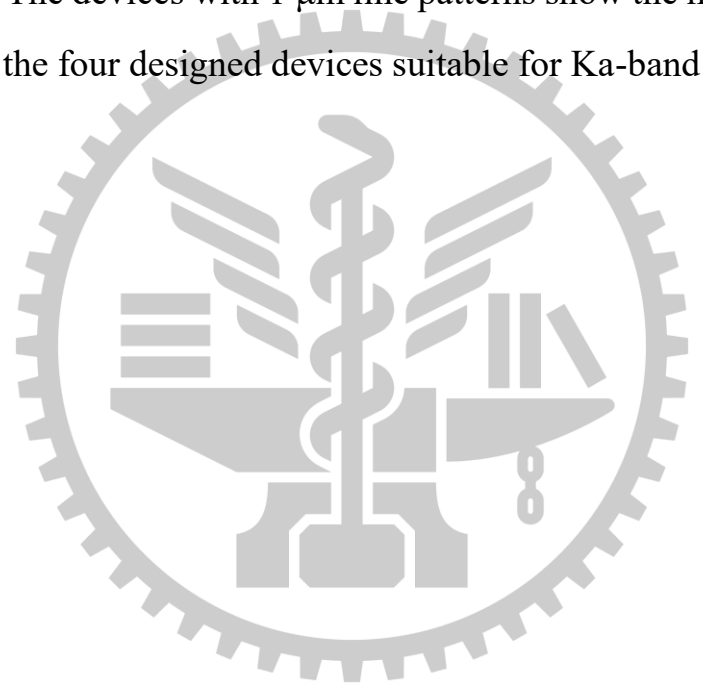
6.2 Results and Discussion

The four designed patterns all contributed to a reduction in the on-resistance, ohmic contact resistance as well as the contact resistivity compared to the devices without any ohmic etching patterns, as shown in Figure 6-4. The reduction of the ohmic contact could be attributed to the increase in contact area between the ohmic metal and the barrier layer. The devices with the pattern of 1 μm lines exhibited the lowest contact resistance of 0.154 Ω·mm and a contact resistivity of 4.04×10^{-7} among the four designed devices, as shown in Table 6-1. The benchmark of the contact resistance in this study with published results are also shown in Figure 6-5. At a V_{DS} bias of 10 V, the devices with the pattern of 1 μm lines also exhibited the highest G_m and I_{DSS} value of 403 mS/mm and 999 mA/mm, respectively, as shown in Figure 6-3 and Table 6-2. Small-signal equivalent circuit model has been shown in Figure 6-6. The small-signal performance of the devices with 1 μm line patterns exhibited the highest f_T and f_{max} of 36.4 and 158.29 GHz, respectively, as shown in Figure 6-7 (a) and (b). The compared extracted small signal parameters are also shown in Table 6-3. The large-signal performance of the devices with 1 μm line patterns also exhibited the highest output power density of 1.94W/mm at 28 GHz with a V_{DS} bias of 10 V, as shown together with other patterned device power results in Figure 6-8 (a), (b), (c), and (d). The load-pull results are listed in Table 6-4 for comparison. Furthermore, the devices with 1 μm line patterns also exhibited the lowest minimum noise figure of 1.75 dB at 28 GHz with a V_{DS} bias of 10 V, as shown together with the other noise figure results in Figure 6-9. The devices with 1 μm line patterns have the advantage of increased contact area

and a relatively lower parasitic capacitance over the other three patterned devices.

6.3 Conclusion

This study demonstrates the adoption of ohmic etching patterns into the design of GaN HEMT devices for Ka-band applications and the results were published. Four different patterns were introduced and fabricated for the GaN HEMT to reduce ohmic contact resistance and improve DC and RF performances. The devices with 1 μm line patterns show the most promising results among the four designed devices suitable for Ka-band applications.



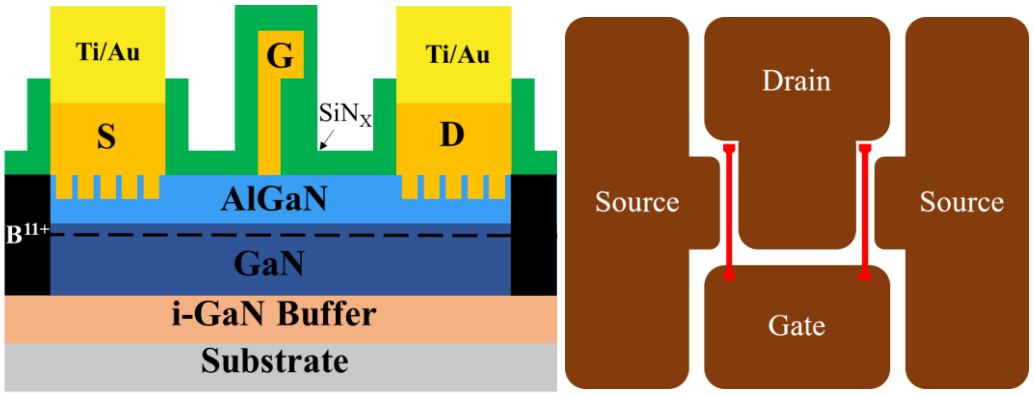


Figure 6-1. The (a) cross section schematic view of the OEP device and the (b) device top view.

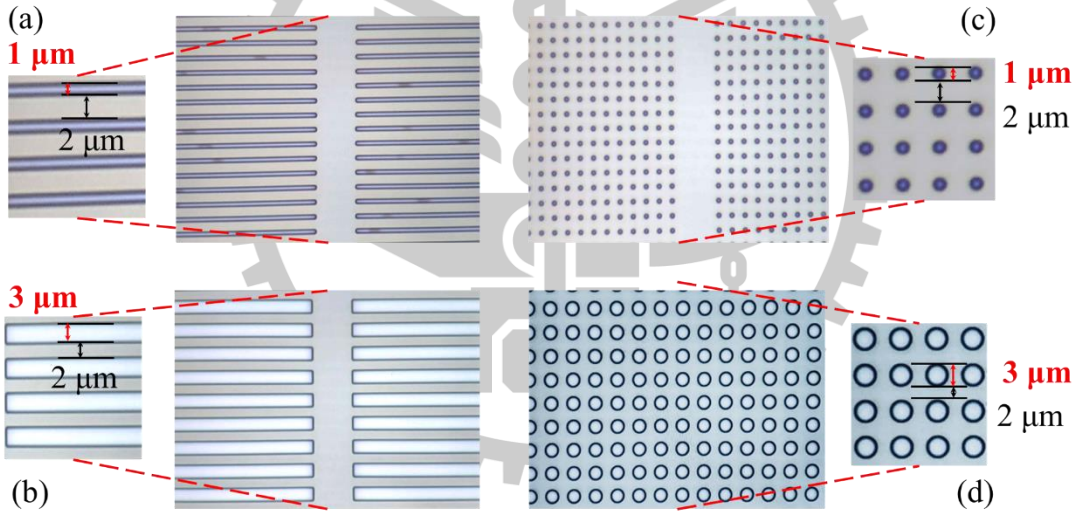


Figure 6-2. The taken optical micrographs of the OEP patterns with (a) 1 μm lines, (b) 3 μm lines, (c) 1 μm holes, and (d) 3 μm holes.

Table 6-1. The measured TLM results of the four fabricated OEP devices.

Ohmic Etching Patterns	ϱ_c (Ω·cm²)	R_c (Ω·mm)
1 μm line	4.04×10^{-7}	0.154
3 μm line	7.80×10^{-7}	0.212
1 μm hole	6.01×10^{-7}	0.191
3 μm hole	7.68×10^{-7}	0.199
w/o OEPs	2.73×10^{-6}	0.429

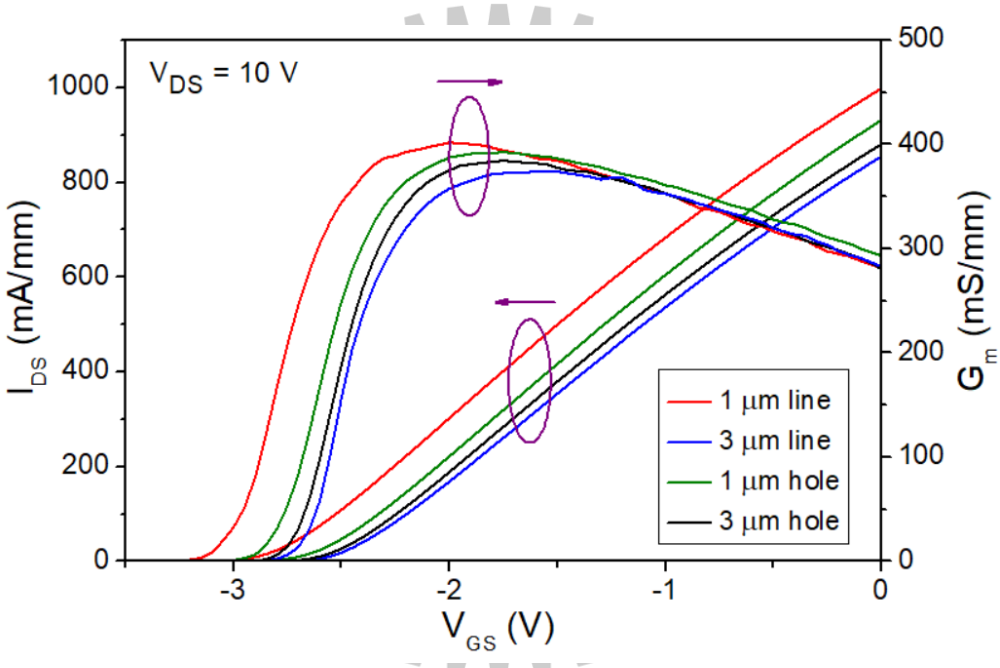


Figure 6-3. The transfer characteristics for the four 2 × 25 μm OEP HEMTs.

Table 6-2. The measured R_{on}, $G_{m,\,peak}$, I_{DSS}, NF_{min}, gain at 28 GHz of the four fabricated OEP devices.

Ohmic Etching Patterns	R_{on} (Ω·mm)	$G_{m,\,peak}$ (mS/mm)	I_{DSS} (mA/mm)	NF_{min} at 28 GHz (dB)	Gain at 28 GHz (dB)
1 μm line	1.61	403	999	1.75	5.98
3 μm line	2.24	374	855	2.00	6.14
1 μm hole	1.63	393	932	1.85	5.80
3 μm hole	1.81	385	880	1.87	6.09

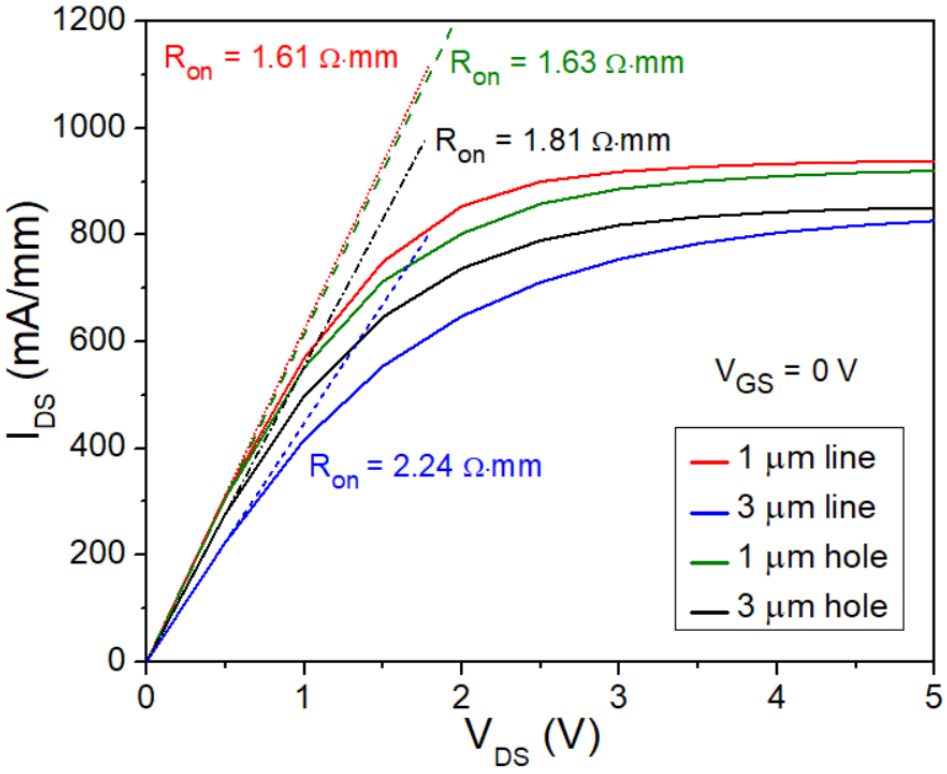


Figure 6-4. The I_{DS}–V_{DS} results for the four 2 × 25 μm OEP HEMTs and the corresponding R_{on}.

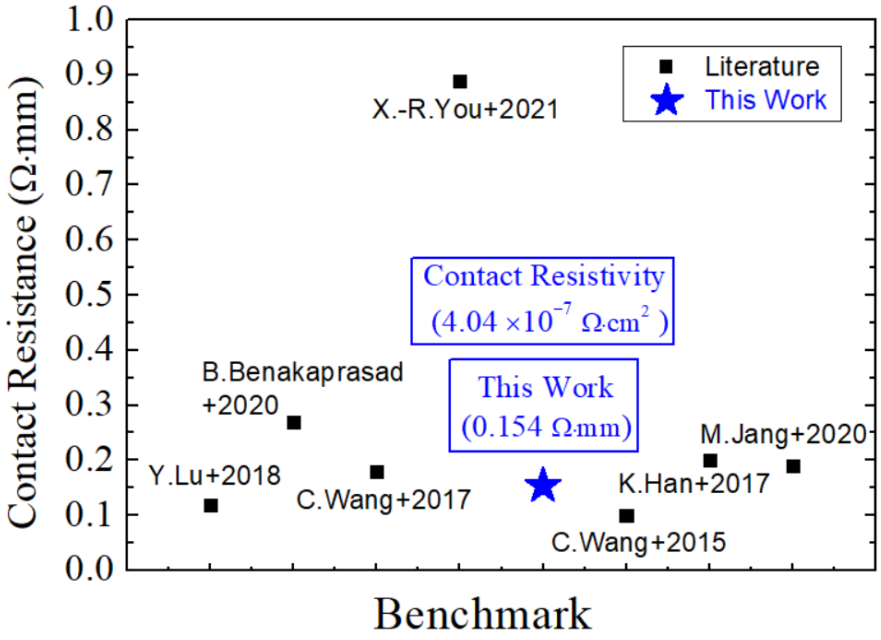


Figure 6-5. The comparison of contact resistance between the best result in this study and publications.

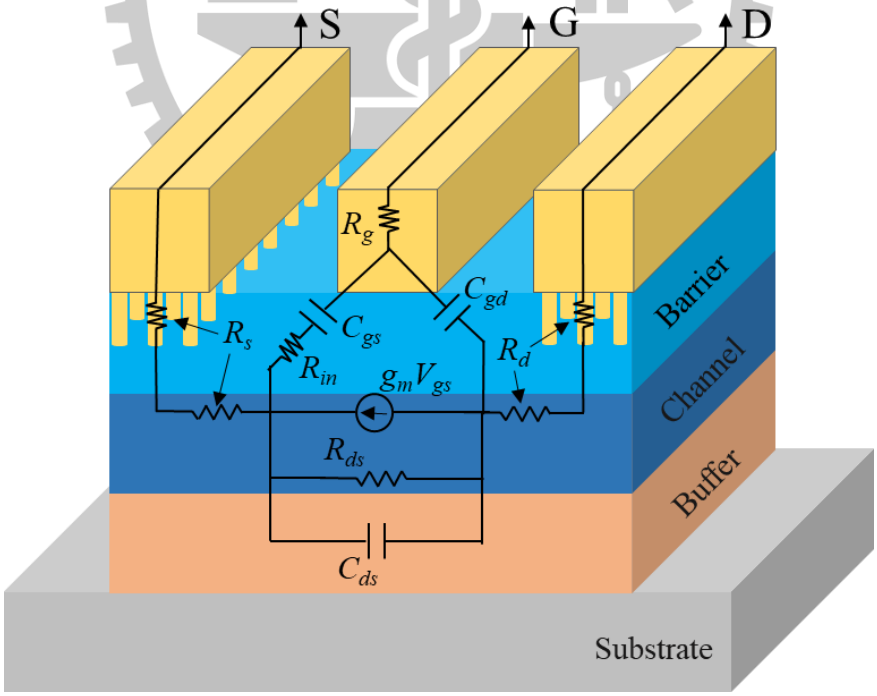
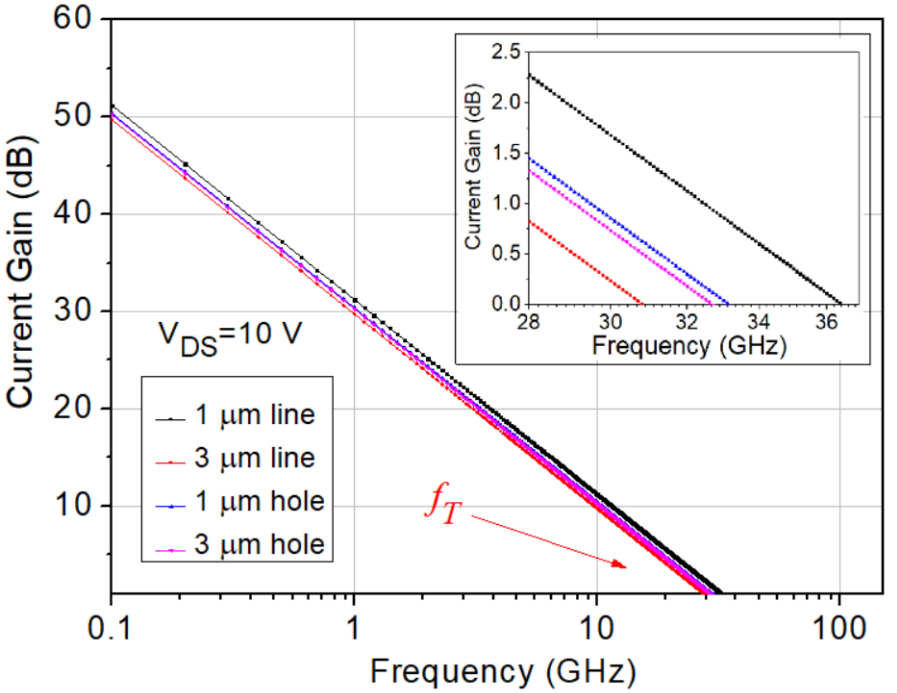
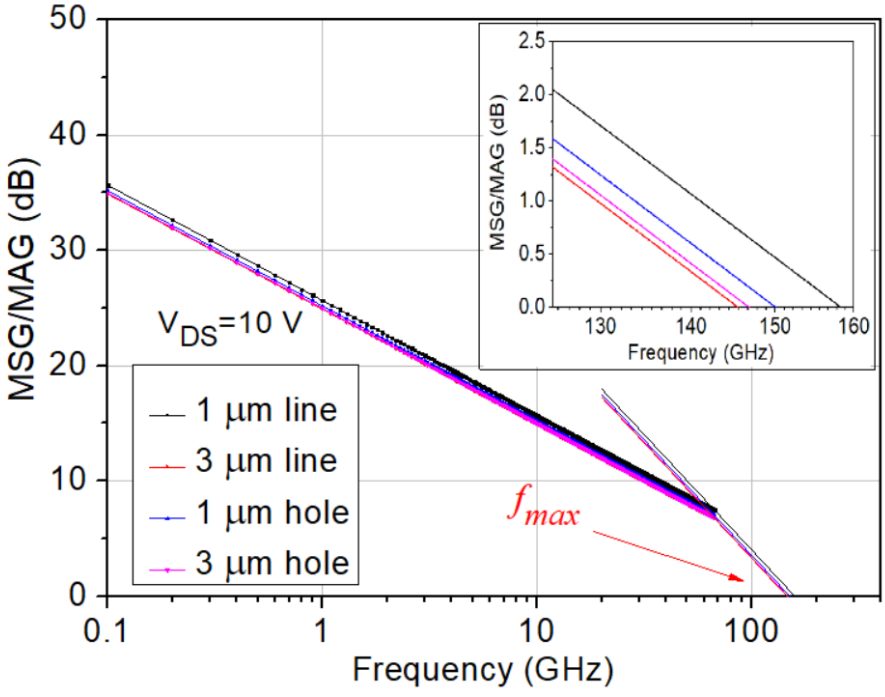


Figure 6-6. The schematic diagram of the OEP HEMT with the small-signal equivalent circuit.



(a)



(b)

Figure 6-7. The (a) current gain versus frequency graph and (b) MSG/MAG versus frequency graph for the four 2 × 25 μm OEP devices.

Table 6-3. The measured f_T, f_{max}, and extracted device parameters of the four fabricated OEP devices.

Ohmic Etching Patterns	f_T (GHz)	f_{max} (GHz)	R_s (Ω)	R_d (Ω)	C_{gs} (fF)	C_{gd} (fF)
1 μm line	36.40	158.29	4.35	2.73	91.03	9.76
3 μm line	30.90	145.50	5.04	3.43	94.84	10.82
1 μm hole	33.10	150.05	4.53	2.81	91.30	10.15
3 μm hole	32.60	146.80	4.75	2.93	93.42	10.56

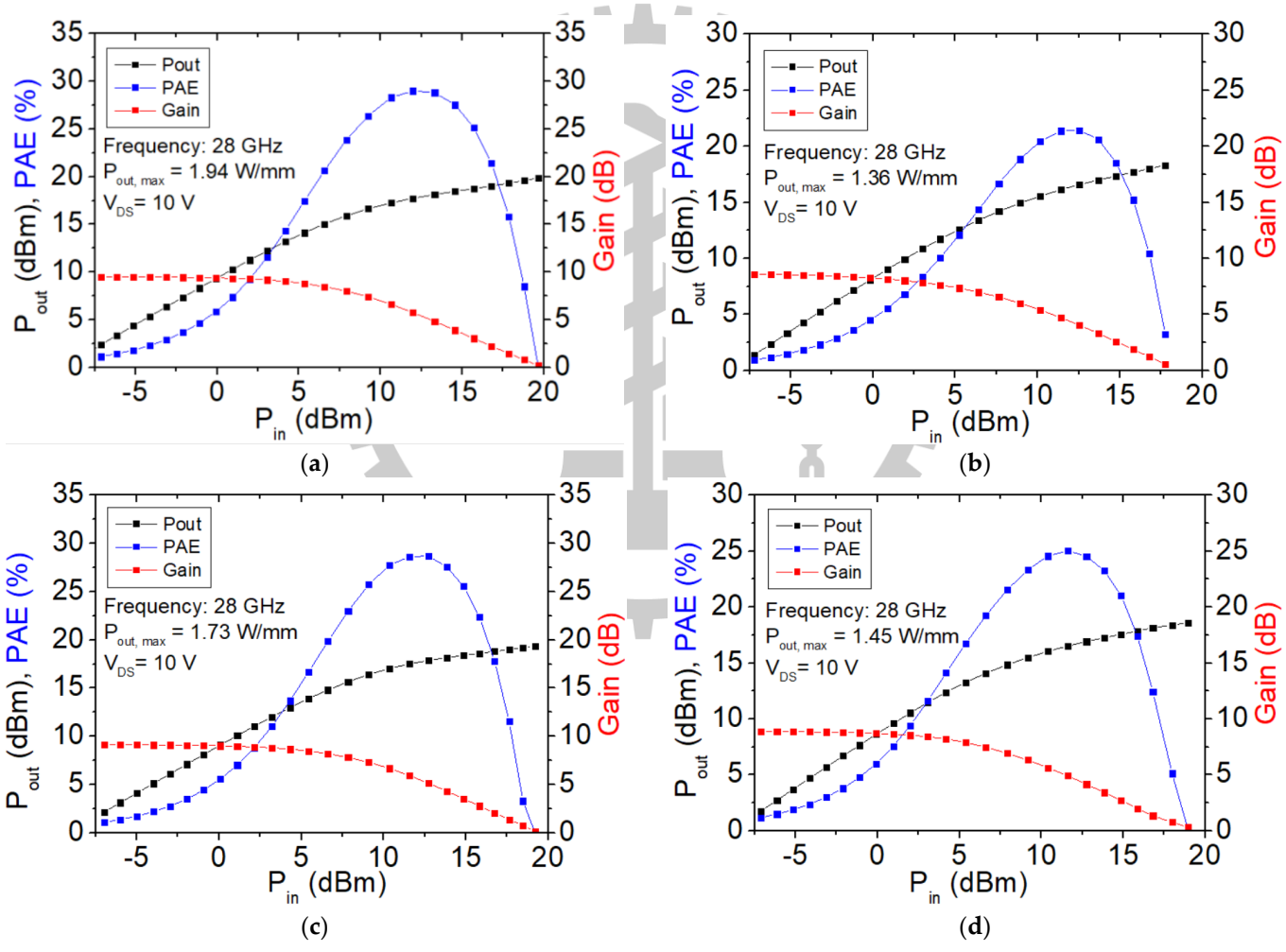
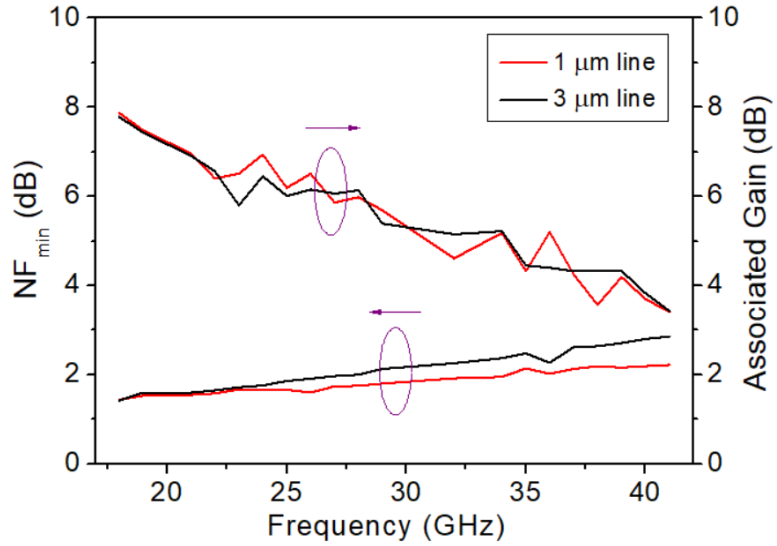


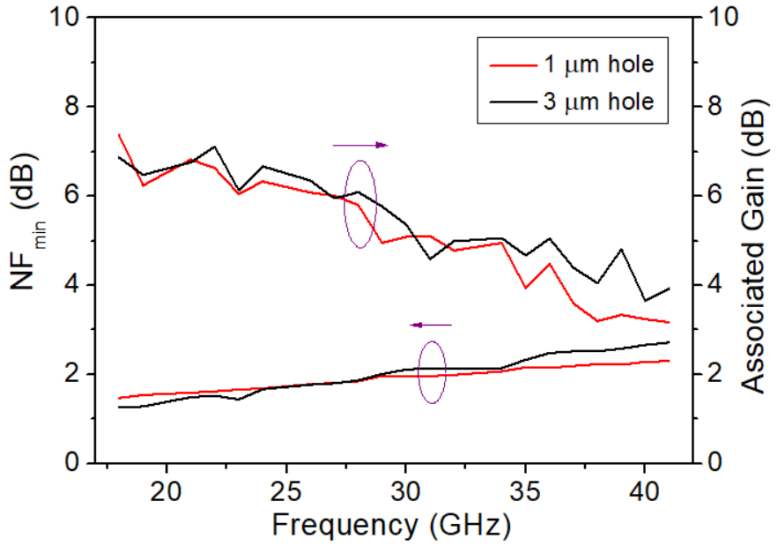
Figure 6-8. The measured large signal results for the fabricated devices with (a) 1 μm lines, (b) 3 μm lines, (c) 1 μm holes, and (d) 3 μm holes, respectively.

Table 6-4. The measured RF power results of the four fabricated OEP devices.

Ohmic Etching Patterns	PAE Peak (%)	Gain (dB)	$P_{out,\ max}$ (dBm)	$P_{out,\ max}$ (W/mm)
1 μm line	29.01	9.52	19.86	1.94
3 μm line	21.44	8.60	18.31	1.36
1 μm hole	28.70	9.12	19.36	1.73
3 μm hole	25.03	8.87	18.60	1.45



(a)



(b)

Figure 6-9. The NF_{min} versus frequency graph for the fabricated devices with (a) line patterns and (b) hole patterns.

Chapter 7

Study of AlGaN/GaN High-Electron-Mobility Transistors on Si Substrate with Thick Copper-Metallized Interconnects for Ka-Band Applications

7.1 Introduction

The improved characteristics and performances of AlGaN/GaN HEMTs fabricated with thick copper-metallized interconnects for Ka-band applications are discussed in this study. The AlGaN/GaN HEMTs in this study are fabricated on a Si substrate for future implementation of the copper-metallized process with CMOS process lines. The thick copper-metallized interconnects were fabricated on the HEMT devices after the definition of the device structure, as depicted in Figure 7-1. The wafer is then spin-coated with the AZ-5214E photoresist and then exposed under an I-line photolithography system for interconnect definition. After developing of the exposed wafer, the wafer is deposited with the Ti/Pt/Ti/Cu/Ti metal stacks using PVD to form the copper-metallized interconnects. The Ti/Pt/Ti metal stacks were deposited to act as a barrier layer to prevent copper interdiffusion. Thermal and stress tests were also done for the copper-metallized HEMTs in this study to demonstrate the stability for the designed barrier layer. DC and RF characteristics are also measured for the fabricated devices with and without the copper metallization to demonstrate the improvement in device performances.

7.2 Results and Discussion

TLM results were done for the devices with and without the 4 μm copper metallization, showing a reduction in contact resistivity from 5.2×10^{-6} to 3.5

$\times 10^{-6}$, as shown in Figure 7-2. The I_{DS}-V_{GS} and I_{DS}-V_{DS} curves were also measured for the devices without and with the 4 μm copper metallization, demonstrating an increased current density from 541.2 to 575.2 mA/mm and an increased G_m from 240.9 to 260.8 mS/mm, as shown in Figure 7-3 (a) and (b). S-parameter measurements were also performed in this study, demonstrating that the maximum stable gain (MSG)/maximum available gain (MAG) increased from 11.0 to 12.0 dB at 28 GHz and increased from 7.8 to 8.7 dB at 60 GHz for the devices without and with copper metallization, as shown in Figure 7-4. Extracted source resistances (R_s) also were also decreased from 12.5 to 8.0 Ω for the devices without and with copper metallization, respectively. The improvement of the DC characteristics, the increase in small-signal gain performance, and the reduction of the R_s may be due to the increased cross-section area after the 4 μm copper metallization. Large-signal results for the fabricated device without and with the copper metallization were also measured with the 28 GHz load-pull system, as shown in Figure 7-5. The RF power results showed an increased output power density at 3 dB compression point (P_{3dB}) from 2.3 to 2.8 W/mm, an increased PAE from 34.8 % to 44.3 %, and an increased linear gain from 7.3 to 7.6 dB. High power performance results were also measured for the fabricated larger devices (4 × 50 μm) with copper metallization, demonstrating a maximum output power density of 6.6 W/mm, a linear gain of 7.8 dB, and a PAE of 45.6 %, as shown in Figure 7-6. 10 hours of on-state stress tests and 100 hours of off-state stress tests were also performed on the devices with copper metallization and no obvious degradation in device

performance were observed, as shown in Figure 7-7, 7-8, 7-9, and 7-10. Thermal stability tests of 300°C annealing for 30 mins and thermal stress stability tests of 10 hours at 150°C operation temperature were also measured for the devices with copper metallization and no obvious degradation in device performance were observed as well, as shown in Figure 7-11 and Figure 7-12.

7.3 Conclusion

The AlGaN/GaN HEMT with a 4μm copper-metallized interconnect for Ka-band application has been fabricated in this study. The DC and RF performances demonstrated improvements after the copper metallization. Thermal stability and stress stability tests were measured for the fabricated copper-metallized devices and no obvious degradation in device performance were observed. High output power density of 6.6 W/mm with a PAE of 45.6 % were also measured for the copper metallized HEMT devices, demonstrating strong potential for high power applications at Ka Band.

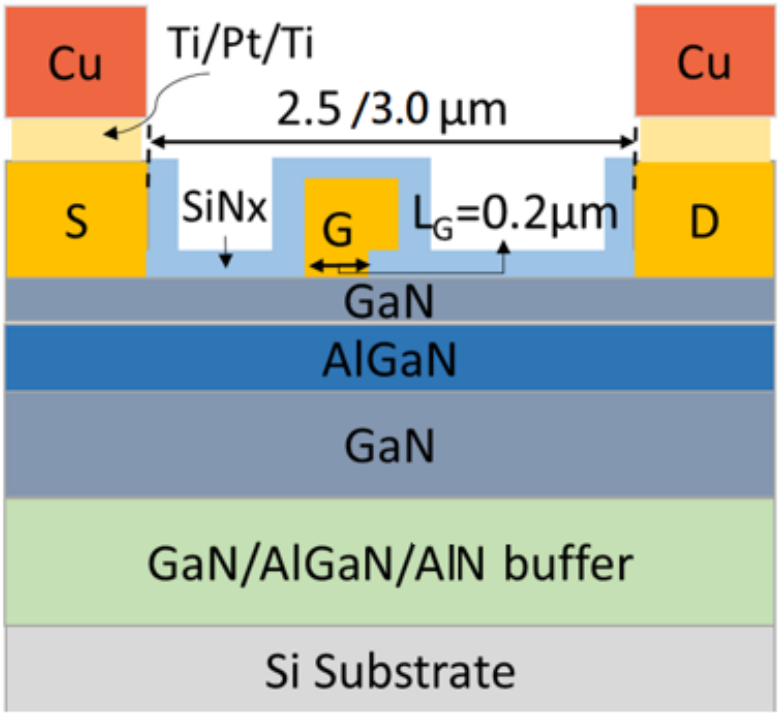


Figure 7-1. The schematic diagram of the fabricated device in this study.

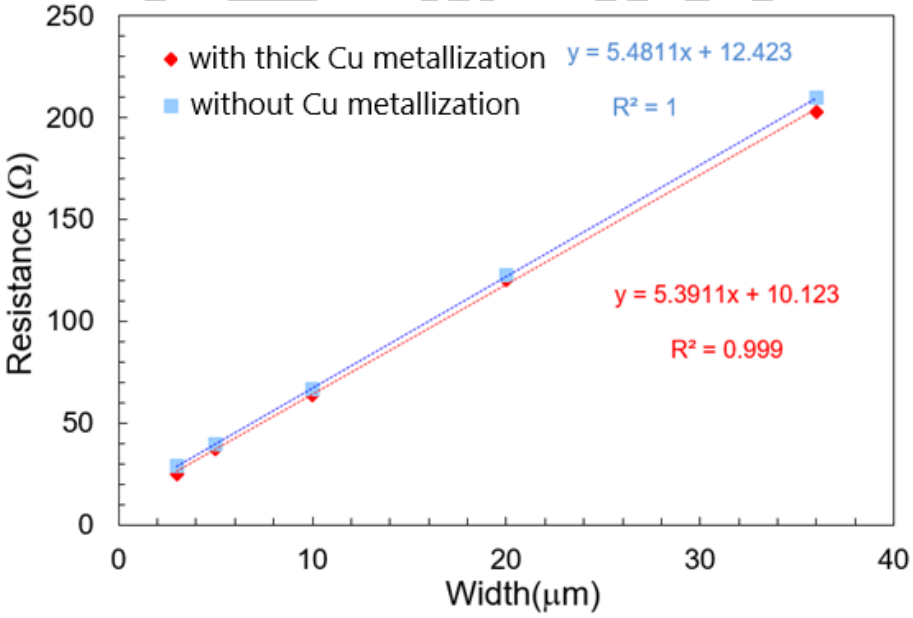


Figure 7-2. The measured TLM results of the fabricated devices with and without thick copper interconnect.

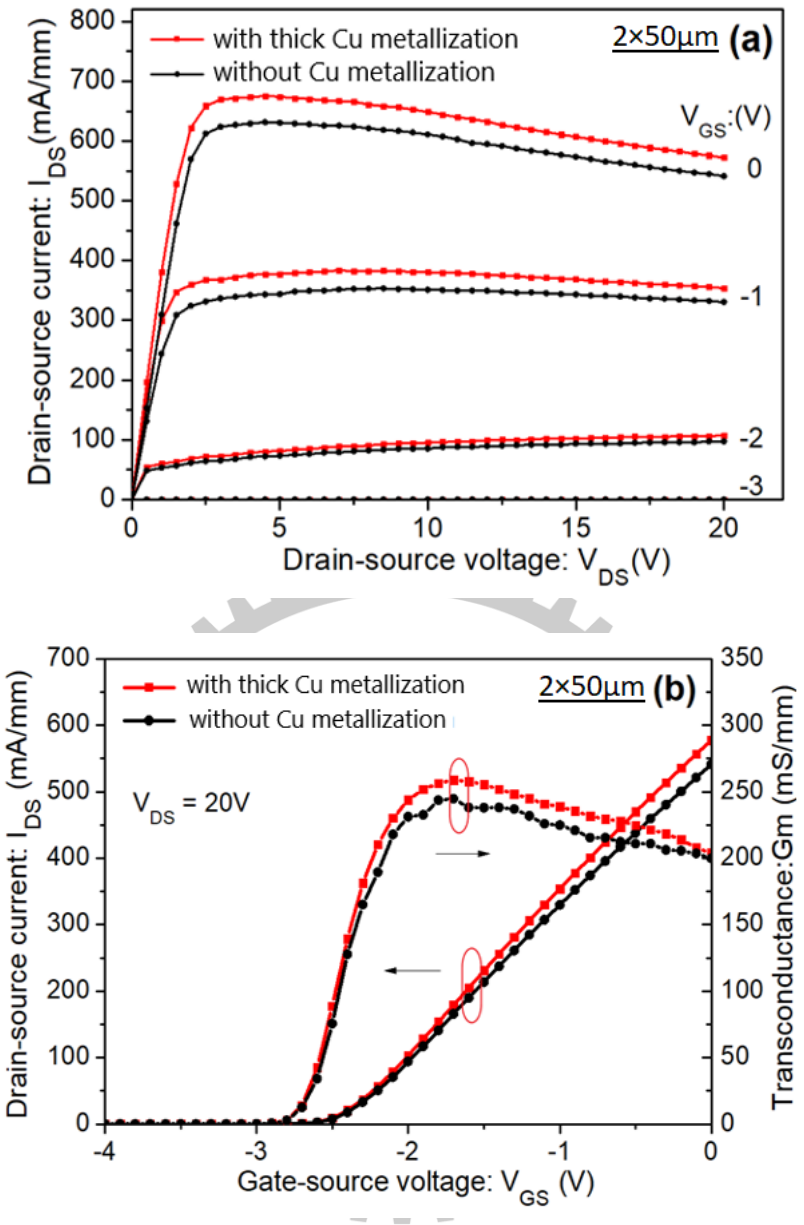


Figure 7-3. The measured (a) I_{DS}-V_{DS} and (b) I_{DS}-V_{GS} curves of the fabricated devices of 2×50 μm with and without copper interconnect.

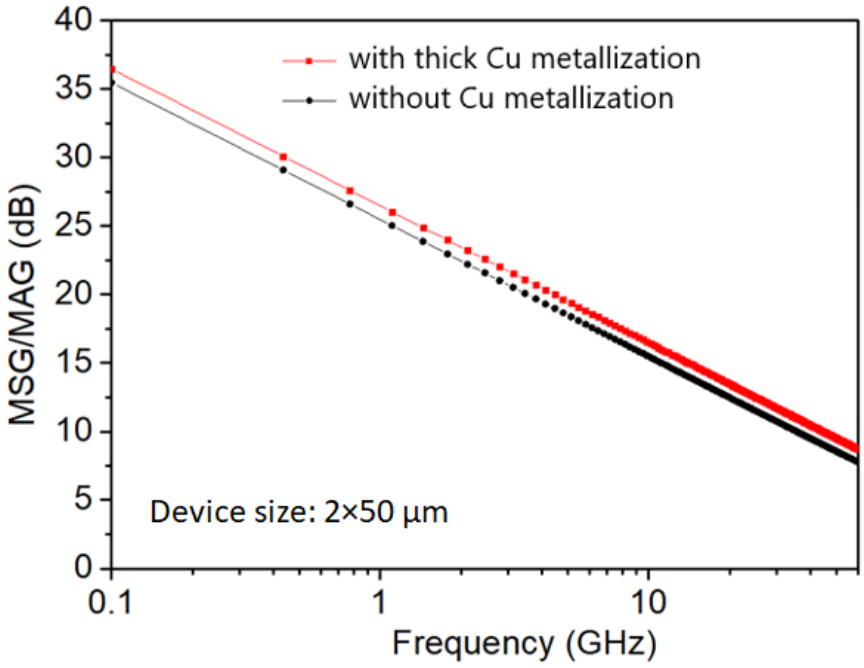


Figure 7-4. The MSG/MAG versus frequency graph of the fabricated 2×50 µm devices with and without thick copper interconnect.

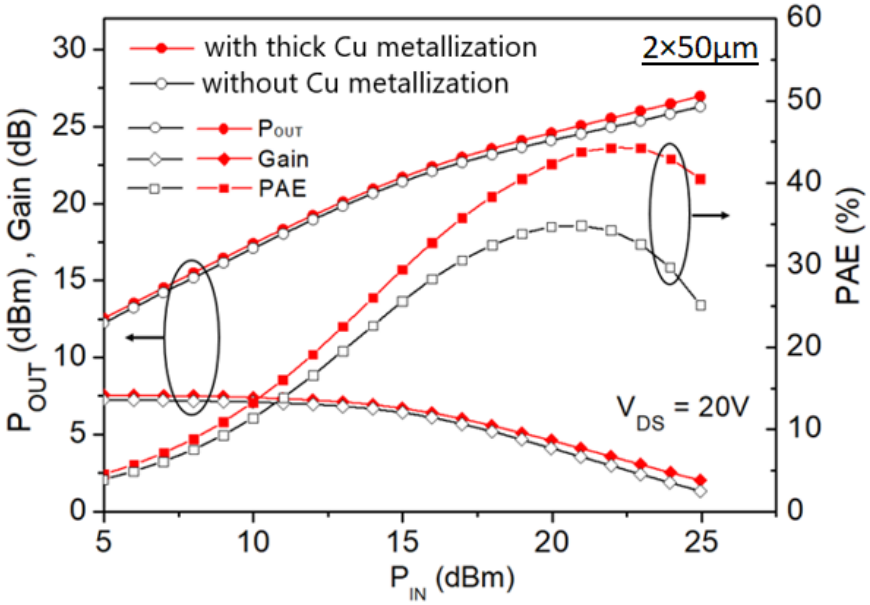


Figure 7-5. The large signal power results of the fabricated 2×50 µm devices with and without thick copper interconnect at class AB bias point.

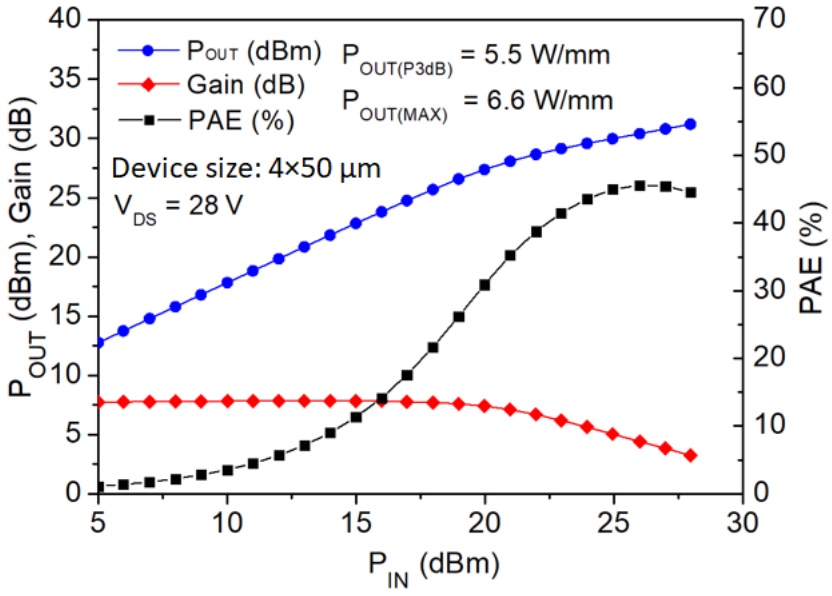


Figure 7-6. The large signal power results of the fabricated 4×50 µm device with 4 µm Cu metallization with a class A gate bias point.

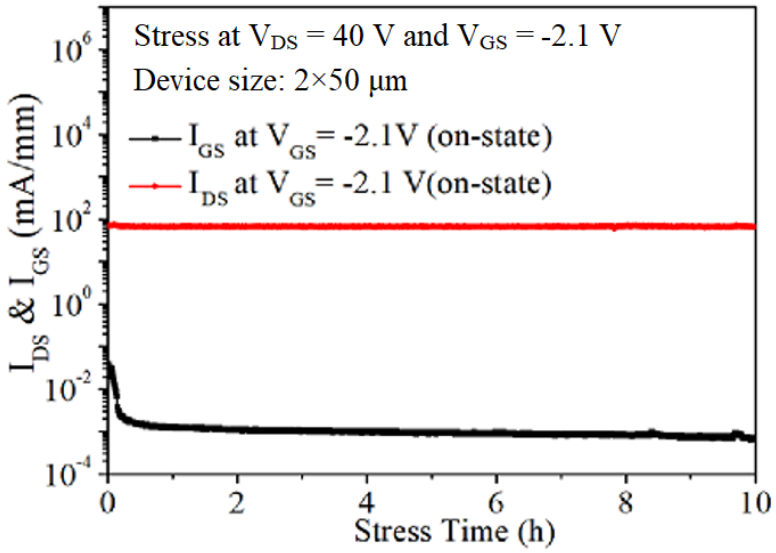


Figure 7-7. The measured on-state I_{DS} and I_{GS} for the fabricated 2×50 µm device with thick copper interconnect after a 10 hour stress test.

Table 7-1. The compared RF power results of the fabricated devices with and without thick copper interconnect and publications.

	This work				[20]	[21]	[22]	[23]			[24]
Freq. (GHz)	28				35	30	21.5	30			40
Substrate	Si				SiC	SiC	SiC	SiC			Si
Lg (nm)	200				150	150	150	150			75
Cu-metallization	w/o	w/			w/o						
Device size (μm)	2×50	2×50	2×50	4×50	8×50	6×50	8×50	2×50	6×50	8×50	2×50
V_{DS} (V)	20	20	28	28	20	20	20	20	17.5	15	25
PA E (%)	34.8	44.3	35.7	45.6	49	39	50	39	29	40	12.5
Pout (@P3dB) (W/mm)	2.3	2.8	4.2	5.2	-	-	3.2	-	-	-	-
Pout (PAE peak) (W/mm)	2.8	3.6	5.0	5.5	3.0	3.5	-	5.0	2.5	3.2	-
Pout (MAX) (W/mm)	4.2	5.0	6.1	6.6	-	-	-	6.0	-	-	2.7

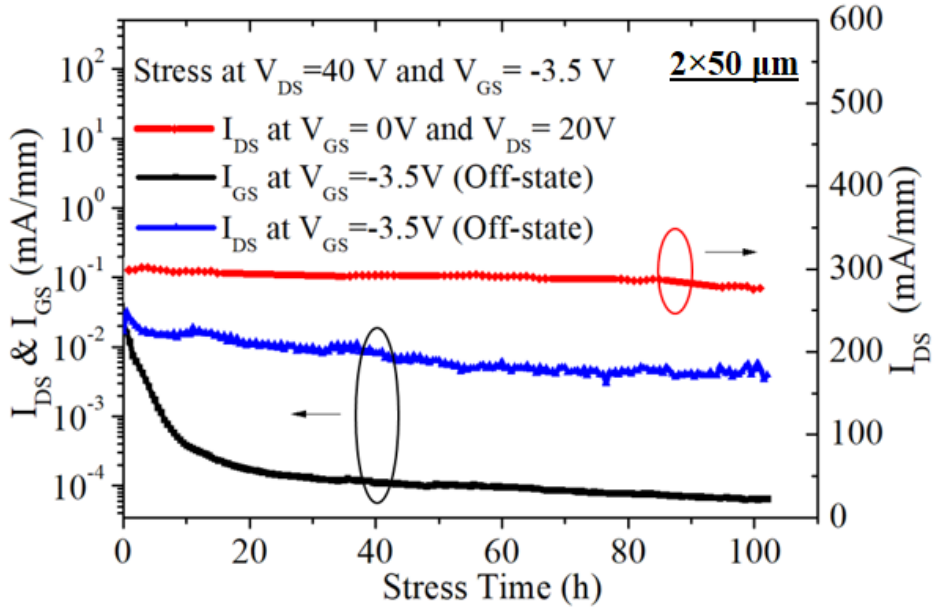


Figure 7-8. The measured off-state I_{DS}, off-state I_{GS}, and on-state I_{DS} for the fabricated 2×50 µm device with thick copper interconnect after a 100 hour stress test.

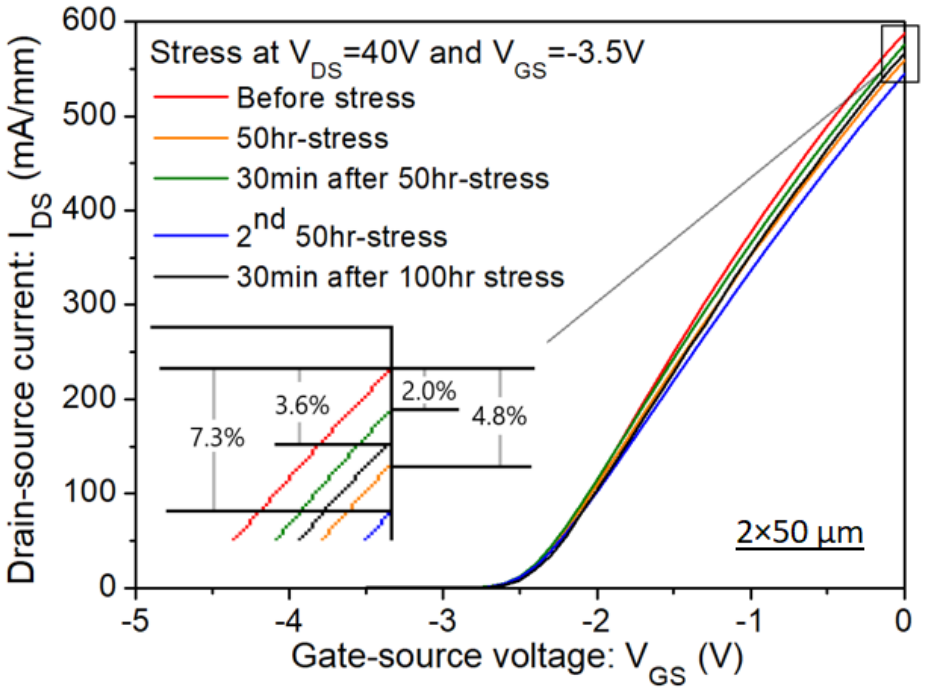


Figure 7-9. The measured off-state stress test results at 40 V for the fabricated 2×50 µm device with a thick copper interconnect.

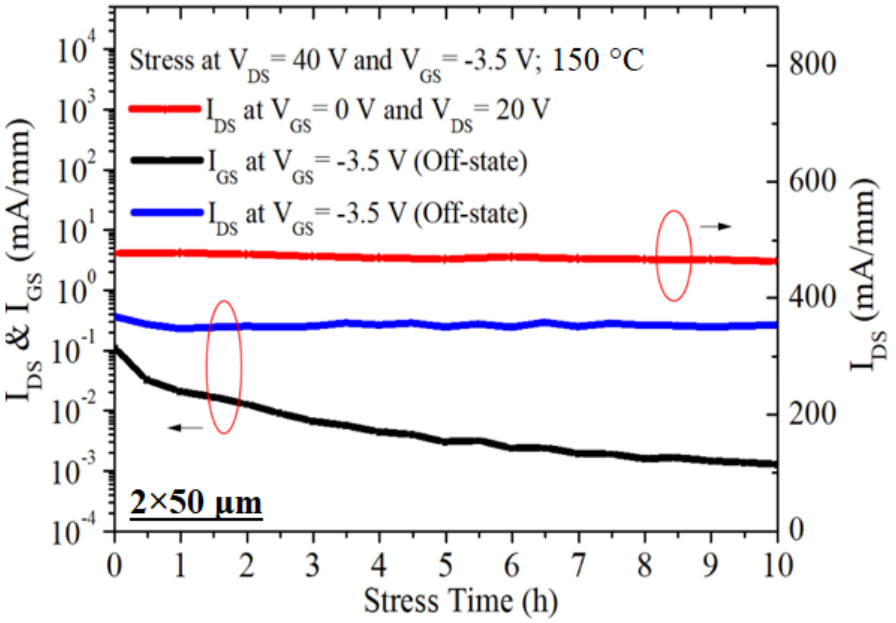


Figure 7-10. The measured off-state I_{DS}, off-state I_{GS}, and on-state I_{DS} at 150 °C for the fabricated 2×50 µm device with a thick copper interconnect after a 10 hour stress test.

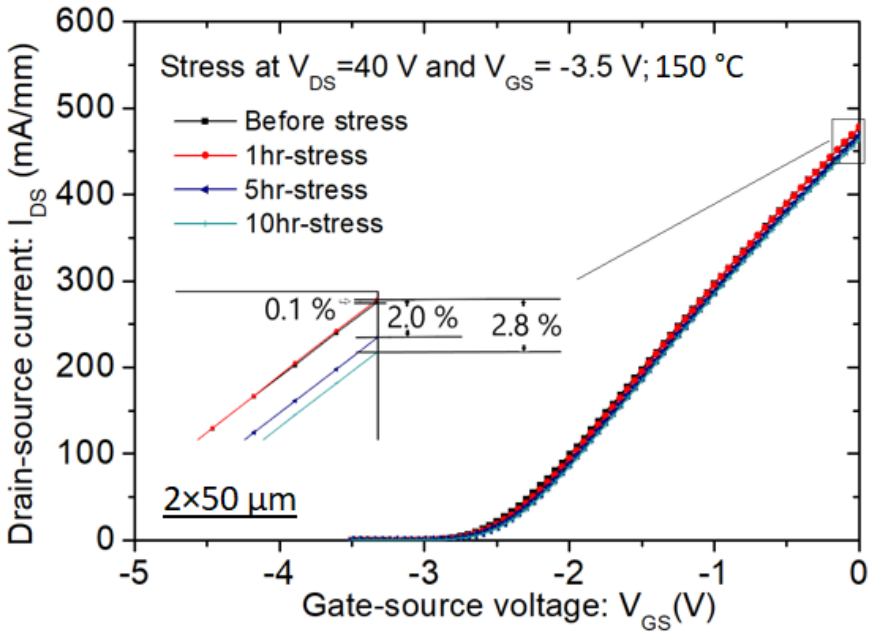


Figure 7-11. The transfer characteristics for the fabricated 2×50 µm deivce with thick copper interconnect after various off-state stress tests at 150 °C.

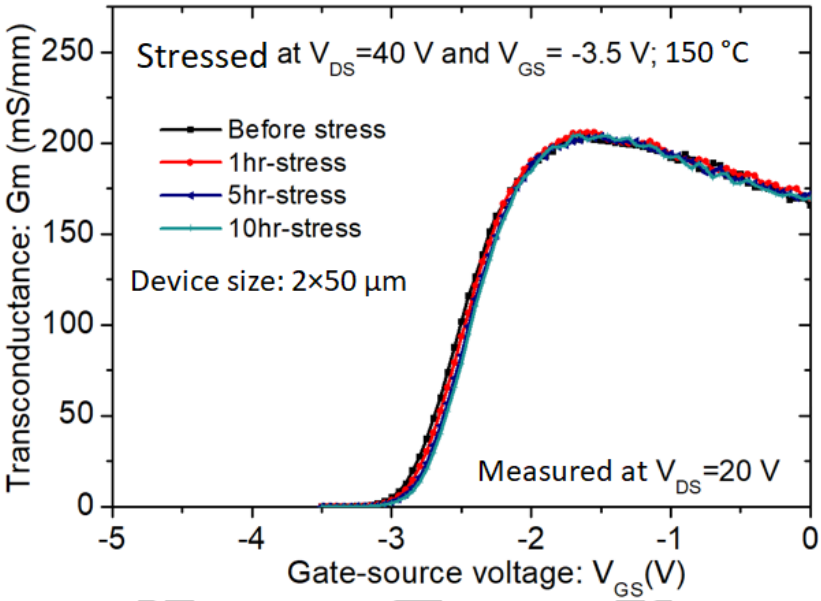


Figure 7-12. The measured G_m-V_{GS} results of the fabricated 2×50 µm devices (L_{SD}= 3.0 µm) after various stress tests at 150 °C.

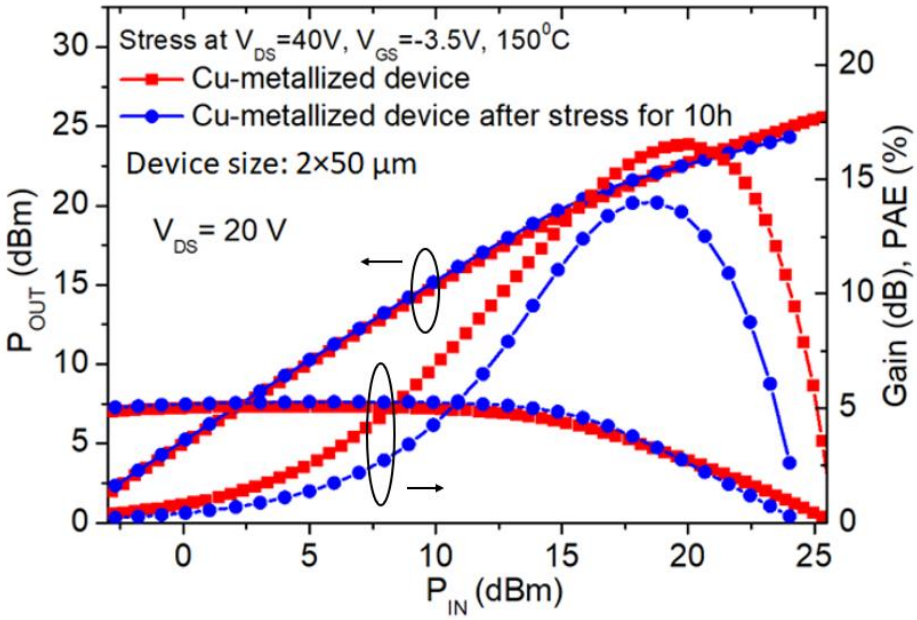


Figure 7-13. The large signal power results of the fabricated 2×50 µm devices with thick copper interconnect (L_{SD}= 3.0 µm) before and after the 10 hour stress test at 150 °C.

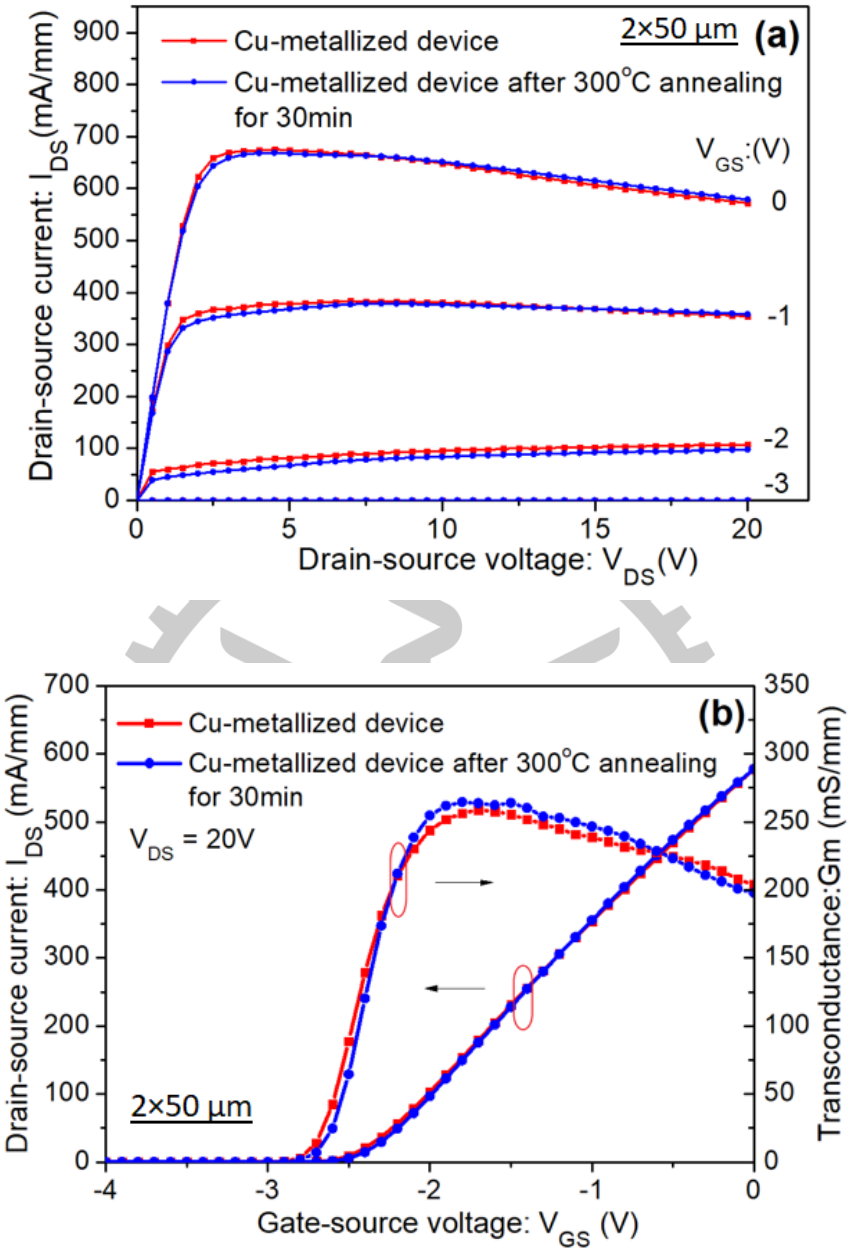


Figure 7-14. The measured (a) I_{DS}-V_{DS} and (b) I_{DS}-V_{GS} & G_m-V_{GS} of the fabricated 2×50 µm device with thick copper interconnect (L_{SD}= 2.5 µm) before and after being annealed at 300 °C for 30 minutes.

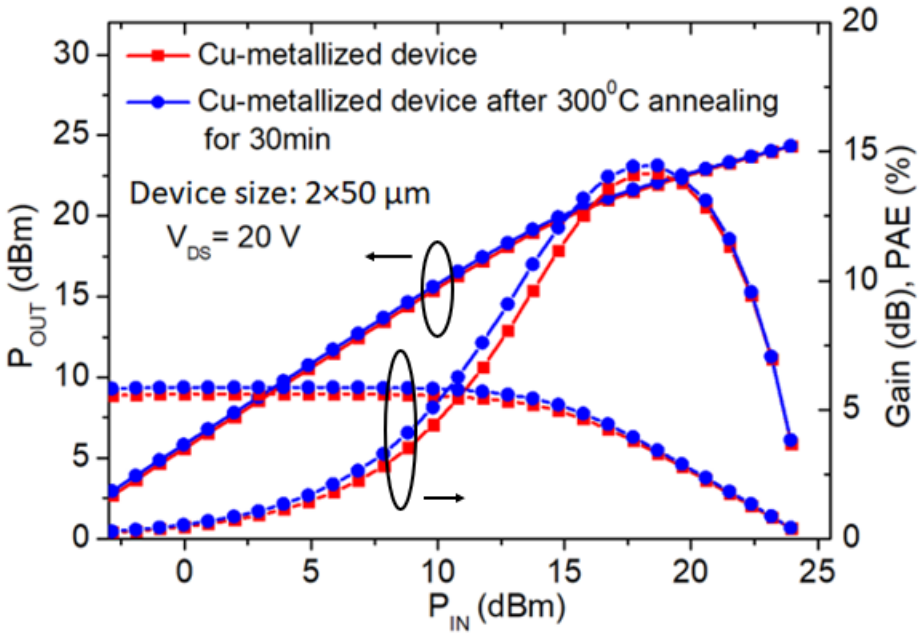


Figure 7-15. The measured large signal power results of the fabricated 2×50 µm device with thick copper interconnect (L_{SD}= 2.5 µm) before and after being annealed at 300 °C for 30 minutes.

Chapter 8

Conclusions

This thesis covers the research and development of four advanced process steps for AlGaN/GaN HEMT fabrication especially for Ka-band applications, including the 2-step photolithography process, the fin-shaped gate design, the ohmic etching patterns, and the thick copper metallization. The integration of these process steps reduces the device gate lengths with increased yield, increases gate controllability with improved linearity, reduces the ohmic contact resistance with improved power performance, and reduces the source and drain resistances with thermal and stress stability. Overall, the advancements discussed in this thesis demonstrate improved RF performances regarding operation frequency, output power, 3rd order intermodulation, and PAE. Further integration of these advanced process steps shows the potential of application in the B5G communication system.

Reference

[1] F. H. Raab et al., "Power amplifiers and transmitters for RF and microwave," in IEEE Transactions on Microwave Theory and Techniques, vol. 50, no. 3, pp. 814-826, March 2002, doi: 10.1109/22.989965.

[2] J. S. Moon et al., "55% PAE and High Power Ka-Band GaN HEMTs With Linearized Transconductance via $\hbox{n}+$ GaN Source Contact Ledge," in IEEE Electron Device Letters, vol. 29, no. 8, pp. 834-837, Aug. 2008, doi: 10.1109/LED.2008.2000792.

[3] M.-Y. Kao, C. Lee, R. Hajji, P. Saunier, and H.-Q. Tserng, “AlGaN/GaN HEMTs with PAE of 53% at 35 GHz for HPA and multi-function MMIC applications,” in IEEE/MTT S Int. Microw. Symp. Tech. Dig., 2007, pp. 627–629, doi: 10.1109/MWSYM.2007.379979.

[4] F. Medjdoub, M. Zegaoui, B. Grimbert, D. Ducatteau, N. Rolland, and P. A. Rolland, “First demonstration of high-power GaN-on-silicon transistors at 40 GHz,” IEEE Electron Device Lett., vol. 33, no. 8, pp. 1168–1170, Aug. 2012, doi: 10.1109/LED.2012.2198192.

[5] P. Altuntas et al., “Power performance at 40 GHz of AlGaN/GaN high-electron mobility transistors grown by molecular beam epitaxy on Si(111) substrate,” IEEE Electron Device Lett., vol. 36, no. 4, pp. 303–305, Apr. 2015, doi: 10.1109/LED.2015.2404358.

[6] Y. Zhang et al., “High-temperature-recessed millimeter-wave AlGaN/GaN HEMTs with 42.8% power-added-efficiency at 35 GHz,” IEEE Electron Device Lett., vol. 39, no. 5, pp. 727–730, May 2018, doi: 10.1109/LED.2018.2822259.

[7] R. C. Fitch et al., “Implementation of high-power density X-band AlGaN/GaN high electron mobility transistors in a millimeter wave monolithic microwave integrated circuit process,” IEEE Electron Device Lett., vol. 36, no. 10, pp. 1004–1007, Oct. 2015, doi: 10.1109/LED.2015.2474265.

[8] Palacios, T.; Chakraborty, A.; Heikman, S.; Keller, S.; DenBaars, S.P.; Mishra, U.K. AlGaN/GaN high electron mobility transistors with InGaN back-barriers. IEEE Electron Device Lett. 2006, 27, 13–15.

[9] S. Arulkumaran, G. I. Ng, and S. Vicknesh, “Enhanced breakdown voltage with high Johnson’s figure-of-merit in 0.3-$\mu{\rm m}$ T gate AlGaN/GaN HEMTs on silicon by $({\rm NH}_{4})_{2}{\rm S}_{x}$ treatment,” IEEE Electron Device Lett., vol. 34, no. 11, pp. 1364–1366, Nov. 2013, doi: 10.1109/LED.2013.2279882.
[10] Y.-C. Lin et al., “Study of the mesa etched tri-gate InAs HEMTs with extremely low SS for low-power logic applications,” in Proc. China Semicond. Technol. Int. Conf. (CSTIC), 2018, pp. 1–3, doi: 10.1109/CSTIC.2018.8369315.
[11] S.-J. Yeon, M. Park, and K.-S. Seo, “Novel sloped etch pro cess for 15nm InAlAs/InGaAs metamorphic HEMTs,” in Proc. 7th IEEE Conf. Nanotechnol. (IEEE NANO), 2007, pp. 1152–1155, doi: 10.1109/NANO.2007.4601387.
[12] M. -W. Lee et al., "Over 10W/mm High Power Density AlGaN/GaN HEMTs With Small Gate Length by the Stepper Lithography for Ka-Band Applications," in IEEE Journal of the Electron Devices Society, vol. 11, pp. 311-318, 2023, doi: 10.1109/JEDS.2023.3277796.
[13] Lee, M.-W.; Lin, Y.-C.; Hsu, H.-T.; Gamiz, F.; Chang, E.-Y. Improvement of AlGaN/GaN HEMTs Linearity Using Etched-Fin Gate Structure for Ka Band Applications. Micromachines 2023, 14, 931. https://doi.org/10.3390/mi14050931
[14] Lee, M.-W.; Chuang, C.-W.; Gamiz, F.; Chang, E.-Y.; Lin, Y.-C. Improvement of AlGaN/GaN High-Electron-Mobility Transistor Radio Frequency Performance Using Ohmic Etching Patterns for Ka-Band Applications. Micromachines 2024, 15, 81. https://doi.org/10.3390/mi15010081
[15] Lee, M., Lin, Y., Lai, K., Weng, Y., Hsu, H. and Chang, E.Y. (2023), Study of AlGaN/GaN High-Electron-Mobility Transistors on Si Substrate with Thick Copper-Metallized Interconnects for Ka-Band Applications. Phys. Status Solidi A, 220: 2200536. https://doi.org/10.1002/pssa.202200536

國立陽明交通大學學位論文發表形式確認書

本人 李明文 依據「國立陽明交通大學著作彙編之學位論文應行注意事項」第四點第一項規定，於2024 年 06 月 28 日與指導教授討論並取得共識：

☑ 在符合「本校博碩士學位論文格式規範」下，本人論文正文 之部分或全部以著作彙編形式為之，並遵守學校訂定著作彙 編之學位論文應行注意事項獲得學位採認準則，並覈實填寫「著作彙編之學位論文資訊及彙編學術著作之共同作者貢獻 聲明書」。

☐ 本人論文不採用著作彙編形式為之。

本人簽名： Ming-Wen Lee 李明文

學 號： 0654016

指導教授簽名： Edward yi chang

系所（學位學程）主管簽名或蓋章：

中 華 民 國 113 年 06 月 28 日

micromachines

Article

Improvement of AlGaN/GaN HEMTs Linearity Using Etched-Fin Gate Structure for Ka Band Applications

Ming-Wen Lee [1,2], Yueh-Chin Lin [1], Heng-Tung Hsu [1], Francisco Gamiz [2] and Edward-Yi Chang [1,*]

[1] International College of Semiconductor Technology, National Yang Ming Chiao Tung University, Hsinchu City 30010, Taiwan; ericlmw.st06@nycu.edu.tw (M.-W.L.); nctulin@yahoo.com.tw (Y.-C.L.); hthsu@nctu.edu.tw (H.-T.H.)
[2] Department of Electronics and Computer Technology, University of Granada, 18014 Granada, Spain; fgamiz@ugr.es
* Correspondence: edc@nycu.edu.tw; Tel.: +886-3-5712121

Abstract: In this paper, AlGaN/GaN high electron mobility transistors (HEMTs) with etched-fin gate structures fabricated to improve device linearity for Ka-band application are reported. Within the proposed study of planar, one-etched-fin, four-etched-fin, and nine-etched-fin devices, which have 50-µm, 25-µm, 10-µm, and 5-µm partial gate widths, respectively, the four-etched-fin gate AlGaN/GaN HEMT devices have demonstrated optimized device linearity with respect to the extrinsic transconductance (G_m) value, the output third order intercept point (OIP3), and the third-order intermodulation output power (IMD3) level. The IMD3 is improved by 7 dB at 30 GHz for the 4 × 50 µm HEMT device. The OIP3 is found to reach a maximum value of 36.43 dBm with the four-etched-fin device, which exhibits high potential for the advancement of wireless power amplifier components for Ka band applications.

Keywords: AlGaN/GaN HEMTs; etched-fin gate structure; Ka band; linearity; SiC substrate

Citation: Lee, M.-W.; Lin, Y.-C.; Hsu, H.-T.; Gamiz, F.; Chang, E.-Y. Improvement of AlGaN/GaN HEMTs Linearity Using Etched-Fin Gate Structure for Ka Band Applications. *Micromachines* **2023**, *14*, 931. https://doi.org/10.3390/mi14050931

Academic Editor: Sadia Ameen

Received: 31 March 2023
Revised: 19 April 2023
Accepted: 24 April 2023
Published: 25 April 2023

1. Introduction

Over the past decade, the world has seen the rapid spread of transmitting electronic devices in favor of networking and communication systems, such as artificial intelligence (AI), Internet of Things (IoT), and big data. Researchers and industrial engineers have been designing high-speed and high-stability wireless components with III-V semiconductor materials [1–4]. Therefore, high electron mobility transistors (HEMTs) have now been widely used in high-frequency electronics, such as antennas and broadband satellites [2]. In addition to Gallium Arsenide (GaAs) HEMTs [5–7], Gallium Nitride (GaN) HEMTs [8–12] have been used in high radio frequency (RF) power components, such as an mm-wave power amplifier, due to its high breakdown voltage, high critical field, wide bandgap, and high electron peak velocity [13–16].

At an ideal linear region, an RF HEMT device works as an active device in a Monolithic Microwave Integrated Circuit (MMIC) and could amplify the RF signals with a constant power gain. Nevertheless, the nonlinear characteristics of a realistic solid state HEMT device cause the power gain to decrease after a certain input power, thereby decreasing the device's output power. Moreover, in a two harmonic wave tone load-pull test, the intermodulation distortion signals (IMD) of the device under test (DUT) increased rapidly with the input power level, which ultimately distorted the fundamental power signal. This is because the input signal of one of the harmonic waveforms intermodulates with the other, and generates third-order intermodulation products, which have now been widely used to quantify the linearity performance of HEMT devices [17,18].

When it comes to improving the linearity of a HEMT device at very high frequency, i.e., the Ka band, the gate controllability performance, such as the G_m and G_m flatness of the device, becomes the critical factor for the improvement of the device's linearity characteristics,

such as the third-order output intercept point (OIP3) and third-order intermodulation output power (IMD3) [19]. A low second derivative value of the G_m curve, meaning a flat G_m curve, is favorable for the RF HEMT device to show that the device can withstand the gate voltage swing under high RF input power, keeping the device's high switching capability as stable as possible [20]. Researchers have shown that better gate controllability could be achieved by etching AlGaN/GaN device gates along the gate width to form fin-shaped gates, overcoming the deficiencies of small gate length GaN devices, which have exhibited poor gate control over the 2DEG channel [21]. The fin-shaped gate structure provides the GaN devices with a high G_m value, as well as a flatter G_m curve [22,23], which is suitable for high-frequency device operation and serves to mitigate the poor gate control caused by short-channel effects for short-channel AlGaN HEMTs with wide bandgaps [24,25].

However, due to large amounts of etched-away AlGaN barrier layers, AlGaN/GaN FinFETs often suffer from a low saturation current, which makes them unable to provide enough output power for high-frequency data transmission. To increase the RF linearity performance of the AlGaN/GaN HEMT device, as well as maintaining the 2DEG current, the number of etched fins should be limited and optimized.

In this study, AlGaN/GaN HEMTs with different etched-fin gate structures are investigated to improve device linearity for Ka band device applications. The direct current (DC) and RF performance are investigated, and the IMD3 and the OIP3 values are measured to study the linearity improvement of the GaN HEMT device with optimized etched-fin gate structures. The gate controllability as well as linearity performance of the HEMT devices with respect to the different drain biases have also been measured and discussed.

2. Materials and Methods

The AlGaN/GaN HEMTs on a SiC substrate wafer was grown by metal organic vapor deposition (MOCVD) on a 4-inch SiC substrate. From the bottom to the top, the structure of the AlGaN/GaN HEMT consists of a 900 nm i-GaN buffer layer, a 500 nm GaN channel layer, a 1 nm AlN spacer layer, and a 22 nm $Al_{0.22}Ga_{0.78}N$ barrier layer; the device's 3D structure is depicted in Figure 1. The room-temperature electron mobility of 1700 $cm^2/V{\cdot}s$ and a sheet carrier density of $8.5 \times 10^{12}/cm^2$ were measured for the structure after material growth.

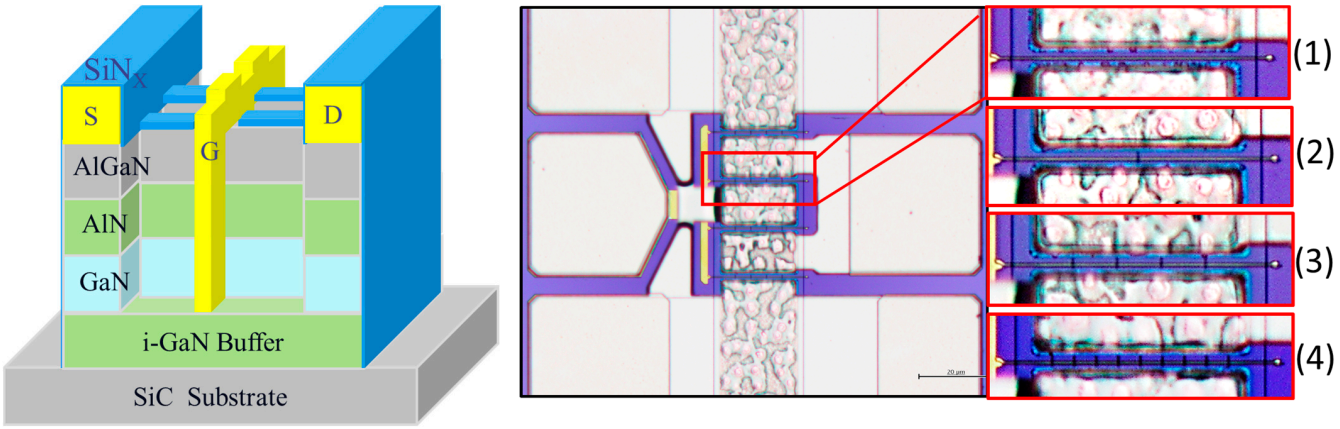


Figure 1. (**a**) The 3D epitaxial and device structure of a 1-etched-fin AlGaN/GaN HEMT device with a single gate, and (**b**) the top-view micrographs of the (1) planar, (2) 1-etched-fin, (3) 4-etched-fin, and (4) 9-etched-fin gate structures.

There are four major steps in the fabrication of AlGaN/GaN HEMTs on a SiC substrate, which include Ohmic contact formation, active region definition, gate formation, and thick metal interconnect fabrication. The Ohmic metal of Ti/Al/Ni/Au was deposited by an e-gun evaporator, and then annealed by a rapid thermal anneal system (RTA) at 850 °C for

30 s in an N_2 atmosphere. Then, the B^{11+} ion implantation isolation process was used to define the active region. The etched-fin gate region was formed by first depositing the SiN_X layer with the plasma-enhanced chemical vapor deposition (PECVD) system and further covering it with an e-beam photoresist.

After this, the etched-fin area was defined using the JEOL e-beam lithography system. The defined fin regions were further etched away using the inductively coupled plasma (ICP) system. In this study, a planar structure (no etched fins) and three different etched-fin gate structures were designed. Trench numbers of 1, 4, and 9 were etched away, with a trench width of 500 nm and a trench depth of around 550 nm to the buffer layer.

Careful removal of the e-beam photoresist after etched fin definition is critical to prevent e-beam photoresist residuals, which may affect the gate length definition during the next e-beam lithography process and may degrade the gate controllability due to poor Schottky contact after gate metal deposition. A larger fin width of up to 500 nm also ensures that the fin etch process is stable and uniform over the whole gate width, which is due to the low aspect ratio of the fin depth and the fin width.

The gate length was defined using the stepper lithography system after the etch fin process, and the wafer was uniformly dipped in a diluted HCl solution ($HCl:H_2O$ = 1:10) for 1 min before metal deposition to remove any AlGaN barrier layer native oxides. A Ni/Au (50 nm/500 nm) gate Schottky metal was deposited on the defined gate region and was deposited down the etched-fin regions, forming direct contact with the AlGaN barrier layers. Finally, a 150 nm SiN_X was passivated on the wafer using the PECVD and a 2 μm thick Au metallization was deposited on the source and drain pads. The schematic cross-section and the top-view micrographs of the device gate structure are shown in Figure 1a,b, respectively, showing the epitaxial material layers and the gate structure with (1) a planar format, (2) 1 etched fin, (3) 4 etched fins, and (4) 9 etched fins.

3. Results and Discussion

Here, 4 × 50 μm AlGaN/GaN HEMTs with different etched-fin gate structures have been fabricated and measured to compare their linearity performance. Figure 2 shows the I_{DS}-V_{GS} and G_m-V_{GS} comparison curves of the fabricated devices with no etched fins (planar), one etched fin (one trench), four etched fins (four trenches), and nine etched fins (nine trenches). The device with four etched fins exhibits the highest G_m value and the device with nine etched fins has a highest threshold voltage (V_{th}) of −4.05 V. The V_{th} in this study is defined as the V_{GS} when I_{DS} reaches 1 mA/mm. The G_m value of the four-etched-fin device increased up to 14% compared to that of the planar device and started to degrade when the etched fin number was increased to nine, which may have been due to the lowering of the gate controllability caused by the increased fin-gate field effect [26], which is also discussed with the Technology Computer-Aided Design (TCAD) simulation results in this study. These transfer characteristics demonstrate the effectiveness of the etched-fin structure in increasing the gate controllability, the device's gate switching capability, and the potential to withstand voltage and current swinging under high input power RF tests.

Next, S-parameter results were measured on-wafer using the E8361C PNA network analyzer and the 4142B DC supplier. The system was calibrated with a short open load-through calibration standard. The calibration accuracy was verified by ensuring that both S21 and S12 of the through standard were less than ±0.01 dB and that both S11 and S22 were less than −45 dB within the measured frequency range after calibration [27]. The current gain (H_{21}) and maximum stable power gain (MSG) were derived using Microwave Office XL, and the f_T and f_{Max} of the devices were obtained by extrapolating the gain curves with a slope of −20 dB/decade. Since the current gain versus frequency curves began to deviate from the slope of −20 dB/decade, the gain values above 25 GHz were hidden for clear visualization. The small signal results show obvious improvements with the etched-fin gate structure, and the four-etched-fin device exhibits the highest f_T and f_{Max} values of 38.7 GHz and 91.9 GHz among the four device structures at a drain bias of 20 V and a gate

bias of −3.05 V, as shown in Figure 3. The f_T and f_{Max} of the nine-etched-fin device did not increase with the increased etched fins, which is due to the lowered transconductance and increased gate-to-source capacitance (C_{gs}) resulting from the doubled etched fins compared to the four-etched-fin device. The C_{gs} increases with the fin number due to the increased contact area between the gate metal and the semiconductor sidewall, causing the change in f_T and f_{Max}, as shown in Figure 3.

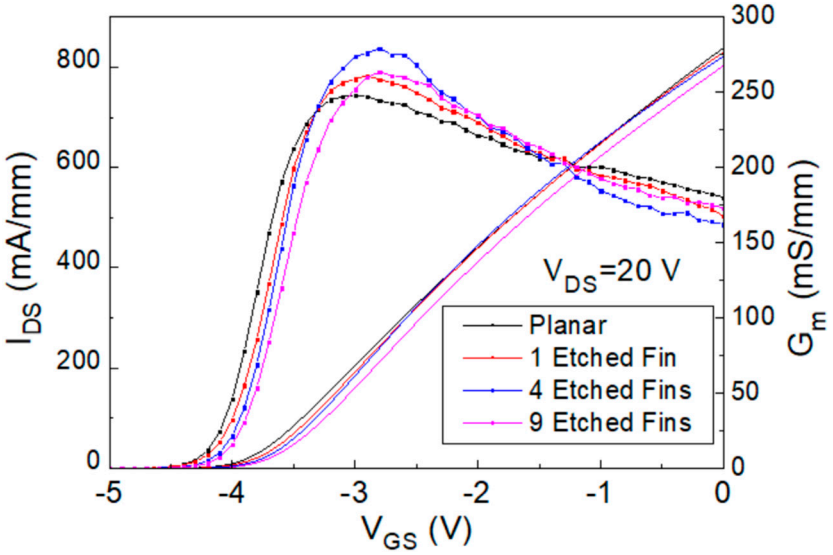


Figure 2. I_{DS}-V_{GS} graph of the fabricated planar, 1-etched-fin, 4-etched-fin, and 9-etched-fin AlGaN/GaN HEMTs on a SiC substrate.

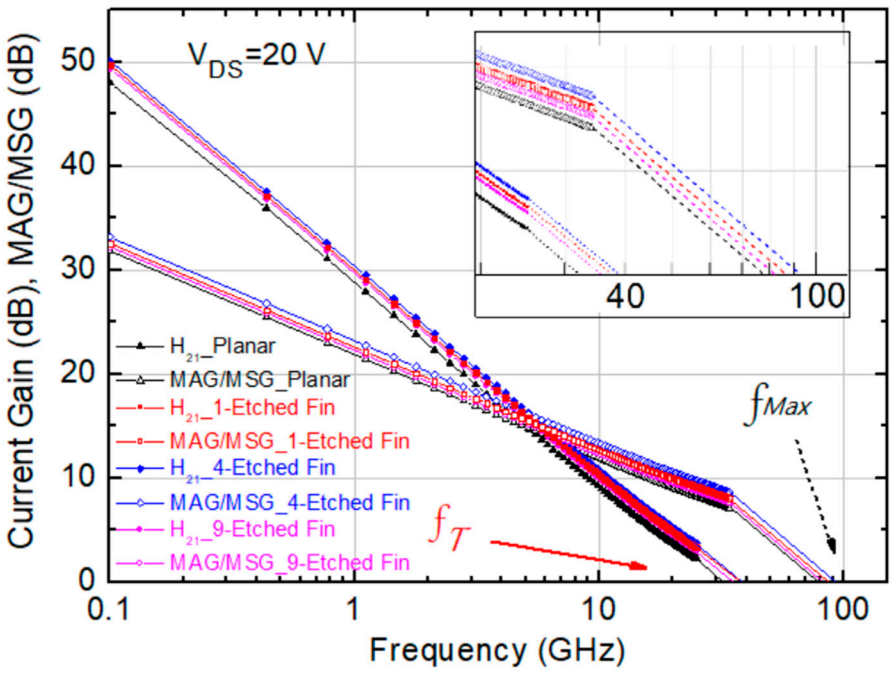


Figure 3. Measured small signal characteristics of the AlGaN/GaN HEMTs on SiC substrate with the planar, 1-etched-fin, 4-etched-fin, and 9-etched-fin gate structures at V_{DS} = 20 V and V_{GS} at G_m, peak.

The polynomial curve fitting technique, using (1), was applied to investigate the I_{DS}-V_{GS} curves of the etched-fin devices [18].

$$G_m(V_{GS}) = \frac{\partial I_{DS}(V_{GS})}{\partial V_{GS}} = a_1 + 2a_2V_{GS} + 3a_3V_{GS}^2 + 4a_4V_{GS}^3 + 5a_5V_{GS}^4 + \cdots . \quad (1)$$

Therefore, if we analyze the linearity of the I_{DS}-V_{GS} curves, we can see that the I_{DS} increases linearly with V_{GS}, giving a lower a_3 and a_5, with a larger a_1 [28]. The I_{DS}-V_{GS} polynomial first-, third-, and fifth-order coefficients of V_{DS} = 20 V are listed in Table 1. Decreased a_3/a_1 and a_5/a_1 values of the devices with four and nine etched fins have been observed, indicating the relatively lower a_3 and a_5 values with relatively higher a_1 values.

Table 1. Comparison of the DC characteristics of the four different device structures at V_{DS} = 20 V.

	Planar	1-Etched-Fin	4-Etched-Fin	9-Etched-Fin
I_{DSS} (I_{DS} at V_{GS} = 0 V, mA/mm)	839	830	822	803
$G_{m,\,max}$ (mS/mm)	247	261	279	264
Threshold Voltage (V)	−4.3	−4.29	−4.20	−4.05
I_{DS}-V_{GS} polynomial 1st-order coefficient (a_1)	−0.12585	0.80071	1.06891	0.36060
I_{DS}-V_{GS} polynomial 3rd-order coefficient (a_3)	−0.07354	0.19897	0.25904	0.06249
a_3/a_1	0.58435	0.24849	0.24234	0.17329
I_{DS}-V_{GS} polynomial 5th-order coefficient (a_5)	−0.00137	0.00226	0.00285	0.00023
a_5/a_1	0.01089	0.00282	0.00267	0.00064

For the device's RF linearity assessment, the OIP3 and IMD3 values could be evaluated using Equations (2) and (3) [18], where G_{ds} is the output conductance, and R_L is the load resistance. Since the transconductance characteristics determine the voltage gain of a HEMT device, the influence of the $G_m{''}$, which is the flatness of the G_m curve, on the IMD3 value and the influence of the G_m on the OIP3 will be the two main concerns in the following discussion [29].

$$P_{IMD3} \propto \frac{(G_m{''})^2}{{G_{ds}}^2 \cdot R_L} \tag{2}$$

$$\text{OIP3} \propto \frac{(G_m)^3}{G_m{''} \cdot {G_{ds}}^2 \cdot R_L} \tag{3}$$

Research has shown that the IMD3 levels of the devices could also be derived as in (4) [18], indicating that the lower a_3 and a_5 values could represent lower IMD3 levels.

$$P_{IMD3} = \frac{3}{8} a_3 A^3 + \frac{50}{32} a_5 A^5. \tag{4}$$

To evaluate the device's RF linearity, two-tone load-pull results were measured with a calibrated 30 GHz frequency signal using the Focus Load-Pull system with a frequency span of 10 MHz. A block diagram of the two-tone load-pull measurement setup with the signal generators, the spectrum analyzer, and the power supply is shown in Figure 4.

First-order intermodulation output power (IMD1) and IMD3 values were measured and OIP3 values were extrapolated using the fundamental power (F1) and third-order intermodulation power (2F1-F2) data curve with a slope of 1 and 3, respectively, at the linear region. The large signal results of different gate biases (0.5, 0.375, 0.25, and 0.125 I_{DSS}) were measured and are shown in Figures 5–8.

First, the 30 GHz large signal load-pull measurement results with the IMD3 value comparison results of the designed 4 × 50 µm AlGaN/GaN HEMT devices, biased at I_{DS} = 0.5 I_{DSS} and V_{DS} = 20 V, were analyzed and are shown in Figure 5. The linear gain improved from 7.38 dB to 8.12 dB, the IMD3 level at 16 dB back-off from P1dB (dBm) decreased from −54.82 dBm to −56.72 dBm, the Δ(OIP3-P1dB) value increased from 9.24 dB to 11.26 dB, and the OIP3 value increased from 33.97 dBm to 35.72 dBm. Furthermore, the 4 × 50 µm devices exhibited a maximum power density of more than 2.1 W/mm. The performance of the four different devices is listed in Table 2.

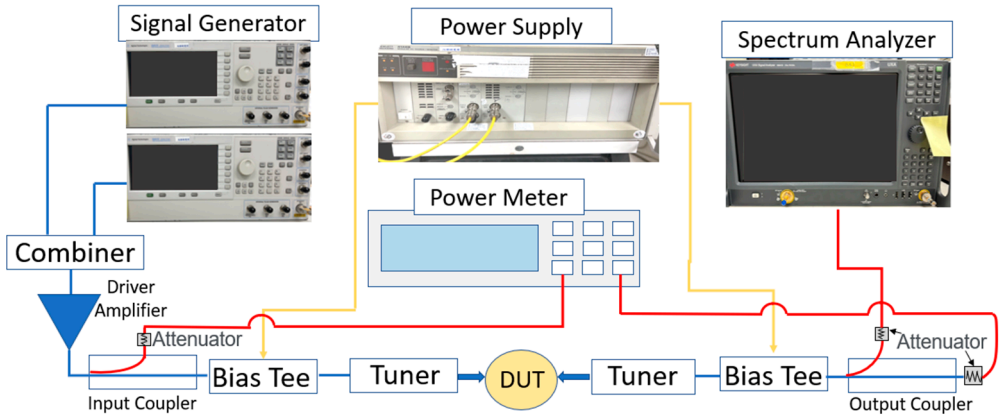
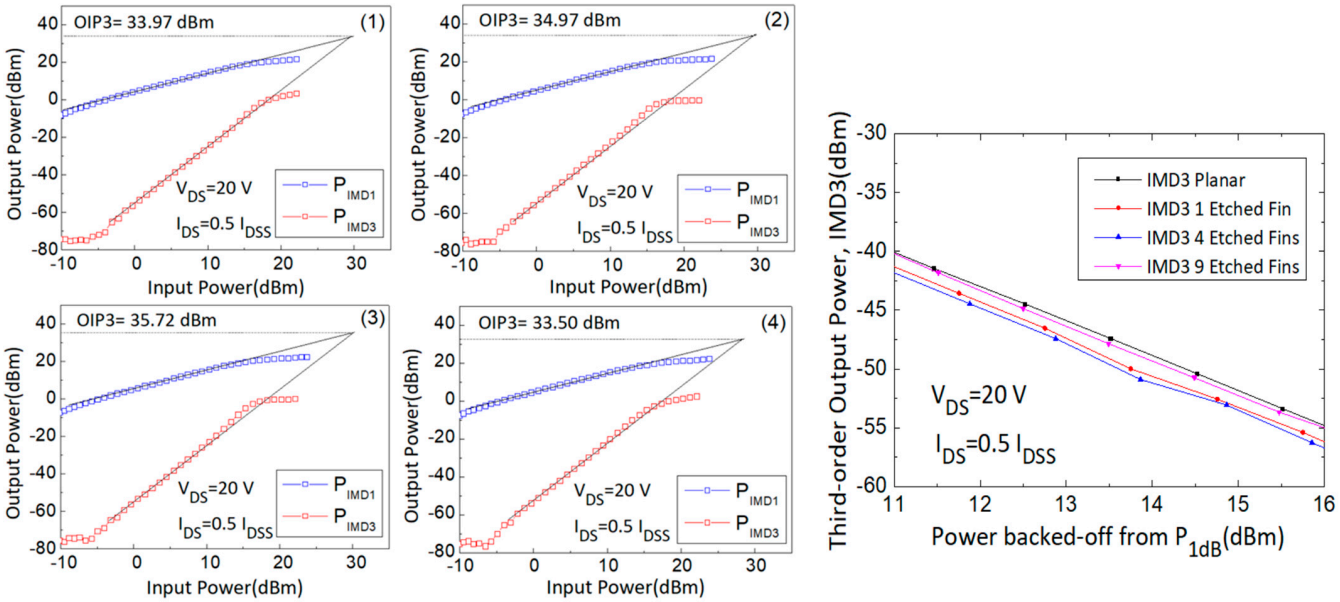


Figure 4. Block diagram of the 2-tone load-pull measurement setup.

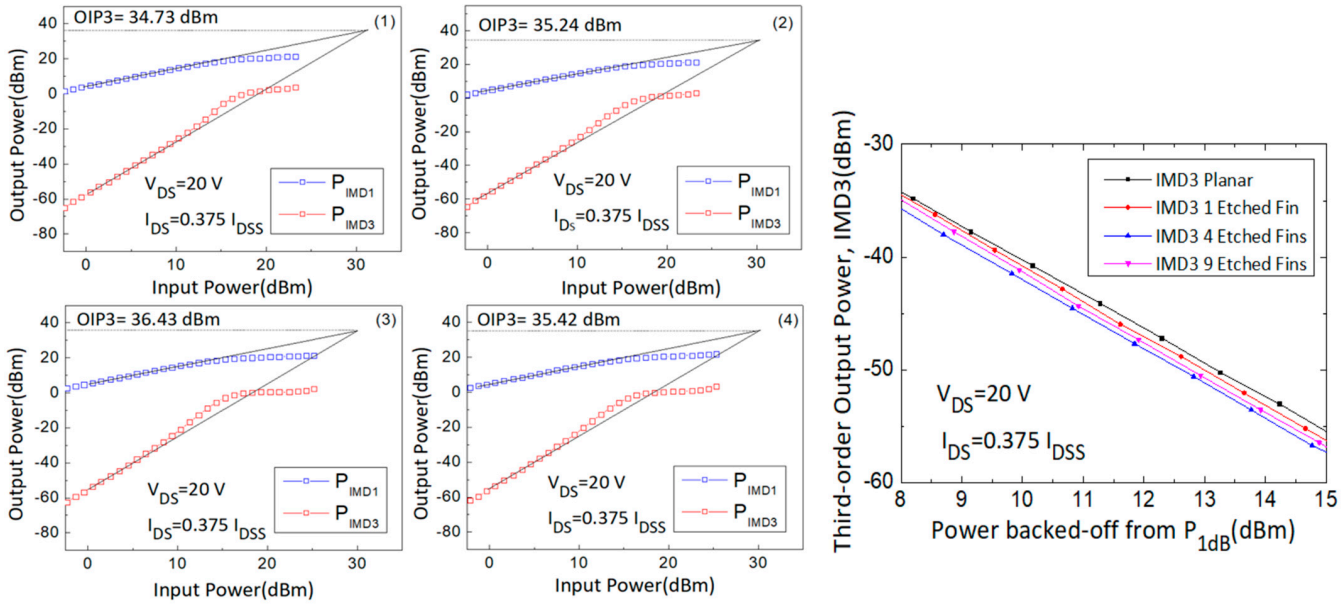


(**a**) (**b**)

Figure 5. (**a**) Measured output power versus input power curves with the (**1**) planar, (**2**) 1-etched-fin, (**3**) 4-etched-fin, and (**4**) 9-etched-fin gate structures at V_{DS} = 20 V and I_{DS} = 0.5 I_{DSS}, and (**b**) IMD3 versus power backed off from P_{1dB} curves of the AlGaN/GaN HEMTs on SiC substrate.

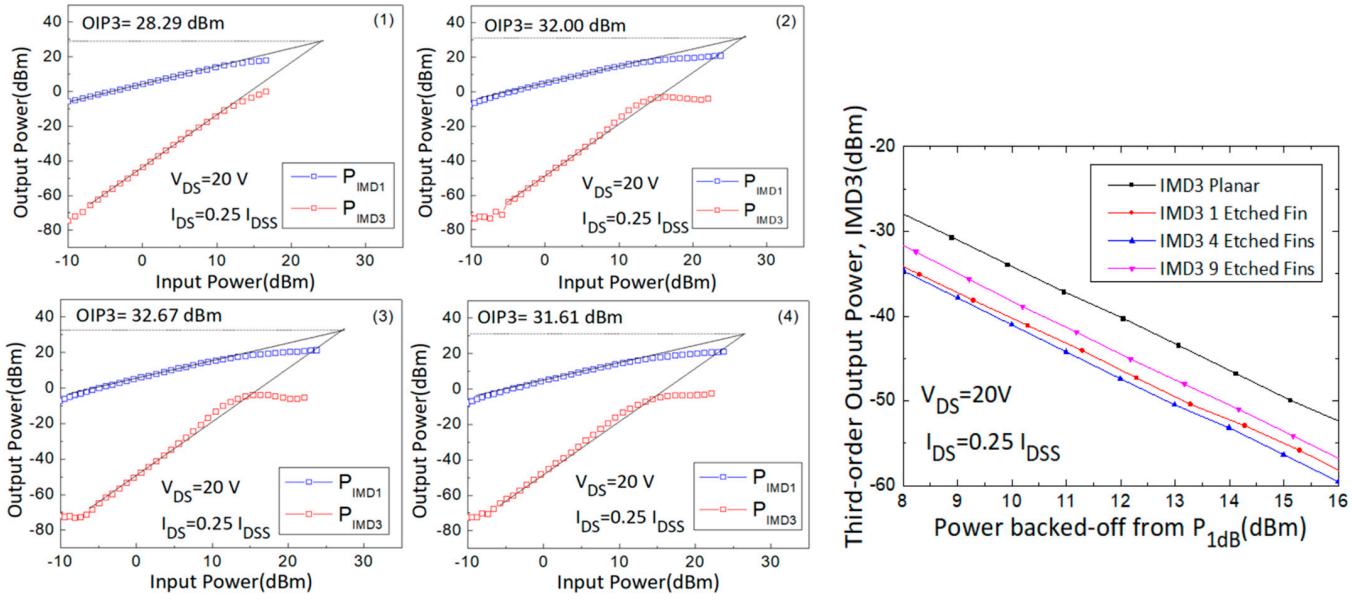
Second, the 30 GHz large signal load-pull measurement results with the IMD3 value comparison results of the 4 × 50 µm AlGaN/GaN HEMT devices, biased at I_{DS} = 0.375 I_{DSS} and V_{DS} = 20 V, were also analyzed and are shown in Figure 6. The linear gain improved from 7.49 dB to 8.38 dB, the IMD3 level at 15 dB back-off from P1dB (dBm) decreased from −55.49 dBm to −57.30 dBm, the Δ(OIP3-P1dB) value increased from 10.60 dB to 12.89 dB, and the OIP3 value increased from 34.73 dBm to 36.43 dBm. The performance of the four different devices is listed in Table 2.

Third, the 30 GHz large signal load-pull measurement results with the IMD3 value comparison results of the 4 × 50 µm AlGaN/GaN HEMT devices, biased at I_{DS} = 0.25 I_{DSS} and V_{DS} = 20 V, were also analyzed and are shown in Figure 7. The linear gain improved from 7.54 dB to 8.28 dB, the IMD3 level at 13 dB back-off from P1dB (dBm) decreased from −52.36 dBm to −59.54 dBm, the Δ(OIP3-P1dB) value increased from 6.73 dB to 11.22 dB, and the OIP3 value increased from 28.29 dBm to 32.67 dBm. The performance of the four different devices is listed in Table 2.



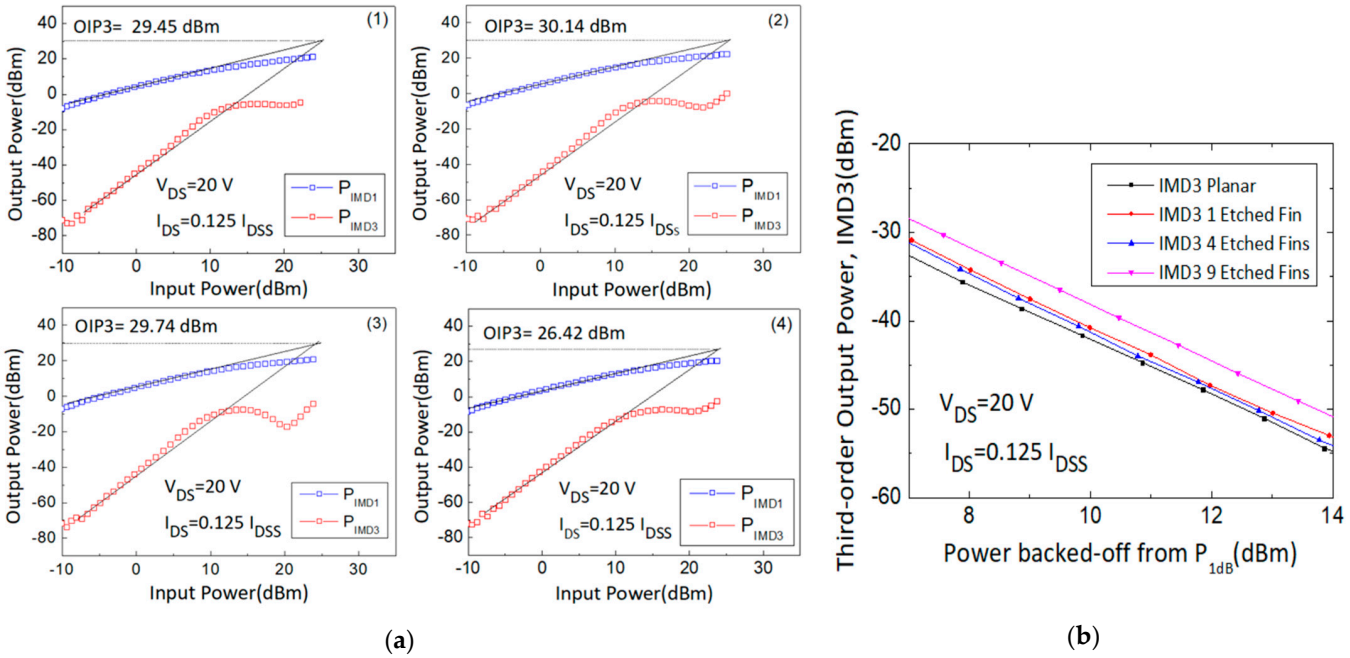
(**a**) (**b**)

Figure 6. (**a**) Measured output power versus input power curves with the (**1**) planar, (**2**) 1-etched-fin, (**3**) 4-etched-fin, and (**4**) 9-etched-fin gate structures at V_{DS} = 20 V and I_{DS} = 0.375 I_{DSS}, and (**b**) IMD3 versus power backed off from P_{1dB} curves of the AlGaN/GaN HEMTs on SiC substrate.



(**a**) (**b**)

Figure 7. (**a**) Measured output power versus input power curves with the (**1**) planar, (**2**) 1-etched-fin, (**3**) 4-etched-fin, and (**4**) 9-etched-fin gate structures at V_{DS} = 20 V and I_{DS} = 0.25 I_{DSS}, and (**b**) IMD3 versus power backed off from P_{1dB} curves of the AlGaN/GaN HEMTs on SiC substrate.



(**a**) (**b**)

Figure 8. (**a**) Measured output power versus input power curves with the (**1**) planar, (**2**) 1-etched-fin, (**3**) 4-etched-fin, and (**4**) 9-etched-fin gate structures at V_{DS} = 20 V and I_{DS} = 0.125 I_{DSS}, and (**b**) IMD3 versus power backed off from P_{1dB} curves of the AlGaN/GaN HEMTs on SiC substrate.

Table 2. Comparison of the RF characteristics of the four different types of devices with I_{DS} = 0.5, 0.375, 0.25, and 0.125 I_{DSS} at 30 GHz.

Device Type (4 × 50 μm)	DC Bias Point: V_{DS} = 20 V, Operation Frequency: 30 GHz						
	RF Bias	I_{DS} (mA)	PIMD3 Level at 16 dB Back-Off from P_{1dB} (dBm)	OIP3 (dBm)	P_{1dB} (dBm)	Δ(OIP3-P_{1dB}) (dB)	Gain (dB)
Planar	0.5 I_{DSS}	83.90	−54.82	33.97	24.73	9.24	7.38
1-Etched-Fin		83.00	−56.21	34.97	24.13	10.84	7.88
4-Etched-Fin		82.20	−56.72	35.72	24.46	11.26	8.12
9-Etched-Fin		80.30	−55.00	33.50	23.74	9.76	7.79
Planar	0.375 I_{DSS}	62.93	−55.49	34.73	24.13	10.60	7.49
1-Etched-Fin		62.25	−56.27	35.24	23.72	11.52	7.84
4-Etched-Fin		61.65	−57.30	36.43	23.54	12.89	8.38
9-Etched-Fin		60.23	−56.86	35.42	23.56	11.86	8.25
Planar	0.25 I_{DSS}	41.95	−52.36	28.29	21.56	6.73	7.54
1-Etched-Fin		41.50	−58.17	32.00	21.43	10.57	8.08
4-Etched-Fin		41.10	−59.54	32.67	21.45	11.22	8.28
9-Etched-Fin		40.15	−56.77	30.62	21.02	9.60	7.67
Planar	0.125 I_{DSS}	20.98	−54.73	29.45	18.36	11.09	7.39
1-Etched-Fin		20.75	−53.15	30.14	19.24	10.90	7.63
4-Etched-Fin		20.55	−54.11	29.74	18.76	10.98	7.84
9-Etched-Fin		20.08	−50.83	26.42	18.46	7.96	7.00

Fourth, the 30 GHz large signal load-pull measurement results with the IMD3 value comparison results of the 4 × 50 μm AlGaN/GaN HEMT devices, biased at I_{DS} = 0.125 I_{DSS} and V_{DS} = 20 V, were also analyzed and are shown in Figure 8. However, although the linear gain improved from 7.39 dB to 7.84 dB, the IMD3 level at 14 dB back-off from P1dB (dBm) increased from −54.73 dBm to −50.83 dBm, the Δ(OIP3-P1dB) value decreased from 11.09 dB to 7.96 dB, and the OIP3 value decreased from 29.45 dBm to 26.42 dBm. The contrasting trends of the results compared to the previous ones show the gate operation voltage limits of these devices. With the G_m curves shown in Figure 2, the G_m values of the four- and nine-etched-fin devices with I_{DS} = 0.125 I_{DSS} were too low for high-frequency operation, causing the relatively poor OIP3 and IMD3 performance. At I_{DS} = 0.125 I_{DSS}, the G_m curves of the four- and nine-etched-fin devices showed a larger slope, indicating a large increase in the G_m'', and resulting in a larger IMD3 value. The performance of the four different devices is listed in Table 2. The RF results correlate with the trends of the transfer characteristics, and from the measured results, the best operation gate biases were found to lie between 0.5 I_{DSS} and 0.25 I_{DSS} for these etched-fin HEMT devices.

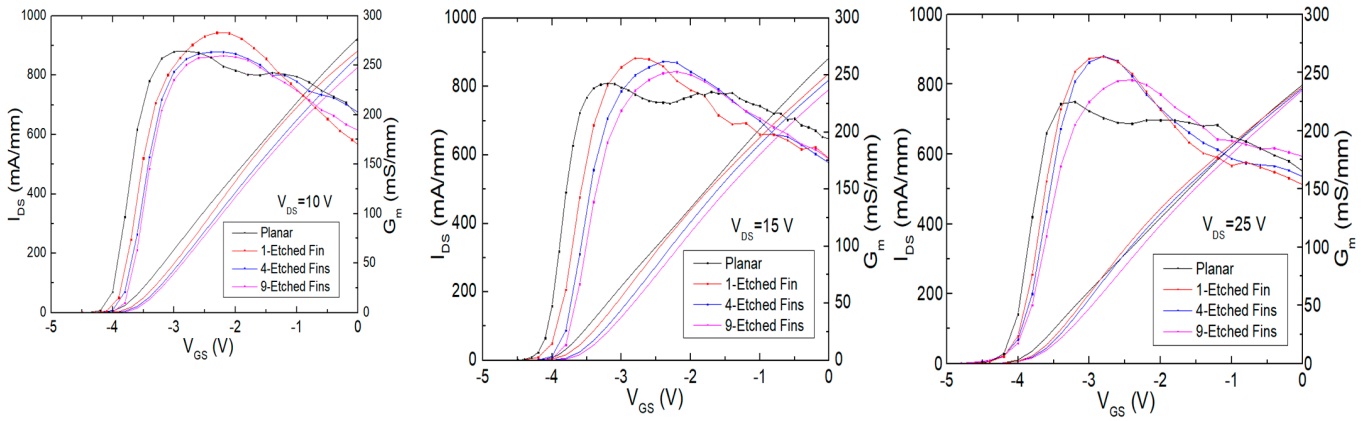
The performance of the four different devices is listed in Table 2, showing the comparison of the RF characteristics with I_{DS} = 0.5, 0.375, 0.25, and 0.125 I_{DSS} at 30 GHz.

From the observations above, the etched-fin device has been concluded to offer obvious improvements regarding the linearity performance compared to that of the planar device, owing to the enhanced gate controllability, represented by the transfer characteristics and right-shifted threshold voltage, which provide the etched-fin devices with a higher power gain under 30 GHz load-pull measurements and improved OIP3 and IMD3 values. However, the nine-etched-fin device has been observed to exhibit lower linearity compared to the four-etched-fin device and one-etched-fin device at specific gate biases. This may be due to the gate electric field effect between adjacent gate fins, and the increase in the C_{gs}. With limited numbers of etched fins, the gate controllability could be increased, but when the fin number continues to increase, the fields coming from the gate fins seem to interfere with one another, and this causes the gate controllability to degrade, lowering the G_m value and increasing the $|G_m''|$ value. Furthermore, the C_{gs} for nine etched fins is higher than in the four-etched-fin device, causing parasitic capacitance effects to deteriorate the device performance, such as the power gain and first and third output power at high-frequency Ka band operation.

To further investigate the buffer deep-etched-fin-gate electric field effect, the AlGaN/GaN HEMT linearity performance with different etched-fin gate structures has been analyzed by changing the drain bias to conduct different drain currents to the channel. The transfer characteristics of the four different devices with different etched-fin gate structures have been measured and two-tone load-pull measurement has been performed at 28 GHz with a frequency span of 10 MHz.

The transfer characteristics of the AlGaN/GaN HEMT devices with different etched-fin numbers, and measured at different drain voltages are shown in Figure 9a–c. At V_{DS} = 10 V, the one-etched-fin device has the highest G_m value, while the four- and nine-etched-fin devices have flatter G_m curves. The IMD3 shows an improvement with the etched-fin gate design, which is consistent with the transfer characteristic curves at the set operation gate bias for the load-pull measurement, as shown in Figures 9a and 10.

On the other hand, as the drain voltage rises to 15 V and 25 V, as shown in Figure 9b,c, the G_m value rises in the one- and four-etched-fin cases, but drops at nine etched fins, which shows that although the existing field effects coming from the gate fins act as a supporter to contribute to the control of the 2DEG channel, there may be a limitation to the number of etched fins, due to the shortened distances between the etched-fin gates, and the decrease in G_m may be due to the repelling of charges in the fins [26].



(**a**) (**b**) (**c**)

Figure 9. Measured transfer characteristic curves of the AlGaN/GaN HEMTs on SiC substrate with the planar, one-etched-fin, four-etched-fin, and nine-etched-fin gate structures at V_{DS} = (**a**) 10 V, (**b**) 15 V, and (**c**) 25 V.

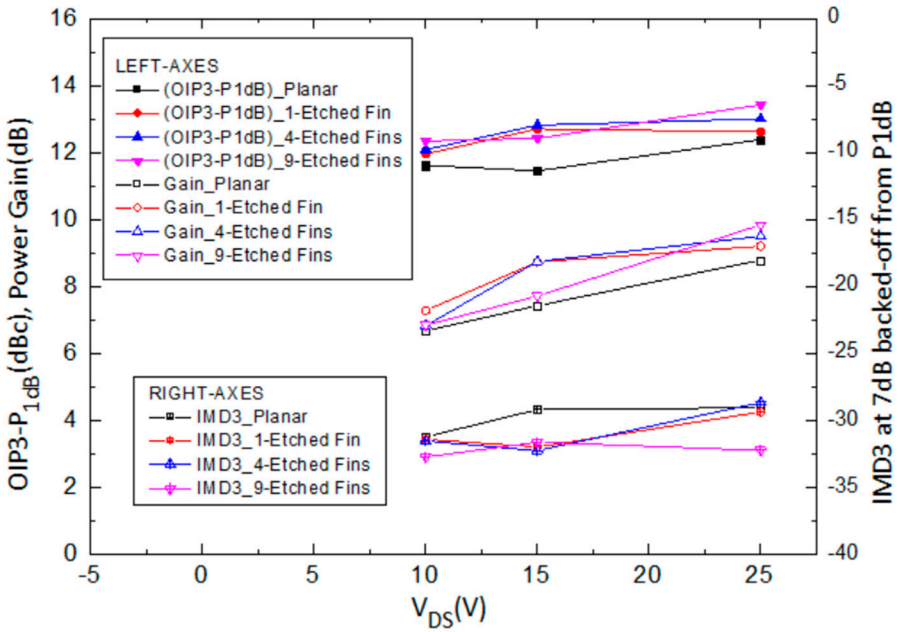
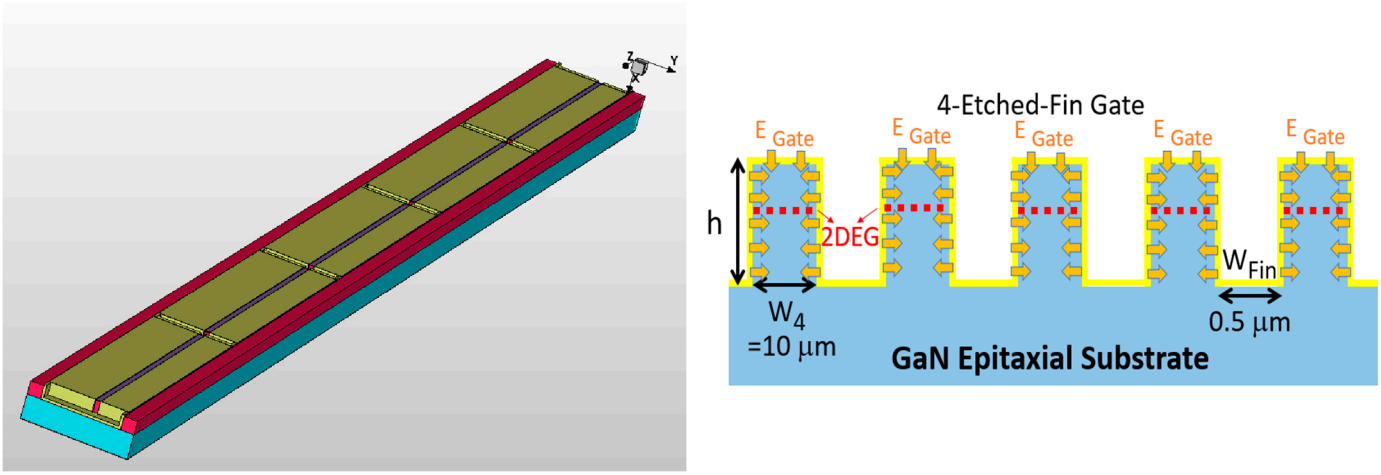


Figure 10. Measured and analyzed Δ(OIP3-P1dB), power gain, and IMD3 level at 7dB back-off from P_{1dB} at different drain biases of the AlGaN/GaN HEMTs on SiC substrate with the planar, 1-etched-fin, 4-etched-fin, and 9-etched-fin gate structures with I_{DS} = 0.25 I_{DSS}.

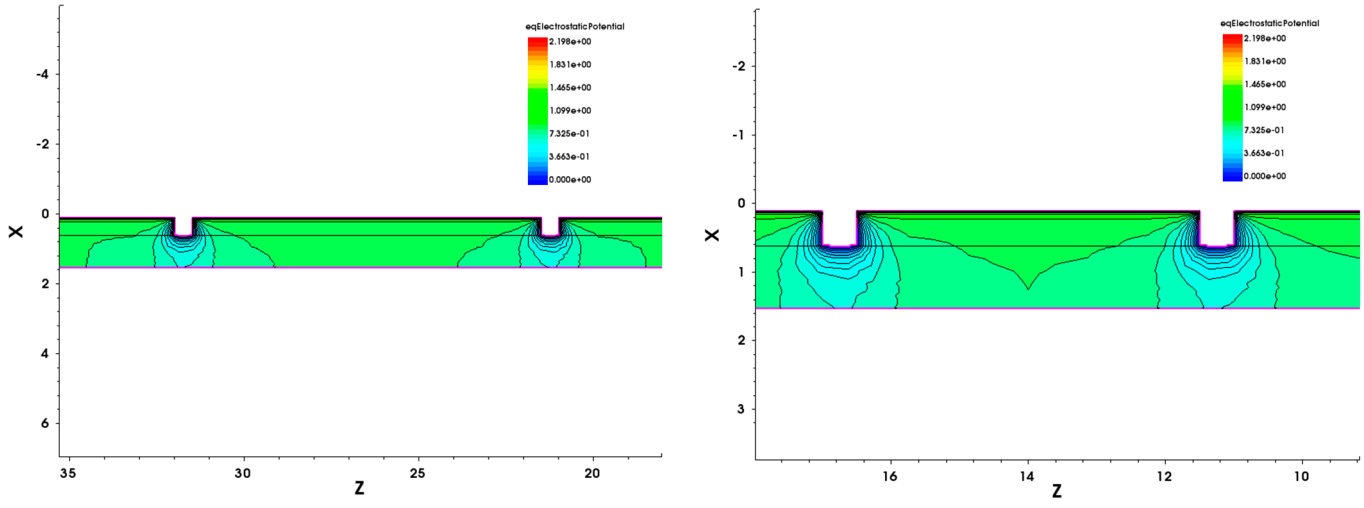
The observations from the transfer characteristics are consistent with those of the RF measurement results. Figure 10 shows the measured and analyzed (OIP3-P1dB), power gain, and IMD3 level at 7 dB back-off from P_{1dB} at different drain biases of the AlGaN/GaN HEMTs on a SiC substrate with the planar, one-etched-fin, four-etched-fin, and nine-etched-fin gate structures. The Δ(OIP3-P1dB) value, power gain value, and IMD3 value versus different drain voltages show that when the devices were operated under lower drain voltages—in this case, 10 V—the devices with four and nine etched fins do not demonstrate significant improvements in power gain and output power, which may be due to the increased gate voltage swing at smaller drain biases [30]. However, at higher drain voltages, the devices show improved performance with increased etched fin numbers, but they still show a limit, which is consistent with the trends shown in Figures 5–8.

The phenomenon concerning the effects of increased numbers of buffer deep fins has also been analyzed and discussed with the simulation results. The repelling of the electrostatic potential between closely packed gate fins has been modeled and visualized using the Sentaurus TCAD simulation tool. The four-etched-fin three-dimensional (3D) AlGaN/GaN HEMT model was built with a single-etched-fin gate design, as shown in Figure 11a. Figure 11b also shows the schematic diagram of a four-etched-fin device, with the height of the fin (h) and the width of the etched fin (W_{Fin}), and the partial width of the gate (W_n), with n equal to the number of etched fins. W_1 represents a 25 µm partial gate width, W_4 is 10 µm, and W_9 is 5 µm. The cross-sections of the fin gate with the equilibrium electrostatic potential distribution are shown in Figure 12a,b. The distances between the two gate fins in Figure 12a,b are 10 µm (W_4) and 5 µm (W_9), respectively. The *X*-axis represents the depth of the etched fin and the *Z*-axis moves along the gate width. The gate voltage is set to −3 V and the drain voltage is set to 20 V. The ranges for the equilibrium electrostatic potential are both set to 0 to 2.19752.



(**a**) (**b**)

Figure 11. (**a**) The 3D 4-etched-fin AlGaN/GaN HEMT model with a single gate and (**b**) schematic diagram of simulated gate electrostatic potential for the 4-etched-fin device.



(**a**) (**b**)

Figure 12. The 3D TCAD simulation results of the electrostatic potential distribution for the etched-fin GaN HEMT with (**a**) 4 etched fins and (**b**) 9 etched fins.

With the schematic diagram in Figure 11b, we can explain that the increase in G_m arises from the increase in the effective gate length ($L_{Gate,\ eff}$). The one-etched-fin device has a $L_{Gate,\ eff}$ of 4 × h + W_1, the four-etched-fin device has a $L_{Gate,\ eff}$ of 10 × h + W_4, and the nine-etched-fin device has a $L_{Gate,\ eff}$ of 20 × h + W_9. However, although the $L_{Gate,\ eff}$ of the etched-fin gate devices increases with increased etched fin numbers, the results from Figure 12 indicate that the electrostatic potentials between the fin gates of the nine-etched-fin device interact with one another more significantly than in the four-etched-fin device due to the short distances between the sidewall gate. It can be concluded that there exists a repelling of the electric fields from the gate sidewalls, which increases when the etched fins are set to be closer to each other—in this case, W_4 to W_9—thus degrading G_m.

4. Conclusions

AlGaN/GaN HEMTs on a SiC substrate with etched-fin gate structures were successfully fabricated and demonstrated good linearity improvements for Ka band applications. The device's DC and RF performance were improved due to the enhanced gate controllability over the gate width using an optimized etched-fin design. High power gains of more than 8 dB were obtained for the device when operated in a 30 GHz measurement environment. Etched-fin devices show better linearity performance at high frequencies than the planar device due to increased G_m values and lowered values of the second derivative of G_m. The four-etched-fin device, which had an optimized 10-µm separation between the etched fins, exhibited optimized linearity performance under a gate bias point of 0.5 I_{DSS}, 0.375 I_{DSS}, and 0.25 I_{DSS} among the planar, one-etched-fin, and nine-etched-fin devices at V_{DS} = 20 V. TCAD 3D device simulation results have also been provided to discuss the effect of increased etched fin numbers, which may degrade the gate controllability. Overall, the etched-fin devices demonstrate improved device linearity performance at the Ka band and show high potential for the advancement of wireless power amplifier systems.

Author Contributions: Conceptualization, M.-W.L. and Y.-C.L.; methodology, M.-W.L. and Y.-C.L.; software, F.G.; validation, Y.-C.L., F.G. and E.-Y.C.; formal analysis, M.-W.L.; investigation, M.-W.L.; resources, F.G., and E.-Y.C.; data curation, M.-W.L. and Y.-C.L.; writing—original draft preparation, M.-W.L.; writing—review and editing, Y.-C.L., H.-T.H., F.G. and E.-Y.C.; visualization, M.-W.L., Y.-C.L. and F.G.; supervision, F.G. and E.-Y.C.; project administration, Y.-C.L. and E.-Y.C.; funding acquisition, F.G. and E.-Y.C. All authors have read and agreed to the published version of the manuscript.

Funding: This work was financially supported by the "Center for the Semiconductor Technology Research" from the Featured Areas Research Center Program within the framework of the Higher Education Sprout Project by the Ministry of Education (MOE) in Taiwan. This work was also supported in part by the Ministry of Science and Technology, Taiwan, under Grants NSTC 111-2218-E-A49-021, NSTC 111-2634-F-A49-008, NSTC 111-2221-E-A49 -173 -MY3 and NSTC 112-2622-8-A49 -013 –SB.

Data Availability Statement: Data are contained within the article. The data presented in this study are available in [Study of AlGaN/GaN HEMTs on SiC Substrate with Etched-Fin Gate Structure to Improve Device Linearity for Ka Band Applications].

Acknowledgments: We acknowledge the Taiwan Semiconductor Research Institute (TSRI), Taiwan, for providing RF measurement support; the Laboratory of Nanoelectronics, Graphene, and 2D-Materials at CITIC-UGR, Spain, for TCAD simulation support; and the Compound Semiconductor Device Laboratory, Taiwan, for wafer fabrication and DC measurement support.

Conflicts of Interest: The authors declare no conflict of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript; or in the decision to publish the results.

References

1. del Alamo, J. Nanometre-scale electronics with III–V compound semiconductors. *Nature* **2011**, *479*, 317–323. [CrossRef] [PubMed]
2. del Alamo, J.A. The High-Electron Mobility Transistor at 30: Impressive Accomplishments and Exciting Prospects. In Proceedings of the 2011 International Conference on Compound Semiconductor Manufacturing Technology, Indian Wells, CA, USA, 16–19 May 2011.
3. Liu, A.-C.; Tu, P.-T.; Langpoklakpam, C.; Huang, Y.-W.; Chang, Y.-T.; Tzou, A.-J.; Hsu, L.-H.; Lin, C.-H.; Kuo, H.-C.; Chang, E.Y. The Evolution of Manufacturing Technology for GaN Electronic Devices. *Micromachines* **2021**, *12*, 737. [CrossRef] [PubMed]
4. O'Hara, J.F.; Ekin, S.; Choi, W.; Song, I. A Perspective on Terahertz Next-Generation Wireless Communications. *Technologies* **2019**, *7*, 43. [CrossRef]
5. Lin, Y.-C.; Yao, J.-N.; Hsu, H.-H.; Wong, Y.-C.; Huang, C.-Y.; Hsu, H.T.; Iwai, H.; Chang, E.Y. Study of the mesa etched tri-gate InAs HEMTs with extremely low SS for low-power logic applications. In Proceedings of the 2018 China Semiconductor Technology International Conference (CSTIC), Shanghai, China, 11–12 March 2018; pp. 1–3. [CrossRef]
6. Yao, J.-N.; Lin, Y.-C.; Hsu, H.-T.; Yang, K.-C.; Hsu, H.-H.; Sze, S.M.; Chang, E.Y. Evaluation of a 100-nm Gate Length E-Mode InAs High Electron Mobility Transistor With Ti/Pt/Au Ohmic Contacts and Mesa Sidewall Channel Etch for High-Speed and Low-Power Logic Applications. *IEEE J. Electron Devices Soc.* **2018**, *6*, 797–802. [CrossRef]
7. Yeon, S.-J.; Park, M.; Seo, K.-S. Novel sloped etch process for 15 nm InAlAs/InGaAs metamorphic HEMTs. In Proceedings of the 2007 7th IEEE Conference on Nanotechnology (IEEE NANO), Hong Kong, China, 2–5 August 2007; pp. 1152–1155. [CrossRef]
8. Medjdoub, F.; Zegaoui, M.; Grimbert, B.; Ducatteau, D.; Rolland, N.; Rolland, P.A. First Demonstration of High-Power GaN-on-Silicon Transistors at 40 GHz. *IEEE Electron Device Lett.* **2012**, *33*, 1168–1170. [CrossRef]
9. Palacios, T.; Chakraborty, A.; Rajan, S.; Poblenz, C.; Keller, S.; DenBaars, S.P.; Speck, J.S.; Mishra, U.K. High-power AlGaN/GaN HEMTs for Ka-band applications. *IEEE Electron Device Lett.* **2005**, *26*, 781–783. [CrossRef]
10. Lin, Y.C.; Huang, Y.X.; Huang, G.N.; Wu, C.H.; Yao, J.N.; Chu, C.M.; Chang, S.; Hsu, C.C.; Jin, H.L.; Kakushima, K. Enhancement-mode GaN MIS-HEMTs with LaHfOx gate insulator for power application. *IEEE Electron Device Lett.* **2017**, *38*, 1101–1104. [CrossRef]
11. Lin, Y.-C.; Chang, C.-H.; Li, F.-M.; Hsu, L.-H.; Chang, E.Y. Evaluation of TiN/Cu gate metal scheme for AlGaN/GaN high-electron-mobility transistor application. *Appl. Phys. Express* **2013**, *6*, 091003. [CrossRef]
12. Medjdoub, F.; Kabouche, R.; Dogmus, E.; Linge, A.; Zegaoui, M. High Electron Confinement under High Electric Field in RF GaN-on-Silicon HEMTs. *Electronics* **2016**, *5*, 12. [CrossRef]
13. Mishra, U.K.; Shen, L.; Kazior, T.E.; Wu, Y. GaN-Based RF Power Devices and Amplifiers. *Proc. IEEE* **2008**, *96*, 287–305. [CrossRef]
14. Mishra, U.K.; Parikh, P.; Wu, Y.-F. AlGaN/GaN HEMTs—An Overview of Device Operation and Applications. *Proc. IEEE* **2002**, *90*, 1022–1031. [CrossRef]
15. Rüdiger, Q.; Dirk, S.; Erdin, T.; Friedbert, R.; Christian, F.; Sebastian, K.; Müller, S.; Steffen, B.; Birte-Julia, G.; Peter, B. High-power microwave GaN/AlGaN HEMTs and MMICs on SiC and silicon substrates for modern radio communication. *Phys. Status Solidi* **2018**, *215*, 1700655. [CrossRef]
16. Xing, W.; Liu, Z.; Qiu, H.; Ranjan, K.; Gao, Y.; Ng, G.I.; Palacios, T. InAlN/GaN HEMTs on Si With High f_T of 250 GHz. *IEEE Electron Device Lett.* **2018**, *39*, 75–78. [CrossRef]
17. Martinez, R.P.; Munzer, D.J.; Zhou, X.Y.; Shankar, B.; Schmidt, E.-M.; Wildnauer, K.; Wu, B.; Murma, B. Best Practices to Quantify Linearity Performance of GaN HEMTs for Power Amplifier Applications. In Proceedings of the 2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Redondo Beach, CA, USA, 7–11 November 2021; pp. 85–89. [CrossRef]
18. Lin, Y.; Chang, E.Y.; Yamaguchi, H.; Wu, W.; Chang, C. A \delta\delta-Doped InGaP/InGaAs pHEMT With Different Doping Profiles for Device-Linearity Improvement. *IEEE Trans. Electron Devices* **2007**, *54*, 1617–1625. [CrossRef]
19. Lin, Y.C.; Chang, E.Y.; Yamaguchi, H.; Hirayama, Y.; Chang, X.Y.; Chang, C.Y. Device linearity comparison of uniformly doped and /spl delta/-doped In/sub 0.52/Al/sub 0.48/As/In/sub 0.6/Ga/sub 0.4/As metamorphic HEMTs. *IEEE Electron Device Lett.* **2006**, *27*, 535–537. [CrossRef]
20. Wang, H.-C.; Su, H.-F.; Luc, Q.-H.; Lee, C.-T.; Hsu, H.-T.; Chang, E.Y. Improved linearity in AlGaN/GaN HEMTs for millimeter-wave applications by using dual-gate fabrication. *ECS J. Solid State Sci. Technol.* **2017**, *6*, 3106–3109. [CrossRef]
21. Raj, A.; Krishna, A.; Hatui, N.; Romanczyk, B.; Wurm, C.; Guidry, M.; Hamwey, R.; Pakala, N.; Keller, S.; Mishra, U.K. GaN/AlGaN superlattice based E-mode p-channel MES-FinFET with regrown contacts and >50 mA/mm on-current. In Proceedings of the 2021 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA; 2021; pp. 5.4.1–5.4.4. [CrossRef]
22. Jo, Y.-W.; Son, D.-H.; Won, C.-H.; Im, K.-S.; Seo, J.H.; Kang, I.M.; Lee, J.-H. AlGaN/GaN FinFET With Extremely Broad Transconductance by Side-Wall Wet Etch. *IEEE Electron Device Lett.* **2015**, *36*, 1008–1010. [CrossRef]
23. Zhang, K.; Kong, Y.; Zhu, G.; Zhou, J.; Yu, X.; Kong, C.; Li, Z.; Chen, T. High-Linearity AlGaN/GaN FinFETs for Microwave Power Applications. *IEEE Electron Device Lett.* **2017**, *38*, 615–618. [CrossRef]
24. Wang, Z.; Cao, J.; Sun, R.; Wang, F.; Yao, Y. Numerical investigation on AlGaN/GaN short channel HEMT with AlGaN/InGaN/AlGaN quantum well plate. *Superlattices Microstruct.* **2018**, *120*, 753–758. [CrossRef]
25. Jessen, G.H.; Fitch, R.C.; Gillespie, J.K.; Via, G.; Crespo, A.; Langley, D.; Denninghoff, D.J.; Trejo, M. Short-Channel Effect Limitations on High-Frequency Operation of AlGaN/GaN HEMTs for T-Gate Devices. *IEEE Trans. Electron Devices* **2007**, *54*, 2589–2597. [CrossRef]

26. Yeh, W.-K.; Zhang, W.; Chen, P.-Y.; Yang, Y.-L. The Impact of Fin Number on Device Performance and Reliability for Multi-Fin Tri-Gate n- and p-Type FinFET. *IEEE Trans. Device Mater. Reliab.* **2018**, *18*, 555–560. [CrossRef]
27. Kim, D.-H.; del Alamo, J.A. 30-nm InAs Pseudomorphic HEMTs on an InP Substrate With a Current-Gain Cutoff Frequency of 628 GHz. *IEEE Electron Device Lett.* **2008**, *29*, 830–833. [CrossRef]
28. Chiu, H.-C.; Yang, S.-C.; Chien, F.-T.; Chan, Y.-J. Improved device linearity of AlGaAs/InGaAs HFETs by a second mesa etching. *IEEE Electron Device Lett.* **2002**, *23*, 1–3. [CrossRef]
29. Bailey, M.J. Intermodulation distortion in pseudomorphic HEMTs and an extension of the classical theory. *IEEE Trans. Microw. Theory Tech.* **2000**, *48*, 104–110. [CrossRef]
30. Nagahara, M.; Kikkawa, T.; Adachi, N.; Tateno, Y.; Kato, S.; Yokoyama, M.; Yokogawa, S.; Kimura, T.; Yamaguchi, Y.; Hara, N.; et al. Improved intermodulation distortion profile of AlGaN/GaN HEMT at high drain bias voltage. In Proceedings of the Digest. International Electron Devices Meeting, San Francisco, CA, USA, 8–11 December 2002; pp. 693–696. [CrossRef]

micromachines

Article

Improvement of AlGaN/GaN High-Electron-Mobility Transistor Radio Frequency Performance Using Ohmic Etching Patterns for Ka-Band Applications

Ming-Wen Lee [1,2], Cheng-Wei Chuang [1], Francisco Gamiz [2], Edward-Yi Chang [1,3] and Yueh-Chin Lin [1,*]

[1] International College of Semiconductor Technology, National Yang Ming Chiao Tung University (NYCU), Hsinchu City 30010, Taiwan; ericlmw.st06@nycu.edu.tw (M.-W.L.); kaszxc861229@gmail.com (C.-W.C.); edc@nycu.edu.tw (E.-Y.C.)
[2] Department of Electronics and Computer Technology, University of Granada, 18014 Granada, Spain; fgamiz@ugr.es
[3] Institute of Microengineering and Nanoelectronics, University Kebangsaan Malaysia, Bangi 43600, Malaysia
* Correspondence: nctulin@yahoo.com.tw; Tel.: +886-3-5712121

Abstract: In this paper, AlGaN/GaN high-electron-mobility transistors (HEMTs) with ohmic etching patterns (OEPs) "fabricated to improve device radio frequency (RF) performance for Ka-band applications" are reported. The fabricated AlGaN/GaN HEMTs with OEP structures were used to reduce the source and drain resistances (R_s and R_d) for RF performance improvements. Within the proposed study using 1 µm hole, 3 µm hole, 1 µm line, and 3 µm line OEP HEMTs with 2 × 25 µm gate widths, the small signal performance, large signal performance, and minimum noise figure (NF_{min}) with optimized values were measured for 1 µm line OEP HEMTs. The cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) value of the 1 µm line OEP device exhibited optimized values of 36.4 GHz and 158.29 GHz, respectively. The load–pull results show that the 1 µm line OEP HEMTs exhibited an optimized maximum output power density ($P_{out,\,max}$) of 1.94 W/mm at 28 GHz. The 1 µm line OEP HEMTs also exhibited an optimized NF_{min} of 1.75 dB at 28 GHz. The increase in the contact area between the ohmic metal and the AlGaN barrier layer was used to reduce the contact resistance of the OEP HEMTs, and the results show that the 1 µm line OEP HEMT could be fabricated, producing the best improvement in RF performance for Ka-band applications.

Keywords: aluminum gallium nitride; etching; HEMTs; large signal; noise figure; ohmic contacts; radio frequency; small signal

Citation: Lee, M.-W.; Chuang, C.-W.; Gamiz, F.; Chang, E.-Y.; Lin, Y.-C. Improvement of AlGaN/GaN High-Electron-Mobility Transistor Radio Frequency Performance Using Ohmic Etching Patterns for Ka-Band Applications. *Micromachines* **2024**, *15*, 81. https://doi.org/10.3390/mi15010081

Academic Editors: Ali Soltani and Aiqun Liu

Received: 30 November 2023
Revised: 25 December 2023
Accepted: 28 December 2023
Published: 30 December 2023

1. Introduction

With the growth of the Internet of Things (IoTs), artificial intelligence (AI), and the increasing demand for high-speed consumer electronics such as smart phones, smart homes, and unmanned aerial vehicles (UAV), lower-frequency system bandwidths for data transmission have become congested [1–4]. As a result, Ka-band systems have emerged in fifth-generation (5G) and beyond 5G (B5G) systems to increase spectrum allocations and data rates, and to reduce antenna sizes [5]. Power amplifiers (PAs) and low noise amplifiers (LNAs) in wireless communication circuits and their transistors are especially crucial when it comes to enhancing efficiency, gaining flatness, and lowering noise over a wide-frequency band [6]. Silicon-based transistors, such as complementary metal–oxide semiconductor field-effect transistors (CMOS FETs), can be used in radio frequency (RF) transceiver circuits given their low costs and high yield, but they suffer from low power gain, a short channel effect, and saturation effects due to scaling [7,8]. III–V-based transistors, such as AlGaAs/GaAs and AlGaN/GaN high-electron-mobility transistors (HEMTs), are also used in high-frequency PAs and LNAs, but GaAs-based HEMTs suffer from low

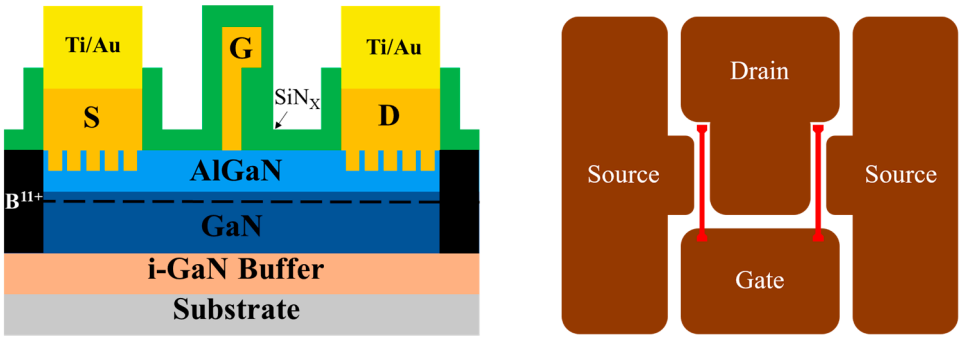
voltage operation, low power per unit, and low power efficiency due to the small energy bandgap and low breakdown voltage [9–11]. On the other hand, GaN-based HEMTs have demonstrated stronger frequency response, higher power-added efficiency (PAE), and better power performance, so are suitable for 5G and B5G systems, ranging from sub-6 GHz to Ka band, due to the high breakdown voltage, high saturation current, and low-frequency noise characteristics [12–17].

Nevertheless, parasitic resistance builds up at ultra-high frequencies for GaN HEMTs due to their high operation voltages, which reduces the overall device performance, such as current density, RF power, and PAE. Solutions have been proposed to reduce the parasitic influences of GaN-based HEMTs through barrier layer recessing, ohmic regrowth, and n-type doping to lower the source and drain resistances (R_s and R_d) for direct current (DC) characteristic improvements [18,19]. In advance, researchers have reported simulated and experimental results regarding contact resistivity improvements using several ohmic recessing patterns to increase the current paths and device saturation current density [20–27].

This study further compared the DC, RF small signal, RF large signal, and RF noise performance of different ohmic etching patterns (OEPs) for Ka-band applications and to design an optimized OEP structure with lower source and drain resistances, higher saturation current density, better RF power performance, and a lower high-frequency noise. The optimized OEP device with a 1 μm line pattern demonstrated the lowest contact resistance, highest small signal and large signal performance, and the smallest minimum noise figure (NF_{min}) at the Ka band among the four OEP structures designed in this study.

2. Materials and Methods

The AlGaN/GaN HEMTs were fabricated on a 4 inch GaN on SiC substrate. The epitaxial wafer was grown with a metal–organic chemical vapor deposition (MOCVD) system and consisted of an i-GaN buffer layer, a 0.9 μm unintentionally doped GaN channel layer, a 25 nm $Al_{0.25}Ga_{0.75}N$ barrier layer, and a 2 nm GaN cap layer, as shown in Figure 1a. The device structure consisted of two gate fingers (red), one gate pad, two source pads, and one drain pad, as shown in Figure 1b. The epitaxial wafer was measured via Hall measurement at room temperature and showed an electron mobility of 1500 $cm^2/V{\cdot}s$, a sheet resistance of 280 Ω/sq, and a sheet carrier density of $1 \times 10^{13}/cm^2$.



(**a**) (**b**)

Figure 1. Schematic graph of the OEP AlGaN/GaN HEMT with the (**a**) cross-section view and the (**b**) top view.

Alignment marks were fabricated first on the epitaxial wafer during the OEP process. Four different OEPs of 1 μm lines, 3 μm lines, 1 μm holes, and 3 μm holes, respectively, were then defined and transferred to the wafer by the stepper photolithography system (stepper) [12]. There are two shapes among the four OEPs, the line patterns and the hole patterns. The defined line patterns are parallel to the current flow and have widths of 1 μm or 3 μm, with lengths equal to the source and drain active area, and separations of 2 μm between the pattern edges. The defined hole patterns have diameters of 1 μm or 3 μm, for

the 1 µm holes and 3 µm holes, respectively, and the hole patterns are distributed uniformly over the source and drain active area with a 2 µm separation between the pattern edges. The optical micrographs of the developed OEP structures on the epitaxial wafer with 1 µm lines, 3 µm lines, 1 µm holes, and 3 µm holes are shown in Figure 2a,b,c,d, respectively. The schematic position of the OEP structures are shown in Figure 1a with the hole pattern rather than the line pattern for clarity.

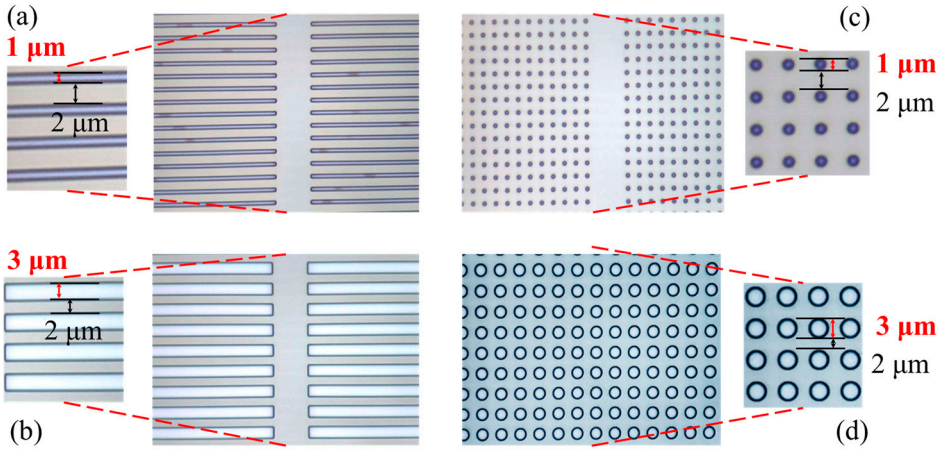


Figure 2. Optical microscope pictures of the developed OEPs with (**a**) 1 µm lines, (**b**) 3 µm lines, (**c**) 1 µm holes, and (**d**) 3 µm holes.

To form OEPs at the source and drain the ohmic contact area, the inductively coupled plasma-reactive ion etching (ICP-RIE) system is then used to dry etch the GaN cap layer and the AlGaN barrier layer with Cl_2/BCl_3 plasma. The OEPs were etched to around 10 nm above the 2-dimensional-electron-gas (2DEG) channel, which etch-stopped at the AlGaN barrier layer. The recessed depths were chosen only above 2DEG, due to the higher contact resistances measured for the devices with recessed depth below 2DEG, as shown in previous research [28]. After wafer cleaning with a diluted hydrochloric acid (HCl) solution to remove the native oxide layer [29], an ohmic metal stack of Ti/Al/Ni/Au was deposited with the e-beam evaporation system (E-gun) and annealed by the rapid thermal annealing system (RTA) at 850 °C for 30 s in N_2 ambient. The RTA process was followed by the B^{11+} ion implantation to define the active region of the devices. After the gate length (L_g) definition of 0.15 µm by the stepper using the 2-step photolithography process [12], the wafer was also uniformly dipped in a diluted HCl solution to remove native oxide layers before gate metal deposition [29]. Ni/Au was then deposited as the gate metal stack for Schottky contact formation and a 100 nm SiN_X passivation layer was deposited using the plasma enhanced chemical vapor deposition (PECVD) for moisture protection [30]. After via-opening of the SiN_X layer on the contact metal pads with the ICP system, thick metallization of a 2 µm Ti/Au metal stack was deposited using an E-gun after a wafer cleaning process using diluted HCl solution.

3. Results and Discussion

3.1. DC Characteristics

Transmission line modeling (TLM) was used in this study to determine the specific contact resistivity (ρ_c) and the contact resistance (R_c) of the epitaxial wafer with the four designed OEP structures and the results are shown in Table 1 [25,26].

Table 1. Contact resistivity and contact resistance results of different OEP structures obtained with the TLM method.

Ohmic Etching Patterns	ρ_c (Ω·cm^2)	R_c (Ω·mm)
1 μm line	4.04×10^{-7}	0.154
3 μm line	7.80×10^{-7}	0.212
1 μm hole	6.01×10^{-7}	0.191
3 μm hole	7.68×10^{-7}	0.199
w/o OEPs	2.73×10^{-6}	0.429

The ρ_c has been improved from 2.73×10^{-6} Ω·cm^2 to 4.04×10^{-7} Ω·cm^2 and the R_c has been improved from 0.429 Ω·mm to 0.154 Ω·mm applying the 1 μm line OEP structure, which is the lowest value among the fabricated TLM structures with the four designed OEPs.

AlGaN/GaN HEMTs with the four designed OEPs were also fabricated on the same epitaxial wafer. The $I_{DS}-V_{GS}$ and G_m-V_{GS} curves for the four fabricated OEP AlGaN/GaN HEMTs are shown in Figure 3. The gate width and source-to-drain spacing (L_{SD}) for the OEP GaN HEMTs are 2 × 25 μm and 2 μm, respectively. The gate-to-drain spacing (L_{GD}) of 1.25 μm, and a gate-to-source spacing (L_{GS}) of 0.6 μm were designed for the devices. The peak extrinsic transconductance ($G_{m,\,peak}$) of 403 mS/mm and the drain-to-source saturation current (I_{DSS}) of 999 mA/mm were measured from the OEP GaN HEMT with the 1 μm line patterns at V_{DS} = 10 V, which both demonstrated the highest value among the four OEP HEMTs, as shown in Table 2. The I_{DSS} is defined as the drain-to-source current (I_{DS}) when the gate-to-source voltage (V_{GS}) equals zero and the $G_{m,\,peak}$ is defined as the peak extrinsic transconductance value of the device with a V_{GS} swept from −4 V to 0 V.

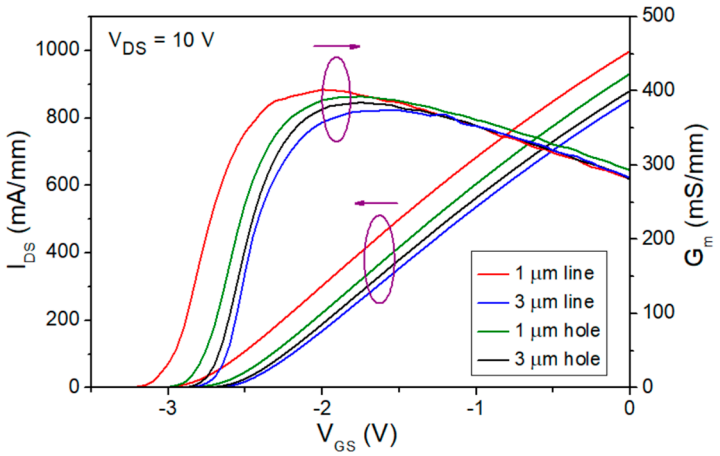


Figure 3. $I_{DS}-V_{GS}$ and G_m-V_{GS} curves for the 2 × 25 μm AlGaN/GaN HEMTs with different OEPs. (Left arrow: $I_{DS;}$ Right arrow: G_m).

Table 2. R_{on}, $G_{m,\,peak}$, I_{DSS}, minimum noise figure at 28 GHz, and associated gain at 28 GHz of the 2 × 25 μm AlGaN/GaN HEMT devices with different OEP structures.

Ohmic Etching Patterns	R_{on} (Ω·mm)	$G_{m,\,peak}$ (mS/mm)	I_{DSS} (mA/mm)	NF_{min} at 28 GHz (dB)	Gain at 28 GHz (dB)
1 μm line	1.61	403	999	1.75	5.98
3 μm line	2.24	374	855	2.00	6.14
1 μm hole	1.63	393	932	1.85	5.80
3 μm hole	1.81	385	880	1.87	6.09

The $I_{DS}-V_{DS}$ curves of the four OEP HEMTs with V_{GS} equals to 0 V and V_{DS} sweeping from 0 V to 5 V and their on-resistance (R_{on}) values were also measured and calculated,

respectively, as shown in Figure 4 and Table 2. The HEMT devices with the 1 µm line OEP structure has the R_{on} of 1.61 Ω·mm, which shows the lowest R_{on} among the four designed OEP HEMTs.

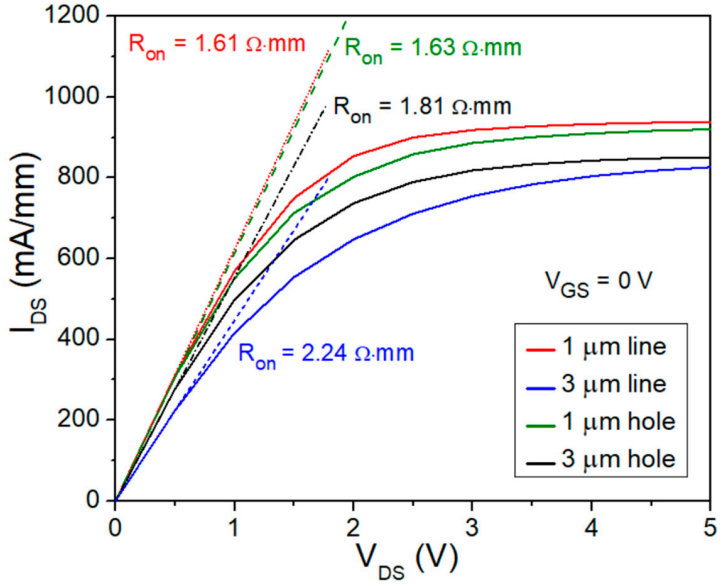


Figure 4. R_{on} and I_{DS}–V_{DS} curves for the four 2 × 25 µm AlGaN/GaN OEP HEMTs.

The measured DC characteristics of the four OEP HEMTs shown in Figure 3, Figure 4, Table 1, and Table 2 exhibit improvements in the device performance. The improvement of ρ_c from 2.73 × 10^{-6} Ω·cm^2 to 4.04 × 10^{-7} Ω·cm^2 and the improvement of R_c from 0.429 Ω·mm to 0.154 Ω·mm using the 1 µm line OEP structure is attributed to the increase of contact area at the interface between the ohmic metal stack and the semiconductor layer, forming more TiN_X layers and nitride vacancies, the inclusion of fringing effects, and the removal of irregular surface oxide layers [20,23,31]. Moreover, the increase in electron tunneling effect at the interface under the ohmic metal stack also stands a crucial role in the improvement of the ρ_c and R_c values and could be explained by the increase in N vacancies, increasing donor doping concentration and electric field, and thus increasing tunneling current [23]. A benchmark has been made to compare the lowest R_c in this work with well-known publications that also fabricated OEP GaN-based HEMTs, demonstrating the low R_c of the designed OEP HEMT in this study, as shown in Figure 5.

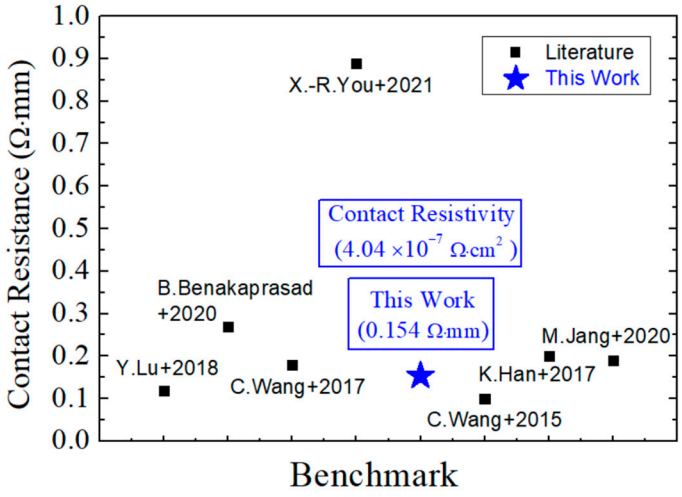


Figure 5. Benchmark of the lowest contact resistance in this study with published literature [20–23,25–27].

The trend of the $G_{m,\,peak}$ and I_{DSS} are also analyzed for the four OEP HEMTs, showing that 1 µm line OEP HEMTs exhibit the highest values among the four designed structures, followed by the OEP HEMTs with the 1 µm holes, the 3 µm holes, and the 3 µm lines, in descending sequence. This is attributed to the larger contact area at the interface of the 1 µm line OEP HEMTs and that the 1 µm line OEP HEMTs still obtain enough AlGaN barrier layer to form enough 2DEG. R_{on} values of the four designed OEP HEMTs were also analyzed and demonstrated a similar trend to that of the I_{DSS} value. The trend of the R_{on} improvement for OEP HEMTs compared to non-OEP HEMTs was also found in previous research [32].

3.2. RF Characteristics

3.2.1. Small Signal Performance

All the designed AlGaN/GaN OEP devices were measured with a E8361C PNA network analyzer and a 4142B DC supplier to obtain the S parameter results for small signal performance analysis. The small-signal equivalent circuit model for the OEP AlGaN/GaN HEMTs was used, as shown in Figure 6. The small signal impedance matching system was calibrated with a short-open-load-thru (SOLT) calibration with an accuracy of less than ±0.01 dB for both the S21 and S12 values and less than −45 dB for both the S11 and S22 values within the measured frequency range [33]. The measured S parameters were first de-embedded and the current gain (H21), maximum stable power gain (MSG), and maximum available gain (MAG) were calculated using the Microwave Office 2000 software. After extrapolating the H21 (dB) to frequency (log scale) curves and MSG/MAG to frequency (log scale) curves with the slope of −20 dB/decade, the cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) values of the OEP devices were obtained, as shown in Figure 7a,b.

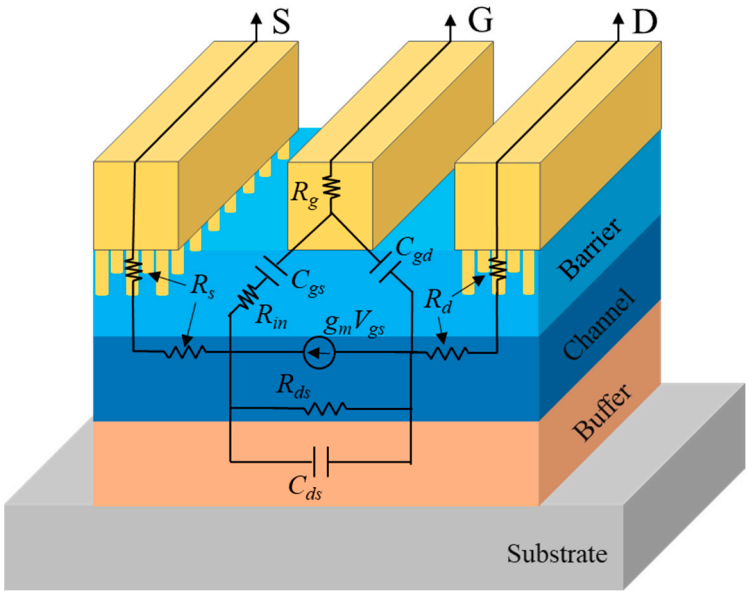


Figure 6. Small-signal equivalent circuit model for the AlGaN/GaN HEMTs with the hole OEPs.

The de-embedded f_T values of the designed 1 µm line, 3 µm line, 1 µm hole, and 3 µm hole OEP HEMTs are 36.40 GHz, 30.90 GHz, 33.10 GHz, and 32.60 GHz, respectively, as shown in Table 3. The de-embedded f_{max} values of the designed 1 µm line, 3 µm line, 1 µm hole, and 3 µm hole OEP HEMTs are 158.29 GHz, 145.50 GHz, 150.05 GHz, and 146.80 GHz, respectively, as shown in Table 3. Among the four designed OEP HEMTs with the gate width of 2 × 25 µm, the f_T and f_{max} value of the 1 µm line OEP device exhibit the largest value of 36.4 GHz and 158.29 GHz, respectively.

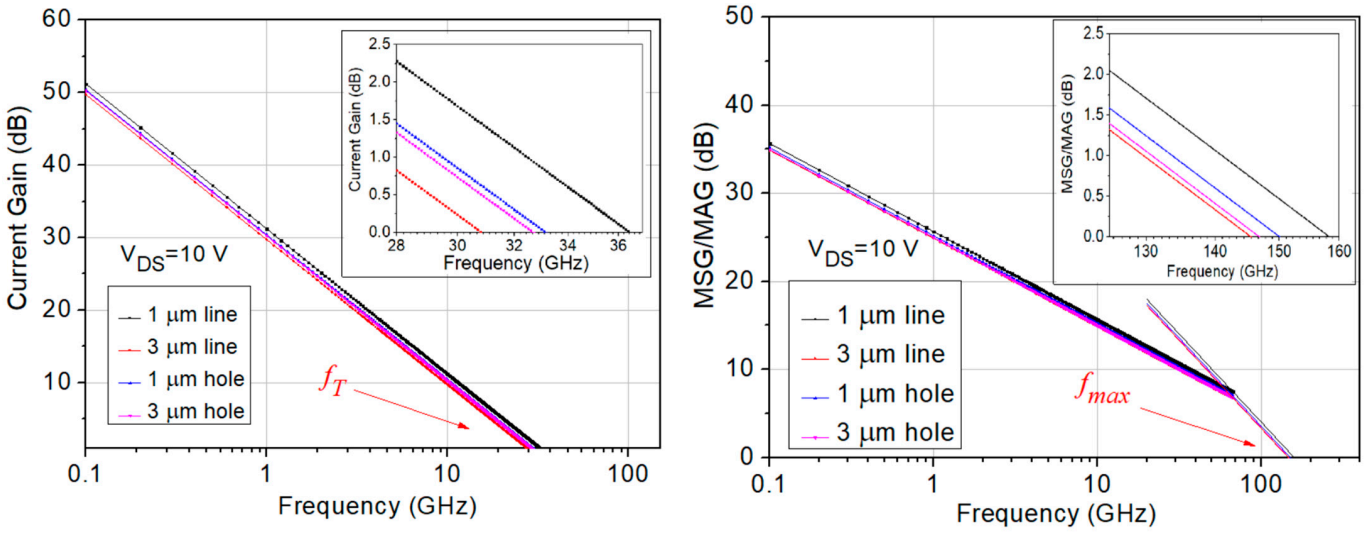


Figure 7. (**a**) Current gain to frequency plot and (**b**) MSG/MAG to frequency plot for the 2 × 25 µm OEP AlGaN/GaN HEMTs.

Table 3. f_T, f_{max}, and extracted small signal parameters of the 2 × 25 µm AlGaN/GaN HEMT devices with different OEP structures.

Ohmic Etching Patterns	f_T (GHz)	f_{max} (GHz)	R_s (Ω)	R_d (Ω)	C_{gs} (fF)	C_{gd} (fF)
1 µm line	36.40	158.29	4.35	2.73	91.03	9.76
3 µm line	30.90	145.50	5.04	3.43	94.84	10.82
1 µm hole	33.10	150.05	4.53	2.81	91.30	10.15
3 µm hole	32.60	146.80	4.75	2.93	93.42	10.56

The parasitic source resistance (R_s), parasitic drain resistance (R_d), parasitic gate-to-source capacitance (C_{gs}), and parasitic gate-to-drain capacitance (C_{gd}) of the four designed OEP HEMTs were also extracted from the S parameter results, as shown in Table 3. The 1 µm line OEP device exhibit the lowest R_s, R_d, C_{gs}, and C_{gd} of 4.35 Ω, 2.73 Ω, 91.03 fF, and 9.76 fF, respectively, among the four designed OEP HEMTs. The small signal results show that the 1 µm line OEP HEMTs exhibit the best small signal performance among the four designed structures, followed by the OEP HEMTs with the 1 µm holes, the 3 µm holes, and the 3 µm lines, in descending sequence.

The measured small signal characteristics of the four OEP HEMTs are shown in Figure 7 and Table 3. The results show that the 1 µm line OEP HEMT exhibited the highest f_T and f_{max} among other OEP HEMTs, which could be attrbuted to the reduction in parasitic resistances and parasitic capacitances. The equations showing the correlation between f_T, f_{max}, and the extracted parameters of R_s, R_d, C_{gs}, and C_{gd} are shown below in Equations (1) and (2) [34].

$$f_T = \frac{g_m}{2\pi\left(C_{gs}+C_{gd}\right)\left[1+(R_s+R_d)g_o\right]+g_m C_{gd}(R_s+R_d)} \quad (1)$$

$$f_{max} = \frac{f_T}{2\sqrt{g_o\left(R_g+R_i+R_s\right)+2\pi f_T R_g C_{gd}}} \quad (2)$$

Equations (1) and (2) show that the f_T and f_{max} value are inversely proportional to the parasitic components of R_s, R_d, C_{gs}, and C_{gd}.

The R_s, R_d, C_{gs}, and C_{gd} values of the four designed OEP HEMTs were analyzed and a similar ascending trend was found. The lowest parasitic values among the four designed structures were extracted from the 1 µm line OEP HEMTs, followed by the OEP HEMTs with the 1 µm holes, the 3 µm holes, and the 3 µm lines, in ascending sequence. This correlates to the trend of the f_T and f_{max} value measured from the four designed OEP HEMTs. The extracted C_{gs} and C_{gd} values of both the 3 µm hole and 3 µm line OEP HEMT are larger than the extracted C_{gs} and C_{gd} values of both the 1 µm hole and 1 µm line OEP HEMT, which shows that the increment in the size of the patterns from 1 µm to 3 µm increases the C_{gs} and C_{gd} values. The extracted C_{gs} and C_{gd} values of the hole OEP HEMTs also show larger values than the line OEP HEMTs, which is due to the increased separated ohmic metal arrays formed by the hole patterns. The increase in the contact area between the ohmic metal and the AlGaN barrier layer were used to reduce the contact resistance of the OEP HEMTs, and the results show that the 1 µm line OEP HEMT could be fabricated with the best improvement in small signal performance at the Ka band.

3.2.2. Large Signal Performance

Load–pull measurements at 28 GHz operation frequency for RF power and PAE analysis were also conducted for the four designed OEP devices with a gate width of 2 × 25 µm. The power sweep curves of the load–pull measurement with input power set from −7.5 dBm to 20 dBm for the four designed OEP device structures with 1 µm lines, 3 µm lines, 1 µm holes, and 3 µm holes are shown in Figure 8a,b,c,d, respectively.

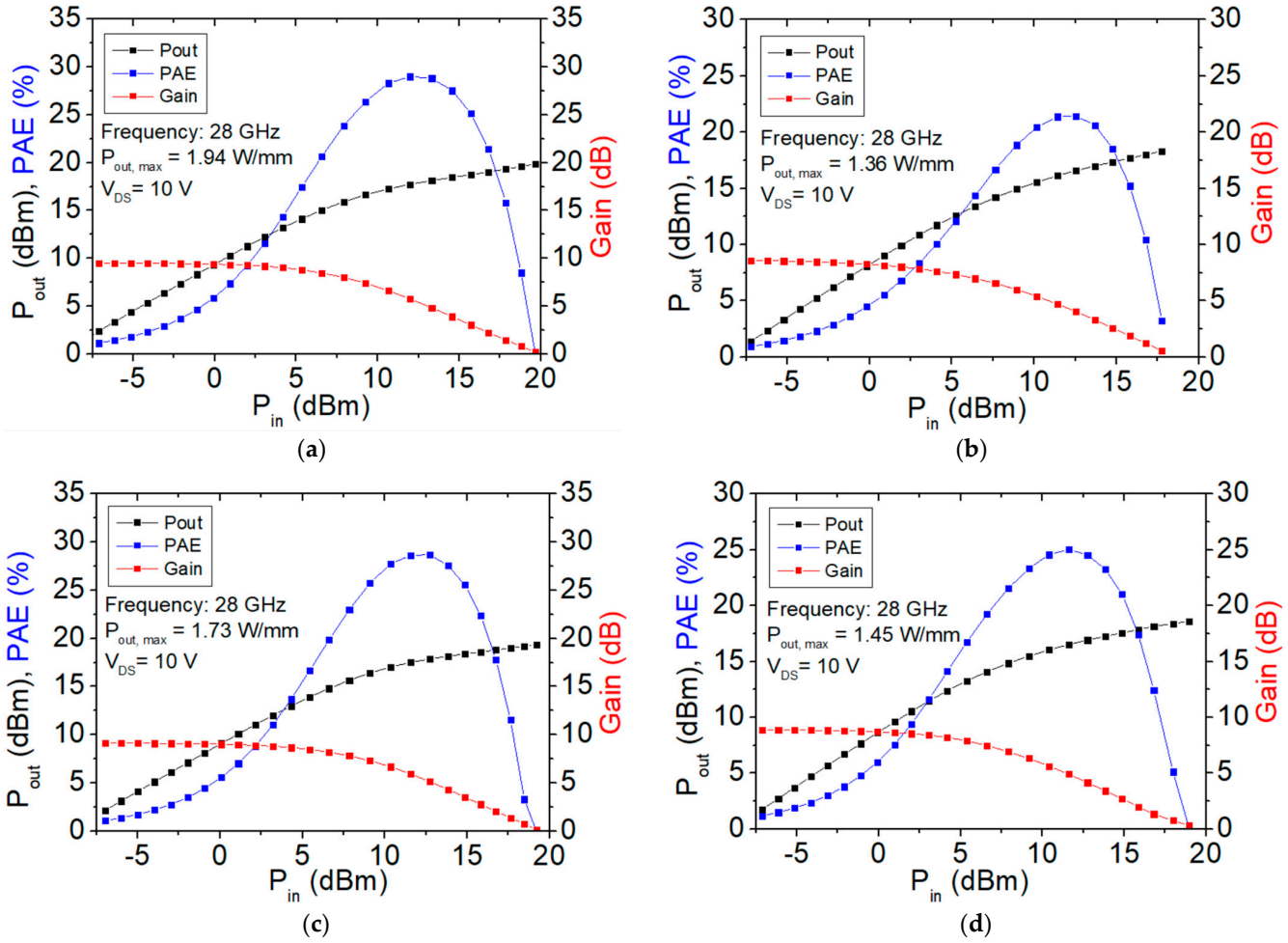


Figure 8. Load–pull curves at 28 GHz operation frequency for the 2 × 25 µm OEP AlGaN/GaN HEMTs with (**a**) 1 µm lines, (**b**) 3 µm lines, (**c**) 1 µm holes, and (**d**) 3 µm holes.

The peak PAE, the power gain, and the maximum output power density ($P_{out,\,max}$) in units of dBm and W/mm of the four OEP HEMTs are shown in Table 4. The peak PAE of the 1 µm line, 3 µm line, 1 µm hole, and 3 µm hole HEMTs are 29.01%, 21.44%, 28.70%, and 25.03%, respectively. The power gain of the 1 µm line, 3 µm line, 1 µm hole, and 3 µm hole HEMTs are 9.52 dB, 8.60 dB, 9.12 dB, and 8.87 dB, respectively. The $P_{out,\,max}$ (dBm) of the 1 µm line, 3 µm line, 1 µm hole, and 3 µm hole HEMTs are 19.86 dBm, 18.31 dBm, 19.36 dBm, and 18.60 dBm, respectively. The $P_{out,\,max}$ (W/mm) of the 1 µm line, 3 µm line, 1 µm hole, and 3 µm hole HEMTs are 1.94 W/mm, 1.36 W/mm, 1.73 W/mm, and 1.45 W/mm, respectively. The load–pull results show that the 1 µm line OEP HEMTs exhibit the best large signal performance among the four designed structures, followed by the OEP HEMTs with the 1 µm holes, the 3 µm holes, and the 3 µm lines, in descending sequence.

Table 4. RF large signal load-pull measurement results of the 2 × 25 µm AlGaN/GaN HEMT devices with different OEP structures.

Ohmic Etching Patterns	PAE Peak (%)	Gain (dB)	$P_{out,\,max}$ (dBm)	$P_{out,\,max}$ (W/mm)
1 µm line	29.01	9.52	19.86	1.94
3 µm line	21.44	8.60	18.31	1.36
1 µm hole	28.70	9.12	19.36	1.73
3 µm hole	25.03	8.87	18.60	1.45

The measured large signal characteristics of the four OEP HEMTs are shown in Figure 8 and Table 4. The 1 µm line OEP HEMTs exhibit the largest gain, PAE, and $P_{out,\,max}$ among the four designed OEP HEMTs, followed by the OEP HEMTs with the 1 µm holes, the 3 µm holes, and the 3 µm lines, in descending sequence. The descending trend obtained from the large signal performance shown in Table 4 matches that of the DC characteristics and the small signal performances shown in Tables 2 and 3, respectively. This could be due to the good thermal dissipation from the SiC substrate and low surface trapping of the OEP HEMTs with well deposited passivation layer [35]. The increase in the contact area between the ohmic metal and the AlGaN barrier layer was used to reduce the contact resistance and increase the saturation current of the OEP HEMTs, and the results show that the 1 µm line OEP HEMT could be fabricated with the best improvement in large signal performance at the Ka band.

3.2.3. Noise Figure

The noise figure measurement at the Ka band was carried out for all four OEP devices with a gate width of 2 × 25 µm. The frequency sweep for the noise figure measurement was set from 18 GHz to 41 GHz. The gain to NF_{min} graphs of the line-etched and hole-etched devices are shown in Figure 9a,b, respectively. At 28 GHz, NF_{min} of 1.75 dB with an associated gain of 5.98 dB and NF_{min} of 2.00 dB with an associated gain of 6.14 dB were measured for the 1 µm line and 3 µm line OEP devices, respectively, as shown in Figure 9a and Table 2. At 28 GHz, NF_{min} of 1.85 dB with an associated gain of 5.80 dB and NF_{min} of 1.87 dB with an associated gain of 6.09 dB were measured for the 1 µm hole and 3 µm hole OEP devices, respectively, as shown in Figure 9b and Table 2. The results show that the OEP devices etched with 1 µm lines exhibit the lowest NF_{min} among the fabricated devices with comparable associated gain.

The measured noise figure characteristics of the four OEP HEMTs are shown in Figure 9 and Table 2. The 1 µm line OEP HEMTs exhibit the smallest NF_{min} among the four designed OEP HEMTs at 28 GHz, followed by the OEP HEMTs with the 1 µm holes, the 3 µm holes, and the 3 µm lines, in ascending sequence. The lowered NF_{min} is due to the reduction of access resistance achieved from the thinned barrier layer at the ohmic patterns and the increased contact area at the ohmic metal and semiconductor interface, which reduce R_s and R_d [19]. However, larger areas of the etched-away barrier layers in the 3 µm line OEP

devices cause larger depletion of the 2DEG and reduction in I_{DS}, which further increase R_s and R_d [20]. The increased R_s and R_d in the 3 µm line OEP devices may also be the reason for the higher NF_{min}, as shown in Equation (3). On the other hand, the parasitic C_{gs} of the HEMT devices also plays an important role in determining the device NF_{min} during high frequency noise figure measurement, as shown in Equation (3) [36]. The parasitic C_{gs} values of the four designed OEP HEMTs are extracted, as shown in Table 3, and show a similar ascending trend to that of the ascending trend found in the measured NF_{min} values of the four designed OEP HEMTs, as shown in Table 2.

$$NF_{min} = 1 + 2\pi f K_f C_{gs} \sqrt{\frac{(R_g + R_s)}{g_m}} \quad (3)$$

The increase in the contact area between the ohmic metal and the AlGaN barrier layer was used to reduce the R_s and R_d of the OEP HEMTs, and the results show that the 1 µm line OEP HEMT could be fabricated with the best improvement in noise figure performance at the Ka band.

Further analysis comparing the device performance of GaN HEMTs with and without the 1 µm OEP structure could be pursued as future work. This analysis might involve exploring various ohmic etching depths to optimize contact resistivity.

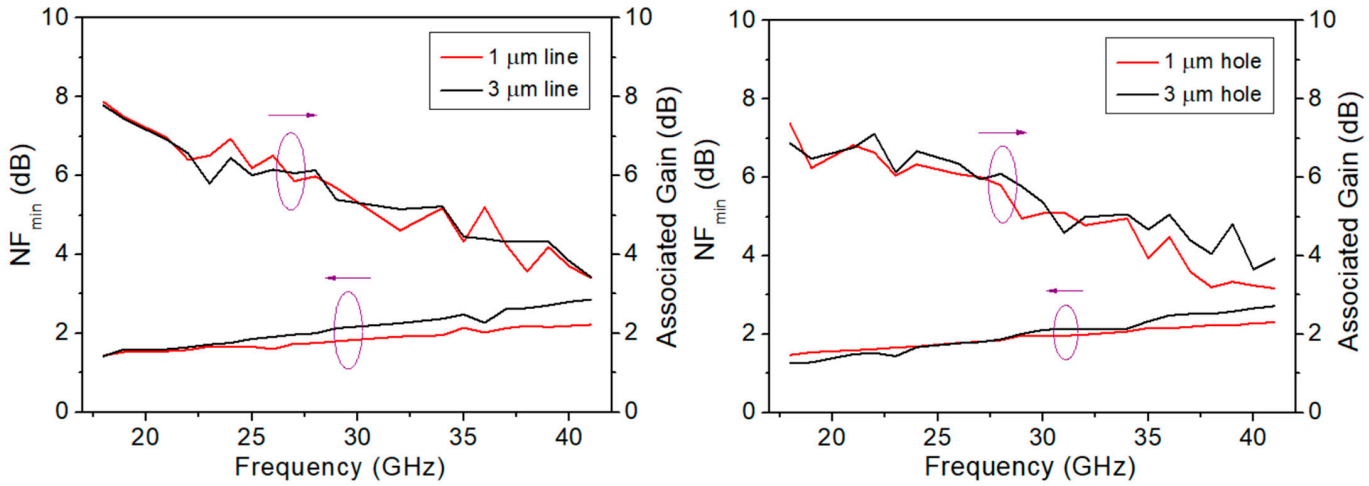


Figure 9. NF_{min}- Frequency curves for the 2 × 25 µm OEP AlGaN/GaN HEMTs with (**a**) etched-line patterns and (**b**) etched-hole patterns. (Left arrow: NF_{min}; right arrow: gain).

4. Conclusions

The design and fabrication of AlGaN/GaN HEMTs with four different OEPs to optimize the Ka-band performances were discussed in this study. The 1 µm line, 3 µm line, 1 µm hole, and 3 µm hole OEP AlGaN/GaN HEMTs were analyzed with regard to DC and RF characteristics. Low ρ_c of 4.04 × 10^{-7} Ω·cm^2 was also measured for the 1 µm line OEP HEMTs. Optimized G_m of 403 mS/mm and the I_{DSS} of 999 mA/mm were measured for the 1 µm line OEP HEMT. The small signal and large signal results of the OEP HEMTs were measured and the optimized performance achieved with the 1 µm line OEP HEMT. Moreover, the lowest NF_{min} of 1.75 dB among four OEP HEMTs was achieved with the fabricated 1 µm line OEP HEMTs, showing improvement in the RF noise figure characteristics. Overall, the increase in the contact area between the ohmic metal and the AlGaN barrier layer were used to reduce the contact resistance of the OEP HEMTs, and the results show that the 1 µm line OEP HEMT could be fabricated with the best improvement in RF performance for future 5G and B5G system applications at the Ka-band.

Author Contributions: Conceptualization, M.-W.L., C.-W.C. and Y.-C.L.; methodology, M.-W.L., C.-W.C. and Y.-C.L.; validation, Y.-C.L. and E.-Y.C.; formal analysis, M.-W.L., C.-W.C. and Y.-C.L.; investigation, M.-W.L., C.-W.C. and Y.-C.L.; resources, Y.-C.L. and E.-Y.C.; data curation, M.-W.L., C.-W.C. and Y.-C.L.; writing—original draft preparation, M.-W.L. and Y.-C.L.; writing—review and editing, F.G., Y.-C.L. and E.-Y.C.; visualization, M.-W.L., C.-W.C., Y.-C.L. and F.G.; supervision, F.G. and E.-Y.C.; project administration, Y.-C.L. and E.-Y.C.; funding acquisition, F.G., Y.-C.L. and E.-Y.C. All authors have read and agreed to the published version of the manuscript.

Funding: This research was financially supported in part by the National Science and Technology Council, Taiwan (project number: NSTC 111-2218-E-A49-018, NSTC 111-2634-F-A49-008, NSTC 111-2221-E-A49-173-MY3, and NSTC 112-2622-8-A49-013–SB), by the Co-creation Platform of the Industry-Academia Innovation School, NYCU, under the framework of the National Key Fields Industry-University Cooperation and Skilled Personnel Training Act, from the Ministry of Education (MOE), the National Development Fund (NDF), and industry partners in Taiwan.

Data Availability Statement: Data are contained within the article.

Acknowledgments: We acknowledge the Taiwan Semiconductor Research Institute (TSRI), Taiwan, for providing RF measurement support, the Centre for Research in Information and Communication Technologies of the University of Granada (CITIC-UGR), Spain, for funding support and the Compound Semiconductor Device Laboratory, NYCU, Taiwan, for wafer fabrication and DC measurement support.

Conflicts of Interest: The authors declare no conflicts of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript; or in the decision to publish the results.

References

1. Zanella, A.; Bui, N.; Castellani, A.; Vangelista, L.; Zorzi, M. Internet of Things for Smart Cities. *IEEE Internet Things J.* **2014**, *1*, 22–32. [CrossRef]
2. McEnroe, P.; Wang, S.; Liyanage, M. A Survey on the Convergence of Edge Computing and AI for UAVs: Opportunities and Challenges. *IEEE Internet Things J.* **2022**, *9*, 15435–15459. [CrossRef]
3. Al-Ali, A.R.; Zualkernan, I.A.; Rashid, M.; Gupta, R.; Alikarar, M. A smart home energy management system using IoT and big data analytics approach. *IEEE Trans. Consum. Electron.* **2017**, *63*, 426–434. [CrossRef]
4. Lorincz, J.; Klarin, Z.; Ožegović, J. A Comprehensive Overview of TCP Congestion Control in 5G Networks: Research Challenges and Future Perspectives. *Sensors* **2021**, *21*, 4510. [CrossRef] [PubMed]
5. Liu, W.; Michelson, D.G. Effect of Turbulence Layer Height and Satellite Altitude on Tropospheric Scintillation on Ka-Band Earth–LEO Satellite Links. *IEEE Trans. Veh. Technol.* **2010**, *59*, 3181–3192. [CrossRef]
6. Nakatani, K.; Komatsuzaki, Y.; Shinjo, S.; Kamioka, J.; Komaru, R.; Nakamizo, H.; Miyawaki, K.; Yamanaka, K. A highly integrated RF frontend module including Doherty PA, LNA and switch for high SHF wide-band massive MIMO in 5G. In Proceedings of the 2017 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR), Phoenix, AZ, USA, 15–18 January 2017; pp. 37–39. [CrossRef]
7. Ellinger, F.; Claus, M.; Schröter, M.; Carta, C. Review of advanced and Beyond CMOS FET technologies for radio frequency circuit design. In Proceedings of the 2011 SBMO/IEEE MTT-S International Microwave and Optoelectronics Conference (IMOC 2011), Natal, Brazil, 29 October–1 November 2011; pp. 347–351. [CrossRef]
8. Mehr, P.; Moallemi, S.; Zhang, X.; Lepkowski, W.; Kitchen, J.; Thornton, T.J. CMOS-Compatible MESFETs for High Power RF Integrated Circuits. *IEEE Trans. Semicond. Manuf.* **2019**, *32*, 14–22. [CrossRef]
9. Lin, Y.-C.; Chang, E.Y.; Yamaguchi, H.; Wu, W.-C.; Chang, C.-Y. A δ-Doped InGaP/InGaAs pHEMT with Different Doping Profiles for Device-Linearity Improvement. *IEEE Trans. Electron Devices* **2007**, *54*, 1617–1625. [CrossRef]
10. del Alamo, J.A. The High Electron Mobility Transistor. In *75th Anniversary of the Transistor*; IEEE: Piscataway, NJ, USA, 2023; pp. 253–262. [CrossRef]
11. Mishra, U.K.; Parikh, P.; Wu, Y.-F. AlGaN/GaN HEMTs-an overview of device operation and applications. *Proc. IEEE* **2022**, *90*, 1022–1031. [CrossRef]
12. Lee, M.-W.; Lin, Y.-C.; Chang, P.-S.; Tsao, Y.-F.; Hsu, H.-T.; Dee, C.-F.; Chang, E.Y. Over 10 W/mm High Power Density AlGaN/GaN HEMTs with Small Gate Length by the Stepper Lithography for Ka-Band Applications. *IEEE J. Electron Devices Soc.* **2023**, *11*, 311–318. [CrossRef]
13. Palacios, T.; Chakraborty, A.; Rajan, S.; Poblenz, C.; Keller, S.; DenBaars, S.; Speck, J.; Mishra, U. High-power AlGaN/GaN HEMTs for Ka-band applications. *IEEE Electron Device Lett.* **2005**, *26*, 781–783. [CrossRef]
14. Nakatani, K.; Yamaguchi, Y.; Komatsuzaki, Y.; Sakata, S.; Shinjo, S.; Yamanaka, K. A Ka-Band High Efficiency Doherty Power Amplifier MMIC using GaN-HEMT for 5G Application. In Proceedings of the 2018 IEEE MTT-S International Microwave Workshop Series on 5G Hardware and System Technologies (IMWS-5G), Dublin, Ireland, 30–31 August 2018; pp. 1–3. [CrossRef]

15. Xu, H.; Sanabria, C.; Chini, A.; Keller, S.; Mishra, U.K.; York, R.A. A C-band high-dynamic range GaN HEMT low-noise amplifier. *IEEE Microw. Wirel. Compon. Lett.* **2004**, *14*, 262–264. [CrossRef]
16. Palacios, T.; Chakraborty, A.; Heikman, S.; Keller, S.; DenBaars, S.P.; Mishra, U.K. AlGaN/GaN high electron mobility transistors with InGaN back-barriers. *IEEE Electron Device Lett.* **2006**, *27*, 13–15. [CrossRef]
17. Gibiino, G.P.; Angelotti, A.M.; Santarelli, A.; Florian, C. Microwave Characterization of Trapping Effects in 100-nm GaN-on-Si HEMT Technology. *IEEE Microw. Wirel. Compon. Lett.* **2019**, *29*, 604–606. [CrossRef]
18. Guo, J.; Li, G.; Faria, F.; Cao, Y.; Wang, R.; Verma, J.; Gao, X.; Guo, S.; Beam, E.; Ketterson, A.; et al. MBE-Regrown Ohmics in InAlN HEMTs With a Regrowth Interface Resistance of 0.05 Ω·mm. *IEEE Electron Device Lett.* **2012**, *33*, 525–527. [CrossRef]
19. Takei, Y.; Kamiya, M.; Tsutsui, K.; Saito, W.; Kakushima, K.; Wakabayashi, H.; Kataoka, Y.; Iwai, H. Ohmic Contact Properties Depending on AlGaN Layer Thickness for AlGaN/GaN High Electron Mobility Transistor Structures. *ECS Trans.* **2014**, *61*, 265–270. [CrossRef]
20. Lu, Y.; Ma, X.; Yang, L.; Hou, B.; Mi, M.; Zhang, M.; Zheng, J.; Zhang, H.; Hao, Y. High RF Performance AlGaN/GaN HEMT Fabricated by Recess-Arrayed Ohmic Contact Technology. *IEEE Electron Device Lett.* **2018**, *39*, 811–814. [CrossRef]
21. Benakaprasad, B.; Eblabla, A.M.; Li, X.; Crawford, K.G.; Elgaid, K. Optimization of Ohmic Contact for AlGaN/GaN HEMT on Low-Resistivity Silicon. *IEEE Trans. Electron Devices* **2020**, *67*, 863–868. [CrossRef]
22. Wang, C.; Zhao, M.D.; He, Y.L.; Zheng, X.F.; Wei, X.X.; Mao, W.; Zhang, J.; Hao, Y. Optimization of ohmic contact for AlGaN/GaN HEMT by introducing patterned etching in ohmic area. *Solid State Electron.* **2017**, *129*, 114–119. [CrossRef]
23. You, X.-R.; Chen, C.-W.; Tzou, J.; Hsin, Y.-M. Study of Au-based and Au-free Ohmic contacts in AlGaN/GaN HEMTs by recessed patterns. *ECS J. Solid State Sci. Technol.* **2021**, *10*, 075006. [CrossRef]
24. Takei, Y.; Kamiya, M.; Tsutsui, K.; Saito, W.; Kakushima, K.; Wakabayashi, H.; Kataoka, Y.; Iwai, H. Reduction of contact resistance on AlGaN/GaN HEMT structures introducing uneven AlGaN layers. *Phys. Status Solidi A* **2015**, *212*, 1104–1109. [CrossRef]
25. Wang, C.; He, Y.; Zheng, X.; Zhao, M.; Mi, M.; Li, X.; Mao, W.; Ma, X.; Hao, Y. Low ohmic-contact resistance in AlGaN/GaN high electron mobility transistors with holes etching in ohmic region. *Electron. Lett.* **2015**, *51*, 2145–2147. [CrossRef]
26. Han, K. Employing hole-array recess of barrier layer of AlGaN/GaN heterostructures to reduce annealing temperature of ohmic contact. *Semicond. Sci. Technol.* **2017**, *32*, 105010. [CrossRef]
27. Jang, M.; Park, J.; Hwang, J.H.; Mun, H.J.; Cha, S.; Hong, S.-M.; Jang, J.-H. Effects of periodic patterns in recessed ohmic contacts on InAlGaN/GaN heterostructures. *Solid-State Electron.* **2020**, *174*, 107917. [CrossRef]
28. Hajlasz, M.; Donkers, J.J.T.M.; Sque, S.J.; Heil, S.B.S.; Gravesteijn, D.J.; Rietveld, F.J.R.; Schmitz, J. Characterization of recessed Ohmic contacts to AlGaN/GaN. In Proceedings of the 2015 International Conference on Microelectronic Test Structures, Tempe, AZ, USA, 23–26 March 2015; pp. 158–162. [CrossRef]
29. Buttari, D.; Heikman, S.; Keller, S.; Mishra, U.K. Digital etching for highly reproducible low damage gate recessing on AlGaN/GaN HEMTs. In Proceedings of the IEEE Lester Eastman Conference on High Performance Devices, Newark, DE, USA, 8 August 2002; pp. 461–469. [CrossRef]
30. Romanczyk, B.; Zheng, X.; Guidry, M.; Li, H.; Hatui, N.; Wurm, C.; Krishna, A.; Ahmadi, E.; Keller, S.; Mishra, U.K. W-Band Power Performance of SiN-Passivated N-Polar GaN Deep Recess HEMTs. *IEEE Electron Device Lett.* **2020**, *41*, 349–352. [CrossRef]
31. Kim, D.-H.; del Alamo, J.A. 30-nm InAs Pseudomorphic HEMTs on an InP Substrate with a Current-Gain Cutoff Frequency of 628 GHz. *IEEE Electron Device Lett.* **2008**, *29*, 830–833. [CrossRef]
32. Buttari, D.; Chini, A.; Meneghesso, G.; Zanoni, E.; Moran, B.; Heikman, S.; Zhang, N.; Shen, L.; Coffie, R.; DenBaars, S.; et al. Systematic characterization of Cl2 reactive ion etching for improved ohmics in AlGaN/GaN HEMTs. *IEEE Electron Device Lett.* **2002**, *23*, 76–78. [CrossRef]
33. Kumazaki, Y.; Ozaki, S.; Okamoto, N.; Hara, N.; Ohki, T. Low-Resistance and Low-Thermal-Budget Ohmic Contact by Introducing Periodic Microstructures for AlGaN/AlN/GaN HEMTs. *IEEE Trans. Electron Devices* **2022**, *69*, 3073–3078. [CrossRef]
34. Lee, P.-H.; Lin, Y.-C.; Hsu, H.-T.; Tsao, Y.-F.; Dee, C.-F.; Su, P.; Chang, E.Y. A Tall Gate Stem GaN HEMT With Improved Power Density and Efficiency at Ka-Band. *IEEE J. Electron Devices Soc.* **2023**, *11*, 36–42. [CrossRef]
35. Binari, S.; Ikossi, K.; Roussos, J.A.; Kruppa, W.; Park, D.; Dietrich, H.B.; Koleske, D.D.; Wickenden, A.E.; Henry, R.L. Trapping effects and microwave power performance in AlGaN/GaN HEMTs. *IEEE Trans. Electron Devices* **2001**, *48*, 465–471. [CrossRef]
36. Jarndal, A.; Arivazhagan, L.; Almajali, E.; Majzoub, S.; Bonny, T.; Mahmoud, S. Impact of AlGaN Barrier Thickness and Substrate Material on the Noise Characteristics of GaN HEMT. *IEEE J. Electron Devices Soc.* **2022**, *10*, 696–705. [CrossRef]

physica status solidi a
www.pss-a.com

Study of AlGaN/GaN High-Electron-Mobility Transistors on Si Substrate with Thick Copper-Metallized Interconnects for Ka-Band Applications

*Ming-Wen Lee, Yueh-Chin Lin, Kuan-Hsien Lai, You-Chen Weng, Heng-Tung Hsu, and Edward Yi Chang**

Herein, the AlGaN/GaN high-electron-mobility transistors (HEMTs) on silicon substrates using thick copper-metallized interconnects with Pt diffusion barrier layer for Ka-band application are reported. High output power density of 6.6 W mm^{-1} with power-added efficiency (PAE) of 45.6% at 28 GHz is achieved for the 4 × 50 μm device in continuous-wave (CW) mode. No obvious change in the drain–source current (I_{DS}) is observed for the device under 40 V high-voltage stress for 100 h and the device shows good thermal stability when annealed at 300 °C for 30 min. It demonstrates that the AlGaN/GaN HEMTs on silicon substrate with thick copper-metallized interconnects can enhance the device performance with good reliability for future 5 G applications.

1. Introduction

Recently, high-frequency devices for Ka band and above are becoming more important for wireless communication due to 5 G and beyond applications. The high-frequency AlGaN/GaN high-electron-mobility transistors (HEMTs) are widely considered for millimeter-wave applications due to high electron mobility, high critical field, excellent electron peak velocity, and wide bandgap of GaN material.[1–4] To reduce the production cost, AlGaN/GaN HEMTs grown on Si substrates are popularly investigated for Ka band applications.[5] Besides, the AlGaN/GaN HEMTs on Si technology has the potential to be integrated into complementary metal-oxide-semiconductor (CMOS) circuits on the same platform.[6]

Over the past, several GaN-based technologies for applications at Ka band or above have been reported. Demonstration of high-efficiency monolithic microwave integrated circuits (MMIC) power amplifiers using 40 nm gate length technology was presented.[7] A 60 nm gate length with graded-channel technology was adopted, exhibiting peak power-added efficiency (PAE) up to 70%.[8,9] While the short gate length approaches effectively led to high efficiency at the desired frequency bands, the power density and overall reliability may be an issue due to the limited breakdown voltage. GaN-on-SiC configuration with very thin barrier of 3 nm was reported, showing a power density of 4 W mm^{-1} under continuous wave (CW) mode at 40 GHz.[10]

In general, gold (Au) is used as the thick metallization metal for III–V HEMTs in the past. Moreover, the price of Au is expensive. To reduce the production cost for mass production of GaN-based device, copper (Cu) is considered to be an ideal candidate to replace Au as metallization metal. Compared to Au, Cu has lower resistivity, and the better thermal conductivity of Cu suggests it to be a suitable replacement. Nevertheless, when Cu is in direct contact with a semiconductor, it tends to diffuse into the semiconductor, sabotaging the substrate and the device.[11–13] Therefore, a diffusion barrier layer is needed to overcome this problem.

Diffusion barrier layers such as tantalum (Ta), tantalum nitride (TaN_x), tungsten nitride (WN_x), Ta/$MnSi_xO_y$ bilayer structures, and platinum (Pt) have been studied in the past years.[13–17] According to the previous reports, Pt is an effective diffusion barrier to prevent Cu diffusion into III–V devices.[8,12,13] Reports have also shown that addition of titanium (Ti) layer to the Au/WN_x or WN_x/Cu interfaces can improve the adhesion between Cu and the semiconductor.[18]

M.-W. Lee, Y.-C. Lin, Y.-C. Weng, H.-T. Hsu
International College of Semiconductor Technology
National Yang Ming Chiao Tung University
Hsinchu 30010, Taiwan

K.-H. Lai
Department of Materials Science and Engineering
National Yang Ming Chiao Tung University
Hsinchu 30010, Taiwan

E. Y. Chang
International College of Semiconductor Technology
Department of Materials Science and Engineering
Department of Electronics Engineering
National Yang Ming Chiao Tung University
Hsinchu 30010, Taiwan
E-mail: edc@mail.nctu.edu.tw

E. Y. Chang
The Institute of Microengineering and Nanoelectronics
Universiti Kebangsaan Malaysia
Bangi 43600, Malaysia

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/pssa.202200536.

DOI: 10.1002/pssa.202200536

Furthermore, the Ti/Pt/Cu material system was proven to be very stable after annealing at 350 °C for 30 min.[19]

In this study, AlGaN/GaN HEMTs on Si substrates with thick Cu-metallized interconnects using Pt as diffusion barrier layer are investigated for Ka-band device applications. The direct current (DC) and radio frequency (RF) performances are investigated, and high-voltage stress test and thermal stability test are performed to study the reliability of the GaN device with thick Cu-metallized interconnects. Finally, it is demonstrated that the Cu-metallized devices are stable and have excellent device performance, even after high-voltage stress test and thermal stability test.

2. Device Fabrication

The AlGaN/GaN HEMTs on Si substrate wafer were grown by metal-organic vapor deposition (MOCVD) on 6-in. high-resistivity (>3 kΩ cm) Si <111> substrates. From the bottom to the top, the epitaxial structure of the AlGaN/GaN HEMTs consists of a GaN (500 nm)/AlGaN (50 nm)/AlN (120 nm) buffer layer, a 500 nm GaN channel layer, a 22 nm $Al_{0.22}Ga_{0.78}N$ barrier layer, and an 1 nm GaN cap layer, and the device structure is shown in **Figure 1**. The 500 nm GaN buffer layer is C doped (5×10^{18} cm^{-3}). The room-temperature electron mobility of 1700 cm^2 V^{-1} s^{-1} and a sheet carrier density of 8.5×10^{12} cm^{-2} were measured and obtained based on the Hall measurement for the structure after material growth.

There are four major steps in the fabrication of AlGaN/GaN HEMTs on Si substrate, which include ohmic contact formation, active region definition, gate formation, and thick metal interconnect fabrication. The ohmic metal of Ti (20 nm)/Al (120 nm)/Ni (25 nm)/Au (100 nm) was deposited by E-gun evaporator and then annealed by rapid thermal anneal (RTA) system at 850 °C for 30 s in N_2 ambient. Then, the B^{11+} ion-implantation isolation process was used to define the active region. Three process steps were used for the gate formation. First, a 100 nm SiN_x passivation layer was deposited through plasma-enhanced chemical vapor deposition (PECVD). Then, the ditch for gate stem was fabricated by e-beam lithography and SiN_x was etched by inductively coupled plasma (ICP). After that, the gate lithography process was performed by e-beam lithography and the gate metal was formed by Ni (50 nm)/Au (500 nm) metal stacks. The gate length of the device was around 200 nm in this study. Finally, the thick metal interconnect was fabricated; the Ti (30 nm)/Au (1,000 nm) thin metal layer was deposited first and then Ti (10 nm)/Pt (50 nm)/Ti (10 nm)/Cu (4,000 nm) thick metal stack was deposited. The schematics of the cross section of the device after Cu metallization are shown in Figure 1. Three kinds of transistors were used for this study, including a 2×50 μm device with $L_{SD} = 2.5$ μm, a 2×50 μm device with $L_{SD} = 3.0$ μm, and a 4×50 μm device with $L_{SD} = 2.5$ μm.

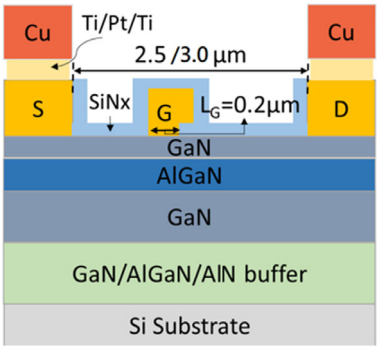


Figure 1. AlGaN/GaN HEMTs epitaxial layer and device structure.

3. Results and Discussion

The transmission line measurement (TLM) coordination diagram of the AlGaN/GaN HEMTs on Si substrate is shown in **Figure 2**. The results were measured using the standard TLM measurement with TLM patterns. TLM patterns with spacings (L) of 3, 5, 10, 20, and 36 μm with a width (W) of 75 μm were used for the TLM measurement. The contact resistances of the devices were 5.2×10^{-6} and 3.5×10^{-6} Ω cm^2 for the devices without and with 4 μm-thick Cu metallization, respectively. The contact resistance reduced because the metal resistance reduced owing to the thick metal used. **Figure 3** shows the DC characteristics for the 2×50 μm devices without and with thick Cu metallization. The saturation drain–source current (I_{DS}) increased from 541.2 to 575.2 mA mm^{-1} when the drain–source voltage (V_{DS}) was biased at 20 V, as shown in Figure 3a, and the maximum transconductance (G_m) increased from 240.9 to 260.8 mS mm^{-1}, as shown in Figure 3b. It can be observed that the I_{DS} and maximum G_m values increased due to the reduction of interconnect resistance.

S-parameter measurement was performed to characterize the 2×50 μm devices. **Figure 4** shows the device performance for the 2×50 μm devices without and with thick Cu metallization. The maximum stable gain (MSG)/maximum available gain (MAG) gain increased from 11.0 to 12.0 dB at 28 GHz and the gain increased from 7.8 to 8.7 dB at 60 GHz. The extracted source resistance (R_S) for the devices without and with thick Cu metallization were 12.5 and 8.0 Ω, respectively. It suggests that the incorporation of thick Cu metallization, which increases the cross-sectional area of the metal interconnections, has successfully reduced R_S.

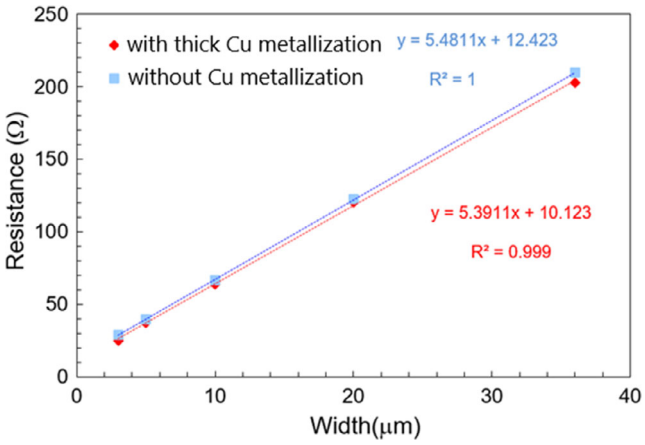


Figure 2. TLM result of AlGaN/GaN HEMTs on Si substrate without and with thick Cu metallization.

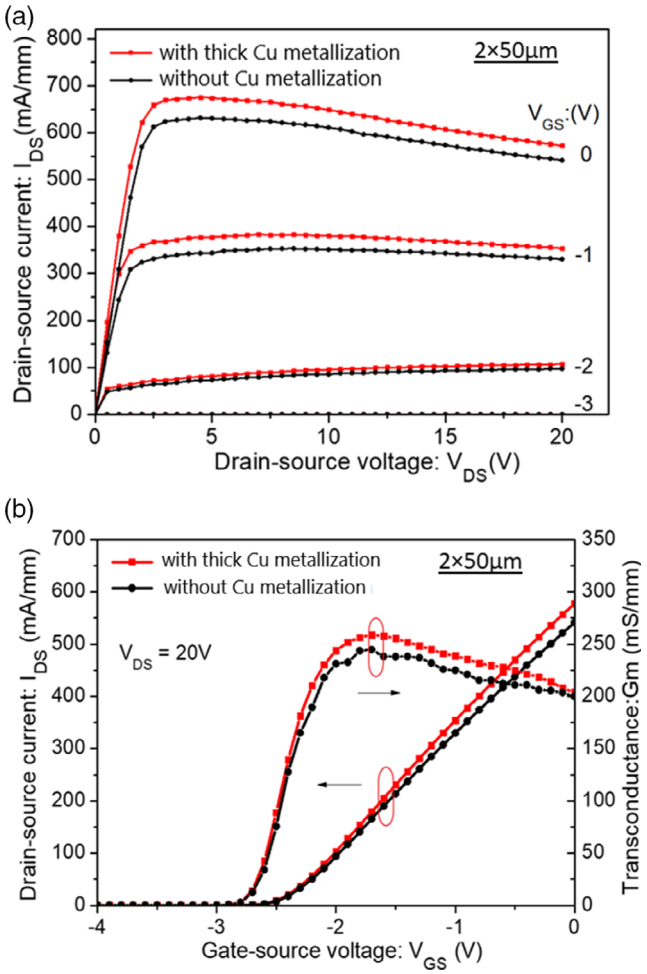


Figure 3. a) I_{DS}–V_{DS} and b) I_{DS}–V_{GS} of the 2 × 50 μm AlGaN/GaN HEMTs on Si substrate without and with thick Cu metallization.

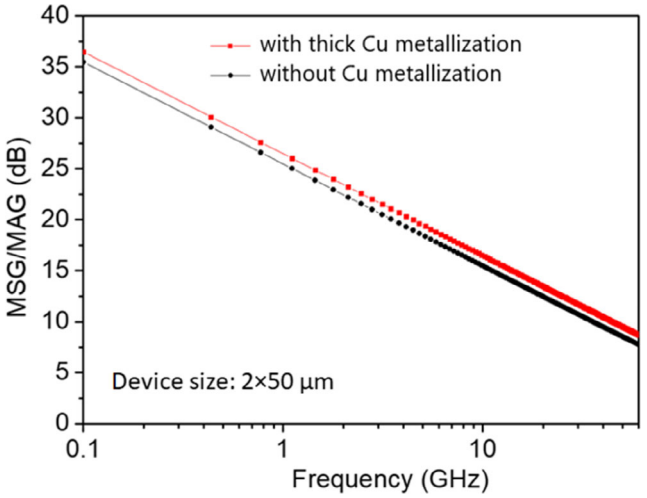


Figure 4. MSG/MAG gain of the 2 × 50 μm AlGaN/GaN HEMTs on Si substrate without and with thick Cu metallization.

The 28 GHz load–pull measurement results of the 2 × 50 μm AlGaN/GaN HEMTs without and with thick Cu metallization are shown in **Figure 5**. The linear gain improved from 7.3 to 7.6 dB, output power density (P_{OUT}) at P3dB increased from 2.3 to 2.8 W mm^{-1}, and PAE increased from 34.8% to 44.3%. The device performances were improved owing to the resistance reduction in the device after the thick Cu metallization. Furthermore, 4 × 50 μm devices were also evaluated since the R_S tends to decrease as the device size increases. The device exhibits a linear gain of 7.8 dB, a high maximum output power of 6.6 W mm^{-1}, and PAE of 45.6%, as shown in **Figure 6**.

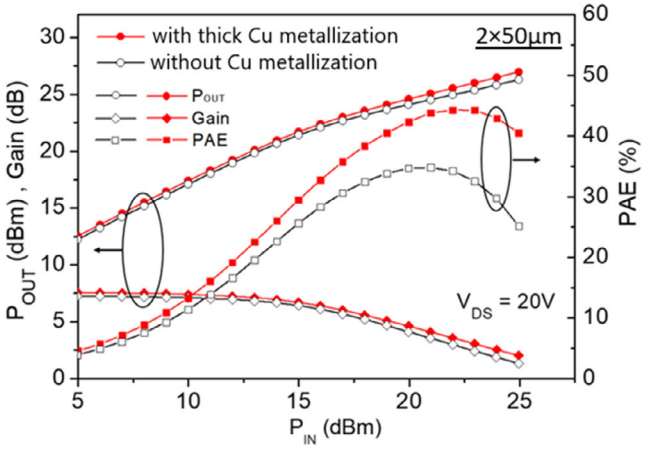


Figure 5. 28 GHz load–pull measurement results of the 2 × 50 μm AlGaN/GaN HEMT on Si substrate without and with 4 μm Cu metallization under class AB bias and at V_{DS} = 20 V.

Table 1 shows the comparison of the AlGaN/GaN HEMTs without and with thick Cu-metallized interconnects and AlGaN/GaN HEMTs fabricated by other groups in recent years using conventional Au metallization. The fabricated devices without and with 4 μm Cu metallization all have 1 μm Au metallization interconnect directly deposited on the ohmic metal. The devices with thick Cu-metallized interconnects show better performance even when compared to AlGaN/GaN HEMTs on SiC fabricated by some other groups using conventional Au

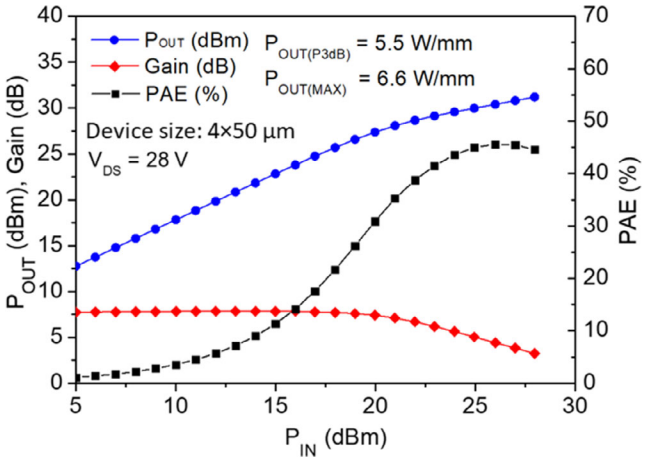


Figure 6. 28 GHz load–pull measurement results of the 4 × 50 μm AlGaN/GaN HEMT on Si substrate with 4 μm Cu metallization under class A bias and at V_{DS} = 28 V.

Table 1. Comparison of the power performances of the fabricated devices without and with 4 μm Cu metallization and other published data in recent years.

	This work				[20]	[21]	[22]	[23]			[24]
Frequency [GHz]	28				35	30	21.5	30			40
Substrate	Si				SiC	SiC	SiC	SiC			Si
L_g [nm]	200				150	150	150	150			75
Cu metallization	w/o		w/					w/o			
Device size [μm]	2 × 50	2 × 50	2 × 50	4 × 50	8 × 50	6 × 50	8 × 50	2 × 50	6 × 50	8 × 50	2 × 50
V_{DS} [V]	20	20	28	28	20	20	20	20	17.5	15	25
PAE [%]	34.8	44.3	35.7	45.6	49	39	50	39	29	40	12.5
P_{OUT} (@P3dB) [W mm^{-1}]	2.3	2.8	4.2	5.2	–	–	3.2	–	–	–	–
P_{OUT} (PAE peak) [W mm^{-1}]	2.8	3.6	5.0	5.5	3.0	3.5	–	5.0	2.5	3.2	–
P_{OUT} (maximum) [W mm^{-1}]	4.2	5.0	6.1	6.6	–	–	–	6.0	–	–	2.7

metallization (2–3 μm). This is mainly due to the use of thicker Cu layer, which has a lower resistivity than Au. The overall reduction of parasitic resistance at high-frequency measuring environments and enhanced heat conductivity with thick Cu layers under high-power measurements enable the fabricated Cu-metallized HEMT devices to outperform published AlGaN/GaN HEMTs on SiC, which would normally be difficult to achieve with the superior characteristics of SiC over Si substrates on thermal conductivity.

For the high-voltage stress test at room temperature, the 2 × 50 μm Cu-metallized interconnect devices with L_{SD} = 2.5 μm were stressed at V_{DS} = 40 V with gate–source voltage (V_{GS}) of −2.1 V for 10 h (on-state) and V_{GS} of −3.5 V for 100 h (off-state), respectively. **Figure 7** shows the on-state I_{DS} and gate-source current (I_{GS}) for the 2 × 50 μm Cu-metallized interconnect devices (L_{SD} = 2.5 μm) after a 40 V high-voltage stress test for 10 h. No clear I_{DS} change was observed after the stress. **Figure 8** shows the off-state I_{DS}, I_{GS}, and the measured I_{DS} degradation for V_{DS} = 20 V at room temperature for the 2 × 50 μm Cu-metallized interconnect devices (L_{SD} = 2.5 μm) after a 40 V high-voltage stress test for 100 h. No obvious increase for the off-state I_{DS} and I_{GS} was found for the devices. The 2 × 50 μm device (L_{SD} = 2.5 μm) saturation I_{DS} variation with

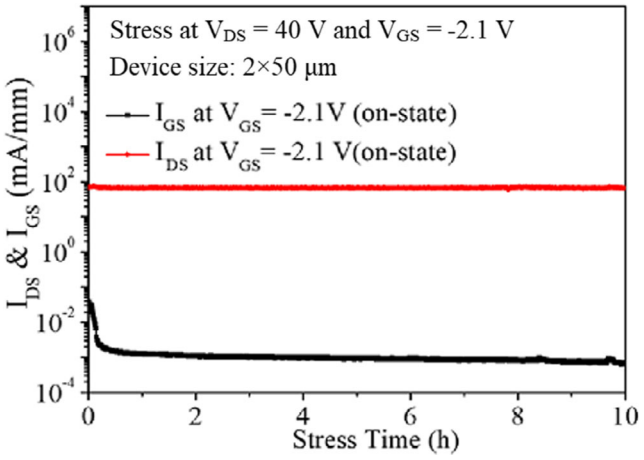


Figure 7. On-state I_{DS} and I_{GS} for the 2 × 50 μm Cu-metallized AlGaN/GaN HEMTs (L_{SD} = 2.5 μm) on Si after stress test for 10 h.

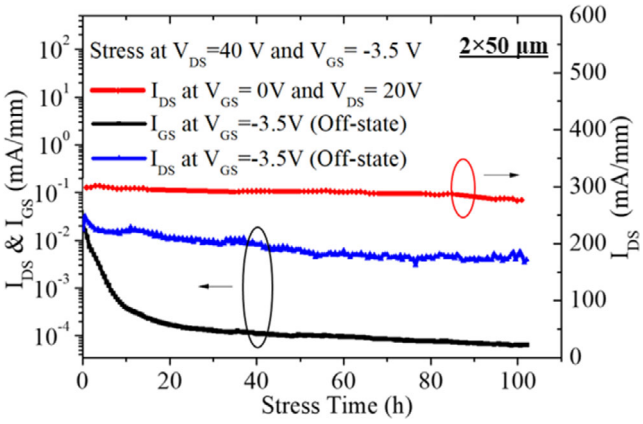


Figure 8. Off-state I_{DS}, off-state I_{GS}, and on-state I_{DS} for the 2 × 50 μm Cu-metallized AlGaN/GaN HEMTs (L_{SD} = 2.5 μm) on Si after stress test for 100 h.

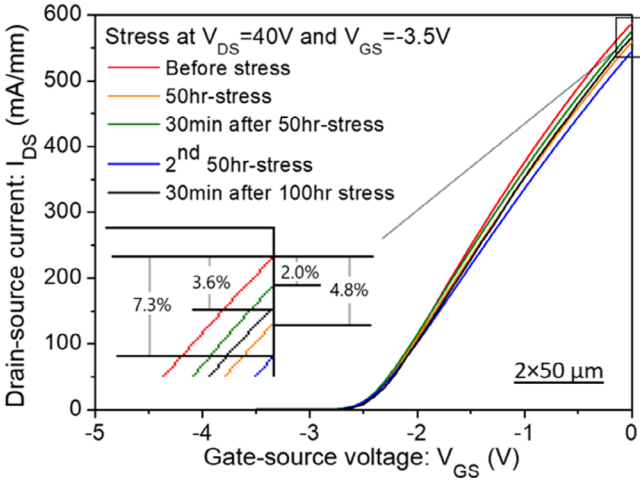


Figure 9. Off-state 40 V stress measurement results for the 2 × 50 μm Cu-metallized AlGaN/GaN HEMTs (L_{SD} = 2.5 μm).

different stress time is shown in **Figure 9**. The 2 × 50 μm device (L_{SD} = 2.5 μm) shows 7.3% I_{DS} degradation from initial values after being stressed for 100 h and recovers to 3.6% I_{DS} degradation after stopped stressed for 30 min. The current degradation is believed to be due to the electrically induced defect formation and charge injection when the devices are under high-voltage stress.[25]

However, even though the electrons injected from the gate electrode during the high-voltage stress flowed into the gate-to-drain region and were captured by the surface states at this region, causing the 2D electron gas (2DEG) density to decrease due to the charge neutralization process, most charge injection was released after the high-voltage stress.[26] The small current change after high-voltage stress indicated that the device with Cu-metallized interconnects was quite stable under high-voltage stress, and the degradation is mainly related to Cu metallization after the 100 h stress.

For the high-voltage stress test at high temperature, the 2 × 50 μm devices with larger S–D spacing of 3 μm were adopted for the reliability test due to the lower gate leakage current and higher breakdown voltage. The main consideration is to prevent other possible breakdown mechanisms from occurring during the stress test. The 2 × 50 μm Cu-metallized interconnect devices were stressed at a V_{DS} of 40 V with V_{GS} of −3.5 V (off-state) for 10 h at 150 °C. **Figure 10** shows the off-state I_{DS}, I_{GS}, and the measured I_{DS} degradation at 150 °C with V_{DS} = 20 V for the Cu-metallized interconnect devices after a 40 V high-voltage stress test for 10 h. No obvious increase for the off-state I_{DS} was found for the devices. The device saturation I_{DS} variation with different stress time is shown in **Figure 11**. The device shows 2.8% I_{DS} degradation from initial values after high-voltage stress. **Figure 12** shows the Gm–V_{GS} curve of the Cu-metallized interconnect devices under 150 °C, 10 h stress test. It can be seen that the device Gm profiles remained similar after the devices were stressed with high voltage at high temperature.

Figure 13 shows the 28 GHz load–pull measurement results for the 2 × 50 μm Cu-metallized AlGaN/GaN HEMTs with 3 μm S–D spacing before and after 40 V high-voltage stress at 150 °C. The device maximum output power (P_{OUT}) degraded from 25.9

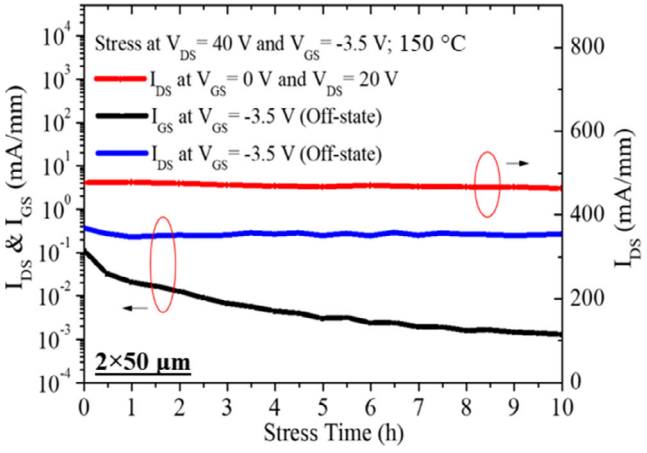


Figure 10. Off-state I_{DS}, off-state I_{GS}, and on-state I_{DS} at 150 °C for the 2 × 50 μm Cu-metallized AlGaN/GaN HEMTs (L_{SD} = 3.0 μm) on Si after stress test for 10 h.

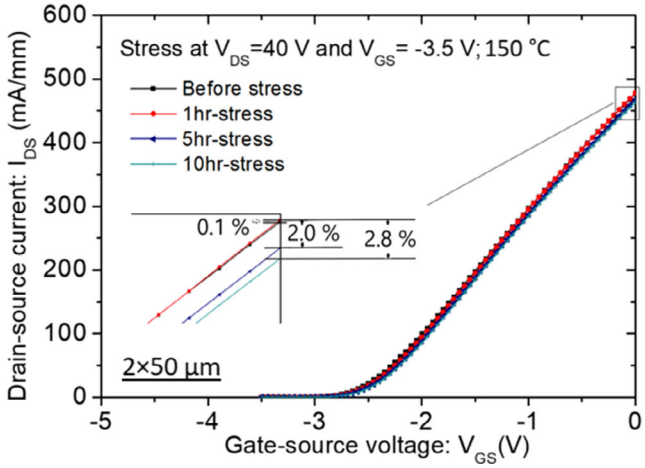


Figure 11. I_{DS}–V_{GS} results for the 2 × 50 μm Cu-metallized AlGaN/GaN HEMTs (L_{SD} = 3.0 μm) after off-state V_{DS} = 40 V under 150 °C stress test for 0, 1, 5, and 10 h.

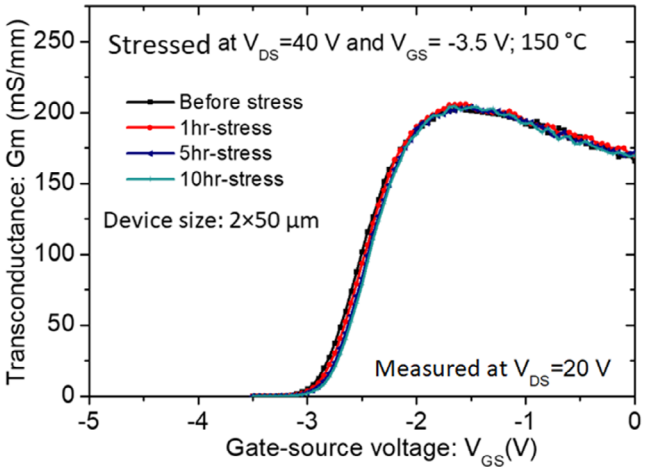


Figure 12. The Gm–V_{GS} curve of the 2 × 50 μm Cu-metallized AlGaN/GaN HEMTs on Si substrate (L_{SD} = 3.0 μm) under 150 °C after stress test for 0, 1, 5, and 10 h.

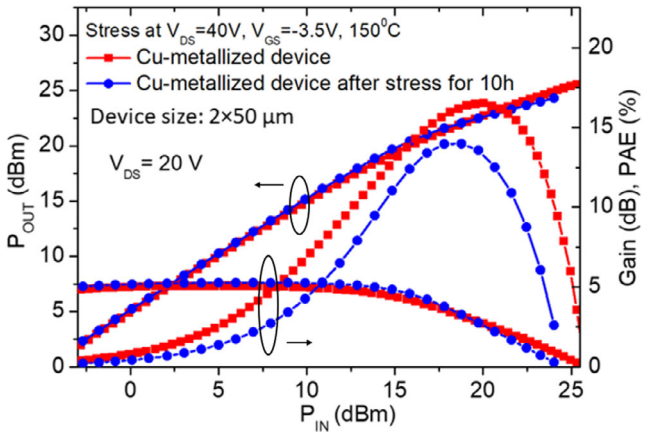


Figure 13. 28 GHz load–pull measurement results of the 2 × 50 μm Cu-metallized AlGaN/GaN HEMTs on Si substrate (L_{SD} = 3.0 μm) before and after 150 °C and 10 h off-state stress test.

to 24.3 dBm, and PAE decreased from 16.6% to 14.0%. The device performance degradation was due to the electrically induced defect formation when the devices were under high-voltage stress at 150 °C.[21]

The measurement results in Figure 5 and 13 show that the device maximum output power was 27 and 25.9 dBm for the devices with 2.5 μm S–D spacing and 3 μm S–D spacing, respectively. With the similar P_{OUT} for the devices with S–D spacing of 2.5 and 3 μm measured, the main degradation found in the maximum PAE was due to the degradation in gain. Such degradation in gain can be related to the degradation in Gm from DC measurement results, which is mainly due to the increase of R_S as the S–D spacing increases.

Thermal stability test was also performed, and the 2 × 50 μm Cu-metallized devices (L_{SD} = 2.5 μm) were annealed at 300 °C for 30 min in N_2 ambient. **Figure 14** shows the I_{DS}–V_{DS} curve and I_{DS}–V_{GS} and Gm–V_{GS} curve of the 2 × 50 μm Cu-metallized AlGaN/GaN HEMTs on Si substrate (L_{SD} = 2.5 μm) before and after annealing. No obvious device degradation and DC characteristics change were observed after the annealing process. **Figure 15** shows the 28 GHz load–pull measurement results for the 2 × 50 μm Cu-metallized devices (L_{SD} = 2.5 μm) before and after annealing at 300 °C for 30 min. No clear degradation was observed for the output power and PAE of the device. The device with Cu-metallized interconnect using Pt as the diffusion barrier showed good thermal stability. Multiple devices were tested throughout the study of the high-voltage stress test, the thermal stability test, and the stress reliability test and showed reproducibility for the application of thick Cu metallization on AlGaN/GaN HEMT on Si substrate devices. With the thick Cu metallization interconnect, the AlGaN/GaN HEMTs on Si substrate were able to show improved DC and RF characteristics, and after the high-voltage stress tests and the thermal stability tests were done on the Cu-metallized HEMT devices, there does not exist obvious device performance degradation. Therefore, the stress and thermal tests were not done on the devices without Cu metallization.

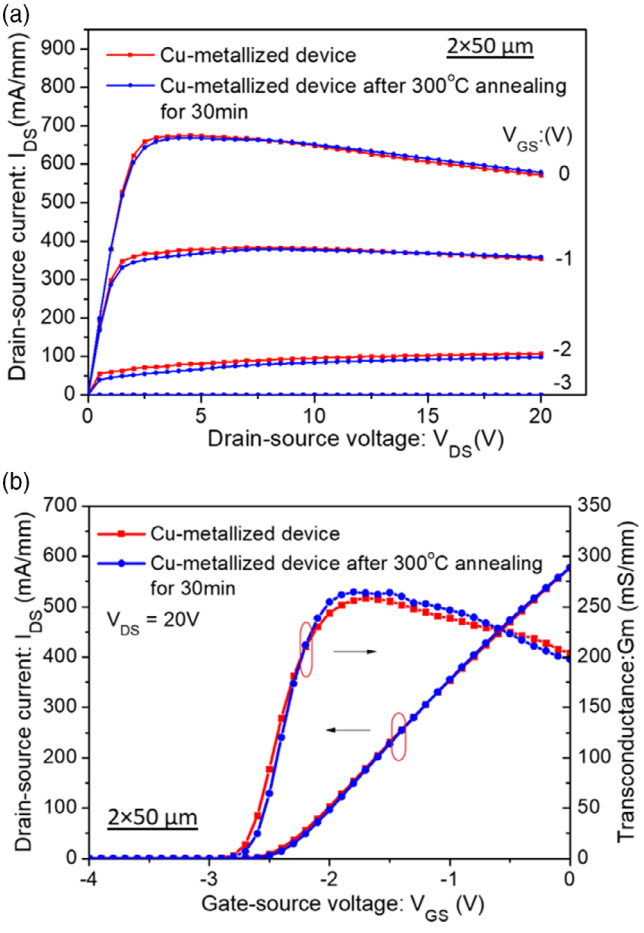


Figure 14. a) I_{DS}–V_{DS} and b) I_{DS}–V_{GS} and Gm–V_{GS} of the 2 × 50 μm Cu-metallized AlGaN/GaN HEMTs on Si substrate (L_{SD} = 2.5 μm) before and after 300 °C for 30 min annealing.

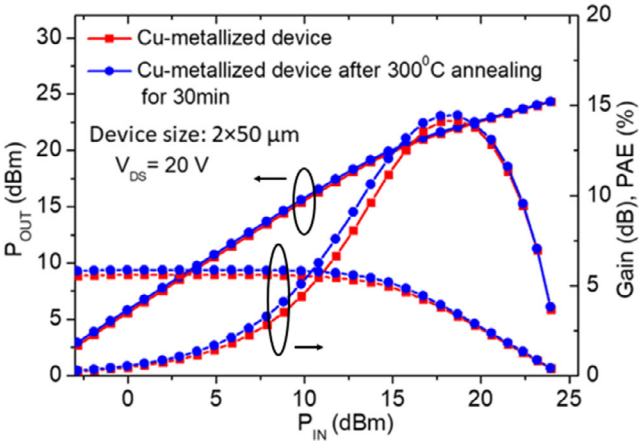


Figure 15. 28 GHz load–pull measurement results of the of 2 × 50 μm Cu-metallized AlGaN/GaN HEMTs on Si substrate (L_{SD} = 2.5 μm) before and after annealing at 300 °C for 30 min.

4. Conclusion

The AlGaN/GaN HEMTs on Si substrate with thick Cu-metallized interconnects using Pt as the diffusion barrier were successfully fabricated and demonstrated good characteristics for Ka-band applications. The device DC and RF performances were improved due to the decrease of parasitic resistance at high frequency, using 4 μm-thick Cu metallization. High-power density of 6.6 W mm^{-1} and PAE of 45.58% were obtained for the 4 × 50 μm device when operated at 28 GHz in the CW mode. No clear device performance degradation was observed for the 2 × 50 μm device after high-voltage stress and high-temperature thermal stability test. Overall, the Cu-metallized devices demonstrated excellent device performance at Ka band and showed stable performance after the high-voltage stress test and high-temperature test.

Acknowledgements

This work was financially supported by the "Center for the Semiconductor Technology Research" from The Featured Areas Research Center Program within the framework of the Higher Education Sprout Project by the

Ministry of Education (MOE) in Taiwan. It was also supported in part by the Ministry of Science and Technology, Taiwan, under grant NSTC 110-2622-8-A49-008-SB, NSTC 111-2622-8-A49-018-SB, and NSTC 111-2634-F-A49-008, as well as National Chung-Shan Institute of Science and Technology NCSIST-404-V407(111).

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

Research data are not shared.

Keywords

AlGaN/GaN high-electron-mobility transistors, copper metallizations, Ka band, platinum, Si substrates

Received: July 31, 2022
Revised: November 14, 2022
Published online: February 15, 2023

[1] U. K. Mishra, P. Parikh, Y.-F. Wu, *Proc. IEEE* **2002**, *90*, 1022.
[2] U. K. Mishra, L. Shen, T. E. Kazior, Y. Wu, *Proc. IEEE* **2008**, *96*, 287.
[3] T. Aggerstam, S. Lourdudoss, H. H. Radamson, M. Sjődin, P. Lorenzini, D. C. Look, *Thin Solid Films* **2006**, *515*, 705.
[4] T. Nanjo, A. Imai, Y. Suzuki, Y. Abe, T. Oishi, M. Suita, E. Yagyu, Y. Tokuda, *IEEE Trans. Electron Devices* **2013**, *60*, 1046.
[5] F. Medjdoub, M. Zegaoui, B. Grimbert, D. Ducatteau, N. Rolland, P. A. Rolland, *IEEE Electron Device Lett.* **2012**, *33*, 1168.
[6] U. Peralagu, A. Alian, V. Putcha, A. Khaled, R. Rodriguez, A. Sibaja-Hernandez, S. Chang, E. Simoen, S. E. Zhao, B. De Jaeger, D. M. Fleetwood, P. Wambacq, M. Zhao, B. Parvais, N. Waldron, N. Collaert, in *IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA **2019**, pp. 17.2.1–17.2.4.
[7] M. Micovic, D. Regan, J. Wong, J. Tai, H. Sharifi, in *Proc. 2019 IEEE BiCMOS Compound semiconductor Integrated Circuits and Technology Symp. (BCICTS)*, IEEE, Piscataway, NJ **2019**, pp. 1–3.
[8] J. Moon, J. C. Wong, B. Grabar, M. Antcliffe, P. Chen, E. Arkun, I. Khalaf, A. Corrion, in *2019 14th European Microwave Integrated Circuits Conf. (EuMIC)*, Paris, France **2019**, pp. 57–59.
[9] J. Moon, R. Grabar, J. C. Wong, M. Antcliffe, P. Chen, E. Arkun, I. Khalaf, A. Corrion, J. Chappell, N. Venkatesan, P. J. Fay, *Electron. Lett.* **2020**, *56*, 678.
[10] K. Harrouche, R. Kabouche, E. Okada, F. Medjdoub, *IEEE J. Electron Devices Soc.* **2019**, *7*, 1145.
[11] Y. C. Lin, T. Y. Kuo, Y. L. Chuang, C. H. Wu, C. H. Chang, K. N. Huang, E. Y. Chang, *Appl. Phys. Express* **2012**, *5*, 066503.
[12] Y. C. Lin, C. H. Chang, F. M. Li, L. H. Hsu, E. Y. Chang, *Appl. Phys. Express* **2013**, *6*, 091003.
[13] T. E. Hsieh, Y. C. Lin, F. M. Li, W. C. Shi, Y. X. Huang, W. C. Lan, P. C. Chin, E. Y. Chang, *J. Electron. Mater.* **2015**, *44*, 4700.
[14] C. Y. Chen, E. Y. Chang, L. Chang, S. H. Chen, *IEEE Trans. Electron Devices* **2001**, *48*, 1033.
[15] C. Hsin, K. Lin, *IEEE Electron Device Lett.* **2016**, *37*, 1048.
[16] Y. C. Wu, E. Y. Chang, Y. C. Lin, H. T. Hsu, S. H. Chen, W. C. Wu, L. H. Chu, C. Y. Chang, *IEEE Microwave Wireless Compon. Lett.* **2007**, *17*, 133.
[17] Y. Wu, E. Y. Chang, Y. Lin, L. Hsu, *IEEE Trans. Device Mater. Reliab.* **2008**, *8*, 621.
[18] C. S. Lee, Y. C. Lien, E. Y. Chang, H. C. Chang, S. H. Chen, C. T. Lee, L. H. Chu, S. W. Chang, Y. C. Hsieh, *IEEE Trans. Electron Devices* **2006**, *53*, 1753.
[19] S. W. Chang, E. Y. Chang, D. Biswas, C. S. Lee, K. S. Chen, C. W. Tseng, T. L. Hsieh, W. C. Wu, *Jpn. J. Appl. Phys.* **2005**, *44*, 8.
[20] S. Chen, S. Nayak, C. Campbell, E. Reese, in *2016 IEEE Compound Semiconductor Integrated Circuit Symp. (CSICS)*, Austin, TX **2016**, pp. 1–4.
[21] L. T. Xuan, R. Aubry, N. Michel, O. Patard, J. Jacquet, S. Piotrowicz, M. Oualli, P. Gamarra, C. Potier, D. Lancereau, S. L. Delage, S. Laurent, P. P. Bouysse, R. Quéré, in *2016 11th European Microwave Integrated Circuits Conf. (EuMIC)* **2016**, pp. 65–68.
[22] Y. S. Noh, I. B. Yom, *IEEE Microwave Wireless Compon. Lett.* **2016**, *26*, 619.
[23] R. Aubry, J. C. Jacquet, M. Oualli, O. Patard, S. Piotrowicz, E. Chartier, N. Michel, L. Trinh Xuan, D. Lancereau, C. Potier, M. Magis, P. Gamarra, C. Lacam, M. Tordjman, O. Jardel, C. Dua, S. L. Delage, *IEEE Electron Device Lett.* **2016**, *37*, 629.
[24] P. Altuntas, F. Lecourt, A. Cutivet, N. Defrance, E. Okada, M. Lesecq, S. Rennesson, A. Agboton, Y. Cordier, V. Hoel, J. C. D. Jaeger, *IEEE Electron Device Lett.* **2015**, *36*, 303.
[25] J. A. del Alamo, J. Joh, *Microelectron. Reliab.* **2009**, *49*, 1200.
[26] J. A. Mittereder, S. C. Binari, P. B. Klein, J. A. Roussos, D. S. Katzer, D. F. Storm, D. D. Koleske, A. E. Wickenden, R. L. Henry, *Appl. Phys. Lett.* **2003**, *83*, 1650.

Received 7 March 2023; revised 19 April 2023 and 12 May 2023; accepted 16 May 2023. Date of publication 18 May 2023; date of current version 29 May 2023.
The review of this article was arranged by Editor G. I. Ng.

Digital Object Identifier 10.1109/JEDS.2023.3277796

Over 10W/mm High Power Density AlGaN/GaN HEMTs With Small Gate Length by the Stepper Lithography for Ka-Band Applications

MING-WEN LEE [1,2] (Graduate Student Member, IEEE), YUEH-CHIN LIN [1], PO-SHENG CHANG [1], YI-FAN TSAO [1] (Member, IEEE), HENG-TUNG HSU [1] (Senior Member, IEEE), CHANG-FU DEE [3], AND EDWARD YI CHANG [1,3,4,5] (Life Fellow, IEEE)

1 International College of Semiconductor Technology, National Yang Ming Chiao Tung University, Hsinchu 300, Taiwan
2 Doctorate Programme in Information and Communication Technologies, University of Granada, 18012 Granada, Spain
3 Institute of Microengineering and Nanoelectronics, Universiti Kebangsaan Malaysia, Bangi 43600, Malaysia
4 Department of Materials Science and Engineering, National Yang Ming Chiao Tung University, Hsinchu 300, Taiwan
5 Department of Electronics Engineering, National Yang Ming Chiao Tung University, Hsinchu 300, Taiwan

CORRESPONDING AUTHOR: E. Y. CHANG (e-mail: edc@nycu.edu.tw)

This work was supported in part by the "Center for the Semiconductor Technology Research" from the Featured Areas Research Center Program within the Framework of the Higher Education Sprout Project by the Ministry of Education (MOE), Taiwan, and in part by the Ministry of Science and Technology, Taiwan, under Grant NSTC 111-2218-E-A49-021, Grant NSTC 111-2634-F-A49-008, Grant NSTC 111-2221-E-A49-173-MY3, and Grant NSTC 112-2622-8-A49-013–SB.

ABSTRACT This study reports AlGaN/GaN high-electron-mobility transistors (HEMTs) fabricated by the Stepper Lithography on a 4-inch wafer for Ka-Band applications. Small gate length (L_G) of 100 nm was achieved through a 2-Step Photolithography Process and the gate region of the AlGaN/GaN HEMT was defined by using two lithography steps to form gamma-shaped gates. The 4-inch AlGaN/GaN HEMT wafer demonstrated high electrical performance uniformity with respect to the maximum drain-source current density (I_{DSS}), the peak extrinsic output transconductance (G_m), and the threshold voltage (V_{th}). At $V_{DS} = 20$ V, the AlGaN/GaN HEMT exhibits an I_{DSS} of 1004.2 mA/mm, a Gm value of 363.6 mS/mm, a maximum output power density ($P_{OUT\ (MAX)}$) of over 10 W/mm, and a power gain of 8.8 dB with a maximum 51.1% Power-added efficiency (PAE) at 28 GHz in Continuous Wave (CW) mode. The results show the potential of AlGaN/GaN HEMT fabrication with high yield and outstanding RF performance using Stepper Lithography for 5G applications.

INDEX TERMS 5G, high uniformity, output power, stepper lithography, small gate length.

I. INTRODUCTION

Gallium Nitride, with its outstanding characteristics by forming 2-Dimensional Electron Gas (2DEG) through piezoelectric and spontaneous polarizations using AlGaN/GaN heterojunction, was used for power high-electron-mobility transistor (HEMT) devices with multi-gigahertz frequency range in the year of 2005 by Eudyna Corporation in Japan [1]. Later, with its high mobility, high bandgap and high thermal conductivity features [2], the GaN HEMT devices became popular worldwide for RF applications due to the inherent material properties which include high breakdown voltage, high current density, low thermal resistance, and low substrate parasitic capacitances [3], [4]. GaN-based HEMTs outperform Si and GaAs-based devices [5] owing to their higher output power characteristics and higher thermal resistance. With the increasing demands of RF power devices at Ka-Band and beyond for applications such as 5G, military radars, satellites, and networks for advanced communication systems, it is essential to reduce the GaN high frequency device manufacturing cost by increasing the device yield and to improve the device DC and RF performance.

Traditionally, researchers fabricate small gate length (L_G) devices with the E-beam Lithography System [6], [7], [8], [33]. However, for mass production of the GaN HEMT for 5G commercial applications, the E-beam Lithography Process is complicated, high cost, and time consuming. Therefore, it is essential to develop more efficient and economical methods with higher yield to meet the industrial needs.

Over the past few decades, Steppers, also known as the Step-and-Repeat Lithography System, have been widely adopted for large scale commercial application of III-V semiconductor integrated circuits for its' simple and direct process steps and capability to utilize a fine reticle with less particles [9], [10], [11]. However, for the conventional stepper process, it is difficult to achieve submicron gate lengths to reduce gate resistance, increase cut-off frequency, and switching speed for high frequency applications.

To scale down the L_G with the Stepper, a 2-Step Photolithography Process is introduced in this study. High performance Ka band HEMT devices on a 4-inch SiC wafer with excellent wafer uniformity using the Stepper Lithography is realized by the approach in this paper.

II. DEVICE FABRICATION

To provide high 2DEG density for the device for high RF power operation, wafers with AlGaN/AlN/GaN layers grown on top of the SiC substrate by the metal organic chemical vapor deposition (MOCVD) system were used. The epitaxy of the SiC wafer includes a 0.3 μm Fe-GaN buffer layer with doping concentration of 1×10^{18} cm^{-3}, a 0.9 μm i-GaN buffer layer, a 0.8-nm AlN layer, and a 17-nm AlGaN barrier layer to realize the heterojunction structure. A 2DEG density of 1.3×10^{13} cm^{-2} and an electron mobility of 2300 cm^2/V·s were obtained based on the Hall measurement of the structure.

Standard fabrication steps of source/drain ohmic contact formation, device isolation, gate Schottky contact formation, passivation and contact via hole formation were processed. After the wafer cleaning process by Acetone (ACE) and Isopropyl alcohol (IPA), the wafer was then immersed in a 10% Hydrochloric acid (HCl) solution to remove the native oxides.

Transfer length method (TLM) was used for the extraction of R_C. The contact resistance was 0.35 Ω·mm, and the contact resistivity is 2.6×10^{-6} Ω·cm^2, as shown in Fig. 4. The Ti/Al/Ni/Au ohmic contact was then deposited by the E-gun evaporator (E-gun) and then annealed at 850 °C for 30 s in N_2 ambient for alloying.

Device isolation was defined by Boron implantation. The gate formation process is shown in Fig. 1. A 150-nm thick SiN_x film was first deposited with Plasma-Enhanced Chemical Vapor Deposition System (PECVD) on the wafer. Then, the first stepper lithography process was done and Position 1 was defined after ICP etch. To ensure the 1st nitride etch reach the barrier layer, the SiN_x layer was etched with CF_4 plasma [12]. The second photolithography step

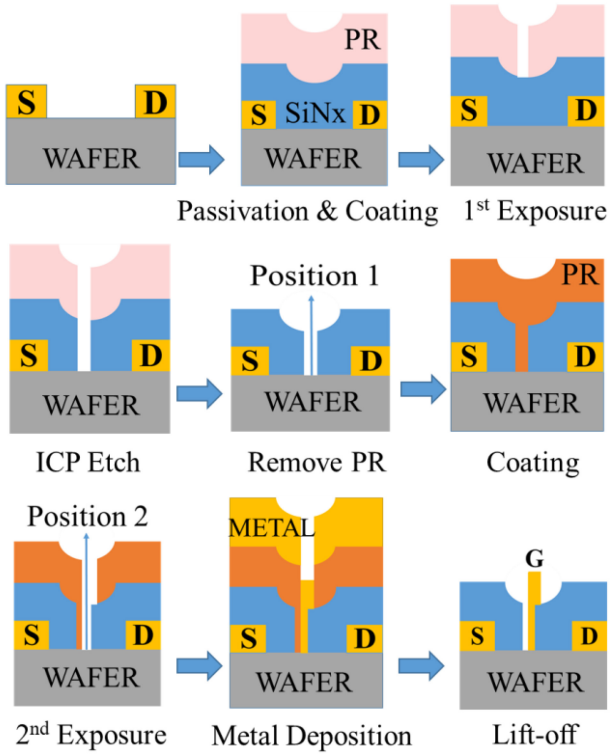


FIGURE 1. 2-Step Photolithography Process shown with its cross section of AlGaN/GaN HEMTs.

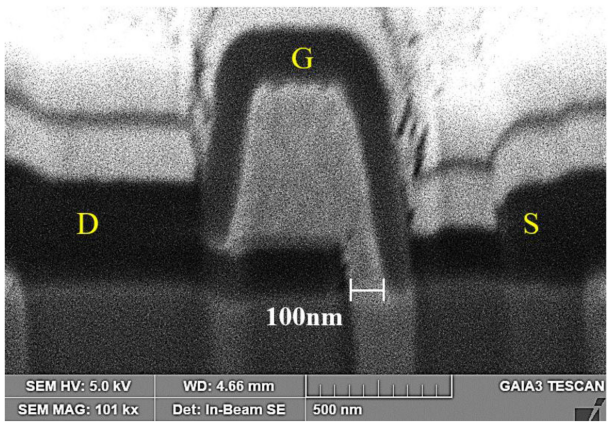


FIGURE 2. SEM image of the gate cross section with gate length of 100 nm.

begins with a shifted gate mask, which is the patterning of the 2nd photoresist layer. Finally, a small opening in the etched SiN_x (Position 2) is defined by the 2nd stepper lithography process. Gate formation was completed by the deposition of Ni/Au stack metal using E-gun. SiN_x passivation layer was grown by the PECVD to protect the wafer surface [13] after gate metal deposition. To reduce the skin effect at high frequency operation, 2μm thick metal interconnects were evaporated on the device contact pads.

The SEM image of the gate is shown in Fig. 2. The bottom of the gate is firmly deposited on the 100 nm opening and the top L_G distribution is defined by the lateral etching of SiN_x

layers [14]. The charges accumulated on the SiN_x surface edges may deflect the incoming ions, leaving a trapezoidal-shaped top gate [15].

III. RESULTS AND DISCUSSION

The I_{DS}-V_{GS}, I_{DS}-V_{DS} and pulsed I_{DS}-V_{DS}, and the transfer characteristics in semi-log scale at V_{DS}=10 V and 1 V of the 2×25 μm AlGaN/GaN HEMT with a L_G of 100 nm, a source-drain spacing (L_{SD}) of 2.250 μm, a gate-drain spacing (L_{GD}) of 1.425 μm, and a gate-source spacing (L_{GS}) of 0.725 μm, as shown in Fig. 3 (a), (b), and (c) respectively.

With the 2-Step Photolithography Process, a maximum drain-source current density of 1004.2 mA/mm and a peak extrinsic transconductance of 363.6 mS/mm were measured. The AlGaN/GaN HEMT DC performance shows the potential of using the proposed lithography method to realize high RF performance Ka band transistors.

The I_{DS}-V_{DS} curves for the 100-nm device with and without pulsed biases ($V_{GS,Q}$ =0V, $V_{DS,Q}$=0V) have been measured and shown in Fig. 3 (b), which show little current dispersion. The pulsed I_{DS}-V_{DS} measurement has a pulse width of 200 ns and a duty cycle of 0.1%. The applied pulse width of 200 ns is shorter than the time constant of most traps, therefore could eliminate thermal and trap effects [36].

Fig. 3 (d) shows the transfer characteristics in semi-log scale at V_{DS}=10 V and 1 V of the 2×25 μm AlGaN/GaN HEMT. In this study, drain induced barrier lowering (DIBL) is defined as $\Delta V_{th}/\Delta V_{DS}$ with V_{th} defined as the gate voltage at I_{DS}=1 mA/mm. A DIBL value of 15 mV/V is further extracted from V_{DS}=10 V and 1 V, showing an increased DIBL due to smaller gate length and smaller gate-to-channel aspect ratio compared to the 150 nm devices [35].

DC mapping for 2×25 μm devices was done to confirm the high wafer uniformity of the 4-inch wafer fabrication with the Stepper lithography, and is shown in Fig. 5. The I_{DSS}, G_m and V_{th} mapping results were shown in Fig. 4(a), (b), and (c), respectively. More than 85% of the AlGaN/GaN HEMTs on the wafer exhibited an I_{DSS} value between 910 to 1000 mA/mm. More than 90% of the AlGaN/GaN HEMTs on the wafer exhibited a G_m value between 310 to 350 mS/mm and more than 95% of the AlGaN/GaN HEMTs on the wafer exhibited a V_{th} value between −4.0 to −3.4 V. The high uniformity is attributed to both the reproducibility of the Stepper Lithography [10] and the simplicity of the 2-Step Photolithography Process.

The device off-state breakdown voltage is measured as shown in Fig. 10. The three terminal breakdown voltage measurement were done on a 2-step photolithography HEMT device with 2×25 μm gate width, L_{SD}=2.25 μm. The device shows a breakdown voltage at I_{DS}=1 mA/mm of 64 V at off-state (V_{GS}= −5 V), which demonstrates the potential of GaN HEMT device for high power Ka-band applications.

To investigate the RF characteristics of the AlGaN/GaN HEMTs with the 2-Step Photolithography Process,

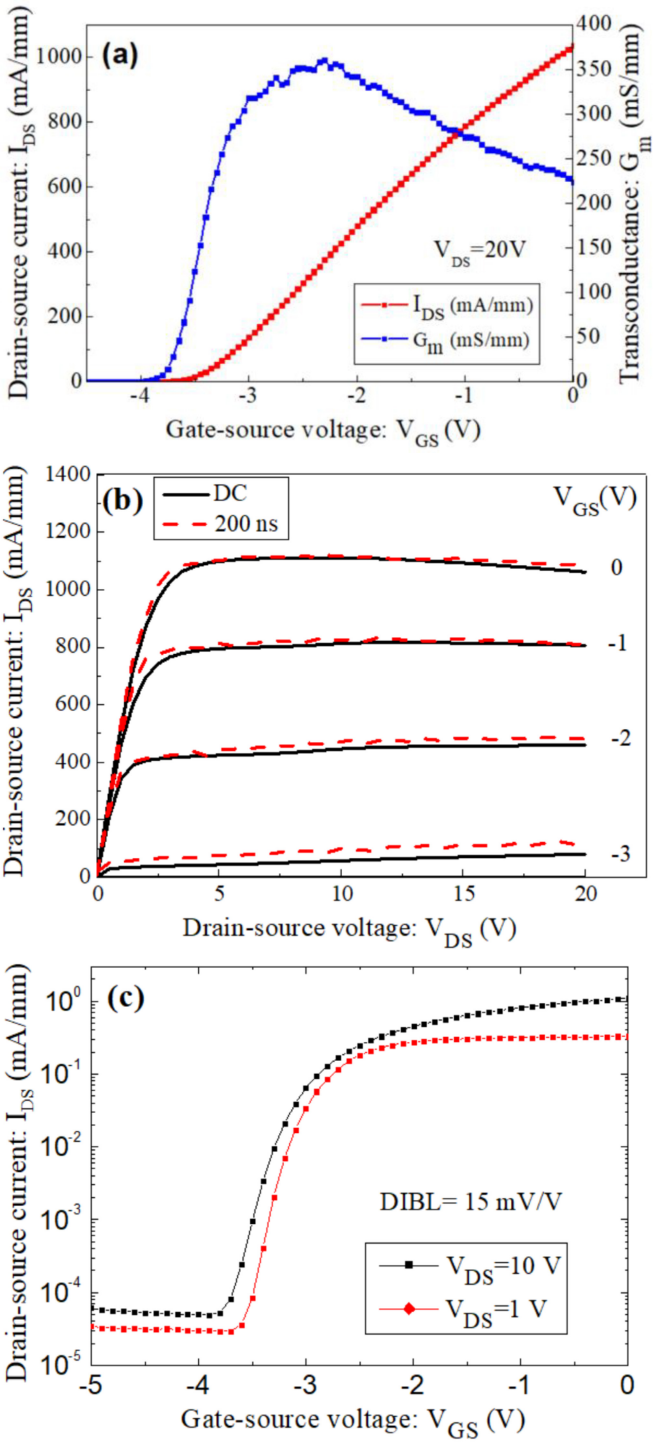


FIGURE 3. (a) I_{DS}-V_{GS}, (b) I_{DS}-V_{DS} and pulsed I_{DS}-V_{DS} curves, and (c) the transfer characteristics in semi-log scale at V_{DS}=10 V and 1 V of the 2×25 μm AlGaN/GaN HEMT.

S parameter results of the AlGaN/GaN HEMT and large signal characteristics of a the AlGaN/GaN HEMT at 28GHz were examined.

S-parameters results were measured on-wafer using the N5227B PNA Microwave Network Analyzer and shown in Fig. 8 after de-embedding. The system was calibrated with a

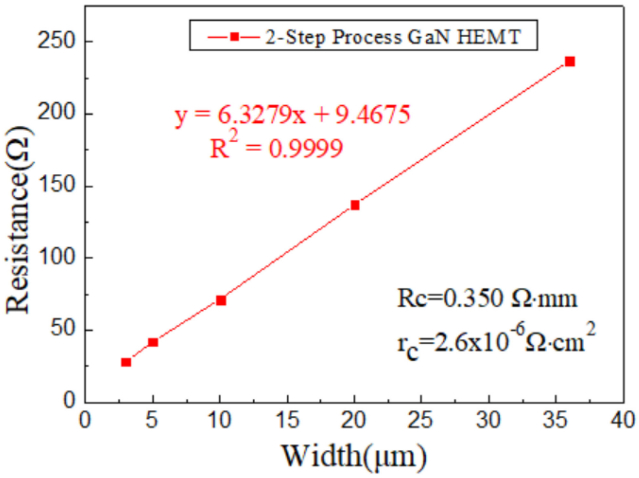


FIGURE 4. **TLM results of the AlGaN/GaN HEMT for the 2-Step Photolithography Process.**

short-open load-through calibration standard. The calibration accuracy was verified by insuring that both S_{21} and S_{12} of the through standard are less than ±0.01 dB and that both S_{11} and S_{22} are less than −45 dB within the measured frequency range after calibration [30].

The current gain cut-off frequency (f_t) of 63 GHz, the unilateral power gain (U) curve, and the maximum oscillation frequency (f_{max}) of 171 GHz for the 2×50 μm AlGaN/GaN HEMT with L_{SD}=2.5 μm using the 2-Step Photolithography Process are shown in Fig. 8.

For large signal characteristics, the 3dB compression point power density ($P_{OUT(P3dB)}$) of 4.3 W/mm, maximum power density ($P_{OUT\ (Pmax)}$) of 10.8 W/mm, and maximum PAE of 51.1% of the 2×25 μm device with L_{SD}=2.25 μm were measured at V_{DS} = 20 V and V_{GS}=−1.58 V (I_{DS}= 460 mA/mm) in Continuous Wave (CW) mode Load Pull measurement, as shown in Fig. 6.

28 GHz CW mode Load-pull measurement tests have also been performed on the 2×50 μm, 8×50 μm, and 8×75 μm devices, as shown in Fig. 7 (a), (b), and (c). The 2×50 μm device with L_{SD}=2.5 μm measured at a bias of V_{DS}=28 V and V_{GS}=−1.66 V (I_{DS}=41.1 mA/mm) exhibits an output power density of 8.1 W/mm. The 8×50 μm device with L_{SD}=2.5 μm measured at a set bias of V_{DS}=28 V and V_{GS}=−2.5 V (I_{DS}=252.5 mA/mm) exhibits an output power of 1.85 W. Moreover, to further increase the output power performances of the 2-Step Process devices, the 8×75 μm device with L_{SD}=3.0 μm and with the increased gate width of 25 μm compared to the 8×50 μm devices have been fabricated and has demonstrated an output power of 2.25 W under 28 GHz load pull measurements with V_{DS}=28 V and V_{GS}=−2.6 V (I_{DS}=233.3 mA/mm).

The RF performance of these devices shows the capability of the 2-Step Photolithography Process to be applied on larger gate periphery devices, while maintaining high wafer yield through a high uniformity analyzation. The decrease of the output power density of the 2-Step devices

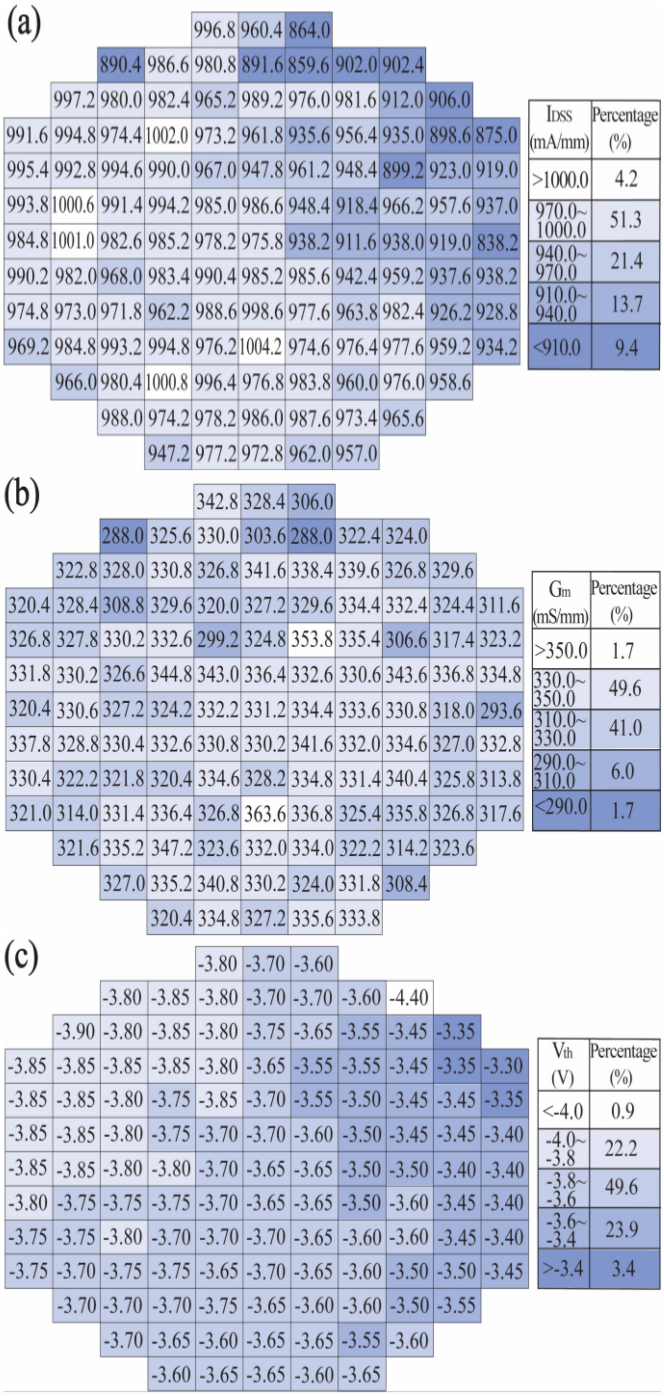


FIGURE 5. **The 4-inch wafer uniformity of a 2×25 μm device on (a) I_{DSS} value, (b) G_m value and (c) V_{th} value.**

with increased device single gate width may result from the increased gate resistance (R_g). The effect of gate width concerning the R_g has been done in detail by Palacios et al. [31]. Palacios et al. shows that for AlGaN/GaN HEMT devices, the R_g scales linearly with the gate width for a device with gate lengths of around 150 nm, and has an important effect on the device RF performances, such as f_{max}.

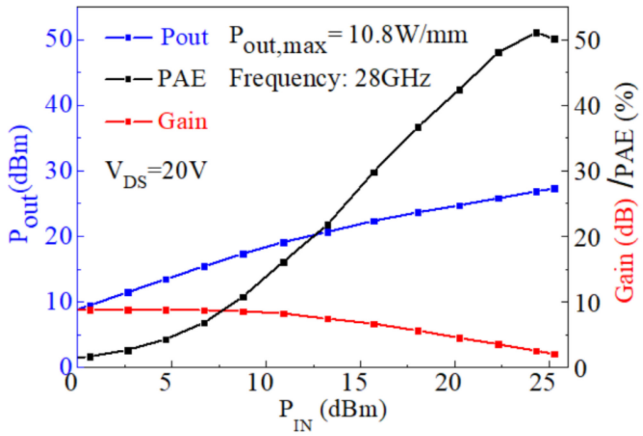


FIGURE 6. Large signal results of a 2×25 μm AlGaN/GaN HEMT for the 2-Step Photolithography Process.

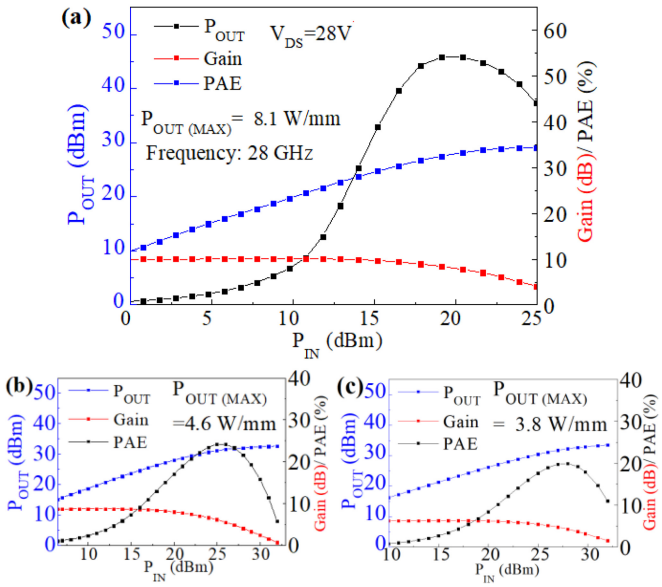


FIGURE 7. Large signal results of the (a) 2×50 μm, (b) 8×50 μm, (c) 8×75 μm AlGaN/GaN HEMTs for the 2-Step Photolithography Process.

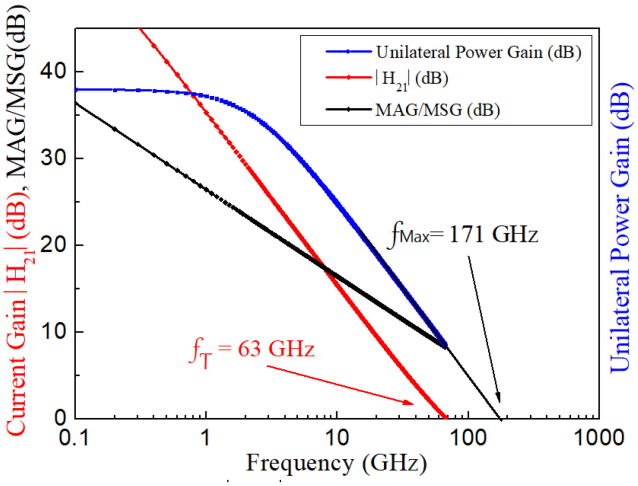


FIGURE 8. Current-gain $|H_{21}|$, unilateral power gain (U), and MAG/MSG vs. Frequency plot for the 2×50 μm AlGaN/GaN HEMT with the 2-Step Photolithography Process.

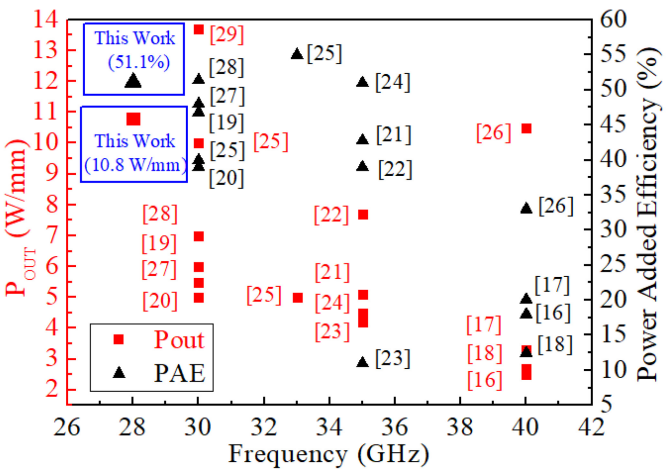


FIGURE 9. Benchmark of the 2-Step device and published results.

The effects of gate width on f_t and f_{max} are also discussed with the small signal of the 2×50 μm and 8×50 μm devices. The f_t and f_{max} values of 43 GHz and 200GHz, respectively, for the 8×50 μm AlGaN/GaN HEMT are shown in Fig. 11.

Compared to the 2×50 μm device in Fig. 8, the 8×50 μm device exhibits a lower f_t value, which may be due to increased gate capacitance from the larger gate width. However, the 8×50 μm device has a higher f_{max} value, which is mainly due to the reduced R_g from increased gate fingers [34].

The decrease of output power density of the devices with more gate fingers in this study may be due to the increase of self-heating effect [32], showing that the increase of self-heating effects with gate fingers during on-wafer measurement reduces the output power density of the SiC MESFET devices, despite the high thermal conductivity of SiC substrates.

The RF power performance of the device with a highest output power density in this study is compared with other published results, as shown in Fig. 9. At Ka-Band, the RF results of a 2×25 μm using the 2-Step Photolithography Process exhibited an outstanding $P_{OUT\ (MAX)}$ among representative published papers. The RF power characteristic shown in this work exhibits over 50% PAE, and a record high output power density of 10.8 W/mm for devices fabricated using only the stepper phtolithography system for L_G definition. Within published Ka band frequency devices [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], the output power density of this work not only standout among state-of-the-art results, but also shows potential for the mass production of high output power density GaN HEMT wafers without using the conventional E-beam lithography system.

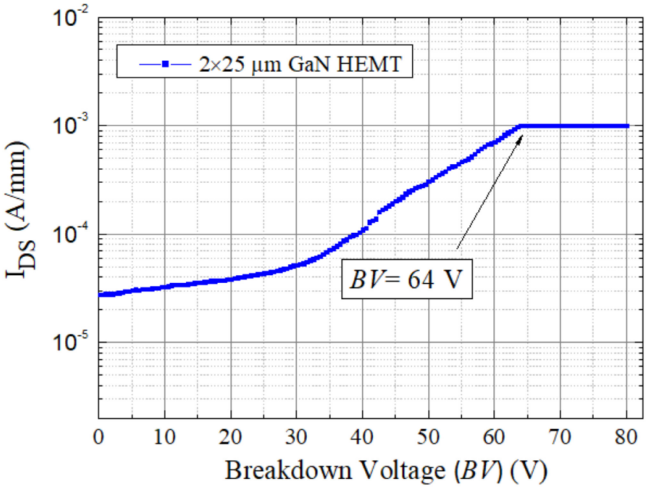


FIGURE 10. **Breakdown Voltage measurement result of the 2×25 μm HEMT device at $V_{GS} = -5$ V.**

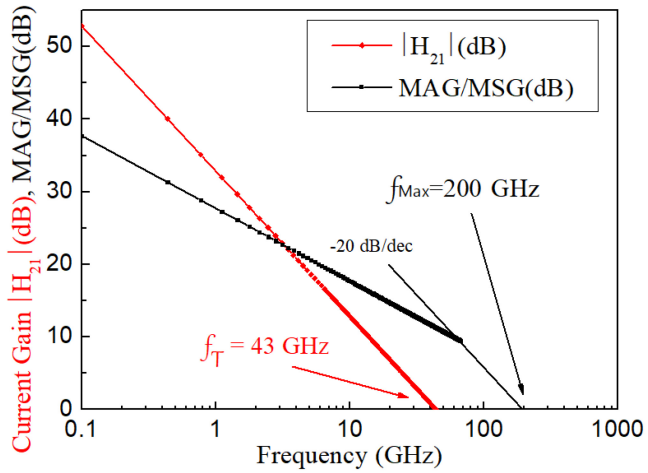


FIGURE 11. **Current-gain $|H_{21}|$ and MAG/MSG vs. Frequency plot for the 8×50 μm AlGaN/GaN HEMT with the 2-Step Photolithography Process.**

IV. CONCLUSION

We have demonstrated AlGaN/GaN HEMTs fabricated by the Stepper Lithography, and with the 2-Step Photolithography Process, we have achieved small gate lengths and achieved high wafer uniformity on the 4-inch wafer with high I_{DSS}, G_m and V_{th} values. At $V_{DS} = 20$ V, the AlGaN/GaN HEMT exhibits an I_{DSS} of 1004.2 mA/mm, a G_m value of 363.6 mS/mm, a maximum output power density ($P_{OUT\ (MAX)}$) of 10.8 W/mm, and a power gain of 8.8 dB with a maximum Power-added efficiency (PAE) of 51.1% at 28 GHz in CW mode. Overall, the high wafer uniformity and the outstanding RF power performance together makes the process applicable for Ka-band device fabrication, and has the potential to mass production on 6- and 8-inch wafers.

REFERENCES

[1] A. Lidow, M. de Rooji, J. Strydom, D. Reusch, and J. Glaser, *GaN Transistors for Efficient Power Conversion* (1.3 GaN and SiC Compared with Silicon), 3rd ed. Hoboken, NJ, USA: Wiley, 2020, p. 2.

[2] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, "GaN-based RF power devices and amplifiers," *Proc. IEEE*, vol. 96, no. 2, pp. 287–305, Feb. 2008, doi: 10.1109/JPROC.2007.911060.

[3] Y. C. Lin et al., "Enhancement-mode GaN MIS-HEMTs with LaHfOx gate insulator for power application," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1101–1104, Aug. 2017, doi: 10.1109/LED.2017.2722002.

[4] Y.-C. Lin, C.-H. Chang, F.-M. Li, L.-H. Hsu, and E. Y. Chang, "Evaluation of TiN/Cu gate metal scheme for AlGaN/GaN high-electron-mobility transistor application," *Appl. Phys. Exp.*, vol. 6, Sep. 2013, Art. no. 91003, doi: 10.7567/APEX.6.091003.

[5] J.-N. Yao et al., "Evaluation of a 100-nm gate length E-mode InAs high electron mobility transistor with Ti/Pt/Au ohmic contacts and mesa sidewall channel etch for high-speed and low-power logic applications," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 797–802, 2018, doi: 10.1109/JEDS.2018.2853547.

[6] S.-J. Yeon, M. Park, and K.-S. Seo, "Novel sloped etch process for 15nm InAlAs/InGaAs metamorphic HEMTs," in *Proc. 7th IEEE Conf. Nanotechnol. (IEEE NANO)*, 2007, pp. 1152–1155, doi: 10.1109/NANO.2007.4601387.

[7] Y.-C. Lin et al., "Study of the mesa etched tri-gate InAs HEMTs with extremely low SS for low-power logic applications," in *Proc. China Semicond. Technol. Int. Conf. (CSTIC)*, 2018, pp. 1–3, doi: 10.1109/CSTIC.2018.8369315.

[8] S. Arulkumaran, G. I. Ng, and S. Vicknesh, "Enhanced breakdown voltage with high Johnson's figure-of-merit in 0.3-$\mu{\rm m}$ T-gate AlGaN/GaN HEMTs on silicon by $({\rm NH}_{4})_{2}{\rm S}_{x}$ treatment," *IEEE Electron Device Lett.*, vol. 34, no. 11, pp. 1364–1366, Nov. 2013, doi: 10.1109/LED.2013.2279882.

[9] J. Xu, S. Zhang, P. Zheng, R. Wang, and X. Tong, "Non-ebeam AlGaN/GaN HEMTs with $f_{\max}$ of 206 GHz for mass production," in *Proc. Int. Conf. Microw. Millimeter Wave Technol. (ICMMT)*, 2019, pp. 1–3, doi: 10.1109/ICMMT45702.2019.8992212.

[10] S. V. Sreenivasan, "Nanoimprint lithography steppers for volume fabrication of leading-edge semiconductor integrated circuits," *Microsyst. Nanoeng.*, vol. 3, Sep. 2017, Art. no. 17075, doi: 10.1038/micronano.2017.75.

[11] J.-E. Muller et al., "A GaAs HEMT MMIC chip set for automotive radar systems fabricated by optical stepper lithography," *IEEE J. Solid-State Circuits*, vol. 32, no. 9, pp. 1342–1349, Sep. 1997, doi: 10.1109/4.628737.

[12] R. Chu et al., "Impact of $\hbox{CF}_{4}$ plasma treatment on GaN," *IEEE Electron Device Lett.*, vol. 28, no. 9, pp. 781–783, Sep. 2007, doi: 10.1109/LED.2007.902849.

[13] A. Ouacha, M. Willander, B. Hammarlund, and R. A. Logan, "Effect of surface passivation with SiN on the electrical properties of InP/InGaAs heterojunction bipolar transistors," *J. Appl. Phys.*, vol. 74, no. 9, pp. 5602–5605, 1993, doi: 10.1063/1.354221.

[14] D. Xu et al., "0.1- μm InAlN/GaN high electron-mobility transistors for power amplifiers operating at 71–76 and 81–86 GHz: Impact of passivation and gate recess," *IEEE Trans. Electron Devices*, vol. 63, no. 8, pp. 3076–3083, Aug. 2016, doi: 10.1109/TED.2016.2579160.

[15] I. W. Rangelow, "Critical tasks in high aspect ratio silicon dry etching for microelectromechanical systems," *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 21, no. 4, pp. 1550–1562, Jul. 2003, doi: 10.1116/1.1580488.

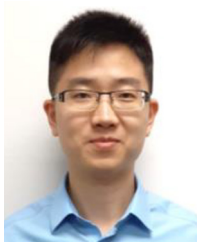
[16] F. Medjdoub, M. Zegaoui, B. Grimbert, D. Ducatteau, N. Rolland, and P. A. Rolland, "First demonstration of high-power GaN-on-silicon transistors at 40 GHz," *IEEE Electron Device Lett.*, vol. 33, no. 8, pp. 1168–1170, Aug. 2012, doi: 10.1109/LED.2012.2198192.

[17] A. Soltani et al., "Power performance of AlGaN/GaN high-electron-mobility transistors on (110) silicon substrate at 40 GHz," *IEEE Electron Device Lett.*, vol. 34, no. 4, pp. 490–492, Apr. 2013, doi: 10.1109/LED.2013.2244841.

[18] P. Altuntas et al., "Power performance at 40 GHz of AlGaN/GaN high-electron mobility transistors grown by molecular beam epitaxy on Si(111) substrate," *IEEE Electron Device Lett.*, vol. 36, no. 4, pp. 303–305, Apr. 2015, doi: 10.1109/LED.2015.2404358.

[19] M. Mi et al., "Millimeter-wave power AlGaN/GaN HEMT using surface plasma treatment of access region," *IEEE Trans. Electron Devices*, vol. 64, no. 12, pp. 4875–4881, Dec. 2017, doi: 10.1109/TED.2017.2761766.

[20] R. Aubry et al., "ICP-CVD SiN passivation for high-power RF InAlGaN/GaN/SiC HEMT," *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 629–632, May 2016, doi: 10.1109/LED.2016.2540164.
[21] Y. Zhang et al., "High-temperature-recessed millimeter-wave AlGaN/GaN HEMTs with 42.8% power-added-efficiency at 35 GHz," *IEEE Electron Device Lett.*, vol. 39, no. 5, pp. 727–730, May 2018, doi: 10.1109/LED.2018.2822259.
[22] R. C. Fitch et al., "Implementation of high-powerdensity *X*-band AlGaN/GaN high electron mobility transistors in a millimeter-wave monolithic microwave integrated circuit process," *IEEE Electron Device Lett.*, vol. 36, no. 10, pp. 1004–1007, Oct. 2015, doi: 10.1109/LED.2015.2474265.
[23] H. Zhou et al., "DC and RF performance of AlGaN/GaN/SiC MOSHEMTs with deep sub-micron T-gates and atomic layer epitaxy MgCaO as gate dielectric," *IEEE Electron Device Lett.*, vol. 38, no. 10, pp. 1409–1412, Oct. 2017, doi: 10.1109/LED.2017.2746338.
[24] M.-Y. Kao, C. Lee, R. Hajji, P. Saunier, and H.-Q. Tserng, "AlGaN/GaN HEMTs with PAE of 53% at 35 GHz for HPA and multi-function MMIC applications," in *IEEE/MTT-S Int. Microw. Symp. Tech. Dig.*, 2007, pp. 627–629, doi: 10.1109/MWSYM.2007.379979.
[25] J. S. Moon et al., "55% PAE and high power Ka-band GaN HEMTs with linearized transconductance via $\hbox{n}+$ GaN source contact ledge," *IEEE Electron Device Lett.*, vol. 29, no. 8, pp. 834–837, Aug. 2008, doi: 10.1109/LED.2008.2000792.
[26] T. Palacios et al., "High-power AlGaN/GaN HEMTs for Ka-band applications," *IEEE Electron Device Lett.*, vol. 26, no. 11, pp. 781–783, Nov. 2005, doi: 10.1109/LED.2005.857701.
[27] J.-S. Moon et al., "Power scaling of graded-channel GaN HEMTs with mini-field-plate T-gate and 156 GHz f_T," *IEEE Electron Device Lett.*, vol. 42, no. 6, pp. 796–799, Jun. 2021, doi: 10.1109/LED.2021.3075926.
[28] S. Zhang et al., "7.05 W/mm power density millimeter-wave GaN MIS-HEMT with plasma enhanced atomic layer deposition SiN dielectric layer," *IEEE Electron Device Lett.*, vol. 42, no. 10, pp. 1436–1439, Oct. 2021, doi: 10.1109/LED.2021.3105817.
[29] Y.-F. Wu et al., "High-voltage millimeter-wave GaN HEMTs with 13.7 W/mm power density," in *Proc. IEEE Int. Electron Devices Meeting*, 2007, pp. 405–407, doi: 10.1109/IEDM.2007.4418958.
[30] D.-H. Kim and J. A. del Alamo, "30-nm InAs pseudomorphic HEMTs on an InP substrate with a current-gain cutoff frequency of 628 GHz," *IEEE Electron Device Lett.*, vol. 29, no. 8, pp. 830–833, Aug. 2008, doi: 10.1109/LED.2008.2000794.
[31] T. Palacios et al., "Optimization of AlGaN/GaN HEMTs for high frequency operation," *Physica Status Solidi*, vol. 203, pp. 1845–1850, May 2006. [Online]. Available: https://doi.org/10.1002/pssa.200565384
[32] W. Liu, C. M. Zetterling, and M. Ostling, "Thermal-issues for design of high power SiC MESFETs," in *Proc. 6th IEEE CPMT Conf. High Density Microsyst. Des. Packag. Compon. Failure Anal. (HDP)*, Shanghai, China, 2004, pp. 331–335, doi: 10.1109/HPD.2004.1346722.
[33] Y.-W. Lien et al., "GaN technologies for applications from L- to Ka-band," in *Proc. IEEE Int. Conf. Microw. Antennas Commun. Electron. Syst. (COMCAS)*, Tel-Aviv, Israel, 2017, pp. 1–5, doi: 10.1109/COMCAS.2017.8244831.
[34] G. Crupi, A. Raffo, V. Vadalà, G. Vannini, D. M. M.-P. Schreurs, and A. Caddemi, "Scalability of multifinger HEMT performance," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 9, pp. 869–872, Sep. 2020, doi: 10.1109/LMWC.2020.3012181.
[35] K. Ranjan, S. Arulkumaran, G. I. Ng, and S. Vicknesh, "High Johnson's figure of merit (8.32 THz·V) in 0.15-μm conventional T-gate AlGaN/GaN HEMTs on silicon," *Appl. Phys. Exp.*, vol. 7, no. 4, 2014, Art. no. 44102, doi: 10.7567/APEX.7.044102.
[36] F. Medjdoub, D. Ducatteau, M. Zegaoui, B. Grimbert, N. Rolland, and P.-A. Rolland, "Trapping effects dependence on electron confinement in ultrashort GaN-on-Si high-electron-mobility transistors," *Appl. Phys. Exp.*, vol. 5, no. 3, Mar. 2012, Art. no. 34103, doi: 10.1143/APEX.5.034103.



MING-WEN LEE (Graduate Student Member, IEEE) was born in Taipei City, Taiwan. He received the B.S. degree in material science and engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2017. He is currently pursuing the Ph.D. degree with the International College of Semiconductor Technology, National Yang Ming Chiao Tung University, Hsinchu, Taiwan, and the Ph.D. degree in doctorate programme in information and communication technologies with the University of Granada, Spain, and enrolled in the Cotutelle Agreement signed between both Universities.

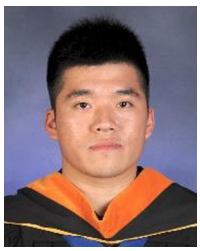
His research interest includes small gate length and high RF linearity AlGaN/GaN HEMT device design and fabrication for Ka Band wireless communication and GaN HEMT TCAD simulation.

YUEH-CHIN LIN was born in Taipei City, Taiwan. He received the B.S. degree in nuclear engineering and engineering physics and the M.S. degree in electrical engineering from Tsing Hua University, Hsinchu, Taiwan, in 1996 and 2000, respectively, and the Ph.D. degree from materials science and engineering, National Chiao Tung University, Hsinchu, in 2006.

From 2004 to 2006, he was with NTT Basic Research Laboratories, where he investigated the growth of AlGaSb/InAs HEMT on Si substrate by molecular beam epitaxy. He is currently a Postdoctoral Fellow with the Department of Materials Science and Engineering and Microelectronics and Information Systems Research Center, NYCU. His research interests include MBE material growth and HEMT device design and fabrication for wireless communication.

PO-SHENG CHANG was born in Kaohsiung, Taiwan. He received the B.S. degree in electronics and electrical engineering and the M.S. degree in lighting and energy photonics from National Chiao Tung University, Hsinchu, Taiwan, in 2013 and 2019, respectively.

His research interest includes HEMT device design and fabrication for wireless communication.



YI-FAN TSAO (Member, IEEE) received the B.S. degree in electro-physics from National Chiao Tung University, Hsinchu, Taiwan, in 2016, the M.S. degree in electrical engineering from the University of California at Los Angeles, Los Angeles, CA, USA, in 2018, and the Ph.D. degree in electrical and computer engineering from Technische Universität Berlin, Berlin, Germany, in 2022. He is currently with the International College of Semiconductor Technology, National Yang Ming Chiao Tung University, Hsinchu. His research interests include millimeter-wave circuit and RF front-end transceiver design.

HENG-TUNG HSU (Senior Member, IEEE) received the B.S. and M.S. degrees in electronics engineering from the National Chiao Tung University, Hsinchu, Taiwan, in 1993 and 1995, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Maryland at College Park, MD, USA, in 2002.

From 2002 to 2005, he was appointed as the Director of Engineering, AMCOM Communications, USA, mainly in charge of the design and development of monolithic microwave integrated circuits for wireless communication systems. From 2006 to 2015, he was with the Department of Communication Engineering, Yuan Ze University, Taiwan. In 2015, he joined the International College of Semiconductor Technology in National Chiao Tung University, Taiwan, where he is currently a Professor and the Deputy Dean. He has authored or coauthored more than 90 journal papers and held three U.S. patents. His research interest includes the design and implementation of RF front-ends, antennas, active and passive microwave components, and RF packaging.

Dr. Hsu was the recipient of the 2012 Y. Z. Hsu's Outstanding Professor Award and received the Silver Medal Award for 2014 Taipei International Invention Show and Technomart.

CHANG-FU DEE received the B.Sc. and M.Sc. degrees in physics from the University of Malaya and the Ph.D. degree in electronic engineering from the Institute of Microengineering and Nanoelectroics (IMEN), Universiti Kebangsaan Malaysia.

He joined the Institute of Microengineering and Nanoelectronics, Universiti Kebangsaan Malaysia in 2004, as a Research Officer and a Research Fellow in 2006. He has been actively involved in the Nanostructures growth Si, ZnO, CuO and SnO2, Molecular Beam Epitaxy, Compound semiconductor, GaAs, PHEMT, HEMT Crystal growth simulation, and Monte Carlo simulation of crystal growth in the IMEN. His research focus is in the area of microelectronics and nanoelectronics materials and devices design for electronics, functional sensor, and actuator applications. These includes the synthesis, fabrication, and characterization of nano-structured metal oxide and epitaxial growth of high-speed compound semiconductor layers. He is a Principal Investigator for FEWS Research Projects mainly in the areas of nano materials.

EDWARD YI CHANG (Life Fellow, IEEE) received the Ph.D. degree from the University of Minnesota, Minneapolis, in 1985. He worked with Unisys Corporation and Comsat Labs, USA from 1985 to 1992. In 1992, he joined National Chiao Tung University, Hsinchu, Taiwan. He is currently the Chair Professor with the Department of Material Science and Engineering, the International College of Semiconductor Technology, and the Department of Electronics Engineering, National Yang Ming Chiao Tung University, Taiwan. He is also a Professor with the Institute of Microengineering and Nanoelectronics, Universiti Kebangsaan Malaysia. He holds more than 40 patents worldwide and has been authored or co-authored of more than 250 journal papers in the related research areas. His current research interests include III-V and GaN based devices for logic, high frequency and power applications. He is a JSAP Fellow International, a TMRS Fellow, and a Distinguished Lecturer of the IEEE Electron Devices Society.