UNIVERSIDAD DE GRANADA

THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Design and assessment of 2D material-based radiofrequency circuits

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Abstract

In the rapidly evolving landscape of modern technology, the unprecedented expansion of connectivity and communication demands innovative solutions. The advanced requirements of 5G and future wireless communication systems, along with the proliferation of Internet of Things (IoT) devices, are increasingly constrained by the physical limitations of conventional electronic technologies. Consequently, the exploration of novel emerging materials has become a crucial focus of research over the past two decades, driving the development of next-generation high-frequency (HF) electronics.

Within this search, graphene, a two-dimensional material with great mechanical and electrical properties, has revolutionized the electronic research world since its isolation for the first time in 2004. Thanks to its high carrier mobility and saturation velocity, it has been proofed to be a great candidate for the development of HF circuits, able to provide high cutoff and maximum oscillation frequencies, two figures of merit that evaluate the HF performance of a transistor.

In this context, this Thesis presents the design and assessment of two-dimensional (2D) material-based radiofrequency (RF) circuits. The goal of the Thesis consists in demonstrating different RF building-block circuits that profit and exploit the unique properties of graphene for HF electronics, making use of two graphene-based electronic devices: the graphene field-effect transistor (GFET), and the metal-insulator-graphene (MIG) diode. More specifically, this Thesis demonstrates the analysis, design, and validation of phase shifters, power gain amplifiers, frequency multipliers and oscillators.

For the phase shifter designs, one of the special properties of graphene, the so-called graphene's quantum capacitance tunability, is used, allowing to change the capacitance of the device, either in a GFET or a MIG diode, with respect to the applied voltage. For the design, two different topologies are proposed: in the case of the GFET, a common-source amplifier topology is adopted, where 3D maps of the transmission S parameter with respect to drain to source and gate to source potentials are represented, showing the ability to produce a phase shift on the input signal while keeping its amplitude constant, and even providing gain. In the case of the MIG diode, a periodic structure topology is proposed: a novel analysis of this type of structures is first shown, exposing how the response of the structure can be controlled with the aim of maximizing the phase shift, while keeping a minimum insertion loss (IL). The topology can also be partially used in different circuit topologies like filters.

With respect to the power gain amplifier design, the objective is to demonstrate the ability of GFETs to provide power gain at high frequencies even when their voltage gain is lower than unity, due to the lack of a clear saturation region. For that matter, the gain expressions used in the high frequency design procedures, such as the maximum

available gain and the maximum stable gain, have been thoroughly analyzed, and it has been shown that the dependence of the power gain on the output conductance is not as strong as it is commonly considered. GFET-based power gain amplifier designs providing HF power gain with the devices working at different high and low values of the output conductance are demonstrated.

Graphene's ambipolarity is also leveraged for a frequency multiplier design. First, it is shown that it is possible to attain a frequency doubler by applying an input signal at the gate of the GFET, if properly biased at the Dirac point, due to its V-shaped transfer curve. Furthermore, the Dirac point shift is unveiled to depend on the drain plus the source voltage, which displaces the minimum conduction point of the transfer curve. This effect is exploited by series connecting two GFETs with a resistor in the middle, which thus produces a different Dirac point on each transistor, producing a W-shaped transfer curve in the circuit, which enables frequency tripling and quadrupling.

Finally, the design of a negative-resistance oscillator is demonstrated. This design, addressed during a research stay at Chalmers University of Technology, demonstrates the ability of GFETs to provide enough instability so to design an oscillator, which is an indispensable block in any wireless transmitter or receiver. The circuit is designed in the X-band, at $10\,\mathrm{GHz}$, and includes a feedback inductor so as to increase the instability of the transistor, a purely reactive terminating impedance, in order to minimize power consumption, and a matching network which also serves as a low pass filter in order to reduce higher order harmonics.

In addition to the design work, both devices used for the designs have been fabricated and characterized as part of the development of the Thesis. In particular, GFETs were fabricated through a research collaboration as part of an European project, the 2D Experimental Pilot Line (2DEPL), and then characterized at the facilities of the Pervasive Electronics Advanced Research Laboratory (PEARL), and for the MIG diode, the fabrication was self-made during a research stay at the non-profit research company AMO GmbH in Aachen, Germany. Devices theoretical description, fabrication process and characterization is addressed.

In conclusion, this Thesis shows the possibility of designing RF circuits with graphene-based devices, namely GFETs, and MIG diodes, paving the way towards the realization of complete RF systems in this technology.

Resumen

En el panorama en rápida evolución de la tecnología moderna, la expansión sin precedentes de la conectividad y la comunicación exige soluciones innovadoras. Los avanzados requisitos de las redes 5G y de los sistemas de comunicación inalámbrica futuros, junto con la proliferación de dispositivos del Internet de las Cosas (IoT, por sus siglas en inglés), están cada vez más limitados por las restricciones físicas de las tecnologías electrónicas convencionales. En consecuencia, la exploración de nuevos materiales emergentes se ha convertido en un punto crucial de investigación durante las últimas dos décadas, impulsando el desarrollo de la próxima generación de electrónica de alta frecuencia (HF, por sus siglas en inglés).

Dentro de esta búsqueda, el grafeno, un material bidimensional con excelentes propiedades mecánicas y eléctricas, ha revolucionado el mundo de la investigación electrónica desde su aislamiento por primera vez en 2004. Gracias a su alta movilidad de portadores y velocidad de saturación, se ha demostrado que es un excelente candidato para el desarrollo de circuitos de HF, capaces de proporcionar altas frecuencias de corte y de oscilación máxima, dos figuras de mérito que evalúan el rendimiento en alta frecuencia de un transistor.

En este contexto, esta Tesis presenta el diseño y evaluación de circuitos de radiofrecuencia (RF) basados en materiales bidimensionales (2D). El objetivo de la Tesis consiste en demostrar diferentes circuitos fundamentales de RF que aprovechen y exploten las propiedades únicas del grafeno para la electrónica de alta frecuencia, utilizando dos dispositivos electrónicos basados en grafeno: el transistor de efecto de campo de grafeno (GFET, por sus siglas en inglés) y el diodo metal-aislante-grafeno (MIG, por sus siglas en inglés). Más específicamente, se demuestra el análisis, diseño y validación de desfasadores, amplificadores de ganancia de potencia, multiplicadores de frecuencia y osciladores.

Para el diseño de los desfasadores, se utiliza una de las propiedades del grafeno, la llamada sintonización de la capacidad cuántica del grafeno, que permite la modificación de la capacidad del dispositivo, ya sea en un GFET o en un diodo MIG, en función del voltaje aplicado. Para el diseño, se proponen dos topologías diferentes: en el caso del GFET, se adopta una topología de amplificador de fuente común, donde se representan mapas 3D del parámetro S con respecto a los potenciales de drenador a fuente y de puerta a fuente, mostrando la posibilidad de producir un cambio de fase en la señal de entrada mientras se mantiene constante su amplitud e incluso proporcionando ganancia. En el caso del diodo MIG, se propone una topología de estructura periódica: primero se muestra un novedoso análisis de este tipo de estructuras, exponiendo cómo se puede controlar la respuesta de la estructura con el objetivo de maximizar el cambio de fase,

manteniendo una mínima pérdida de inserción (IL). La topología planteada también puede ser utilizada en diferentes tipos de circuitos, como por ejemplo en el diseño de filtros.

Con respecto al diseño del amplificador, el objetivo es demostrar la capacidad de los GFETs para proporcionar ganancia de potencia a altas frecuencias, incluso cuando, debido a la falta de una región de saturación, su ganancia de voltaje es inferior a la unidad. Para ello, se han analizado en detalle las expresiones de ganancia utilizadas en los procedimientos de diseño de alta frecuencia, como la ganancia máxima disponible y la ganancia máxima estable, y se ha demostrado que su dependencia con respecto a la conductancia de salida no es tan fuerte como se considera comúnmente. Así, se demuestran diseños de amplificadores basados en GFETs que proporcionan ganancia de potencia a alta frecuencia para valores distintos, altos y bajos, de la conductancia de salida.

La ambipolaridad del grafeno también se aprovecha para el diseño de un multiplicador de frecuencia. En primer lugar, se demuestra que es posible implementar un doblador de frecuencia aplicando una señal de entrada en la puerta del GFET, si se polariza adecuadamente en el punto de Dirac, debido a su curva de transferencia en forma de V. Además, se muestra que el desplazamiento del punto de Dirac depende de la suma del voltaje de drenador y de fuente, lo que desplaza el punto de mínima conducción de la curva de transferencia. Este efecto se explota conectando en serie una resistencia entre dos GFETs, lo que produce un punto de Dirac diferente en cada transistor, dando lugar a una curva de transferencia en forma de W en el circuito. Polarizando adecuadamente, esto permite triplicar y cuadruplicar la frecuencia de entrada.

Finalmente, se demuestra un oscilador de resistencia negativa. Este diseño, abordado durante una estancia de investigación en la Universidad Tecnológica de Chalmers, demuestra la capacidad de los GFETs para proporcionar suficiente inestabilidad para diseñar un oscilador, un bloque indispensable en cualquier transmisor o receptor inalámbrico. El circuito se diseña en la banda X, a 10 GHz, e incluye una bobina de realimentación para aumentar la inestabilidad del transistor, una impedancia terminal puramente reactiva, para minimizar el consumo de potencia, y una red de adaptación que también actúa como un filtro paso bajo para reducir los armónicos de orden superior.

Además del trabajo de diseño, ambos dispositivos utilizados para los diseños han sido fabricados y caracterizados como parte del desarrollo de la Tesis. En particular, los GFETs se fabricaron a través de una colaboración de investigación como parte de un proyecto europeo, la 2D Experimental Pilot Line (2DEPL), y luego se caracterizaron en las instalaciones del Laboratorio de Investigación Avanzada en Electrónica Pervasiva (PEARL, por sus siglas en inglés), y para el diodo MIG, la fabricación se realizó de manera autónoma durante una estancia de investigación en la empresa de investigación sin ánimo de lucro AMO GmbH en Aquisgrán, Alemania. Se aborda la descripción teórica de los dispositivos, el proceso de fabricación y su caracterización.

En conclusión, esta Tesis muestra la posibilidad de diseñar circuitos de RF con dispositivos basados en grafeno, a saber, GFETs y diodos MIG, allanando el camino hacia la realización de sistemas RF completos en esta tecnología.

Acronyms

1D one-dimensional.

2D two-dimensional.

2D-EPL 2D Experimental Pilot Line.

ADS advanced design system.

ALD atomic layer deposition.

BOIP Benelux Office for Intellectual Property.

CAD computer-aided design.

Cu copper.

CVD chemical vapor deposition.

DD drift-diffusion.

DI deionized.

DIBL drain-induced barrier lowering.

DPS Dirac point shift.

FET field-effect transistor.

GFET graphene field-effect transistor.

GSG ground-signal-ground.

h-BN hexagonal boron nitride.

HEMT high electron mobility transistor.

HF high-frequency.

IC integrated circuit.

IP intelectual property.

IPA isopropanol.

IR image reversal.

MFP mean-free-path.

MIG metal-insulator-graphene.

MIM metal-insulator-metal.

MoS_2 molybdenum disulfide.

MOSFET metal-oxide-semiconductor field-effect transistor.

MPW multi-project wafer.

PEB post exposure bake.

PMMA poly(methyl methacrylate).

QAM quadrature amplitude modulation.

RF radiofrequency.

RIE reactive-ion etching.

SBH Schottky barrier height.

SCE short-channel effects.

Si silicon.

SMU source measure unit.

SWR standing wave ratio.

TC transfer characteristic.

TL transmission line.

TMDC transition metal dichalcogenide.

TRL technology readiness level.

UV ultraviolet.

VGA variable-gain amplifier.

WSe_2 tungsten diselenide.

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Part I.

Introduction

Chapter 1. Introduction

1.1. Introduction

The exponential growth of data traffic and the insatiable demand for faster, more powerful wireless devices drive the relentless pursuit of miniaturized, high-performance electronics [1]. For decades, the semiconductor industry has relied upon the remarkable properties of silicon (Si) to enable the downscaling of transistors, in line with Moore's Law [2]. However, as conventional Si-based devices approach fundamental physical limits, their ability to operate at increasing frequencies with acceptable power and efficiency diminishes [3]. The inherent bottlenecks associated with the downscaling of Si-based electronics have instigated a paradigm shift in materials research, leading to the emergence of novel materials with the potential to revolutionize the landscape of the electronic industry [4].

The isolation of graphene for the first time in 2004 [5] and the subsequent demonstration of the first GFET [6] signified a turning point on the search for alternatives to conventional Si-based devices. Graphene, a single-atom-thick sheet of carbon atoms arranged in a honeycomb lattice, exhibited extraordinary carrier mobility [7], unmatched thermal conductivity [8], and superior mechanical strength [9]. These unique characteristics positioned it as a compelling candidate for the development of ultra-fast, energy-efficient, and flexible electronics [10].

Since then until now, the research community has made great efforts in using graphene for a wide range of applications. One of the major responsible for this research boost was the release in 2013 of the greatest European joint research project "Graphene Flagship", which created a vast network of 118 academic and industrial partners focusing on embracing and developing graphene research in its fullness [11]. This ambitious effort spanning multiple research projects in several disciplines, aimed at securing Europe's position as a global leader in graphene-based innovation. As a result of this and other external research endeavours, not only has our understanding of graphene broaden at an academic level but also has it translated into tangible results for the industry, as the funding of new companies whose core product portfolio is based on graphene, like Graphenea or Grolltex.

Indeed, graphene has found several fields of applications outside the electronics. Some examples are water filtering applications in order to remove heavy metals, which is currently being studied in the GRAPHIL project [12], in the automotive industry in

order to increase CO_2 capturing levels or helping with heat distribution, in the biomedical domain due to its functionalization possibilities which can help in detecting certain molecules or viruses, in the aeronautics sector improving the functionality of plane parts by enabling their construction to be thinner and lighter, or for composites and coatings in the building industry by enhancing the properties of concrete, as stated in [13].

One of the main differences found on this wide range of graphene applications is the method used for synthesising the graphene, which ultimately determines its cost, its quality and the scalability of the process [14]. While low-quality graphene is enough for some applications, in order to build electronic devices, where a high mobility is critical, it is essential to use fabrication techniques that yield a very high-quality graphene. As of today, two synthesis techniques for obtaining high-quality graphene are commonly used: exfoliated graphene [15] and chemical vapor deposition (CVD)-grown graphene on copper (Cu)-foil [16]. Despite exfoliation providing higher mobilities, CVD is commonly the preferred method due to its scalability [17], allowing already its transfer at wafer-scale.

In the electronics realm, it was early observed the unique X-shaped band structure of graphene, with its valence and conduction bands touching in only one point, the so-called Dirac point. This gapless structure is the reason for some of its most standing properties (e.g., extraordinarily high carrier mobilities), but also prevents graphene-based transistors from being effectively turned off, which soon eliminated them as candidates for digital circuitry [18]. With the aim of solving this, the use of bilayer graphene (two graphene layers one on top of the other) was suggested, as a bandgap can be opened as a result of a perpendicular electric field applied to the material [19]. However, it also degrades the mobility [20], frustrating one of the most noteworthy properties of graphene. In the recent years, the research on this area has focused on the use of transition metal dichalcogenides (TMDCs) such as molybdenum disulfide (MoS_2) or tungsten diselenide (WSe_2) which, also being two-dimensional materials, naturally exhibit a bandgap and can be thus inherently exploited for digital electronics [21], [22].

After the initial hype that came with the discovery of graphene and its outstanding properties, a change in the way graphene had been thought up to that point was needed: from assuming it would be the Si sucesor to thinking of it as a complementary technology that could be used in some specific applications where its properties could be maximized. Graphene's unprecedented observed mobility and saturation velocity presumed a great performance in the field of high frequency analog circuits, where how good the transistor turns off is not anymore the way to evaluate its performance, and instead a quick carrier response to an applied high-frequency (HF) signal is desired.

The rest of the chapter is organized as follows: section 1.2 discusses on the two main graphene-based devices used in this Thesis, namely the GFET and the MIG diode, and section 1.3 shows the scope and outline of the Thesis.

1.2. Graphene-based devices for high-frequency electronics

The high carrier mobility and saturation velocity postulate graphene as a promising material for radiofrequency (RF) circuits, predicting high operation frequencies. In fact, some graphene-based RF circuits can already be found in the literature. Some examples are amplifiers, power detectors, rectifiers, or mixers [23]–[30]. In many cases, they make use of two devices made from graphene: the GFET and the MIG diode, which will be now introduced.

1.2.1. Graphene field-effect transistor

As metal-oxide-semiconductor field-effect transistors (MOSFETs) continue to shrink to nanometer scales following Moore's roadmap [31], they encounter a host of challenges that jeopardize their performance and reliability. Of special importance are the so-called short-channel effects (SCE) [32], which impact the device performance in different ways such as making the gate to loose precise control over the channel, decreasing switching efficiency, threshold-voltage roll-off, drain-induced barrier lowering (DIBL), or impaired drain-current saturation [32]. Power dissipation becomes also a major issue, hindering the development of energy-efficient devices [32].

GFETs offer a compelling solution to the scaling limitations faced by MOSFETs. First, its monoatomic thickness allows ultra-scaled device operation, due to the reduction of the SCEs. Besides, graphene's exceptional properties, like its superior electron transport and high carrier mobility [7], promise significantly faster operation compared to Si [33]. What is more, graphene's exceptional thermal conductivity [34] allows for efficient heat dissipation, which can help overcoming power limitations in high-density circuits. In addition, graphene is elastic and mechanically strong [35], enabling the fabrication of flexible electronic devices [36]. These advantages pave the way for the development of faster, more energy-efficient, and unique electronic devices [18].

However, in spite of the great expectations, the research and development of the GFETs has encountered several challenges to face in order to fully leverage graphene's high aspirations. First of all, the intrinsic high carrier mobility measured on suspended graphene [7] is worsened by two to three orders of magnitude when graphene is transferred onto a substrate like SiO_2 due, among other aspects, to electron-phonon scattering [37]. The search for substrates which remarkably keep the intrinsic mobility and saturation velocity has encountered hexagonal boron nitride (h-BN) as a suitable substrate that, e.g., increases mobility by up to one order of magnitude with respect to SiO_2, due to its atomically smooth surface and its similar lattice constant to that of graphite [38]–[40], and, in addition, it can be used as the gate-dielectric due to its insulating properties. This increase in mobility leads to an increase in the operation frequency of RF-targeted devices [41]–[43].

Finally, the lack of a clear current saturation region on the output characteristic of the GFETs has also been acknowledged as a critical aspect [33], due to its relation with the

ability of the device to provide gain. This is of critical importance, for analog circuit designers, to whom current saturation is essential for achieving high voltage gains, as $A_{\mathrm{v}} = g_{\mathrm{m}}/g_{\mathrm{ds}}$, where A_{v} is the voltage gain, g_{m} is the transconductance and g_{ds} is the output conductance. If a transistor cannot be biased at the current saturation regime, a non negligible g_{ds} will entail very low voltage gain.

Even though all these set of drawbacks, competitive graphene-based transistors with high cutoff (f_{T}) and maximum oscillation (f_{max}) frequencies, have indeed been obtained. The cut-off frequency, f_{T}, is the frequency at which the current gain of the transistor drops to $0\,$dB when the output port is shorted, while the maximum frequency of oscillation, f_{max}, is the frequency at which the unilateral power gain drops to $0\,$dB. Regarding f_{T}, a GFET with a $67\,$nm gate length exhibiting $427\,$GHz has reported the highest value so far in the literature [44]. This f_{T} value is not that far from the record f_{T} exhibited by other competing field-effect transistors (FETs), e.g. $688\,$GHz for a $40\,$nm GaAs high electron mobility transistor (HEMT) [45]. In contrast to their impressive f_{T} performance, GFETs behave rather poor in terms of the f_{max}. The highest f_{max} value reported so far is $200\,$GHz, corresponding to a GFET of a $60\,$nm channel length [46], which is further from the several hundreds of GHz demonstrated by its III-V competitors. For instance, a record f_{max} surpassing $1\,$THz has been demonstrated by an InP HEMT device of $35\,$nm channel length [47]. Finally, for the sake of a fair comparison, it is worth mentioning that, as expected, the length of the device is the most critical parameter that affects f_{T} and f_{max} [48], reducing it increases both (). Graphene-based transistors have shown a good scaling behavior, following the trendline $1/L_{\mathrm{g}}^{0.9}$ [49] typical for Si-MOSFETs and HEMTs [33], where L_{g} stands for the transistor's gate length.

1.2.2. Metal-insulator-graphene diode

Diodes are fundamental building blocks in the world of electronics, serving diverse purposes in countless applications, such as safeguarding circuits from over-voltage or reverse-voltage conditions, or as light detectors (photodiodes). Within the RF realm, their non-linear characteristics make them very useful for signal detection in receivers, multiplication, up and down conversion, power rectification, and even energy harvesting [50]–[52].

In the RF field, conventional p-n semiconductor junction and Schottky diodes have during decades dominated the landscape due to their great nonlinear characteristic, well controlled processing technology and high RF bandwidth [52]–[55]. However, they exhibit an intrinsic limitation arising caused by the way charge carriers move within them. In this traditional semiconductor junction technology, when the bias is changed from positive to negative, minority charge carriers do not immediately traverse the junction, causing them to build-up within the depletion region. During rapid bias changes, this region needs to discharge before it can block current, creating a momentary undesired conductive state. This unavoidable charge rearrangement, significantly lengthens reverse recovery time in this type of diodes. This delay, often surpassing 10 nanoseconds, severely limits their suitability for high-frequency applications [56].

In contrast to this technology, thin-film MIM diodes offer a distinct approach. First of all, their simplified fabrication process makes them attractive for specialized applications where traditional semiconductor diodes might face integration challenges or performance limitations [57]. In addition to that, the current conduction mechanism, the so-called thermionic emission, does not suffer from the restrictive speed limitation of p-n junctions, making them great candidates for RF operation [58], [59].

In the last decade, an alternative to the MIM diodes has emerged, the MIG diode. This maintains the same structure as the MIM diode replacing one of the metals by a graphene layer [53]. The addition of graphene improves the nonlinearity, asymmetry and confers the diode the ability of working as a varactor thanks to the graphene's tunable quantum capacitance [60], [61]. This allows MIG diodes to be used for a different range of applications that can fully exploit the properties of graphene and thus avoid to directly compete with more mature technologies in conventional designs and applications.

MIG diodes hold significant promise for high-frequency applications due to the unique properties of graphene. The combination of graphene's high carrier mobility and work function tunability, together with the rectifying nature of the metal-insulator junction suggests potential for ultrafast rectification, frequency mixing in communication systems, and even terahertz devices [30], [53], [62], [63].

Indeed, MIG diodes have been already used in RF applications benefiting from their nonlinearity and asymmetry, showing improved characteristics when compared to similar devices like MIM diodes, such as power detectors, mixers or even a complete microwave receiver [25], [30], [63].

1.3. Thesis scope and outline

1.3.1. Scope

This Thesis tackles the design and assessment of graphene-based high frequency circuits. This will be accomplished in two different ways: on the one hand, applying conventional RF circuit design techniques to newly graphene-based devices; on the other hand, benefiting from the unique properties of graphene-based devices in order to realize new circuit designs that would not be possible with conventional technologies. The objective is thus to develop and optimize those RF graphene-based topologies that were already present in the literature, and to purpose new circuit designs when possible.

Specifically, this Thesis pursues the following specific objectives:

- Design and assessment of analog phase shifters based on graphene.
- Design and assessment of frequency multipliers using GFET technology.
- Design and assessment of graphene-based oscillators.
- Demonstration of GFET-based RF power gain amplifiers.
- Layout design of graphene-based devices an RF circuits.

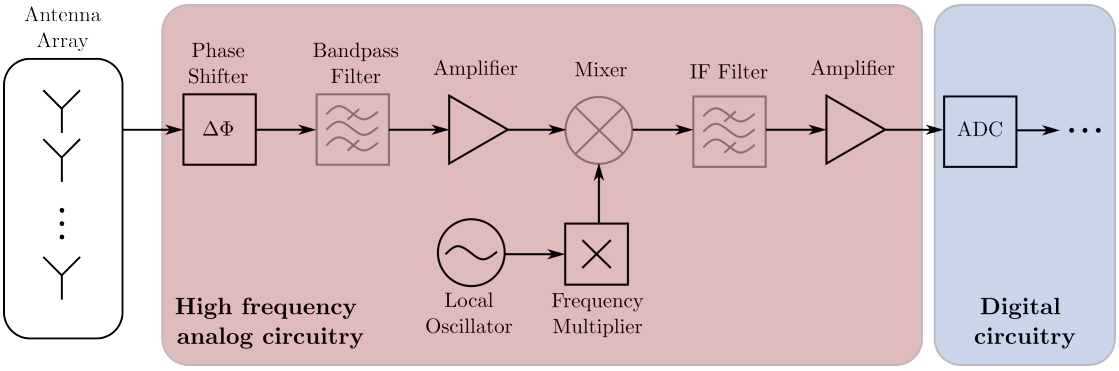


Figure 1.1.: Architecture of a wireless receiver. Within the high frequency analog circuitry, the blocks that are in black are the ones covered in this Thesis.

- Fabrication of graphene-based devices.

Those objectives, together with graphene-based mixers and filters, could be used for building a complete wireless receiver as the one shown in Fig. 1.1. Mixers and filters, shaded on the receiver of Fig. 1.1, have not been covered in this Thesis, as they are the focus of other works within the Pervasive Electronics Advanced Research Laboratory (PEARL), in which this Thesis is framed.

1.3.2. Outline

This Thesis is organized as follows:

- Chapter 2 introduces the two graphene-based devices used for the circuit designs: the MIG diode and the GFET, including its physical description and working principle.
- Chapter 3 addresses the clean-room design and fabrication of MIG diodes during a research stay at AMO GmbH, a non-profit research-oriented company in Aachen, Germany; the design and fabrication of GFETs through the 2D-EPL; as well as the DC and AC electrical characterization of both devices.
- Chapter 4 shows the circuit designs that were developed making use of the GFET as the main device; namely, a phase shifter, a power gain amplifier, a frequency multiplier, and an oscillator.
- Chapter 5 exhibits the explored circuit designs which employ the MIG diode as the main device: periodic structures and phase shifters.
- Finally, Chapter 6 presents the conclusions of the work and outlines the future work.

Part II.

Graphene-based devices: analysis, fabrication, and characterization

Chapter

2. Graphene-based devices: analysis

In this chapter, two of the most relevant electronic devices made with graphene will be presented: the GFET and the MIG diode. These two devices will be the basis for the development of RF circuits in the following chapters. We will first introduce the electronic properties of graphene. Then, we will comment on the devices working principle, and show their characteristic curves. Finally, we will present their equivalent circuit models and analytically calculate their most relevant FoMs.

2.1. An introduction to graphene's electronic properties

Graphene is a 2D material consisting of a planar hexagonal arrange of carbon atoms, forming a structure that recalls that of a honeycomb, as can be seen in Fig. 2.1a. Particular attention deserves its band structure, shown in Fig. 2.1b, where the valence and conduction bands intersect in a point of zero available states, the so-called Dirac energy level E_{D} [10]. As a consequence, graphene is regarded as a zero-gap semiconductor (or semimetal) [64], in which Fermi energy levels, E_{F}, below the Dirac point (E_{D}) will result in a graphene layer populated with holes, while E_{F} above E_{D} will populate the material with electrons. When the Fermi level is located exactly at the the Dirac point, i.e., $E_{\mathrm{F}} = E_{\mathrm{D}}$, graphene, in practical situations, exhibits a non-zero conductance [5], reason why devices made with graphene channels cannot be effectively switched off and are thus usually disregarded for digital electronics [18].

Figure 2.2a shows the charge density for electrons and holes on a graphene layer with respect to $E_{\mathrm{D}} - E_{\mathrm{F}}$, where the electron (hole) charge density is defined as $Q_{\mathrm{n}} = -qn$ ($Q_{\mathrm{p}} = qp$), where q is the elementary charge, and n and p the electron and hole concentration, respectively. These are evaluated by means of the following equations [65]:

$$n = \frac{2}{\pi(\hbar v_{\mathrm{F}})^2} \int_0^\infty \frac{E}{1 + e^{\frac{E - E_{\mathrm{F}}}{k_{\mathrm{B}} T}}} dE \tag{2.1}$$

$$p = \frac{2}{\pi(\hbar v_{\mathrm{F}})^2} \int_0^\infty \frac{E}{1 + e^{\frac{E + E_{\mathrm{F}}}{k_{\mathrm{B}} T}}} dE \tag{2.2}$$

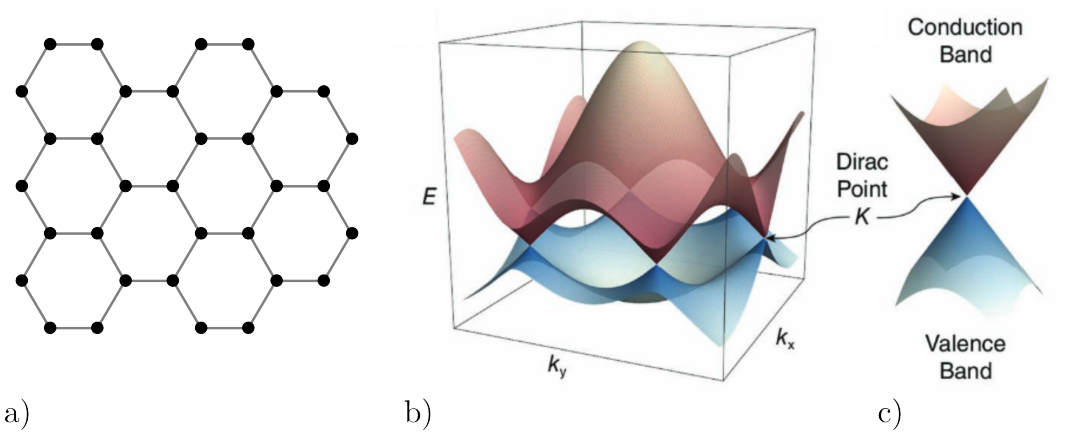


Figure 2.1.: a) Graphene characteristic hexagonal arrange forming a honeycomb-alike structure. b) Band structure of graphene. c) Detail of the band structure showing the conical shape of conduction and valence bands near their intersection, at the so-called Dirac point. Figures b) and c) taken from [10] and reproduced with permission ©2012 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

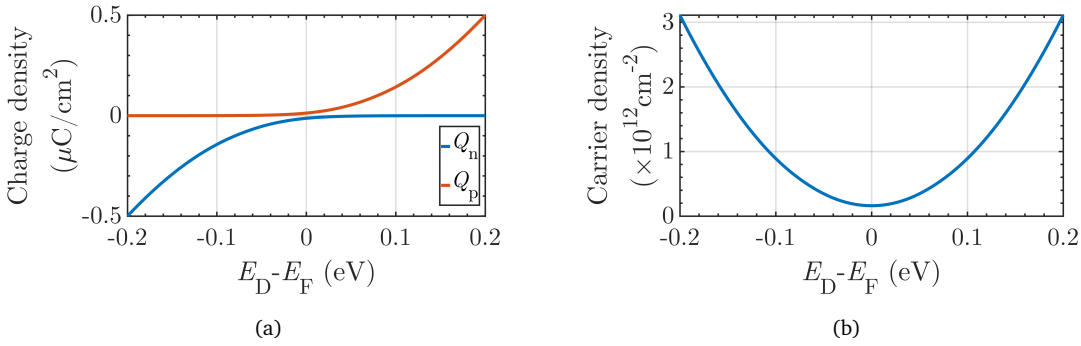


Figure 2.2.: a) Electron and hole charge density, and b) mobile carrier density, of a graphene layer.

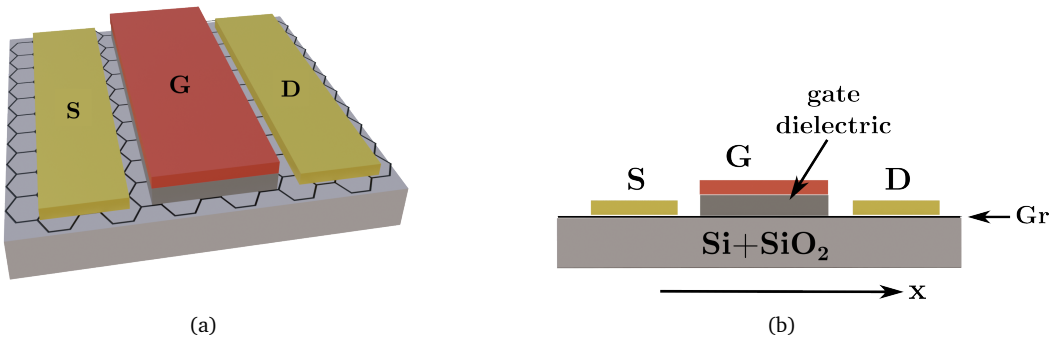
In Fig. 2.2b the corresponding total carrier density, $p + n$, is depicted, where the ambipolar nature of graphene is revealed.
where $\hbar$ is the reduced Planck constant, v_F is the Fermi velocity, k_B is the Boltzmann constant, and T is the temperature.

In the vicinity of the Dirac point, the band structure displays a conical shape, as illustrated in Fig. 2.1c, which produces carriers in graphene to behave as massless Dirac fermions [10], leading to the outstanding reported carrier mobilities in the order of $10^6\,\mathrm{cm}^2/\mathrm{Vs}$ [66], [67], paving the way towards the use of graphene-based electronic devices for the design of high-speed electronics [10].

Many other fascinating electronic properties have been studied and reported for graphene, such as Chiral tunneling [68], or spin-orbit coupling [69], which are, however, out of the scope of this thesis.

2.2. Graphene field-effect transistor

2.2.1. Device description and working principle



(a) (b)

Figure 2.3.: (a) Side and (b) lateral views of the GFET. The gate contact is colored in red, while the drain and source contacts are displayed in yellow.

The GFET is an electronic device formed by a graphene channel which is directly contacted at its ends by two metallic contacts, which act as drain and source. The gate is separated from the channel by an insulator, providing the so-called field-effect. The structure of a typical device is shown in Fig. 2.3, where the drain and source metallic contact are in yellow, and the gate is in red. The shown geometry assumes the gate on top topology, though other geometries can be found in the literature [18]. The device is symmetric with respect to the gate, meaning that drain and source are, in general, just a naming convention, but they do not entail any physical distinction on the device.

In principle, the behavior of a GFET is similar to that of a conventional MOSFET: there is a lateral electric field formed when a potential difference is applied between drain and source terminals, V_{DS}, and there is a vertical electric field formed by the gate-to-source voltage, V_{GS}. Each potential has an impact on the band structure and on the current along the device. Fig. 2.4 shows the change on the resistivity of single-layer graphene at $1\,\mathrm{K}$, ρ, when a gate bias, V_{g}, is applied. The Dirac cones in the inset show the case where $V_{\mathrm{g}} < 0\,\mathrm{V}$ (left) and thus the Fermi level is below the Dirac point, populating the graphene layer with holes and thus lowering the resistivity; the equilibrium case in which $V_{\mathrm{g}} = 0\,\mathrm{V}$ (right-up) and thus $E_{\mathrm{F}} = E_{\mathrm{D}}$, increasing resistivity to its maximum (but non-infinite); and the case where $V_{\mathrm{g}} > 0\,\mathrm{V}$ (right-down), for which the Fermi level is located above the Dirac point, and as a consequence the resistivity of the graphene decreases, exposing the ambipolar nature of graphene [64]. Thus, the applied gate voltage modifies the conductivity of the graphene layer and ultimately its current in a FET configuration, increasing it (for a constant non-zero V_{DS}) in both directions away from the Dirac point, accordingly moving the Fermi level away from the Dirac energy, forming the characteristic V-shaped transfer curve.

On the other hand, the drain voltage drifts the carriers between drain and source

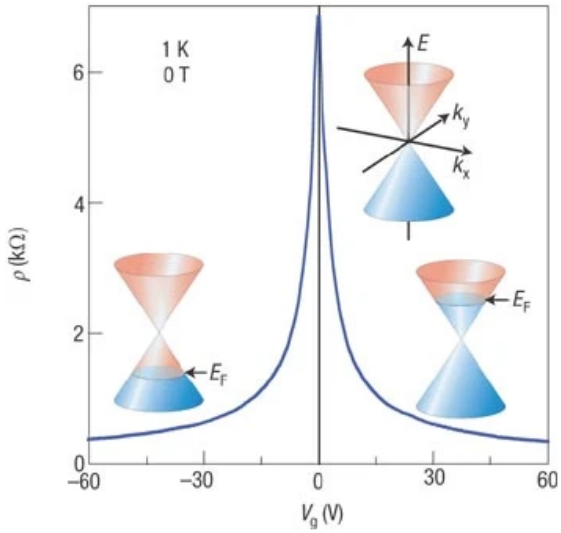


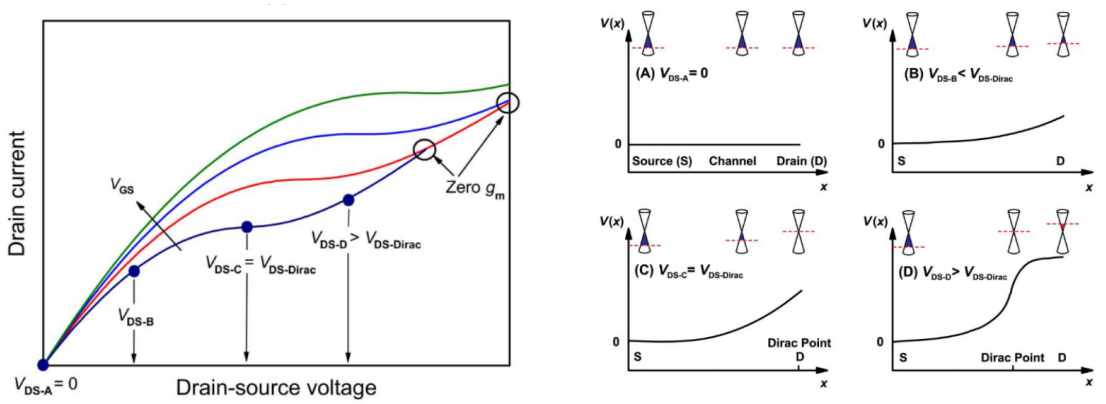
Figure 2.4.: Resistivity versus gate voltage showing the field-effect on single layer graphene. The inset shows the Dirac cones at three different V_{G} values. Image taken from [64] and reproduced with permission from Springer Nature.

terminals, but also modifies the Fermi level on the graphene layer along the channel. To better understand this effect, Fig. 2.5a shows the drain current, I_{DS}, versus the drain-source voltage, V_{DS}, for different gate-source voltages (V_{GS}). Fig. 2.5b shows the voltage on the channel for different drain-source voltages versus the position x (as marked in Fig. 2.3b), assuming source terminal is grounded. The inset shows the Fermi level variation along the channel, marked with a red dashed line plotted on the Dirac cones. Both images are taken from [33]. Four different cases are distinguished, A-D, and the corresponding V_{DS} values are labeled as $V_{\mathrm{DS_A}}$ to $V_{\mathrm{DS_D}}$:

- Case A (Fig. 2.5b up-left panel): if $V_{\mathrm{DS-A}} = 0\,\mathrm{V}$, then the Fermi level is constant along the channel, which has initially been assumed to be located below the Dirac point, which means the graphene is populated with holes. Here, no current will appear as there is no longitudinal field.

- Case B (Fig. 2.5b up-right panel): if $V_{\mathrm{DS-B}} < V_{\mathrm{DS-Dirac}}$, where $V_{\mathrm{DS-Dirac}}$ is the Dirac voltage, then there is a voltage drop along the channel but the Fermi level is still within the valence band along the graphene channel. As shown in Fig. 2.5a, at this point the drain current behaves linearly with respect to the drain-to-source bias.

- Case C (Fig. 2.5b down-left panel): if $V_{\mathrm{DS-C}} = V_{\mathrm{DS-Dirac}}$, then the potential at the drain equals the Dirac voltage, meaning that the Fermi level at the drain is located at the Dirac energy level, where the conductivity is minimum due to the lack of available states. Thus, for this drain source potential, the drain current saturates, as can be seen in Fig. 2.5a.



a) b)

Figure 2.5.: a) Drain current versus drain-source voltage for different gate-source voltages. b) Voltage on the channel of a GFET for different drain-source voltages versus the position (as in Fig. 2.3b. The inset shows the Fermi level variation along the channel, marked with a red dashed line plotted on the Dirac cones. Image taken from [33] and reproduced with permission ©2013 IEEE.

- Case D (Fig. 2.5b down-right panel): if $V_{\mathrm{DS-D}} > V_{\mathrm{DS-Dirac}}$, then the potential at the drain moves the Fermi level above the Dirac point, entering in the conduction band, while the Fermi level at the source continues within the valence band. This means that at the drain, there are again available states for carriers to populate the channel and the drain current again linearly increases, as depicted by Fig. 2.5a.

In conclusion, the Fermi level shift on the drain terminal for different applied drain voltages explains the formation of a quasi-saturation region named kink at $V_{\mathrm{DS}} = V_{\mathrm{kink}}$ [70]. For $V_{\mathrm{DS}} > V_{\mathrm{kink}}$, the Fermi level at the drain enters the conduction band, populating the drain side of the channel with electrons, producing a new increase in the drain current, which is sometimes referred as second linear region [33].

Regarding the transport, the drift-diffusion (DD) theory properly models the current conduction on a GFET considering its length large enough so that collisions between carriers within the channel are dominant against ballistic transport, which can be equivalently expressed saying that the length of the devices, L, must be much larger than the mean-free-path (MFP), λ ($L \gg \lambda$), which is the case for devices with a channel length greater than $L \sim 300\,\mathrm{nm}$ [20] and which will be the case for most of the experimentally fabricated GFETs.

2.2.2. Current-voltage characteristic

Following the DD current mechanism, the expression for the current on a GFET versus the applied voltage can be found as [71]:

$$I_{\mathrm{DS}} = W Q_{\mathrm{tot}}(x) \mu_g(x) \frac{\mathrm{d}V}{\mathrm{d}x} \tag{2.3}$$

where:

- W is the channel width;
- $Q_{\mathrm{tot}}(x) = q[p(x) + n(x) + n_{\mathrm{res}}]$, is the available charge sheet density along the channel at position x, with n_{res} being the residual carrier concentration [20];
- $\mu_{\mathrm{g}}(x)$ is the carrier mobility, considered the same for electron and holes and depends on a constant saturation velocity;
- V is the quasi Fermi level. This variable is equal to V_{d} and V_{s} at $x = 0$ and $x = L$, respectively.

A thorougher analysis and expression for the current can be found in the literature [72], [73]. In this work, however, a qualitative approach will be followed, skipping the intricate analytical expressions to directly jump into the observational details that can be more useful from a circuit designer's perspective.

Figures 2.6a and b show the transfer and output characteristics for different V_{DS} and V_{GS} values, respectively, of a typical GFET as the one shown in Fig. 2.3, with $W = L = 10\,\mu\mathrm{m}$, insulator thickness of $t_{\mathrm{ox}} = 40\,\mathrm{nm}$ and insulator relative permittivity of $\epsilon_{\mathrm{r}} = 7$ and a mobility of $\mu = 2000\,\mathrm{cm}^2/\mathrm{Vs}$.

Figure 2.6a exposes ambipolarity of the graphene, as commented earlier. It can also be observed in this same Figure that the Dirac point shifts with the applied $V_{\mathrm{DS,e}}$. This is a consequence of the Fermi level shifting in the graphene not only with $V_{\mathrm{GS,e}}$ but also with $V_{\mathrm{DS,e}}$. The Dirac point can be calculated as [74]:

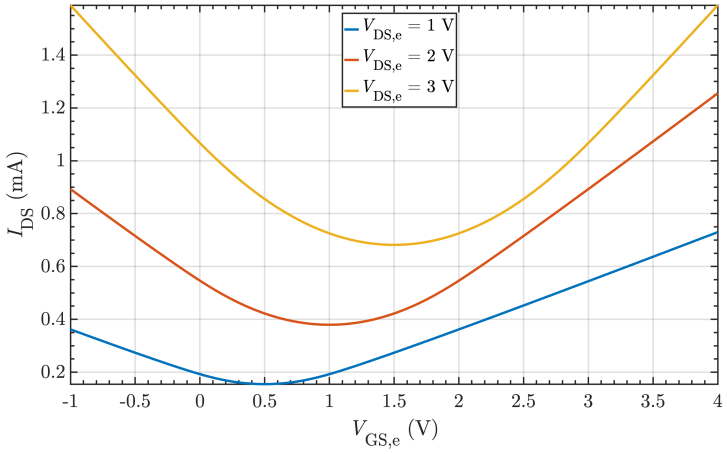
$$V_{\mathrm{Dirac}} = V_{\mathrm{go}} + \frac{V_{\mathrm{d}} + V_{\mathrm{s}}}{2} \tag{2.4}$$

where V_{go} is the offset potential, modeling any possible residual doping of the graphene which directly shifts the Dirac point.

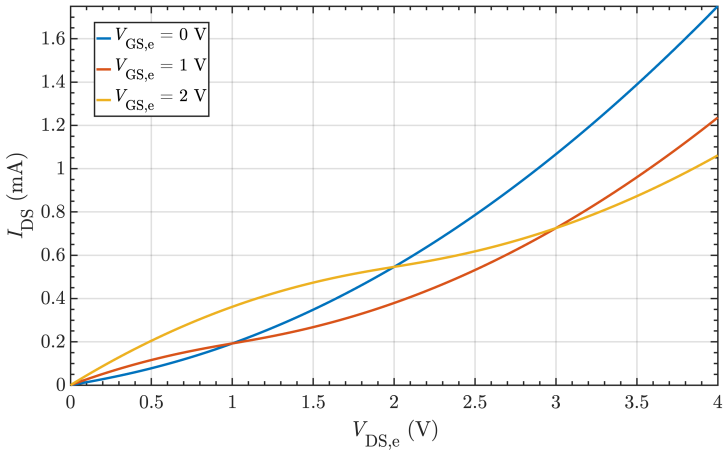
Finally, the output curve is shown in Fig. 2.6b, where the first and second linear regions together with the kink are observed, as explained earlier.

2.2.3. Small-signal model

The equivalent small-signal model of the GFET is shown in Fig. 2.7 [75]. The intrinsic device is framed. R_{d} and R_{s} model the series of the contact and access resistances of the drain and source terminals, respectively, while R_{g} is the gate pad resistance. C_{gs}, C_{gd}, C_{sd} and C_{dg} are the intrinsic device capacitances; g_{m} is the transconductance; and g_{ds} is the output conductance.



(a)



(b)

Figure 2.6.: Current characteristic versus $V_{GS,e}$ (a) and $V_{DS,e}$ (b) for different $V_{DS,e}$ and $V_{GS,e}$ values, respectively.

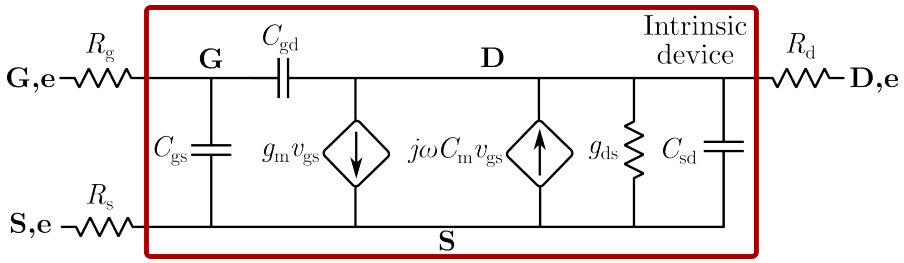


Figure 2.7.: Small-signal model of the GFET.

2.2.4. FoMs and comparison with other technologies

FoMs analytical calculation for the GFET

Some relevant FoMs that can measure the performance of a device at high frequency are the cut-off frequency, f_{T}, and the maximum oscillation frequency, f_{max}. The first refers to the frequency at which the current gain of the device equals one (zero in decibels) assuming a short circuit on the second port, and is calculated by means of the hybrid parameter $h_{21} = \frac{i_2}{i_1}\Big|_{v_2=0}$ i.e. $f_{\mathrm{T}} = f\Big|_{|h_{21}|=1}$, while the second refers to the point where the unilateral power gain of the device equals one (zero in decibels), assuming the device is unilateral (i.e., $|S_{12}| = 0$), and is calculated through the Mason's invariant or unilateral power gain, U. Both expressions can be analytically calculated for the GFET using its small-signal model shown in Fig. 2.7. For this calculation we will only consider the intrinsic device, i.e., neglecting contact resistances.

The expression for the h_{21} of the intrinsic device of the GFET is shown in eq. (2.5). Equalling its modulus to one and solving for the frequency leads to the expression of f_{T} as shown in eq. (2.6), in which it can be directly observed that a higher intrinsic transconductance $g_{\mathrm{m}} = \mathrm{d}I_{\mathrm{DS}}/\mathrm{d}V_{\mathrm{GS}}$ produces a higher f_{T}.

$$h_{21} = \frac{-C_{\mathrm{dg}}\omega}{\omega(C_{\mathrm{gd}} + C_{\mathrm{gs}})} - j\frac{g_{\mathrm{m}}}{\omega(C_{\mathrm{gd}} + C_{\mathrm{gs}})} \tag{2.5}$$

$$f_{\mathrm{T}} = f\Big|_{|h_{21}|=1} = \frac{|g_{\mathrm{m}}|}{2\pi\sqrt{(C_{\mathrm{gd}} + C_{\mathrm{gs}})^2 - C_{\mathrm{dg}}^2}} \tag{2.6}$$

The intrinsic theoretical expression of U for the GFET, i.e. without contact resistances nor gate resistance, tends to infinity, reason why at least the gate resistance R_{g} has to be considered in order to obtain a delimited expression. If contact resistances are neglected but R_{g} is considered, it gives the following equation:

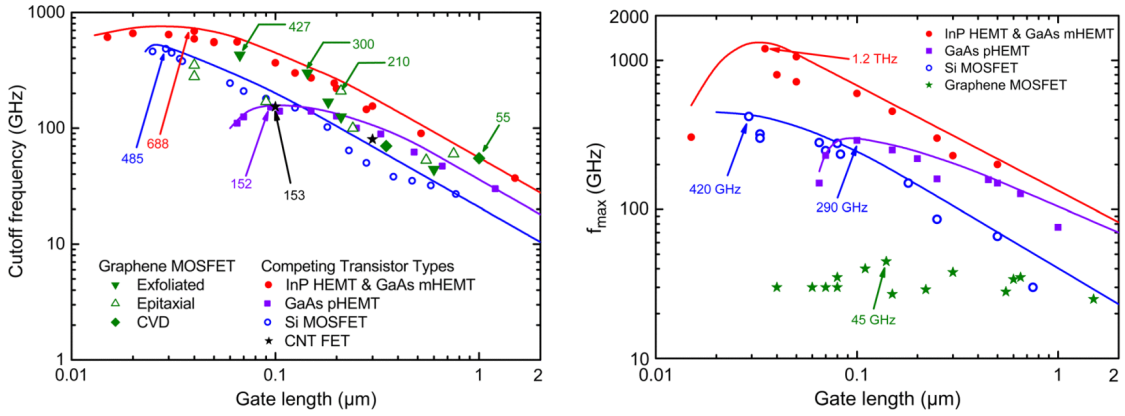
$$U = \frac{\omega^2(C_{\mathrm{dg}}^2 - 2C_{\mathrm{dg}}C_{\mathrm{gd}} + C_{\mathrm{gd}}^2) + g_{\mathrm{m}}^2}{4R_{\mathrm{g}}\omega^2(C_{\mathrm{gd}} + C_{\mathrm{gs}})(C_{\mathrm{gd}}g_{\mathrm{ds}} + C_{\mathrm{gs}}g_{\mathrm{ds}} + C_{\mathrm{gd}}g_{\mathrm{m}})} \tag{2.7}$$

where $g_{\mathrm{ds}} = \mathrm{d}I_{\mathrm{DS}}/\mathrm{d}V_{\mathrm{DS}}$. Equalling its modulus to one and solving for the frequency, we obtain the intrinsic maximum oscillation frequency:

$$f_{\mathrm{max}} = \frac{|g_{\mathrm{m}}|}{2\pi\sqrt{4R_{\mathrm{g}}(C_{\mathrm{gd}} + C_{\mathrm{gs}})(C_{\mathrm{gs}}g_{\mathrm{ds}} + C_{\mathrm{gd}}(g_{\mathrm{ds}} + g_{\mathrm{m}})) - (C_{\mathrm{dg}} - C_{\mathrm{gd}})^2}} \tag{2.8}$$

It can be indeed seen that if $R_{\mathrm{g}} = 0$, then U and $f_{\mathrm{max}} \to \infty$, showing the great impact of the gate resistance in the performance of the device at high frequency.

If also the drain and source contact resistances R_{d} and R_{s} are included in the calculation of f_{T} and f_{max}, then we can obtain their extrinsic values, however the complexity of the expressions grows considerably, reason why they are not explicitly shown in this document (they can be found in [75]). Observing the full expression for the extrinsic



(a) (b)

Figure 2.8.: a) f_{T} and b) f_{max} versus gate length of different state-of-the-art devices including GFETs (images taken from [33]).

FoMs it can be concluded that the lower the R_{g}, R_{d} and R_{s} values, the higher the f_{T} and f_{max} values. For this reason, their reduction will always be a goal for the circuit designer as well as for the process engineer, and will always positively impact the performance of the transistor at high and low frequencies.

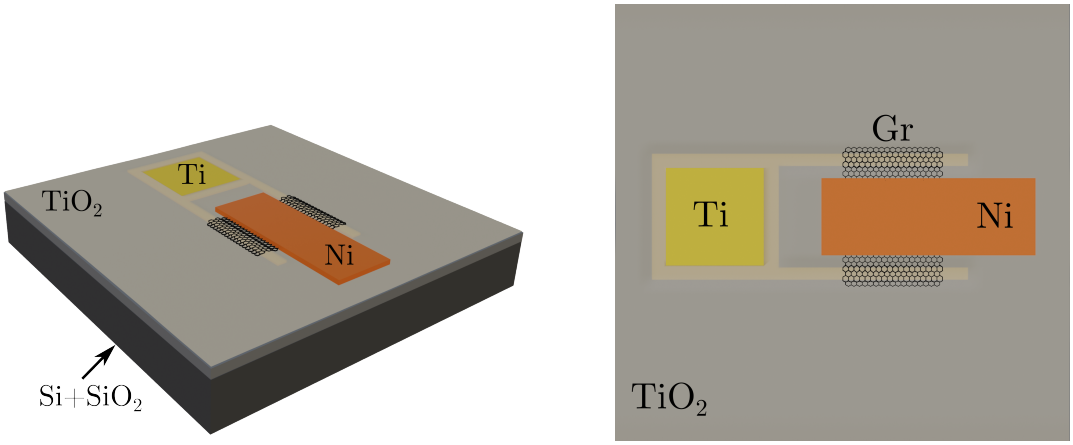
Comparison with other technologies

Fig. 2.8 show a comparison taken from [33] of the a) f_{T} and b) f_{max} values for different devices, including the GFET. It can be seen that in terms of f_{T}, the GFET is competitive and comparable to the highest f_{T} devices of indium phosphide high electron mobility transistor (InP HEMT) and gallium arsenide metamorphic high electron mobility transistor (GaAs mHEMT). However, in terms of f_{max}, the GFET ranks below the compared device technologies and also for most of the compared GFETs devices $f_{\mathrm{max}} < f_{\mathrm{T}}$. The reasons behind low f_{max} value are various and in fact the gain performance of the device which is directly related to this FoM will be studied in detail in the following chapters, but a clear factor impacting the gain performance of the device is due to drain and source contact resistances and gate resistance. Indeed, it has been seen that reducing these resistances has led to GFETs showing $f_{\mathrm{max}} > f_{\mathrm{T}}$ [76].

2.3. Metal-insulator-graphene diode

2.3.1. Device description and working principle

The MIG diode is an electronic device formed by a metal-insulator-graphene stack. In order to contact the graphene layer, an additional metallic pad is added on top, which forms a contact resistance, R_{c}, at the interface between the metal and the graphene due



(a) (b)

Figure 2.9.: (a) Side and (b) top views of the MIG diode.

to poor injection and extraction of carriers [77]. The structure of the device is shown in Fig. 2.9.

The physical behavior of the diode is explained by two mechanisms: thermionic emission and graphene Fermi level tuning. Thermionic emission, on the one hand, explains the transport mechanism, and occurs when the carriers jump over a potential barrier due to the energy that the temperature provides them, provoking an exponential increase in the current with respect to the applied voltage. On the other hand, graphene Fermi level tuning explains the large variation of the graphene-insulator barrier height, which allows for a high modulation of the current on the diode [78].

To further explore the latter mechanism, Fig. 2.10 shows the band diagram of the MIG diode (a-c) and of a MIM diode (d-f) for a negative, zero, and positive biases, respectively. When a negative bias is applied to the metal of the MIG diode with the graphene grounded through the top contact pad, the graphene-insulator barrier height is increased, as shown in Fig. 2.10c by the term ϕ_{G}. This increase in the barrier height directly influences the thermionic current; consequently, overall current flow becomes higher than it would be in a standard MIM diode where the metal-insulator barrier heights are fixed, as shown in Fig. 2.10d. Conversely, a positive bias applied to the metal while keeping the graphene grounded decreases the graphene-insulator barrier height, increasing the overall thermionic current, which is now higher than that of a MIM diode, as seen in Figs. 2.10c and f, respectively. This possibility of tuning the barrier height of the graphene-insulator interface thanks to the Fermi level tuning on graphene translates into greater nonlinearity, improved responsivity, and higher asymmetry in the MIG diode with respect to MIM diodes [62].

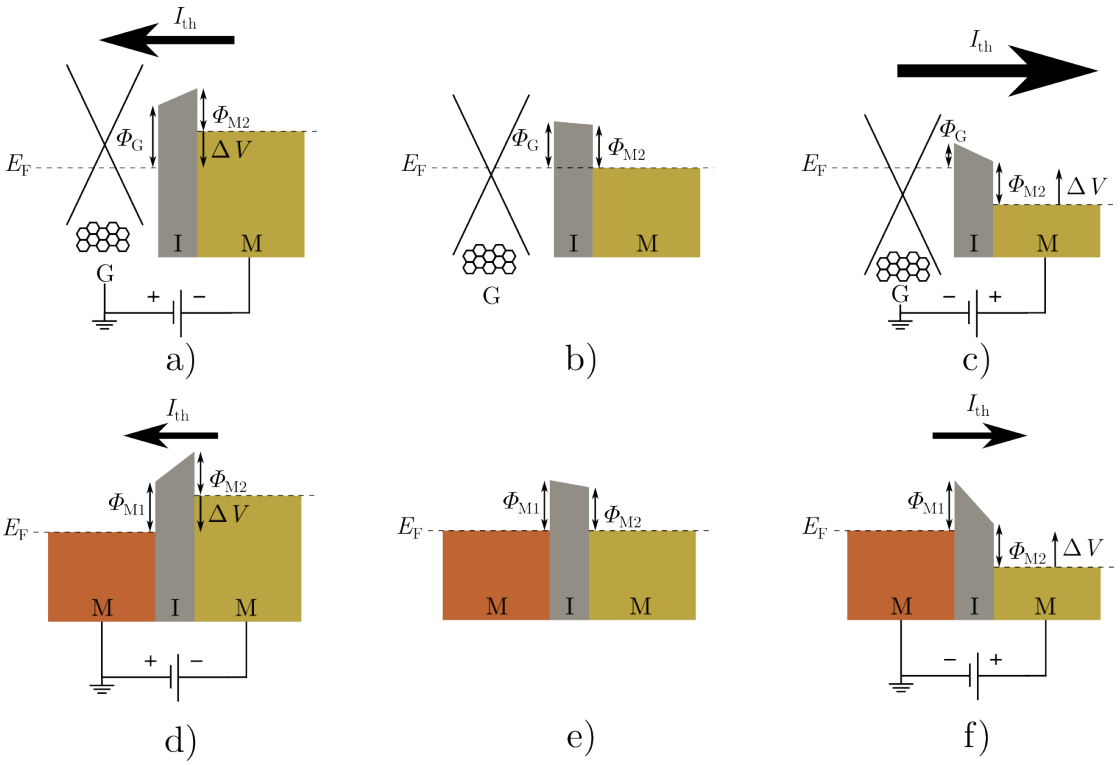


Figure 2.10.: Band diagram of the a)-c) MIG diode and of the d)-f) MIM diode for a positive, zero, and negative bias, respectively. Image created based on the one in [62].

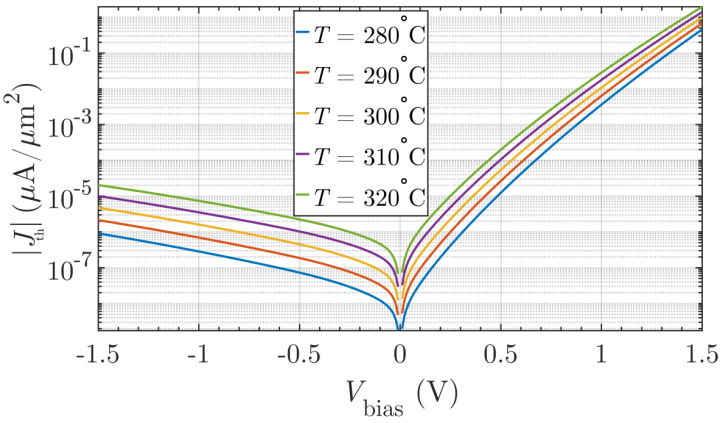


Figure 2.11.: Current-voltage characteristic of the MIG diode.

2.3.2. Current-voltage characteristic

The vertical transport on the MIG diode is produced due to a combination of thermionic emission and of the modulation of the graphene-insulator barrier height as a consequence of the Fermi level tunability of graphene. This can be described by the Dirac-Schottky model, giving the following expression for the current on the device [78]:

$$I_{\mathrm{th}} = WL\frac{qk_B^3T^3}{\pi\hbar^3\nu_F^2}e^{-\frac{q\phi_b-\frac{\delta_p^2}{2k_BT}}{k_BT}}\left(e^{\frac{q(V_{\mathrm{a}}-V_{\mathrm{c}})}{\eta k_BT}}-1\right) \tag{2.9}$$

where W and L are the width and length of the device, respectively; q is the elementary charge; k_{B} is the Boltzmann constant; T is the temperature; $\hbar$ is the reduced Planck constant; ν_{F} is the Fermi velocity; ϕ_{b} is the height of the barrier; η is the ideality factor; δ_p estimates the spreading of the Fermi level; and $(V_{\mathrm{a}} - V_{\mathrm{c}})$ is the anode-to-cathode voltage. As can be seen in eq. (2.9), the diode current exponentially depends on the anode-to-cathode voltage and on the Schottky barrier height (SBH).

The $J_{\mathrm{th}} - V_{\mathrm{bias}}$ curve of a typical two-finger MIG diode as the one shown in Fig. 2.9 with finger size of $L \times W = 4\,\mu\mathrm{m}\times 70\,\mu\mathrm{m}$, insulator thickness of $t_{\mathrm{ox}} = 6\,\mathrm{nm}$ and insulator relative permittivity of $\epsilon_{\mathrm{r}} = 20$ and for different temperatures is shown in Fig. 2.11, where the current density is calculated per unit area. The clear current density dependence with the temperature is a sign of the thermionic emission being the dominant transport mechanism.

Thus, the current through the diode highly depends on the temperature, on the applied voltage, which has been seen to modify the height and shape of the graphene-insulator barrier, but also on the insulator thickness.

2.3.3. Capacitance-voltage characteristic

In addition to the current characteristic, the MIG diode also exhibits a variable capacitance that changes with the applied bias. This variable capacitance is due to graphene's quantum capacitance, C_{q}, which is defined as the net charge variation with respect to the potential difference on the graphene channel, $C_{\mathrm{q}} = \mathrm{d}Q_{\mathrm{net}}/\mathrm{d}V_{\mathrm{ch}}$, and which shows a minimum at the so-called Dirac point, the minimum conduction point of graphene [60]. The value of C_{q} can be analytically calculated as [79]:

$$C_{\mathrm{q}} = \frac{2q^2 k_{\mathrm{B}} T}{\pi(\hbar\nu_{\mathrm{F}})^2} \ln\left[2\left(1+\cosh\left[\frac{qV_{\mathrm{ch}}}{k_{\mathrm{B}}T}\right]\right)\right] \tag{2.10}$$

In the MIG diode, there is a series connection of C_{q} with the fixed-value geometric capacitance formed in the metal-insulator-graphene stack, C_{ox}, in the form:

$$C_{\mathrm{T}} = \frac{C_{\mathrm{ox}} C_{\mathrm{q}}}{C_{\mathrm{ox}} + C_{\mathrm{q}}} \tag{2.11}$$

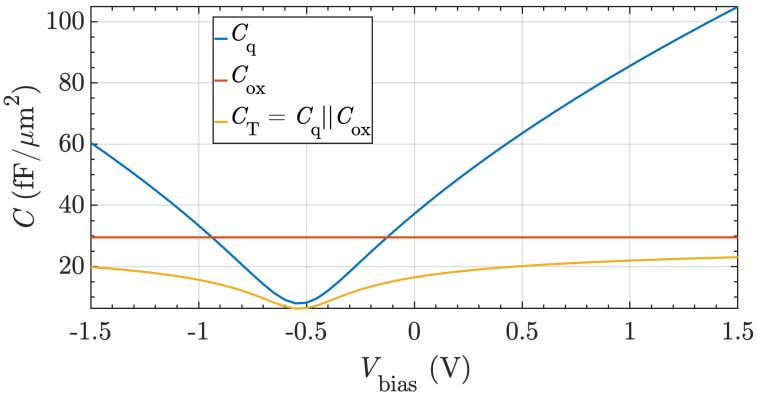
Thus, in order to reflect the variation of C_{q} in the total capacitance C_{T}, the geometric capacitance needs to be much higher than the quantum capacitance of the graphene, $C_{\mathrm{ox}} \gg C_{\mathrm{q}}$, so that the series association is dominated by C_{q}. Otherwise, the variation of C_{q} will be masked by C_{ox}.

The total capacitance per unit area of a typical two-finger MIG diode, as the one in Fig. 2.9 with finger size of $L \times W = 4\,\mu \times 70\,\mu\mathrm{m}$, $\epsilon_{\mathrm{r}} = 20$, and two different values of the insulator thickness, $t_{\mathrm{ox}} = [6, 1]\,\mathrm{nm}$, is shown in Figs. 2.12a and b, respectively. In both cases it can be seen that the capacitance variation is produced by C_{q}, while the total variation range is damped by the value of C_{ox}, because it is within the same range of C_{q}. Designing $C_{\mathrm{ox}} \gg C_{\mathrm{q}}$ would make the total capacitance tend to C_{q}, thus increasing its variation range, which is of interest for some particular applications, as will be shown in chapter 5, where the designs where that make use of MIG variable capacitance will be exhibited.

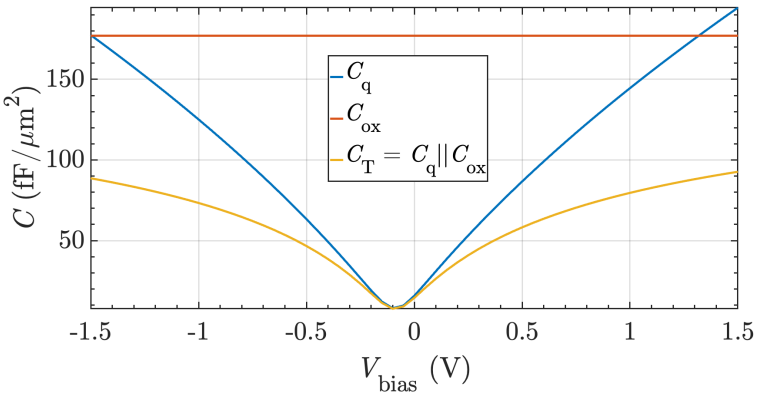
A solution to increase C_{ox} is to reduce the insulator thickness. However, this will increase the current on the device and thus the power consumption. Besides, direct tunnelling will also start to replace thermionic emission as the dominant conduction mechanism on the device, as aforementioned. On the other hand, making the insulator thicker will rapidly decrease the current conduction at the cost of losing capacitance variation range. As earlier discussed, the insulator thickness on the MIG diodes is a critical design parameter, and thus a trade-off should be achieved depending on the target application.

2.3.4. Equivalent circuit model

The equivalent circuit model of the MIG diode is shown in Fig. 2.13. It consists of a voltage-dependent current source, which models the current through the diode, and a voltage-dependent capacitance, modelling the series association of C_{ox} and C_{q}, both



(a)



(b)

Figure 2.12.: Capacitance-voltage characteristic of the MIG diode for (a) a 6 nm and (b) a 1 nm insulator.

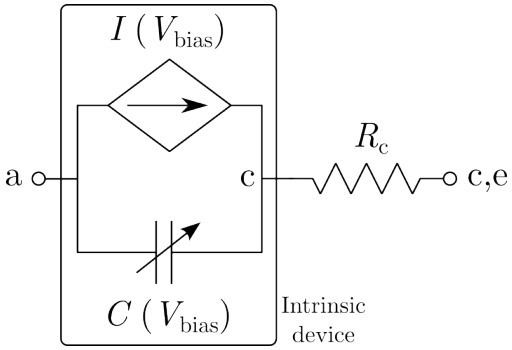


Figure 2.13.: MIG diode equivalent circuit model formed by a shunt connection of a voltage-dependent current source and a voltage-dependent capacitor.

shunt-connected. In addition, a series resistance R_{c} is added to account for the graphene contact resistance that is formed between the graphene and the top metallic contact.

2.3.5. FoMs of the MIG diode

MIG diodes have been already used in a variety of nonlinear applications such as power detection [25], [63], [80] or mixing [30], and it has also been seen that they outperform MIM diodes in terms of nonlinearity, responsivity and asymmetry, as shown in the comparison tables of [53], [62]. It is now time to define each of these FoMs, which gives the circuit and device designer an idea of how good or bad will a certain device perform on a specific task. On the one side, we would like to evaluate how well will the diode performs in nonlinear applications, such as rectifiers, power detectors or mixers, where a measurement of the nonlinearity of the $I-V$ curve is searched for. For that purpose, asymmetry, nonlinearity and responsivity are three useful FoMs, which are defined respectively as:

$$f_{\mathrm{ASYM}} = \left|\frac{J_{\mathrm{F}}}{J_{\mathrm{R}}}\right| \tag{2.12}$$

$$f_{\mathrm{NL}} = \frac{\mathrm{d}J/\mathrm{d}V}{J/V} \tag{2.13}$$

$$f_{\mathrm{RES}} = \frac{\mathrm{d}^2J/\mathrm{d}V^2}{\mathrm{d}J/\mathrm{d}V} \tag{2.14}$$

with J_{F} and J_{R} being the forward and reverse current density on the diode, respectively.

On the other hand, we are also interested on determining up to which frequency will the diode will properly work, which is given by the cutoff frequency, f_{c}. This FoM defines at which frequency the impedance of the parallel capacitor of the diode C equals the series resistance R_{s}, and can thus be evaluated as:

$$f_c = \frac{1}{2\pi R_s C} \tag{2.15}$$

In the case of the MIG diode, the series resistance is mainly formed by the contact resistance R_c due to its high value as shown in the equivalent diode model of Fig. 2.13 [81].

From the cutoff frequency expression, it is clear that reducing the series resistance and parallel capacitor as much as possible is desired in order to increase the cutoff frequency. In the case of the MIG diodes, even though the series resistance due to the metallic contact is lower compared to other technologies, the contact resistance between the metal and the graphene is much higher, increasing the overall series resistance and thus lowering f_c [53].

This FoM can be understood as the frequency value that makes the current on the diode to be filtered through the capacitor instead of contributing to the nonlinear behavior of the device. However, for applications where the $C-V$ characteristic wants to be exploited, most of the current circulating through the parallel capacitance is precisely the desired behavior, which exposes that f_c should not be understood as a global maximum frequency of operation for the MIG diode. It will always be the specific application where the diode is applied what defines the maximum frequency up to which the diode can work. For the circuit designer, FoMs should be thus looked as general reference values that allow for technology comparison rather than as non-breakable limits.

As a final remark, it is interesting to note that due to its variable capacitance coming from graphene's quantum capacitance, C_q, MIG diodes can be alternatively be used for nonlinear applications such as rectifiers or as varactors in applications where a change on the capacitance is beneficial, exposing the attractive double role that MIG diodes can play.

2.4. Conclusions

In this chapter, first, an introduction to graphene's electronic properties has been presented. Then, a closer look into graphene field-effect transistors (GFETs) and metal-insulator-graphene (MIG) diodes has been shown. Their physical description, working principle, main characteristic curves, equivalent models, and FoMs have been exposed.

GFETs show a very unique transfer characteristic, with a parabola alike shape close to the Dirac point. The peculiar conical band structure of graphene with valence and conduction band touching in only one point makes the device not to turn off. Besides, this gapless structure produces a curious output curve, in which a kink is observed in the so-called quasi-saturation region. In addition, the Dirac voltage is not fixed but changes with the drain plus the source voltages, which will be exploited in the design of frequency multipliers, as will be shown in Chapter 4. Finally, it has been shown how the cutoff frequency, f_T, seems to be competitive with other state-of-the-art technologies, while f_{max} lacks behind.

On the other hand, MIG diodes demonstrate superior performance in nonlinear applications due to their enhanced asymmetry, nonlinearity, and responsivity compared to MIM diodes, thanks to the graphene's Fermi level tunability. They also exhibit a variable capacitance thanks to graphene's quantum capacitance, which allows for their use as varactors in applications like phase shifters or voltage controlled oscillators.

Chapter 3.

Graphene-based devices: fabrication and characterization

This chapter presents the fabrication and characterization of MIG diodes and GFETs, devices presented in Chapter 2. In the case of the diode, the fabrication was performed by the author of the Thesis during a 6-months research stay at AMO GmbH, a non-profit research-oriented company in Aachen, Germany. The placement was done under the supervision of Prof. Dr.-Ing. Max Christian Lemme and Dr. Zhenxing Wang. As for the GFETs, after the mask was designed, the fabrication process was also performed at AMO GmbH, although as a part of an European project in which we participated, the 2D Experimental Pilot Line (2D-EPL), with reference 952792, funded by the European Union's Horizon 2020 research and innovation programme [82].

The contents of this chapter that correspond to the fabrication of the MIG diodes come from a mix of the acquired during the mentioned research stay by discussion, information gathering and experimentation, together with the contents exposed on, e.g., [83]–[86].

3.1. MIG diode fabrication process

The MIG diode fabrication process is illustrated in Fig. 3.1 and consists of the following steps, which will be later explained in detail:

1. Substrate preparation: Si + SiO_2 (90 nm)
2. M1: first metal deposition (bottom contact): Al (25 nm) + Ti (7.5 nm).
3. OX1: insulator deposition: TiO_2 (6 nm).
4. V1: via opening through the insulator and via filling: Ni (12.5 nm).
5. Gr: wet transfer of the graphene.
6. M2: last metal deposition (top contact): Ni (50 nm).

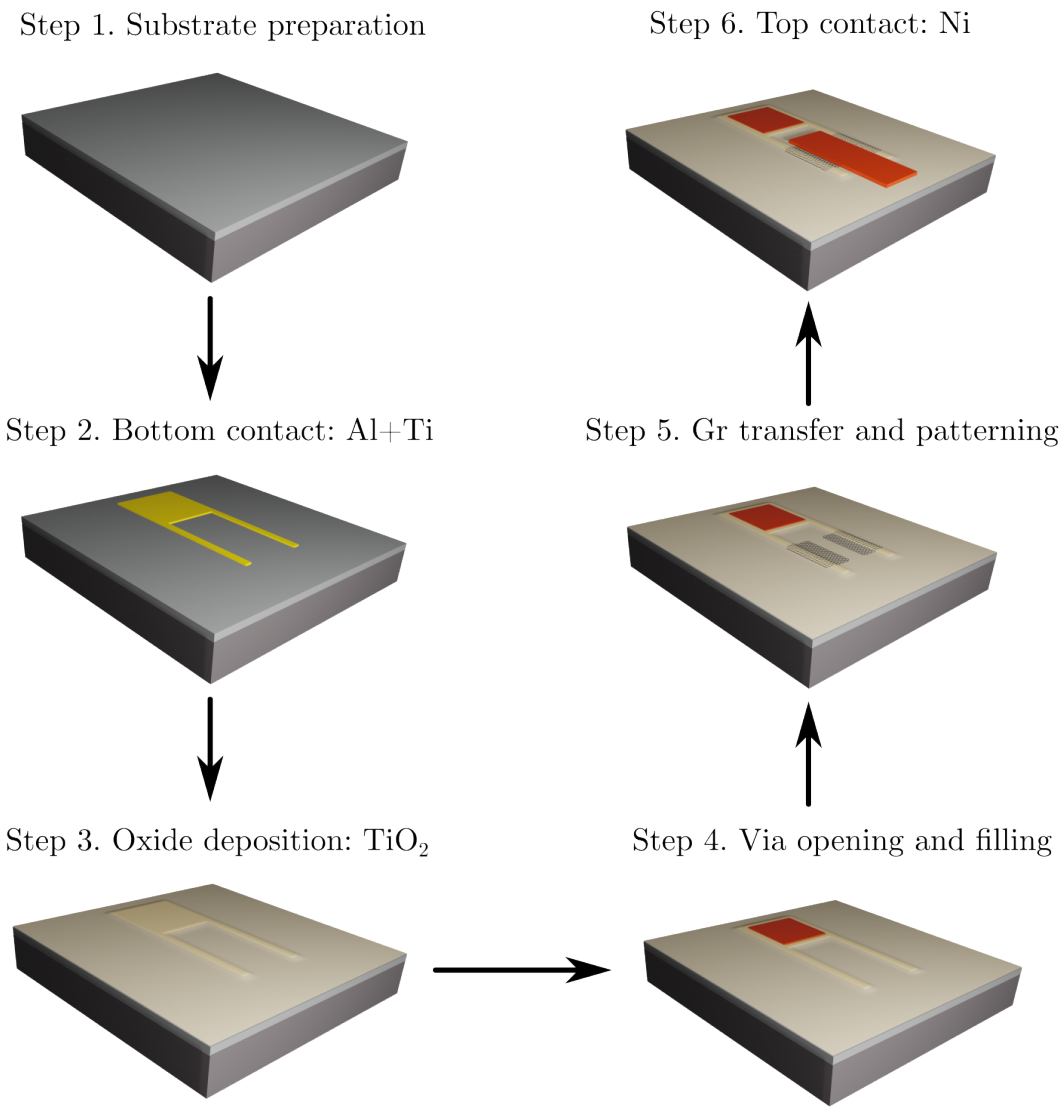
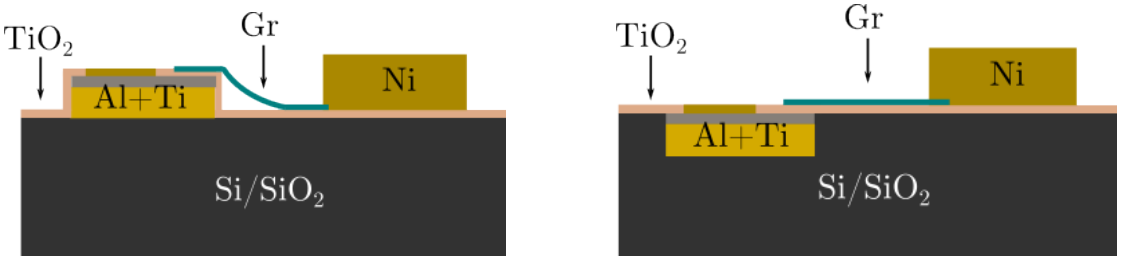


Figure 3.1.: Illustration of the fabrication process of the MIG diode.



(a) (b)

Figure 3.2.: Lateral view of the MIG diode fabrication process. The bottom contact formed by an Al+Ti stack, can be placed (a) on top of the substrate or (b) buried into the silicon substrate.

The side-view of the device fabricated according to the process described in Fig. 3.1 is shown in Fig. 3.2a. It can be observed that, due to the thickness of the bottom contact, the graphene layer is suspended between bottom and top contacts. An alternative process to the one followed here, which would allow for the graphene to lay flat on the device, consists in burying the bottom contact into the substrate, as can be observed in Fig. 3.2b [53]. In addition to the graphene being flat, this alternative process allows the metal stack comprising the bottom contact to be made thicker, which can improve the device performance when operated at high frequencies [63].

In the following, each of the fabrication steps will be described in detail. Please notice, some specific details are not shared in order to avoid any leak of protected information. In case of interest, please contact the author or advisors of the dissertation.

3.1.1. Substrate preparation

The first step consist of cleaning the substrate in order to remove any particle that could be on the surface. For this purpose, first, the 2×2 cm Si sample with 90 nm SiO_2 used in this process is dipped in acetone and ultrasonicated for 5 minutes. After that, the process is repeated in a new beaker with new acetone for another 5 minutes. Finally, the chip is dipped into isopropanol (IPA) and again ultrasonicated for another 5 minutes.

During this process, the acetone together with the ultrasonication eliminate most of the organic particles from the top of the sample. The IPA bath removes acetone residues. Finally, the IPA is removed via a nitrogen stream with a gun.

3.1.2. Bottom metal deposition

Once the sample has been cleaned, the next step is to deposit the bottom contact, a stack of 25 nm of Al (bottom) and 7.5 nm of Ti (top). In order to place the metal contacts in the desired location, a three-step process is followd: i) first, a photolithography is patterned; ii) then, the metals are deposited via e-beam evaporation; and iii) finally, a lift-off process removes the metal from the unwanted areas. These three steps are now

(a) (b)

Figure 3.3.: Resist profile illustration of (a) negative and (b) positive resist processing modes after development.

detailed.

Photolithography

For the lithography, a single-layer image reversal (IR) resist called AZ5214E is used in the negative mode. IR resists can be processed either in positive or in negative mode. Processing an IR resist in the negative mode means that the firstly-exposed areas remain, in contrast to operating them in the positive mode, where the exposed areas are removed. Although the negative mode process takes longer time in comparison with the positive one, it has the advantage that, once the resist is developed, it exhibits an undercut profile. This means that the sidewalls of the resist have less than 90 degrees (like a trapezoid with its lower base shorter than its upper one), allowing for the lift-off process, which will be later explained [83]. An illustration of both, negative and positive resist profile, is shown in Fig. 3.3.

The process states as follows: first, the AZ5214E resist is spin coated on the sample with an angular speed of $2400\,\mathrm{rpm}$ in order to get the desired resist thickness value of $1.8\,\mu\mathrm{m}$. Then, the sample is baked at $95\,^{\circ}\mathrm{C}$ during 2 minutes in order to harden the spin-coated liquid resist. After that, it is exposed with an ultraviolet (UV) light, to which the resist is sensitive, using a photolithography mask. This exposure weakens the bonds between the molecules within the resist only in the areas where the light penetrates the mask, according to the device layout design. After that, the sample is baked again at $115\,^{\circ}\mathrm{C}$ during 2 minutes, in the so-called post exposure bake (PEB) step, which strengthens the bonds of the previously weakened molecules within the exposed areas. The whole sample is next evenly exposed to the UV light, which now makes the unexposed areas on the first exposure step to be weakened. Finally, the sample is dipped in the developer, which removes the resist from the areas which were not initially exposed [83].

Deposition

Once the resist is patterned, an Al+Ti stack is e-beam evaporated using the e-beam and resistive evaporator FHR Star 200 EVA, single wafer system. The aluminum gives the contact some critical thickness, while the titanium makes it compatible with the subsequently deposited titanium dioxide (TiO_2). Depositing the metal via e-beam evaporation

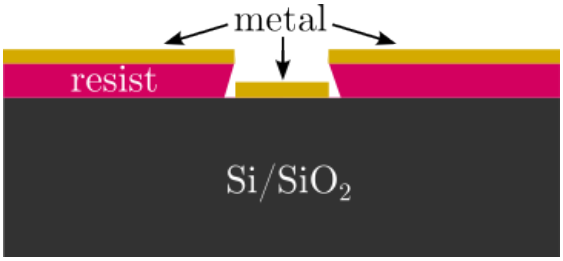


Figure 3.4.: Illustration of the sample right before the lift-off process.

produces a clean non-conformal anisotropic metal film [84], which allows for a successful lift-off process [83].

Lift-off

Once the Al+Ti metal stack has been deposited on top of the previously patterned resist, it is necessary to remove the metal from the unwanted areas. This is made with a lift-off process, where the sample is introduced in a beaker filled with hot acetone for at least half an hour. If an undercut profile has been developed in the resist, there will be a space between the metal deposited on the resist and the metal deposited on the cavities. The acetone will then be able to come into contact and dissolve the resist, thus lifting the metal on its top. An illustration of the sample right before introducing it in the acetone is shown in Fig. 3.4 [83]. After removing the sample from the acetone, it is directly introduced in an IPA bath.

Several considerations should be taken into account for a successful lift-off process. First, it is of great importance to introduce the samples in the acetone once this is already heated. The temperature shock between the sample and the acetone seems to help to produce a quicker and better lift-off. In addition, a pipette can be used to "blow" the sample while in the acetone, so that the metal pieces that might have begun to detach from the sample can be mechanically helped to permanently detach. On the other hand, the exact time that the samples must stay in the acetone bath cannot be determined beforehand, but has to be visually determined when all the metal layer detaches from the sample. In principle, longer times in the acetone provide a better lift-off, but the relation is not linear: most of the times the lift-off occurs in the first minutes.

A relatively common issue during the lift-off process is that the metal is not completely removed from the sample. If that happens, a quick solution consists in using ultrasonication, which improves the lift-off at the cost of breaking the detached metal pieces into tiny pieces that mix with the acetone, thus being not anymore possible to distinguish, with the naked eye, when the lift-off has finished. This procedure cannot be used once the graphene or any 2D material has been transferred to the sample, as it will break the van-der-Waals bonds between the 2D material and the substrate, which will delaminate as a consequence. Finally, it is also important to note that, once the sample is removed from the acetone bath, introducing it again will not improve the lift-off, which means that this is a one-trial process.

3.1.3. Oxide deposition: TiO_2

Right after the bottom contact fabrication has been completed, the deposition of the titanium oxide (TiO_2) is made via atomic layer deposition (ALD) with the Oxford Instruments FlexAL ALD tool, in a process that uses titanium tetrachloride ($TiCl_4$) and oxygen as precursors and an oxygen plasma at $300°C$.

In each ALD cycle, the precursors are consecutively pumped in and out of the chamber where the sample is placed, producing a self-limiting chemical reaction on the surface of the sample which produces a one-molecule thickness layer on the sample [86]. The number of ALD cycles is thus key in order to get the desired thickness of $6\,nm$. As a control technique for this thickness, a dummy Si sample is processed inside the ALD chamber together with the target sample within the same process, and afterwards measured with the PQ Ruby Philips ellipsometer. For the ellipsometer measurement to be precise, a dummy Si sample without oxide on top (except from the native SiO_2 of around $1.5\,nm$, which can not be avoided). Within this fabrication process, a thickness of $t_{ox} = 5.66\,nm$ was measured.

3.1.4. Via opening and filling

In order to contact the Al+Ti stack from the top of the device after the TiO_2 has been deposited, a via needs to be opened through the oxide.

First, for the lithography, a double-layer resist stack is used (AZ5214E + LOR3A). The one on the top is the same IR resist used during the M1 deposition step, and the one underneath is LOR3A, a polymer which dissolves on a solvent different from the acetone called DMSO. Thus, after appropriate exposure, the sample is developed using MF26A developer to which the bottom resist is sensitive. The resist on top will only develop on the exposed areas, while the resist underneath will continue to dissolve, forming an undercut profile even more pronounced than with the IR resist operated in negative mode, with a mushroom-like shape as can be seen in Fig. 3.5. This double-layer process has some advantages against the single-layer case, such as an easier lift-off and a thicker resist stack. The latter allows for thicker depositions or, as in this case, for deeper etching processes.

Once the resist is patterned, for the etching of the oxide, a so-called reverse sputtering process is employed, which consists in using the Sputtering Creavac Creamet500s tool without any target material. In this way, the argon (Ar) ionized gas will collide with the TiO_2 molecules and provide them enough kinetic energy to detach from the surface of the sample [86]. Once the vias are opened, they are straightaway filled with nickel (Ni) also via sputtering, in order to avoid breaking the vacuum that would cause the exposed Al+Ti bottom contact to oxidize.

Figure 3.5.: Illustration of the profile of a double layer resist after development. Both, pink and orange, represent the two resists on the resist stack.

3.1.5. Graphene transfer and patterning

The graphene transfer process is illustrated in Fig. 3.6. First, and before the transfer process starts, an auxiliary layer of poly(methyl methacrylate) (PMMA) is spin coated on top of the CVD graphene, which is acquired from Grolltex©, and subsequently baked, in order to provide mechanical stability to the graphene layer during the rest of the transfer process (steps 1 to 3 in Fig. 3.6).

Once the PMMA is deposited, the copper underneath is etched by dipping the stack copper-graphene-PMMA (from bottom to top) in a hydrochloric acid solution (H_2O + H_2O_2 + HCl) (step 4 in Fig. 3.6). After some time, the copper is completely etched and, after dipping the stack (now graphene-PMMA) in deionized (DI) water again to remove any residues from the acid solution, the sample is vertically positioned on a shelf to naturally dry.

Once the water has dried out, the graphene-PMMA stack is transferred onto the sample and subsequently baked, in order to help the graphene layer to fully attach to the substrate (step 5 in Fig. 3.6). Finally, the PMMA auxiliary layer is removed with an acetone bath, and the graphene transfer is completed (steps 6 and 7 in Fig. 3.6).

In order to remove the transferred graphene from the unwanted areas, an oxygen plasma is used inside a reactive-ion etching (RIE) chamber, for the so-called graphene patterning. For the lithography, as this is an etching step and not a deposition step like with metal depositions, there is no need to do a lift-off. An IR resist processed in the positive mode is used. The oxygen molecules accelerate and impact the graphene layer in those areas which are not covered by the resist, removing it.

3.1.6. Top metal deposition

Finally, for the lithography of the deposition of the top metal, first a lift-off process equal to the one used for the bottom contact in Section 3.1.2 is used. Then, the 50 nm Ni metallic contact is evaporated on top using e-beam evaporation. After this step, the fabrication process is finished.

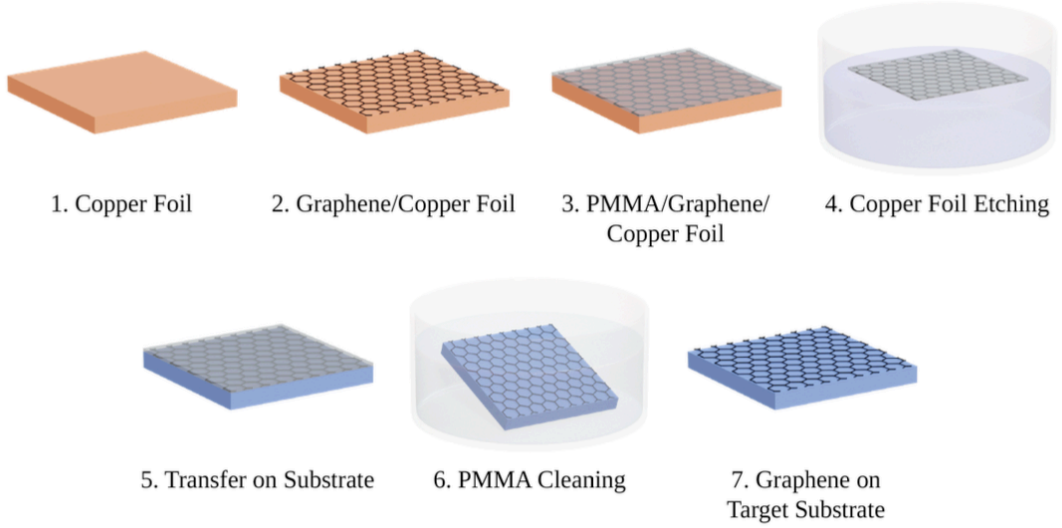


Figure 3.6.: Illustration of the graphene transfer process. Image taken from [87].

3.2. MIG diodes characterization and compact model

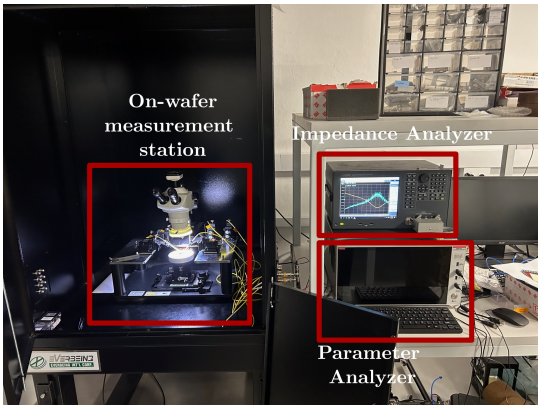
3.2.1. Characterization

Electrical characterization of fabricated MIG diodes was performed at the Pervasive Electronics and Advanced Research Laboratory (PEARL) of the University of Granada. The characterization includes DC and AC measurements, in order to extract the current-voltage ($I_{\text{th}} - V_{\text{bias}}$) and capacitance-voltage ($C - V_{\text{bias}}$) characteristics, respectively.

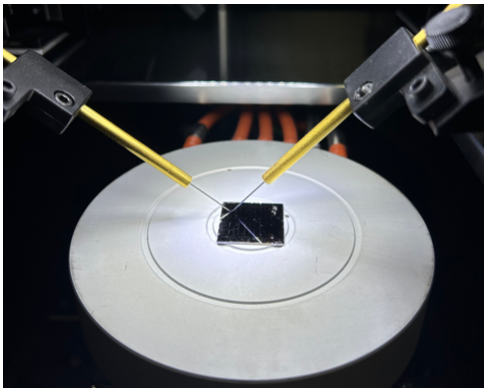
DC measurements were made with a Keithley 4200A-SCS parameter analyzer, with 4200 PA source measure units (SMUs), while AC measurements were performed with a Keysight E4990A Impedance Analyzer, using the 16048G 1 meter extension at a relatively low frequency of 1 MHz, in order to avoid parasitic effects from different sources. For contacting the sample, an Everbeing C-3 on-wafer measurement station from Everbeing Int'l Corp was used. The setup configuration is shown in Fig. 3.7.

The complete mask layout designed for the fabrication of the MIG diodes is shown in Fig. 3.8a and a microscope image of the fabricated chip is exhibited in Fig. 3.8b. Fig. 3.9a depicts the mask of one of the MIG diodes of the chip, labeled I15, while Fig. 3.9b shows a microscope image of the same device, which has six fingers, with a size of $W \times L = 70\,\mu\text{m} \times 4\,\mu\text{m}$ per finger, and an access region of $1\,\mu\text{m}$ due to the photolithography resolution. This access region is undesired, as it is not only useless for the device operation but also provokes parasitics to appear at high frequencies, and should therefore be reduced as much as possible in future runs.

While the current characteristics of the device are straightforwardly achieved, extracting the $C - V_{\text{bias}}$ curve from the measured impedance, Z_{in}, is a bit more complex. For



(a)



(b)

Figure 3.7.: (a) DC and AC measurement setup for the MIG diodes, showing the on-wafer probe station and the measurement equipments. (b) Detail of the probes contacting the self-fabricated sample.

that purpose, an analysis of the equivalent circuit of the measurement setup is needed. This is shown in Fig. 3.10, where the voltage-dependent current source $I(V_{\mathrm{bias}})$ of Fig. 2.13 has been substituted by a variable resistor, $R_{\mathrm{p}}(V_{\mathrm{bias}})$, which allows the impedance modeling of the MIG diode.

Solving the circuit for Z_{in}, the following equations system is obtained:

$$\begin{cases} \mathrm{Re}\{Z_{\mathrm{in}}\} = R_{\mathrm{c}} + \frac{G_{\mathrm{p}}}{G_{\mathrm{p}}^2+\omega^2 C^2} \\ \mathrm{Im}\{Z_{\mathrm{in}}\} = \frac{-\omega C}{G_{\mathrm{p}}^2+\omega^2 C^2} \end{cases} \tag{3.1}$$

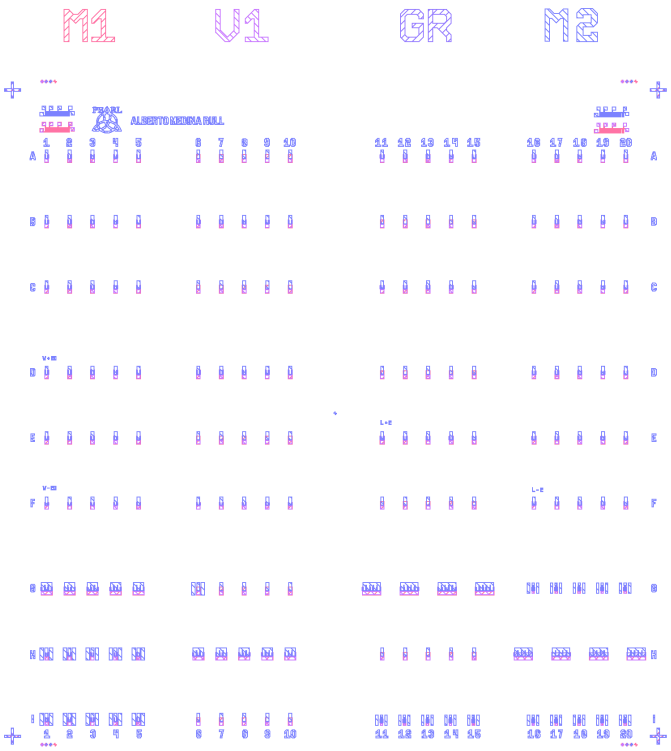
where $G_{\mathrm{p}} = R_{\mathrm{p}}^{-1}$. There are three unknowns to be evaluated: $R_{\mathrm{p}}(V_{\mathrm{bias}})$, $C(V_{\mathrm{bias}})$ and R_{c}; but only two equations, given by the real and the imaginary part of the measured input impedance, Z_{in}. It is though possible to first obtain the R_{c} value profiting from the bias case $V_{\mathrm{bias}} = 0\,\mathrm{V}$, where $R_{\mathrm{p}} \to \infty$ and the equivalent circuit model of the diode is thus reduced to the contact resistance R_{c} series connected to the variable capacitance $C(V_{\mathrm{bias}})$, so that the real part of Z_{in} equals R_{c}:

$$R_{\mathrm{c}} = \mathrm{Re}\{Z_{\mathrm{in}}\}\Big|_{V_{\mathrm{bias}}=0\,\mathrm{V}} \tag{3.2}$$

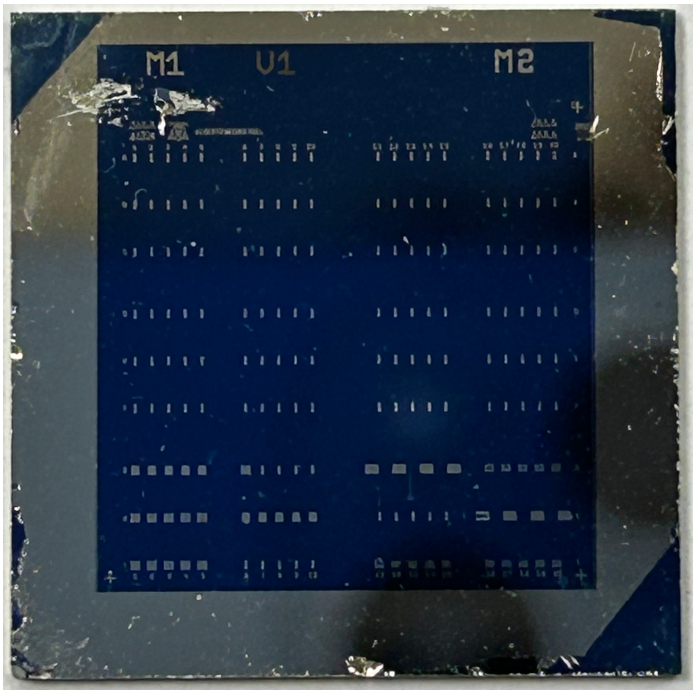
Provided that the value of R_{c} has been evaluated, the equation system (3.1) can be solved for G_{p} and C as:

$$G_{\mathrm{p}} = -\frac{R_{\mathrm{c}} - \mathrm{Re}\{Z_{\mathrm{in}}\}}{R_{\mathrm{c}}^2 - 2R_{\mathrm{c}}\,\mathrm{Re}\{Z_{\mathrm{in}}\} + \mathrm{Im}\{Z_{\mathrm{in}}\}^2 + \mathrm{Re}\{Z_{\mathrm{in}}\}^2} \tag{3.3}$$

$$C = -\frac{\mathrm{Im}\{Z_{\mathrm{in}}\}}{\omega R_{\mathrm{c}}^2 - 2\omega R_{\mathrm{c}}\,\mathrm{Re}\{Z_{\mathrm{in}}\} + \omega\,\mathrm{Im}\{Z_{\mathrm{in}}\}^2 + \omega\,\mathrm{Re}\{Z_{\mathrm{in}}\}^2} \tag{3.4}$$

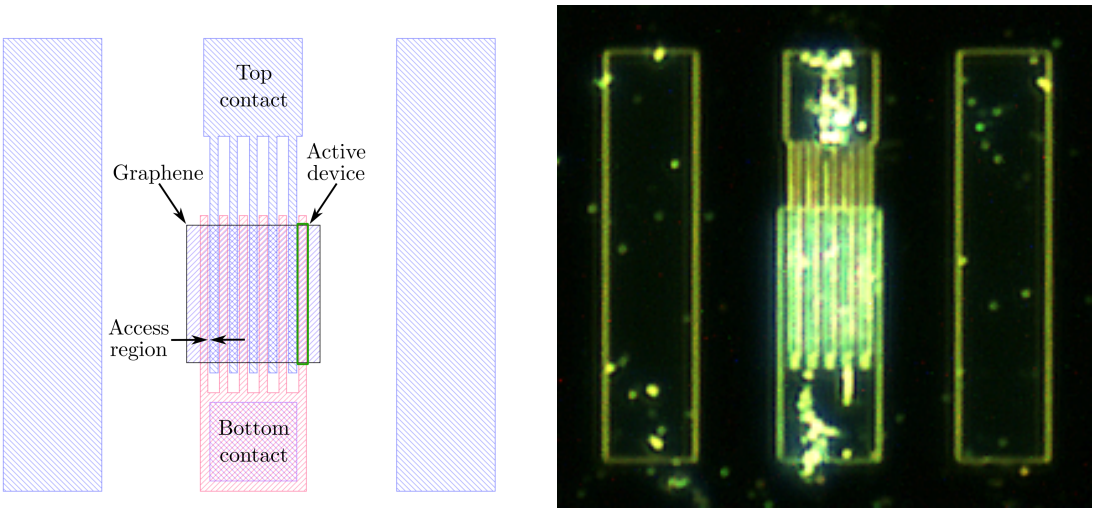


(a)



(b)

Figure 3.8.: a) Mask layout chip containing, among other devices, the MIG diodes. b) Microscope image of the chip.



(a) (b)

Figure 3.9.: a) Mask of I15 multifinger MIG diode. b) Microscope image of device I15.

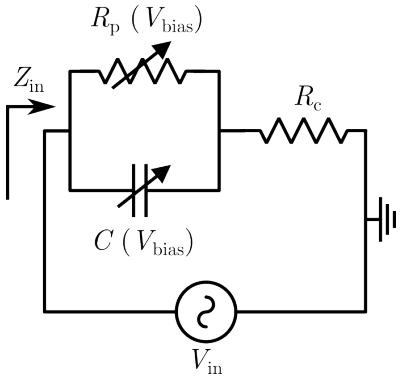


Figure 3.10.: MIG diode $C-V$ measurement setup equivalent circuit.

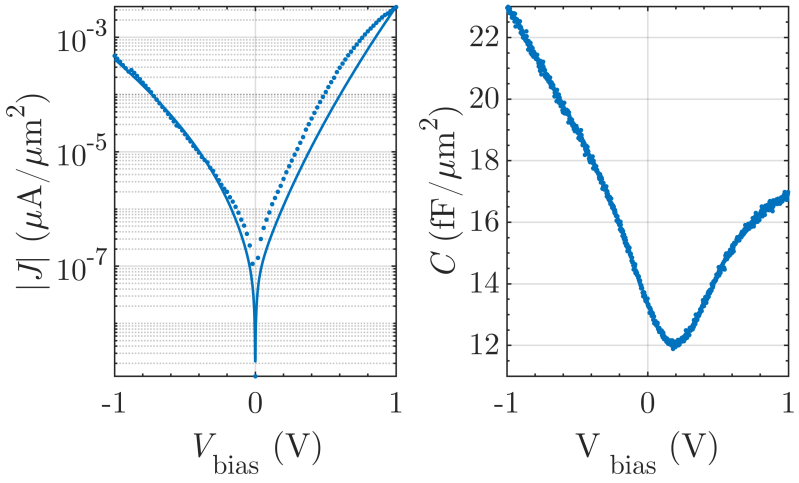


Figure 3.11.: Measured a) $|J| - V_{\text{bias}}$ and b) $C - V_{\text{bias}}$ characteristic of device I15.

Figures 3.11a and b show, with dots, the $|J| - V_{\text{bias}}$ and $C - V_{\text{bias}}$ experimental curves corresponding to the device I15, where, in order to attain the $C - V$ characteristic, eqs. (3.3) and (3.4) have been employed. Figure 3.11a shows with a solid line the result of the simulation of the MIG diode in ADS after conveniently fitting the model parameters. The values of the fitting are the ones shown in Fig. 3.12.

3.2.2. Compact model

In order to model the behavior of the MIG diode, a large-signal model developed in [78] is implemented in Verilog-A and included in ADS as a computer-aided design (CAD) tool. The intelectual property (IP) of the CAD tool is protected under registration through the Benelux Office for Intellectual Property (BOIP) [88].

The model is shown in Fig. 3.12, where "L_g" and "W_g" are the device length and width, respectively; "t_{ox}" and "kappa" are the oxide thickness and dielectric constant, respectively; "W_m", "W_{m2}" and "W_g" are the work function of the anode metal, cathode metal and graphene, respectively; and "Q_o" is the sum of fixed charge, constant interface trapped charge and possible chemical doping. The parameters shown are tuned in order to fit the experimental $J - V_{\text{bias}}$ measurement of the fabricated I15 device.

3.3. GFET fabrication through the 2DEPL

As part of the Graphene Flagship, an European research project among different research institutions in Europe, the 2D Experimental Pilot Line (2D-EPL), with reference number 952792, funded by the European Union's Horizon 2020 research and innovation programme, was launched in 2021 in order to provide device and circuit designers

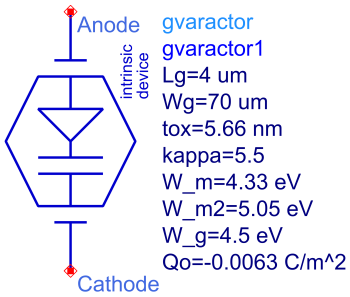


Figure 3.12.: MIG diode compact model embedded into ADS.

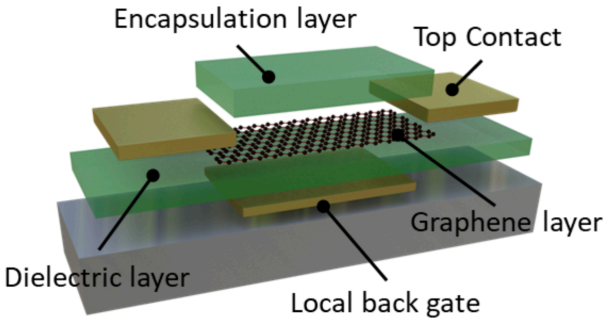


Figure 3.13.: Illustration of the GFET fabrication process taken from the 2D-EPL fact sheet.

with a platform to be able to get their 2D materials-based devices/circuits fabricated. Thus, the devices shown here were fabricated as part of the MPW run 3 at AMO's GmbH foundry, which offered the fabrication of GFETs with the process illustrated in Fig. 3.13 and summarized in Table 3.1.

According to the layer distribution, we designed the mask layout including many different GFETs designs, which can be seen in Fig. 3.14a. A microscope image of the fabricated chip is shown in Fig. 3.14b. As an example, Fig. 3.15a shows the mask design of four single GFETs, where G, D, S and Gr state for gate, drain, source and graphene, as marked in the Figure. Fig. 3.15b shows a microscope image of the same four devices, once fabricated. It can be observed that the devices have two fingers, and the length and width of the channel of each finger are: $L_g = W_g = 10\,\mu m$, for the B row, and $L_g = 20\,\mu m$, $W_g = 10\,\mu m$, for the C row. All of them have a $10\,\mu m$ access region, as the design rules for the process set the minimum spacing between layers at $10\,\mu m$. Thus, the smallest possible device channel length was $10\,\mu m$, which corresponds to the devices on

Layer	Material	Thickness
Rigid substrate	Si/SiO_2	90 nm
1 Back Gate Contact	Ti/Pd	5/40 nm
2 Dielectric	Al_2O_3	40 nm
3 Adhesion layer for Top Contact Pad	Ni	25 nm
4 Graphene	Single layer	CVD on Cu
5 Top Contact	Pd	40 nm
6 Encapsulation	Al_2O_3	80 nm

Table 3.1.: Details of the fabrication process of the GFET offered by the 2D-EPL showing the layers, materials, and thicknesses.

Parameter	Target	Result
Graphene mobility	$> 1000\,cm^2/Vs$	$872\,cm^2/Vs$
Average sheet resistance	$1\,k\Omega$	$0.7\,k\Omega$
Average contact resistance	$1\,k\Omega\mu m$	$1.1\,k\Omega\mu m$
Minimum working devices	$> 80\%$	86%
Dirac Point	$< 15\,V$	13 V

Table 3.2.: Target and result parameters of the reference devices of the corresponding MPW from which the measured devices originate.

row B. It can also be observed that the devices layout is designed in order to be able to contact them with ground-signal-ground (GSG) probes for their RF characterization.

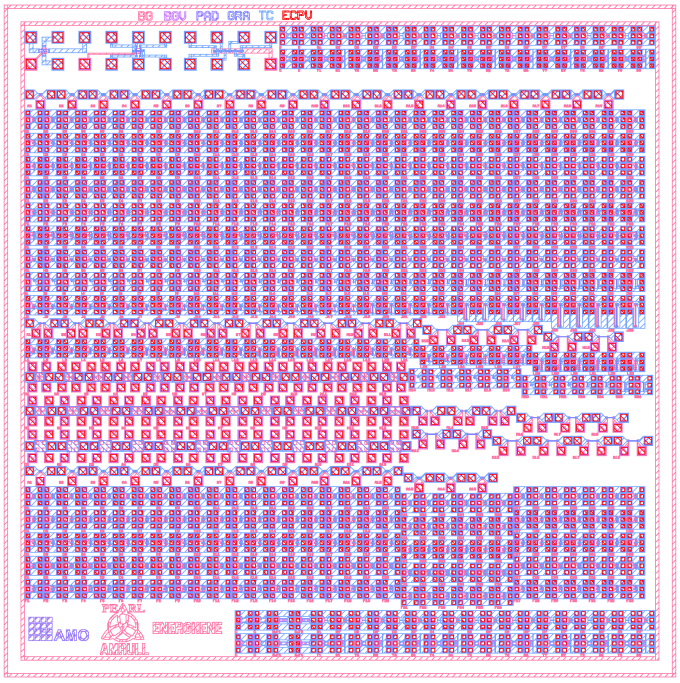
Finally, Table 3.2 shows the target and the results from the fabrication process in terms of mobility, sheet and contact resistances, percentage of working devices, and Dirac point shared by the manufacturer (AMO GmbH) within the final report. These results expose a mobility slightly lower than the target, a higher average contact resistance, and a relatively high Dirac voltage though within the target. On the other hand they show a higher than expected yield, and a lower than expected average sheet resistance.

3.4. GFETs characterization and compact model

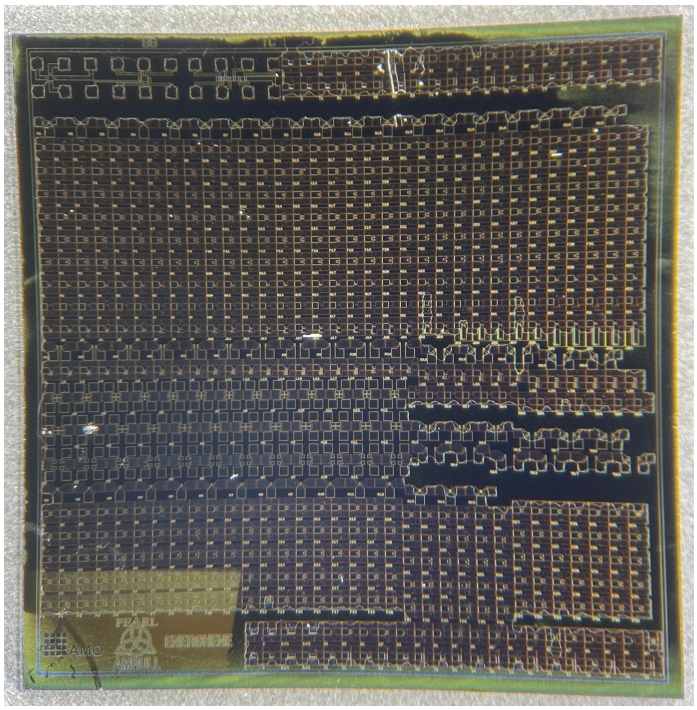
3.4.1. Characterization

For the characterization of the GFETs, a DC setup has been employed, also performed with the Keithley 4200A-SCS parameter analyzer and the 4200 PA SMUs, and with the on-wafer measurement station Everbeing C-3 from Everbeing Int'l Corp, with three DC probing tips for each terminal.

The measured transfer curves of one the GFETs from row C, with $L = 20\,\mu m$, a width of $W = 10\,\mu m$ (for only one of the fingers) for different V_{DS} values are shown in Fig. 3.16, together with the simulation results from ADS after conveniently fitting the GFET model, showing a reasonable agreement. The GFET simulation symbol with its adjusted

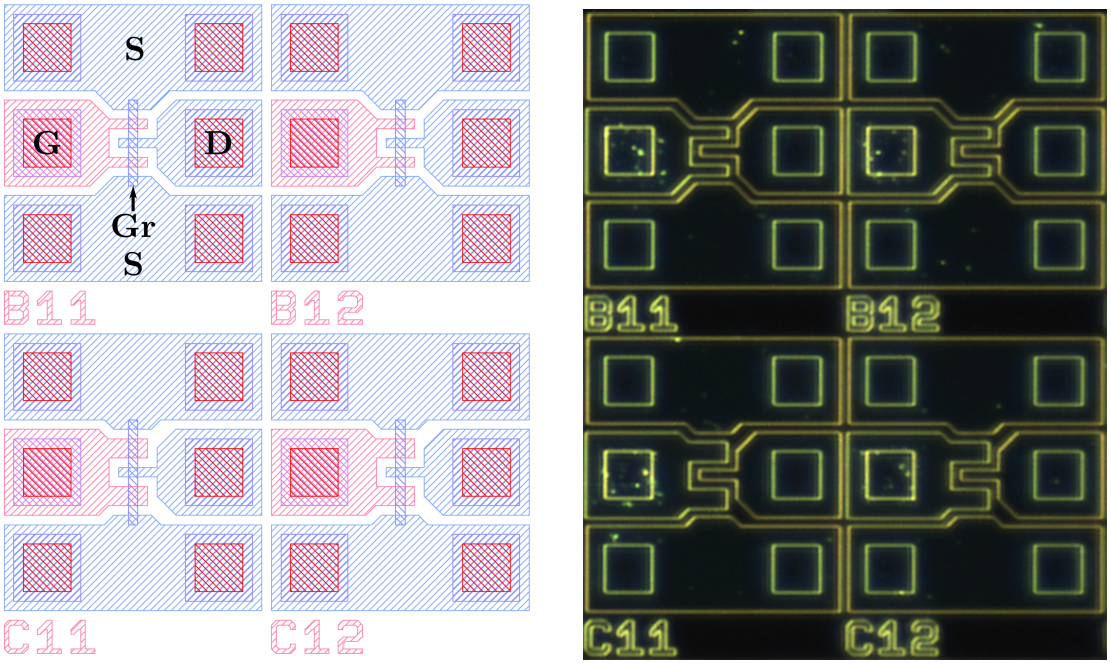


(a)



(b)

Figure 3.14.: a) Mask layout of the chip containing the design for the MPW run 3 of the 2D-EPL. b) Microscope image of the chip.



(a) (b)

Figure 3.15.: a) Mask design of four GFETs with channel lengths of 30 µm (row B) and 40 µm (row C). b) Microscope picture of the same devices.

parameters to fit the measurements, are shown in Fig. 3.17. Contact resistances and access regions are also included in the simulation schematic, though not shown here. It can be seen how the increase in the drain-to-source voltage shifts the Dirac point, as stated in eq. (2.4). The Dirac point is located around $V_{\mathrm{Dirac}} = 24\,\mathrm{V}$, a little higher than the value on the manufacturer report of Table 3.2.

3.4.2. Compact model

As with the MIG diode, a large-signal model of the GFET, derived in [71], is implemented in Verilog-A and included in ADS. The IP of the CAD tool is protected under registration through the BOIP [89].

The resulting schematic symbol together with its parameters is shown in Fig. 3.17, where "L_g" and "W_g" are the channel length and width, respectively; "tox_top" and "kappa_top" are the thickness and permittivity of the top oxide; "V_{gso}" is the offset voltage, which accounts for the possible doping of graphene and which directly shifts the Dirac point as governed by eq. 2.4; "Delta" is the potential inhomogenity of electron-holes puddles; and "mu" is the effective mobility of graphene. The values depicted in Fig. 3.17 correspond to the fitting of the technology which produces the simulation results shown in Fig. 3.16.

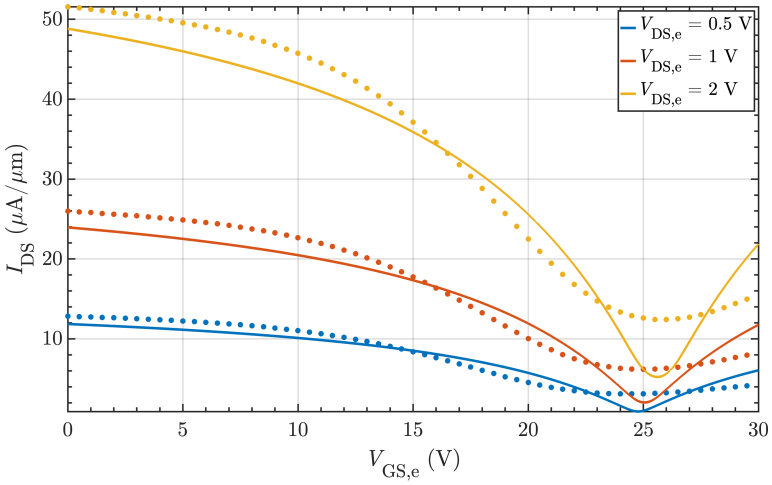


Figure 3.16.: Transfer curve of one of the fingers of a GFET from row C, with a channel length of $L = 20\,\mu m$, a width of $W = 10\,\mu m$, for $V_{DS,e}$ values from 0.5 to $2\,V$. Solid lines represent the simulation in ADS using the fitted GFET model, and the dots are the experimental measurements.

3.5. Conclusions

In this chapter, the fabrication and characterization processes of MIG diodes and GFETs have been addressed.

For the MIG diode, the fabrication process consists of six steps: i) substrate preparation, ii) bottom contact deposition, iii) TiO_2 deposition, iv) via opening and filling, v) graphene transfer and patterning, and vi) top metal deposition. Each step has been detailed and thoroughly explained throughout the chapter.

Challenges encountered during cleanroom fabrication have also been reported. Lift-off processes, crucial for patterning the metal contacts, can be susceptible to incomplete metal removal, potentially affecting device performance. Additionally, the side-view geometry with a suspended graphene layer potentially impact device performance, which could limit high-frequency operation. Exploring alternative fabrication techniques, such as those employing buried bottom contacts, could mitigate these limitations by enabling thicker, more robust bottom contacts.

In the case of the GFETs, the designed devices were fabricated through the 2D-EPL.

The characterization of both, MIG diodes and GFETs, has been performed at the PEARL facilities at the University of Granada. The DC characteristics were straightforwardly obtained in both cases and show the expected behavior, matching the simulations. As for the AC characterization, in the case of the $C - V_{bias}$ curve of the MIG diode, taking parasitics of the specific setup into account has been checked as a critical need for the success of the process, providing the equations needed to extract the variable capacitance as a function of the voltage from the impedance analyzer measurement. The

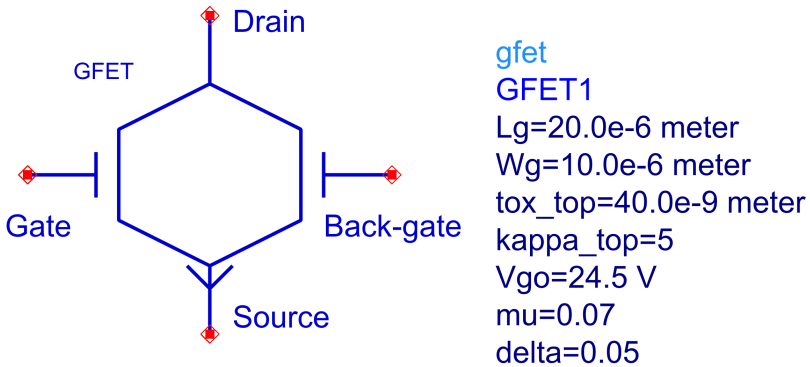


Figure 3.17.: GFET schematic symbol with its parameters showing the values that fit the measurements of a fabricated device from row C of the 2D-EPL.

AC characterization of the GFETs is being currently performed and therefore it cannot be included in this dissertation.

Part III.

RF circuit designs

Chapter 4.

GFET-based RF circuit designs

4.1. Introduction

This chapter presents four different designs based on graphene-FETs, in the following order: a phase shifter, an amplifier, a frequency multiplier and an oscillator, each of them exploiting a different and unique property of the graphene-based device. In every design, the compact simulation model of the GFET presented in Chapter 3 is employed, and its parameters are adjusted to a fabricated technology in order to validate the simulation results.

The successful realization of the four circuits advances on the RF circuit design based on graphene-based devices, and has the goal of paving the way towards the eventual inclusion of graphene-based devices into more complex systems such as radas or antenna arrays, or in any other system where their benefits could be leveraged.

The content of this chapter is an adaptation of published and submitted journal papers and conferences, as specified at the beginning of each section.

4.2. GFET model fitting

Before starting with the circuit designs, a fitting procedure of the GFET large-signal model that validates the simulation results is needed. This adjustment process has to consider both, DC and RF characteristics of the fabricated device. Fig. 4.1 graphically illustrates the adjustment process that has been followed throughout this Chapter:

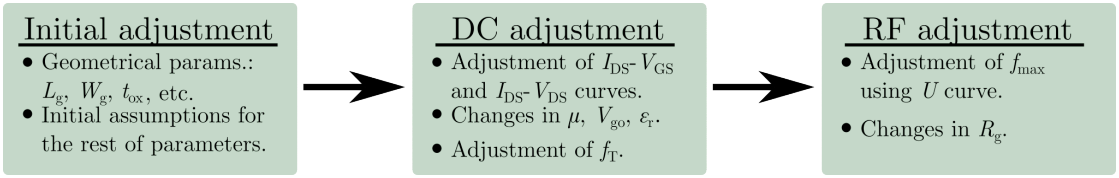


Figure 4.1.: Adjustment process of the GFET large-signal simulation model in order to fit the experimental measurements.

1. First, the geometrical and measured parameters of the device according to the information provided by the manufacturing partners are set , e.g., L_{g}, W_{g}, t_{ox}, $R_{\mathrm{d,s}}$, and μ, and for the rest of the parameters an initial assumption is made.

2. Then, in order to adjust the DC curves, the parameters that mostly impact the current density of the device, the Dirac point, and the shape of the parabola of the transfer curve, and that have not been fixed in the previous step, e.g., ϵ_{r}, V_{go} and n_{res}, are adjusted. The cutoff frequency, f_{T}, also depends on the current, and thus it will be simultaneously adjusted in this step.

3. Finally, in order to adjust the value of the maximum oscillation frequency, f_{max}, the value of the gate resistance, R_{g}, is adjusted. This parameter directly controls the position of f_{max} and has no impact on the DC characteristics, being therefore reserved as the last parameter to fit.

As a final remark of this process, it is important to note that every device and every manufacturing partner is different, and for that reason the parameters of the model to adjust on each step can significantly vary from one device to another.

4.3. Phase shifter: leveraging graphene's quantum capacitance

The following section is an adaptation of the journal paper [90] titled: "A graphene field-effect transistor based analog phase shifter for high-frequency applications", published in *IEEE Access* in November 2020 by the following authors: Alberto Medina-Rull, Francisco Pasadas, Enrique G. Marín, Alejandro Toral-Lopez, Juan Cuesta, Andrés Godoy, David Jiménez, and Francisco G. Ruiz.

4.3.1. Introduction

Even though phase shifters are well-known RF systems, the design of purely analog architectures, advantageous due their higher precision and speed and reduced complexity, has been technologically limited to two main approaches. First, the use of varactors as periodical loads of transmission lines, so to modify the equivalent circuit capacitance with a control voltage [91]–[94], which due to its passive nature will always present some (IL). Second, the implementation of transistor-based architectures either in all-pass filter configurations, with a flat amplitude passing band and a voltage-dependent phase [95], or emulating the varactor structure by employing high electron mobility transistors [96].

An alternative strategy is to look for phase variations based on quadrature amplitude modulation (QAM) techniques, where the so-called in-phase and quadrature signals (I/Q), with a 90° phase difference between each other, feed two variable-gain amplifiers (VGAs), and are later added up. The resulting phase shift is controlled by changing

the relative amplitudes of the I/O signals [97]–[102]. This strategy, results in quite complex circuits (including the I/Q generator, VGAs, and signal adders) as well as a digital control system.

However, in spite of the increasing number of effective prototypes of graphene RF devices such as GFETs [103], as well as one-dimensional (1D) flexible RF diodes [57], none of these systems have still explored the potential application of graphene or related two-dimensional materials to the aforementioned purpose. In this context, a bias-controlled analog phase shifter based on a GFET is here proposed, by taking advantage of the possibility of tuning the graphene quantum capacitance with the FET terminal biases thanks to its low density of states around the Dirac point [104], as explained in Chapter 2.

Not only it is the use of graphene-based technology for this application novel and relevant, but also the fact that the phase shift can be controlled solely by an analog signal, without impacting its gain. In this regard, the proposed phase shifter architecture consists of only one device and the role of the control signal is played by the gate bias with the drain bias linearly depending on it. When only one transistor is considered, a 85° phase shift can be achieved, keeping a gain of $0\,$dB with a maximum variation of $1.3\,$dB. In order to reduce the source mismatch, the design is improved by applying a balanced branch-line amplifier configuration, which provides return losses higher than $30\,$dB. The performance and main FoMs of the proposed graphene-based phase shifters are compared against the state-of-the-art, with promising results.

4.3.2. Graphene FET as phase shifter

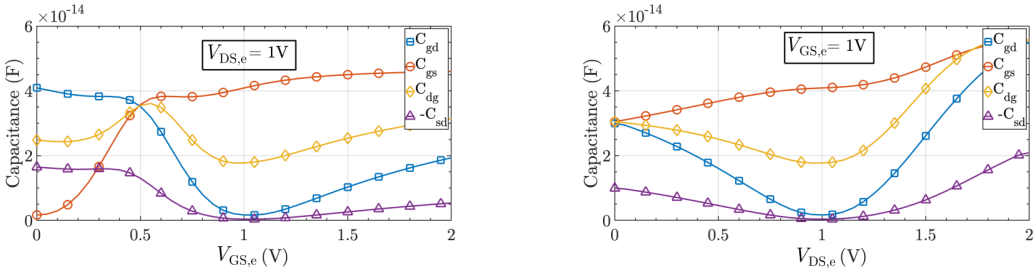
The design and analysis of an RF phase shifter founded in graphene, requires first a physics-based description of the electrical behavior of a GFET, at a compact and analytical level suitable for standard circuit simulators. To this purpose, we employ the large-signal model implemented in Verilog-A by some authors [105], embedding it into Advanced Design System. This GFET compact model has been thoroughly validated in [106] by the assessment of DC, transient dynamics, and frequency response of a variety of graphene-based circuits such as a HF voltage amplifier [107], a high-performance frequency doubler [108], a subharmonic mixer [109], and a multiplier phase detector [110] showing very good agreement between measurements and simulations. Therefore, its use here to explore the feasibility of using GFETs to build RF analog phase shifters is sufficiently justified.

In order to proceed with the device-level analysis, Table 4.1 summarizes the graphene technology parameters considered for this design.

As already mentioned, the inspirational property of a GFET that postulates it as a candidate to be the core of an active analog phase shifter is the bias-tunable quantum capacitance originated by the reduced density of states of graphene around the Dirac point [104]. To take advantage of this inherent property, the graphene quantum capacitance, C_{q}, has to be dominant over the gate geometrical oxide capacitance, $C_{\mathrm{ox}} = \epsilon_0 \epsilon_{\mathrm{ox}} / L_{\mathrm{t}}$, as explained in section 2.3.3. In a MIG structure C_{ox} and C_{q} are working in series [114], therefore, achieving a design with $C_{\mathrm{ox}} \gg C_{\mathrm{q}}$ allows to leverage the C_{q} tunability. This

Param.	Value	Param.	Value
L_g	$1\,\mu m$	μ	$0.2\,m^2/Vs$
W_g	$1\,\mu m$	V_{go}	$0\,V$
C_{ox}	$0.11\,pF\mu m^{-2}$	$R_{d,s}W_g$	$100\,\Omega\mu m$ [111]–[113]
n_{res}	$6.86 \times 10^{11} cm^{-2}$	R_gL_g	$5\,\Omega\mu m$

Table 4.1.: GFET technology for the phase shifter design.



(a) (b)

Figure 4.2.: Intrinsic capacitances C_{gs} (red circles), C_{gd} (blue squares), C_{sd} (yellow diamonds) and C_{dg} (purple triangles) of the GFET employing the technology summarized in Table 4.1 versus (a) gate-to-source bias and (b) drain-to-source bias.

effect can be observed by analyzing the intrinsic device capacitances (C_{ij}) of the GFET which relate the incremental charge (ΔQ_i) at a terminal i with a varying voltage (ΔV_j) applied to a terminal j assuming that the voltage at all the other terminals remains constant [105],

$$C_{ij} = \begin{cases} -\frac{\partial Q_i}{\partial V_j}, & i \neq j \\ \frac{\partial Q_i}{\partial V_j}, & i = j \end{cases} \tag{4.1}$$

where i and j stand for g (gate), d (drain), and s (source) respectively. The dynamic regime of a three-terminal GFET can be described by just four out of nine intrinsic capacitances [78], [115], C_{ij} in eq. (4.1). In order to illustrate the device capacitive tunability with terminal biases, Fig. 4.2 shows the gate ($V_{GS,e}$) and drain ($V_{DS,e}$) bias dependences of the selected set of capacitances, namely C_{gs}, C_{gd}, C_{sd} and C_{dg}, considering the device technology described in Table 4.1. As can be observed, all intrinsic capacitances show large variations in the selected range of bias, proving that, due to the C_q tunability, using a control signal based on $V_{GS,e}$ and/or $V_{DS,e}$ is a feature that can be eventually exploited for phase shifting operation through the control of the capacitive response of the device.

To the purpose of selecting the RF band of operation, a bare estimation of the RF performance limits of the GFET technology can be obtained by calculating the cut-off frequency, f_T, and maximum oscillation frequency, f_{max} [116], [117]. In particular the expected RF FoMs for the technology described in Table 4.1 are $f_T = 18.9\,GHz$ and $f_{max} = 25.1\,GHz$, at $V_{GS,e} = V_{DS,e} = 1\,V$. As a rule of thumb, the operating frequency

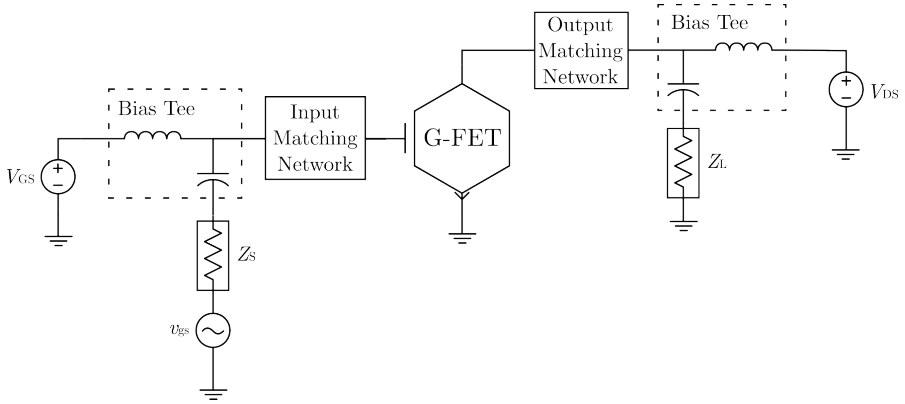


Figure 4.3.: Schematic of the phase shifter. The GFET is used as the active element. IMN and OMN allow to maximize the power transfer from the source to the load and, at the same time, minimize signal reflection from the load. Bias tees at both input and output ports are considered, each one consisting of an ideal capacitor to allow the AC through but uncoupling the DC, and an ideal inductor to allow the DC through but uncoupling the AC signal.

must be lower than 20% of $f_{\max}$ so as to guarantee sufficient power gain [118]. In order to fulfill with this requirement, we have opted for a design at $f = 3\,\text{GHz}$, within the S-band.

4.3.3. Phase shifter circuit design

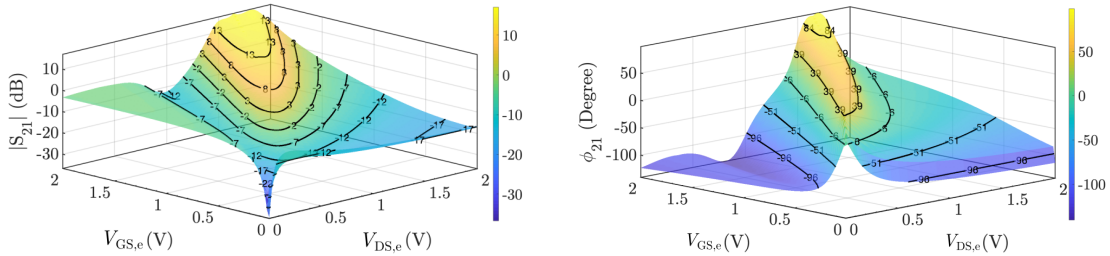
As it is known, an analog phase shifter is expected to produce a phase shift in the output with respect to the input, as dictated by a control signal, while the amplitude of the output is minimally attenuated by a constant factor. In order to implement this concept using graphene, we propose a GFET operating in common-source (CS) configuration, thus forming a two-port network. In particular, building upon the GFET device model, we propose the phase shifter design whose schematic is shown in Fig. 4.3. The RF signal and DC biases are combined by using bias tees consisting of L/C networks which properly block the AC/DC component, respectively. Source and load impedances, Z_S and Z_L respectively, are assumed equal to the characteristic impedance, set to $Z_0 = 50\,\Omega$. In order to achieve a good power transfer, two matching networks are employed, while to the purpose of gaining stability, a shunt resistor of $1.65\,\text{k}\Omega$ is added to the gate of the GFET, assuming this will entail some gain loss. Unconditional stability is achieved for $V_{\text{GS,e}}$ and $V_{\text{DS,e}} = 1\,\text{V}$, which allows us to calculate the reflection coefficients Γ_S and Γ_L for the maximum available gain (MAG). Input and output matching networks (IMN and OMN, respectively) are designed to satisfy $\Gamma_\text{in} = \Gamma_\text{S}^*$ and $\Gamma_\text{out} = \Gamma_\text{L}^*$ so as to yield conjugate matching in both ports, which maximizes power transfer. Both networks are composed by a shunt capacitor ($C_\text{IMN} = 465.26\,\text{fF}$, $C_\text{OMN} = 55.13\,\text{fF}$) and a series inductor ($L_\text{IMN} = 35.07\,\text{nH}$, $L_\text{OMN} = 37.32\,\text{nH}$). The IMN is configured in a C-L topology, while the OMN is configured in a L-C topology.

In a phased controlled antenna array, the phase shifter feeds each element of the array, in a way that the amplitude and phase difference of the input current at each element determine, respectively, the shape and direction of the main lobe of radiation of the array. Thus, for a proper array design, it is of utmost relevance to be able to select the direction of the main lobe (changing the relative phases between the input signals of the antennas), while keeping the shape of the radiation pattern unaltered (maintaining the signal amplitudes of all elements balanced). Therefore, in terms of the scattering (S) parameters, the phase shifter element feeding each antenna must be able to keep the magnitude of S_{21} ($|S_{21}|$) constant while tuning in a controlled way its phase (ϕ_{21}), where ports 1 and 2 of the system refer here to the gate-source and drain-source terminals, respectively. The rest of the S parameters (S_{11}, S_{12} and S_{22}) are also important to guarantee an acceptable power transfer from the input to the output and are addressed by the proper design of IMN and OMN.

In particular, IMN and OMN in Fig. 4.3 are optimized in order to achieve a value of the matching coefficient, M, as high as possible. Generally, matching networks are designed for a single bias point, but in this case both, $V_{\mathrm{GS,e}}$ and $V_{\mathrm{DS,e}}$, will be changed in order to produce the phase shift, so it is crucial to have an M value as high as possible for a wide range of bias. We have assessed M is over 0.7 for almost every bias $V_{\mathrm{GS,e}}$ or $V_{\mathrm{DS,e}}$ condition what will allow us to get an acceptable gain value.

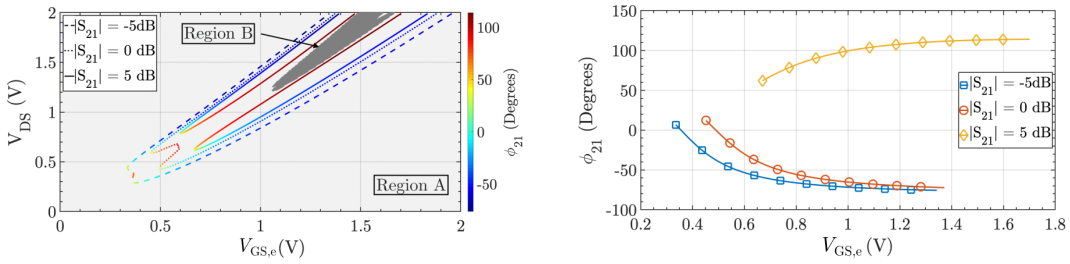
In the design of Fig. 4.3, we expect that by changing $V_{\mathrm{GS,e}}$ or $V_{\mathrm{DS,e}}$ the intrinsic capacitances of the GFET will vary, as shown in Fig. 4.2a, and so will do ϕ_{21}. The interest of the design is to keep at the same time a constant $|S_{21}|$. In order to better understand ϕ_{21} and $|S_{21}|$ dependencies on V_{DS} and V_{GS} we show in Figs. 4.4a) and 4.4b) $|S_{21}|$ and ϕ_{21} as a function of $V_{\mathrm{DS,e}}$ and $V_{\mathrm{GS,e}}$, together with the corresponding isocurves. As can be observed both $|S_{21}|$ and ϕ_{21} show a strong dependence on $V_{\mathrm{DS,e}}$ and $V_{\mathrm{GS,e}}$ what can be exploited for the design of the phase shifter. It should be highlighted that each isocurve of Fig. 4.4a) and b) provides a $V_{\mathrm{GS,e}} - V_{\mathrm{DS,e}}$ combination which ensures a constant $|S_{21}|$ and ϕ_{21}. Moreover, the phase isocurves depict a different dependence on $V_{\mathrm{GS,e}} - V_{\mathrm{DS,e}}$ compared to amplitude isocurves, unveiling the possibility of applying a bias combination (i.e., a simultaneous variation of both $V_{\mathrm{GS,e}}$ and $V_{\mathrm{DS,e}}$) such that, harnessing the quantum capacitance tunability of graphene would yield a constant amplitude while the phase is appropriately modified.

It is also interesting to note here that it would be possible to change the design technique playing with the amplitude of the output signal ($|S_{21}|$) while maintaining a constant phase shift ϕ_{21}, and this result would also be of notable interest as it would allow the radiation pattern to change while keeping the direction of the main lobe constant.



(a) (b)

Figure 4.4.: Isocurve plots of a) $|S_{21}|$ (dB) and b) ϕ_{21} (Degree) versus both $V_{GS,e}$ and $V_{DS,e}$.



(a) (b)

Figure 4.5.: a) Bias dependence of the phase shift ϕ_{21} for three gain values $|S_{21}| = -5$ dB (dashed line), 0 dB (dotted line) and 5 dB (solid line). Bias combinations that do not guarantee unconditional stability for the device are coloured in dark grey, and are represented by region B. b) Gate bias dependence of the phase shift for the same three constant gain values by considering that the drain bias is simultaneously modified to maintain the selected $|S_{21}|$ value (analog control).

Following on with the phase shifter design, Fig. 4.5a shows ϕ_{21} variation (color scale) as a function of the bias combinations that keep a constant value of $|S_{21}|$, for three different cases: -5 dB (dashed line), 0 dB (dotted line) and 5 dB (solid line). Region B in dark grey, represents the bias combinations where the unconditional stability is not guaranteed according to the K-Δ test [119], and therefore should be avoided. In contrast, Region A in light grey, represents the bias combinations where the stability is assured.

Using a purely digital control, i.e. being possible to attain any of the $V_{GS,e} - V_{DS,e}$ combinations that provide a constant specific gain, would yield very large phase shift ranges, e.g. $\Delta\phi_{21} \simeq 180°$ at $|S_{21}| = 0$ dB. If a purely analog control is considered, i.e., a linear relation is forced between $V_{DS,e}$ and $V_{GS,e}$, the $\Delta\phi_{21}$ range is diminished. Nevertheless, in that case, the control would rely only on one signal, e.g., $V_{GS,e}$, and a simpler control circuit would be required (that may be implemented by a DC-DC converter, or in case efficiency is not a constraint, a simple voltage divider). This linear relation between both bias voltages can be estimated for each $|S_{21}|$ isocurve by a standard linear regression, selecting those branches with smaller $V_{DS,e}$ and fitting them with a determination

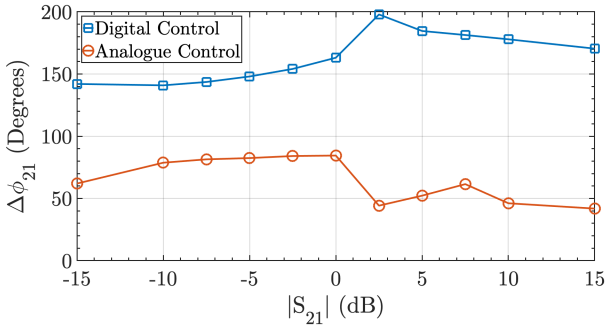


Figure 4.6.: Maximum feasible phase shift with digital (blue squares) and analog (red circles) control versus $|S_{21}|$.

coefficient $R^2 > 0.9999$. By following this procedure, we have been able to evaluate the bias dependence of the phase shift for the three $|S_{21}|$ values considered in Fig. 4.5a, as a function of only $V_{\text{GS,e}}$ (see Fig. 4.5b), demonstrating $\Delta\phi_{21}$ values higher than 50° for the three gain values considered and with a remarkable value of $\Delta\phi_{21}$ higher than $80°$ for $|S_{21}| = 0\,\text{dB}$.

As the maximum phase shift range $\Delta\phi_{21}$ depends on the gain value, we have evaluated it under two scenarios: (i) when digital control is selected, and (ii) when the linear relation between $V_{\text{GS,e}}$ and $V_{\text{DS,e}}$ is assumed. The results are depicted in Fig. 4.6, where $\Delta\phi_{21}$ is plotted for gains ranging from $-15\,\text{dB}$ up to $15\,\text{dB}$, considering either a digital or an analog control. According to Fig. 4.6, $|S_{21}| = 0\,\text{dB}$ happens to be in good trade-off between power gain and phase shift when designing an analog phase shifter. It should be highlighted that it is possible to obtain a higher gain at the expense of losing some phase shift. This trade-off, however, can be balanced with the inclusion of an additional amplifier in the design of the phase shifter.

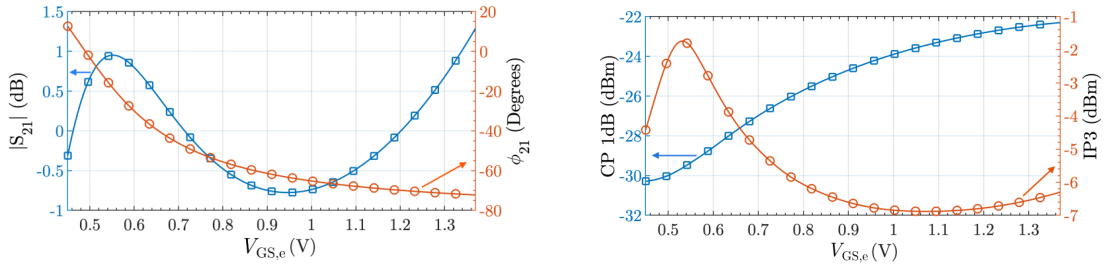
In order to evaluate the variations in $|S_{21}|$ that the purely analog control of the phase shifter induces (due to the small depart from linearity of the actual $V_{\text{GS,e}} - V_{\text{DS,e}}$ combinations), Fig 4.7a) depicts the outcome of the analog-controlled phase shifter for $|S_{21}| = 0\,\text{dB}$. As can been seen when forcing the linear relation for $V_{\text{GS,e}} - V_{\text{DS,e}}$, still a $85°$ phase shift range is achieved, while satisfying a gain of $0\,\text{dB}$ and a maximum variation of $1.3\,\text{dB}$ of $|S_{21}|$.

Figure 4.7b completes the analysis of the analog controlled phase shifter showing the compression point at $1\,\text{dB}$ (CP $1\,\text{dB}$) and the third order interception point (IP3) as main FoMs to assess the linearity of the amplifier. The CP $1\,\text{dB}$ is considerably low (lower than -30 dBm for the worst case), which limits the input power of the phase shifter to $P_{\text{in}} = -30\,\text{dBm}$. When using this device in reception applications, the signal may be free from any distortion as the power of the received signals in most of the wireless transmission protocols are typically lower than that value. However, the current design for the graphene phase shifter would be quite limited for transmission applications, and power stages should be added after it to provide enough power to the transmitted signal. In any case, due to the likely interest of using the proposed phase shifter as both,

Phase shifting method	Control Type	Frequency (GHz)	IL (dB)	RL (dB)	$\Delta\phi$ (Degrees)	Reference
Switched Line	Digital	13-18	2.7	22	349.3	[120]
Reflection type	Analogue	2	1	13.4	385	[121]
Network type	Digital	0.5-1	2.5	13	360	[122]
Loaded Transmission Line	Analogue	1	2	15	183	[123]
GFET CS Amplifier	Digital	3	-2.5	0.9	197.9	This work
GFET CS Amplifier	Analogue	3	0	0.4	84.5	This work
Balanced Amplifier	Analogue	3	0	30.4	85.5	This work

Table 4.2.: Comparison among state-of-the-art phase shifter topologies.

transmitter and receiver, a bidirectional configuration of the device is proposed in the following section.



(a) (b)

Figure 4.7.: a) $|S_{21}|$ (blue squares) and ϕ_{21} (red circles) variation versus gate bias; and b) compression point at 1 dB (blue squares) and third order interception point (red circles) versus the analog control provided by the gate bias.

Finally, we have carried out in Table 4.2 a comparison among different state-of-the-art topologies currently employed to implement phase shifters and the one proposed in this section. In terms of IL, our proposal is the only one which is able to supply some gain to the signal. On the other hand, the main limitations of our design are: (i) () are still limited to poor values, and (ii) the range of phase shift is not the widest, although this is to a certain point balanced by the particular simplicity of the analog control hardware.

With the aim of achieving better performance in terms of return losses, we explore the feasibility of using a balanced configuration with a branch-line coupler. The attention paid to the achievement of flat insertion losses and a wide range of phase shift, may lead to a degradation of the standing wave ratio (SWR) at input and output ports, thus endangering the power generator as the reflected power could be too high. In our particular situation, we are continuously changing the bias of the device, and therefore operating the device in different bias points to those for which the matching networks were originally designed. This is the reason why the analysis of the return losses shown in Table 4.2 gives poor results in the worst case. The use of a balanced configuration solves this issue by using two hybrid couplers at input and output ports, along with two amplifiers [124]. The schematic of the circuit designed to this purpose is depicted in Fig. 4.8. The hybrid coupler is characterized by its scattering parameters, which can be

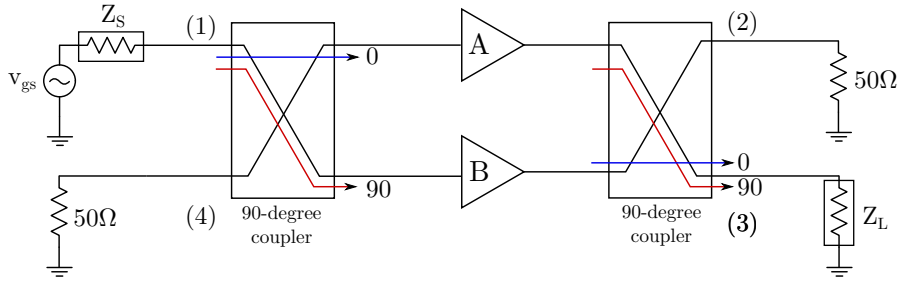


Figure 4.8.: Schematic of the balanced amplifier. Two amplifiers, A and B, are used along with two 90° hybrid couplers. The schematic of the amplifiers is shown in Fig. 4.3.

ideally described as:

$$[S] = \frac{-1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix} \tag{4.2}$$

So that, if all ports of the coupler are matched, the power entering into port 1 is evenly divided between ports 2 and 3, with a 90° phase shift one respect to the other. Port number 4 is isolated, so no power would be coupled to it [119]. With the proper analysis, the global parameters of the network S_{11} and S_{21} can be calculated by following eqs. (4.3) and (4.4), respectively, where a and b subscripts denote the S-parameters of A and B amplifiers respectively. It is of special interest the case where both amplifiers are alike, as in this case $S_{11} = S_{22} = 0$ and $S_{21} = S_{12}$ and equal to the gain of one of the parallel branches of the coupler (with a phase shift of 90°). This means that it is possible to get rid of any reflected power at the input port, with no gain losses, at the cost of a higher complexity of the circuit.

$$S_{11} = \frac{e^{-j\pi}}{2}(S_{11a} - S_{11b}) \tag{4.3}$$

$$S_{21} = \frac{e^{-j\frac{\pi}{2}}}{2}(S_{21a} + S_{21b}) \tag{4.4}$$

Finally, Fig. 4.9 compares S_{11} as a function of the device bias for the single branch configuration (Fig. 4.3) and the alternative balanced configuration (Fig. 4.8). As expected, the results show that, as both branches of the design are identical, the reflection coefficient is strongly diminished, providing a reduction of more than 30 dB in S_{11}. Adopting this new configuration, the return losses are RL= 30.4 dB for the worst case, which makes the balanced amplifier phase shifter topology comparable to the rest of the technologies considered in Table 4.2.

As for the phase shift range shown in Table 4.2, even though our solution yields a range which is one fourth of other state-of-the-art devices, it does not preclude its use

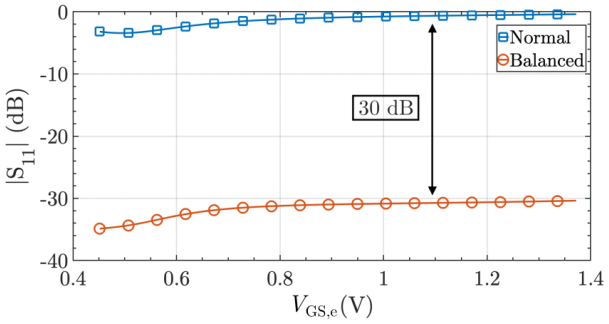


Figure 4.9.: Comparison of the $|S_{11}|$ parameter (blue squares) of the former configuration presented in Fig. 4.3 and the balanced amplifier (red circles) presented in Fig. 4.8.

for numerous applications: many antenna arrays would need no more than 10° shift in their pointing, for which a controllable phase shift of 80° is enough.

A broader phase shift range would be easily achieved by cascading several balanced amplifiers. As the reflection parameter of the balanced amplifier configuration of the phase shifter is extremely low, the cascading would be successfully obtained and, therefore, a multi-stage phase shifter can be readily attained. Eventually, if we cascaded four of these balanced structures, a phase shift range of around 360° would be obtained, making our device fully competitive with other ones in terms of phase shift range.

4.3.4. Bidirectional Operation

This section shows the results of employing the balanced amplifier phase shifter simultaneously as a transmitter and as a receiver. These calculations are of great importance, as they may be required for its application in phased-array techniques in reception and transmission, thus improving the global efficiency of the system not just in one direction but in both. This device is made by vertically mirroring amplifier B so that its input is fed in port 3, and the output is extracted from port 1. The final schematic is shown in Fig. 4.10.

In this device, $S_{22} = S_{11}$ and $S_{12} = S_{21}$. As can be seen in Fig. 4.11a), the shape of the amplitude and phase of the bidirectional amplifier is the same of Fig. 4.7a), but instead of 0 dB now we have a -6 dB gain, which is still acceptable even though it means we are lossing some power. The phase is also shifted but the range of variation remains identical. The reflection parameter $|S_{22}|$ shows values lower than -7 dB for the worst case, in Fig. 4.11b). Although this value is not optimal, it is still acceptable, considering we are trying to use the same device in both directions. In conclusion, we have demonstrated a device able to work as a phase shifter in both directions symmetrically with a -6 dB gain and RL$=7$ dB for the worst case.

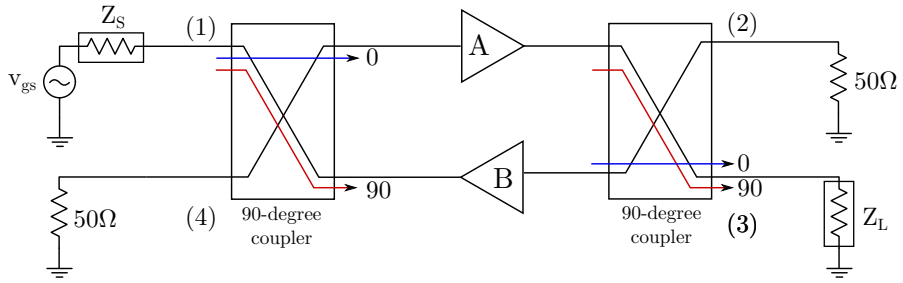
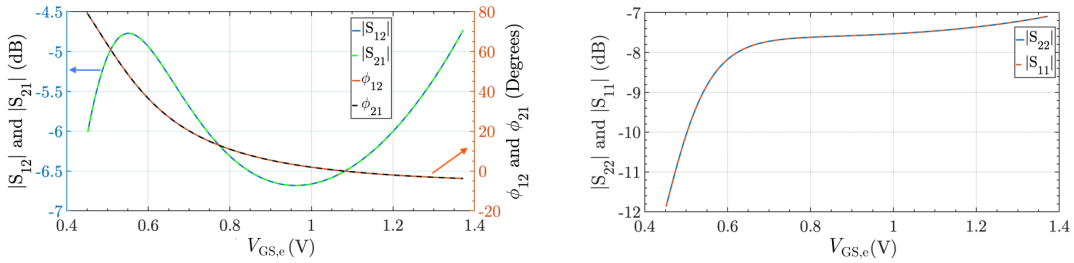


Figure 4.10.: Schematic of the balanced amplifier in a bidirectional operation. In this case, amplifier B is mirrored vertically, so that its input is fed in port 3, and the output is extracted from port 1. The schematic of the amplifiers employed in this design is depicted in Fig. 4.3.



(a) (b)

Figure 4.11.: a) $|S_{12}|$ and ϕ_{12} variation versus $V_{GS,e}$ and b) $|S_{22}|$ variation versus $V_{GS,e}$.

4.3.5. Conclusions

A graphene-based phase shifter operating in the S-band has been designed, able to produce a phase shift on an input RF signal while maintaining a constant gain. Quantum capacitance tunability of graphene is leveraged in order to achieve this phase modulation, combined with an original design procedure. Phase shifts higher than $180°$ are possible, as well as gains above 15 dB. Moreover, a completely analog operation with the gate voltage acting as the control signal has been demonstrated achieving a phase shift up to $84.5°$ without gain loss. These results demonstrate the potential of graphene technology for the future development of improved high frequency applications and in particular for analog phase shifters.

4.4. Amplifier: exploring the impact of the output conductance

The following section is an adaptation of the paper [125] titled: "On the impact of the output conductance on high-frequency amplification in graphene transistors", submitted for journal publication in May 2024 by the following authors: Alberto Medina-Rull,

Pankaj Kumar, Aida Mansouri, Francisco G. Ruiz, Omid Habibpour, Herbert Zirath, Anibal Pacheco-Sanchez, Enrique G. Marin, Wei Wei, Luca Anzi, Amaia Zurutuza, Henri Happy, Roman Sordan, Andrés Godoy, David Jiménez, and Francisco Pasadas. This work is thus a result of a research collaboration including Universidad de Granada, Universitat Autònoma de Barcelona, Politecnico di Milano, IEMN Lille, Graphenea, and Chalmers University of technology, led by the Thesis author.

4.4.1. Introduction

The metrics that rule the performance of common-source amplifier circuits, based on traditional semiconductor field-effect transistors (FETs), are usually linked to the low-frequency (LF) voltage gain, i.e. $A_{\mathrm{v,i}} = g_{\mathrm{m}}/g_{\mathrm{ds}}$; where $g_{\mathrm{m}} = \partial I_{\mathrm{DS}}/\partial V_{\mathrm{GS}}$ and $g_{\mathrm{ds}} = \partial I_{\mathrm{DS}}/\partial V_{\mathrm{DS}}$ stand for the transconductance and output conductance, respectively; and I_{DS}, V_{DS} and V_{GS} are the the drain-source current and voltage, and gate-source voltage [56]. In particular, in conventional Si FETs at LF the voltage amplification exploits the current saturation regime where the I_{DS} depends solely on V_{GS}, i.e., when a pinch-off is formed at the channel edge next to the drain. In this scenario, I_{DS} becomes practically independent of the applied V_{DS}, meaning that $g_{\mathrm{ds}} \sim 0$, resulting in high $A_{\mathrm{v,i}}$. At sufficiently small gate input levels, a linear amplification is then obtained at the drain. This amplification can be measured in terms of current gain, voltage gain, or power gain (the latter being the product of the former two). Although voltage gain turns out to be the design criteria in many LF cases, as in audio applications [56], the primary objective of an amplifier is to provide power gain.

This common design dissociation between power and voltage gains is especially critical when increasing the operation frequency. LF analog circuit implementations focus on $A_{\mathrm{v,i}}$ because at these frequencies, power gain is typically abundant and impedance-transforming networks (in the form of transformers) are unnecessary.

In the RF domain, in contrast, the limited power gain requires careful consideration (with the design oriented to its optimization) and from there the notable importance of impedance matching networks [126]. Although the distinction is evident and well-known, the demand of high $A_{\mathrm{v,i}}$ in LF has somehow permeated the design criteria in RF leading to the wrong statement that a g_{ds} close to zero is crucial also at high-frequencies (HFs).

This mindset is at the origin of the widespread assessment that graphene FETs (GFETs) cannot work as proper electronic HF amplifiers. As explained in Chapter 2, GFETs do not exhibit a pronounced saturation region, but a small kink between the shift of carrier type within the channel. Thus GFET technology has, sustained by this reasoning, been disregarded in the literature for RF amplifying applications [33], [127], [128]. However, no detailed analysis has been provided to show the actual RF power amplification limits of GFETs, considering that at HF it is the power gain (and not the voltage gain) the metric that actually rules the performance of an amplifier [126]. This is in part motivated by the poor results obtained by present implementations of GFETs in terms of the intrinsic f_{max} as compared to the outstanding values of intrinsic f_{T}, as exposed in Chapter 2.

These results, however, cannot be detached from the infancy stage of graphene technology and its integration into millimeter-wave integrated circuit design [129]. The quality of the graphene synthesis determines the GFET channel mobility, and can become a noticeable bottleneck. As an improved technological control is expected to be achieved so to push graphene technology towards higher technology readiness levels (TRLs) in the forthcoming years, it becomes more and more important to better understand if GFETs would eventually offer competitive RF FoMs for signal amplification from a critical predictive analysis.

The aim of this section is two-fold. Firstly, it seeks to dissociate the observed weak current saturation in the output characteristics of GFETs from their potential performance in terms of RF power gain. Secondly, it demonstrates the design of GFET-based amplifiers with different values of g_{ds} exhibiting a reasonably large RF power gain, even when $A_{\mathrm{v,i}} < 1$, provided the proper impedance matching is employed.

The rest of the section is organized as follows. Subsection 4.4.2 presents the theoretical microwave analysis under small-signal operation, specifically evaluating the impact of the output conductance on the power gain of a common-source amplifier. In subsection 4.4.3, the fabricated GFETs are characterized and modeled by a circuit-compatible computer-aided design (CAD) tool and a modeling set of parameters, which are used for circuit design in ADS. Subsection 4.4.4 is devoted to the demonstration of the feasibility of designing GFET-based high-frequency power amplifiers with $A_{\mathrm{v,i}} < 1$, by properly addressing the impedance matching networks. Finally, the conclusions are given in subsection 4.4.6.

4.4.2. Small-signal analysis of a GFET-based power gain amplifier

The maximum gain, $G_{\max}$, and the microwave stability of the GFET can be analyzed from $\mathbf{Y}$, the admittance matrix of the GFET small-signal model shown in 2.7. $G_{\max}$ is determined by the maximum available gain (G_{MA}), when the device is unconditionally stable (US), or the maximum stable gain (G_{MS}), when the device is potentially unstable (PU) [130]:

$$G_{\max} = \begin{cases} G_{\mathrm{MA}} = \left|\frac{Y_{21}}{Y_{12}}\right| \left(K - \sqrt{K^2 - 1}\right) & \text{US} \\ G_{\mathrm{MS}} = \left|\frac{Y_{21}}{Y_{12}}\right| & \text{PU} \end{cases} \tag{4.5}$$

where K is the Rollet constant, defined as:

$$K = \frac{2\,\mathrm{Re}(Y_{11})\,\mathrm{Re}(Y_{22}) - \mathrm{Re}(Y_{21}Y_{12})}{|Y_{21}Y_{12}|}. \tag{4.6}$$

The explicit expression of G_{MS} reads as:

$$G_{\mathrm{MS}} = \frac{1}{\omega}\sqrt{\frac{\omega^2\left[C_{\mathrm{dg}} + R_{\mathrm{s}}A\right]^2 + \left[g_{\mathrm{m}} + R_{\mathrm{s}}\omega^2 B\right]^2}{\left[C_{\mathrm{gd}} + R_{\mathrm{s}}A\right]^2 + R_{\mathrm{s}}^2\omega^2 B^2}} \tag{4.7}$$

where the terms A and B are given by:

$$A = C_{\mathrm{gd}} g_{\mathrm{ds}} + C_{\mathrm{gs}} g_{\mathrm{ds}} + C_{\mathrm{gd}} g_{\mathrm{m}} \tag{4.8}$$

$$B = C_{\mathrm{gd}}^2 - C_{\mathrm{dg}} C_{\mathrm{gd}} + C_{\mathrm{gd}} C_{\mathrm{gs}} + C_{\mathrm{gd}} C_{\mathrm{sd}} + C_{\mathrm{gs}} C_{\mathrm{sd}} \tag{4.9}$$

The first observation from (4.7) is that, given an operating DC bias point, out of all resistive elements, only the contact resistance at the common terminal (R_{s} in the common-source configuration) impacts G_{MS}. However, both R_{d} and R_{s} influence the intrinsic small-signal elements: R_{d} and/or R_{s} determine the internal biases, resulting in different values of the intrinsic g_{m}, g_{ds}, and capacitances [131]. The aim of this section is to evaluate the impact of the output conductance g_{ds} on the power gain to elucidate whether achieving current saturation in GFETs, e.g. by bandgap engineering [132], is mandatory to get high power gain at high frequencies. If a negligible contact resistance at the common terminal is assumed, i.e. $R_{\mathrm{s}} \to 0\,\Omega$, we obtain:

$$G_{\mathrm{MS}}\Big|_{R_{\mathrm{s}} \to 0\,\Omega} = \frac{\sqrt{C_{\mathrm{dg}}^2 \omega^2 + g_{\mathrm{m}}^2}}{\omega C_{\mathrm{gd}}} \tag{4.10}$$

which does not show a direct dependence on g_{ds}. This means that, in an ideal scenario, where a more mature graphene technology is reached, i.e. where R_{s} and R_{d} are considerably reduced, the lack of current saturation would not significantly affect the maximum attainable stable gain. This trend has already been observed in GFETs fabricated in Si-standard environments for mass production [133]. High TRL fabricated GFETs showing contact resistances $< 5\,\Omega$ have been recently demonstrated [134], [135], bringing to light that the mentioned ideal scenario is not far from more mature forthcoming graphene technologies.

As for G_{MA}, its value does not show a direct dependence on g_{ds} only if both, the gate and the contact resistances are negligible. In this case, G_{MA} reads as:

$$G_{\mathrm{MA}}\Big|_{R_{\mathrm{s}}, R_{\mathrm{d}}, R_{\mathrm{g}} \to 0} = \frac{|Y_{21}|}{|Y_{12}|}(K - \sqrt{K^2 - 1}) = \\ = \sqrt{C_{\mathrm{dg}}^2 \omega^2 + g_{\mathrm{m}}^2} \left(\frac{C_{\mathrm{dg}}}{C_{\mathrm{gd}}^2 \omega} - j \frac{g_{\mathrm{m}}}{C_{\mathrm{gd}}^2 \omega^2} \right) \tag{4.11}$$

As commented on the phase shifter design, for an amplifier to guarantee sufficient practical power amplification in realistic applications, the operating frequency should follow the rule of thumb of employing up to a 20% of f_{max}. Under this condition, the vast majority of the active GFETs are potentially unstable [136], [137], and consequently G_{MS} should be the metric that rules the design in the search of maximum amplification. Together with the evaluation of the maximum gain, U will be evaluated as well, as it provides important information about the performance of the device. Finally, the amplifier stability will be evaluated in this section through the magnitudes μ and μ' [138], which represent the Euclidean distance between the center of the Smith chart and the closest point of the input and output stability curves, respectively.

Although the small-signal equivalent circuit of the GFET in Fig. 2.7 is extremely useful to guide a simplified (but insightful) theoretical analysis, the electrical response of the GFET operating at RF and, consequently, the discussion and design of RF amplifiers requires of the description of the dynamic large-signal operation of the transistor, which will be provided by the compact simulation model of the GFET in ADS. The large-signal model predictions will be complemented by experimental realizations of GFETs to assess the key ideas introduced here about the limited impact of g_{ds} on G_{MS} under a high graphene TRL scenario; and, therefore, to elucidate whether seeking current saturation in GFETs is actually mandatory to get high power gain at high frequencies or should be disregarded.

4.4.3. GFET technology: fabrication, characterization and modeling

Experimental methods: Fabrication of GFETs

The GFETs were fabricated from graphene grown by CVD. The graphene channel and all contacts were defined by electron-beam (e-beam) lithography using polymethyl methacrylate resists. The graphene channel was etched using O_2 plasma. The metal contacts were deposited by e-beam evaporation at a base pressure of $\sim 10^{-6}$ mbar. The gate was fabricated in the first step and consisted of 200-nm-thick Al. After the devices were exposed to ambient air, the Al gate oxidized on all its surfaces, including the interface with the graphene channel. This formed a native ∼4-nm-thick AlO_x gate insulator resulting in an oxide capacitance per unit area of $\sim 1.4\mu F/cm^2$ [139]. The source and drain contacts were made of 80-nm-thick pure Au to reduce the contact resistance. The GFETs had a gate length $L_g = 1\mu m$ and channel width $W_g = 10\mu m$. To reduce losses at high frequencies, the GFETs were fabricated on a highly resistive Si substrate with 1-µm-thick SiO_2 on top.

Experimental methods: DC and high-frequency characterization of GFETs

The electrical characterizations were performed in air ambient. The DC characterizations were performed using a two-channel Keithley source measure unit 2636B and a FormFactor Summit 11000 probe station. The high-frequency characterizations were performed by measuring the S-parameters using a vector network analyzer (VNA) of a bandwidth of 66 GHz and two Keithley source measure units 2600.

Calibration of the GFET model

Next, we fitted our compact GFET large-signal model to the experimental measurements as described in Section 4.2. Table 4.3 summarizes the parameters as a result of the adjustment process.

Parameter	Value	Parameter	Value
L_g	$1.04\,\mu\mathrm{m}$	μ	$0.77\,\mathrm{m^2/Vs}$
W_g	$10\,\mu\mathrm{m}$	V_go	$-0.05\,\mathrm{V}$
C_ox	$14\,\mathrm{fF}\mu\mathrm{m}^{-2}$	$R_\mathrm{d,s}W_\mathrm{g}$	$736\,\mathrm{k}\Omega\mu\mathrm{m}$
n_res	$3.55\times10^{11}\mathrm{cm}^{-2}$	$R_\mathrm{g}L_\mathrm{g}$	$0.1\,\Omega\mu\mathrm{m}$

Table 4.3.: GFET technology for the power gain amplifiers design.

Although graphene is expected to exhibit a symmetrical electron-hole conduction because of its band structure [140], experiments have shown [141] that it is highly susceptible to symmetry-breaking perturbations [142] like: i) scattering mechanisms [118], [143], [144], such as phonon scattering, impurity scattering, or edge scattering, which affect electrons and holes disparately, resulting in differences in their mobility and conductivity [136], [137]; ii) substrate properties impacting material quality and leading to distinct electrical characteristics for electron and hole conduction [145], [146]; iii) uncontrolled doping selectively enhancing the concentration of either electrons or holes and influencing also both conductivity and mobility, where the latter depends on carrier concentration; and iv) the metal-graphene contact and access resistances introducing asymmetry in the transfer characteristics of GFETs [147], [148].

Here, for the sake of undertaking a theoretical performance projection of GFET-based amplifers in mature forthcoming graphene TRLs, we assume the same conduction characteristics for both carrier types and a uniform contact technology ($R_\mathrm{s} = R_\mathrm{d}$). Both considerations are pivotal for maximizing the potential of GFETs in high-frequency applications, particularly in RF analog electronics, exploiting ambipolarity, e.g., in frequency multipliers [149]–[152], subharmonic mixers [153]–[157], and modulators [158], [159], among others [160].

The CAD tool was calibrated in both *n*- and *p*-type conduction branches in Fig. 4.12, comprising operating biases $V_\mathrm{GS,e} > V_\mathrm{Dirac}$ and $V_\mathrm{GS,e} < V_\mathrm{Dirac}$, respectively, where V_Dirac is the Dirac voltage of a biased GFET. The modulation of the charge neutrality point, i.e., the Dirac voltage, depends on the operating bias point and a careful consideration must be undertaken for the design of RF circuits. For a single-gated GFET in common-source configuration, $V_\mathrm{Dirac} = V_\mathrm{go} + (V_\mathrm{DS,e}/2)$. In Fig. 4.12, the well-known kink (or quasi saturation) is observed in the current, which is manifested as a *plateau* in the output characteristic curve at which g_ds reaches its minimum value. The kink is obtained at $V_\mathrm{DS,e} = V_\mathrm{kink}$ when the pinch-off is located at the drain edge of the channel [161]. The kink specifically occurs for $V_\mathrm{GS,e} > V_\mathrm{go}$ at $V_\mathrm{DS,e} > 0\,\mathrm{V}$, and $V_\mathrm{GS,e} < V_\mathrm{go}$ at $V_\mathrm{DS,e} < 0\,\mathrm{V}$, due to $V_\mathrm{go} < 0\,\mathrm{V}$ in our devices. V_kink determines the border between the *n*- and *p*-type conduction branches, also known as the first (for $|V_\mathrm{DS,e}| < |V_\mathrm{kink}|$) and second (for $|V_\mathrm{DS,e}| > |V_\mathrm{kink}|$) linear regimes.

The model calibration also addresses the RF performance. The predicted (solid lines) and measured (symbols) hybrid transmission parameter, h_{21}, and the Mason's invariant, U, are compared in Fig. 4.13. A two-step de-embedding procedure was carried out to reduce the GFET to the equivalent circuit shown in Fig. **??**. The procedure consisted

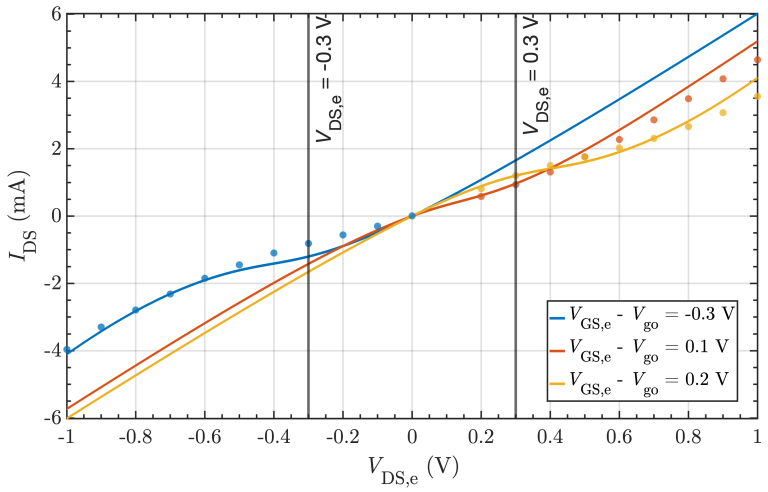


Figure 4.12.: Simulated (solid lines) and measured (symbols) output characteristic curves for different overdrive gate voltages.

of subtracting the contribution of the pad and interconnection parasitics based on measurements of the on-wafer open and short dummy structures [162]. At $V_{\mathrm{DS,e}} = 0.3\,\mathrm{V}$, the cut-off and maximum oscillation frequencies of our GFETs are 6.55 GHz and 8.43 GHz, respectively, as can be observed in Fig. 4.13.

In both DC and RF regimes, the modeled and measured data show an adequate agreement. The calibrated CAD tool is employed for the design of RF amplifiers operating at 2.4 GHz based on the investigated GFETs. Symmetrical conduction and uniform constant resistances are assumed in the performance projection.

4.4.4. Power amplification based on GFETs in common-source configuration

Unveiling the impact of the operating bias point on the amplifier performance

This study seeks to demonstrate that current saturation (i.e., low g_{ds}) is not mandatory, as widely assumed in the literature, to fully exploit GFETs for RF amplification. To prove this hypothesis, we address the design of RF amplifiers, based on our graphene technology. The GFETs are described by the compact model with the parameters listed in Table 4.3, operating in a non-saturated region, resulting in $A_{\mathrm{v,i}} < 1$.

For the sake of clarity, the output conductance g_{ds} (cf. Fig. **??**) differs from the extrinsic output conductance, $g_{\mathrm{ds,e}} = \partial I_{\mathrm{DS}}/\partial V_{\mathrm{D,e}}$, which could be straightforwardly extracted from the measurements [131]. The density plots in Fig. 4.14 show the dependence of both g_{ds} and the maximum gain G_{max} (at $f = 2.4\,\mathrm{GHz}$) at the extrinsic overdrive gate voltage, $V_{\mathrm{GS,e}} - V_{\mathrm{go}}$, and drain bias, $V_{\mathrm{DS,e}}$. In Figs. 4.14a and b, four regions, where $G_{\mathrm{max}} > 0\,\mathrm{dB}$, are delimited with dashed lines and labelled from I to IV. The red solid line marks the path of minimum g_{ds}, highlighting the operating bias points that produce the

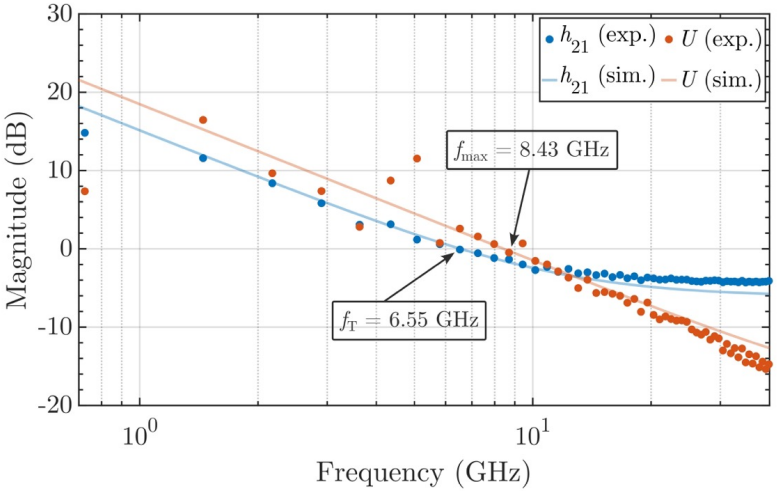
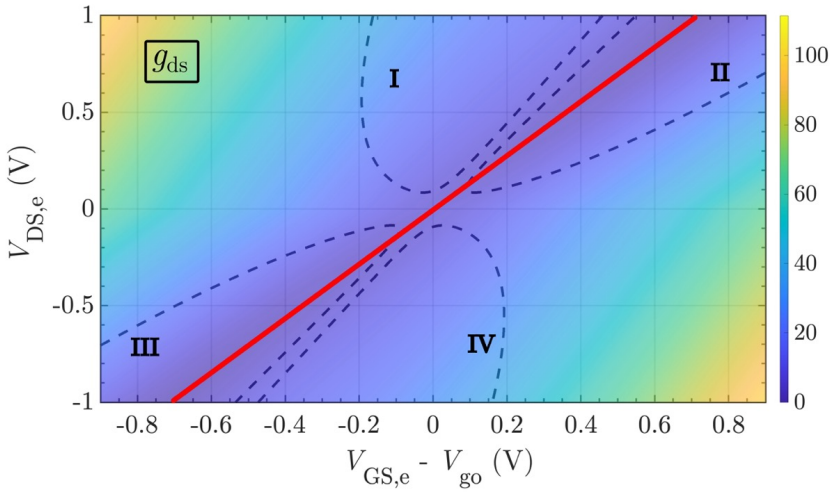


Figure 4.13.: h_{21} and U as a function of frequency for $V_{GS,e} - V_{Dirac} = 0.1\,V$ and $V_{DS,e} = 0.3\,V$. The solid lines correspond to simulated curves, while symbols represent the measurements of the fabricated GFET.

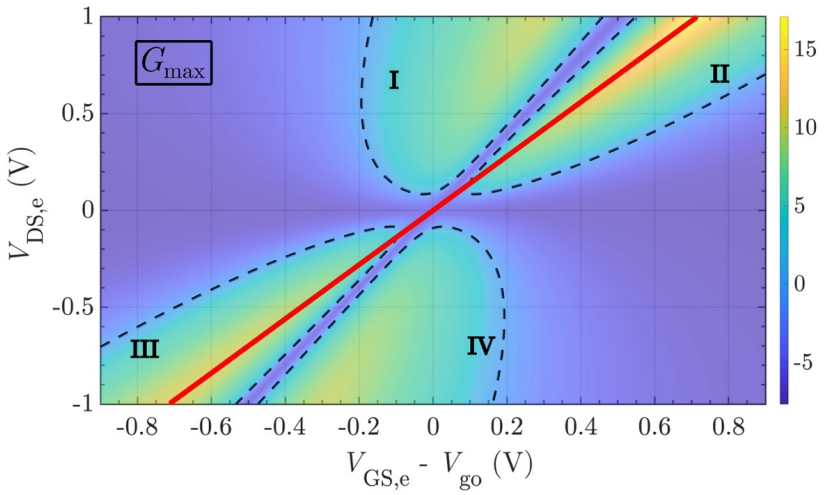
kink in the output characteristics. According to the voltage gain argument, only regions marked with numbers II and III should be the used in the amplifier design because g_{ds} reaches the lowest value in these regions. They show slightly higher attainable G_{max} (at $f = 2.4\,GHz$) than regions I and IV. However, for symmetrical conduction and uniform contact technology, the difference in the maximum attainable G_{max} in the four regions is not significant. In the ideal case, where the extrinsic resistances were absent, the difference is theoretically negligible, as addressed in Eqs. (4.10) and (4.11). The regions I and IV can also provide sufficient power gain when the operating point is placed in the zone where g_{ds} is higher, i.e. when the GFET operates in the linear regime, far from the quasi-saturation region reached at the kink highlighted by the red line in Fig. 4.14. Four different amplifiers, one in each of the four regions, is in the following designed here. They achieved a similar and reasonable power gain, regardless of their corresponding g_{ds}.

Fig. 4.15 shows some of the critical design metrics as a function of $V_{GS,e} - V_{Dirac}$ for two extrinsic drain biases: a) $V_{DS,e} = 0.3\,V$ and b) $V_{DS,e} = -0.3\,V$. In particular, the evaluated metrics (from top to bottom) are the intrinsic output conductance, g_{ds}; the absolute value of the intrinsic transconductance, $|g_m|$; the maximum gain, G_{max}, at $f = 2.4\,GHz$; and the stability parameters, μ and μ'. Red and black dots mark the G_{max} values that are calculated from the experimental S-parameter measurements at the corresponding $V_{GS,e}$ and $V_{DS,e}$ bias points. The grey shaded regions represent the bias regions in which the gain is $< 0\,dB$, delimited by the horizontal dash-dotted line corresponding to $G_{max} = 0\,dB$. The green shaded regions mark the operating bias points where the device is unconditionally stable, i.e., the regions in which $\mu > 1$ and $\mu' > 1$. The shaded yellow regions represent the biases where the device is potentially unstable.

In the shaded yellow regions, two gain maxima are found in G_{max}, for $V_{GS,e} > V_{Dirac}$



(a)



(b)

Figure 4.14.: Density plot of a) g_{ds} and b) G_{max} versus $V_{GS,e} - V_{go}$ and $V_{DS,e}$, at $f = 2.4$ GHz. The red solid line goes over the minimum values of g_{ds}. Four regions where $G_{max} > 0$ dB are highlighted and enclosed by dashed-lines: regions II and III include the minimum g_{ds} value line, while higher values of g_{ds} are achieved at regions I and IV given that the GFET would be operating at the linear regime.

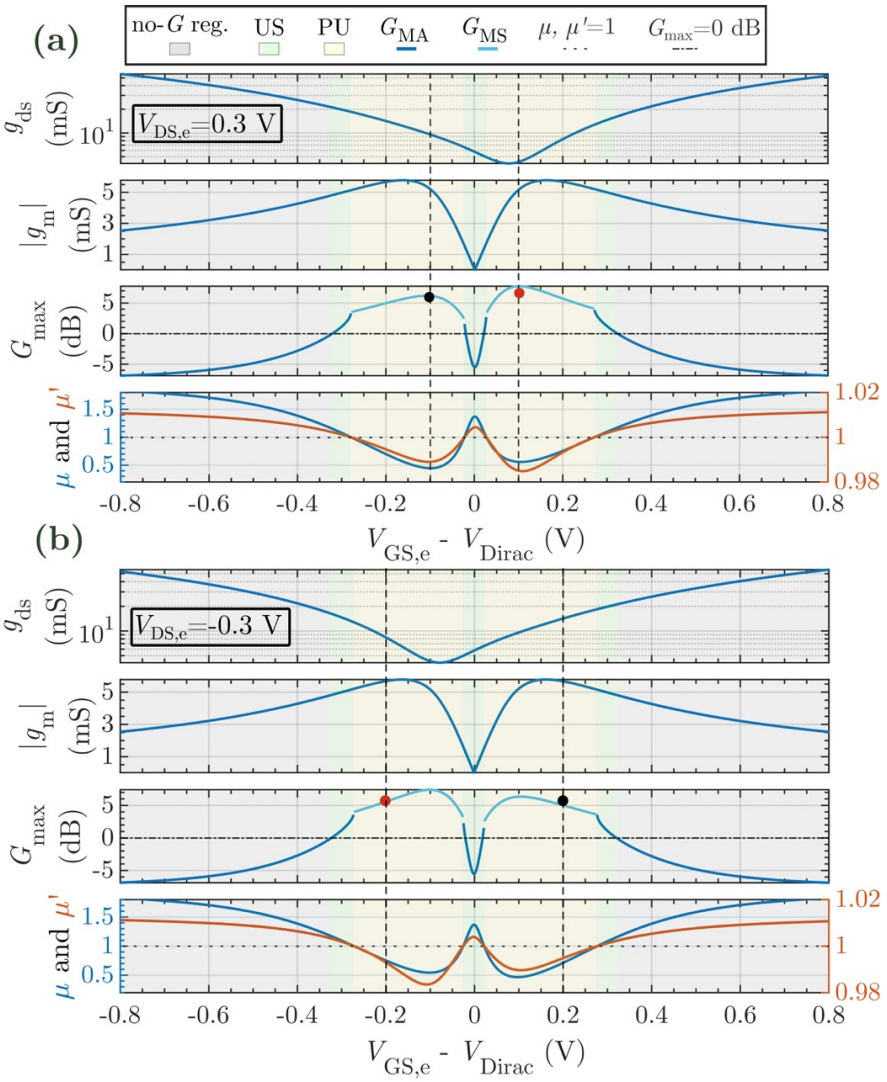


Figure 4.15.: From top to bottom: output conductance, g_{ds}; transconductance, $|g_{\mathrm{m}}|$; maximum gain G_{max}; and stability parameters, μ and μ'; as a function of $V_{\mathrm{GS,e}} - V_{\mathrm{Dirac}}$, for a fixed drain-to-source voltage of a) $V_{\mathrm{DS,e}} = 0.3\,\mathrm{V}$ and b) $V_{\mathrm{DS,e}} = -0.3\,\mathrm{V}$. Black and red symbols correspond to measurements. Legend: no-G reg.: no gain region; US: unconditionally stable; PU: potentially unstable.

and $V_{\mathrm{GS,e}} < V_{\mathrm{Dirac}}$ (close to experimentally extracted red and black symbols). On the one hand, the highest G_{max} values, near the red symbols, correspond to operating bias points close to the kink in the output curve (quasi-saturation regime), i.e., g_{ds} is in the vicinity of its minimum value, as can be confirmed in the upper panels of Figs. 4.15a-b. On the other hand, the G_{max} maxima close to the black symbols, constitute singular results arisen from the particular graphene ambipolarity, and have been previously evidenced in the literature (subsection 4.4.5). However, their origin from a GFET operating under a linear regime, far from current (quasi) saturation, have not been rationalized and discussed yet. In fact, while the $|g_{\mathrm{m}}|$ curve is symmetric around $V_{\mathrm{GS,e}} = V_{\mathrm{Dirac}}$, as our model considers same carrier mobilities, such symmetry is not observed in the g_{ds} plot. This confirms the weak correlation between G_{max} and g_{ds}, and shows that the current saturation is indeed not mandatory for power amplification based on GFETs as hypothesized.

This lack of strong correlation, explained here for the first time, can be found (although not previously identified) in the literature. A couple of examples are explicitly commented on subsection 4.4.5. This result can be leveraged in multiple scenarios: building phase-shift keying (PSK) modulators based on a symmetrical power amplification with a single device, given that the operating point at $V_{\mathrm{GS,e}} < V_{\mathrm{Dirac}}$ for $V_{\mathrm{DS,e}} > 0\,\mathrm{V}$, and $V_{\mathrm{GS,e}} > V_{\mathrm{Dirac}}$ for $V_{\mathrm{DS,e}} < 0\,\mathrm{V}$, entails a change of 180° in the output amplified signal; a better design of power amplifiers based on GFET focusing on the $|g_{\mathrm{m}}|$ maximum; avoiding instability of power amplifiers based on GFETs due to negative differential resistance [163]–[165], especially when operating at high drain biases (by optimizing the operating bias point in a linear region of the output characteristics).

Designs of RF GFET-based amplifiers

Next, four GFET-based amplifier designs are addressed for the four different operating bias points identified for G_{max} in Fig. 4.15 (i.e. red and black symbols). The amplifier topology for all the designs is shown in Fig. 4.16, which considers a typical common-source configuration with input and output matching networks and input and output bias tees. The goal is to reach a power gain as close as possible to the maximum stable gain, G_{MS}, given that the device is potentially unstable at the selected bias points. The resulting transducer gain ($G_{\mathrm{T}} = |S_{21}|$) for the four designs is shown in Fig. 4.27. The stability of the amplifiers is guaranteed by observing the transient response of the amplifiers to an input voltage pulse in the time domain [166] using standard 50-Ω ports [167]–[169]. Table 4.4 shows the key parameters of the four amplifier designs: operating bias point, voltage gain, power gain and stability. It can be concluded that similar power gains and comparable microwave stability are feasible with the same $|g_m|$, but very different g_{ds}. Note the lack of straightforward correlation between the low-frequency voltage gain, $A_{\mathrm{v,i}}$, and maximum achievable power gain G_{max}. For example, an RF amplifier with $G_{\mathrm{max}} > 5\,\mathrm{dB}$ is predicted for $A_{\mathrm{v,i}} = 0.4 < 1$, which would result in a low-frequency voltage attenuator.

It is worth to highlight the relevance of the strong dissociation demonstrated in Fig. 4.27 and Table 4.4 between output conductance and power gain. There is a wide interest

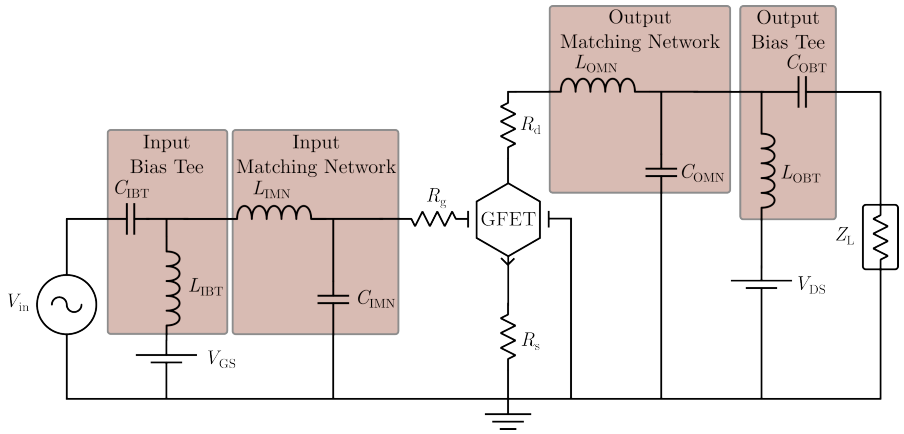


Figure 4.16.: Schematic of the design of a GFET-based common-source amplifier.

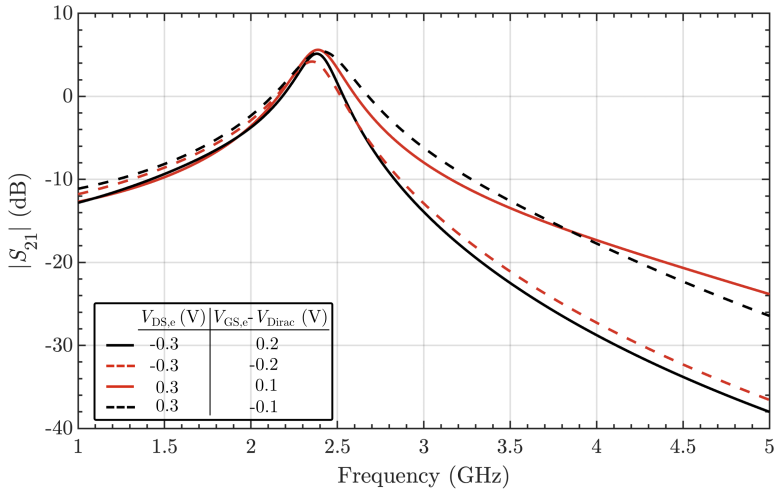


Figure 4.17.: Transducer gain ($|S_{21}|$) vs. frequency for the four amplifier designs. The legend indicates the operating bias points, corresponding to the red and black symbols in Fig. 4.15.

Parameter	Design 1	Design 2	Design 3	Design 4
$V_{DS,e}$ (V)	-0.30	-0.30	0.30	0.30
$V_{GS,e}$ - V_{Dirac} (V)	-0.20	0.20	-0.10	0.10
g_{ds} (mS)	8.39	14.19	9.59	4.29
$\|g_m\|$ (mS)	5.67	5.67	5.22	5.16
$A_{v,i} = \|g_m\|/g_{ds}$	0.68	0.40	0.54	1.20
μ/μ'	0.75/0.99	0.72/0.99	0.45/0.99	0.56/0.99
G_T (dB)	5.58	5.04	4.19	5.42

Table 4.4.: Operating biases and figures of merit of the GFET-based amplifier designs.

in the opening of a bandgap in graphene to improve current saturation, i.e., to reduce the g_{ds}, even at the cost of degrading the carrier mobility, and consequently reducing $|g_{\mathrm{m}}|$. The strategies for this bandgap engineering in graphene [132] range from the application of a perpendicular electric field in the case of bilayer graphene [170]–[174], strain engineering [175], the confinement in graphene nanoribbons [176], [177], to molecular intercalation and/or chemical doping [174], [178]–[180], among others. The results presented here aim to draw the attention at the actual possibility to reach RF amplification with GFET devices despite the absence of bandgap and current saturation, enabling second thoughts and reinterpretation on these seminal works.

4.4.5. Evidences in the literature

There are several evidences in the literature pointing out the possibility of designing a microwave amplifier based on a GFET in a bias region far from current saturation. One of these examples is observed in Ref. [46], where the state-of-the-art f_{max} of a GFET is reported. In Fig. 4.18, the typical room-temperature DC and RF electrical characteristics of a GFET with channel width of $20\,\mu$m are shown. According to Ref. [46], $V_{\mathrm{GS,e}} = 0.6\,\mathrm{V}$ and $V_{\mathrm{DS,e}} = 0.35\,\mathrm{V}$ was the operating bias point used when measured the record high f_{max}. Looking at this bias point in Fig. 4.18(a) and (b), where vertical red lines have been drawn to highlight the bias conditions, we realise that:

1. In Fig. 4.18(a), for $V_{\mathrm{GS,e}}$ ranging from -1 V to 1V, we observe that none of the curves show saturation at $V_{\mathrm{DS,e}} = 0.35\,\mathrm{V}$. The GFET is operating in the linear region for $V_{\mathrm{GS,e}} = 0.6\,\mathrm{V}$ and $V_{\mathrm{DS,e}} = 0.35\,\mathrm{V}$. Saturation is observed for higher drain biases, around $V_{\mathrm{DS,e}} = 0.8\,\mathrm{V}$.

2. In Fig. 4.18(b), the closest $V_{\mathrm{DS,e}}$ value to the bias used for the record f_{max} is $0.3\,\mathrm{V}$, which is the upper black curve. At $V_{\mathrm{GS,e}} = 0.6\,\mathrm{V}$, we observe that $V_{\mathrm{GS,e}} < V_{\mathrm{Dirac}}$, and as $V_{\mathrm{DS,e}} > 0\mathrm{V}$, we can conclude, by means of the analysis made in Fig. 4.14, that the operating bias point is within the Region I, meaning that the record f_{max} in GFET technology has been measured at an operating bias point far from current saturation.

Additionally, in [181] a small-signal model of GFETs extended to the ambipolarity regime is proposed. The validation of the equivalent circuit was assessed against measurements from an ambipolar GFET. In particular, Fig. 4.19 shows the intrinsic and extrinsic (black and red, respectively) current and unilateral power (purple) gains measured (symbols) at an operating frequency of 1 GHz and $V_{\mathrm{DS,e}} = 0.5\,\mathrm{V}$. A clearly M-shaped trend, with a minimum at $V_{\mathrm{GS,e}} = V_{\mathrm{Dirac}}$, can be observed in the measured performance of a symmetrical GFET, confirming the availability of power gain when the transistor is operating in a linear regime far from the quasi-saturation regime ($V_{\mathrm{GS,e}} < V_{\mathrm{Dirac}}$ at $V_{\mathrm{DS,e}} > 0\mathrm{V}$). In this particular case, the GFET even presented better RF perfomance when operating in the linear regime, bringing to light to consider $|g_{\mathrm{m}}|$ as the magnitude relevant for power amplification purposes.

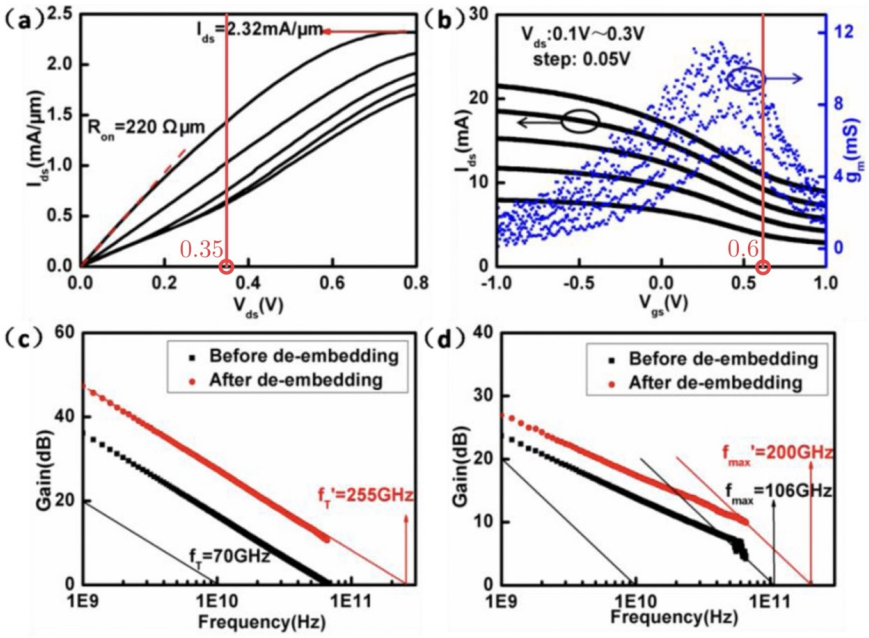


Figure 4.18.: (a) $I_{\mathrm{DS}} - V_{\mathrm{DS,e}}$ output characteristics at various gate voltages ($V_{\mathrm{GS,e}} = -1, -0.5, 0, 0.5$, and $1\,\mathrm{V}$); (b) transfer characteristic at different bias voltage ($V_{\mathrm{DS,e}} = 0.1, 0.15, 0.2, 0.25$, and $0.3\,\mathrm{V}$); (c) h_{21} before (black dot) and after (red dot) de-embedding; (d) U before (black dot) and after (red dot) de-embedding. Reproduced with permission from [46], Copyright 2016, American Chemical Society.

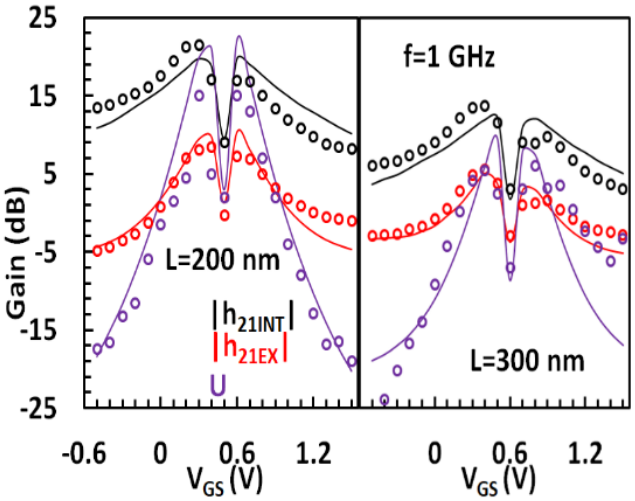


Figure 4.19.: Intrinsic, extrinsic small-signal current gain and unilateral power gain $|h_{21\mathrm{INT}}|$, $|h_{21\mathrm{EX}}|$, U, respectively for two GFETs with $W_{\mathrm{g}} = 24\,\mu\mathrm{m}$ and $L_{\mathrm{g}} = 200\,\mathrm{nm}$ (left subplot), $L_{\mathrm{g}} = 300\,\mathrm{nm}$ (right subplot) versus $V_{\mathrm{GS,e}}$ for $1\,\mathrm{GHz}$ at $V_{\mathrm{DS,e}} = 0.5\,\mathrm{V}$. Symbols: measurements, lines: model. Reproduced with permission from [181], Copyright 2023, IEEE.

4.4.6. Conclusions

We theoretically assessed that current saturation is not mandatory, as widely assumed in the literature, to fully exploit GFETs for RF amplification. The analytic expressions of the figures of merit related to the power gain and microwave stability of a graphene RF amplifier in a common-source configuration were derived, observing that, as long as the contact resistance at the common terminal is negligible, there is no direct relation between the achievable power gain, $G_{\max}$, and the output conductance, g_{ds}. The connection between g_{ds} and $G_{\max}$ in practical cases, was further analyzed by presenting different designs of power gain amplifiers with $G_{\max} > 5\,\mathrm{dB}$ at $2.4\,\mathrm{GHz}$ exhibiting $A_{\mathrm{v,i}}$ higher and lower than unity, demystifying the need for current saturation for the realization of graphene RF power amplifiers. The designs employed in our investigation were based on a physics-based compact simulation model of a GFET calibrated with the fabricated devices, showing an excellent agreement. From the present analysis, we conclude that efforts must be focused on preserving the superb intrinsic carrier mobility in graphene to guarantee a high transconductance, instead of pursuing the opening of a bandgap in graphene to achieve current saturation and the corresponding low output conductance.

4.5. Frequency multiplier: fostering graphene's ambipolarity

The following section is an adaptation of the paper [74] titled: "Exploiting Ambipolarity in Graphene Field-Effect Transistors for Novel Designs on High-Frequency Analog Electronics", published in *Small* in August 2023 by the authors: Francisco Pasadas, Alberto Medina-Rull, Francisco G. Ruiz, Javier Noe Ramos-Silva, Anibal Pachecho-Sanchez, Mari Carmen Pardo, Alejandro Toral-Lopez, Andrés Godoy, Eloy Ramírez-García, David Jiménez, and Enrique G. Marin.

4.5.1. Introduction

To push graphene electronics towards higher TRLs, and shaping GFETs as the core of novel RF applications, it is first necessary to deeply comprehend those factors that more critically impact the circuit performance [6], [33], [182]. Among them, the DPS is crucial in defining the circuit performance. Specifically, applications based on graphene ambipolarity need a tight control of the DPS. To this purpose, the inclusion of a back-gate in the GFET architecture has been the standard strategy followed so far. Numerous examples have been reported such as the polarity-controllable graphene inverter, the voltage controlled resistor [183], [184], or the graphene-based frequency tripler [185] and quadrupler [186] successfully implemented thanks to a carefully adjusted voltage separation of two cascaded GFETs. However, a more advanced graphene technology might require to abandon the four-terminal architecture because of the higher com-

plexity inherent to the fabrication process and, more importantly, the appearance of parasitics due to the back gate, seriously compromising the high-frequency performance [187]. Hence, a thorough understanding of the bias-dependent DPS is required for circuit design, an example of which will be presented to obtain frequency multiplication with single-gated GFETs.

On the other hand, the vast majority of experimental GFET-based circuits reported so far are founded on single-transistor stages [188]. However, the better performing circuits to come will rely on multiple-transistor stages, where the direct observations extracted from single devices become inappropriate. This section shows that a careful consideration of the DPS bias dependence is necessary to reach the optimal performance of multitransistor circuits. Specifically, the DPS experienced by each GFET in a differential topology can ruin the required symmetry, spoiling their performance. This deleterious effect has been reported, e.g., in [189] where a dissymmetry under large drain-to-source biases appeared between the two GFETs comprising a balun. In addition, a different DPS rate from the usually expected, i.e. half of the externally applied drain-to-source bias, has been observed in [190] for two GFETs connected in a complementary-like inverter topology. It is in this forthcoming technological arena where the DPS can hamper the performance of multi-GFET circuits; an issue that we intend to describe and rationalize in this section, which is structured as follows: first we deepen into the theory behind the DPS, by analyzing the electrostatics, and a comparison of the predictions against DC measurements of a GFET reported elsewhere [191]. Then we show the development of the frequency multiplier by making use of the DPS concept and of its understanding. Finally, the conclusions are drawn.

4.5.2. Dirac point shift (DPS): theory vs experiment

The Dirac voltage (V_{Dirac}) of a GFET is defined as the gate bias that sets the charge neutrality condition in the graphene channel, namely, the gate bias that results in a minimum conductivity, and therefore, it can be readily located at the vertex of the V-shaped transfer characteristic (TC) of the GFET. For a well-behaved long-channel GFET, we can estimate V_{Dirac} by considering same electron/hole mobility as well as symmetrical charge distribution, i.e., same electron/hole concentration at the source and drain edges. These concentrations can be obtained upon application of Gauss' law along a vertical cut of the GFET structure, i.e., assuming the gradual channel approximation, and after considering the quasi-Fermi levels equal to V_{s} and V_{d} at the source and drain terminals, respectively [192]. For ultra-short-channel devices, the 2D Poisson equation should be considered instead [193]. Aiming to get a compact equation that could be easily handled by circuit designers, only the long- channel case has been considered in this section.

Using the abovementioned methodology, the V_{Dirac}-terminal-bias dependence of a four-terminal GFET can be written as:

$$V_{\mathrm{Dirac}} = V_{\mathrm{go}} + \left(\frac{C_{\mathrm{t}} + C_{\mathrm{b}}}{C_{\mathrm{t}}}\right)\frac{V_{\mathrm{d}} + V_{\mathrm{s}}}{2} - \frac{C_{\mathrm{b}}}{C_{\mathrm{t}}}(V_{\mathrm{b}} - V_{\mathrm{bo}}) \tag{4.12}$$

where C_{t} and C_{b} are the top and bottom oxide geometrical capacitances per unit area, respectively, and $V_{\mathrm{g}} - V_{\mathrm{go}}$ and $V_{\mathrm{b}} - V_{\mathrm{bo}}$ are the top and bottom gate voltage overdrive, respectively. These quantities embrace work-function differences between the gates and the graphene channel and the possible presence of additional charges due to impurities or doping. The dependence of V_{Dirac} in eq. (4.12) on V_{d} and V_{s} is a unique feature in devices with ambipolar transport [194], and has also been observed in carbon nanotube devices [195], [196]. Indeed, the term $\frac{C_{\mathrm{b}}}{C_{\mathrm{t}}}(V_{\mathrm{b}} - V_{\mathrm{bo}})$ in eq. (4.12) has been usually used to experimentally obtain the ratio $(C_{\mathrm{b}}/C_{\mathrm{t}})$ by sweeping V_{b} while keeping the rest of terminal biases constant [70], [197], [198].

If one of the gate capacitances per unit area, e.g. the top-gate, is much larger than the other, i.e. $C_{\mathrm{t}} \gg C_{\mathrm{b}}$, then the four-terminal GFET can be considered as a three-terminal device and eq. (4.12) simplifies into:

$$V_{\mathrm{Dirac}} = V_{\mathrm{go}} + \frac{V_{\mathrm{d}} + V_{\mathrm{s}}}{2} \tag{4.13}$$

as shown in Chapter 2.

Most of experimental GFETs found in the literature are either three-terminal devices or four-terminal ones where the condition $C_{\mathrm{t}} \gg C_{\mathrm{b}}$ is met, and therefore, eq. (4.13) commonly applies. Remarkably, the bias dependence of V_{Dirac} reported in the literature [189], [190], [199]–[201] is in many cases successfully connected to the external drain and source biases, $V_{\mathrm{d,e}}$ and $V_{\mathrm{s,e}}$, respectively, specifically to $(V_{\mathrm{d,e}} - V_{\mathrm{s,e}})/2 = V_{\mathrm{ds,e}}/2$, instead of $(V_{\mathrm{d}} + V_{\mathrm{s}})/2$ predicted in eq. (4.13) (Figure 4.20a schematically depicts the difference between external and intrinsic voltages). We have found out the reason of such a coincidence and carried out measurements to demonstrate that eq. (4.13) should be considered instead.

Figure 4.20a shows the equivalent resistive networks of both three- and four-terminal GFETs with the intrinsic graphene channel resistance (R_{ch}) and the extrinsic drain (R_{d}) and source (R_{s}) resistances. These include the drain and source metal-graphene contact resistances, respectively, which are currently crucial and undesirable elements impacting the RF performance of GFETs [24], [57], [77], [117], [202]–[207]. For the sake of simplicity, bias-independent contact resistances have been considered in the device modelling approach of this section. The bias dependence of physical effects at metal-graphene interfaces affecting the carrier transport [204], [207] can be embraced by the channel charge description as incorporated by the device model used here [71]. Assuming that the drain/source extrinsic resistances are similar $R_{\mathrm{ext}} = R_{\mathrm{d}} \approx R_{\mathrm{s}}$, then the intrinsic drain and source voltages (V_{d} and V_{s}, respectively) can be determined as:

$$V_{\mathrm{d}} = V_{\mathrm{d,e}}\frac{1+x}{2+x} + V_{\mathrm{s,e}}\frac{1}{2+x} \tag{4.14}$$

$$V_{\mathrm{s}} = V_{\mathrm{d,e}}\frac{1}{2+x} + V_{\mathrm{s,e}}\frac{1+x}{2+x} \tag{4.15}$$

where $x = R_{\mathrm{ch}}/R_{\mathrm{ext}}$. Interestingly, from eq. (4.15) we observe, adding up both expressions, that the equality $V_{\mathrm{d}} + V_{\mathrm{s}} = V_{\mathrm{d,e}} + V_{\mathrm{s,e}}$ holds and as $V_{\mathrm{s,e}}$ is usually shorted to ground,

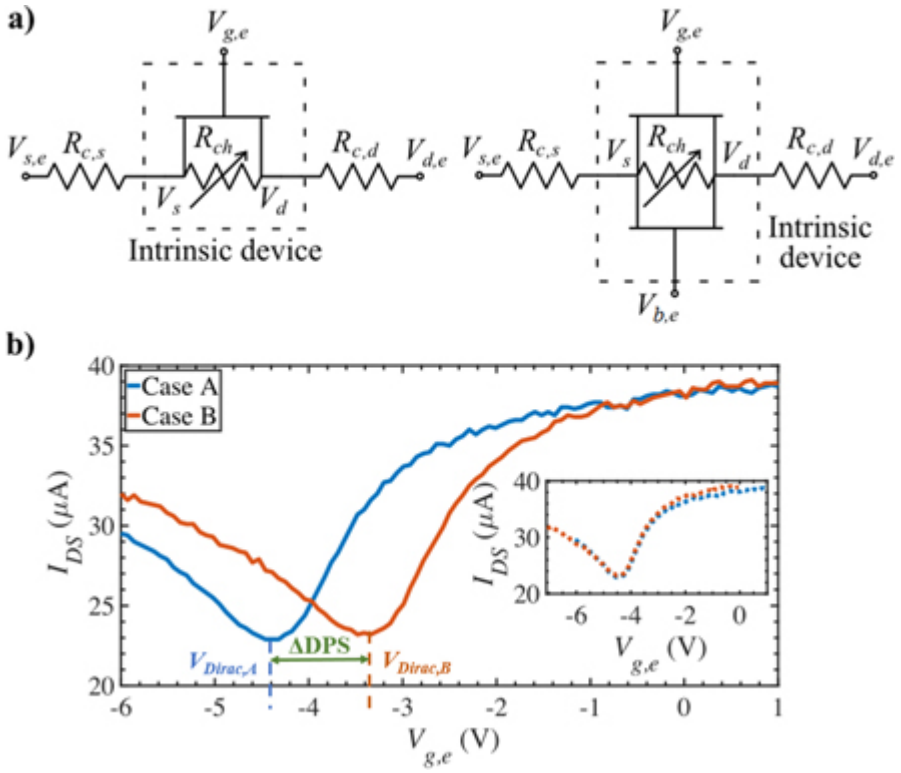


Figure 4.20.: a) Schematics of the three- (left) and four-terminal (right) GFET resistive networks. The electrostatic modulation of the bias-dependent channel resistance (R_{ch}) is achieved via the gate terminal(s)($V_{\mathrm{g,e}}$ and/or $V_{\mathrm{b,e}}$). Due to the non-negligible metal-graphene contact resistances (R_{s} and R_{d}), a substantial potential drop is produced so that the intrinsic voltages (V_{s} and V_{d}), not accessible in practice, are quite different from the external ones ($V_{\mathrm{s,e}}$ and $V_{\mathrm{d,e}}$). b) Measurements of the DC TCs of the GFET reported in [31] at two different operating bias point: (Case A) $V_{\mathrm{d,e}} = 0.1\,\mathrm{V}$ and $V_{\mathrm{s,e}} = 0\,\mathrm{V}$; and (Case B) $V_{\mathrm{d,e}} = 1.1\,\mathrm{V}$ and $V_{\mathrm{s,e}} = 1\,\mathrm{V}$, showing a different DPS despite considering the same $V_{\mathrm{ds,e}}$ in both cases (ΔDPS$= V_{\mathrm{Dirac,A}} - V_{\mathrm{Dirac,B}}$). (inset) Measured transfer characteristics after countering the DPS according to the model proposed in eqs. (4.13) and (4.15).

Param.	Value	Param.	Value
L_g	$1\,\mu m$	μ	$0.2\,m^2/Vs$
W_g	$1\,\mu m$	V_{go}	$0\,V$
$C_{ox} = C_t$	$8\,fF\mu m^{-2}$	$R_{d,s}W_g$	$200\,\Omega\mu m$
n_{res}	$6.86 \times 10^{11} cm^{-2}$	R_gL_g	$5\,\Omega\mu m$

Table 4.5.: GFET technology for the frequency multiplier design.

then $(V_d + V_s) = V_{ds,e}$. However, this is not a general case, 4.20b shows a proper counterexample: the TCs of a 14-µm-length GFET reported in [31] in two scenarios: (Case A) $V_{d,e} = 0.1\,V$ and $V_{s,e} = 0\,V$; and (Case B) $V_{d,e} = 1.1\,V$ and $V_{s,e} = 1\,V$; thus keeping in both cases same $V_{ds,e} = 0.1\,V$, but in case B breaking the condition of $V_{s,e}$ grounded. As it can be seen, in spite of what has been so far widely reported [189], [190], [199]–[201], the DPS indeed depends on $(V_d + V_s)$, as the same $V_{ds,e}$ cannot explain these two different DPSs. The inset in figure 4.20b shows the measured TCs after countering the DPS according to eqs. (4.13) and (4.15), supporting the exposed theory and demonstrating a perfect cancellation of the shift.

More importantly, because of the presence of non-negligible extrinsic resistances in GFETs, the potential V_s cannot be shorted to reference in practice. Indeed, recent studies on contact resistance of GFETs [208], [209] show that the ratio $x = R_{ch}/R_{ext}$ is lower than 1 for the vast majority of experimental devices, meaning that most of the external $V_{ds,e}$ drops at the extrinsic resistances. Thus any change in either $V_{g,e}$ or $V_{d,e}$ would cause a change in V_s, revealing that the DPS needs to be taken into account in the circuit design.

4.5.3. Frequency multiplier design

The V_{Dirac} shifting originated by tuning V_d and V_s together with graphene ambipolarity can be both exploited to build a circuit with a W shaped TC, enabling frequency multiplication with control of the harmonic amplitudes [210]. The simplest implementation of such circuit considers a lumped resistor (R_X) between two GFETs connected in cascade. The resistor produces a controlled splitting between the V_{Dirac} of both GFETs, $V_{Dirac,1} - V_{Dirac,2}$, which is proportional to the voltage drop at R_X as shown in Figure 4.20a. Indeed, the role of R_X can be played by the sum of extrinsic source and drain contact resistances of GFET1 and GFET2, respectively, as well as intentional graphene access resistance introduced between both devices. It is worth to note that the frequency multiplier design only demands a W-shaped TC and therefore the actual implementation could exploit different mechanisms for controlling the V_{Dirac} splitting, e.g., with a single split-gate GFET architecture [211] or by means of different R_s and R_d metal engineering in ultrascaled structures [212]. Indeed, W-shaped responses have been already observed in back-gate GFETs [210], although in an uncontrolled way as illustrated by the fact that devices with the same structure and dimensions presented different behaviors.

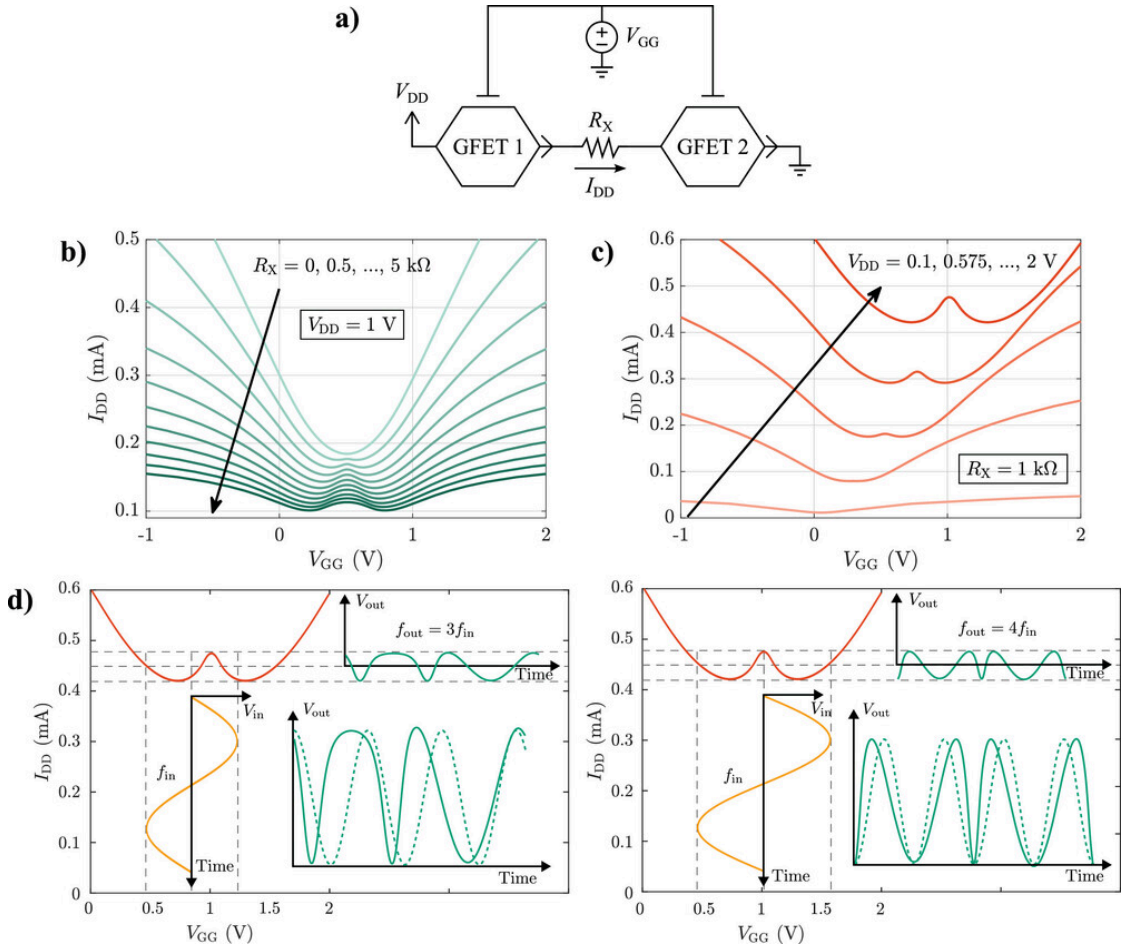


Figure 4.21.: a) Schematics proposed to build graphene-based frequency multipliers taking advantage of graphene ambipolarity. GFET technology used is described in Table 4.5. The inclusion of a resistor, R_X, between two cascaded GFETs is proposed so to originate W-shaped transfer characteristics which can be leveraged to frequency multiplication. Transfer characteristics for different b) values of R_X (at $V_{DD} = 1\,V$); and c) supply biases, V_{DD} (considering $R_X = 1\,k\Omega$). d) Working principle for the GFET-based frequency tripler (left) and quadrupler (right) based on the transfer characteristic at $V_{DD} = 2\,V$ and $R_X = 1\,k\Omega$. (Green solid lines) Output signals of the frequency tripler (left) and quadrupler (right) compared against (green dashed lines) pure sinusoids at corresponding frequencies.

Figure 4.21a depicts the simplest design of a controlled frequency multiplier exploiting the GFET ambipolarity: the two GFETs are governed by the same gate bias (V_{GG}) and are connected in series through R_{X}. The GFET technology used in the design is shown in Table 4.5. The drain of the first GFET is coupled to the power supply (V_{DD}) while the source of the second FET is DC grounded. The description of the used graphene technology is shown in Table 4.5. The output of the frequency multiplier is the GFET current. Figures 4.21b and c show the resulting W-shaped TC for different values of R_{X} (with $V_{\mathrm{DD}} = 1\,\mathrm{V}$) and for several values of V_{DD} (with $R_{\mathrm{X}} = 1\,\mathrm{k\Omega}$), respectively. The minima of the W-shaped TC correspond to the Dirac voltages of each GFET. The splitting between these charge neutrality points increases with the value of R_{X}, which also results in an increasing voltage drop at the resistor, reducing the overall current. The DC bias operation point of the multiplier completely defines the multiplication factor given by the frequency multiplier (Figure 4.21d). Roughly, for tripler operation, V_{GG} must be set in the mid-point between the $V_{\mathrm{Dirac},1}$ (or equivalently $V_{\mathrm{Dirac},2}$)and the relative maximum of the W, while for a frequency quadrupler, the operating bias point must correspond with the relative maximum, as shown in Figure 4.21d). It is well known that a frequency doubler can be also implemented just with one GFET by DC biasing at the V_{Dirac}, and this also holds for the cascaded design. The possibility of generating different harmonic multiplication factors simply by changing the DC operation point becomes a sort of reconfiguration capability enabled by the ambipolarity of the GFET, which substantially simplifies the circuit design for frequency manipulation. Figure 4.21d exemplifies the operation of the circuit as a frequency tripler and quadrupler with a sketch of input and output AC signals around the corresponding operation points (for $V_{\mathrm{DD}} = 2\,\mathrm{V}$ and $R_{\mathrm{X}} = 1\,\mathrm{k\Omega}$ with the TC shown with a green solid line in Figure 4.21c). A comparison between the predicted output signals (solid) and pure sinusoids at corresponding frequencies (dashed), shows that there is still an evident distortion in not optimized devices. As a case in point, for an input frequency of $f_{\mathrm{in}} = 1\,\mathrm{MHz}$, the analysis of the output power spectrum, achieved from circuit-level simulations in the nonoptimized scenario, indicates that the resulting HF relative power for the frequency tripler and the quadrupler at $3f_{\mathrm{in}}$ and $4f_{\mathrm{in}}$, respectively, are around the 50%. The performance of GFET-based frequency multipliers can nevertheless be improved by optimizing the W-shaped TC together with additional matching and stability networks.

4.5.4. Conclusions

This section demonstrates that the DPS in GFETs is proportional to the intrinsic voltages $(V_{\mathrm{d}} + V_{\mathrm{s}})$, not accessible in practice, which can be considerably different from the externally applied biases due to the non-negligible metal-graphene contact resistances. It has been shown that the validity of the usual approximation that considers the DPS proportional to $V_{\mathrm{ds,e}}$, is limited and should be avoided.

Thus, a simple analytic equation for long-channel GFETs has been provided in order to evaluate the bias-dependence of DPS that could be compensated by the automatic application of an effective gate bias. As a proof of concept, a frequency tripler/quadrupler

based on W-shaped transfer characteristic of two cascaded single-gated GFETs is proposed, evidencing that monitoring the bias-dependence of the DPS is pivotal for the design of RF applications. In summary, this section provides critical insights on DPS phenomenon paving the way towards the development of RF multi-transistor circuits based on graphene technology.

4.6. Oscillator: exploiting instability

The following section is an adaptation of the paper [213] titled: "10 GHz Negative Resistance Oscillator Using a Graphene Field-Effect Transistor", submitted for journal publication in May 2024 by the following authors: Alberto Medina-Rull, Francisco Pasadas, Enrique G. Marin, Andrés Godoy, Andrei Vorobiev, Jan Stake and Francisco G. Ruiz.

4.6.1. Introduction

Oscillators are key building blocks of numerous radio-frequency (RF) circuits, such as mixers, modulators, or phase-locked loops (PLLs) [214]. They are indispensable in RF systems like transceivers, vector network analyzers (VNAs) or signal generators [119]. Despite their crucial role within wireless transceivers, their implementation on graphene-based technologies remains partially unexplored, with only ring [139], [215] and mechanical [216], [217] oscillators being demonstrated.

This section presents the design and performance projection of a negative-resistance oscillator (NRO) based on a graphene field-effect transistor (GFET) operating at $\sim 10\,\mathrm{GHz}$. First, the fabrication and characterization of the GFET technology is discussed. Next, the GFET compact simulation model is calibrated to reproduce the experimental data. Finally, the oscillator design procedure following the negative-resistance method is shown, and the resulting NRO performance is assessed.

4.6.2. Device technology and CAD model calibration

For the design of the oscillator, a CVD graphene FET is employed as the active device. Fig. 4.22 shows a scanning electron microscope (SEM) image of the fabricated device, with a gate length of $L_\mathrm{g} = 0.5\,\mu\mathrm{m}$, a width of $W_\mathrm{g} = 2\,\mu\mathrm{m}\times 15\,\mu\mathrm{m}$, and a $22\,\mathrm{nm}$ ALD-deposited Al_2O_3 gate oxide (equivalent oxide thickness, EOT, of $= 14.8\,\mathrm{nm}$). The device is fabricated on a silicon/silicon dioxide (Si/SiO_2) substrate, with a SiO_2 thickness of $1\,\mu\mathrm{m}$ in order to reduce parasitic pad capacitances that form between the pads and the Si substrate. Further details on the fabrication process can be found in [76].

DC and RF characterization of the fabricated device were performed with a Keithley 2612B dual-channel source meter, and an Agilent N5230A network analyzer using the on-wafer CS-5 calibration substrate, respectively.

Table 4.6 shows the GFET parameters resulting from the calibration. Fig. 4.23a displays the $I_\mathrm{DS} - V_\mathrm{GS,e}$ curve for $V_\mathrm{DS,e} = -0.1\,\mathrm{V}$, showing the experimental data (red

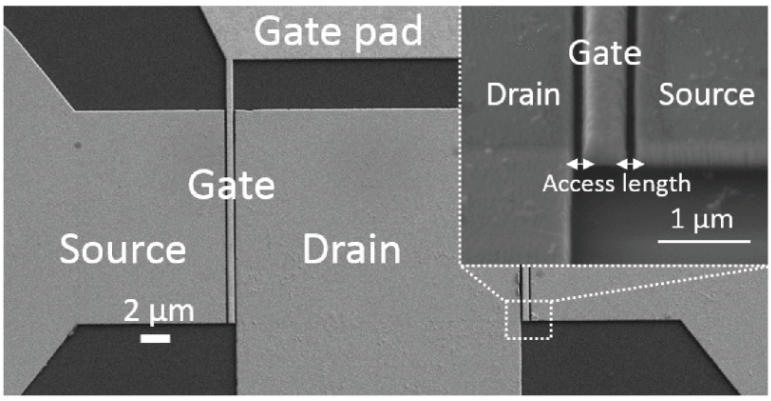


Figure 4.22.: SEM image of the fabricated GFET. The inset shows a 70° tilted view of the gate area. Image taken from [76].

Param.	Value	Param.	Value
L_g	$0.5\,\mu m$	μ	$0.16\,m^2/Vs$
W_g	$2 \times 15\,\mu m$	V_{go}	$1.38\,V$
C_{ox}	$2.3\,fF\mu m^{-2}$	$R_{d,s}W_g$	$90\,\Omega\mu m$
n_{res}	$8.3 \times 10^{11}\,cm^{-2}$	R_gL_g	$18\,\Omega\mu m$

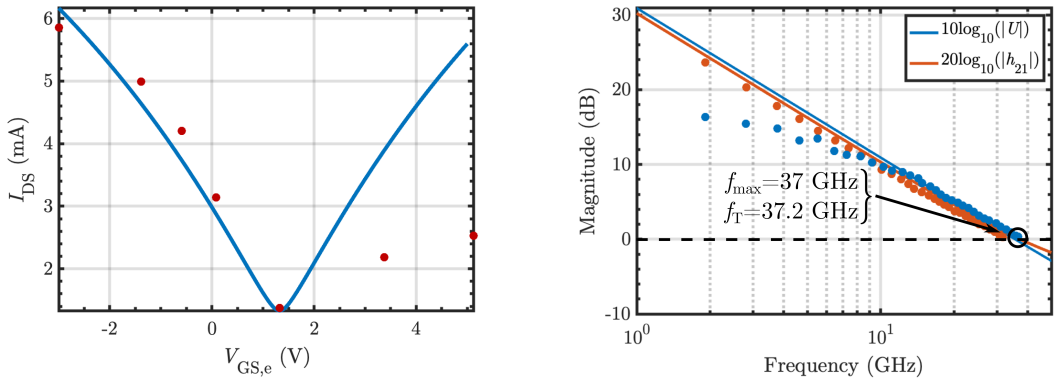
Table 4.6.: GFET technology for the oscillator design.

dots) and the simulated data (blue curve), exhibiting a good agreement on the hole conduction branch, which will be the transport region used for the design. As for the RF performance, the device is evaluated in a common-source configuration, with Fig. 4.23b showing the U the h_{21}, marking their crosses with the dashed $0\,dB$ line. A very good agreement in both curves is observed, with simulated values of $f_{max} = 37\,GHz$ and $f_T = 37.2\,GHz$, compared to the measured $f_{max} = 37\,GHz$, $f_T = 34\,GHz$ [76].

As for design convenience, only one finger of the device will be used, i.e., a GFET with $W_g = 15\mu m$ will be considered in the design, while the rest of the parameters will be kept as in Table 4.6.

4.6.3. Oscillator design and results

The design method of choice is the negative-resistance method [214], consisting in using the active device, in this case the GFET, to get an input impedance which has a negative real part, i.e., a negative resistance. Assuming the active device as a two-port circuit, this can only be achieved if there is some terminating impedance Z_T, in any of the two-ports, that provokes the magnitude of the reflection coefficient at the other port (hereinafter, the input port) greater than one. After that, selecting the proper load impedance at the remaining port of the transistor so that $Z_L = -Z_{in}$ will result in a stable oscillation. A simplified diagram of the circuit is shown in Fig. 4.24.



(a) (b)

Figure 4.23.: (a) $I_{DS}-V_{GS,e}$ adjustment for $V_{DS,e} = -0.1\,V$. (b) U and h_{21} versus frequency pointing fitted f_{max} and f_T values, respectively, at $V_{GS,e} = 0.5\,V$ and $V_{DS,e} = -1.1\,V$. The dashed line marks the 0 dB value. In both figures lines correspond to simulations, while dots to measurements.

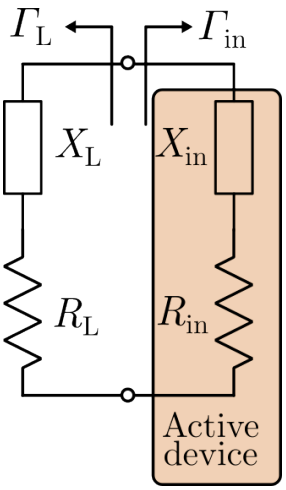
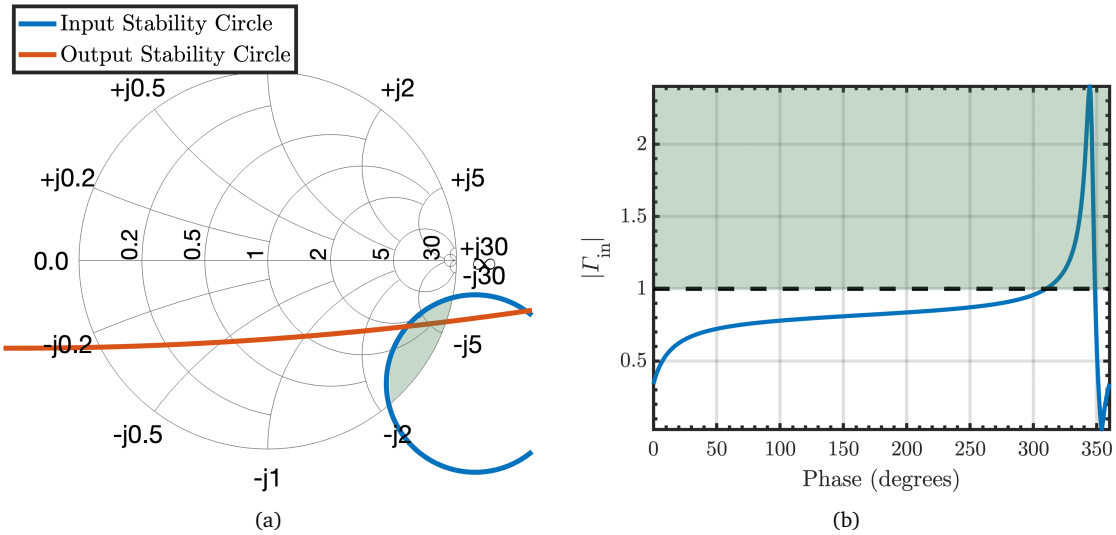


Figure 4.24.: Diagram of the negative-resistance method.



(a) (b)

Figure 4.25.: (a) Input and output stability circles and (b) $|\Gamma_{\mathrm{in}}|$ as a function of the phase of Γ_{T}. The green regions show the areas where $|\Gamma_{\mathrm{in}}| > 1$.

However, in order for the oscillation to arise, at the beginning we need $R_{\mathrm{in}} + R_{\mathrm{L}} < 0$ and after some time $R_{\mathrm{in}} + R_{\mathrm{L}} = 0$ and also $X_{\mathrm{L}} + X_{\mathrm{in}} = 0$, i.e., $Z_{\mathrm{L}} = -Z_{\mathrm{in}}$. This change in the sum $R_{\mathrm{in}} + R_{\mathrm{L}}$ is possible due to the dependence of Z_{in} with the amplitude of the signal in the circuit, i.e., $Z_{\mathrm{in}} = Z_{\mathrm{in}}(\omega_0, A)$, where ω_0 is the design angular frequency. For this reason, a large-signal analysis of the oscillator is required to determine the value of Z_{L} that triggers the oscillation.

In order to find proper loading conditions for the GFET, we need to first analyze its stability at the initial design frequency $f_{\mathrm{i}} = 10\,\mathrm{GHz}$. For that matter, in Fig. 4.25a, the input (blue, gate port) and output (orange, drain port) stability circles are plotted on a Smith chart for a bias of $V_{\mathrm{GS,e}} = 0\,\mathrm{V}$ and $V_{\mathrm{DS,e}} = -1.3\,\mathrm{V}$. An inductive feedback between the drain and the gate of the GFET has been added in order to increase instability. In our design, the gate port is selected for the terminating impedance, and for this reason the unstable region of the input stability curve has been shaded in green. Any Z_{T} choice within this region will produce an input reflection coefficient with modulus greater than one in the drain port ($|\Gamma_{\mathrm{in}}| > 1$), i.e., an input impedance with negative resistance. However, not every value of Z_{T} provides the same value of $|\Gamma_{\mathrm{in}}|$: thus, in order to get a better grasp of the influence of the selected value of Γ_{T}, Fig. 4.25b represents $|\Gamma_{\mathrm{in}}|$ against the phase of Γ_{T}, assuming $|\Gamma_{\mathrm{T}}| = 1$, which will give a purely reactive Z_{T} and minimize power consumption at the gate port. The highest $|\Gamma_{\mathrm{in}}|$ value occurs at $\Gamma_{\mathrm{T}} = e^{j344^\circ}$, which is thus the selected for the design. At the initial design frequency, the resulting Z_{T} value is achieved with a $C_{\mathrm{T}} = 58\,\mathrm{fF}$ capacitor. The narrow phase window in which the unstable region of $|\Gamma_{\mathrm{in}}|$ moves could be problematic if C_{T} changes its value during fabrication. For that reason, it has been checked that, assuming a 10% tolerance for this capacitor, the value of $|\Gamma_{\mathrm{in}}|$ would still be well within the unstable region.

Once Z_{T} is determined, Z_{L} is typically designed using the rule of thumb $X_{\mathrm{L}} = -X_{\mathrm{in}}$

P_{AVS} (dBm)	Z_{in} (Ω)	P_{ADD} (dBm)
-18	-6.3+j56.1	-24.1
-14	-5.3+j57.3	-21.1
-10	-2.8+j59.7	-20.1
-6	2.2+j63.5	$\notin \mathbb{R}$

Table 4.7.: Large-signal analysis results showing the average power, P_{AVS}, the input impedance, Z_{in}, and the added power, P_{ADD}.

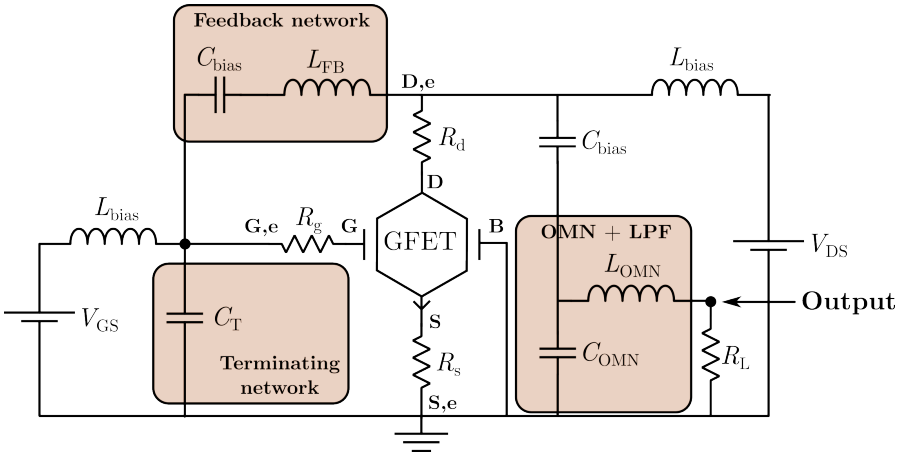


Figure 4.26.: Schematic of the oscillator circuit ($Z_0 = 50\,\Omega$).

and $R_{\mathrm{L}} = |R_{\mathrm{in}}|/3$. However, in order to optimize the power transfer to the load, a large-signal analysis of the input impedance Z_{in} is performed [214]. For that, with the designed C_{T} connected to the gate port, a signal generator is attached to the drain port and a Harmonic Balance simulation is performed, sweeping the input available power P_{AVS}. The results of this analysis are shown in Table 4.7, where P_{ADD} is the added power, defined as $P_{\mathrm{ADD}} = P_{\mathrm{AVS}}(|\Gamma_{\mathrm{in}}|^2 - 1)$, which is a fair good approximation of the resulting oscillator power [214]. As the power of the input signal increases, R_{in} becomes less negative, up to the point where it becomes positive. The strategy here is to select a high value P_{AVS} that keeps R_{in} negative, so that the oscillation stabilizes at a high power value. In our design, a suitable value can be found close to $P_{\mathrm{AVS}} = -10\,\mathrm{dBm}$, where $Z_{\mathrm{L}} = -Z_{\mathrm{in}} = (2.82 - j59.70)\,\Omega$, which will be thus the desired load impedance that will be transformed from a standard $50\,\Omega$-load using an L-C network.

The schematic of the designed oscillator is shown in Fig. 4.26. Three parts of the design have been remarked: the feedback network, including a feedback inductance between drain and gate terminals; the terminating network, designed to obtain a negative-resistance input impedance seen from the output port of the GFET; and finally the output matching network, which matches a $50\,\Omega$ load to the desired Z_{L} (for $P_{\mathrm{AVS}} = -10\,\mathrm{dBm}$). This output matching network has also been designed to be a low-pass filter that suppresses the third harmonic, which initially resulted higher than desired.

Param.	Value	Q
C_{T}	58 fF	10
L_{FB}	5.5 nH	10
L_{OMN}	5.5 nH	10
C_{OMN}	180 fF	10

Table 4.8.: Lumped components for the designed GFET NRO.

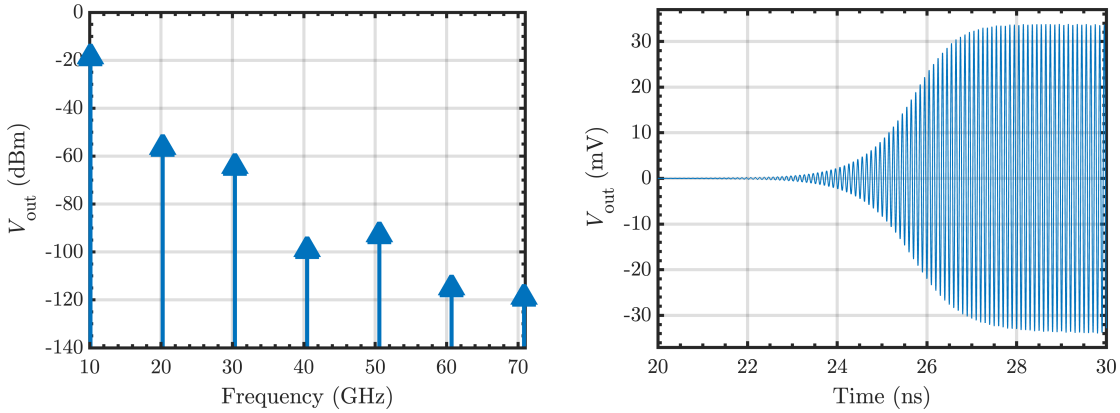


Figure 4.27.: (a) Frequency spectrum and (b) transient response of the output voltage V_{out}, as a result of the Harmonic Balance and Transient simulations, respectively. The time domain analysis shows the begin of the oscillations while the frequency spectrum reveals a fundamental frequency of oscillation of 10.12 GHz with an output power of $P_{\mathrm{out}} = -18.81$ dBm.

A quality factor of $Q = 10$ has been assumed for all the components in the simulations, which makes the initially designed impedances Z_{T} and Z_{L} to slightly change, and consequently modifies the oscillation frequency and the output power. In order to solve this, a final tuning process on the L-C matching network has been carried out with the aim of i) adjusting the oscillation frequency to 10 GHz, and ii) maximizing the output power. The final values of the passive elements in the design are shown in Table 4.8. A fabrication process allowing for the fabrication of the proposed passives could be similar to the one in [218].

Figures 4.27a and 4.27b show the frequency spectrum and the time domain signal of the output voltage, V_{out} (as labeled on the schematic of Fig. 4.26), obtained from the Harmonic Balance and transient simulations, respectively. The frequency spectrum of Fig. 4.27a shows the fundamental oscillation frequency at 10.12 GHz and an output power of $P_{\mathrm{out}} = -18.81$ dBm delivered to the 50 Ω load. The second and higher order harmonics are strongly reduced (> 30 dB) with respect to the fundamental oscillation frequency. Finally, the transient analysis of Fig. 4.27b depict the oscillation initiation and stabilization, which is fully achieved after ~ 30 ns.

4.6.4. Conclusions

This section presents the design of a graphene-based microwave oscillator. The oscillator is designed following the negative-resistance method and a fabricated GFET is considered as the active device. The design includes an inductive feedback between the drain and the gate of the GFET, in order to increase the instability of the device, a purely reactive terminating impedance, which minimizes power consumption, and an output matching network which matches a $50\,\Omega$ load to the desired load impedance, while simultaneously acting as a low-pass filter in order to suppress the higher harmonics. The performance projection shows an oscillation frequency of $10.12\,$GHz, and a 50-ohm delivered power greater than $-19\,$dBm.

Chapter

5. MIG-based RF circuit designs

This chapter is an adaptation of the paper [219] titled: "A Novel Analysis of Periodic Structures Based on Loaded Transmission Lines", published in *IEEE Journal of Microwaves* in May 2023 by the following authors: Alberto Medina-Rull, Francisco Pasadas, Enrique G. Marn, Andrs Godoy, and Francisco G. Ruiz.

5.1. Introduction

Periodic structures are recurrent in physics, ranging from electronics to quantum mechanics, passing by material science and semiconductor crystal theory [220]–[222]. In the particular realm of microwave engineering, periodically loaded transmission lines are well known and have been widely exploited as filters [119], [223]–[225] and phase shifting devices [226]–[230]. The latter application has been recently addressed by the employment of complex structures, enabling the improvement of the phase shift range while, simultaneously, increasing the return losses [231]–[233].

Being a long-established topic in microwave engineering, the analysis of periodic transmission line structures has led to different treatments. The most general and well-known study focuses on the necessary conditions for a wave to propagate without attenuation through an infinite periodic structure, formed by repeated unit-cells such as the one shown in Fig. 5.1 (see, for example, [119] or [223] and the references therein). The unit-cell of this periodic structure comprises two segments of a TL and a shunt susceptance in between. The condition for the wave to propagate unattenuated is that the voltage (V_n) and current (I_n) at some point n of the periodic structure must equal the voltage (V_{n+1}) and current (I_{n+1}) at the point $n+1$, except for a phase shift difference due to the propagation delay from point n to $n+1$. This delay is related to the propagation constant of the periodically loaded TL, $\gamma = \alpha + j\beta$, where α is the attenuation constant and β the phase constant. If $\alpha = 0$ and $\beta \neq 0$, the wave is not attenuated through the line, delimiting the so-called passbands of the structure. In contrast, when $\alpha \neq 0$ and $\beta = 0$, the wave is attenuated during its propagation, giving rise to the so-called stopbands [119], [223] (see Fig. 5.2).

This remarkable frequency response reveals itself more striking when looking in more detail at the passbands, which exhibit a comb-alike shape, yielding to new pass and

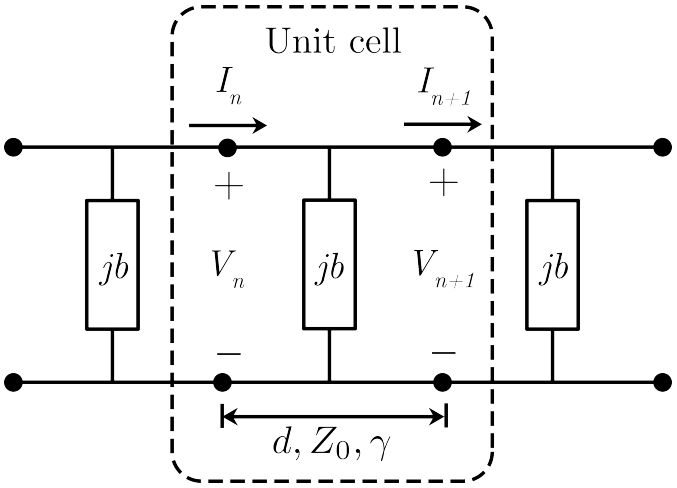


Figure 5.1.: Periodic structure unit-cell. V_n and I_n are the voltage and current at port n, respectively. d, Z_0 and γ are the total length, characteristic impedance and propagation constant of the TLs conforming the unit-cell, respectively. b is the susceptance of the shunt admittance.

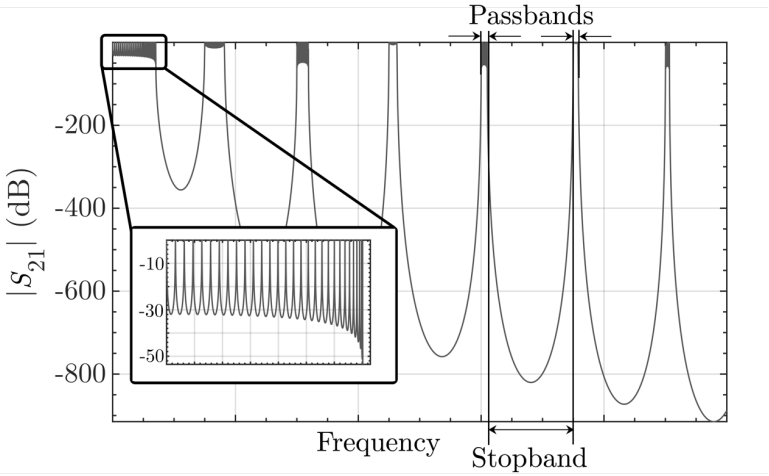


Figure 5.2.: Characteristic frequency response of the periodic structure of Fig. 5.1 for a very large number of unit-cells. The inset shows a zoom of one of the passbands.

stopbands very close to one another (see Fig. 5.2 inset). Moreover, this peculiar ripple is also observed when sweeping the susceptance (b), meaning that the use of a variable capacitor would enable the possibility of changing from one band to another. In fact, even though these nested passbands/stopbands are not as highly differentiated in magnitude as the main ones, the considerably smaller spacing between two consecutive bands is a distinguishing advantage with great potential for a number of microwave applications, such as tunable filters or phase shifters. To bring this potential to practice, it becomes essential to accurately know the position of the transmission peaks, i.e., the points where the available power is transmitted to the load. However, in spite of the simplicity and relevance of the analysis, this has been historically obliterated and concealed from practical microwave applications, mostly motivated by the twofold intrinsic limitations of the generic analysis [119], [223]: (i) it is based on an infinite periodic structure, and (ii) it considers only two alternatives for the wave in the structure: either it does propagate or not, meaning that it is not possible to account for the ripple inside each passband.

In the case of the analysis of a finite periodic structure, it is worth to mention a few works shedding light on the topic. In [234], an analysis of the input impedance of cascaded identical twoport networks was addressed, concluding that its value approached one of the iterative impedances of the twoports no matter what termination was used. In a specific case of the study it was observed that the input impedance was cyclic, meaning that for a certain number of unit-cells n, the input impedance was the same as for $2n, 3n, 4n$, etc. In [235], an alternative analysis was presented based on second-degree difference equations for the current along a cascade network. One of the examples provided to illustrate the analysis consisted of uniform networks with symmetrical passive sections, similar to the unit-cell shown in Fig. 5.1, where each TL section is replaced by an inductor (note that an inductor can be a fair good approximation of a short TL under certain conditions [236]). The analysis developed by means of this methodology resulted in the observation of the ripple inside the main passband, yet no exact method was provided to calculate the transmission peaks of this ripple.

Both references were, indeed, indebted to the original theory developed in [237] for the cascading of matrices and its use to calculate the transmission and reflection coefficients of a periodic structure. Also based on this theory, almost three decades later another investigation experimentally observed the ripple and proposed a theoretical analysis to rationalize the measurements [238], but still no exact expression was specified so as to calculate the transmission peaks nor to enable the design of the structure. Nonetheless, some relevant findings resulted, being the most remarkable one that the number of transmission peaks inside the first passband is $N = n - 1$, with n the number of cascaded unit-cells.

Among all these studies, the work by Griffiths and Steinke [239] stands out, presenting a thorough and complete analysis of wave propagation in one-dimensional periodic structures within different media, ranging from quantum mechanics to optical media, giving equations to calculate the transmission characteristics of finite periodic structures with any arbitrary number of unit-cells.

Despite the interest of these pioneering works, there are still many relevant aspects about the periodic structures to be unveiled in order to take full advantage of the pos-

sibilities that they provide. Specifically, only the frequency response of the structures has been considered in the previous analyses, but none of them explores the impact of changing the properties of the loading element, e.g. the capacitance in the case of a capacitive loading, which could be of great utility as it could be used to tune the circuit response once it is fabricated and by keeping the operating frequency. In addition, none of the previous analyses presents explicit expressions to determine the position of the transmission peaks of the ripple inside the main passbands.

To the purpose of giving a response to these questions, this chapter proposes a novel and comprehensive analysis based on S-parameters of periodic structures formed by TLs periodically loaded able to determine the position of the transmission peaks when sweeping the frequency of the input signal (frequency response) and, especially, when changing the properties of the loading. In our case, we will use the MIG diode as the loading due to its ability of changing its capacitance with the applied bias, behaving like a varactor, as explained in Chapter 2 and measured in Chapter 3.

The chapter is structured as follows: first, section 5.2 approaches the analysis and simulation of the structures by focusing on the behavior of only one unit-cell, aiming at its optimization with the goal of designing a phase shifter. Then, section 5.3 exposes the general analysis for the case of a periodic structure with any arbitrary number, n, of unit-cells, giving as a result the equation that allows to calculate the susceptance values where the transmission points occur within the structure. After that, section 5.4 extends the analysis and gives a more complete set of equations that can be used to gain control of both, the frequency response of the structure and its dependence with parameters such as the susceptance (b) or the characteristic impedance of the TLs (Z_0). This set of equations provides all the information regarding the particular response of the structure, giving the possibility of exploiting it in a large number of microwave applications, such as tunable filters, phase shifters, or reconfigurable matching networks. Later, in section 5.5, our theory is experimentally tested by the fabrication of a demonstrator circuit with five unit-cells, whose behavior is compared against both circuit simulations and the here-developed theory, achieving an excellent agreement. After that, section 5.6 firstly presents the phase behavior of the periodic structures aiming at using them as phase shifters and then shows the design of a phase shifter using a metal-insulator-graphene diode. Finally, conclusions are drawn in section 5.7.

5.2. An empirical approach: optimizing the unit-cell

5.2.1. Analysis and design

Before showing the full theoretical analysis of a periodic structure with n unit-cells, let's first approach the problem by thoroughly analyzing the behavior of one single unit-cell.

The main goal when designing a phase shifter is to obtain a phase that changes with respect to a control signal, in this case the bias applied to the varactor, while keeping constant the magnitude of the transmission parameter and as close to one as possible for this same bias variation, so as to avoid introducing neither losses nor amplitude

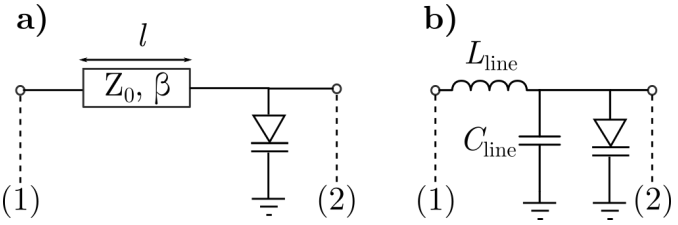


Figure 5.3.: Periodic structure unit-cell formed by a shunt MIG diode acting as a varactor and a section of transmission line implemented with a) distributed, and b) lumped elements.

variations on the transmitted signal. Let's thus first try to analytically calculate the S_{21} parameter of a single unit-cell as the one shown in Fig. 5.3a by means of the $ABCD$ parameters, which allow for direct matrix multiplication when circuit elements are cascaded, and optimize it for the commented premise. The $ABCD$ matrix of the shunt capacitive element of the unit-cell reads as:

$$ABCD_c = \begin{bmatrix} 1 & 0 \\ j\omega C & 1 \end{bmatrix} \tag{5.1}$$

where ω is the angular frequency and C the capacitor value. If we concatenate the TLs sections, the global $ABCD$ matrix of the complete unit-cell is given by:

$$ABCD_t = \begin{bmatrix} \cos(\beta d) - Z_0 \sin(\beta d)\omega C & jZ_0 \sin(\beta d) \\ j[Y_0 \sin(\beta d) + \cos(\beta d)\omega C] & \cos(\beta d) \end{bmatrix} \tag{5.2}$$

with β the phase constant and d the length of the TL; and $Y_0 = Z_0^{-1}$, where Z_0 is the characteristic impedance of the TL. By using the appropriate conversion formulae [240], $ABCD$ parameters can be converted to S parameters for a given port reference impedance Z_{ref}. In this regard, the magnitude of the S_{21} parameter reads as:

$$\begin{aligned} |S_{21}| = 2 \big[& \cos^2(\beta d) \left(4 + Z_{\text{ref}}^2 \omega^2 C^2\right) + \\ & \sin^2(\beta d) \left(Z_0^2 \omega^2 C^2 + 2 + Z_0'^2 + Y_0'^2\right) + \\ & 2\cos(\beta d)\sin(\beta d)\omega C \left(Z_{\text{ref}}^2 / Z_0 - Z_0\right) \big]^{-1/2} \end{aligned} \tag{5.3}$$

where $Z_0' = Z_0/Z_{\text{ref}}$ and $Y_0' = Y_0/Y_{\text{ref}}$ are the normalized transmission line impedance and admittance, respectively, Z_{ref} is the port reference impedance and $Y_{\text{ref}} = 1/Z_{\text{ref}}$. Although it is possible to analyse $|S_{21}|$ in (5.3), the problem can be simplified if the characteristic impedance of the TL and the port reference impedance are supposed to be equal, i.e., $Z_0 = Z_{\text{ref}}$. Under this assumption, (5.3) simplifies to:

$$|S_{21}| = \frac{2}{\sqrt{4 + (Z_0 \omega C)^2}} \tag{5.4}$$

From 5.4, if $|S_{21}|$ needs to be kept as close to the unity as possible, the condition $(Z_0\omega C)^2 \ll 4$ has to be met. Solving for Z_0, this condition provides the inequality $Z_0 \ll 2/(\omega C^{\max})$, where $C^{\max}$ is the highest capacitance value of the tunable capacitance (varactor). Therefore, it is possible to ensure very low IL ($|S_{21}| \sim 1$) by designing $Z_0 = Z_{\text{ref}}$, given the operating frequency f and the $C^{\max}$ that can be achieved by the varactor.

It is also worth mentioning that under this condition, $|S_{21}|$ has no dependence with the length of the TL, which can be useful for the distributed phase-shifter design process discussed later.

The phase of the S_{21} parameter, ϕ_{21}, can be calculated considering $Z_0 = Z_{\text{ref}}$:

$$\phi_{21} = \arctan\left(\frac{4\sin(\beta d) + 2Z_0\omega C\cos(\beta d)}{4\cos(\beta d) - 2Z_0\omega C\sin(\beta d)}\right) - \frac{\pi}{2} \tag{5.5}$$

The Z_0 value which provides the maximum phase shift range, i.e., the maximum difference between the highest and the lowest value of ϕ_{21}, the function $\Delta\phi_{21}$ is defined as: $\Delta\phi_{21} = \left|\phi_{21}(C^{\max}) - \phi_{21}(C^{\min})\right|$. This function can be maximized, resulting in the following value for Z_0:

$$Z_0 = \frac{2}{\omega\sqrt{C^{\max}C^{\min}}} \tag{5.6}$$

Guaranteeing $|S_{21}| \sim 1$ and maximum $\Delta\phi_{21}$ cannot be simultaneously met given that both conditions lead to the contradiction $C^{\max} \ll C^{\min}$. This means that there is a trade-off on choosing the Z_0 between achieving low IL and getting a wide phase shift range. However, provided that very low IL and RL are attained, it is possible to solve an eventual small phase shift range by concatenating several unit-cells.

5.2.2. Results for the empirical approach

In order to evaluate and validate the theory developed previously, the circuit shown in Fig. 5.3a is simulated in ADS using the compact simulation model of the MIG diode presented in Chapter 3. The length of the TL is chosen to be $l = \lambda/20$, and the operating frequency is set to be $f = 3\,\text{GHz}$. In Fig. 5.4, C of a MIG diode with the parameters shown in Table 5.1 is represented as a function of V_{bias} for two different Q_0 values. A bias range from -1.5 to $0.5\,\text{V}$ is considered, as it ensures coherence with the assumption of the small-signal model of the diode as a unique variable capacitor and also entails a very low dc power consumption. The capacitance in this range varies between 0.6 and $0.71\,\text{pF}$ for the value of Q_0 shown in Table 5.1. It is worth mentioning that the MIG diode technology we are considering, described in Table 5.1, has demonstrated high performance for applications that leverage the modulation of the insulator barrier height[78], [241]–[245]. However, the presence of a high residual charge density Q_0 limits the capacitance tunability to be very low for the considered bias window. In this regard, a lower value, e.g., $Q_0' = Q_0/3$ would improve the capacitance tunability from 0.15 to $0.52\,\text{pF}$ for the same bias window, what would mean a change in the relative

Parameter	Value	Parameter	Value
L_g	2 µm	T	295 K
W_g	80 µm	Q_0	-0.03 C/m^2
C_{ox}	7.1 fF/µm^2	$R_c W_g$	2 kΩµm

Table 5.1.: MIG diode technology benchmarked in [78] and used in the demonstration of the unit-cell developed theory for the design of a phase shifter.

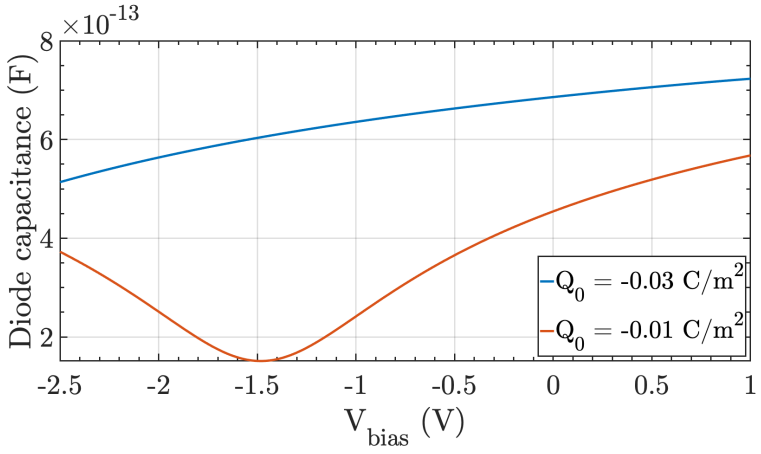


Figure 5.4.: Equivalent capacitance of the MIG diode described in Table 5.1 versus the bias voltage, V_{bias}, for two different Q_0 values.

capacitance tuning from 18.3% in the current technology to a 247.7% in the reduced residual charge density scenario. In addition, according to chapter 2 and as discussed in [246], to take advantage of the bias tunable graphene quantum capacitance, C_q, this has to be dominant over the geometrical oxide capacitance by achieving $C_{ox} \gg C_q$, which is not the case for the considered MIG diode technology meaning that there is room for improvement.

As mentioned above, there exists a trade-off with Z_0 between reducing the losses of the system in terms of getting the lower ILs, along with getting the desired phase shift range. In order to illustrate this trade-off, Fig. 5.5 depicts both $|S_{21}|$ and $\Delta\phi_{21}$ as a function of Z_0. In this work, we try to optimize the values of IL and RL as this would allow the concatenation of several stages, which can eventually enable the achievement of a larger phase shift range.

The design of Z_0 to achieve low IL is developed by fulfilling $Z_0|_{f=3\,\text{GHz}} \ll 150\,\Omega$. In doing so, Z_0 is chosen as $15\,\Omega$. In order to adapt the circuit to the standard measurement reference ports of $50\,\Omega$, two $\lambda/4$ adapters are used at input and output ports. Figure 5.6 depicts $|S_{21}|$ and $|S_{11}|$ in two scenarios: first, employing the value designed to provide low IL ($Z_0 = 15\,\Omega$, solid lines); second, the standard case where $Z_0 = 50\,\Omega$ (dashed lines). As shown, much better performance is achieved for $Z_0 = 15\,\Omega$, as IL can be reduced from around 1 dB down to around 0.2 dB; as a consequence, RL are also increased from around 11.5 dB up to 21.5 dB. On the other hand, Fig. 5.7 represents the

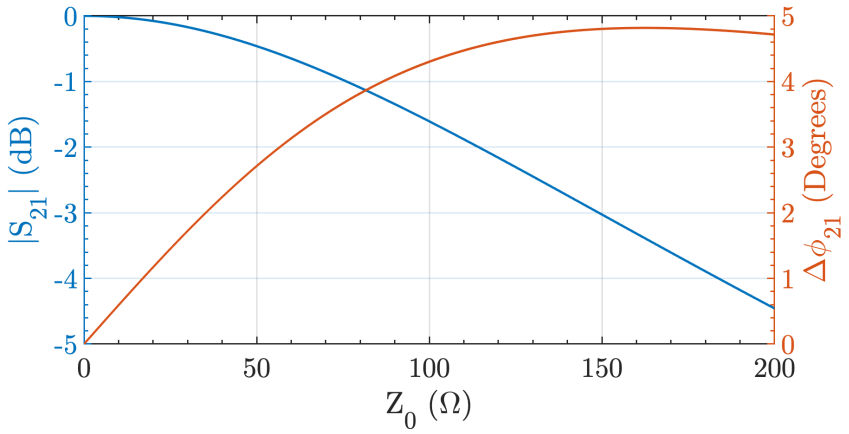


Figure 5.5.: $|S_{21}|$ (left axis) and $\Delta\phi_{21}$ (right axis) versus the characteristic impedance of the TL as well as the reference port impedance Z_0.

V_{bias} dependence of ϕ_{21}. As expected, the phase shift range is larger when $Z_0 = 50\,\Omega$ (1.44°) than for $Z_0 = 15\,\Omega$ ($\Delta\phi_{21}$ =0.55°). Nevertheless, the better values for IL and RL obtained for $Z_0 = 15\,\Omega$, according to Fig. 5.6, will be chosen to concatenate several unit-cells to linearly increase $\Delta\phi_{21}$, as will be shown later.

Figures 5.8 and 5.9 show the performance for $N = 10$ cascaded unit-cells with $Z_0 = 15\,\Omega$ (solid lines). It can be seen that IL ~ 2 dB and RL ~ 18 dB are kept under reasonable values; while for the case $Z_0 = 50\,\Omega$, IL are increased up to around 5 dB while RL are decreased down to around 10 dB. The phase shift range has been increased linearly with N as: $\Delta\phi_{21}|_N = N \cdot \Delta\phi_{21}|_{N=1}$. This means that the phase shift range is still better in the case of $Z_0 = 50\,\Omega$ (12.85°) than in the case of $Z_0 = 15\,\Omega$ (4.97°). However, at this point it would be possible to further concatenate unit-cells in the latter case, while it would be quite difficult to do it when $Z_0 = 50\,\Omega$, as IL are already quite high and would even increase when cascading more stages.

As part of the fabrication process, it might be sometimes preferred to replace TLs by lumped components (e.g., at low frequencies, due to the extremely lengthy TLs). For this reason, it is important to note that thanks to the conscientiously-designed short TLs, it is also possible to substitute the TL sections by LC structures, according to the equivalent circuit of a lossless TL shown in Fig. 5.3b. The design frequency f, the phase velocity v_{p} and the characteristic impedance Z_0 fully define the per-unit-length capacitance and inductance of the TL. For the proposed design with a TL of length $\lambda/20$ and $Z_0 = 15\,\Omega$ at $f = 3$ GHz, the values of the equivalent inductor and capacitor are: $C_{\text{line}} = 1.13$ pF and $L_{\text{line}} = 0.25$ nH. The predicted results are also depicted in Figs. 5.8 and 5.9 (dotted-dashed lines), showing that both TL- and lumped element-based implementations of the phase shifter are feasible.

It should be highlighted that the MIG technology considered here is not optimized for the targeted application, that requires a high tunability of the graphene C_{q}. This is the main cause of the low $\Delta\phi_{21}$ achieved. However, for the sake of stressing the usefulness

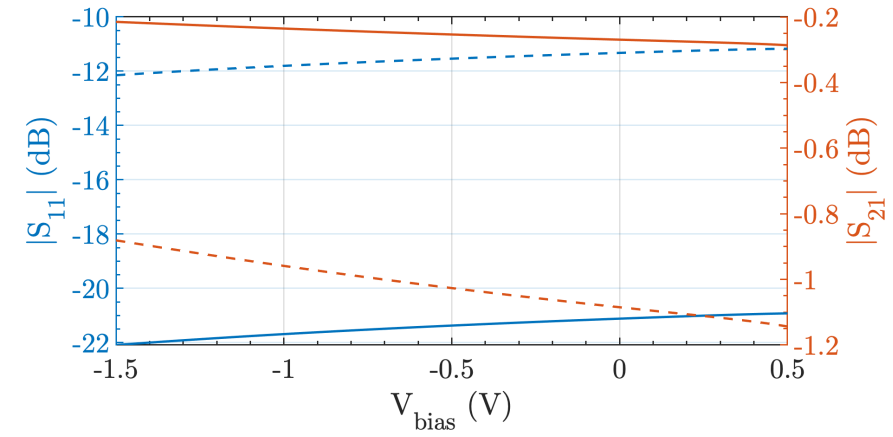


Figure 5.6.: $|S_{11}|$ (left axis) and $|S_{21}|$ (right axis) versus V_{bias}. Solid lines state for the case where $Z_0 = 15\,\Omega$; while dashed lines correspond to $Z_0 = 50\,\Omega$.

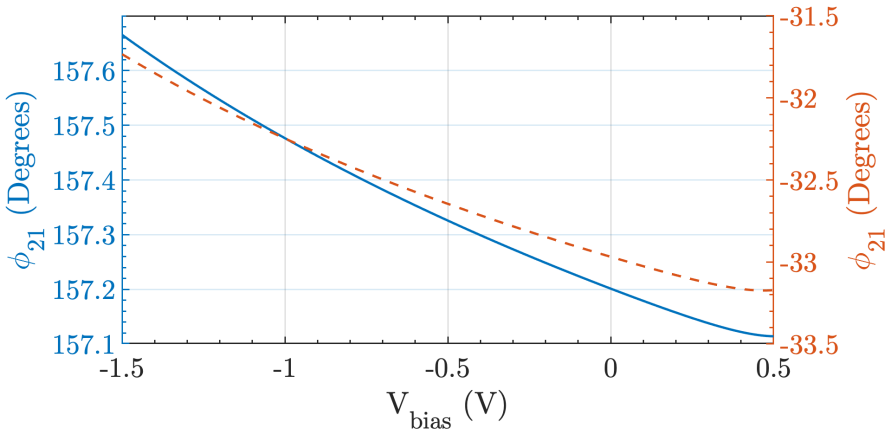


Figure 5.7.: Bias tunability of ϕ_{21} for $Z_0 = 15\,\Omega$ (solid line, left axis); and $Z_0 = 50\,\Omega$. (dashed line, right axis)

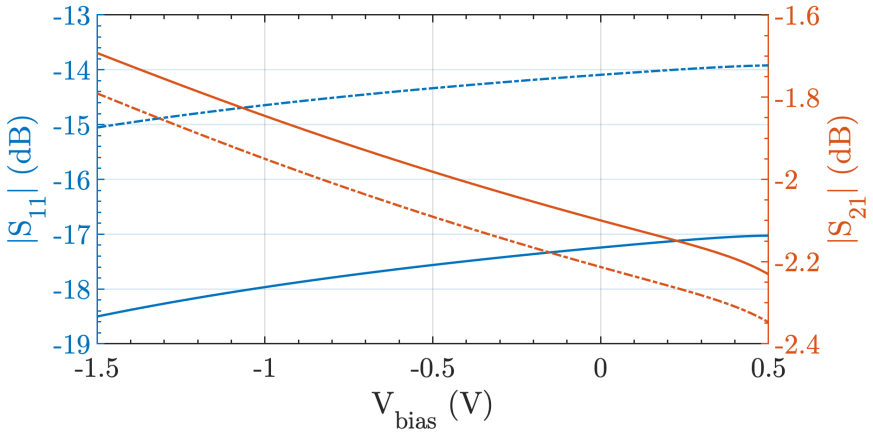


Figure 5.8.: V_{bias} dependence of $|S_{11}|$ (left axis) and $|S_{21}|$ (right axis) for a cascade of 10 unit-cells as the one shown in Fig. 5.1, with $Z_0 = 15\,\Omega$. Solid lines state for the TL design while dotted-dashed lines correspond to the LC equivalent design.

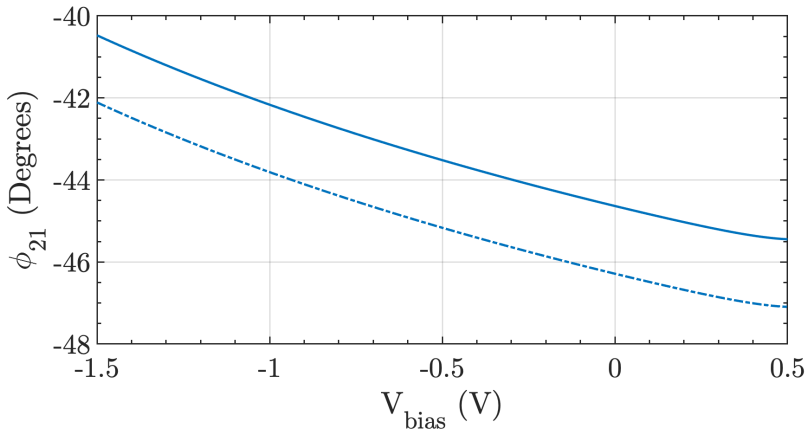


Figure 5.9.: Bias tunability of ϕ_{21} for a cascade of 10 unit-cells, with $Z_0 = 15\,\Omega$. Solid lines state for the TL design while dotted-dashed lines correspond to the LC equivalent design.

of the proposed methodology, we have considered a reduced residual charge density technology where, e.g., $Q_0' = Q_0/3$ (the corresponding capacitance variation for this case was depicted in Fig. 5.4). In such a case, the performance of a 10 cascaded unit-cells is predicted to be IL = 1.29 dB, RL = 20.14 dB, $\Delta\phi_{21} = 24.09°$, bringing to light the potential of using optimized MIG diodes for future RF phase shifters aiming for both rigid and flexible substrates [247].

Still, the resulting value for $\Delta\phi_{21}$ is not as high as a circuit designer could expect for a potential application, and alternative methods need to be explored.

5.3. Theoretical analysis of the structures

Now that we have analyzed the behavior and practical implementation of a single unit-cell, we suggest a different way of facing the problem. Instead of focusing on optimizing one single unit-cell in terms of phase shift and ILs so that we can afterwards cascade them, we focus on the theoretical analysis of a periodic structure with n cascaded unit-cells.

Therefore, we now want to calculate the S parameters of the concatenation of n unit-cells. For that purpose, we start by defining the transmission matrix ($\boldsymbol{T}$) of the unit-cell in Fig. 5.1 (note that for a matter of conveniente, in this analysis we will use T parameters instead of $ABCD$). Assuming lossless TL sections (i.e., $\alpha = 0$), we can write:

$$\boldsymbol{T} = \begin{bmatrix} \left(1+\frac{y}{2}\right)e^{j\beta d} & -\frac{y}{2} \\ -\frac{y}{2} & \left(1-\frac{y}{2}\right)e^{-j\beta d} \end{bmatrix} \tag{5.7}$$

where $y = Y/Y_0$ is the admittance of the shunt element (Y) normalized to the characteristic admittance of the TL sections (Y_0); β is the phase constant of the TL, and d is the physical length of the TL sections of each unit-cell. In a periodic structure with n identical unit-cells, the T-matrix of the cascade can be evaluated as $\boldsymbol{T}^n$, where the n-th power of the T-matrix can be written as [237]:

$$\boldsymbol{T}^n = U_{n-1}(\nu)\boldsymbol{T} - U_{n-2}(\nu)\boldsymbol{I} \tag{5.8}$$

with U_n the second kind Tschebysheff polynomial of order n, $\boldsymbol{I}$ the identity matrix and ν:

$$\nu = \frac{T_{11} + T_{22}}{2} \tag{5.9}$$

where T_{ij} stands for the (i,j) element of $\boldsymbol{T}$. Assuming that the shunt admittance of the unit-cell of Fig. 5.1 is purely imaginary, $y = jb$, ν can be evaluated using eqs. (5.9) and (5.7) as:

$$\nu = \cos(\beta d) - \frac{b}{2}\sin(\beta d) \tag{5.10}$$

so that $\nu \in \mathbb{R}$.

Thus, the T-matrix of a periodic structure formed by the concatenation of n unit-cells can be written as:

$$\boldsymbol{T}^n = \begin{bmatrix} T_{11,n} & T_{12,n} \\ T_{21,n} & T_{22,n} \end{bmatrix} = \begin{bmatrix} U_{n-1}T_{11} - U_{n-2} & U_{n-1}T_{12} \\ U_{n-1}T_{21} & U_{n-1}T_{22} - U_{n-2} \end{bmatrix} \tag{5.11}$$

where we have introduced the notation $T_{ij,n}$ for the (i,j) matrix element of $\boldsymbol{T}^n$. The conversion matrix between T and S-parameters [119] enables the evaluation of the periodic structure performance in terms of its S-parameters:

$$\boldsymbol{S}_n = \begin{bmatrix} S_{11,n} & S_{12,n} \\ S_{21,n} & S_{22,n} \end{bmatrix} = \begin{bmatrix} \frac{T_{21,n}}{T_{11,n}} & \frac{\Delta_{T^n}}{T_{11,n}} \\ \frac{1}{T_{11,n}} & -\frac{T_{12,n}}{T_{11,n}} \end{bmatrix} \tag{5.12}$$

where $\Delta_{T^n} = T_{11,n}T_{22,n} - T_{12,n}T_{21,n}$. It is worth to note that $\boldsymbol{S}_n$ is the S-matrix of the whole periodic structure with n sections, and $S_{ij,n}$ its corresponding (i,j) element.

Then, in order to find the transmission peaks, i.e. the points where the whole available power is transmitted from the input to the output, it is necessary to impose $|S_{21,n}| = 1$. From Eq. (5.12), this is achieved if and only if $|T_{11,n}| = 1$, or equivalently $|U_{n-1}T_{11} - U_{n-2}| = 1$. The resulting equation becomes impractical. In order to exemplify this assessment, we propose to address a periodic structure of $n = 3$ unit-cells. We calculate $\boldsymbol{T}^3$ as:

$$\boldsymbol{T}^3 = U_2(\nu)\boldsymbol{T} + U_1(\nu)\boldsymbol{I} = \begin{bmatrix} (4\nu^2-1)T_{11} - 2\nu & (4\nu^2-1)T_{12} \\ (4\nu^2-1)T_{21} & (4\nu^2-1)T_{22} - 2\nu \end{bmatrix}$$

where $U_1(\nu)$ and $U_2(\nu)$ are determined by using Eq. (5.10) and the recursive formula $U_{n+1}(\nu) = 2\nu U_n(\nu) - U_{n-1}(\nu)$:

$$U_1(\nu) = 2\left(\cos(\beta d) - \frac{b}{2}\sin(\beta d)\right) U_2(\nu) = 4\nu^2 - 1 = 4\left(\cos(\beta d) - \frac{b}{2}\sin(\beta d)\right)^2 - 1$$

To calculate the $S_{21,3}$ parameter, we would need to evaluate $T_{11,3} = (4\nu^2-1)T_{11} - 2\nu$ and we would still have to calculate the inverse of the expression and further simplify it to be able to obtain the magnitude and argument of S_{21}. As abovementioned, even in this simple scenario with $n = 3$, the resulting solution is impractical.

Fortunately, a lossless passive linear network as the one in Fig. 5.1 complies with the condition $|S_{21,n}| = 1 \Leftrightarrow |S_{11,n}| = 0$. From Eq. (5.12), $S_{11,n} = T_{21,n}/T_{11,n}$, so that $|T_{21,n}| = 0$ is the only way of accomplishing $|S_{11,n}| = 0$. Thus the transmission peaks satisfy:

$$|T_{21,n}| = |U_{n-1}T_{21}| = 0 \tag{5.13}$$

whose solutions imply: (i) $|T_{21}| = 0 \Leftrightarrow b = 0$, i.e. the susceptance is zero, which is discarded as it is a non practical case; (ii) $|U_{n-1}(\nu)| = 0$, i.e. the zeros of the Tschebysheff polynomial of order $n-1$, whose position is determined as [248]:

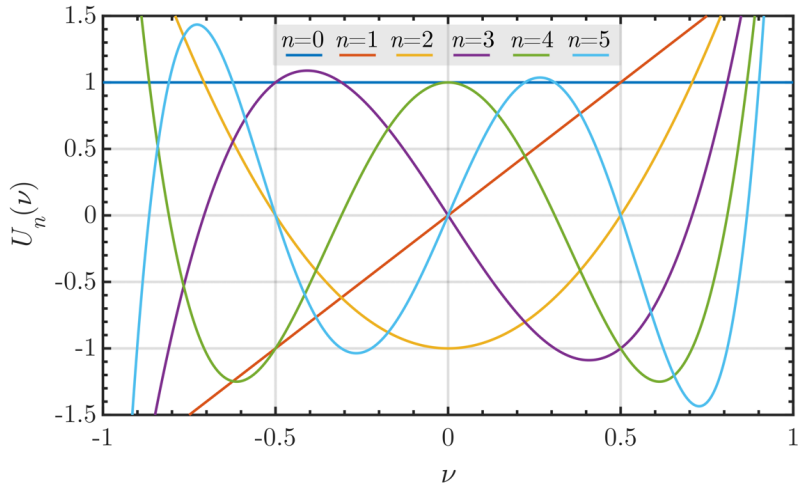


Figure 5.10.: Evaluation of the Tschebysheff polynomials of the second kind of order $n = 0, 1, ..., 5$.

$$\nu_k^{n-1} = \cos\left(\frac{\pi k}{n}\right) \tag{5.14}$$

with ν_k^{n-1} denoting the k-th zero of the second kind Tschebysheff polynomial of order $n-1$, and $k = [1, n-1]$ with $k \in \mathbb{Z}$.

From the properties of a passive linear microwave network (and assuming $T_{11,n}$ is finite and $T_{21,n} \neq 0$), we can observe that:

$$|U_{n-1}| = 0 \Leftrightarrow |T_{21,n}| = 0 \Leftrightarrow |S_{11,n}| = 0 \Leftrightarrow \\ \Leftrightarrow |S_{21,n}| = 1 \Leftrightarrow |T_{11,n}| = 1 \Leftrightarrow |U_{n-2}| = 1 \tag{5.15}$$

but indeed, a known property is that, at the zeros of the $n-1$ Tschebysheff polynomial, $|U_{n-1}(\nu = \nu_k^{n-1})| = 0$, the $n-2$ Tschebysheff polynomial satisfies $|U_{n-2}(\nu = \nu_k^{n-1})| = 1$ [248]. If we evaluate the recursive formula of the second kind Tschebysheff polynomials at $\nu = \nu_k^n$, we can derive by using this property:

$$|U_{n+1}(\nu = \nu_k^n)| = |U_{n-1}(\nu = \nu_k^n)| = 1, \forall k = \{[1, n] \in \mathbb{Z}\} \tag{5.16}$$

This is, the Tschebysheff polynomials of the second kind of order $n-1$ and $n+1$, are 1 in magnitude at the zeros of the Tschebysheff polynomials of order n, namely $|U_{n+1}(\nu = \nu_k^n)| = |U_{n-1}(\nu = \nu_k^n)| = 1$, while $|U_n(\nu = \nu_k^n)| = 0$. This can be observed in Fig. 5.10, where $|U_n(\nu)|$ versus ν is shown. For example, at the zero of $|U_2|$, i.e., $|U_2(\nu = 0.5)| = 0$, we can observe that $|U_1(\nu = 0.5)| = 1$ and $|U_3(\nu = 0.5)| = 1$.

Thus, for a periodic structure based on a lossless passive linear network with n unit-cells, $|S_{11,n}| = 0$ and $|S_{21,n}| = 1$ if and only if $|U_{n-1}(\nu)| = 0$, i.e. for $\nu = \nu_k^{n-1}$ as

defined by eq. (5.14). The number of transmission peaks for n unit-cells is $N = n - 1$, in addition to the zero produced by the case $b = 0$, as it was indeed experimentally observed in [238].

We can thus determine the conditions that are fulfilled at the transmission peaks by relating eqs. (5.10) and (5.14):

$$\nu_k^{n-1} = \cos(\beta d) - \frac{b}{2}\sin(\beta d) = \cos\left(\frac{\pi k}{n}\right) \tag{5.17}$$

Solving (5.17) for b we obtain:

$$b_k = \frac{2}{\sin(\beta d)}\left[\cos(\beta d) - \cos\left(\frac{\pi k}{n}\right)\right] \tag{5.18}$$

where the notation b_k is introduced for the k-th solution of the equation.

Equation (5.18) provides an explicit expression to calculate the values of b_k that correspond to the transmission peaks ($|S_{21,n}| = 1$ and $|S_{11,n}| = 0$) of the lossless periodic structure. In other words, the proposed expression constitutes the design equation for a periodic structure with an arbitrary number n of unit-cells, and determines the conditions for the optimum transmission peaks in terms of the different parameters of the unit-cell (e.g. TL length and susceptance). It is worth noting that while changing the structure of the unit-cell will modify ν, the design equations are general for any unit-cell (provided it is lossless, passive and linear) and can thus be exploited by straightforwardly recalculating ν of the new unit-cell and using it in eq. (5.17).

5.4. System Design and Fabrication

5.4.1. Inductive or capacitive susceptance, b

Equation (5.18) allows both positive- and negative-valued solutions of b_k, which correspond to a capacitive or inductive-like susceptance, respectively. For our design, we have opted for a physical implementation of the periodic TL based on a variable capacitor, and thus have to analyze under which particular circumstances would b_k be positive. Assuming that the length of each TL section will be lower than $\lambda/4$, then $\beta d \leq \pi/2$, making $\cos(\beta d)$ and $\sin(\beta d)$ non-negative. Under this assumption, b_k will be positive when the following relation is accomplished:

$$\cos\left(\frac{\pi k}{n}\right) < \cos(\beta d) \tag{5.19}$$

Since in the first quadrant ($\beta d < \pi/2$) the cosine is a monotonically decreasing function, eq. (5.19) implies:

$$\beta d < \frac{\pi k}{n} \Leftrightarrow d < \frac{k}{2n}\lambda \tag{5.20}$$

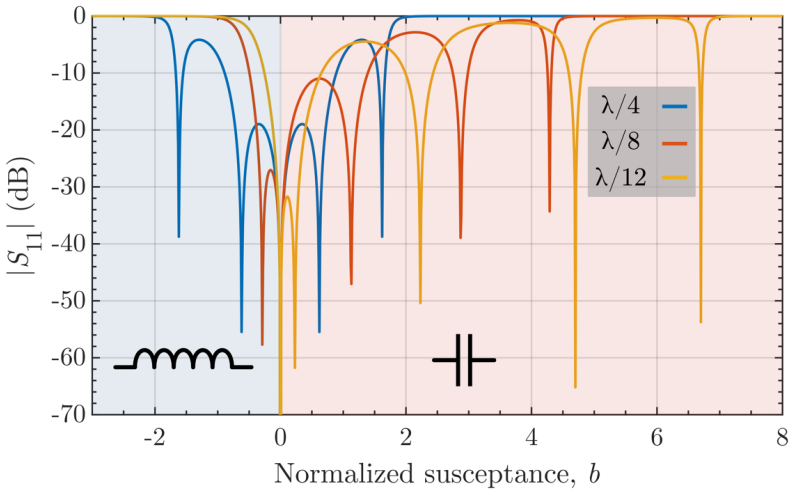


Figure 5.11.: $|S_{11}|$ (dB) parameter of a periodic structure with $n = 5$ versus the normalized susceptance of the periodic loading, b, for different values of the electrical length of the TL sections: $\lambda/4$, $\lambda/8$, $\lambda/12$. Only when $d = \lambda/12$ (i.e., $d < \lambda/10$) the four expected zeros, b_k, are positive.

From eq. (5.20) it can be concluded that the most restrictive situation occurs for $k = 1$; in this case, the condition to guarantee $b > 0$ and thus that the susceptance corresponds to a capacitance reads as:

$$d < \frac{\lambda}{2n} \tag{5.21}$$

In other words, the total number of unit-cells of the periodic structure sets a limit for the length of the TLs of each unit-cell in order to guarantee positive values for b_k. To gain further insight, we have simulated a periodic structure as the one in Fig. 5.1 with $n = 5$ and $f = 3$ GHz, making use of the commercial circuit simulator ADS. For this particular case, eq. (5.21) imposes the limit $d < \lambda/10$. Fig. 5.11 shows the simulation results in terms of the $|S_{11}|$ parameter for different values of the electrical length, $d = \lambda/4$, $\lambda/8$, $\lambda/12$. It can be observed that, according to eq. (5.21), the case that satisfies $d < \lambda/10$ shows the four expected zeros for positive values of b. Although physically meaningless, $b = 0$ is always a zero as discussed in eq. (5.13).

5.4.2. Fully locating the transmission peaks

Once the susceptance $b > 0$ is physically realized in the form of a variable capacitor, i.e., $b = Z_0\omega C$, with $\omega = 2\pi f$, the value of b depends on the capacitance of the varactor and on the frequency. Even though both entail a proportional change on b, sweeping f does not only change b, but it concomitantly modifies the electrical length of the TLs. As a consequence, changing f will not produce the same result as changing C, and the

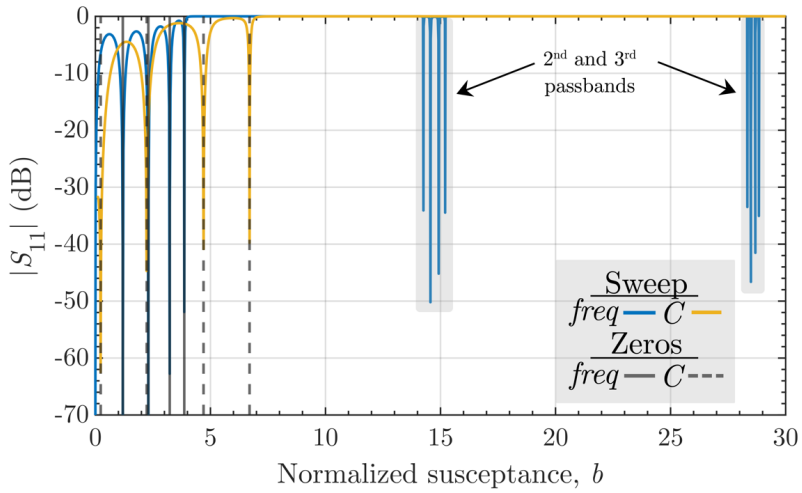


Figure 5.12.: Simulated $|S_{11}|$ (dB) as a function of b, for a periodic structure with $n = 5$ and $d = \lambda/12 = 8.3\,\text{mm}$ at $f = 3\,\text{GHz}$, considering $v_p = c$. A frequency sweep with constant capacitance $C_{\text{var}} = 2.5\,\text{pF}$ (blue line) and a capacitance sweep with constant frequency $f = 3$ GHz (yellow line) have been considered. Vertical lines correspond to theoretical values for the zeros of the $|S_{11}|$ obtained from eq. (5.22). The zeros on the second and third passbands on the frequency sweep are not shown due to visualization purposes.

frequency position of the transmission peaks, corresponding to the zeros of $|S_{11}|$ in Fig. 5.11, cannot be directly inferred from the values of b.

In order to predict these frequency zeros, from eq. (5.17) we can write:

$$\cos\left(\frac{2\pi d}{v_p}f\right) - Z_0\pi f C \sin\left(\frac{2\pi d}{v_p}f\right) = \cos\left(\frac{\pi k}{n}\right) \tag{5.22}$$

where v_p is the propagation speed: $v_p = c/\sqrt{\epsilon_{\text{eff}}}$; and ϵ_{eff} is the effective dielectric constant of the media. Equation (5.22) can be indeed solved to obtain both, the frequency and the capacitance transmission peaks by fixing either the capacitance or the frequency, respectively.

In addition to the simulation, eq. (5.22) has been solved for f (fixing C_{var}) and for C_{var} (fixing f) in order to reveal the theoretical frequency and capacitance positions of the zeros of the structure. The results, depicted as vertical lines in Fig. 5.12, coincide with the simulated zeros of $|S_{11}|$, demonstrating the ability of eq. (5.22) to predict the position of the zeros as much when changing f as when changing b. Equation (5.22) can be thus deemed as the main design equation of the structures.

5.4.3. Fabrication and measurement setup

To experimentally validate the previous design, we have fabricated a periodic structure with five unit-cells ($n = 5$) in microstrip technology (Fig. 5.13), using an FR4 substrate

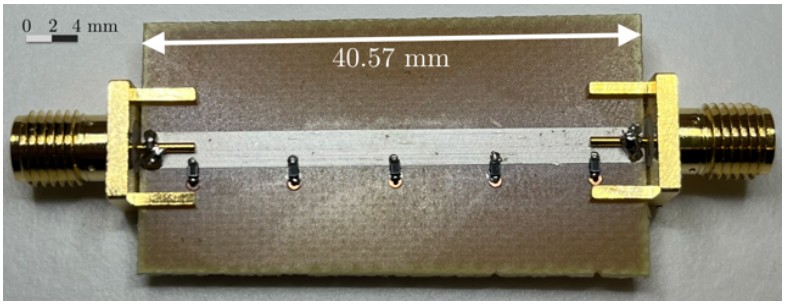


Figure 5.13.: Fabricated periodic structure with $n = 5$ in microstrip technology.

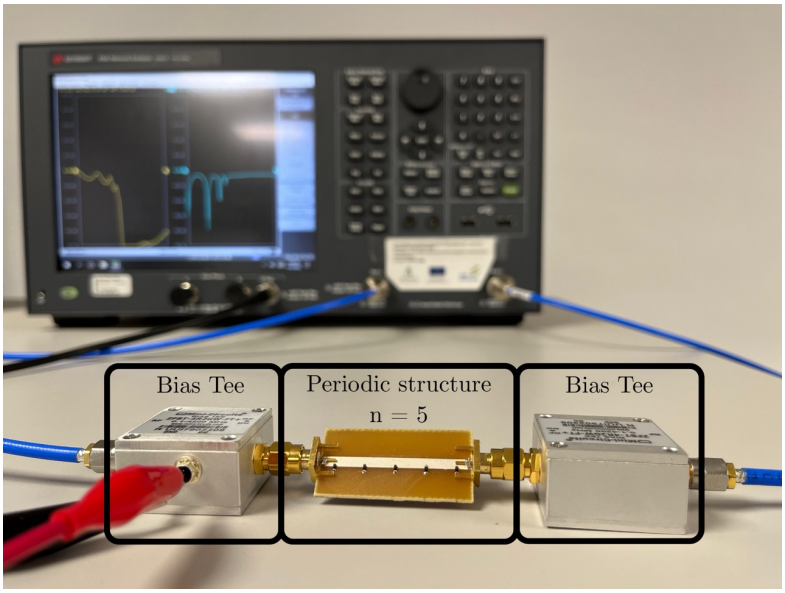
fabricated by C.I.F.™ [249] with a dielectric constant of $\epsilon_r = 4.7$ and a dielectric thickness of $H = 1.6\,\text{mm}$, where the back conductor is made of a $35\,\mu\text{m}$ copper layer while the top conductor is made of a curated conductive silver ink fabricated by Voltera™ with a resistivity of $1.27\text{x}10^{-7}\,\Omega\text{m}$ [250]. For the vias, copper rivets have been used, while the Infineon™ BBY55-02V varactor is used as the variable capacitor [251]. For input and output connections, two SMA connectors have been welded to the input and output ports of the structure.

The measurement setup consists of the Keysight™ ENA 5061B and two ZFBT-4R2GW-FT+ Mini-Circuits™ bias tees. The DC output of the ENA was used for biasing. The overall measurement setup is shown in Fig. 5.14a. Besides, the Impedance Analyzer Keysight™ E4990A, with the SMD component test fixture Keysight™ 16034E (Fig. 5.14b), was used to characterize the C-V_R curve of the commercial varactors up to a maximum frequency of $40\,\text{MHz}$, with V_R being the reverse voltage applied.

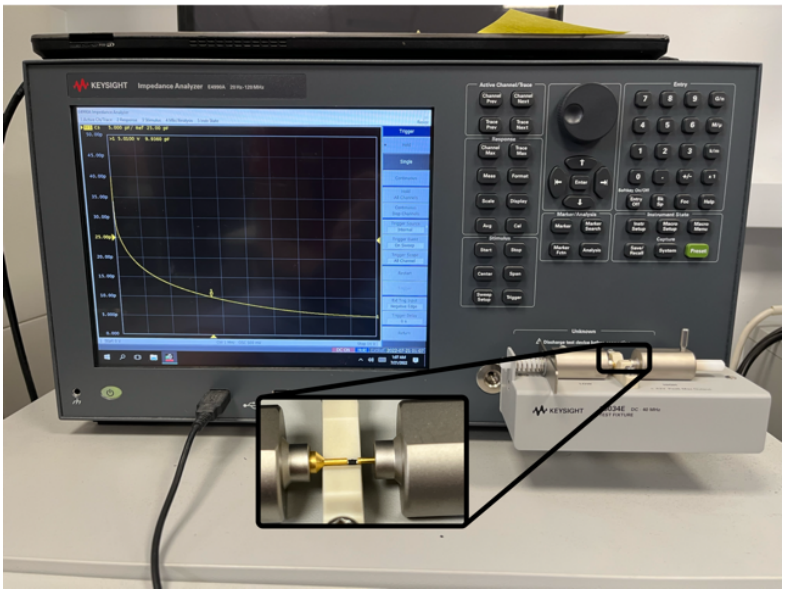
5.5. Results

The system designed and fabricated in this work, i.e. a microwave periodic structure formed by loaded TLs, relies on microstrip technology and surface mounted commercial varactors, which demands to carefully characterize the eventual parasitics that could affect the intrinsic behavior of the circuit, especially at high frequencies. This limitation of the employed technology is not intrinsic to the here proposed theoretical analysis and design procedure, which could be fairly exploited in integrated circuit (IC) technology, but becomes relevant in the present implementation at high frequencies.

In particular, we identify two main extrinsic effects that must be de-embedded for a fair comparison with the theory. The first one is produced by the parasitic elements inherent to the commercial varactors. Due to the packaging, some parasitic series and/or shunt elements need to be considered in the form of extrinsic inductors, resistors or capacitors for a proper modeling of the actual varactor. Even though these parasitic elements are commonly disregarded, their effect — particularly at high frequencies — is not negligible, as will be evinced later. The second extrinsic effect has its origin on the ground vias. In microstrip technology, grounding is usually achieved by connecting the top and bottom sides of the printed circuit board (PCB) with conductive vias. These



(a)



(b)

Figure 5.14.: a) Keysight™ ENA 5061B and additional circuitry employed for prototype RF measurements, and b) Keysight™ E4990A impedance analyzer along with the SMD component fixture Keysight™ 16034E for SMD component characterization.

vias, whose length equals the thickness of the board, add a section of TL whose electrical length cannot be neglected as the frequency increases.

Due to these parasitics, the impedance of the varactors changes and so does their capacitance. In order to assess this effect and at the same time to characterize the varactors, in Fig. 5.16 the equivalent varactor capacitance ($C_{\rm eq}$) versus the applied reverse bias ($V_{\rm R}$) curves obtained from three different sources are shown: (i) from the manufacturer datasheet at 1 MHz (blue dotted line); (ii) from the experimental measurements carried out with the impedance analyzer at 1 MHz and 40 MHz (blue and red dashed lines, respectively); and (iii) from circuit simulations performed with ADS™ of the equivalent circuit that includes the parasitics provided by the manufacturer, shown in the inset of Fig. 5.19, at 1 MHz, 40 MHz and 730 MHz (blue, red and yellow solid lines, respectively). Two conclusions can be extracted from this Figure: (i) as frequency increases, the equivalent capacitance of the varactors ($C_{\rm eq}$) is higher than their reported variable capacitance ($C_{\rm var}$), highlighting the crucial role that the parasitics play as frequency increases, and only at low frequencies $C_{\rm eq} = C_{\rm var}$; and (ii) the packaging parasitics provided by the manufacturer do not match the measured ones, as can be seen at the $f = 40$ MHz curve, where the measured equivalent capacitance is higher than the simulated one (which is still very close to the 1 MHz curves). This mismatch increases as the applied reverse voltage is reduced (i.e., as $C_{\rm var}$ is bigger). So as to account for the effects of the parasitics and with the aim of making a fair comparison between measurements and simulations, a de-embedding procedure that allows for the transformation of the equivalent capacitance $C_{\rm eq}$ to the actual varactor capacitance $C_{\rm var}$ is implemented by using:

$$C_{\rm var} = \frac{C_2 - C_{\rm eq} + C_2 C_{\rm eq}(L_1 + L_3)\omega^2}{\omega^2[C_2 L_2 - C_{\rm eq} L_{\rm t} + C_2 C_{\rm eq} L_2 (L_1 + L_3)\omega^2] - 1} \tag{5.23}$$

where $L_{\rm t} = L_1 + L_2 + L_3$, and the elements L_1, L_2, L_3, $C_{\rm var}$ and C_2 are shown in the inset of Fig. 5.19, with their values provided by the manufacturer [252]. Hence, due to their above-mentioned underestimation, a certain deviation of the simulated with respect to the experimental data is expected, especially for low $V_{\rm R}$ (high $C_{\rm var}$) and high f.

For a deeper understanding of the considerable impact that the packaging and the ground vias has on the circuit performance, Fig. 5.15 shows a comparison between the outcome of three different situations: (i) the equivalent circuit shown in Fig. 5.19 (dotted lines); (ii) the circuit without considering the ground vias elements (dashed lines); and (iii) the circuit without considering the ground vias nor the parasitic elements (solid lines). It can be observed the great impact that these two factors due to the technology used for our demonstrator have on the final evolution of the parameters, shifting considerably the position of the transmission peaks along the frequency axis, as well as changing their magnitude and distance. It can be thus concluded that parasitics must be taken into account for a proper circuit design.

Now, we proceed to evaluate the goodness of the proposed theoretical analysis and system design by comparing (see Figs. 5.17 and 5.18): (i) the simulation of the periodic structure depicted in Fig. 5.19 making use of ADS (solid lines), (ii) the experimental

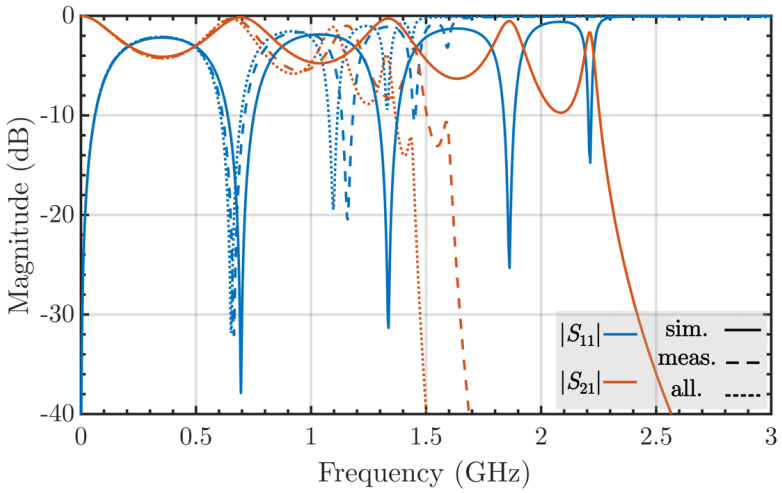


Figure 5.15.: $|S_{11}|$ and $|S_{21}|$ as a function of frequency for a periodic structure with $n = 5$ and $d = \lambda/12$ at $f = 3\,\text{GHz}$ with $\epsilon_r = 4.7$, under different simulation scenarios: (i) taking parasitic elements and ground vias into account (solid lines); (ii) taking only parasitic elements into account (dashed lines); (iii) neglecting both effects (dotted lines). The theoretically expected position of the transmission peaks based on the ideal scenario are shown with grey vertical lines.

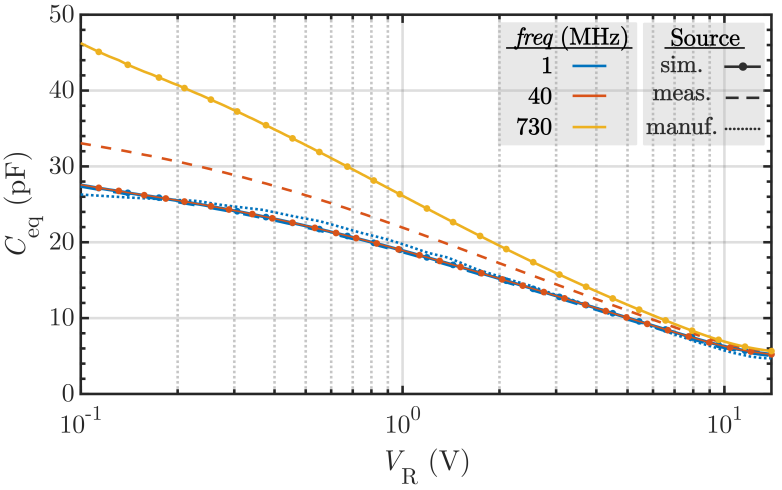


Figure 5.16.: BBY55-02V variable capacitor characterization. The measurements performed with the impedance analyzer are represented by dashed lines; with solid lines, the simulation results are shown; and the dotted curve is the one provided by the manufacturer.

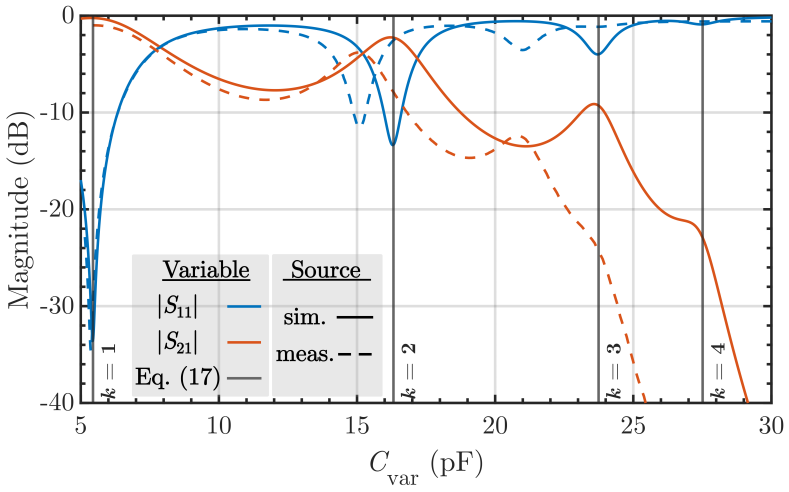


Figure 5.17.: $|S_{11}|$ and $|S_{21}|$ (dBs) as a function of the capacitance of the varactors (C_{var}), for a frequency value of 730 MHz. A voltage sweep from 0 to 14 V is performed. The solid lines represent the circuit simulation results, the dashed lines represent the experimental measurements. The vertical lines correspond to the theoretically calculated values for the transmission peaks.

measurements of the circuit (dashed line), and (iii) the theoretical transmission peaks positions calculated with eq. (5.22) (grey vertical lines). In particular, Fig. 5.17 depicts $|S_{11}|$ and $|S_{21}|$ in decibels as a function of the varactor capacitance C_{var} for $f = 730\,\text{MHz}$, which is the frequency that allows the exhibition of the four expected zeros when the voltage is swept from 0 to 14 V. Fig. 5.18 shows $|S_{11}|$ and $|S_{21}|$ in decibels as a function of the frequency for a reverse bias $V_{\text{R}} = 10\,\text{V}$, that corresponds with a capacitance value of the varactors of $C_{\text{var}} = 7\,\text{pF}$. As mentioned earlier, in Fig. 5.17 the x-axis has been de-embedded making use of eq. (5.23), in addition to that, the effect of the vias connected to the ground has been accounted as much in the simulations, by using the ADS element to that effect, as in the de-embedding, by following the same theoretical approach as in the ADS element [253].

Figures 5.17 and 5.18 highlight the good agreement achieved between circuit simulation and experimental measurements as well as with the theoretically predicted transmission peaks. In particular, in Fig. 5.17, for $C_{\text{var}} < 12\,\text{pF}$, the agreement is excellent. However, due to the analyzed underestimation of the parasitics, for $C_{\text{var}} > 12\,\text{pF}$, the predicted behavior is shifted towards higher capacitive values. In contrast, in Fig. 5.18, for $C_{\text{var}} = 7\,\text{pF}$ the agreement is excellent as the frequency has a low impact on the equivalent capacitance for $C_{\text{var}} < 12\,\text{pF}$, as Fig. 5.16 shows. Figures 5.17 and 5.18 clearly show the $N = n - 1 = 4$ transmission peaks (in addition to the transmission peak at $b = 0$).

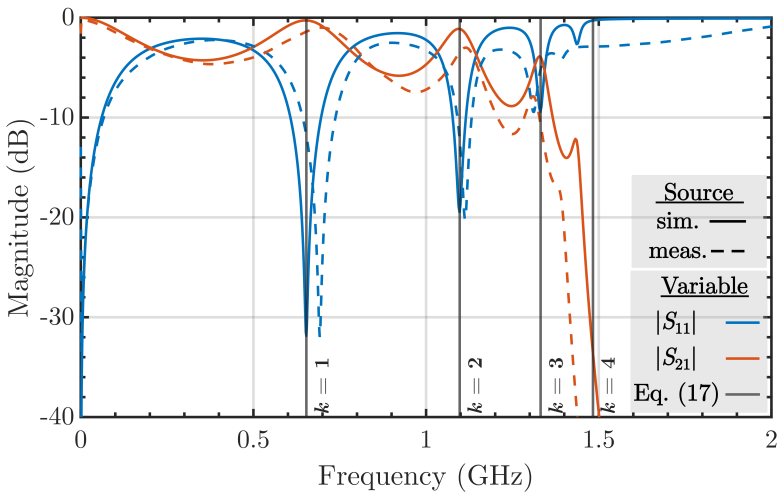


Figure 5.18.: $|S_{11}|$ and $|S_{21}|$ (dBs) as a function of the frequency for a reverse bias of $V_{\mathrm{R}} = 10\,\mathrm{V}$, that corresponds with a $C_{\mathrm{var}} = 7\,\mathrm{pF}$. The solid lines represent the simulation results, and the dashed lines represent the experimental measurements. The vertical lines correspond to the theoretically calculated values for the transmission peaks.

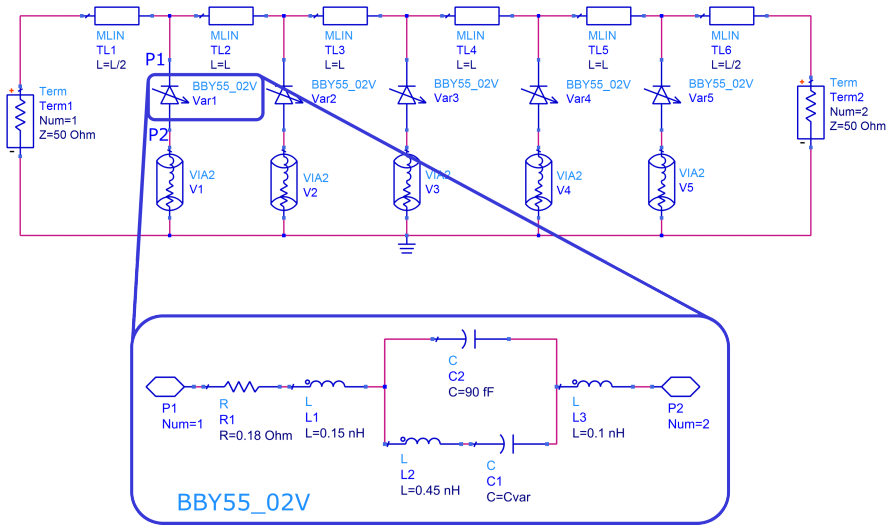


Figure 5.19.: Simulation schematic of the periodic structure considering the parasitic elements and the ground vias. Inset: BBY55-02V equivalent circuit showing the parasitic elements provided by the manufacturer.

5.6. Analysis of the phase behavior

5.6.1. Proof of the need for a compact explicit expression of U_n

Following with the discussion of section 5.3, and in order to design not only at the points where the power of the signal is well transmitted, but also to take into consideration the effect that the periodic structure has on the phase of the signal, it is necessary to find an explicit expression for the second kind Tschebysheff polynomials, as will be now justified.

Let us first analyze what occurs to the phase of a signal which is travelling through a periodic structure with n unit-cells. We can calculate the transmission parameter of the structure, S_{21}, as:

$$S_{21,n} = \frac{1}{T_{11,n}} = \frac{1}{U_{n-1}(\nu)T_{11,n} - U_{n-2}(\nu)} \tag{5.24}$$

As we saw before, in the ν values where $|S_{11}| = 0$, i.e., $\nu = \nu_k^{n-1}$ (transmission points), $U_{n-1}(\nu) = 0$, and thus $S_{21} \in \mathbb{R}$ because $U_n(\nu) \in \mathbb{R}$. However, if we move from $\nu = \nu_k^{n-1}$, the condition $U_{n-1}(\nu) = 0$ is not satisfied, and as a consequence, $S_{21} \in \mathbb{C}$. This is, at the points where all the power is transmitted (the zeros of the structure), the phase is zero as S_{21} is real. However, as soon as we move away from these points, S_{21} becomes complex again and therefore, it provides a phase shift that needs to be evaluated.

In general, for any n value we have a complicated expression for the phase of the S_{21} parameter, as it depends on $U_{n-1}(\nu)$ and $U_{n-2}(\nu)$ whose complexity will increase with n:

$$\phi_{21}^n(\nu) = -\arg[U_{n-1}(\nu)T_{11,n} - U_{n-2}(\nu)] \tag{5.25}$$

Thus, an explicit expression for $U_n(\nu)$ needs to be achieved so that it allows to get an expression to directly evaluate ϕ_{21} for any n value.

5.6.2. S_{21} phase explicit expression: ϕ_{21}^n, and phase shift range trade-off

Equation (5.26) shows the expression of the phase of the S_{21} parameter for a n-unit-cells periodic structure. As can be seen, it depends on n, which is the number of concatenated structures, and on ν. For the obtention of this function we have used the explicit expression of $U_n(\nu)$ and set it inside eq. (5.25):

$$\phi_{21}^n(\nu) = \tan^{-1}\left[\frac{\sin(\beta d) + \frac{b}{2}\cos(\beta d)}{\frac{\sin[(n-1)\cos^{-1}(\nu)]}{\sin[n\cos^{-1}(\nu)]} - \nu}\right] = \tan^{-1}\left[\frac{\sin(\beta d) + \frac{b}{2}\cos(\beta d)}{\frac{\nu T_{n-1}(\nu) - T_n(\nu)}{T_{n-1}(\nu) - \nu T_n(\nu)} - \nu}\right] \tag{5.26}$$

with $T_n(\nu)$ the first kind Tschebysheff polynomial of order n.

We can see that ϕ_{21} depends on multiple variables, including the number of unit-cells or the susceptance. However, thinking on the circuit once it is fabricated, only the bias voltage can be modified, V_{bias}, which changes the value of C associated to the varactor, and is this change on C the one that produces a proportional change on b (and thus in ν), and eventually makes ϕ_{21}^n to change, producing a certain phase shift. However, at the same time this same change on b will move us away from the zeros of the $|S_{11}|$, i.e., from the transmission points, thus worsening power transmission. For this reason, the variation of b, Δb, will be a critical value, and a trade-off will need to be found between having a phase shift range as wide as possible but achieving a good power transmission at the same time.

Now that we are aware of the crucial role that b plays on the design, we would like to explore if there is a way to maximize the phase shift range minimizing insertion losses, i.e., the loss of transmitted power. In order to find out if there is a particular value of b that produces a higher variation of the phase when moving a certain amount away from b, we will now calculate the variation of ϕ_{21} with respect to b, $\partial\phi_{21}/\partial b$. This derivative together with the $|S_{11}|$ versus b are represented in Fig. 5.20 under the same x-axis for different n values. It can be observed that increasing either the value of b or the number of unit-cells, n, increases the rate at which the phase changes with respect to b, namely its derivative, meaning that in principle increasing the number of unit-cells or the value of b could be beneficial.

In addition, this representation allows us to notice that the maxima of the derivative of ϕ_{21} occur at the exact same b points as the zeros of the $|S_{11}|$. This is very reassuring for the designer, as designing at the best power transmission points values of b will also assure that the variation of the phase with respect to b at these points is maximum.

We have now observed that increasing n and/or b also increases the phase shift variation with respect to b, as Fig. 5.20 shows. However, what happens with the transmitted power? How does it change with n and b? In the following subsections we will discuss on that.

Study of the impact of increasing n on the phase shift range

In order to investigate the effect that increasing n has on the transmitted power, in Fig. 5.21 $|S_{11}|$ and ϕ_{21} are plotted versus b for different n values. If a certain value of RL, e.g. RL $>$ 10 dB, needs to be guaranteed, it can be seen that increasing the value of n does not help increasing the phase shift range, as represented by the arrows in the figure. We conclude thus that the total phase shift range that can be achieved with a periodic structure in order to keep a constant value of return losses (similarly $|S_{11}|$ value) is independent of the number of unit-cells. This means that, when designing a phase shifter using periodic structures, the same amount of phase shift can be attained independently of the number of unit-cells used. However, for a smaller value of n, the range of b that needs to be covered by the structure to get the same phase shift range of a structure with more unit-cells is bigger, which can indeed be a limiting factor for the varactor technology that will produce the susceptance change.

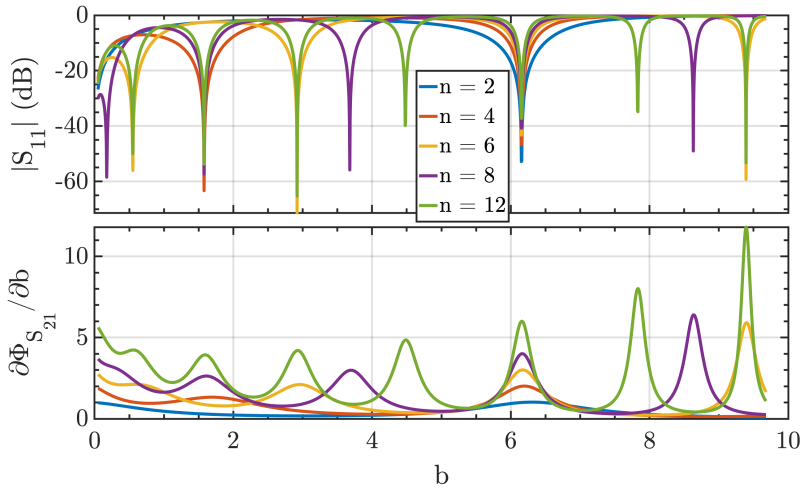


Figure 5.20.: $|S_{11}|$ and $\partial\phi_{21}/\partial b$ versus b. It can be seen that the zeros of the S_{11} occur at the same points as the maxima of the derivative of ϕ_{21} with respect to b.

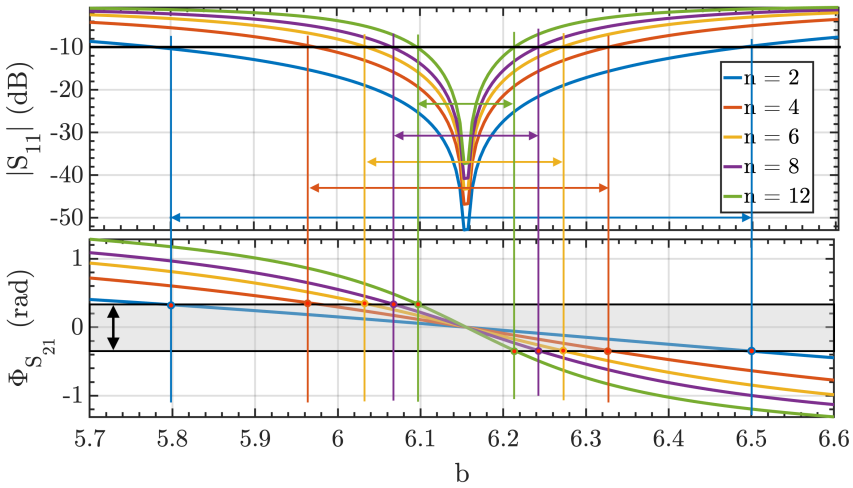


Figure 5.21.: $|S_{11}|$ and ϕ_{21} versus b. It can be seen that as n increases, the Δb value decreases if we want to keep $|S_{11}| < -10\,\text{dB}$, giving a phase shift range that is the same for every value of n.

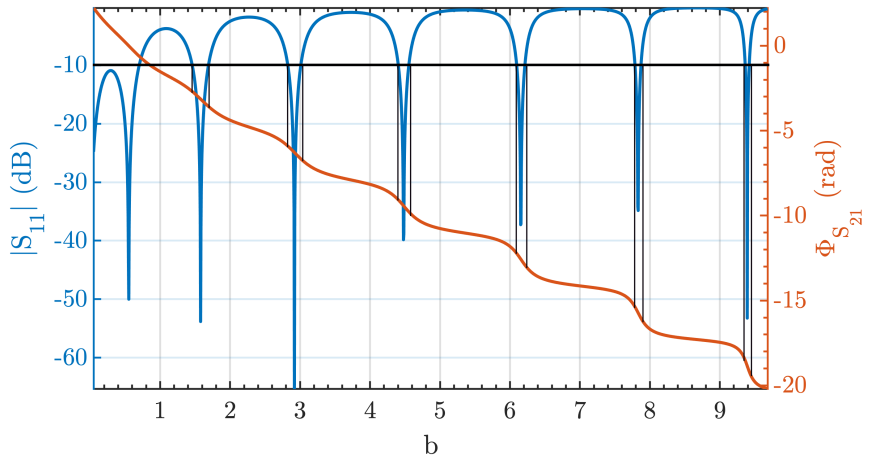


Figure 5.22.: $|S_{11}|$ (left) and ϕ_{21} (right) versus b for $n = 12$. A black horizontal line shows where the $|S_{11}| = -10\,\text{dB}$ value is, and several black vertical lines show the corresponding phase variation for the allowed Δb.

Study of the impact of Δb on the phase shift range

Now, we will evaluate the influence of b assuming a constant number of unit-cells, which could be another way of increasing the phase shift range as Fig. 5.20 showed.

Fig. 5.22 shows $|S_{11}|$ on the left axis, and ϕ_{21} on the right axis versus b for $n = 12$ (twelve unit-cells concatenated). A black horizontal line remarks the $|S_{11}| = -10\,\text{dB}$ value, and several black vertical lines show the corresponding phase variation for the allowed Δb. As can be observed, increasing the value of b does not increase the phase shift range. The reason is that even though the phase changes quicker as b increases, also Δb decreases with the rise of b, compensating one with each other.

5.6.3. Design of a phase shifter based on a metal-insulator-graphene diode

As an example of the design of a phase shifter using periodic structures, the design of a graphene-based phase shifter is shown here. For the design, a MIG diode is used as the varactor inside the unit-cell, using the simulation model presented in Chapter 3. The fabricated devices are two-finger MIG diodes with a size of $L_\text{g} \times W_\text{g} = 4\,\mu\text{m} \times 70\,\mu\text{m}$, a 6 nm layer of TiO_2 as insulator, and Ti and Ni for the bottom and top contacts, respectively. The devices used for this fitting were fabricated following the fabrication process described in Chapter 3 but in a previous run. The simulation model has been adjusted to fit the measurements of the fabricated devices, and their final technology parameters are shown in Table 5.2. Figure 5.23 shows the results from the adjustment, comparing the measured and simulated $C - V$ curve, which is the main curve of interest for the phase shifter design.

Parameter	Value	Parameter	Value
L_g	4 µm	W_{Ti}	4.33 eV
W_g	70 µm	W_{Ni}	5.05 eV
t_{ox}	6 nm	W_{Gr}	4.50 eV
ϵ_r	11.85	Q_o	31.40 mC/m^2

Table 5.2.: Fitted parameters of the MIG simulation model. L_g and W_g are the device length and width, respectively; t_{ox} and ϵ_r are the oxide thickness and relative permittivity, respectively; W_{Ti}, W_{Ni} and W_{Gr} are the titanium, niquel and graphene work functions; and Q_o is the sum of the fixed charge, constant interface trapped charge and possible chemical doping of the device.

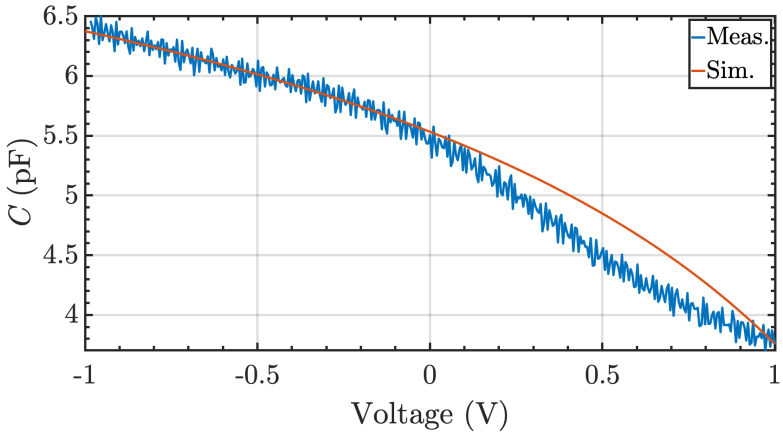


Figure 5.23.: Measured (blue) and simulated (red) capacitance versus the applied bias.

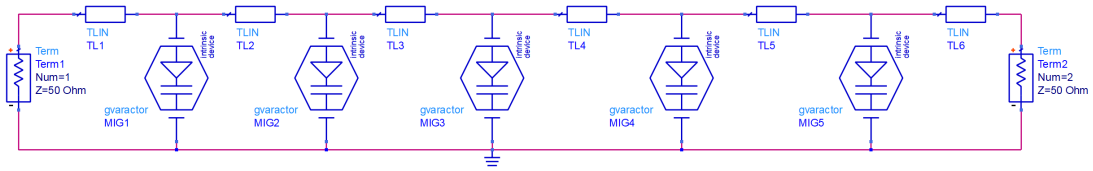


Figure 5.24.: Schematic of the simulated periodic structure with 5 unit-cells ($n = 5$).

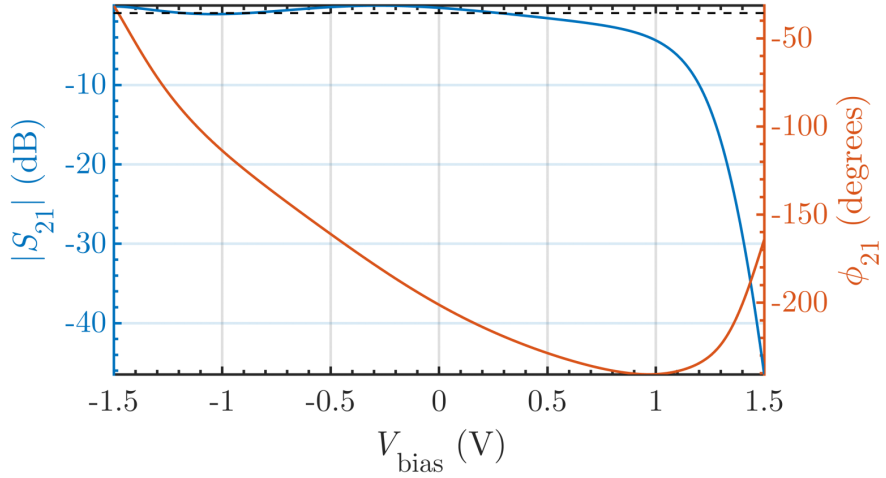


Figure 5.25.: $|S_{21}|$ and ϕ_{21} of the simulated periodic structure ($n = 5$) using the adjusted MIG model in ADS. The dashed line marks the -1 dB value and the considered bias range.

Once the simulation model has been adjusted, the periodic structure shown in Fig. 5.24 with 5 unit-cells ($n = 5$) has been designed and simulated at a frequency of $f = 1$ GHz. Ideal transmission lines have been considered, with a length of 0.18λ per unit-cell. The results show a total phase shift range of $\Delta\phi_{21} = 187.33°$ with insertion losses lower than 1 dB for the bias range $V_{\text{bias}} = [-1.5, 0.3]$ V, as shown in Fig. 5.25. The TL parameters of the unit-cell have been conveniently designed in order to maximize the phase shift range keeping insertion losses as low as possible.

5.7. Conclusions

In this chapter, we have presented a novel analysis of periodically loaded transmission lines that provides the explicit design equations to locate the transmission peaks originated by these structures, focusing on the response when changing the characteristics of the periodically loading element. These equations account for the physical and electrical characteristics of the unit-cell, such as the electrical length, characteristic impedance, operating frequency or loading susceptance, and, importantly, the number of unit-cells

that form the system. We have validated the developed theory against both, simulations carried out with ADS, and experimental measurements of a fabricated prototype, achieving an excellent agreement. The achieved accurate control of such transmission peaks is planned to be exploited in the design of a variety of microwave applications such as phase shifters or tunable filters. Finally, though the microwave theory conceived in this chapter is expected to be applied in integrated circuit technology, the demonstrator is fabricated with SMD components, and therefore, the extrinsic contribution of parasitics due to the packaging of the varactors and the ground vias impacts on the circuit performance, mainly at high frequencies. These aspects can be nevertheless captured by our theoretical model by substituting the ideal susceptance by an equivalent one that includes the effect of all the extrinsic elements at high frequency, evidencing that the theory here presented can be adapted to real scenarios where deviations from the ideal device behavior are expected.

With respect to the phase, first, the need of the use of an explicit expression of the Tschebysheff second kind polynomials is exposed. Then, it is used to calculate the phase of an n-unit-cells circuit, as shown in eq. (5.26). Then, a discussion about the trade-off between having both, a big phase shift range and high return losses is made. Specifically, it is observed that increasing the variable capacitance range of the varactors allows for a higher phase shift range, but at the same time modifies the $|S_{11}|$ value and increases RL. In addition, it has been seen that neither increasing the number of unit-cells n, nor increasing the value of the normalized susceptance b, seem to benefit the trade-off in any manner, as always the effect of increasing or decreasing the Δb range where RL>10 dB, impacts the phase shift range in the opposite way. This makes that the effect of increasing/decreasing Δb compensates with the increase/decrease of n or b, thus keeping the phase shift range constant to a certain value.

Finally, the simulation of an $n = 5$ periodic structure at $f = 1$ GHz, whose unit-cell is formed by a transmission line loaded with a MIG diode, has been shown. The MIG diode simulation model has been adjusted using the experimental measurements from the fabricated MIG diodes showing a good agreement on the $C - V$ curve. The phase shifter shows a total phase shift range of $\Delta\phi_{21} = 187.33°$ with IL lower than 1 dB for the bias range $V_{\text{bias}} = [-1.5, 0.3]$ V. The fabrication of the designed phase shifter is proposed as a future work.

Part IV.

Conclusions and future outlook

Chapter 6. Conclusions and future outlook

6.1. Conclusions

This Thesis has shown the design and assessment of several essential RF circuits such as phase shifters, amplifiers, frequency multipliers or oscillators, using graphene-based devices, in particular the graphene field-effect transistor (GFET) and the metal-insulator-graphene (MIG) diode.

The conclusions of each chapter are here summarized:

- Chapter 1 outlined the motivation and justified the research line followed in this Thesis. In brief, graphene-based devices emerge as an alternative to conventional technologies due to the unique properties of graphene. In particular, in the field of high-frequency electronics, its high-carrier mobility and saturation velocity postulate graphene-based devices as promising for high-frequency applications. Although several fabrication and technological issues have hampered their promising potential, graphene technology is reaching higher readiness levels.

- In Chapter 2, a thorough exploration of the structure and working principle of the GFETss and the MIG diodes has been presented. GFETs are field-effect transistors where the semiconductor is replaced by a graphene layer. This makes the device behave differently as in a conventional MOSFET thanks to the peculiar band structure of graphene, with a conical instead of parabolic shape, and valence band and conduction band touching in one point, the so-called Dirac point, instead of presenting a bandgap. These characteristics produce singular effects, such as the transfer characteristic exhibiting a V-shaped curve, the fact that it is not possible to turn the transistor completely off, or the difficulties to reach current saturation. MIG diodes are formed by a vertical stack of graphene-insulator-metal, where the current flows between the metal and the graphene through the insulator barrier, via thermionic emission. Graphene's Fermi level tunability allows for a high asymmetry on the device, while its quantum capacitance tunability enables the use of the diode as a varactor.

- In Chapter 3, the fabrication and characterization of MIG diodes and GFETs, have been presented. MIG diodes were manufactured during a research stay at AMO

GmbH, in Aachen, Germany. As for the GFETs, they were fabricated through the 2D-EPL project. The characterization of both devices were performed at the University of Granada, in the facilities of the PEARL group.

- Chapter 4 has presented the design and simulation of four different GFET-based RF circuits: a power gain amplifier, a phase shifter, a frequency multiplier, and an oscillator.
  - A graphene-based phase shifter operating in the S-band has been designed, able to produce a phase shift on an input RF signal while maintaining a constant gain. Quantum capacitance tunability of graphene is leveraged in order to achieve the phase modulation, combined with an original design procedure. Phase shifts higher than 180° are possible, as well as gains above 15 dB. Moreover, a completely analog operation with the gate voltage acting as the control signal, has been demonstrated achieving a phase shift up to 84.5° without gain loss. These results demonstrate the potential of graphene technology for the future development of improved high frequency applications and in particular for analog phase shifters.
  - Regarding the power gain amplifier, we have theoretically assessed that current saturation is not mandatory, as widely assumed in the literature, to fully exploit GFETs for RF amplification. The analytic expressions of the figures of merit related to the power gain and microwave stability of a graphene RF amplifier in a common-source configuration have been derived. As long as the contact resistance at the common terminal is negligible, there is no direct relation between the achievable power gain, G_{max}, and the output conductance, g_{ds}. The connection between g_{ds} and G_{max} in practical cases, has been further analyzed by presenting different designs of power gain amplifiers based on fabricated GFETs with $G_{\mathrm{max}} > 5\,\mathrm{dB}$ at $2.4\,\mathrm{GHz}$ exhibiting $A_{\mathrm{v,i}}$ higher and lower than unity, demystifying the need for current saturation for the realization of graphene RF power gain amplifiers. Efforts must be focused on preserving the superb intrinsic carrier mobility in graphene to guarantee a high transconductance, instead of pursuing the opening of a bandgap in graphene to achieve current saturation and the corresponding low output conductance.
  - As for the frequency multiplier, is has been shown that the Dirac point shift (DPS) in GFETs is proportional to the sum of the drain and source intrinsic voltages, not accessible in practice, which can be considerably different from the externally applied biases due to the non-negligible metal-graphene contact resistances. It has been shown that the validity of the usual approximation that considers the DPS proportional to the external drain-to-source bias, is limited and should be avoided. Thus, a simple analytic equation for long-channel GFETs has been provided in order to evaluate the bias-dependence of the DPS. As a proof of concept, a frequency tripler/quadrupler based on W-shaped transfer characteristic of two cascaded single-gated GFETs has been proposed, evidencing that monitoring the bias-dependence of the DPS is piv-

otal for the design of RF applications. In summary, this section has provided critical insights on DPS phenomenon paving the way towards the development of RF multi-transistor circuits based on graphene technology.

  - Finally, the oscillator section has presented the design of a graphene-based microwave oscillator. The oscillator has been designed following the negative-resistance method and a fabricated GFET has been considered as the active device. The design includes an inductive feedback between the drain and the gate of the GFET to increase the instability of the device. Besides, a purely reactive terminating impedance, which minimizes power consumption, and an output matching network which matches a $50\,\Omega$ load to the desired load impedance, while simultaneously acting as a low-pass filter to suppress the higher harmonics. The performance projection has showed an oscillation frequency of $10.12\,$GHz, and a power delivered to a $50\,\Omega$ load greater than $-19\,$dBm.

- Finally, Chapter 5 is focused on the design of MIG-based circuits. First, a unit-cell formed by a section of transmission line loaded with a shunt varactor was analyzed and optimized, where the MIG diode was used as the variable capacitor, exposing its phase shifting possibilities with a simulated demonstrator. Then, a novel analysis of periodically loaded transmission lines has been presented, extending the previous study to the case of n unit-cells within a periodic structure and providing explicit design equations to locate the transmission peaks originated by these structures, focusing on the response when changing the characteristics of the periodically loading element. These equations account for the physical and electrical characteristics of the unit cell, such as the electrical length, characteristic impedance, operating frequency or loading susceptance, and, importantly, the number of unit cells that form the system. The developed theory has been validated against both, circuit simulations and experimental measurements of a fabricated prototype, achieving an excellent agreement. Finally, the simulation of an $n = 5$ periodic structure at $1\,$GHz, whose unit-cell is formed by a transmission line loaded with a MIG diode, has been shown. The MIG diode simulation model has been adjusted using the experimental measurements from the fabricated MIG diodes showing a good agreement on the $C - V$ curve. The phase shifter shows a total phase shift range of $\Delta\phi_{21} = 187.33°$ with IL lower than $1\,$dB for the bias range $V_{\text{bias}} = [-1.5, 0.3]\,$V.

6.2. Future work

As stated throughout the Thesis, the research line on the design of circuits using graphene and in general 2D materials-based electronic devices entails a great opportunity to help traditional semiconductor technologies to continue the reign of the electronic industry as one of the most prominent of our society. In order to continue with the work presented in this Thesis, several future work lines are hereby proposed:

- Develop fabrication processes that can combine GFET and MIG diodes, which could be useful for circuits like the oscillator, where the MIG diode could be use as a varactor for the controlling of the oscillation frequency of the whole circuit.
- Development of filters making use of graphene-based devices, specifically profiting from the developed theory of the periodic structures in Chapter 5, which outlines their feasibility.
- Fabrication of demonstrators of the circuits that have not been fabricated, in order to further corroborate simulation results. This could be done in more advanced stages of the 2D-EPL, or participating in projects like Infrachip [254].
- Once the performance of each individual circuit has been assessed, development and fabrication of an entire wireless receiver, as the one shown in Fig. 1.1 of Chapter 1, completely based in graphene technology.

Journal Publications

[J1] **A. Medina-Rull**, F. Pasadas, E. G. Marin, A. Godoy, A. Vorobiev, J. Stake, and F. G. Ruiz, "10 ghz negative resistance oscillator using a graphene field-effect transistor," submitted, 2024.

[J2] **A. Medina-Rull**, P. Kumar, A. Mansouri, F. G. Ruiz, O. Habibpour, H. Zirath, A. Pacheco-Sanchez, E. G. Marin, W. Wei, L. Anzi, A. Zurutuza, H. Happy, R. Sordan, A. Godoy, D. Jiménez, and F. Pasadas, "On the impact of the output conductance on high-frequency amplification in graphene transistors," submitted, 2024.

[J3] F. Pasadas, **A. Medina-Rull**, F. G. Ruiz, J. N. Ramos-Silva, A. Pacheco-Sanchez, M. C. C. Pardo, A. Toral-Lopez, A. Godoy, E. Ramírez-García, D. Jiménez, *et al.*, "Exploiting ambipolarity in graphene field-effect transistors for novel designs on high-frequency analog electronics," *Small*, vol. 19, no. 49, p. 2 303 595, 2023.

[J4] **A. Medina-Rull**, F. Pasadas, E. G. Marin, A. Godoy, and F. G. Ruiz, "A novel analysis of periodic structures based on loaded transmission lines," *IEEE Journal of Microwaves*, vol. 3, no. 3, pp. 1019–1027, 2023.

[J5] **A. Medina-Rull**, F. Pasadas, E. G. Marin, A. Toral-Lopez, J. Cuesta, A. Godoy, D. Jiménez, and F. G. Ruiz, "A graphene field-effect transistor based analogue phase shifter for high-frequency applications," *IEEE Access*, vol. 8, pp. 209 055–209 063, 2020.

Conference Publications

[C1] **A. Medina-Rull**, F. Pasadas, M. C. Pardo, M. G. Palomo, E. G. Marin, A. Godoy, A. Vorobiev, J. Stake, and F. G. Ruiz, "Graphene-based microwave oscillator," in *Graphene Conference 2024*, Madrid, Spain, Jun. 2024.

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[C3] **A. Medina-Rull**, F. Pasadas, M. C. Pardo, E. G. Marin, M. G. Palomo, A. Godoy, A. Vorobiev, J. Stake, and F. G. Ruiz, "Graphene-based microwave oscillator," in *Workshop on 2D Materials for Future Electronics*, Aachen, Germany, Feb. 2024.

[C4] **A. Medina-Rull**, S. Stoll, A. Esteki, F. Pasadas, M. C. Pardo, A. Toral-Lopez, E. G. Marín, A. Godoy, Z. Wang, M. C. Lemme, and F. G. Ruiz, "Periodic structures-based phase shifter using metal-insulator-graphene diodes," in *Graphene Week 2023*, Göteborg, Sweden, Sep. 2023.

[C5] **A. Medina-Rull**, F. Pasadas, M. C. Pardo, J. Cuesta-Lopez, A. Toral-Lopez, E. G. Marín, A. Godoy, and F. G. Ruiz, "Microwave circuit design using 2D materials," in *Graphene Study 2023*, Obergurgl, Austria, Apr. 2023.

[C6] **A. Medina-Rull**, F. Pasadas, M. C. Pardo, A. Toral-Lopez, E. G. Marín, A. Godoy, and F. G. Ruiz, "Periodic structures based on two-dimensional materials: Application to phase shifters," in *XXXVII Conference on Design of Circuits and Integrated Systems (DCIS 2022)*, Pamplona, Spain, Nov. 2022.

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[C10] **A. Medina-Rull**, F. Pasadas, M. C. Pardo, M. La Mura, P. Lamberti, D. Jiménez, and F. G. Ruiz, "Graphene-based analogue phase shifters for phased array antennas in aerospace/aeuronautical applications," in *11th EASN Conference on Innovation in Aviation & Space to the Satisfaction of European Citizens*, Virtual, Sep. 2021.

Additional Journal and Conference Publications

[J7] F. Pasadas, T. El Grour, E. G. Marin, **A. Medina-Rull**, A. Toral-Lopez, J. Cuesta-Lopez, F. G. Ruiz, L. El Mir, and A. Godoy, "Compact modeling of two-dimensional field-effect biosensors," *Sensors*, vol. 23, no. 4, p. 1840, 2023.

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