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Low-Frequency Noise in InGaAs-OI Transistors

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***Abstract*—III-V compounds have recently attracted high expectation due to their potential to relieve the semiconductor scaling constraints. Scaled indium gallium arsenide (InGaAs) transistors have recently proved to operate as single transistor DRAM exploiting the floating-body effect, enabling getting rid of the external capacitor and minimizing the cell footprint. However, extensive characterization of the interface quality and disturbing mechanisms affecting the device operation are still required. This work addresses the low frequency noise characterization of these III-V InGaAs transistors focusing on their DRAM operation. The experimentally extracted power spectral density of current follows a flicker-noise characteristic which points to carrier number fluctuations as the main noise source. However, mobility degradation associated to trapping-detrapping carrier phenomena has to be also taken into account to model the device operation. Finally, the device dimension and the back-gate bias dependence on the effective trap density have been evaluated.**

I. Introduction

In the last decades, the limitations to accomplish the integration density requirements in the Moore's Law have been solved shrinking the transistor dimensions (particularly channel length) [1], [2], incorporating high-κ insulators [3] and implementing new device architectures (FinFET, SOI, trigate, forksheet or complementary FET) [4], [5], [6]. The advances in the lithography (deep ultraviolet (DUV) and multi-patterning techniques) have been employed to shrink the dimensions of transistors down-to sub-10nm channel lengths [2]. Extreme ultraviolet (EUV) lithography is being used to improve the pitch resolution and further scale the gate length but assuming an important increase of the manufacturing cost and complexity [7]. At the same time, other alternatives to increase the performance of the integrated circuits are being considered [7]: Silicon channel material substitution [8], [9] and the integration of multiple transistor levels in a three-dimensional (3-D) scheme [10], [11] have been perceived as promising alternatives to follow the Moore's Law. High-mobility or/and wide band-gap materials such as Germanium (Ge), silicon-germanium (SiGe) and III-V compounds have been widely analyzed with relevant results in high power, memory and photonics applications [12]. Moreover, III-V material are also promising for a potential 3-D integration, where a semiconductor layer is achieved on top of the processed bottom tier device and interconnect layers, due to their relatively low process thermal budget [13], [14]. In fact, active III-V layers have been successfully transferred [15] and epitaxially grown [16] showing outstanding performance. Regarding the memory solutions, static random access memory (SRAM) circuits have been validated employing InGaAs n-FinFET layer on fully-depleted silicon-on-insulator CMOS [17] and capacitor-less one-transistor dynamic random access memory (DRAM) cell has been demonstrated employing n-type InGaAs-on-insulator with a silicon back-gate [18]. This latter implementation, denoted as 1T-DRAM, supposes a footprint miniaturization approach removing the external capacitor and is one of the best positioned alternatives in DRAM scaling. Some implementations employing several architectures have been already evaluated in different silicon nodes [19], [20], [21], [22], [23]. In the 1T-DRAM approach, the charge that represents the information is stored within the transistor body. Indeed, in the case of this InGaAs 1T-DRAM approach, the operation as memory cell has already been modeled and exhaustively characterized in previous works demonstrating promising results with ms-order of retention times in devices scaled down to a gate length of 14 nm [24], [25], [18]. In addition, it is also reported that enhancing the top and bottom interfaces quality, cell performing would improve as density of states is related to the retention time degradation [18]. However, the novelty of the fabrication and integration processes, the use of high-mobility channel materials and the implementation of a back-gate to modulate the body charge together with the floating-body effect employed in the memory operation may induce some doubts about the origin and behaviour of the disturbing mechanisms. To shed light on the trapping and detrapping events, the noise sources and the implications with the device scaling, we have experimentally characterized the low-frequency noise signature of these scaled InGaAs-OI transistors operating as 1T-DRAM cell.

II. Experimental setup

The n-type InGaAs-OI transistors on silicon substrates were fabricated by metal–organic chemical vapour deposition (MOCVD) at IBM Research Zurich [26]. Ultra-Thin-Body and BOX (UTBB) InGaAs-OI sample fabrication began with a (100)-oriented InP donor wafer, then an $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ etch-stop heterostructure was grown at 550^oC followed by growth of an $In_{0.53}Ga_{0.47}As$ active layer. The wafers were loaded into an atomic layer deposition tool and the Al_2O_3 buried oxide (BOX) was deposited at 250^oC, capping the active layer. The target wafer was transferred to the substrate (100)-oriented p-type

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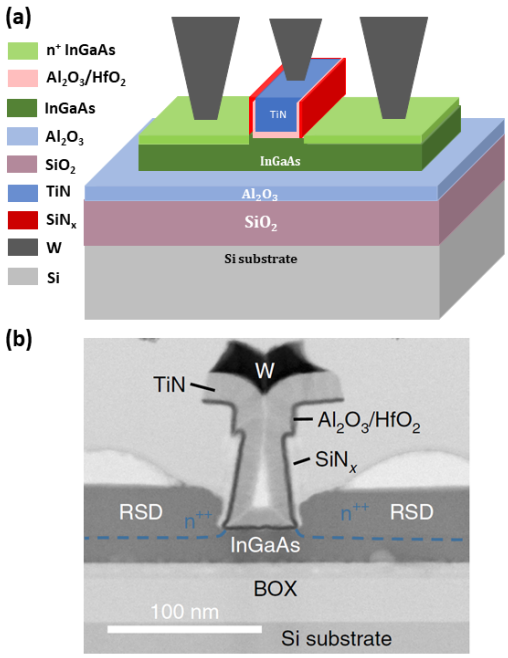

Fig. 1. (a) Schematic transistor representation and (b) TEM image of one of the characterized III-V transistors.

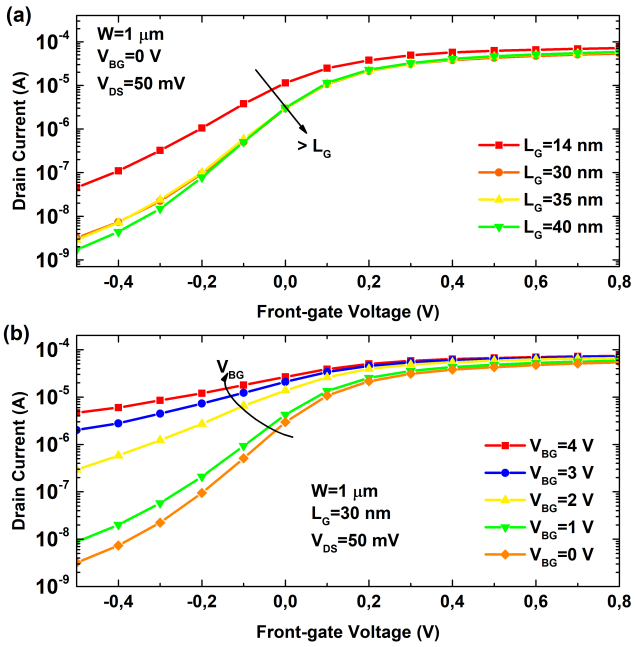

Fig. 2. Drain current as a function of the front-gate bias for different (a) channel lengths and (b) back-gate biases in a 30 *nm*-length and 1 μm-width transistor.

Si wafer by direct wafer bonding (DWB). Selective MOCVD regrowth of the $In_{0.53}Ga_{0.47}As$ raised source/drain (RSD) was achieved using a low-temperature Sn-doping process. The samples feature a residually n-type doped ($N_D \approx 2{\cdot}10^{16}$ cm^{-3}) thin $In_{0.53}Ga_{0.47}$ as channel layer of 20 nm thickness. This thickness is enough to enable memory operation suppressing a potential supercoupling effect. To perform the back gate (BG) a Al_2O_3/SiO_2 bilayer of 10/25 nm thickness is employed as buried oxide (BOX) underneath the device body. Regarding the front gate (FG), a 4-*nm*-thick Al_2O_3/HfO_2 high-κ insulator (1 nm SiO_2 equivalent oxide thickness) is employed to ensure good front-channel electrostatic control. Both source and drain (S/D) regions are raised by 25 nm, reducing the access series resistance with doping concentration $N_D \approx 10^{19}$ cm^{-3}, while 9-nm-thick SiN_x spacers are formed to isolate the gate stack from the S/D regions. A device scheme and a transmission electron microscopy (TEM) image of a scaled III–V transistor are provided in Figures 1.a and 1.b, respectively. Different device lengths and widths were characterized directly in a Suss PA-300 probe station. For the direct-current (DC) characterization Keysight B1500 is used, while the low-frequency noise measurements were carried out by using a low-noise-current amplifier connected to a software-based spectrum analyzer [27].

III. Results and Discussion

A. Static DC characteristic

The transfer characteristic of devices with different aspect ratio are shown in Figure 2.a demonstrating the proper electrostatic control of the front-gate. Figure 2.b depicts how the back-gate bias influences on the transfer characteristic of a 30 *nm*-length and 1 μm-width device. Regarding the threshold voltage, the V_{th} of the front gate, when the ground plane is grounded, typically range from 0 to 0.1 V. As the back-gate voltage increases, the current flow gradually switches from the top to the bottom channel. The inversion channel shifts towards the back interface, flattening the current as it becomes more insensitive to the front-gate electrostatic control (and reducing the threshold voltage). This relation confirms the inter-gate coupling effect [28], enabling the 1T-DRAM operation [18].

B. Low-frequency noise characteristic

The normalized drain current noise spectral density as a function of front-gate bias for devices with different aspect ratio and operating in linear region is shown in Figure 3. They show the typical 1/f dependence according to flicker noise characteristics [29], [30]. Moreover, for the very short channel device presented in Figure 3.a, a $1/f^2$ dependence observed at high frequency suggests individual carrier trapping at the oxide interface related to generation-recombination or random telegraph noise signals [31], [32]. The fact that the normalized noise levels are similar regardless the front-gate bias discards the generation of trap states for these operation conditions. However, when a positive back-gate voltage is applied, the normalized power spectral density of the noise presents lower level, as Figure 4 shows. This fact highlights the importance of the back-gate-channel interface and its contribution on the noise level.

To corroborate the source of the noise for these specific structures, in Figure 5, the normalized power spectral density of the noise as a function of the drain current is depicted for devices with different aspect ratio. According to the carrier number fluctuations model based on the McWhorter's charge

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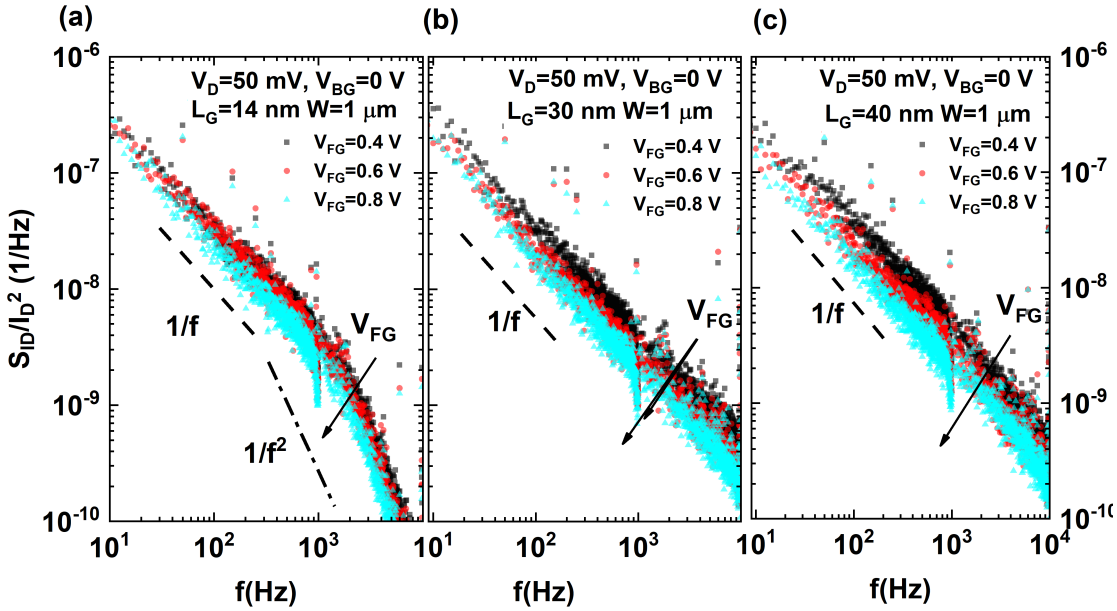

Fig. 3. Normalized current noise spectral densities as a function of the frequency for devices featuring different gate lengths: (a) L_G =14 *nm* (b) L_G =30 *nm* and c) L_G =40 *nm* and for different front gate biases. V_D =50 *mV* and W =1 μm.

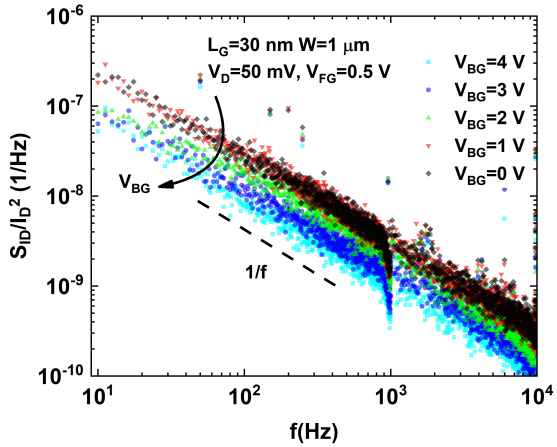

Fig. 4. Normalized current noise spectral densities as a function of the frequency for a device under different positive back-gate biases.

trapping theory [33], the normalized power density of the noise should follow the equation [34]:

$$\frac{S_{ID}}{I_D^2} = S_{Vfb}\left(\frac{g_m}{I_D}\right)^2 \tag{1}$$

where S_{Vfb} is the flat band voltage noise associated with the interface charge fluctuations of spectral density and g_m and I_D are the device trasnconductance and drain current, respectively. To evaluate the fitting with this model, the square of normalized transconductance, $(g_m/I_D)^2$, is plotted in Figure 5 employing dashed lines. However, there is not a proper fit for any of the characterized devices, especially at strong inversion (high current levels), suggesting that the carrier number fluctuation model, by itself, cannot describe the noise level dependence. This normalized noise behavior, constant in weak inversion and rolling-off in strong inversion, was already demonstrated by Reimbold [35]. The Hooge mobility fluctuations model [30] neither explains this behavior. In this latter case, a reciprocal variation between the normalized PSD and the drain current ($\propto 1/I_D$) would be expected from weak to strong inversion due to fluctuations in bulk mobility. However, in our case, this reciprocal variation is only observed at high inversion regime (magenta dotted lines in Figure 5) and not for all the devices (30 *nm*-thick device presents a quadratic variation with the current). Therefore, these results suggest that the low frequency noise is dominated by the fluctuation of the carrier number together with a significant correlated mobility fluctuation term. This carrier number fluctuations and correlated mobility fluctuations approach was proposed [36], [34] and then extensively corroborated in Si and SOI MOSFETs [37], junctionless devices [38] and also for III-V structures [39], [40], [41], [42]. To model this mobility dependence, an analysis including the supplementary mobility charges μ_{eff} due to the modulation of the scattering rate induced by the interface charge fluctuations is included:

$$\frac{S_{ID}}{I_D^2} = \left(1+\Omega\frac{I_D}{g_m}\right)^2 S_{Vfb}\left(\frac{g_m}{I_D}\right)^2 \tag{2}$$

where the noise parameter related to the Coulomb scattering coefficient α ($\approx 10^4$ Vs/C for electrons and 10^5 Vs/C for holes [37]) is included as $\Omega = \alpha\mu_{eff}C_{ox}$ being μ_{eff} the effective mobility and C_{ox} the gate oxide capacitance. The normalized drain current and input gate voltage noise can be related for strong inversion as $S_{VG} = S_{ID}/g_m^2$ and therefore, the the input gate voltage noise can be described as [37]:

$$S_{VG} = S_{Vfb}\left(1+\Omega\frac{I_D}{g_m}\right)^2 \tag{3}$$

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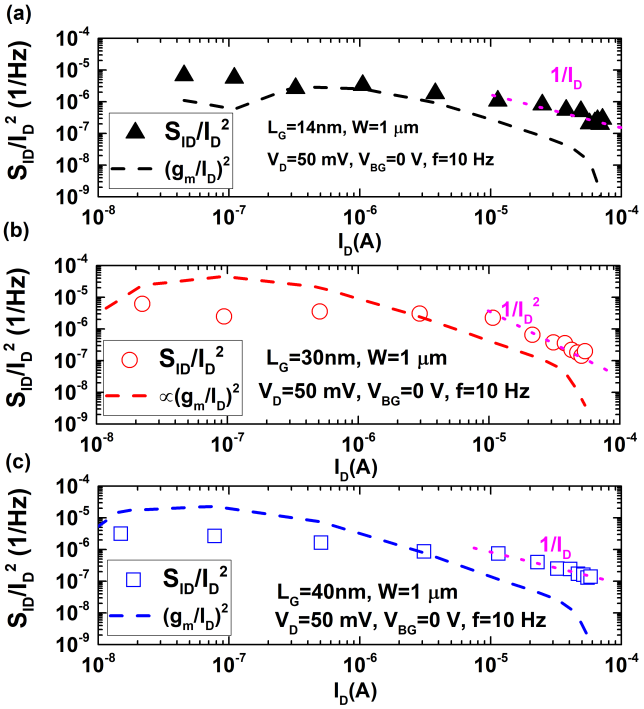

Fig. 5. Normalized current noise spectral densities as a function of the drain current for two devices featuring different gate region lengths (a) L_G =14 *nm*, (b) L_G =30 *nm* and (c) L_G =40 *nm*. Frequency f =10 *Hz*. T = 300 *K*.

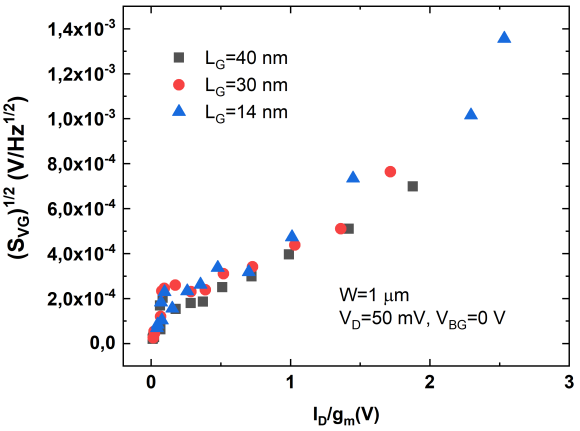

Fig. 6. Square root of the input gate voltage noise $\sqrt{S_{VG}}$ as a function of I_d/g_m for three devices featuring L_G =40 *nm*, L_G =30 *nm* and L_G =14 *nm*. Frequency f =10 *Hz*. T = 300 *K*.

If the trapping mechanisms into oxide are due to tunneling process, the flat-band voltage spectral density can be defined as [35], [34]:

$$S_{Vfb} = \frac{q^2 kT\lambda N_T}{WLC_{ox}^2 f} \tag{4}$$

were f is the frequency, λ is the tunnel attenuation distance (≈0.1 nm), kT is the thermal energy and N_T is the volumetric oxide trap density (eV^{-1}cm^{-3}).

Then, the previous expressions can be unified (at high current levels) as:

$$\frac{S_{ID}}{I_D^2} = S_{VG}\left(\frac{g_m}{I_D}\right)^2 = \frac{q^2 kT\lambda N_T}{WLC_{ox}^2 f}\left(1+\Omega\frac{I_D}{g_m}\right)^2\left(\frac{g_m}{I_D}\right)^2 \tag{5}$$

The lack-of-fit between the normalized noise and the $(g_m/I_D)^2$ dashed line observed in Figure 5 points that S_{VG} is not constant for the range of drain currents measured. Therefore, an important contribution of mobility fluctuations is expected for these devices. This can be observed in Figure 6 where the input gate voltage noise S_{VG} has been experimentally extracted from $S_{VG} = S_{ID}/g_m^2$. As observed, an important contribution of the mobility fluctuations is expected at high inversion regime. This contribution is modelled with the second term in the parentheses of Expression 3 [37].

However, from expression 5, there are parameters whose dependence with current and gate overdrive $(V_G - V_{th})$ voltage could not be neglected. Other works have demonstrated that μ_{eff} is gate voltage dependent while α is expected to decrease with the drain current due to the charge screening in the channel [41]. Besides, N_T could vary with respect to energy with a minimum in vicinity to the InGaAs conduction band and increasing both above a below [41]. To clarify these aspects parameters such as the input flat-band voltage noise (related to the oxide trap density) and Ω (related to the effective Coulomb scattering coefficient) can be extracted experimentally from a plot of $\sqrt{S_{VG}}$ versus I_D/g_m as [43]:

$$\sqrt{S_{VG}} = \sqrt{S_{Vfb}}\left(1+\Omega\frac{I_D}{g_m}\right) \tag{6}$$

Input flat-band voltage noise and Ω have been derived from the experimental data through Expression 6. Then S_{VG} has been calculated according to Expression 3. Finally, the complete model of Expression 5 has been evaluated comparing with S_{ID}/I_D^2 experimentally characterized results in Figure 7. The inclusion of the factor S_{VG} yields an accurate fit for the carrier number and the mobility fluctuations in strong inversion. The fitting is less accurate at low inversion due to the high inversion regime approaches taken in Expression 3. Moreover, discrepancies from the straight line could be detected in short devices, particularly at very high inversion regime, resulting in decreased fitting accuracy. Table I shows the S_{Vfb} and Ω values for devices with different aspect ratio. The coefficient of determination, R^2 is also included. Values of average gate dielectric trap density are in accordance with these obtained in other III-V devices [39], [40], [41] being higher than these found for silicon nanoscaled MOSFETs [43], [38]. Regarding the relationship between the volume trap density or Coulomb scattering coefficient and the aspect ratio of these devices, there is not a clear trend. However, thinner device generally present a higher volume trap density and a lower correlated mobility fluctuations. This fact highlights the importance of the border traps and effects.

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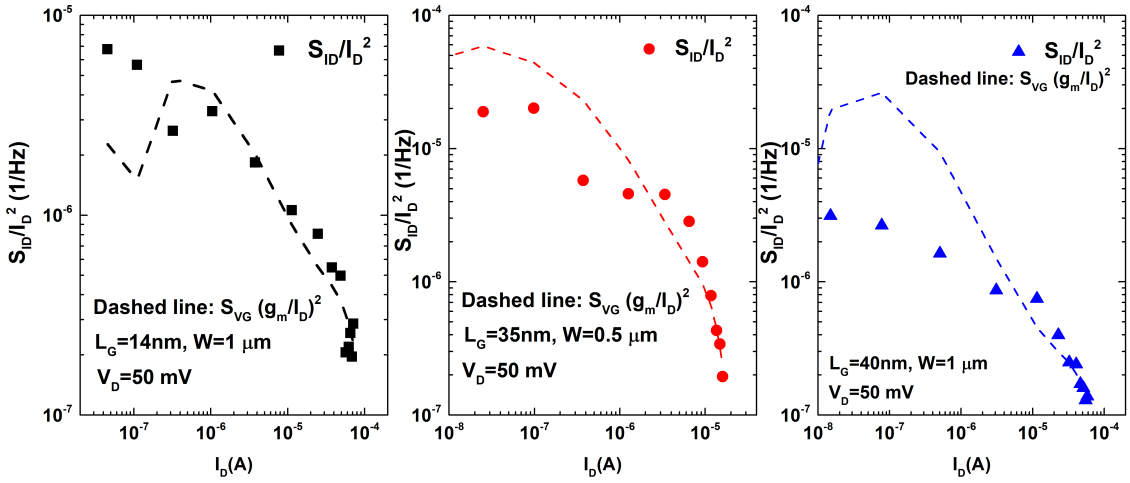

Fig. 7. Normalized current noise spectral densities (measured in solid and modelled in dashed line) as a function of the drain current for devices featuring different gate region lengths or widths. Frequency $f = 10\ Hz$. $T = 300\ K$.

L_G (nm)	W_G (μm)	S_{Vfb} (V^2/Hz)	Ω (V^{-1})	N_t (cm^{-3} eV^{-1})	R^2
14	1	0.47×10^{-8}	6.70	1.18×10^{19}	0.98
30	1	0.70×10^{-8}	4.38	3.80×10^{19}	0.94
35	1	2.60×10^{-8}	1.81	1.63×10^{20}	0.99
40	1	0.22×10^{-8}	7.28	1.62×10^{19}	0.99
50	1	0.89×10^{-8}	3.44	8.05×10^{19}	0.97
30	0.5	4.43×10^{-8}	3.86	1.19×10^{20}	0.87
35	0.5	12.2×10^{-8}	0.62	3.85×10^{20}	0.93
70	0.5	7.14×10^{-8}	2.27	4.49×10^{20}	0.98
80	0.5	3.18×10^{-8}	3.67	2.28×10^{20}	0.95

TABLE I
EXTRACTED VALUES ACCORDING TO EQUATION 5 FOR DIFFERENT ASPECT RATIO DEVICES.

V_{BG} (V)	S_{Vfb} (V^2/Hz)	Ω (V^{-1})	N_t (cm^{-3} eV^{-1})	R^2
0	0.70×10^{-8}	4.38	3.80×10^{19}	0.94
1	1.84×10^{-8}	2.06	9.90×10^{19}	0.96
2	2.94×10^{-8}	1.21	1.58×10^{20}	0.98
3	3.98×10^{-8}	1.02	2.14×10^{20}	0.85
4	3.73×10^{-8}	0.96	2.01×10^{19}	0.89

TABLE II
EXTRACTED VALUES ACCORDING TO EQUATION 5 FOR DIFFERENT BACK-GATE BIASES IN A $L = 30$ NM AND A $W = 1\ \mu m$ DEVICE.

Finally, the influence of the back-gate bias on the devices performance is depicted in Table II. The values of volume trap density and Coulomb scattering coefficient have been extracted for a $30nm$-length and $1\mu m$-width device under back-gate voltages from 0 to 4 volts. An increase of the carrier number of fluctuation dependence versus the mobility fluctuations is observed when the inversion channel shifts towards the back interface. This may be considered as a lower influence of the mobility fluctuation when current is more insensitive to the front-gate electrostatic control.

IV. Conclusions

The low-frequency noise characterization of these III-V InGaAs 1T-DRAM cells has pointed to carrier number fluctuations as the main noise source. However, carrier mobility fluctuations induced by these trapping/de-trapping carrier exchanges have demonstrated an important influence that may impact on the 1T-DRAM operation and variability. Normalized noise has been successfully modelled included both phenomena for different devices. In addition, low frequency noise characterization has demonstrated an important carrier mobility fluctuation influence in wide devices which is limited when the gate width is reduced or the back-gate bias increases.

Acknowledgment

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References

[1] D. Frank, R. Dennard, E. Nowak, P. Solomon, Y. Taur, and Hon-Sum Philip Wong, "Device scaling limits of Si MOSFETs and their application dependencies," *Proceedings of the IEEE*, vol. 89, no. 3, pp. 259–288, mar 2001.

[2] M. L. Rieger, "Retrospective on VLSI value scaling and lithography," *Journal of Micro/Nanolithography, MEMS, and MOEMS*, vol. 18, no. 04, p. 1, 2019.

[3] V. Narayanan, "High-k/Metal Gates- from research to reality," in *2007 International Workshop on Physics of Semiconductor Devices*. IEEE, dec 2007, pp. 42–45. [Online]. Available: http://ieeexplore.ieee.org/document/4472451/

[4] C. Maleville, "Engineered substrates for Moore and more than Moore's law: Device scaling: Entering the substrate era," *2015 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference, S3S 2015*, no. 2, 2015.

[5] H. Mertens, R. Ritzenthaler, Y. Oniki, B. Briggs, B. Chan, A. Hikavyy, T. Hopf, G. Mannaert, Z. Tao, F. Sebaai, A. Peter, K. Vandersmissen, E. Dupuy, E. Rosseel, D. Batuk, J. Geypen, G. T. Martinez, D. Abigail, E. Grieten, K. Dehave, J. Mitard, S. Subramanian, L. Ragnarsson, P. Weckx, D. Jang, B. Chehab, G. Hellings, J. Ryckaert, E. D. Litta,

and N. Horiguchi, "Forksheet fets for advanced cmos scaling: Forksheet-nanosheet co-integration and dual work function metal gates at 17nm n-p space," in *2021 Symposium on VLSI Technology*, 2021, pp. 1–2.

[6] S.-W. Chang, P.-J. Sung, T.-Y. Chu, D. D. Lu, C.-J. Wang, N.-C. Lin, C.-J. Su, S.-H. Lo, H.-F. Huang, J.-H. Li, M.-K. Huang, Y.-C. Huang, S.-T. Huang, H.-C. Wang, Y.-J. Huang, J.-Y. Wang, L. W. Yu, Y.-F. Huang, F. K. Hsueh, C.-T. Wu, W. C.-Y. Ma, K.-H. Kao, Y. J. Lee, C.-L. Lin, R. W. Chuang, K.-P. Huang, S. Samukawa, Y. Li, W. H. Lee, T.-S. Chao, G. W. Huang, W.-F. Wu, J. Y. Li, J.-M. Shieh, W. K. Yeh, and Y.-H. Wang, "First demonstration of cmos inverter and 6t-sram based on gaa cfets structure for 3d-ic applications," in *2019 IEEE International Electron Devices Meeting (IEDM)*, 2019, pp. 11.7.1–11.7.4.

[7] S. B. Samavedam, J. Ryckaert, E. Beyne, K. Ronse, N. Horiguchi, Z. Tokei, I. Radu, M. G. Bardon, M. H. Na, A. Spessot, and S. Biesemans, "Future logic scaling: Towards atomic channels and deconstructed chips," *Technical Digest - International Electron Devices Meeting, IEDM*, vol. 2020-December, pp. 1.1.1–1.1.10, 2020.

[8] J. A. Del Alamo, D. A. Antoniadis, J. Lin, W. Lu, A. Vardi, and X. Zhao, "III-V MOSFETs for Future CMOS," *2015 IEEE Compound Semiconductor Integrated Circuit Symposium, CSICS 2015*, pp. 1–4, 2015.

[9] S. Das, A. Sebastian, E. Pop, C. J. McClellan, A. D. Franklin, T. Grasser, T. Knobloch, Y. Illarionov, A. V. Penumatcha, J. Appenzeller, Z. Chen, W. Zhu, I. Asselberghs, L.-J. Li, U. E. Avci, N. Bhat, T. D. Anthopoulos, and R. Singh, "Transistors based on two-dimensional materials for future integrated circuits," *Nature Electronics*, vol. 4, no. 11, pp. 786–799, Nov. 2021. [Online]. Available: https://www.nature.com/articles/s41928-021-00670-1

[10] A. Mallik, A. Vandooren, L. Witters, A. Walke, J. Franco, Y. Sherazi, P. Weckx, D. Yakimets, M. Bardon, B. Parvais, P. Debacker, B. W. Ku, S. K. Lim, A. Mocuta, D. Mocuta, J. Ryckaert, N. Collaert, and P. Raghavan, "The impact of sequential-3D integration on semiconductor scaling roadmap," *Technical Digest - International Electron Devices Meeting, IEDM*, pp. 32.1.1–32.1.4, 2018.

[11] D. Jayachandran, R. Pendurthi, M. U. K. Sadaf, N. U. Sakib, A. Pannone, C. Chen, Y. Han, N. Trainor, S. Kumari, T. V. Mc Knight, J. M. Redwing, Y. Yang, and S. Das, "Three-dimensional integration of two-dimensional field-effect transistors," *Nature*, vol. 625, no. 7994, pp. 276–281, Jan. 2024. [Online]. Available: https://www.nature.com/articles/s41586-023-06860-5

[12] M. Heyns and W. Tsai, "Ultimate scaling of CMOS logic devices with Ge and III-V materials," *MRS Bulletin*, vol. 34, no. 7, pp. 485–488, 2009.

[13] D. Caimi, H. Schmid, T. Morf, P. Mueller, M. Sousa, K. E. Moselund, and C. B. Zota, "III-V-on-Si transistor technologies: Performance boosters and integration," *Solid-State Electronics*, vol. 185, 2021.

[14] C. Convertino, C. B. Zota, H. Schmid, D. Caimi, L. Czornomaz, A. M. Ionescu, and K. E. Moselund, "A hybrid III–V tunnel FET and MOSFET technology platform integrated on silicon," *Nature Electronics*, vol. 4, no. 2, pp. 162–170, feb 2021. [Online]. Available: http://www.nature.com/articles/s41928-020-00531-3

[15] C. Convertino, C. B. Zota, D. Caimi, M. Sousa, and L. Czornomaz, "InGaAs FinFETs 3-D Sequentially Integrated on FDSOI Si CMOS with Record Performance," *IEEE Journal of the Electron Devices Society*, vol. 7, pp. 1170–1174, 2019.

[16] O. P. Kilpi, M. Hellenbrand, J. Svensson, A. R. Persson, R. Wallenberg, E. Lind, and L. E. Wernersson, "High-Performance Vertical III-V Nanowire MOSFETs on Si with gm> 3 mS/μm," *IEEE Electron Device Letters*, vol. 41, no. 8, pp. 1161–1164, 2020.

[17] V. Deshpande, H. Hahn, E. O'Connor, Y. Baumgartner, D. Caimi, M. Sousa, H. Boutry, J. Widiez, L. Brevard, C. Le Royer, M. Vinet, J. Fompeyrine, and L. Czornomaz, "Demonstration of 3-D SRAM Cell by 3-D Monolithic Integration of InGaAs n-FinFETs on FDSOI CMOS with Interlayer Contacts," *IEEE Transactions on Electron Devices*, vol. 64, no. 11, pp. 4503–4509, 2017.

[18] C. Navarro, S. Karg, C. Marquez, S. Navarro, C. Convertino, C. Zota, L. Czornomaz, and F. Gamiz, "Capacitor-less dynamic random access memory based on a III–V transistor with a gate length of 14 nm," *Nature Electronics*, vol. 2, no. 9, pp. 412–419, sep 2019. [Online]. Available: http://dx.doi.org/10.1038/s41928-019-0282-6 https://doi.org/10.1038/s41928-019-0282-6 http://www.nature.com/articles/s41928-019-0282-6

[19] S. Okhonin, M. Nagoga, J. M. Sallese, and P. Fazan, "A capacitor-less 1T-DRAM cell," *IEEE Electron Device Letters*, vol. 23, no. 2, pp. 85–87, feb 2002.

[20] N. Rodriguez, S. Cristoloveanu, and F. Gamiz, "New concepts for 1T-DRAMs: Overcoming the scaling limits," in *CAS 2011 Proceedings (2011 International Semiconductor Conference)*. Sinaia: IEEE, oct 2011, pp. 11–14.

[21] M. Bawedin, S. Cristoloveanu, and D. Flandre, "Novel capacitor-less 1T-DRAM using MSD effect," in *Proceedings - IEEE International SOI Conference*, 2007, pp. 109–110.

[22] S. Navarro, C. Navarro, C. Marquez, H. El Dirani, P. Galy, M. Bawedin, A. Pickering, S. Cristoloveanu, and F. Gamiz, "Experimental Demonstration of Operational Z 2 -FET Memory Matrix," *IEEE Electron Device Letters*, vol. 39, no. 5, pp. 660–663, may 2018. [Online]. Available: https://ieeexplore.ieee.org/document/8325461/

[23] F. Gamiz, N. Rodriguez, C. Navarro, C. Marquez, and S. Cristoloveanu, "Tri-Dimensional A2-RAM Cell: Entering the Third Dimension," in *Functional Nanomaterials and Devices for Electronics, Sensors and Energy Harvesting*, A. Nazarov, F. Balestra, V. Kilchytska, and D. Flandre, Eds. Cham: Springer International Publishing, 2014, pp. 105–124.

[24] C. Navarro, S. Navarro, C. Marquez, C. Sampedro, L. Donetti, S. Karg, H. Riel, and F. Gamiz, "Towards InGaAs MSDRAM Capacitor-Less Cells," *ECS Transactions*, vol. 85, no. 8, pp. 195–200, 2018.

[25] C. Navarro, S. Navarro, C. Marquez, L. Donetti, C. Sampedro, S. Karg, H. Riel, and F. Gamiz, "InGaAs Capacitor-Less DRAM Cells TCAD Demonstration," *IEEE Journal of the Electron Devices Society*, vol. 6, no. July, pp. 884–892, 2018.

[26] L. Czornomaz, N. Daix, P. Kerber, K. Lister, D. Caimi, C. Rossel, M. Sousa, E. Uccelli, and J. Fompeyrine, "Scalability of ultra-thin-body and box ingaas mosfets on silicon," in *2013 Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, 2013, pp. 143–146.

[27] J. Chroboczek, "Automatic, wafer-level, low frequency noise measurements for the interface slow trap density evaluation," in *International Conference on Microelectronic Test Structures, 2003.* IEEE, 2003, pp. 95–98.

[28] Hyung-Kyu Lim and J. G. Fossum, "Threshold voltage of thin-film Silicon-on-insulator (SOI) MOSFET's," *IEEE Transactions on Electron Devices*, vol. 30, no. 10, pp. 1244–1251, 1983.

[29] S. Machlup, "Noise in semiconductors: Spectrum of a two-parameter random signal," *Journal of Applied Physics*, vol. 25, no. 3, pp. 341–343, 1954.

[30] F. Hooge, "1/f noise," *Physica B+C*, vol. 83, no. 1, pp. 14–23, 1976.

[31] K. Ralls, W. Skocpol, L. Jackel, R. Howard, L. Fetter, R. Epworth, and D. Tennant, "Discrete Resistance Switching in Submicrometer Silicon Inversion Layers: Individual Interface Traps and Low-Frequency (1/f?) Noise," *Physical Review Letters*, vol. 52, no. 3, pp. 228–231, jan 1984.

[32] C. Marquez, N. Rodriguez, F. Gamiz, R. Ruiz, and A. Ohata, "Electrical characterization of Random Telegraph Noise in Fully-Depleted Silicon-On-Insulator MOSFETs under extended temperature range and back-bias operation," *Solid-State Electronics*, vol. 117, pp. 60–65, mar 2016.

[33] A. L. McWhorter, *1/f Noise and Germanium Surface Properties*. Semiconductor Surface Physics, 1957.

[34] G. Ghibaudo, O. Roux, C. Nguyen-Duc, F. Balestra, and J. Brini, "Improved analysis of low frequency noise in field-effect mos transistors," *physica status solidi (a)*, vol. 124, no. 2, pp. 571–581, 1991. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/pssa.2211240225

[35] G. Reimbold, "Modified 1/f Trapping Noise Theory and Experiments in MOS Transistors Biased from Weak to Strong Inversion—Influence of Interface States," *IEEE Transactions on Electron Devices*, vol. 31, no. 9, pp. 1190–1198, 1984.

[36] K. Hung, P. Ko, C. Hu, and Y. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors," *IEEE Transactions on Electron Devices*, vol. 37, no. 3, pp. 654–665, mar 1990. [Online]. Available: http://ieeexplore.ieee.org/document/47770/

[37] J. Jomaah, F. Balestra, and G. Ghibaudo, "Low frequency noise in advanced Si bulk and SOI MOSFETs," *Journal of telecommunications and information technology*, vol. 1, no. 1, pp. 24–32, 2005.

[38] T. A. Oproglidis, T. A. Karatsori, C. G. Theodorou, D. Tassis, S. Barraud, G. Ghibaudo, and C. A. Dimitriadis, "Origin of Low-Frequency Noise in Triple-Gate Junctionless n-MOSFETs," *IEEE Transactions on Electron Devices*, vol. 65, no. 12, pp. 5481–5486, dec 2018. [Online]. Available: https://ieeexplore.ieee.org/document/8494709/

[39] K.-s. Im, M. Siva Pratap Reddy, R. Caulmilone, C. G. Theodorou, G. Ghibaudo, S. Cristoloveanu, and J.-H. Lee, "Low-Frequency Noise Characteristics of GaN Nanowire Gate-All-Around Transistors With/Without 2-DEG Channel," *IEEE Transactions on Electron Devices*, vol. 66, no. 3, pp. 1243–1248, mar 2019. [Online]. Available: https://ieeexplore.ieee.org/document/8636409/

[40] S. Vodapally, C. G. Theodorou, Y. Bae, G. Ghibaudo, S. Cristoloveanu, K. S. Im, and J. H. Lee, "Comparison for 1/f Noise Characteristics of AlGaN/GaN FinFET and Planar MISHFET," *IEEE Transactions on Electron Devices*, vol. 64, no. 9, pp. 3634–3638, 2017.

[41] M. Hellenbrand, O. P. Kilpi, J. Svensson, E. Lind, and L. E. Wernersson, "Low-frequency noise in nanowire and planar III-V MOSFETs," *Microelectronic Engineering*, vol. 215, no. May, p. 110986, 2019. [Online]. Available: https://doi.org/10.1016/j.mee.2019.110986

[42] T. A. Karatsori, K. Bennamane, C. G. Theodorou, L. Czornomaz, J. Fompeyrine, C. Zota, C. Convertino, and G. Ghibaudo, "Static and Low Frequency Noise Characterization of InGaAs MOSFETs and FinFETs on Insulator," in *2018 48th European Solid-State Device Research Conference (ESSDERC)*. IEEE, Sep. 2018, pp. 166–169.

[43] E. Ioannidis, C. Dimitriadis, S. Haendler, R. Bianchi, J. Jomaah, and G. Ghibaudo, "Improved analysis and modeling of low-frequency noise in nanoscale MOSFETs," *Solid-State Electronics*, vol. 76, pp. 54–59, 2012.