Assessment of Frequency-induced Hysteresis Inversion in MoS$_2$ FETs

J. Cuesta-Lopez*, Mohit D. Ganeriwala, E. G. Marin, F. Pasadas, F. G. Ruiz and A. Godoy$^\sharp$

Dept. of Electronics and Computer Technology
University of Granada
Granada 18071, Spain
*jcuesta@ugr.es; $^\sharp$ agodoy@ugr.es

Abstract—**This work analyzes the combined effect of interface traps and mobile ions in the hysteretic performance of MoS$_2$-based FETs. Clockwise or anti-clockwise hysteresis is observed depending on the voltage sweep rate, evidencing the different underlying physical mechanism associated with the charge/discharge of interface traps and ion displacement. The memory window resulting from the device hysteresis is analyzed as a function of the operating frequency showing non-zero values for $0.1 < f < 10$ Hz (i.e. for the characteristic time of traps) and $f > 10$kHz (i.e the frequency-limited ion mobility). Both regions are separated by a frequency span where hysteresis is not present in the device response. The presented results constitute a first step towards a better understanding of the hysteretic behavior of iontronic devices and its potential application as analog memories.**

I. INTRODUCTION

With the widespread adoption of artificial-neural-network (ANN) based computing, the hardware realization of synaptic responses is at the forefront of the electronics research. Layered two-dimensional (2D) materials have added a twist to this exploration by promising extreme scalability and low power operation. Recently, a charge trap memory device based on a MoS$_2$ channel FET has been employed to implement a reservoir-computing based system for image classification [1]. In this case, the memory behavior arises due to the capture and emission of carriers by the traps located at the oxide-MoS$_2$ interface [2]. In contrast, another experiment has demonstrated a memory behavior mediated by the electric field driven ion migration in the amorphous gate oxide of a FET [3]. In both cases, the conductivity of the channel is modulated by applying a voltage pulse at the gate terminal which is manifested in the hysteresis of the transfer characteristics (I$_{ds}$-V$_{gs}$). To optimize the device performance as a component of future ANNs, it is indispensable to thoroughly analyze and understand its

hysteresis behavior. Most importantly, the input voltage sweep rate determines the time scale at which the hysteresis occurs, it modulates the channel conductivity and can be tuned in an analog fashion.

To partake the study, this work presents an *in-house* numerical tool that self-consistently solves the electrostatics and time-dependent electronic and ionic transport, along with the trapping/detrapping of carriers at the oxide-semiconductor interface. Our multi-scale approach enables the use of *ab-initio* techniques to estimate the MoS$_2$ density of states (DOS), required to calculate the channel charges. The validated simulation setup is then used to analyze the combined effect of the interface traps and mobile ions on the hysteresis behavior of the MoS$_2$ based FET.

II. METHODS

The numerical simulator self-consistently solves (1)-(3), i.e.: i) the Poisson equation describing the device electrostatics; ii) the time-dependent continuity equation for electron and holes, with the current described by the gradient of the pseudo-Fermi energy; and iii) the time-dependent continuity equation for ions with the ionic migration defined in terms of a Scharfetter-Gummel scheme [4].

$$\vec{\nabla} \cdot \left(\varepsilon \vec{\nabla} V \right) = -\rho \tag{1}$$

$$\vec{\nabla} \cdot \vec{J}_n = \vec{\nabla} \cdot \left[q\mu_n n \vec{\nabla} E_{F,n} \right] = +q\frac{\partial n}{\partial t} \tag{2}$$

$$\vec{\nabla} \cdot \vec{J}_i = \vec{\nabla} \cdot \left[-s_i q D_i e^{-z_i \Phi} \vec{\nabla} \left(c_i e^{z_i \Phi} \right) \right] = -z_i q \frac{\partial c_i}{\partial t} \tag{3}$$

where V is the electrostatic potential, ρ is the charge density, ε is the dielectric constant, $\vec{J}$ is the current density, q is the elementary charge unit, μ is the mobility, n is the electron density, E_F is the pseudo-Fermi energy level, t is the time, z is the ion valence with $s = |z|/z$ being the ion valence sign, c is the ion concentration, D is the diffusion coefficient, which follows the Einstein relationship $D_i = \mu_i k_B T/(z_i q)$, k_B is the Boltzmann constant, T is the temperature, $\Phi = qV/(k_B T)$ is the normalized potential, and the sub-indexes n and i denote electrons and each ion species, respectively.

The electron density in the channel is evaluated by using the density of states of MoS$_2$, $g(E)$, and Fermi-Dirac statistics,
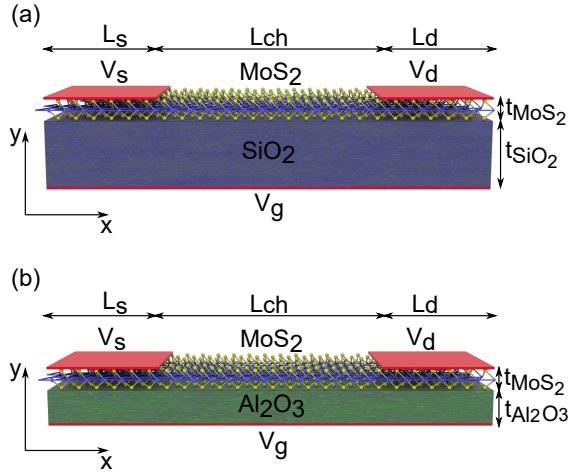
Fig. 1. Depiction of the simulated devices, a monolayer MoS$_2$-based back-gate FETs. (a) The experimental device employs a 90 nm-thick layer of SiO$_2$, while (b), the ferroelectric-like FET makes use of a 10 nm-thick layer of amorphous Al$_2$O$_3$. The lengths of source, channel and drain regions are L$_s$ = 50 nm, L$_{ch}$ = 100 nm and L$_d$ = 50 nm, respectively.

Fig. 2. Comparison between experimental data (symbols) from [5] and simulated data (solid lines). Gate bias was swept from V$_{gs}$ = 20 V to V$_{gs}$ = -20 V with a sweep rate of 2 V/s. The drain voltage was set to V$_{ds}$ = 0.1 V (red), 0.3 V (green), 0.5 V (blue). The device width is assumed to be W = 680 μm. Inset: Interface charge trapped density (cm^{-2}) at the middle point of the channel length.

$f(E)$, and integrating over all energies above the bottom of the conduction band edge, E_c:

$$n = \int_{E_c}^{+\infty} g(E)f(E)dE. \tag{4}$$

III. EXPERIMENTAL VALIDATION

The suitability of the *in-house* simulator was tested by benchmarking it against the experimental measurements presented in [5]. The simulated device architecture is depicted in Fig. 1(a), with its geometrical and material parameters summarized in Table I. A MoS$_2$ monolayer, with thickness t$_{MoS_2}$ = 0.65 nm, lays on top of a t$_{SiO2}$ = 90nm-thick SiO$_2$, with a 200 nm-long back-gate. The channel effective length is L$_{ch}$ = 100 nm, with top source and drain contacts regions of length L$_s$ = L$_d$ = 50 nm. Electron mobility was scaled down by a factor 1/10 to account for the device channel length reduction from L$_{ch}$ = 1 μm to L$_{ch}$ = 100 nm (aiming to decrease the computational burden). More details about the device fabrication can be found elsewhere [5]. Interface traps are considered at the oxide-semiconductor junction. According to reported experimental measurements [6], traps at the SiO$_2$/MoS$_2$ interface are donor-like (i.e., neutral when occupied and positively charged when unoccupied through the emission of an electron). For this device, they were assumed to be present in a concentration of D$_{it}$ = 10^{13} eV^{-1}cm^{-2}, spreading through a thickness of 1 nm close to the interface, and uniformly distributed along all energy levels located inside the MoS$_2$ bandgap. The capture and emission time constants were set to τ_c = 5 s and τ_e = 2.5 s, respectively. The MoS$_2$ density of states, $g(E)$, and its bandgap, E_g = 1.73 eV, were evaluated using the density functional theory (DFT) as implemented in Quantum ATK [7]. In particular, the calculations are carried out using Generalized Gradien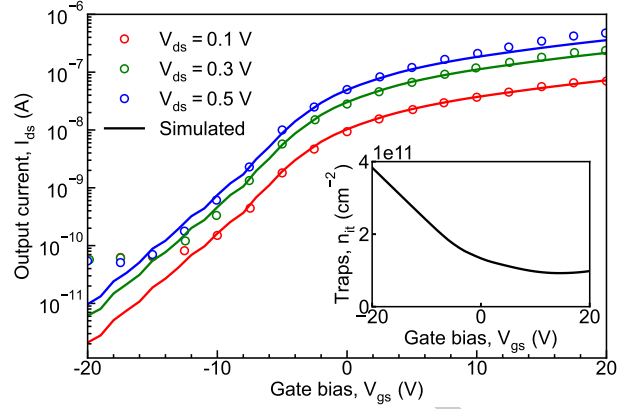t Approximation (GGA) with the LCAO basis and the Perdew-Berke-Erzenhof exchange-correlation functional with norm-conserving SG15 pseudo-potential. Brillouin-zone integration was performed over Monkhorst-Pack Grid of $10 \times 10 \times 1$ for structural optimization and $17 \times 17 \times 1$ for DOS calculation. A sufficiently large energy cutt-off of 250 Ry was used and the resultant forces are minimized to be less than 0.01 eV/Å.

The transfer characteristics depicted in Fig. 2 demonstrate very good agreement between experimental and simulated data, thus proving the potential of the developed numerical tool. The gate bias was swept from V$_{gs}$ = 20 V to V$_{gs}$ = -20 V, with a voltage sweep rate of 2 V/s . Three different drain voltage values were set, namely V$_{ds}$ = 0.1 V, 0.3 V, and 0.5 V. The inset depicts the density of the charge trapped measured at the middle point of the channel length. High positive values of V$_{gs}$ help the occupation of traps, while negative values of V$_{gs}$ stimulate the emission of electrons, leaving positively charged donor-like traps behind them.

IV. RESULTS AND DISCUSSION

As reported in [5], traps present in the device were responsible for hysteresis at slower sweeps rates. Here, we use this calibrated simulation setup to provide further insights in the hysteresis by adding the effect of mobile ions present in amorphous oxides, along with the effect of interface traps, whose time constants remain on the order of seconds. To

TABLE I
GEOMETRICAL AND MATERIAL PARAMETERS OF THE SIMULATED
DEVICES SHOWN IN FIG. 1.

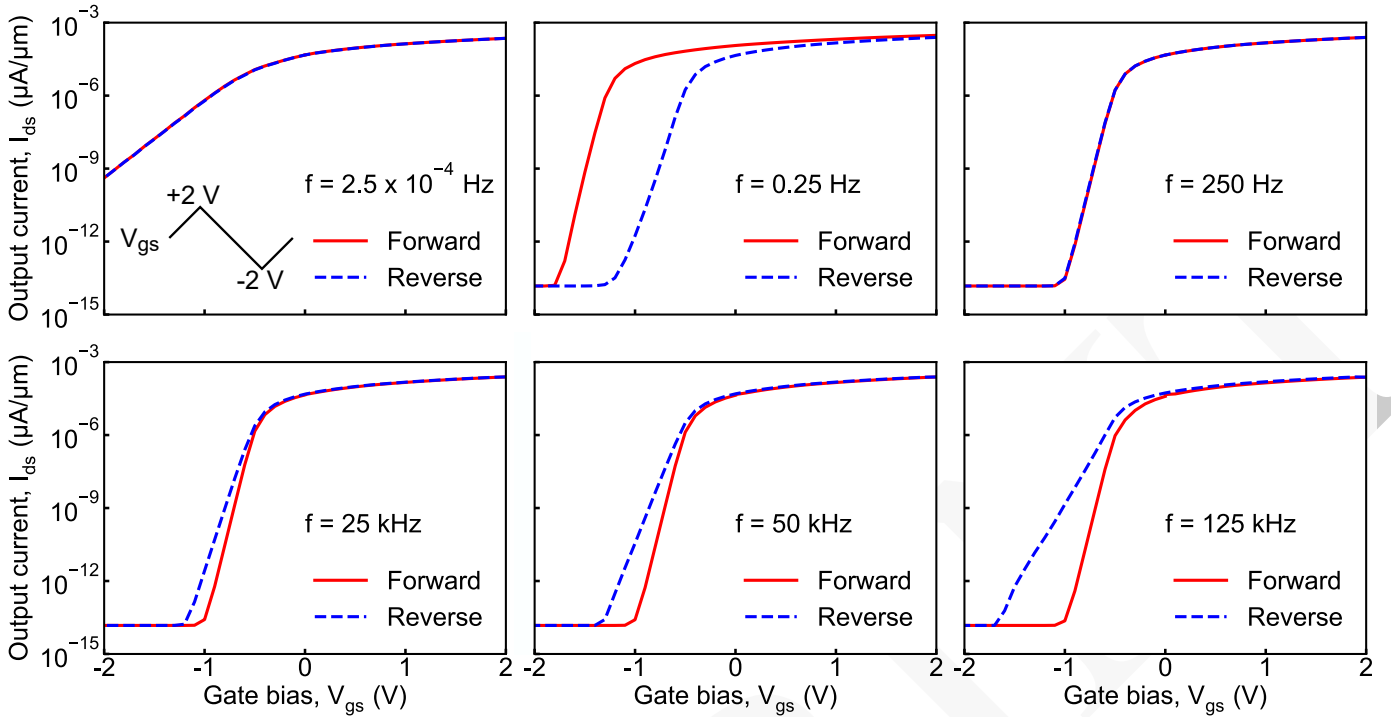| Geometry parameters	L$_s$, L$_d$	L$_{ch}$	t$_{MoS_2}$	t$_{SiO_2}$	t$_{Al_2O_3}$
	50 nm	100 nm	0.65 nm	90 nm	10 nm
Material parameters	μ_n	E$_{g_{MoS_2}}$	ε_{MoS_2}	ε_{SiO_2}	$\varepsilon_{Al_2O_3}$
	$\frac{1.5}{10}$ ($\frac{cm^2}{Vs}$)	1.73 eV	7.6	3.9	9
Ions and traps	c$_i$	μ_i	D$_{it}$	τ_c	τ_e
	10^{17} cm^{-3}	10^{-12} $\frac{cm^2}{Vs}$	$\frac{10^{13}}{eVcm^2}$	5 s	2.5 s

Fig. 3. Transfer characteristics simulated at different sweep frequencies for triangular gate bias pulses. Forward sweeps (red solid lines) were performed from V_{gs} = -2 V to V_{gs} = +2 V, while reverse sweeps (blue dashed lines) were applied from V_{gs} = +2 V to V_{gs} = -2 V, as depicted in the top left schematic. The applied drain voltage was set to V_{ds} = 0.1 V in all cases. Clockwise hysteresis appears for low frequencies, while anti-clockwise hysteresis manifests for high frequencies, both behaviors separated by a region of no hysteresis.

carry out this study, the device architecture presented in Fig 1(b) substitutes the SiO_2 gate oxide by an amorphous layer of Al_2O_3 with thickness $t_{Al_2O_3}$ = 10 nm. Amorphous alumina is known to contain a high intrinsic concentration of ionized defects, i.e. oxygen ions (O^{2-} anions) and oxygen vacancies (V_O^{2+} cations) [8]. The mobility and concentration of both ionic species are set to $\mu_i = 10^{-12}$ cm^2/Vs and $c_i = 10^{17}$ cm^{-3}, respectively [9], [10]. Thus, oxygen ions and vacancies are able to drift and diffuse confined to the insulator Al_2O_3 region under the effect of an electric field.

A triangular gate bias pulse between V_{gs} = -2 V and V_{gs} = +2 V, with a fixed drain voltage of V_{ds} = 0.1 V was applied, and the sweep rate modified to assess the influence of traps and ions at different operating frequencies.

As shown in Fig. 3, each frequency yields a characteristic device response. For $f = 2.5 \times 10^{-4}$ Hz, both traps and ions are able to react according to the gate bias, avoiding the hysteresis in the I-V characteristic. For f = 0.25 Hz, the delay in the response of interface traps gives rise to a clockwise hysteresis loop (in good agreement with the literature [6]). For a forward sweep (starting at V_{gs} = -2 V), interface traps are unoccupied and positively charged, thus producing a lower threshold voltage, V_T, than the one measured during a reverse sweep (starting at V_{gs} = +2 V), where traps are occupied and neutral. For this frequency, ions move with no delay with respect to the applied bias. Next, for higher frequencies, interface traps do not follow anymore the applied signal while ions keep on

moving gently with it. Hysteresis appears again for frequencies above 25 kHz with anti-clockwise direction. This is caused by voltage-driven ion migration. In fact, a scenario departing from $V_{gs} > 0$ V will drive oxygen vacancies next to the MoS_2 interface, decreasing V_T with respect to a situation where the starting point is $V_{gs} < 0$ V, in which oxygen ions are closer to the MoS_2 interface and V_T is increased. The dynamics of traps and ions for different frequencies are clearly depicted in Fig. 4.

Although the particular frequencies defining the clockwise and anti-clokwise hysteresis, as well as the frequency bandgap separating these two behaviors, are specific for the time constant of the traps and the mobility and concentration of ions considered here, the results reveal the following conclusion. Traps and ions: i) initially follow the applied signal with no delay for very low frequencies (but with different frequency thresholds); ii) are out of phase with the applied bias (i.e. creating hysteresis) for a particular range of frequencies that will depend upon the the characteristic time constant of the traps and the values of c_i and μ_i for the ions; and iii) will eventually not respond to very fast stimuli, losing totally the hysteretic behavior. Consequently, the collapse and the eventual inversion of the hysteresis is obtained.

To get further insights into the frequency dependence of the hysteresis, we calculate the evolution of the device threshold voltage (V_T) defined as the gate voltage required to achieve an output current of $I_{ds} = 10^{-6}$ µA/µm. When the device
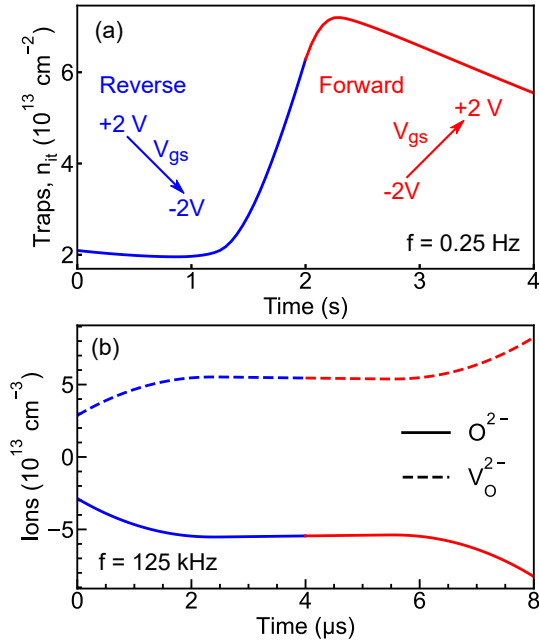
Fig. 4. (a) Evolution of interface charged trap density, n_{it} (cm^{-2}), according to a V_{gs} sweep applied with a frequency of 0.25 Hz. (b) Variation of ion density with respect to the initial concentration ($c_i = 10^{17}$ cm^{-3}) after the application of a V_{gs} sweep with a frequency of 125 kHz, for both oxygen ions (O^{2-}, solid lines) and vacancies (V_O^{2+}, dashed lines). All data were measured at the middle point of the Al_2O_3/moS_2 interface. Blue refers to a reverse sweep (from +2V to -2V), while red depicts a forward sweep (from -2V to +2V).

Fig. 5. (a) Memory window, MW, and (b) threshold voltage, V_T, measured at $I_{ds} = 10^{-6}$ µA/µm, for different operating frequencies. A negative MW is issued from V_T^{for} being lower than V_T^{rev}, resulting in clockwise hysteresis. On the contrary, a positive value of MW is originated by $V_T^{for} > V_T^{rev}$, corresponding to the device exhibiting anti-clockwise hysteresis. The fact that MW = 0 V and $V_T^{for} = V_T^{rev}$ means that there is no hysteresis.

exhibits hysteresis, two different values of V_T can be measured depending on the direction of the voltage sweep, namely, a forward (V_T^{for}) or reverse one (V_T^{rev}). The difference between both threshold voltages is defined as the Memory Window (MW): MW = V_T^{for} - V_T^{rev}. Fig. 5 depicts the variation of MW and $V_T^{rev/for}$ as a function of the operating frequency. For f around 0.1 Hz a minimum for the MW is found, with a negative value, meaning that $V_T^{for} < V_T^{rev}$ and their separation is maximum. For $f \in [100, 1000]$ Hz, there is no hysteresis, namely, MW = 0 V and $V_T^{for} = V_T^{rev}$. Finally, for f higher than 20 kHz, anti-clockwise hysteresis is clearly exhibited, a phenomenon that translates into $V_T^{for} > V_T^{rev}$ and MW > 0 V. The memory behavior of the device could, therefore, be changed in an analog fashion by modulating the sweep rate of the input signal, with possibility of obtaining both positive and negative memory windows.

V. CONCLUSIONS

This work analyzes the combined effect of interface traps and mobile ions in the hysteretic performance of MoS_2-based FETs. This study is carried out thanks to an *in-house* numerical simulator specifically designed to incorporate the combined influence of both traps and ions on the current-voltage characteristic of these devices. The analysis of different sweep rates for the applied gate bias disentangle the innate role played by charged traps and mobile ions on the hysteresis behavior depicted by the device, with the trap time constants and the ion mobility and concentration determining the range of sweep
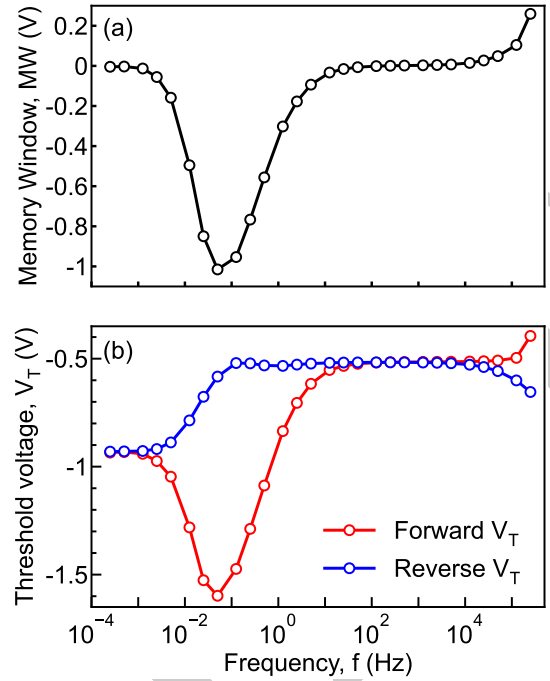
frequencies displaying hysteresis and their clockwise or anti-clockwise feature.

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