Flexible Laser-Induced Graphene Memristor: Fabrication and SPICE based Emulation of an Artificial Neural Network

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***Abstract*—This work demonstrates laser-induced graphene memristors, fabricated using a patterning-free, low cost and simple process directly on a flexible polyimide substrate. The fabricated memristors show repeatable non-volatile bipolar resistive switching with state retention up to 10^3 seconds. A simple perceptron network for the classification of black-and-white images is later implemented using an experimentally extracted compact model. Successful training of the network by integrating SPICE model with MATLAB shows the possibility to emulate the on-chip learning process. Further, by properly modulating the applied voltage pulse amplitude and period, a reduction in the energy consumed by training the neural network is achieved.**

I. Introduction

Artificial Intelligent (AI) systems should be able to carry out tasks similar to those routinely performed by living organisms. Aiming at this ultimate goal, a neuromorphic system designed to implement brain-like artificial neural networks (ANNs) should sit at the intersection of the sensors and the computing, providing massively parallel and robust computing ability while operating at very low power [1]. Towards this end, two-terminal memristors able to mimic the event driven synaptic plasticity, are expected to become a crucial component in the realization of the future ANNs. With the additional feature of the extreme area scaling provided by the two-dimensional materials (2DMs), ANNs based on memristive synapse implemented in a cross-bar configuration could also be able to achieve the massive high density of biological neural networks [2].

Currently, considerable research efforts are directed towards the experimental demonstration of 2DM-based memristors; nevertheless, their fabrication routinely involves the use of high-temperature, time consuming and multi-stepped chemical synthesis processes, constraining the experimental exploration in this field to high-tech facilities [3]. Recently, Laser-Induced Graphene (LIG) has emerged as a cost-effective alternative technique for the production and patterning of graphene films using commercial laser machines on flexible substrates [4]. LIG with high electrical conductivity (25 $S{\cdot}cm^{-1}$) and good thermal stability ($>$ 900 ºC) [4], [5] has already been demonstrated for numerous flexible electronic applications such as sensors and supercapacitors.

Here, we report a prototype of an LIG non-volatile memristor on a commercial flexible polyimide substrate. The process used here provides high-control of the fabrication and the induced graphene parameters, while the absence of any precursor and patterning mask provides a substantial simplification of the process, reducing considerably the manufacturing time and cost.

To further demonstrate the ability of the fabricated LIG memristors to implement the weight of an ANN, we have design the ANN crossbar in an SPICE-level simulation. In more detail, by interfacing the SPICE of Pathwave Advanced Design System (ADS)® with MATLAB®, it is possible to emulate the real time on-chip learning of hardware ANNs. Such a setup offers the possibility to further add the peripheral components needed to implement the ANN circuitry, and allows the estimation of the energy consumption of in-situ training. We show that, by exploiting the inherent dependency of the memristors conductance on both the frequency and the amplitude of the applied voltage pulses, the energy requirements of the ANN training can be reduced.

II. Methodology

Figure 1a shows a schematic representation of the LIG memristor fabrication process. A laser is used to engrave a flexible polyimide substrate (Kapton® sheet, DuPont™ 300HN). The highly localized heating, induced by the laser, breaks and rearranges the polyimide bonds, producing a chain of carbon atoms, resembling the 2D graphene. Both the top and the bottom surfaces of the polyimide sheet are engraved, with laser power tuned to keep a thin insulating layer in between, as depicted in Fig. 1b. An Everbeing® C-4 Probe Station

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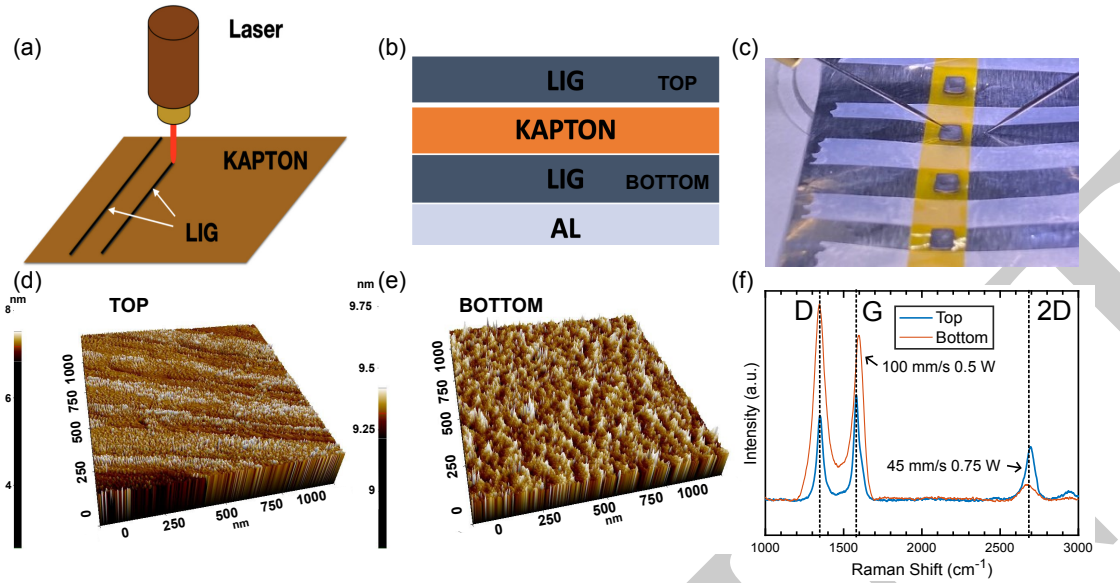


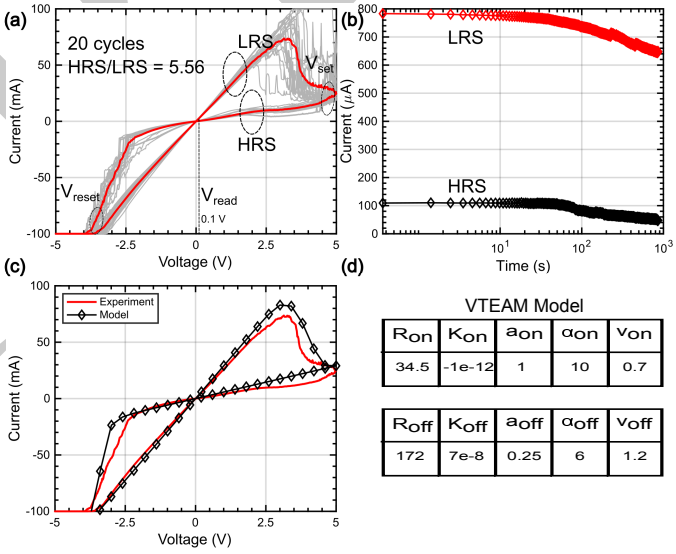
Fig. 1. (a) Schematic of the patterning process on Kapton® polyimide sheets, (b) Stack layer scheme of the proposed LIG memristor, (c) Measurment setup of the fabricated devices with Al bottom and and Tungsten probes as top electrodes respectively, AFM image of the LIG morphology of the (d) top and (e) bottom layer and (f) Raman spectra for top and bottom LIG region engraved with different laser intensity.

connected to a Keithley ® 4200A-SCS parameter analyzer is used for the electrical measurements. The bottom section of the LIG is contacted using an Aluminium sheet, while the tungsten electrode of the probe station acts as the top contact, Fig. 1c. The laser power and velocity were modulated to adjust the properties of the LIG, as can be seen from the measured Raman spectra, Fig. 1f. The higher intensity applied to the top surface results in LIG with D and G peaks narrower than the bottom surface, where a lower laser intensity was used, while the 2D peak increases in magnitude for the higher intensity and lower velocity sample. This signifies a reduction of oxygen content and structural defects, corresponding to the production of few layer graphene [6].

III. Results and Discussion

Figure 2a depicts the electrical characterization of the non-volatile LIG memristors for 20 repeated I-V sweeps (grey lines). A repeatable bipolar resistive switching is obtained from the initial high resistive state (HRS) to a low resistive state (LRS) after the voltage reaches a set voltage $V_{set} \approx 4.5$ V. The memristor retains its state for the changing voltage polarity, and switches back to the HRS after a negative reset voltage $V_{reset} \approx -3$ V. The resistive switching ratio (HRS/LRS), calculated using the median I-V curve (red), is ≈ 5.56. Fig. 2b proves the capability of the LIG memristors to retain the resistance value at least up to 10^3 seconds.

Next, the VTEAM compact model [7] is used to match the experimental data (Figure 2c), showing an excellent agreement between the model and experiments. The model parameters are included in Figure 2d. The Verilog-A code of the model is integrated into the SPICE of the Advance Design System (ADS), to implement the memritive crossbar schematically



R_{on}	k_{on}	a_{on}	α_{on}	v_{on}
34.5	-1e-12	1	10	0.7

R_{off}	k_{off}	a_{off}	α_{off}	v_{off}
172	7e-8	0.25	6	1.2

Fig. 2. (a) I-V measurements for 20 consecutive cycles (gray line). The red line shows the median data, (b) Measurements showing 10^3 s of retention time for high- and low-resistance states and (c) VTEAM model fitting for the median experimental data, with (d) the corresponding model parameters.

shown in Fig. 3a (the dots correspond to the memristor position).

In the quest for potential applications of the fabricated LIG memristor, circuit simulations are carried out to emulate the in-situ learning process of an ANN. As a reference, one of the earliest hardware implementation of memristor based ANN [8], which implements a single-layer perceptron network with 10 inputs and 3 outputs, was selected. Despite its simplicity, this ANN is able to classify 3×3 pixel black and white images

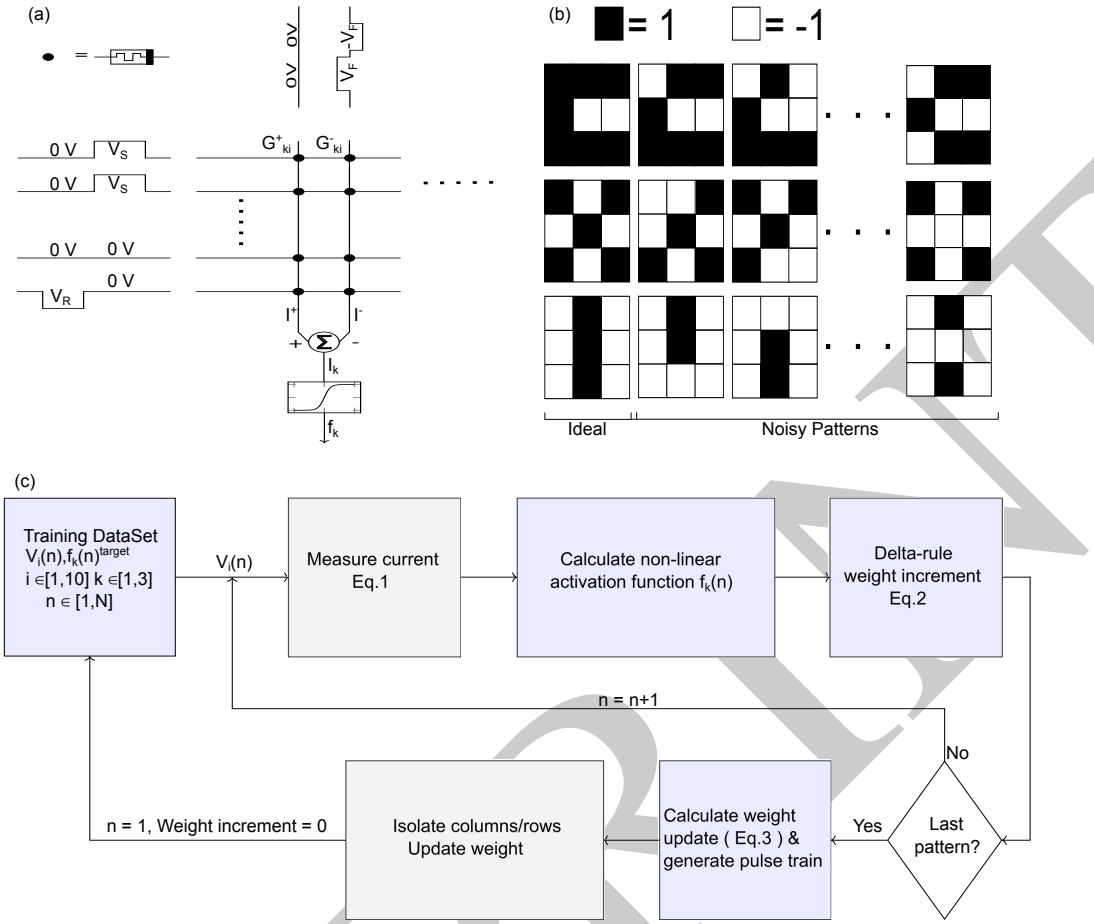


Fig. 3. (a) Schematic of the memristive crossbar pair, activation function, and the input pulses scheme to change state of the memristors in the first column, (b) Ideal and noisy input patterns, and (c) Flow chart of the algorithm for training the ANN using SPICE (Gray boxes) implemented in ADS, and Blue boxes implemented in MATLAB.

into three different classes ($k = 1, 2, 3$). The input image set consists of 1 correct and 10 noisy versions of Latin alphabets C, X and I, making a total of N = 33 different input patterns, as represented in Fig. 3b. Each image (n) is divided into 3×3 grid resulting into 9 pixels per image, which are coded into 9 voltage inputs (v_i). A bias voltage is also applied, resulting into a 10 rows (i) crossbar network.

A flowchart representing the network training is schematized in Fig. 3c, where the blocks in grey are implemented in ADS, while those in blue are implemented in MATLAB. At each epoch of the training loop, one image of the set is applied to the network, which performs the multiply and accumulate operation:

$$i_k = \sum_{i=1}^{10} W_{ki} v_i(n), \quad W_{ki} = G^+_{ki} - G^-_{ki} \tag{1}$$

Here, each synaptic weight W_{ki} is represented by a differential pair of memristors with conductance (G^+_{ki} and G^-_{ki}), leading to a total of 60 memristors. By measuring the current through each column in ADS, the output of Eq. (1) is evaluated. The output of the neuron corresponding to each class, k, is calculated using a nonlinear activation function, $f_k = \tanh(\beta \mathrm{i_k})$, where β is the scaling factor. Based on the gradient descent optimization algorithm, the delta-rule weight increment, Δ_{ki}, is obtained for each image (n) as:

$$\Delta_{ki} = \delta_k(n) v_i(n) \tag{2}$$

with

$$\delta_k(n) = [f_k(n)^{\mathrm{target}} - f_k(n)] \frac{\partial f}{di}_{|i=i_k(n)} \tag{3}$$

Once the N patterns are applied, the synaptic weight modification ΔW_{ki} is calculated using the Manhattan update rule:

$$\Delta W_{ki} = \eta \cdot \mathrm{sgn} \sum_{\mathrm{n}=1}^{\mathrm{N}} \Delta_{\mathrm{ki}} \tag{4}$$

where η is the rate constant. Setting it to 1.6%, approximately 60 different resistance levels are achieved. Once the desired ΔW_{ki} is calculated, the appropriate voltage pulse is generated through MATLAB and fed into ADS. The memristor weights are updated in two steps for each column. First, all the memristors in a column whose weights need to be incremented are simultaneously biased with a voltage difference of $V_S > V_{\mathrm{set}}$ and, in a second step, those memristors whose weights

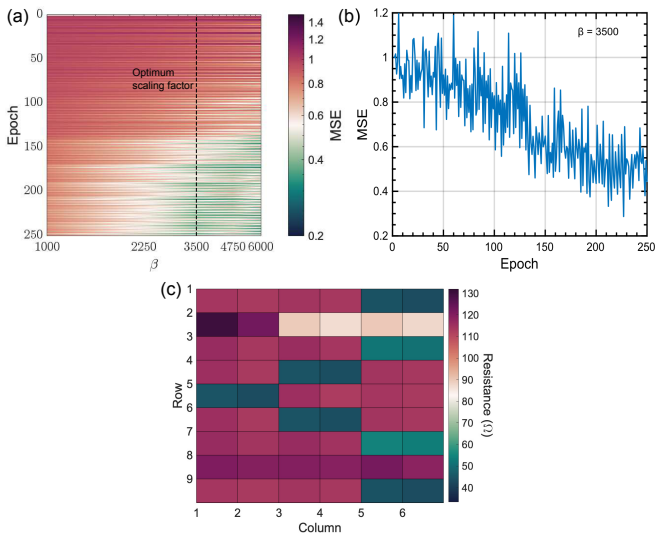


Fig. 4. Mean Square Error (MSE) averaged over each image class (a) as a function of the scaling factor (β) and epochs and (b) as a function of epoch for the optimum β of 3500 and (c) Matrix showing the resultant resistance values after the final epoch. All results are for pulse width of T = 10 ms

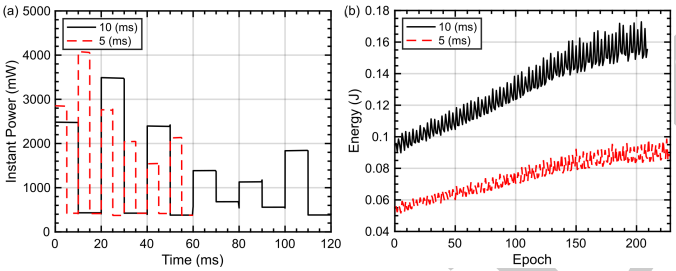


Fig. 5. (a) Instantaneous power consumption for last epoch for pulse widths of 10 ms (solid black) and 5 ms (red dashed) and (b) Energy dissipated at each epoch until 100% of patterns are classified.

need to be decreased are biased with a voltage difference of $|V_R| > |V_{\text{reset}}|$. In order to isolate a column (such that all other memristors remain unchanged) a fixed bias of $\pm V_F$ is applied respectively during the increment and the decrement step such that the voltage difference i.e. $|V_F|, |V_S - V_F|$ and $|V_R - V_F|$, is lower then both V_{set} and $|V_{reset}|$ as shown in Fig. 3. In order to reduce the computational cost, a pulse train is generated so that the weight of the entire crossbar is updated in a single ADS run.

Figure 4 represents the results achieved from the network training for 250 epoch. First, an optimum β value is selected so as to get an acceptably low mean square error (MSE $= \frac{1}{N}\sum_{n=1}^{N}[f_k(n)^{\text{target}} - f_k(n)]^2$. Accordingly, a $\beta = 3500$ is chosen, which is marked by the vertical dashed line in Fig. 4a. An evaluation of the MSE averaged over k per epoch is shown in Fig.4b. The resistance matrix of the crossbar after 250 epoch is also depicted in Fig. 4c. As demonstrated, the ADS+MATLAB interface is able to emulate the in-situ training of a memristor based ANN hardware.

As the conductance change of the memristor depends on both the period (T) and the amplitude (V_S, V_R) of the applied voltage input, this feature is exploited here in order to optimize the ANN training power consumption. Two different sets of parameters for the training pulse trains are considered: (a) T = 10 ms, $V_S = 4.66\ V$, $V_R = -3.34\ V$; and (b) T = 5 ms, $V_S = 5.08\ V$, $V_R = -3.63\ V$. Since both pulse trains produce the same conductance modification, there is no difference in the network training and the same MSE is achieved with both of them. However, they result into very different amount of power consumed by the network. Fig. 5a shows the instantaneous power consumed by the network during the final epoch. Calculating the energy consumed per epoch proves that a reduction of the pulse width, which demands only a slight increment of the applied voltage, results into a shrinkage of the the total energy consumed by the network during its training, emphasizing the relevance of the proper selection of V_S, V_R and T.

IV. Conclusions

A laser-induced-graphene memristor, fabricated using a patterning-free process on a flexible polyimide substrate, was shown to have repeatable non-volatile bipolar resistive switching characteristics. A compact model matched to the experimental data was subsequently used to implement and train an ANN, for black and white image classification. Interfacing SPICE model with MATLAB opens the possibility of emulating the on-chip learning process. Further, by exploiting the setup, and modulating the input pulse period and amplitude a reduction in the energy consumption during the training process is achieved.

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