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PH.D THESIS

Low-cost soft-error hardened D-Latch in nano CMOS technology

Doctoral Programme in Information and Communication Technologies

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Palabras clave: Hardened D-latch; Complementary Metal Oxide Semiconductor technology (CMOS technology); Power-Delay Product (PDP); Soft Error (SE); Single Event Upset (SEU); High Impedance State (HIS); Single Event Transient (SET), Dual Interlocked Storage Cell (DICE), Triple Path DICE (TPDICE), Quadruple-Node Upsets (QNUs), Delay-Power-Area Product (DPAP).

Resumen:
En un entorno hostil con una enorme radiación como la del espacio, la parte de memoria de los circuitos electrónicos, como los biestables D puede perder sus valores almacenados y volverse más vulnerable a eventos de alteración de múltiples nodos (*multiple node upsets*, MNU). Para abordar este problema, los chips integrados de un sistema aeroespacial deben diseñarse con un alto nivel de confiabilidad contra errores leves. Un fallo puede provocar el mal funcionamiento de los módulos o sistemas de un cohete, de una nave espacial o de un satélite en entornos hostiles, poniendo en riesgo estos equipos y vidas humanas. Además, es necesario reducir la tecnología para aumentar la potencia de procesamiento y la densidad de integración, pero al hacerlo, no nos podemos olvidar de seguir manteniendo la confiabilidad de los circuitos; en particular, en los nodos de biestables D a nanoescala se pueden producir errores de alteración de múltiples nodos cuando funcionan en entornos radiactivos hostiles. Por lo tanto, es necesario diseñar módulos de almacenamiento autorecuperables capaces de realizar cálculos altamente confiables en cualquier situación en el espacio exterior. Esta tesis aborda así el diseño de un biestable D tolerante a errores en un nodo, a errores en dos nodos y a errores en cuatro nodos, proponiendo así un nuevo biestable D robusto, de bajo coste, alta confiabilidad y autorrecuperabilidad usando para ello una estrategia de diseño adecuada.

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Keywords: Hardened D-latch; Complementary Metal Oxide Semiconductor technology (CMOS technology); Power-Delay Product (PDP); Soft Error (SE); Single Event Upset (SEU); High Impedance State (HIS); Single Event Transient (SET), Dual Interlocked Storage Cell (DICE), Triple Path DICE (TPDICE), Quadruple-Node Upsets (QNUs), Delay-Power-Area Product (DPAP).

Abstract:
In a harsh environment with huge radiation as space, the memory part of electronic circuits, such as D-latches, can lose their stored values and become more vulnerable to multiple node upsets (MNUs) events. To tackle this issue, the on-board chips of aerospace system have to be designed with a high-level reliability against soft errors. One failure can cause the malfunction of modules or systems of a rocket, spacecraft, or satellite in harsh environments putting equipment and lives at risk. Also, scaling down the technology is necessary to boost processing power and density of integration, but in doing so keeping the reliability of circuits is a concern that cannot be neglected; in particular, D-latches nodes at nano-scale confront multiple-node upset errors when they are operated in harsh radiative environments. Therefore, it is mandatory to design self-recoverable storage modules capable of highly-reliable computing under any outer space situation. This thesis addresses the design of a single-node-upset, double-node-upset, and quadruple-node-upset tolerant D-Latch, which is a new approach of hardened D-latch featuring low-cost, high-reliability, and self-recoverability under the proper design strategy.

Declaration of Authorship

I, Seyedehsomayeh Hatefinasab, as Ph.D. Candidate under the Doctoral Program in Information and Communication Technologies of the University of Granada, I authorize the location of the following copy of the Doctoral Thesis in the library of the center so that can be consulted by people who want it.

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Granada, 6th October 2023

D. **Noel Rodríguez Santiago**, Full Professor of the the Department of Electronics and Computer Technology at the University of Granada.

Dña. **Encarnación Castillo Morales**, Professor Department of Electronics and Computer Technology at the University of Granada.

Declare:

That the research entitled **Low-cost Soft-Error Hardened D-Latch in Nano CMOS Technology** has been conducted under our supervision by Mrs. **Seyedehsomayeh Hatefinasab**, a Ph.D. Candidate enrolled in the Doctoral Program in Information and Communication Technologies at the University of Granada.

Throughout the course of this research, proper acknowledgment has been given to other authors by citing their publications and findings whenever they have been utilized. We grant authorization for the defense of the aforementioned work in front of the appropriate academic tribunal.

This statement is issued and undersigned in Granada, in the month of October 2023.

The supervisors:

Noel Rodríguez Santiago

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Thanks a lot, to my mother, brother and sisters, even from long distance our heart are connected to each other.

Contents

List of Figures

List of Tables

Part I. Introduction

Chapter 1

Introduction

In the contemporary era, electronic devices have pervaded all facets of our lives; exemplars include mobile phones, computers, tablets, and the like, with their numbers poised to continuously surge. As technology scales down, it becomes imperative to enhance processing power and integration density. Yet, this progression must be juxtaposed with the imperative of circuit reliability. The downsizing of transistors, integral to scaling, results in the concomitant reduction of node capacitors. In order to uphold electrostatic integrity and manage power dissipation, the supply voltage is reduced. Both these factors augment circuit susceptibility to particle-induced charge. The accumulation of particle-induced charge can instigate transient faults, manifested as single event transients (SETs). Moreover, a single event upset (SEU) may arise from an SET traversing combinational logic circuits and subsequently impinging on sequential circuits, such as flip-flops or latches [1].

The D-latch constitutes a pivotal component of sequential digital systems. The design of VLSI circuits mandates meticulous consideration of various factors for D-latches, encompassing high performance, transistor count, reliability, power-delay, and power-area ratios. The operational frequency of digital circuits is chiefly bounded by the D-latches. Notably, D-latches and clock distribution networks account for a substantial fraction of chip power consumption, while an escalated transistor count results in larger chips or increased manufacturing costs. Given that latches are deployed for data storage, their reliability holds paramount importance across various circuit states, even in the presence of glitches or significant charge injection into internal nodes. This concern has fostered the introduction of novel latch designs commonly known as hardened latches.

Extensive research endeavors have been devoted to the hardening of latches, often achieved by augmenting their basic designs with additional transistors [2-6]. Four categories of hardened latches exist based on their immunity against SEU, SET

filtering, and HIS sensitivity. The first category encompasses latches that can tolerate SEU in certain nodes but are not fully SEU-immune; such latches may incur corruption of values following particle strikes. The second category encompasses latches fully tolerant against SEU yet unable to filter SET at their inputs, potentially leading to a high-impedance state at the output node. The third category comprises latches that are fully immune against SEU, devoid of high-impedance states in output nodes, albeit unable to filter input SET. Finally, the fourth category features latches fully immune against SEU, lacking high-impedance states at output nodes, and possessing the ability to filter input SET.

In the design of hardened latches, myriad parameters demand consideration: power consumption, (D-Q) propagation delay, and Power-Delay Product (PDP), immunity against SEU and SET, temperature dependence, process variability, area penalty.

Recent research has placed emphasis on single event double-upset (SEDU), arising from the injection of multiple charges into different internal nodes of latches or flip-flops [7-8]. This concern has gained prominence with the advent of nano-scale transistor technology in the sub-nanometer range. Several hardening strategies have been proposed, encompassing node spacing increase, guard rings, multiple-modular redundancy, and well isolation.

The ensuing sections furnish an overview of diverse designs of hardened D-latches, including the subsequent types: Low-Cost and highly Reliable Radiation-hardened latch (LCHR latch), Circuit and Layout Combination Technique latch (CLCT latch), Double Node charge sharing-Soft error interception latch (DNCS-SEI latch), and triple Path DICE latch (TPDICE-based latch).

The LCHR latch employs Schmitt trigger inverters' hysteresis property to filter SET. It utilizes three loops for data retention and SEU tolerance, aligning with the first category of hardening latches previously described [1].

The CLCT latch leverages Clocking-Gate (CG) technology, featuring no active feedback loops within the Dual Interlocked storage Cell (DICE). The transparent mode employs a keeper, rendering it a power-efficient solution. In latching mode, the data of DICE and keeper counteract SEU or SEDU. As DICE and the keeper are linked to a Triple-input Muller C-element (TMCE), the output may adopt a high-impedance state. However, this D-latch is not entirely immune against SEDU [6].

The DNCS-SEI latch is fully SEU-immune, with each triple-input Muller C-element (TMCE) capable of blocking SEU. TMCE can self-recover due to the loop. In cases where SEDU impacts both TMCE inputs and information recovery is not

possible, the keeper can prevent a high-impedance state at the output (Q). Additionally, if SEDU affects the loop and the Q node, the latch can remain immune and self-recover. However, this latch cannot filter SET, and its extended loop and greater number of additional transistors contribute to higher power consumption [5].

The TPDICE-based latch is entirely immune against SEDU and SEU, while also capable of filtering SET at the input [8]. It comprises a TPDICE for data storage and a TMCE for SEDU tolerance. A keeper thwarts the output node from entering a high-impedance state, and a Schmitt Trigger Inverter (STI) filters SETs from combinational gates at the preceding stage of the D-latch [8].

1.1 Objectives

The main objective of this Doctoral Thesis is to study the behaviour and to develop harden latches required for an emerging nano-electronics nodes. This objective also can be applied for the detailed analysis of the advantages/challenges of using memory cells or flip flops at the forthcoming nanotechnology scale.

The main objective can be split in five specific objectives, with main focus on third and fifth objectives:

1. Node sensitivity analysis in D-latches based on subcircuits and transistors.
2. Exploration of single node upset (SNUs), double node upset (DNUs), triple node upset (TNUs), quadruple node upset (QNUs) in dynamic D-latch circuits.
3. Designing the D-latch to achieve optimum performance over the whole operating states in terms of minimum power dissipation, delay and highly reliable.
4. Verify the theoretical analysis by software and available tools.
5. Validation of the prototype considering final application requirements in terms of: efficiency, size, reliability against supply voltage and temperature or process variations.

1.2 Thesis outline

This thesis is presented as a compendium of articles. The structure of Articles is the following:

- **Publication I**: This publication covers the low-cost hardened SNU with high reliability against of temperature and process variations, such as (W/L) and threshold voltage transistor variability. Also, other previous SNU tolerant D-latch is explained and compered with them.

- **Publication II**: This publication covers QNU tolerant D-latch (HRQNU) with high reliability against process variations, such as threshold voltage and (W/L) transistor variability. Also, this D-latch can mask single event transients in the transparent mode. Also, other previous QNU tolerant D-latch is explained and compered with them.

- **Publication III**: This publication covers a low-cost, self-recoverable, double-node upset tolerant latch. This D-latch features this character because of rule design combined with other techniques. This design can be used for multiple node upset (MNU) hardened D-latch, such as QNU tolerate D-latch.

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Chapter 2

Materials and Methods

2.1 Soft error

An electronic circuit without any hardware problems can face some events resulting in spontaneous single-bit changes in the system without any such failures. This phenomenon in the computer industry is known as a "soft fail". Accruing a soft error in the hardware system does not mean that it features less reliability because the soft fail is completely random. These soft fails can be from well-known electronic noise sources such as power supply fluctuations, lightning, and electrostatic discharge (ESD) [1], or the thermal radiation from the galaxy, such as radiation-emitting stars and atmospheric gases. A soft or non-permanent fault is a non-destructive fault and falls into two categories [2]:

1. Transient faults [3], caused by environmental conditions like temperature, voltage, power supply, vibrations, fluctuations, electromagnetic, interference, ground loops, cosmic rays and alpha particles. However, by applying enhanced design and manufacturing technology, non-environmental conditions may not affect nano-technology semiconductor reliability. Meanwhile, the errors caused by cosmic rays, and alpha particles remain a dominant factor causing errors in electronic systems.

2. Intermittent faults caused by non-environmental conditions like loose connections, aging components, critical timing, power supply noise, resistive or capacitive variations or couplings, and noise in the system.

As the soft errors in digital electronics, such as electronic anomalies are random in the monitoring equipment. Recent Soft Error Rate (SER) testing results for SRAM-based FPGAs shows a significant risk of functional failures due to the corruption of configuration data, especially when the system has higher densities [4]. It is expected that neutron induced soft errors will get worse by a factor of two as we move from

130nm to 90nm technology. Radiation induced soft errors have become one of the most important and challenging failure mechanisms in modern electronic devices. Therefore, SER of commercial chips is considered and classified in four-phase approach [5]:

1. Methods to protect chips from soft errors (prevention).
2. Methods to detect soft errors (testing).
3. Methods to estimate the impact of soft errors (assessment).
4. Methods to recover from soft errors (recovery).

2.2 Sensitive Regions in Silicon Devices

A SET can be generated by charges from a single particle (proton or heavy ion) passing through a sensitive node in the circuit [6]. SET in linear devices differs significantly from other types of single event effects (SEE) like SEU in a memory. A SET features the unique characteristics like polarity, waveform, amplitude, duration, which depend on particle impact location, particle energy, device technology, device supply voltage and output load. The junction area of CMOS transistor during "off" state are most sensitive area to struck SEU from a heavy ion particles. When these particles hit the silicon bulk, minority carriers are created and, if collected by the source/drain diffusion regions, a change in the voltage value of the signal node can happen [7].

A particle can induce SEU when it strikes at the channel region of an nMOS transistor during "off" state or the drain region of a pMOS transistor during "off" state. The ionization induces a current pulse in a p-n junction. In the other words, when the charge injected in the form of the current pulse at a sensitive node, which are more than a critical charge (Q_{crit}), a SET is generated at this junction.

2.3 Single Event Transient

A SET is produced after a high-energy ionizing particle strikes a silicon device near a sensitive node [8]. The transient charge collected from the radiation event produces a current pulse at the junction. If enough charge is collected by a node, the logic state of the silicon device may change.

2.4 Soft Error Mitigation Techniques

Soft error-tolerant design techniques can be classified into two types: prevention and recovery. The methods to protect microchips from soft errors are the prevention methods [9], which are applied during chip design and development. The recovery

methods include online recovery mechanisms from soft errors in order to achieve the chip robustness requirement.

2.4.1 Prevention Techniques

a. Purify the Fabrication Material

A significant reduction in the soft error rate of microelectronics can be achieved by eliminating or reducing the sources of radiation. To reduce the alpha particle emission in packaged ICs, high-purity materials and processes are employed, but the SER caused by the high-energy cosmic neutron interactions cannot be easily shielded.

b. Radiation Hardened Process Technologies

An SER parameter can be significantly improved by a process technology that increases the critical charge (Qcrit) [10]. One approach is applying additional well isolation (triple-well or guard-ring structure) to reduce the amount of charge collected by creating potential barriers.

2.4.2 Recovery Techniques

Fault-tolerant computing methods are considered in this method. Online testing techniques are frequently used as recovery solutions for soft error mitigation.

a. Redundancy

The basic idea of redundancy design is to gain higher system reliability by sacrificing the minimality of time or space, or both. The classic triple modular redundancy (TMR) with a majority voter is the common technique in this method. Mitra et al. [11] combine a self-checking design with time redundancy based on the C-element gate to compare two samples of the output signal from a combinational circuit. The C-element can eliminate glitches at combinational outputs. Space and time redundancy are often combined to meet high fault-tolerance requirements with reduced hardware overhead, such as duplication and comparison instead of TMR.

b. Error-Correcting Code and Parity

Memories are one of the most important parts of modern systems. Because of the high density of storage cells, a large memory is more sensitive to ionizing particles than logic gates. A simple solution for protecting a memory is adding parity bits to each memory word.

During the write operation of a memory, a parity generator computes parity bits for the data to be written. The parity bits are written into memory along with the data. If a particle strike alters the state of a single bit of a memory word, now including

the parity bits, the error can be discovered by checking the parity code during the read operation. Depending on the number of parity bits used, this scheme can detect errors, and correct them as well. Such schemes are often combined with system-level approaches for error recovery [12]. In most situations, however, the error recovery in memory is more complex so protection of the memory through codes like error correcting code (ECC) is preferable.

Based on the investment done, the best way to protect memory part is Redundancy technique, which is more reliable and has less penalty. Therefore, this thesis is based on this technique. In the following, the Methodology of this thesis with details is presented.

2.5 Methodology

A detailed explanation of the objectives and how to be achieved are presented below.

1. Node sensitivity analysis in D-latch

   This objective addresses the technique to identify the sensitive node of D-latches and the analysis of the SEU sensitivity of these nodes, also including the application of node analysis information for selective node hardening techniques. One of the ways to reduce the node sensitivity to SEU are the selective harden nodes (SHN). The SNH technique is based on the transistor scaling of the logic gates associated with the sensitive nodes. Unlike other hardening techniques (i.e., TMR, DICE, etc.) which are coupled with large area overhead and more propagation delays, the proposed selective node hardening does not result in a large area overhead because it only targets the PMOS channel widths W_p of the logic gates closely connected to the more vulnerable node.

2. Exploration of SEUs, DNUs, TNUs, QNUs in dynamic d-latch circuits

   The analysis of SEU, DNU, TNU, QNU effect in dynamic latches has not been explored in detail so far. Current SEU analysis on dynamic latches or node stored charged with feedback should be comprehensively addressed. In this sense, a new SEU analysis approach is expected to be developed.

3. Designing the D-latch to achieve optimum performance over the whole operating states in terms of minimum power dissipation

   Designing harden D-latches needs extra transistors in simple latches. This strategy introduces area and power consumption penalty in the circuit. In this regard, within this objective, the development of a new structure of harden D-latch will be targeted

in order to outperform the existing alternatives by stablishing a better trade off of area and power consumption.

4. Verify the theoretical analysis by software.

   All previous discussed items should be verified based on a software demonstrator. Taking into account the previous designs and comparing them to the new design, the advantages will be displayed with the support of numerical simulations.

5. Validation of the prototype considering final application requirements in terms of: efficiency, size, process variation reliability, supply voltage and temperature variation reliability, etc.

   The main target of this step is to have a practical view of the new design of the D-latch or harden D-latch and to understand the impact of the real application requirements.

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Part II. Publications

Chapter 3

Low-Cost Soft Error Robust Hardened D-Latch for CMOS Technology Circuit

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Low-Cost Soft Error Robust Hardened D-Latch for CMOS Technology Circuit

Abstract: In this paper, a Soft Error Hardened D-latch with improved performance is proposed, also featuring Single Event Upset (SEU) and Single Event Transient (SET) immunity. This novel D-latch can tolerate particles as charge injection in different internal nodes, as well as the input and output nodes. The performance of the new circuit has been assessed through different key parameters, such as power consumption, delay, Power-Delay Product (PDP) at various frequencies, voltage, temperature, and process variations. A set of simulations has been set up to benchmark the new proposed D-latch in comparison to previous D-latches, such as the Static D-latch, TPDICE-based D-latch, LSEH-1 and DICE D-latches. A comparison between these simulations proves that the proposed D-latch not only has a better immunity, but also features lower power consumption, delay, PDP, and area footprint. Moreover, the impact of temperature and process variations, such as aspect ratio (W/L) and threshold voltage transistor variability, on the proposed D-latch with regard to previous D-latches is investigated. Specifically, the delay and PDP of the proposed D-latch improves by 60.3% and 3.67%, respectively, when compared to the reference Static D-latch. Furthermore, the standard deviation of the threshold voltage transistor variability impact on the delay improved by 3.2%, while its impact on the power consumption improves by 9.1%. Finally, it is shown that the standard deviation of the (W/L) transistor variability on the power consumption is improved by 56.2%.

Keywords: Hardened D-latch; Complementary Metal Oxide Semiconductor (CMOS) technology; Power-Delay Product (PDP); Soft Error (SE); SEU (Single Event Upset); High Impedance State (HIS); Single Event Transient (SET)

3.1 Introduction

The advent of nano-scale transistors is a movement towards the reduction of the supply voltage of circuits, but this implies increases in delay and parasitic effects [1]. Thus, nano-scale CMOS circuits are more vulnerable to errors, such as the Soft Error (SE) caused by Single Event Upset (SEU) [1]. These errors have a huge negative impact on hardware security of integrated circuits, which is invested frequently [2,3], even for electronic applications [4–6]. In the particular case of SE, they have to be addressed as a hardware security or hardware reliability issue since they can be caused by and from the environment. Environmental radiation can be constituted by high energy particles (such as neutrons, protons, alpha particles, etc.), whose impact is similar to an injected charge or SEU to internal nodes. These charge injections can potentially change the

value of stored data inside digital circuits. Another typical error is Single Event Transient (SET), which is the result of a combinational path connecting to the input of D-latch in digital circuits [7]. This undesirable pulse, as error, can change the output voltage level of a D-latch. Traditional D-latches and memory cells are very vulnerable against upsets; thus, many approaches have been proposed to solve this problem; among these are hardened circuit design [8], error correcting codes (ECC) [9] and temporal redundancy [10]. Many new D-latches have also been proposed to increase immunity against SEU [11–17] and SET [7,13]. The design of these D-latches is based on filtering the SEU or/and SET. However, the highest immunity of D-latches against the SEU and SET is achieved by increasing the number of transistors, which yields several penalties such as higher power consumption, larger area, and delay. This work proposes a new D-latch considering this trade-off and aiming at achieving a better solution in terms of power consumption, delay, working condition (temperature), process variation, and filtering the possible length of SET pulses. Immunity against SEU for various nodes is also observed. These features have been paired with a low-cost and reliable design, having a power consumption and delay close to the Static D-latch, set as a reference D-latch.

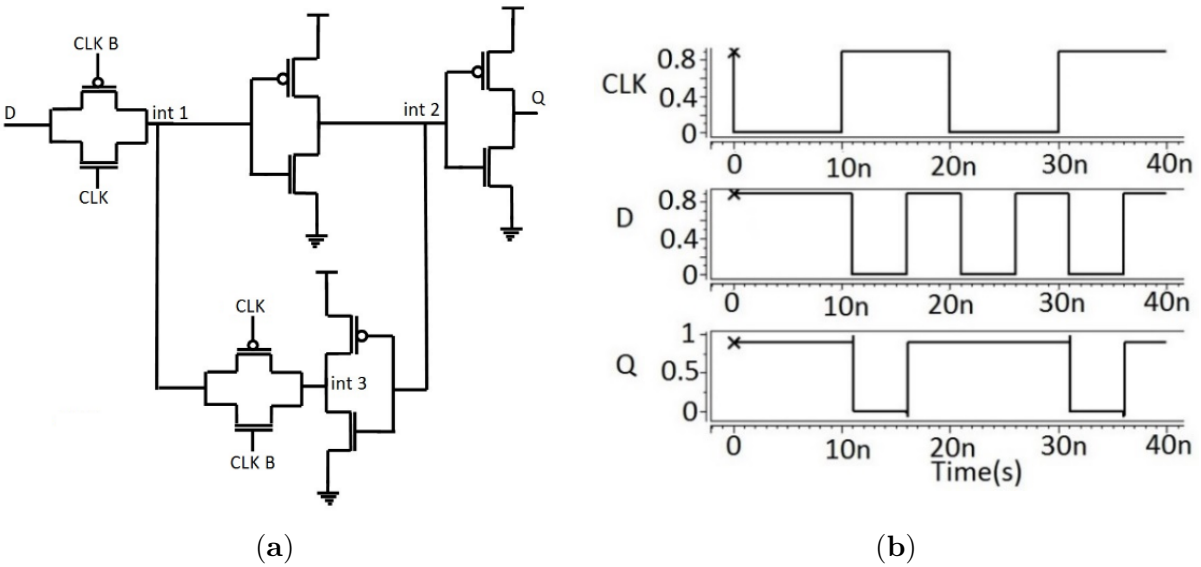
The paper is structured as follows: Section 3.2 revisits previous works on the topic including a review of existing hardened latches. The new D-latch architecture is introduced in Section 3.3, where SEU and SET immunity of the proposed D-latch are also tested by an exponential current pulse model that is inserted in various internal nodes. In Section 3.4, the impact of technological variability and temperature on the proposed and previous D-latches is investigated. The main conclusions are drawn in Section 3.5.

3.2 Previous Work

Traditional D-latches are very vulnerable against upset, which reduces their reliability for storing data in environments affected by single ionizing particles striking sensitive nodes. One of the better known of these traditional D-latches is the so-called Static D-latch. Among the advantages of this latch are its low power consumption and simplicity. However, it is not immune to SEU and SET. The input and output signals of the Static D-latch and its schematic are shown in Figure 3.1.

As the reliability of data storage in the D-latch is of paramount importance, D-latches are typically classified in four types based on their immunity against SEU and SET:

(i). The first type of D-latch can tolerate SEU in some nodes, but they have some sensitive nodes against charge injection. The proposed D-latches in [13–15] are examples of this first type. It is important to mention that only some of this kind of D-latch can filter the SET by using a delay element, which is usually in the input lines [18–20].



(**a**) (**b**)

Figure 3.1. (a) Static D-latch schematic; (b) input and output signals of the Static D-latch

(ii). The second type of D-latch is fully immune against the SEU, but they cannot filter input SET. In this family the output can also be in a high impedance state (HIS). An example of this type of D-latch is the Dual Interlocked storage CEll (DICE) latch [8].

(iii). The third type of D-latch can tolerate SEU in various nodes and avoids high impedance states, so high impedance at output cannot occur. However, they cannot filter the SET [21].

(iv). The fourth type of D-latch is not only fully immune against the SEU and SET, but also has a high impedance state at the output [22–24]. The high impedance state of the output can be solved by a keeper, which is a buffer that connects input and output nodes [22–24].

A summary of the different types of D-latch is shown in Table 3.1. According to the four types of hardened D-latch, the so-called DICE belongs to the second type of hardened latch, being immune against SEU based on-cross the coupled inverter [8]. When SEU occurs in one node, the DICE structure can handle this SEU since it stores the input data in two different nodes. However, it cannot tolerate two simultaneous upsets to the two sensitive nodes and cannot filter SET pulses. Furthermore, the DICE presents high power consumption and delay in comparison to other hardened D-latches [25].

Table 3.1. Classification of different type of D-latch in regard to their soft-error immunity.

Type	Full Immune SEU	Filtering SET	HIS Insensitive	Examples
First	×	×	×	[14–16]
Second	✓	×	×	DICE [8], TMR [23]
Third	✓	✓	×	[21]
Fourth	✓	✓	✓	TPDICE-based [24], FERST [23], LSEH-1 [7]; LSEH-2 [1,7], This work

The Triple Modular Redundancy (TMR) latch presents a hardened design that makes it totally immune against upset, which fits the second type [23]. The TMR architecture can detect and correct SEU. However, it has a large number of transistors, which means that power consumption, area and delay penalty of this latch are far from ideal. In [23], a TMR D-latch including three Static D-latches with a voting circuit is discussed in regard to its performance and how it can be fully immune against upsets. In [23] a feedback redundant SEU/SET-tolerant latch (FERST) is also presented. FERST consists of two feedbacks and a delay element to avoid upset and there are two inverters as keepers to avoid a floating output node. Despite being fully immune against SEU, it consumes less power in comparison to TMR.

In [26], the authors proposed a latch design applying the hysteresis property of the Schmitt trigger inverter to increase immunity against SET; however, a Schmitt trigger based inverter with hysteresis property can reduce the speed of the D-latch. The feedback of this D-latch includes a C-element and two dynamic inverters. This feedback is active when CLK is “0” and holds the data in one node.

On the other hand, a Low-cost and Soft Error Hardened (LSEH) D-latch is proposed in [7], called LSEH-1, which has two separated paths to store the input data. These two paths have different delays to filter the SET of the input data. These two paths are connected to the C-element to trigger the output stage. LSEH-1 has three stages to store the input data at holding time. If the particle strikes in one stage, the two other stages can correct the output without any upsets. Furthermore, a so-called LSEH-2 is proposed in [7] having two latching stages in two different paths, which are connected to the C-element. Each input data, “0” and “1”, passes through a different path to reach the output nodes, so SET pulses can be filtered in this D-latch. These LSEH-1 and LSEH-2 D-latches are benchmarked against the TMR in different parameters, such as delay, power consumption, temperature variation and process variation. This comparison shows better performance of these two LSEH-1 and LSEH-2 D-latches when compared to that of TMR [7].

In addition, full immunity against the SEU in any single node and filtering SET are the features of the D-latch proposed in [1]. This D-latch stores the data in two inverters with positive feedbacks during holding time. Moreover, it can tolerate single event multiple upsets (SEMUS), along with other features, such as reliability and low-cost structure.

Finally, the Triple Path DICE (TPDICE)-based D-latch in [24] can tolerate SEU and filter SET. It can handle Single Event Double-Upset (SEDU), which means that this D-latch can tolerate different charge injections at multiple nodes. The structure of this D-latch consists of a TPDICE, a triple-input Muller C-element, a Schmitt trigger inverter, and a keeper in the output node. The TPDICE is triggered by the clock and the D-input. The inputs of the triple-input Muller C-element of this D-latch are provided by TPDICE. This structure of TPDICE with C-element can recover the data, with a single event upset in one node. Moreover, the TPDICE is applied in this D-latch to tolerate SEDU. The keeper is used in the output of TPDICE-based D-latch to avoid the high impedance state at the output. Besides, the embedded Schmitt trigger inverter on the propagation path can filter SET of the input.

It is worth mentioning that although this work focusses on SEU, hardened D-latches to tackle DNU (double node upset) [5,27], and TNU (triple node upset) [28] are also being investigated. However, those alternatives, out of the scope of this work, are also penalized by higher transistor count and power consumption.

The proposed D-latch in this paper belongs to the fourth type and its immunity against SEU is better than that of the TPDICE-based D-latch [24], which is already considered fully immune, since the proposed design can tolerate a significant charge injection. The proposed D-latch also has lower transistor count and better performance in comparison to the TPDICE-based D-latch and other previous D-latches, regarding lower process variation, power consumption and delay. The next two sections are devoted to the presentation of the proposed D-latch and to analyzing these benefits in detail.

3.3 Proposed D-Latch

The schematic of the novel D-latch is shown in Figure 3.2a. The D-input passes through two paths; one path is integrated by one switch connecting the input to the output D-latch and the other path is formed by two inverters and one switch that is ON when CK = “1”. The “X4” and “X2” nodes are connected to the first C-element to delete the SET of D data; this C-element increases the delay because it is ON when CK = “1”. The third and fourth C-elements are used to store the output for the holding time. The second C-element of the feedback path is ON when CLK = “0” and provides the feedback in the hold mode. Storing the D-input in two different C-elements makes the structure reliable against SEU. The C-element with the same inputs works as an inverter; however, when the values of two or three inputs are not the same, the output

of the C-element does not change. For example, when one SEU occurs in one of the two or three different paths, the output node does not change. The layout of the proposed D-latch is shown in Figure 3.2b. The equivalent schematics for each case (CK = “0” and CK = “1”) are also shown in Figure 3.2c and Figure 3.2d, respectively.

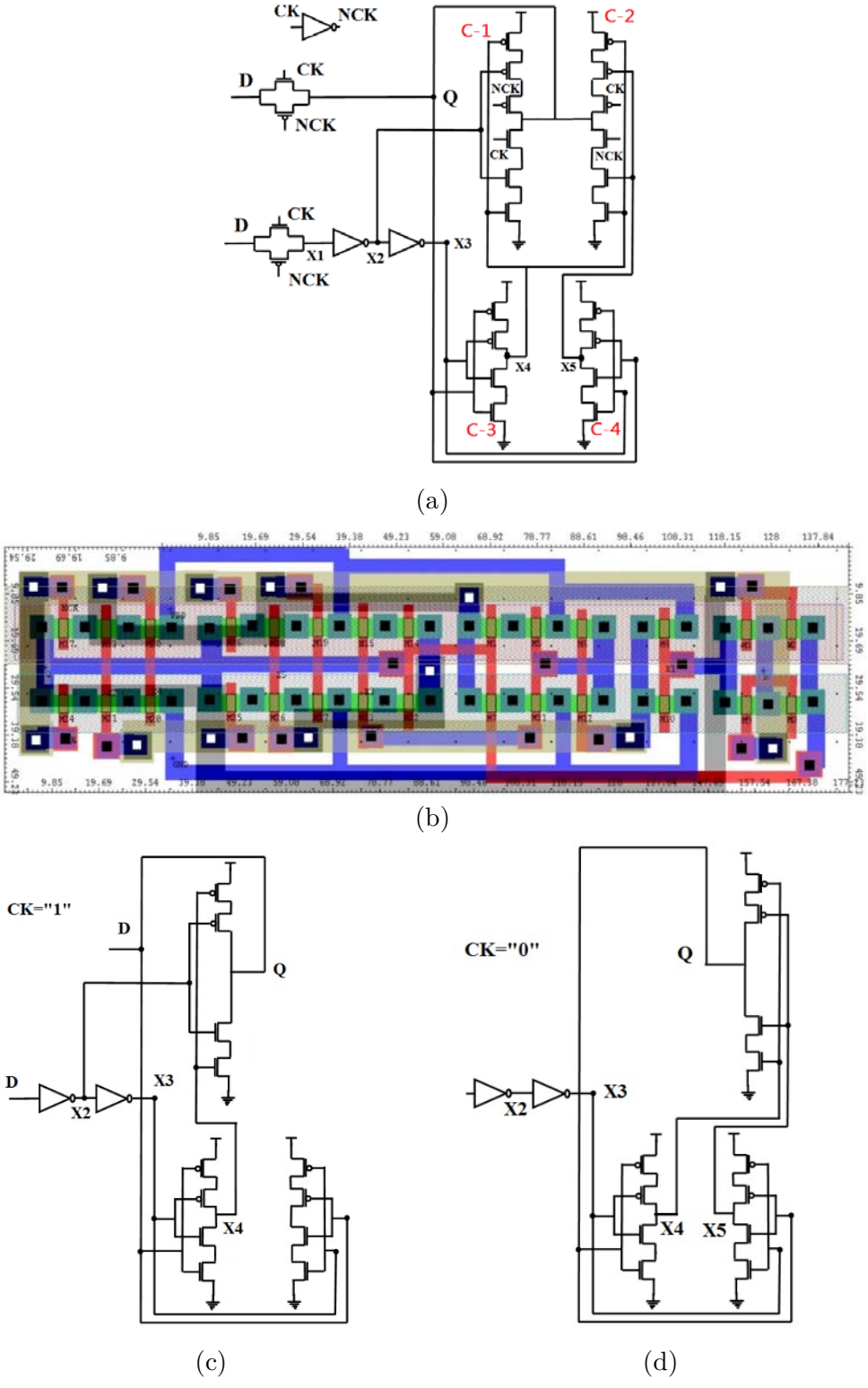


Figure 3.2. Proposed D-latch (a) schematic; (b) layout; (c) equivalent schematic when CK =”1”; (d) equivalent schematic when CK =”0”.

As mentioned above for the D-latch in [26], the feedback is applied to hold the data during the holding time. As the positive feedback of the D-latch increases the side effects of the process variations, the activation of the positive feedback only during holding time reduces power consumption and improves immunity against process variability in threshold voltage and W/L.

As can be seen, the proposed D-latch has extra circuitry for masking SET, which turns into area consumption and larger delay. However, when CK = "1", there are two paths to connect input to output: one path consists only of the transmission gate and the other comprises inverters and the C-1, and C-3 elements. Therefore, the second path introduces more delay and masks SET. However, in this design input and output are connected by the transmission gate, therefore the delay will be reduced and it is not directly affected by the inverters and the C-1, and C-3 elements. Similarly to other approaches of hardened D-latches [5,24], two sample paths of input are used for improved reliability. Furthermore, the proposed D-latch features two separated circuits in transmission mode and holding that, combined with clock-gating technique, lead to a very low power consumption.

To investigate the SEU capability of the proposed D-latch, a number of SEUs are injected to various internal nodes. Then, the output signal is monitored to prove immunity against SEU at different nodes. The model of injected charge is based on an exponential current source [23]. The charge injection with different values is introduced during 0.3 ns and 0.9 V supply voltage at different internal nodes in reference CMOS technology at room temperature. Since different nodes can tolerate different values of charge injections, the maximum value of charge injection has been calculated for each specific node to produce voltage spikes slightly over the supply voltage and under zero volts [7,24], as shown in Figures 3.3–3.5 to test SEU immunity. The shape of the current source can be expressed mathematically [29]:

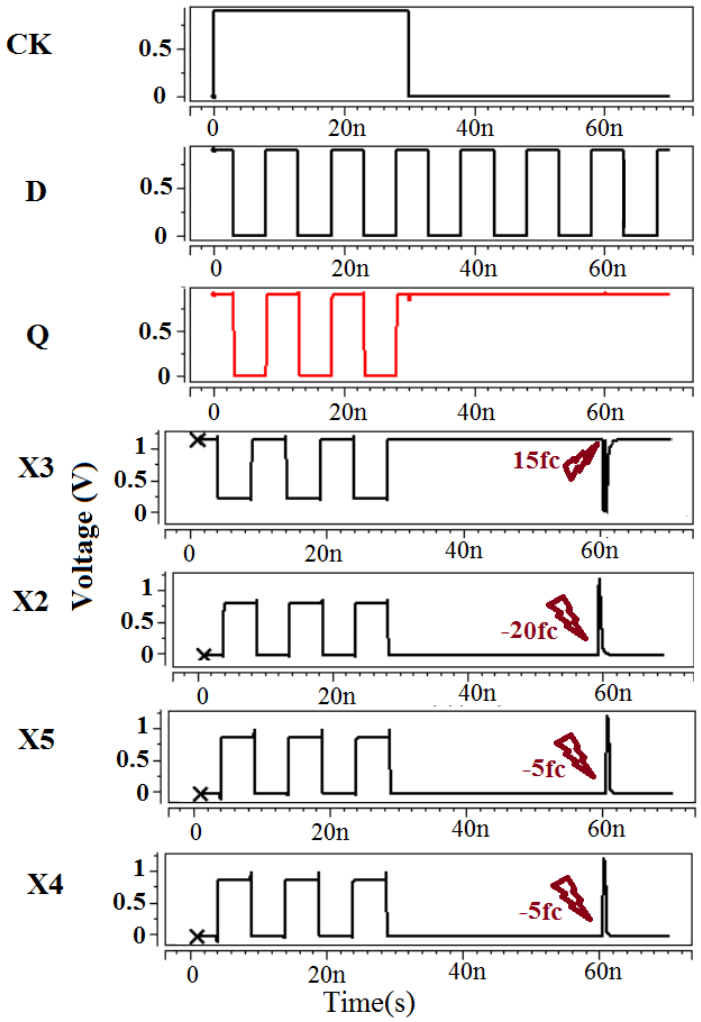
$$Q = \int_0^t \frac{Q_{total}}{\tau_f - \tau_r} \times \left(e^{-t/\tau_f} - e^{-t/\tau_r} \right).dt \qquad (1)$$

where Q_{total} is the total charge generated by the upset, τ_f is a constant coefficient of fall time and τ_r is a constant coefficient of rise time. Four different situations for each node are considered to test the proposed D-latch to observe the output. For example, the positive and negative charge injections are introduced to the "X1" node, when the output is "1" or "0" at the holding time. Thus, these four situations are tested for all internal nodes. Figure 3.3 shows the results of this test, when the output is "1" during the holding time with positive charge injections introduced in "X3" node and with negative charge injections introduced in "X2", "X4", and "X5" nodes. As can be observed, the output node "Q" is not affected by the SEU event in each one of these tests. For example, when the negative charge is injected in the "X5" node when "Q" is in the high logic value "1", the value after this charge injection maintains the valid value. In another test, the positive charge is injected to the "X3" node when the value of "Q" is "1" and, as can be seen, the value of "Q" does not change. This kind of test

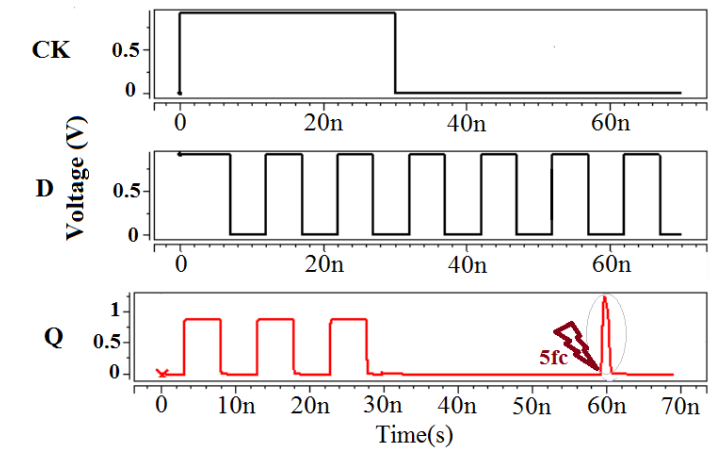
shows the immunity of the proposed D-latch against SEU. Moreover, for all of these tests (SEU immunity) for various nodes and for monitoring the Q node, the high impedance state does not occur, which means this proposed D-latch is insensitive to high impedance.

Figures 3.4 and 3.5 show test results of charge injection when the output is "0" during the holding time. In Figure 3.4, "Q" and "X3" nodes in the direct path are injected with charge. In Figure 3.4a, the positive charge injection is introduced to the "Q" node and, as shown, the proposed D-latch can tolerate this injection since the value of the output does not change after the upset.

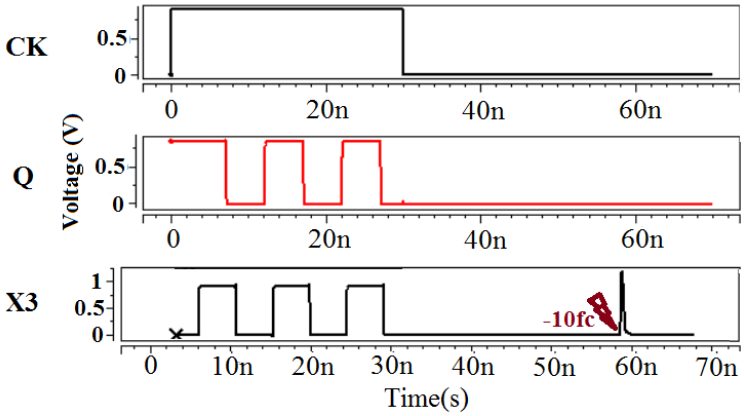
Figure 3.3. Test results for SEU injection to nodes when the output is "1" during the holding



time; positive SEU injection to "X3" and negative SEU injection to "X2", "X4", and "X5" nodes.



(a)



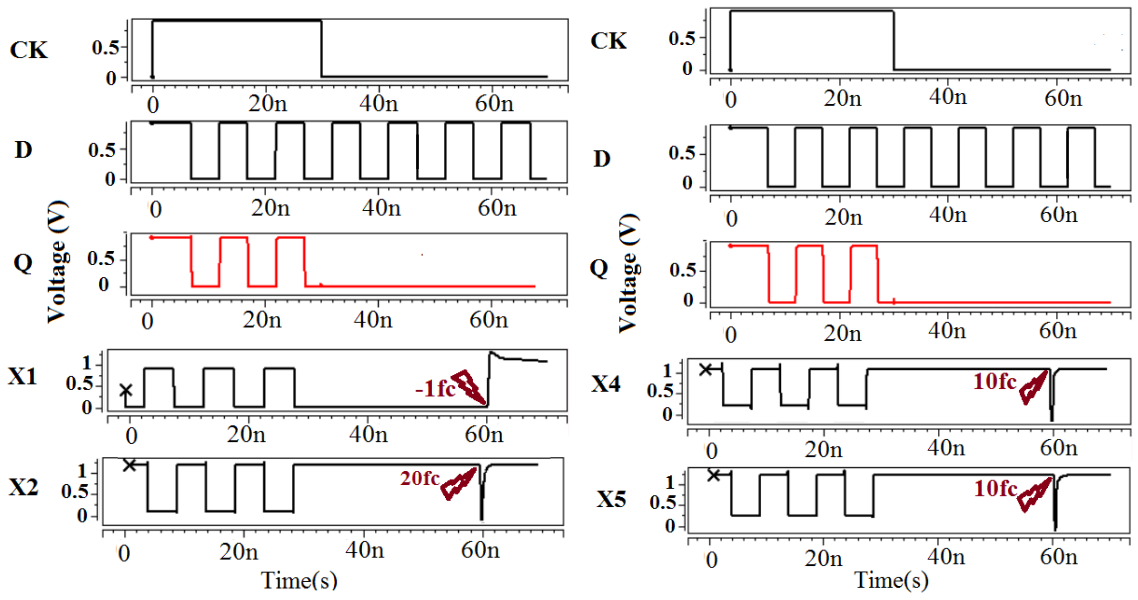
(b)

Figure 3.4. Test results for a positive and negative SEU injections to nodes when the output is "0" during the holding time: (a) to "Q" node; (b) to "X3" node.

In Figure 3.4b, the test is performed for the "X3" node; in this case too the output of the proposed D-latch does not change its value.

Figure 3.5 shows results when the output is "0" and a negative injection is introduced in "X1" node and a positive injection is introduced in "X2", "X4", and "X5" nodes. As can be observed in this figure, in neither case would the output be affected.

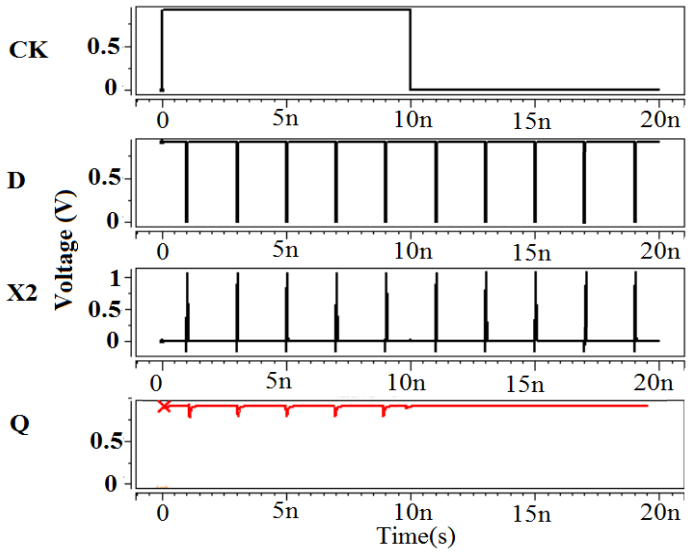
The results of the study on critical charge injection in different nodes show that N1 can lose its data and valid logic state by small charge injections. N2 has more tolerance against charge injection. If more than 85 fC charge is injected to N2, it loses its value, but even this situation does not affect the Q value. The tolerance of N3, N4 is better, as they can tolerate up to 800 fC without disturbance in the data. Tolerance of N5 is lower since approximately 160 fC can be injected without losing the data. More importantly, for all these situations, the logic value of Q does not change. The previous figures for charge injections are very high, substantially over the usual value for testing SEU immunity, i.e., 20 fC [7].



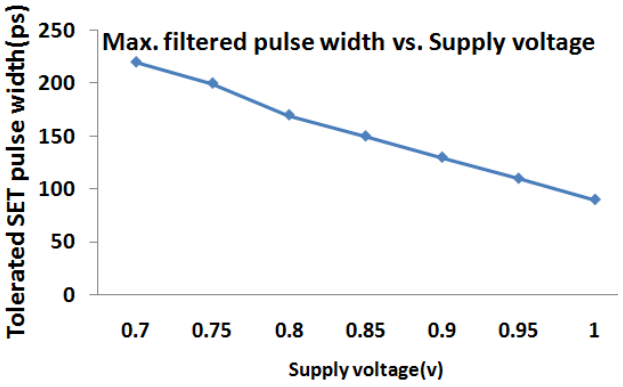
(a) (b)

Figure 3.5. Test results when the output is "0" during the holding time: (a) negative and positive SEU injection to "X1" and "X2" nodes, respectively; (b) positive SEU injection to "X4" and "X5" nodes, respectively.

A further test has been carried out to demonstrate the SET masking capability of the proposed D-latch. The result of this test is shown in Figure 3.6. The proposed design can mask undesirable pulses that are generated at the combinational digital circuits of previous D-latch stages. In the transparent mode, SET can be filtered by two simple inverters and the first and third C-elements comparing data of two paths, with differences in two inverters and two C-elements to produce delay. Those two inverters, and the first, and third C-elements in the direct path, increase the delay but provide the D-latch with one important feature: the filtering of the SET. SET has no impact on the output from the feedback path from "X4" and "X5" nodes, since the second C-element connecting these nodes is not ON at the transparent mode. In Figure 3.6a, the input signal is shown with a 100 ps SET pulse at 0.9 V supply voltage, illustrating how this SET pulse is filtered by the proposed D-latch. It is worth mentioning that this masking depends on the supply voltage, the width of SET pulse, the delay and the temperature. The maximum width of SET pulses filtered by the proposed D-latch is shown as a function of supply voltages in Figure 3.6b. As can be seen, the maximum pulse width of SET decreases as the voltage supply increases (higher conductivity of the transistors) [7]. This dependency should be considered when it is necessary to suppress the SET pulse in sensitive applications [30–32]



(a)



(b)

Figure 3.6. (a) SET pulse filtering capability of the proposed D-latch; (b) maximum pulse width of SET filtered by the proposed D-latch at various supply voltages.

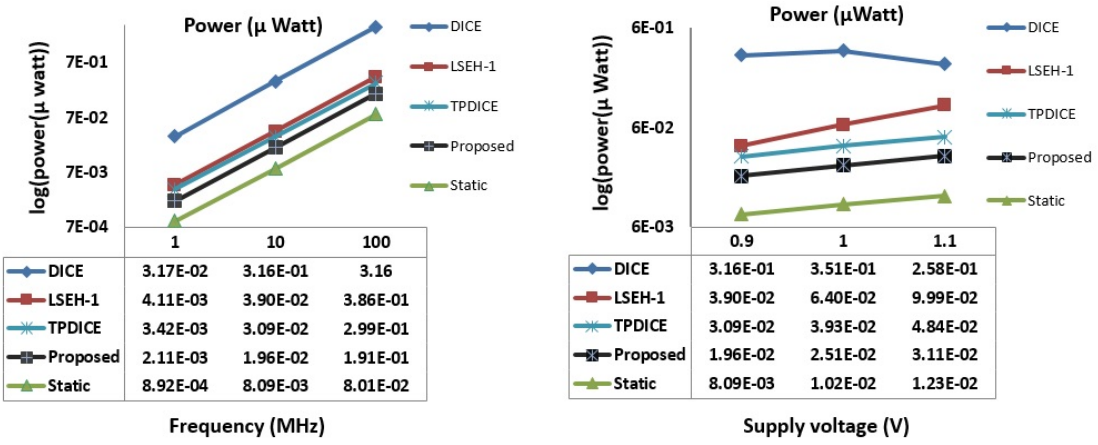
It is worth mentioning that in [24], aiming at masking SET, a Schmitt Trigger Inverter is used in transparent mode; however, it has a large impact on delay because of the hysteresis property. LSEH-2 [7] also has two different paths for two different inputs, “0” and “1”, which implies huge power consumption and area for filtering SET without double sampling, reducing reliability. These solutions are avoided in this work in order to achieve reasonable delay and accuracy. Thanks to the double sampling with different delays, SET is masked. The delay of the two paths (one transmission gate, and the inverters and C-elements) depends indirectly on the delay of inverters and C-1 and C-3 elements. The aspect ratio of PMOS and NMOS of the inverter and C-1 and C-3 element can also affect the delay. However, in our design they do not have a significant impact in comparison to the approach used for masking SET in other D-latches [7,23,24]; therefore, this effect has been neglected.

3.4 Latch Evaluation and Benchmarking

In this section the Static D-latch, DICE [8], TPDICE-based D-latch [24], LSEH-1 D-latch [7] and the proposed D-latch are simulated at three power supply voltages and three frequencies using HSPICE in the reference TSMC 65nm CMOS technology. In these simulations, the aspect ratio of PMOS transistors is W/L = 130nm/65nm, while the aspect ratio of NMOS transistors is W/L = 120nm/65nm. Benchmarking of various important characteristics, such as power consumption, Power Delay Product (PDP), and (D-Q) delay is presented. All these D-latches are immune against SEU apart from the Static D-latch, which is chosen as a reference since it features less power consumption and propagation delay. Furthermore, the proposed D-latch, TPDICE-based D-latch, and LSEH-1 D-latches can filter SET pulses.

3.4.1 Power Consumption

As can be observed in Figure 3.7, the power consumption of the proposed D-latch is lower than those of all the other previous hardened D-latches (all of them designed to achieve minimum footprint), DICE [8], TPDICE-based D-latch [24] and LSEH-1 latch [7]. They all have been simulated at different frequencies, from 1 MHz to 100 MHz. at 0.9 V power supply voltage (Figure 3.7a), and different supply voltages, ranging from 0.9 to 1.1 V, at 10 MHz input frequency (Figure 3.7b). The power consumption of the proposed D-latch is higher than that of the Static D-latch, with an increment of 142%, but with the introduction of immunity against SEU and SET. The lower power consumption of the proposed D-latch in comparison to the other alternatives is attributed to the use of the clock-gating C-elements. There are two clock-gating C-elements in the proposed D-latch: the first one on the transparent path for filtering SET, which is ON whenever the CK = "1", and the second in the feedback path, which is ON whenever CK = "0".



	1	10	100
DICE	3.17E-02	3.16E-01	3.16
LSEH-1	4.11E-03	3.90E-02	3.86E-01
TPDICE	3.42E-03	3.09E-02	2.99E-01
Proposed	2.11E-03	1.96E-02	1.91E-01
Static	8.92E-04	8.09E-03	8.01E-02

	0.9	1	1.1
DICE	3.16E-01	3.51E-01	2.58E-01
LSEH-1	3.90E-02	6.40E-02	9.99E-02
TPDICE	3.09E-02	3.93E-02	4.84E-02
Proposed	1.96E-02	2.51E-02	3.11E-02
Static	8.09E-03	1.02E-02	1.23E-02

(**a**) (**b**)

Figure 3.7. Power consumption of various D-latches: (a) at three frequencies from 1 MHz to 100 MHz and 0.9 V power supply voltage; (b) at three supply voltages and 10 MHz input frequency.

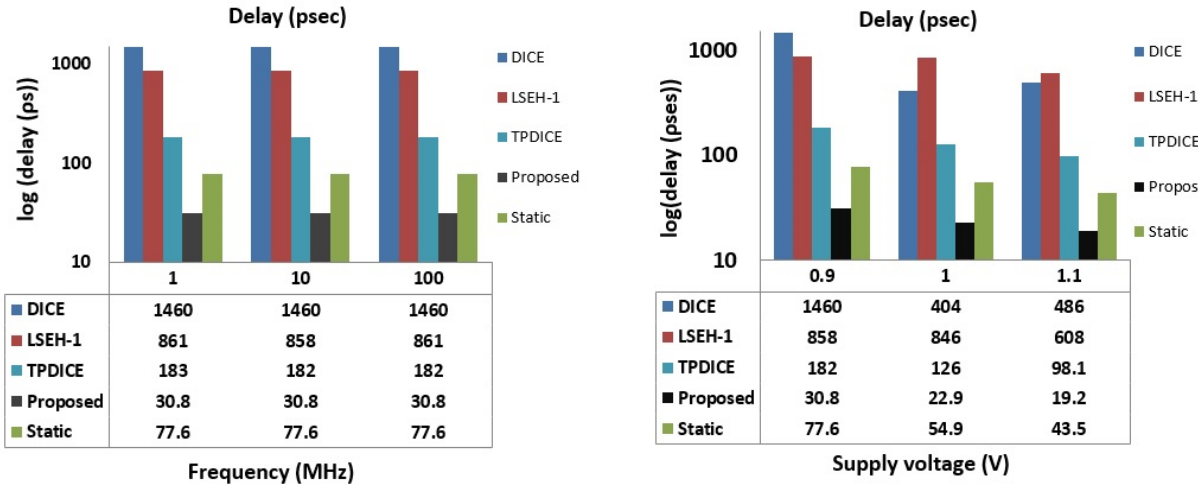
Moreover, the proposed D-latch has separate stages for transparent mode and holding time, which further reduces power consumption and delay. The delay decreases because in transparent mode the output can be set without passing from the saving nodes, which are used for holding time, while power consumption is reduced since, by separating two modes, it is possible to use clock gating-based C-elements.

3.4.2 Delay

The delay is one of the most important parameters of D-latches. This decreases with increasing supply voltages due to the higher conductivity of the channel of the transistors, as shown in Figure 3.8. According to the results, the improvement of the proposed D-latch delay in comparison to the Static D-latch is up to 60%.

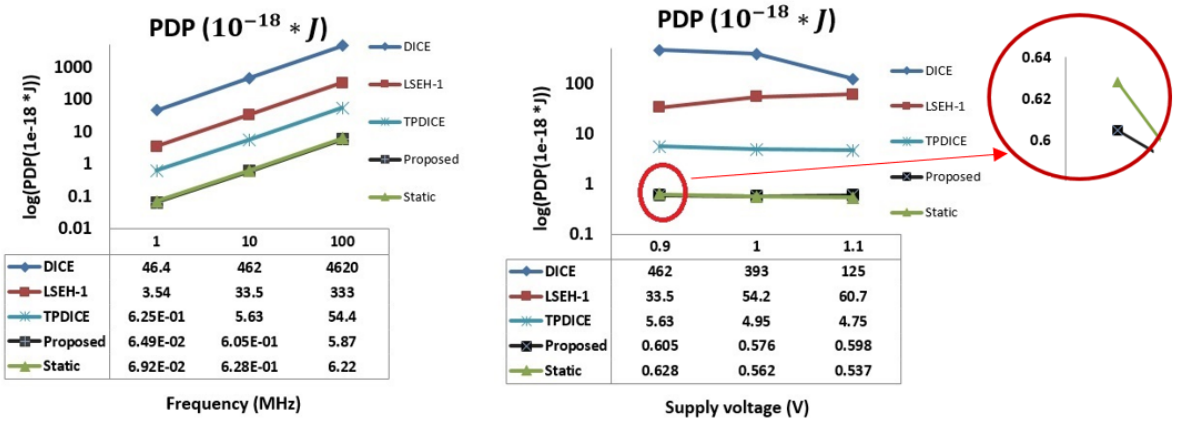
3.4.3 PDP

Furthermore, as PDP is a figure of merit showing the total performance of D-latches and, in particular, commonly used to evaluate hardened D-latches [7,30], a PDP comparison of the proposed and previous D-latches is shown in Figure 3.9. As can be seen, the PDP of the proposed D-latch is even slightly better than that of the Static D-latch, with a 3.67% improvement. This improvement is achieved by reducing delay, as PDP is power consumption multiplied by delay.



(a) (b)

Figure 3.8. Delay of various D-latches: (a) at various frequencies from 1 MHz to 100 MHz and 0.9 V power supply voltage; (b) at three supply voltages and 10 MHz input frequency.



(a) (b)

Figure 3.9. PDP of various D-latches: (a) at various frequencies from 1 MHz to 100 MHz and 0.9 V power supply voltage; (b) at three supply voltages and 10 MHz input frequency.

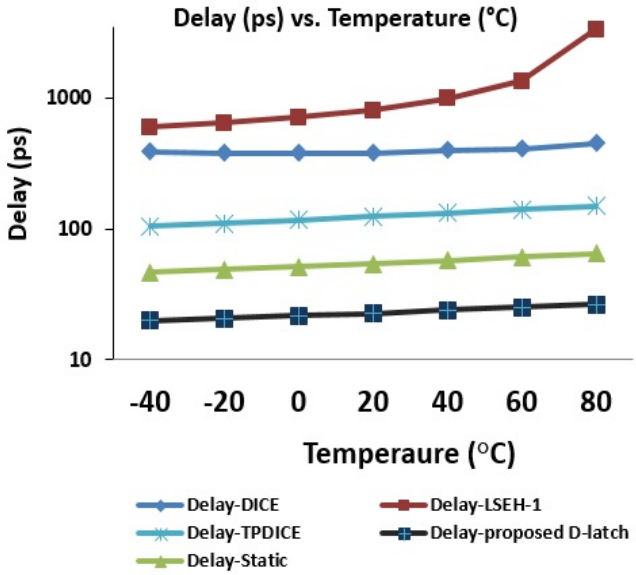
3.4.4 Temperature Variation

One of the most important operational parameters considerably affecting the D-latch performance is temperature, which may change dramatically under different conditions. To show this impact, the DICE, TPDICE-based D-latch, Static, LSEH-1, and proposed D-latches are simulated at different temperatures ranging from −40 °C to 80 °C (industrial range) with 10 °C steps.

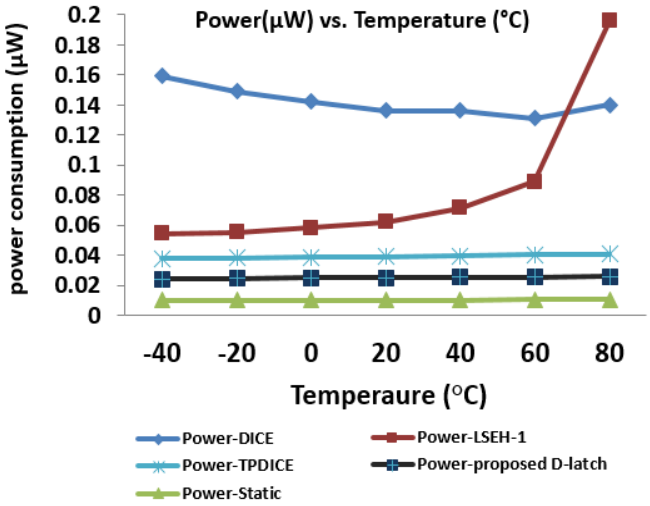
As expected, raising the temperature increases the delay (above 30 °C for DICE) due to the lower electrical conductivity (lower carrier's mobility) and increases the power consumption (above 60 °C for DICE), as high temperature increases current leakage [33]. However, the temperature effect on the proposed D-latch is lower than in other D-latches, such as LSEH-1, DICE, and TPDICE-based D-latches, as deduced from Figure 3.10 (a comparative study in terms of a temperature coefficient has been included in Appendix A).

3.4.5 Area Usage

Another important benchmarking parameter is area usage; this parameter can be evaluated from the device layout. Table 3.2 shows the area comparison between the proposed D-latch and previous D-latches designed with Tanner L-EDIT [34] (all designs targeting minimum area). As can be observed, the proposed D-latch footprint matches that of DICE with the advantage of presenting better immunity and power consumption parameters.



(a)



(b)

Figure 3.10. Temperature variation effect on: (**a**) delay vs. temperature; (b) power consumption vs. temperature.

Table 3.2. Comparative area of D-latches.

D-Latch	**Proposed D-Latch**	**Static**	**TPDICE [19]**	**DICE [8]**	**LSEH-1 [7]**
Area $(\mu m)^2$	7.959	3.0816	18.04	7.944	12.21

3.4.6 Process Variations

Finally, process variability, such as variation of transistor aspect ratio (W/L) or threshold voltage are analyzed. Monte Carlo simulations constitute a helpful tool to assess how the delay and power consumption are affected by these variations. A Gaussian distribution has been considered to model (W/L) and threshold voltage variability. The maximum deviations from the original (W/L) values of transistors and threshold voltages are set from 2% to 16%, which is the probable range of change normally used for comparison in this kind of study [1,7,27]. For each maximum deviation, 20 simulations are carried out to study the effect of (W/L) and threshold voltage variability on the delay and power consumption. Figure 3.11 shows the delay as the result of (W/L) transistor variability. In Figure 3.11a, the delay changes of the proposed D-latch as a result of (W/L) transistor variations are shown. It can be seen that the results have approximately the same delay variation as that of the TPDICE-based D-latch (Figure 3.11c), and the Static D-latch (Figure 3.11b), while it is much better than that of DICE (Figure 3.11d) and LSEH-1 D-latches (Figure 3.11e). The results are normalized to the delay of the original D-latch without any process variation. This normalization helps better visualize the effect of (W/L) transistor variations on delay. Figure 3.11f clearly shows the minimum variations of delays for the proposed D-latch when compared to other D-latches in maximum deviation.

In Figure 3.12, the effect of (W/L) variability on the power consumption is shown. As can be seen by varying (W/L) of the transistors by 2%–16% deviations from the original value, the power consumption of the proposed D-latch is affected similarly to that of the TPDICE-based D-latch and it is much better than that of the Static-latch, DICE, and LSH-1 latches.

The maximum variance (σ_{max}) and standard deviation (dev_{max}) are calculated for the delay and power consumption of the proposed, Static, and TPDICE-based D-latch, DICE, and LSEH-1 D-latches. These variance and standard deviation measurements are for the maximum deviation from the original (W/L) transistors, which is 16%. Maximum variance and deviation are shown in the insert of the plot for each D-latch in Figures 3.11–3.14. The impact of (W/L) variations on the power consumption of the proposed D-latch is low, but the delay deviation of the proposed D-latch is more than that of the Static D-latch. The delay standard deviations of the proposed D-latch, Static, and TPDICE-based D-latch, DICE, and LSEH-1 are 0.04, 0.012, 0.02, 0.18 and 0.14, respectively. The maximum variance of the delay of the proposed D-latch, Static, TPDICE-based D-latch, DICE, and LSEH-1 are 0.05, 0.014, 0.03, 0.26, and 0.19, respectively.

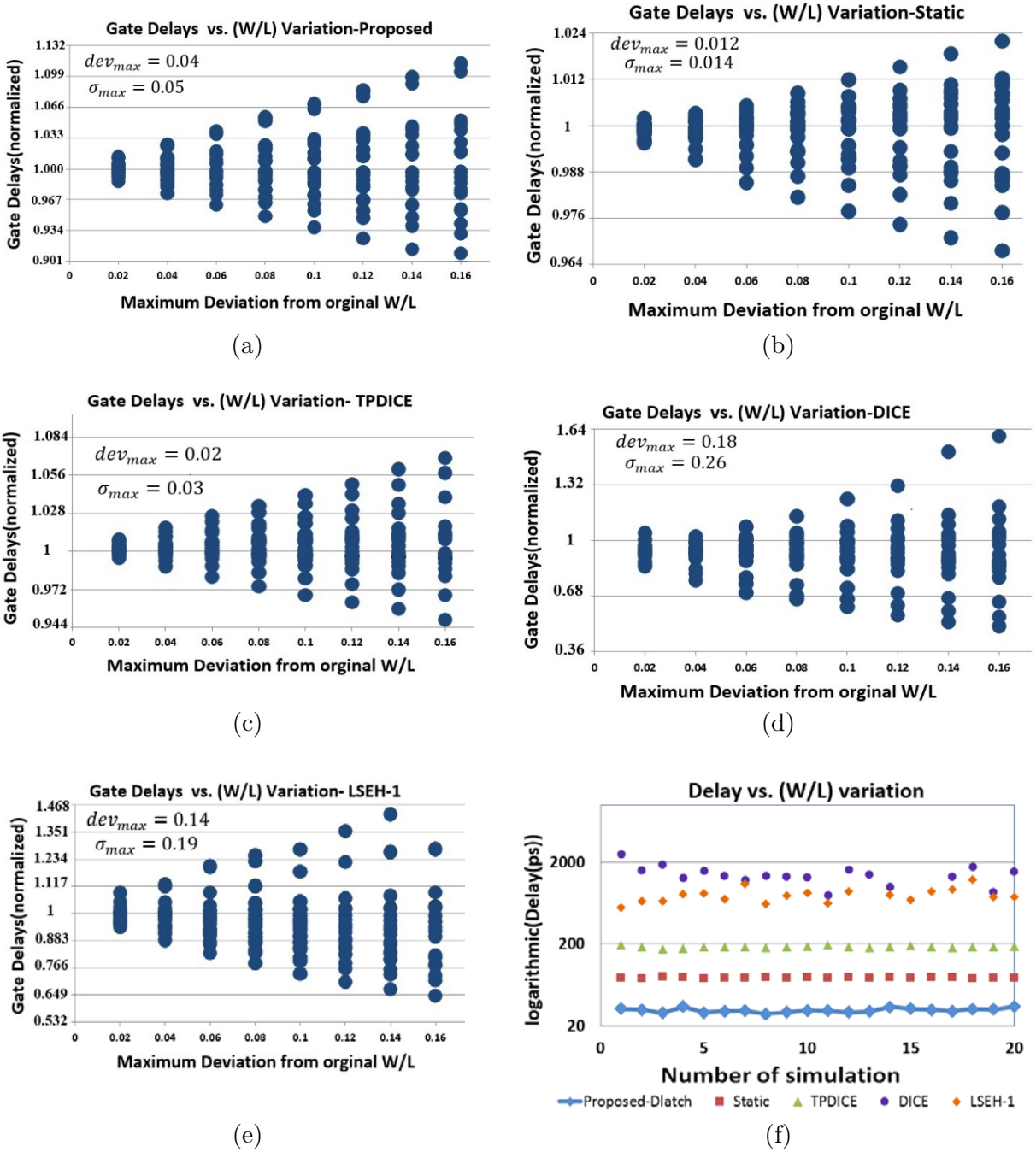


Figure 3.11. (W/L) variation effect on D-latch delay: (a) proposed D-latch; (b) Static D-latch (c) TPDICE-based D-latch (d) DICE (e) LSEH-1 latch (f) delay of D-latches with maximum deviation, 0.16, from original W/L.

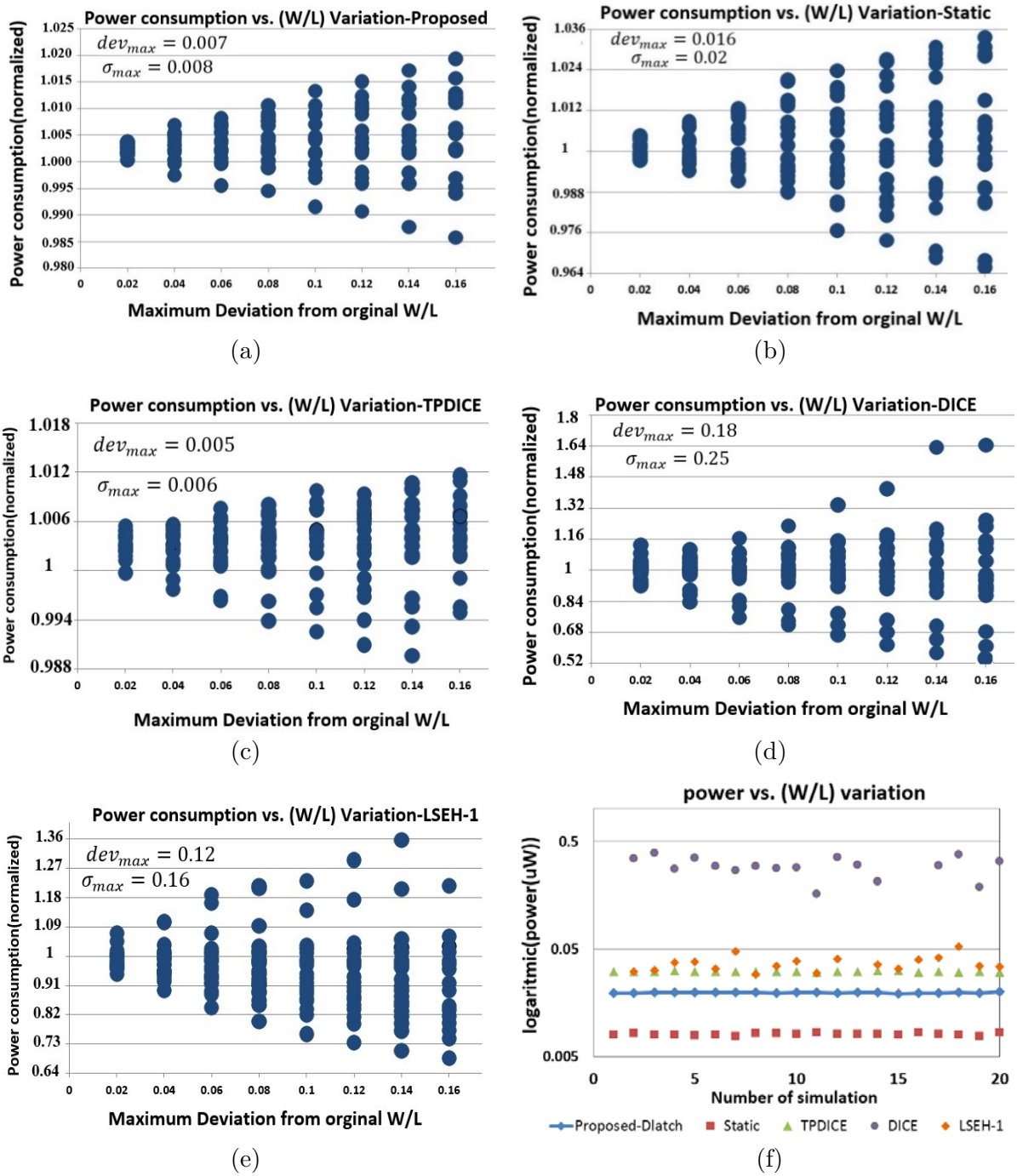


Figure 3.12. (W/L) variation effect on power consumption: (a) proposed D-latch (b) Static D-latch (c) TPDICE-based D-latch (d) DICE (e) LSEH-1 latch (f) power consumption of D-latches with maximum deviation, 0.16, from original W/L value.

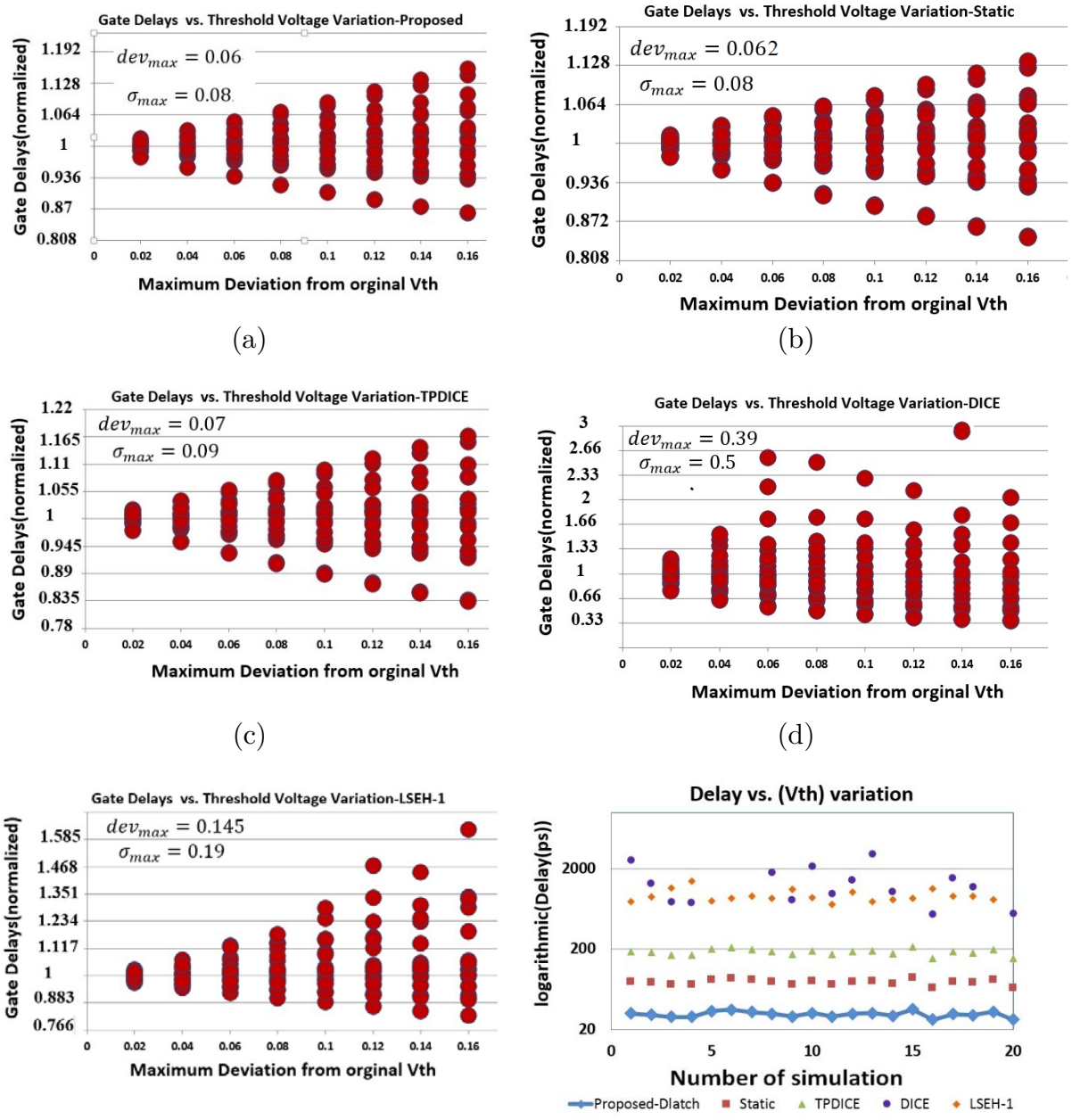


Figure 3.13. Threshold voltage variation effect on D-latch delay: (a) proposed D-latch (b); Static D-latch (c); TPDICE-based D-latch (d); DICE (e) LSEH-1 latch (f); delay of D-latches with maximum deviation, 0.16, from original threshold voltage.

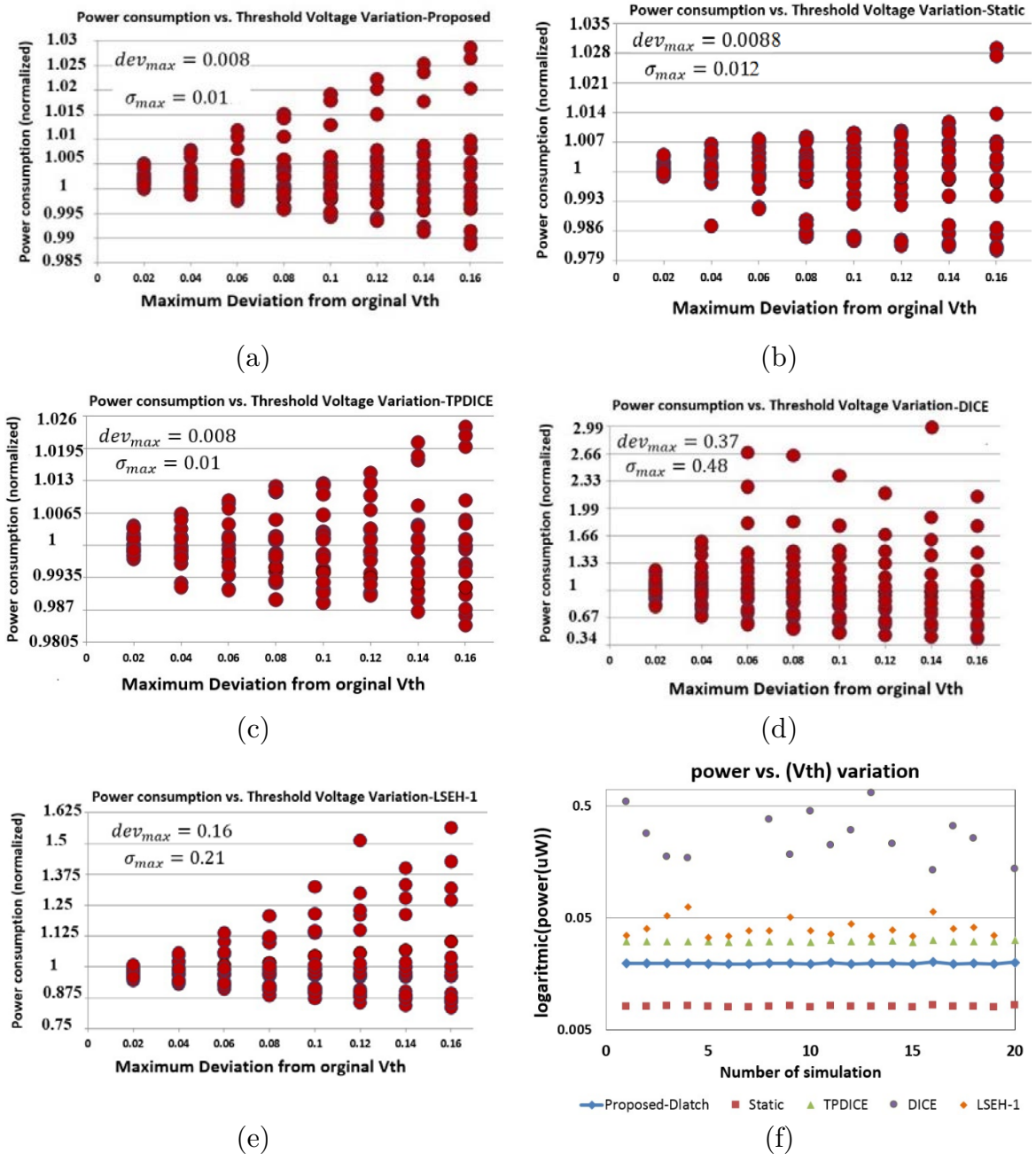


Figure 3.14 Threshold voltage variation effect on power consumption: (a) proposed D-latch; (b) Static D-latch; (c) TPDICE-based D-latch; (d) DICE; (e) LSEH-1; (f) power consumption of D-latches with maximum deviation, 0.16, from original threshold voltage.

The standard deviation improvement of the (W/L) transistor variability on power consumption of the proposed D-latch, compared with the Static D-latch as reference, is 56.2%. In general, process variations have a negative effect on power consumption and delay.

The gate delay and power consumption variation versus threshold voltages are shown in Figures 3.13 and 3.14, respectively. The threshold voltages of the different transistors are changed by 2%–16% of their original values. As can be seen in Figures 3.13 and 3.14, the delay (D-Q) and power consumption variations of the proposed D-latch are lower in comparison to those of Static, TPDICE-based D-latch, DICE, and LSEH-1 D-latches. This fact demonstrates a superior reliability of the proposed D-latch as compared to other alternatives. These lower variations of power consumption and delay for the proposed D-latch can be attributed to the lower effect of the positive feedback loop in this design (positive feedback yields huge process variation): in the proposed D-latch positive feedbacks are only activated during holding time and their paths are separated from the transparent path. These feedbacks enter a clock-gating C-element, which may reduce the effect of the positive feedback loop.

The impact of threshold voltage variations on the power consumption of the proposed D-latch is negligible. The delay standard deviations of the proposed D-latch, Static, and TPDICE-based D-latch, DICE, and LSEH-1 are 0.06, 0.062, 0.07, 0.39 and 0.145, respectively. The maximum threshold voltage variance of the delay of the proposed D-latch, Static, TPDICE-based D-latch, DICE, and LSEH-1 are 0.08, 0.08, 0.09, 0.5, and 0.19, respectively. The standard deviation improvement of threshold voltage transistors variability on the delay of the proposed D-latch, compared with that of a Static D-latch set as reference, is 3.2% and improvement for power consumption is 9.1%. In summary, threshold voltage variations have low effect on power consumption and delay on the proposed D-latch in comparison to the other hardened alternatives considered in this study.

3.5 Conclusions

In this contribution, a low-cost hardened D-latch is proposed with full immunity against SET and SEU. Additionally, it features a lower power consumption and delay in comparison to those of previous hardened D-latches alternatives, such as DICE, TPDICE-based D-latch, and LSEH-1. For benchmarking, the performance of the Static D-latch is set as reference, and the proposed D-latch provides the closest values in terms of delay and power consumption. The delay and PDP of the proposed D-latch improve 60.3% and 3.67%, respectively, in comparison to those of the reference latch at the expense of a power consumption increase (142%) with regards to the reference latch. A comparison between Static, DICE, TPDICE-based D-latch, LSEH-1, and the proposed D-latches reveals the superior performance of the proposed D-latch and a lesser impact from temperature and process variability in terms of transistor threshold

voltage and aspect ratio. The standard deviation improvement of threshold voltage transistor variability impact on the delay is improved by 3.2%, whereas its impact on the power consumption is improved by 9.1%. Furthermore, it has been shown that the standard deviation improvement of (W/L) transistor variability on the power consumption is 56.2%. Finally, the additional benefits do not come at the expense of a significative increase in cost (PDP, power consumption, area, delay) in comparison to the other hardened alternatives.

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Appendix A

To show how the temperature effects on delay, the following coefficient can be defined.

$$\alpha = \frac{\left(delay - delay_{ref}\right)}{\left(T - T_{ref}\right) delay_{ref}} \tag{A1}$$

In (A1), reference temperature is 20 °C and α is the delay coefficient by temperature, which is calculated for different D-latches and the proposed D-latch in Table 3.A1. As can be seen, the delay coefficient of the proposed D-latch is lower than those of the other alternatives.

Table 3.A1. Comparative delay coefficient by temperature of D-latches.

D-Latch	Proposed	Static	TPDICE	DICE	LSEH-1[7]
Delay coefficient by temperature	0.0028	0.0032	0.0034	0.0031	0.053

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Chapter 4

Highly Reliable Quadruple-Node-Upset-Tolerant D-Latch

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Highly Reliable Quadruple-Node-Upset-Tolerant D-Latch

Abstract: As CMOS technology scaling pushes towards the reduction of the length of transistors, electronic circuits face numerous reliability issues, and in particular nodes of D-latches at nano-scale confront multiple-node upset errors due to their operation in harsh radiative environments. In this manuscript, a new high reliable D-latch which can tolerate quadruple-node upsets is presented. The design is based on a low-cost single event double-upset tolerant (LSEDUT) cell and a clock-gating triple-level soft-error interceptive module (CG-SIM). Due to its LSEDUT base, it can tolerate two upsets, but the combination of two LSEDUTs and the triple-level CG-SIM provides the proposed D-latch with remarkable quadruple-node upsets (QNU) tolerance. Applying LSEDUTs for designing a QNU-tolerant D-latch improves considerably its features; in particular, this approach enhances its reliability against process variations, such as threshold voltage and (W/L) transistor variability, compared to previous QNU-tolerant D-latches and double-node-upset tolerant latches. Furthermore, the proposed D-latch not only tolerates QNUs, but it also features a clear advantage in comparison with the previous clock gating-based quadruple-node-upset-tolerant (QNUTL-CG) D-latch: it can mask single event transients. Specific figures of merit endorse the gains introduced by the new design: compared with the QNUTL-CG D-latch, the improvements of the maximum standard deviations of the gate delay, induced by threshold voltage and (W/L) transistors variability of the proposed D-latch, are 13.8% and 5.7%, respectively. Also, the proposed D-latch has 23% lesser maximum standard deviation in power consumption, resulting from threshold voltage variability, when compared to the QNUTL-CG D-latch.

Index Terms: Power-Delay Product (PDP), Soft Errors (SE), Single Event Upset (SEU), High Impedance State (HIS), Single Event Transient (SET), Dual Interlocked storage Cell (DICE), Triple Path DICE (TPDICE), Quadruple-Node Upsets (QNUs).

4.1 Introduction

Nano-scaling integrated circuits and systems rises a sensitivity challenge to soft errors generated by radiation-induced charges when the size of the transistors is reduced [1]. There are different designs of hardened D-latch against soft errors such as single-node upsets [2] and double-node upsets (resulting from a striking particle injected to double nodes [3], [4], [5]). Furthermore, the reduction of transistor size can cause a striking particle to affect multiple nodes (more than two). This effect can cause multiple-node upsets (MNUs), leading to triple-node upsets [6] and quadruple node upsets [7]. This represents a huge concern to design reliable storage modules, specially for their safe application when used in harsh radiative environments [8].

There is a lot of investment in hardened circuit structures to reduce the side effect of soft errors. These circuits comprise memory cells [9], [10], flip-flops [11], [12], and latches [13]. But yet most of the existing hardening approaches face limitations; for example, some hardened D-latches cannot recover reliably after flipping, even if the output node stores its value. Some D-latch designs have overcome this drawback proposing complete self-recovery after single-node upset (SNU) [14]. However, even if they can self-recover from SNU, they cannot recover fully against double-node upset (DNU). Later in time some of DNU hardened D-latches [15] have been proposed to face this issue, nonetheless, in their designs there is one-pair of their nodes that cannot tolerate high charges, which means they are not completely DNUs self-recoverable. One step beyond is given in [5], [16], [17], [18], where DNU D-latches able to fully self-recover are presented, however, those designs are lacking the triple-node-upset (TNU) tolerance. This latter challenge has been addressed in [8], [19] where TNU can be tolerated but not self-recovered. By the best knowledge of the authors of this manuscript, there is not a complete self-recovery TNU D-latch [20]. Finally, there are some recent quadruple-node-upset-tolerant D-Latch (QNU) designs [7], [21] which are not self-recoverable.

Since D-latches have a long holding time due to power consumption constraints, the possibility of being affected by striking particles in rigid conditions, such as QNUs is always present. The importance of QNU is supported by the fact that only double-node upset D-latches can be fully self-recovered and there are not TNU D-latches that can be fully recovered. If a DNU-tolerant D-latch is affected by TNU, as it cannot recover itself, the error will take place and the output will be not correct. As the holding time is long, the D-latch can be also affected by SNU; the combination of both TNU and SNU can lead to QNU. Based on the explanation in [8], the occurrence possibility of single event multiple upset (SEMU) or multiple event multiple upset (MEMU) increases sharply by reducing the size of transistors in nano-scale technology. Also, in [22], the authors demonstrate that CMOS technology below 90nm node has an unneglectable QNU probability, being this possibility dramatically increased below 40nm node.

The possibility of QNU happening in nano-CMOS circuits depends on different parameters, such as layout topology (using adjacent transistors decrease single event upset (SEU) probability [23], and using the master-salve interleaving approach enhances dual interlocked storage cell (DICE) against the SEU tolerance [24]), technology data [22], the type of particles, temperature environment, and supply voltage.

The above discussion of reliability issues of hardened D-latch has encouraged the development of a quadruple-node-upset-tolerant D-latch. In this manuscript, a low power consumption, single event transient (SET) filterable, and high reliable quadruple-node-upset-tolerant D-Latch is presented. The proposed D-latch consists of two connected low-cost single event double-upset tolerant (LSEDUT) cells [25], and a clock-gating triple-level soft error interceptive module (CG-SIM), which consists of three levels of CG-based 2-input C-elements connected to each other. Three nodes of each LSEDUT cell are connected to three inputs of the first stage of the CG-SIM. The second stage input of the CG-SIM is connected to the output of the first stage of the CG-SIM and the output of the second stage of the CG-SIM is connected to the third stage of the CG-SIM. Following the strategy of the LSEDUT latch in [25], implementing a triple-input Muller C-element (TMCE) to filter soft errors, the proposed D-latch features two LSEDUT cells, and a triple-level CG-SIM is used to perform the same function as TMCE of LSEDUT D-latch. The simulation results show that any QNUs for all internal and output nodes can be tolerated. Also, this latch can filter SET pulses in the transparent mode and there is not high impedance state (HIS) at the output node.

The manuscript is organized as follows: Section 4.2 revisits previous approaches of hardened D-latches. In Section 4.3, the proposed D-latch design, immunity, characteristics, and implementation are presented. In Section 4.4, simulation results on the robustness and a comparison with previous latches are reported, followed by the conclusions in Section 4.5.

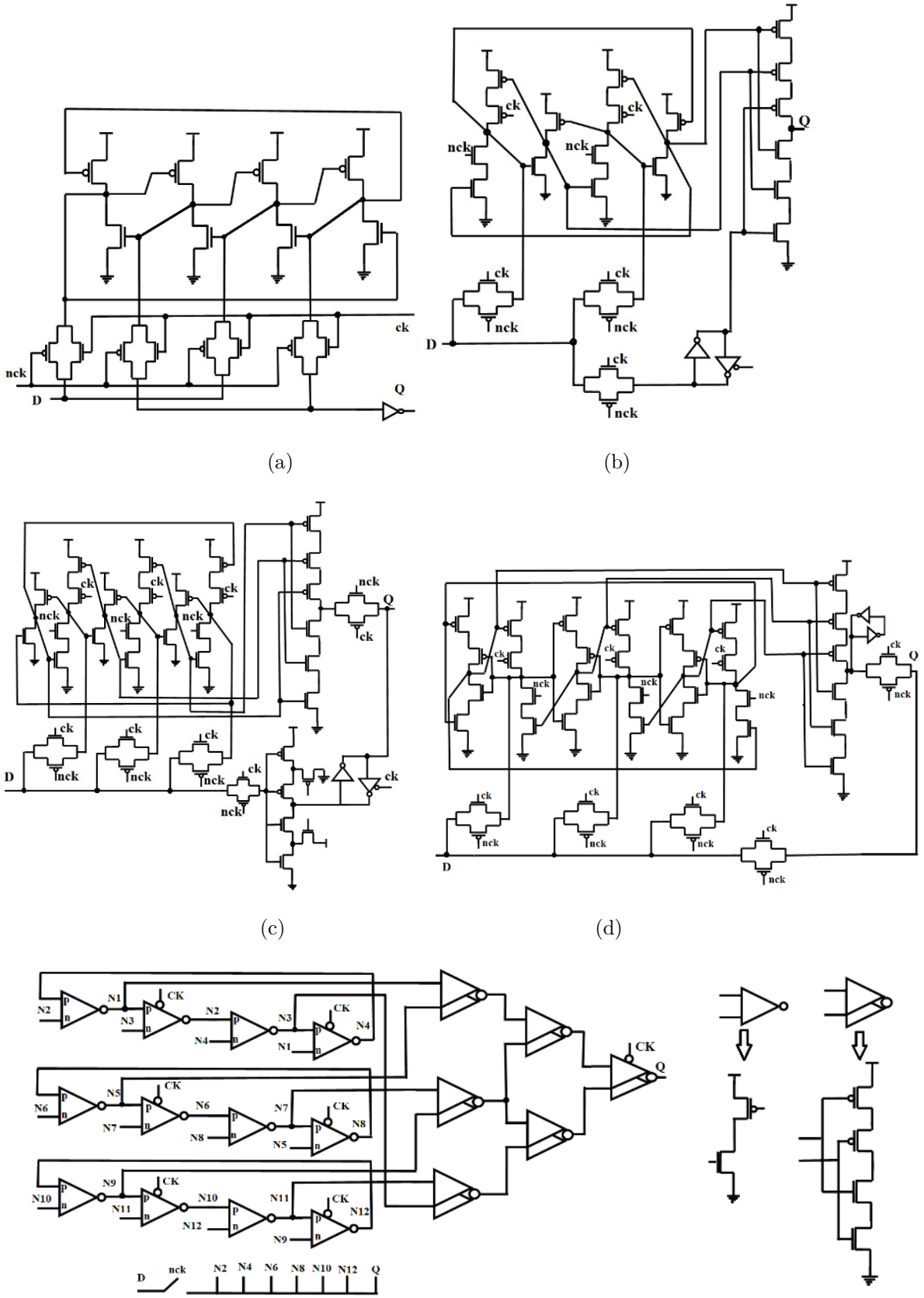
4.2 Previous Hardened D-latch

4.2.1 DICE

Many techniques have been presented to mitigate SNU in D-latches and among those hardened D-latches, DICEs are very effective [26]. In Fig. 4.1a, the schematic of a DICE structure is shown. This structure can recover from any SNU and it is self-recoverable to the DNUs in some nodes.

4.2.2 CLCT

Circuit and layout combination technique (CLCT), which is shown in Fig. 4.1b, operates based on clock-gating technology, in which there are not positive feedback



(a) (b) (c) (d) (e)

Figure 4.1. (a) DICE [26]; (b) CTCL latch [15]; (c) TPDICE-based D-latch [27]; (d) LSEDUT D-latch [25]; (e) QNUTL-CG D-latch [7]

loops of its DICE in the transparent mode to prevent current competition in the output node [15]. The data at holding time can be retained in the DICE and keeper; then can be transferred to the output by a C-element tolerating both SNU and Single Event Double-Upset (SEDU).

CLCT [15] has a high impedance state in the output node when SNU or SEDU take place; for example, when SNU happens in the keeper or SEDU happens in CG-based DICE, the output goes to a high impedance state. Also, this D-latch is not fully hardened against SEDU.

4.2.3 TPDICE-based D-latch

Triple path DICE (TPDICE) is a hardened D-latch alternative with immunity against SET, SNU, DNU, and a HIS insensitivity [27], which is shown in Fig. 4.1c. In this structure, a TPDICE is used for retaining the data in holding time; furthermore, it includes a three-input C-element for filtering SEDU, an embedded Schmitt trigger inverter for filtering the SET in the transparent path, and a keeper for avoiding a high impedance state in the output node.

4.2.4 LSEDUT D-latch

Fig. 4.1d shows the LSEDUT latch having full use of its interlocked node character to make it reliable for saving data with a CG-based C-element to transfer the stored data to the output in holding time. A three-input C-element is used to filter SNU or SEDU, and a keeper to avoid a high impedance state [25]. This structure is based on the TPDICE but three transmission gates of the input are connected to four transistors, which yields a larger capacitance at the input node to store data in comparison with TPDICE in [27].

4.2.5 QNUTL-CG D-latch

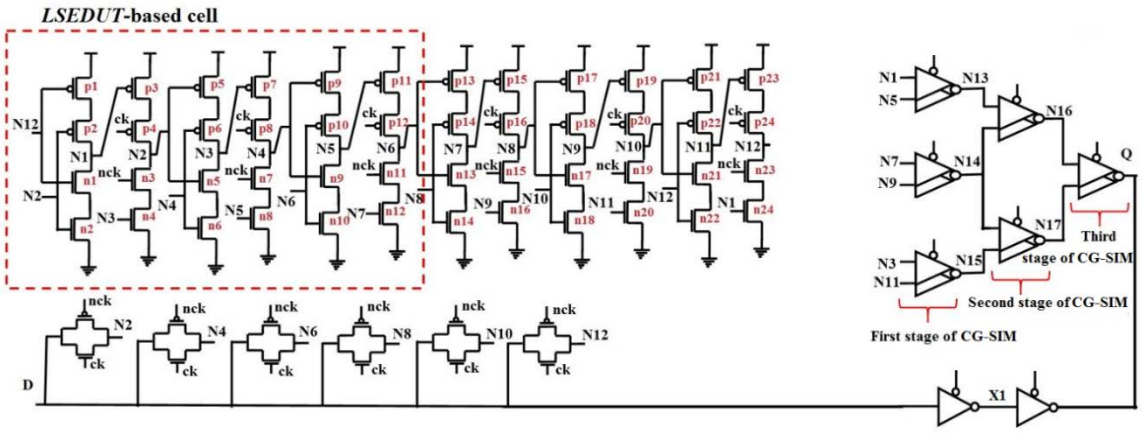
The clock gating-based quadruple-node-upset-tolerant latch (QNUTL-CG D-latch) has been presented against MNUs [7] and it is reproduced in Fig. 4.1e. This D-latch has three CG-based DICEs and a triple-level soft-error interceptive module (SIM) for filtering soft errors. Since CG-based DICE can tolerate SNU and these three-level C-elements can filter SNU, QNUTL is immune against the QNU.

4.3 Proposed D-latch

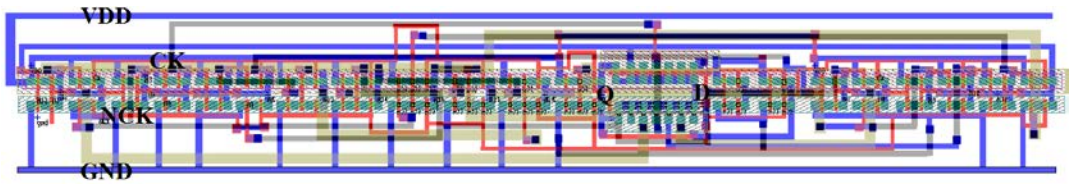
Fig. 4.2a shows the LSEDUT-based proposed D-latch with triple-level CG-SIM and two CG-inverters to filter SET in transparent mode. The layout of the device is shown in Fig. 4.2b. In this latch, D and Q are the input and output; ck and nck are the clock circuit and inverter clock circuit rails, respectively. When ck=1, nck=0, the latch works in the transparent mode and the gate of transistors connected to N2, N4, N6, N8, N10,

N12, and Q are charged or discharged by the D input through transmission gates. Then, the D input propagates through six 2-input C-elements and stablishes the values of N1, N3, N5, N7, N9, and N11. In the transparent mode, the positive feedback of the LSEDUT part is not active, and the triple-level CG-SIM is not connected to the output node to avoid current competition, which also decreases power consumption and delay. Moreover, this hardened D-latch has SET-filtering feature in transparent mode. If a SET arrives at D from a previous combinational part before the D-latch, it will pass through the CG-inverter and will arrive at x1 node reversing the SET. Then, by passing through the second CG-inverter and achieving the Q node, the SET is filtered by the delay introduced by these two inverters. For example, if SET comes and D becomes low, a positive SET (low-high-low) at x1 will appear. But, the right value of x1 is low and the NMOS transistor of the second inverter is off. Therefore, the value of Q cannot change until x1 becomes high, which needs time to charge the NMOS capacitors of the second inverter. In the transparent path, these two CG-inverters are applied to introduce delay for filtering the SET.

In the latching time, when ck=0 and nck=1, N2, N4, N6, N8, N10, N12, and Q are disconnected from the D input, however, two LSEDUTs with triple-level CG-SIM are connected to Q. This implies that Q is driven by a triple-level CG-SIM instead of the D input in the transparent path. Additionally, the feedback loops of each LSEDUT are activated to hold values. Therefore, the proposed D-latch can properly store values and drives valid values to the output node (Q). The output node does not present any HIS in the holding time when SNU, DUN, TUN, or QUN take place.



(a)



(b)

Figure 4.2. Proposed D-latch (a) schematic; (b) layout.

It is worth mentioning that the triple-level CG-SIM has three stages CG-3 input C-elements, which are less power demanding, but as this part does not connect to Q in transparent mode, the values of N13, N14, N15, N16, N17 are floating.

If any particle strikes at any node of the proposed D-latch as one SNU, this structure is self-recoverable like an LSEDUT latch. In the following subsections, we cover different situations where different levels of upsets occur at different nodes of the proposed D-latch and its immunity is systematically evaluated.

4.3.1 Immunity against SNU

Since the proposed design is very symmetric, N1, N3, N5, N7, N9, and, N11 have the same value (inverted input data) and N2, N4, N6, N8, N10, and N12 have the same value as the input value. Also, N13, N14, N15 have the same value as the input value (D-input passes through two inverters), and N16, N17 present the same value as the inverted value of the input. So, five different cases (e.g., N1, N2, N13, N16, and Q) should be investigated for a SNU. For the internal nodes of the LSEDUT, N1 or N2, if one of them suffers from a SNU, for example, N1 is affected when D=0 (N2=0, N1=1), then it will be discharged to 0, p3 is turned one, and N2 becomes unstable, but this charge cannot make N2 turn into high level, because n4 is ON; as the result, N1 and N2 can be recovered by N12 and N3, respectively. Even, if this charge is large enough to change the value of N2, it will be filtered by the tripe-level CG-SIM. This SNU cannot affect the output of the proposed D-latch. If any SNU affects the N2 node, the analysis of recovery is the same as for N1. When N13 or N16 are affected by SNU, as they are derived by LSEDUTs connected to the first stage of the CG-SIM, they can recover their value. If Q is affected by a SNU, it will flip temporarily, but as the LSEDUTs and the triple-level CG-SIM save their values and they are not affected by the SNU, therefore, Q will be recovered. As a summary, the proposed D-latch is immune against any SNUs.

4.3.2 Immunity against DNU

After evaluating against SNU, the immunity of the proposed D-latch against DNU is considered. As this circuit is symmetric, three cases can be studied for this immunity analysis. In the first case, when two nodes are inside of the LSEDUT, there are different analysis for the two pairs of nodes inside of LSEDUT [25], which yields three cases: 1a, 1b, and 1c.

Case 1a: if these pairs of nodes are inside of the LSEDUT and the triple-level CG-SIM is not affected by DNU. There are six key pairs of LSEDUT nodes [25]. These pairs are (1) <N1, N2>, <N3, N4>, <N5, N6>, <N7, N8>, <N9, N10>, and <N11,

N12>, which have the same situation against DNU. The explanation of their immunity is as follows. When D=0, N2, N4, N6, N8, N12 are set on the low logic state and all of the PMOSs of the 2-input C-elements are turned ON, and, N1, N3, N5, N7, N9, and N11 are set to high logic state: if N1 and N2 are affected (N1 is discharged to 0 and N2 is charged to 1), n24 and p2 transistors are turned off and transistors p3, n2, n5 are turned ON. Since n6 is off, N3 cannot discharge through n5 to the ground. So other nodes in the LSEDUT except N1, and N2 are not affected by DNU, and then N1, and N2 self-recover from N12 and N3, respectively. This shows immunity of the proposed D-latch against DNU in case 1a.

Case 1b: in this case, the pairs inside the LSEDUT to be considered are (1) <N1, N4>, <N3, N6>, <N5, N8>, <N7, N10>, <N9, N12>; (2) <N2, N3>, <N4, N5>, <N6, N7>, <N8, N9>, <N10, N11>, <N12, N1>; (3) <N2, N5>, <N4, N7>, <N6, N9>, <N8, N11>, <N10, N1>, and <N12, N3>. When D=0, N4=0 and N1=1, if, for example, N1 and N4 are affected, N1 will become 0 and N4 will become 1, and n24, p6, and p9 will be turned off and p3, n6, and n9 will be turned ON. Since p3 is ON, N2 is unstable but N5 cannot discharge because n10 is turned off and there isn't any path through n9 to the ground. Although N2 is unstable, it cannot turn to high logic level by any SNU. N4 and N1 are self-recovered by N5 and N12, respectively. Even, if N2 is affected by SNU, it becomes high logic level, N2 and N4 can upset N3, which means that N2 and N4 cannot be self-recovered; however, this upset cannot change the value of N16 because N14 isn't affected. This shows immunity of the proposed D-latch against DNU in case 1b.

Case 1c: in this case, the two pairs affected are inside the LSEDUT including (1) <N1, N3>, <N3, N5>, <N5, N7>, <N7, N9>, <N9, N11>, <N11, N1> (2) <N2, N4>, <N4, N6>, <N6, N8>, <N8, N10>, <N10, N12>. If N1 and N3 are affected, for example when D=0, N2=0, and N1=1 and after charge injected to N1 and N3, N1 and N3 are discharged to "0", n24 and n4 are turned off and p3 and p7 are turned ON. This situation makes N2 to turn to the high logic level and n4 becomes unstable which means that N2 and N4 cannot be self-recovered. In spite of that, this soft error can be filtered by the triple-level CG-SIM and it will not appear at Q which means the proposed D-latch is immune against DNU in case 1c.

Case 2: DNU affects one node in the triple-level CG-SIM and one node of LSEDUTs. This situation for LSEDUTs and the triple-level CG-SIM is the same since they are affected by SNU. As the structure of the proposed D-latch is symmetric, the pairs that should be considered are <N1, N13>, <N1, N16>, and <N1, Q>. In this situation, as explained before if N1 is upset, N3 will not be affected and the LSEDUT is self-recovered from SNU; therefore, SNU in N1 cannot change the value of N13. Even if

there is a SNU in N13 simultaneously, as N14 is not affected by any DNU, N16 will not be affected and it would have the valid value, therefore Q will store its valid data. Also, other pairs of nodes in case 2 have the same analysis, which means that Q is immune against DNU in this case, therefore, this proposed D-latch is immune against DNU in case 2.

Case 3: the DNU affects only two nodes of the triple-level CG-SIM, and as the triple-level CG-SIM is symmetric, the following pairs of nodes should be considered, <N13, N14>, <N13, N16>, <N13, N17>, <N13, Q>, <N16, N17>, and <N16, Q>. As the LSEDUTs of the D-latch is not affected by DNU and they have valid data, the data of N1, N3, N5, N7, N9, N11 are valid and they can recover the data of the triple-level CG-SIM and Q after being affected by the charge injected. This recovery means that the proposed D-latch is immune against DNU in case 3.

When D=1, the performance of the proposed D-latch is similar to the case when the input data is D=0. This structure is immune against DNU when two charges are injected inside of the LSEDUTs and the triple-level CG-SIM.

4.3.3 Immunity against TNU

In this section, we detail the characteristics that make the proposed D-latch immune against TNU. For this test, there are four cases described below:

Case 1: there is no charge affecting the LSEDUTs and all three charges affect the triple-level CG-SIM. As the SIM is a symmetric circuit, only five triplets of nodes should be considered for TNU, being those <N13, N14, N15>, <N13, N14, N16>, <N13, N14, N17>, <N13, N16, Q>, and <N16, N17, Q>. As for all of these situations LSEDUTs are not affected, therefore, N1, N3, N5, N7, N11 have valid values and the LSEDUTs can recover the value of the triple-level CG-SIM and Q. This means that the proposed D-latch is immune against TNU in case 1.

Case 2: one charge affects one node of the LSEDUTs and the two other charges affect the triple-level CG-SIM. As the circuit is symmetric, five situations should be considered, being those <N1, N17, Q>, <N1, N13, N14>, <N1, N13, N16>, <N1, N13, Q>, and <N1, N16, N17>. This situation for the LSEDUTs is similar to the case when the LSEDUTs experiences an SNU and as it was explained, the LSEDUTs are immune against SNU and they can tolerate SNU. As LSEDUTs can be self-recovered from SNU, N1, N3, N5, N7, N9, and N11 have valid values and even if two charges are injected into the triple-level CG-SIM, these two nodes can be recovered by the LSEDUTs. Therefore, this TNU cannot change the value of Q and the proposed D-latch is immune against TNU in case 2.

Case 3: two charges injected to the LSEDUTs and one charge injected to the triple-level CG-SIM. As the proposed D-latch has a symmetric structure, there are six groups of triplets of nodes that must be considered under this situation: <N1, N2, N13>, <N1, N2, N16>, <N1, N2, Q>, <N1, N3, N13>, <N1, N3, N16>, and <N1, N3, Q>, <N1, N4, N13>, <N1, N4, N16>, and <N1, N4, Q>. In the DNU section, it was explained how <N1, N2> can be self-recovered whenever there is a DNU injected into the LSEDUT. Therefore, the LSEDUT has valid values and N1, N3, N5, N7, N9, N11 have valid values to launch the triple-level CG-SIM, which can be recovered from LSEDUTs. Also, if two charges are injected to the case of <N1, N3>, even if they lose their value, Q cannot change its value because N5, N7, N9, N11 do not lose their values. The values of N13, N14, and N15 are not changed by the upset of N1 and N3 because they are connected to different C-elements of the CG-SIM and they cannot change the value of N13 or N15. If N13 is upset, it could not change the value of N16 and Q either. The case of <N1, N3, N16> follows the same analysis since N1 and N3 cannot change the value of the triple-level CG-SIM and if N16 is upset and loses its data, still N17 has a valid value, which means that Q will retain the valid value. Also, for the case of <N1, N3, Q>, as the charges injected to N1 and N3 cannot change the value of N13, N14, and N15, these nodes have valid data and even if Q becomes upset due to the charge injection, it can recover by N16 and N17, which have valid data. As the result, Q maintains its value and the proposed D-latch is immune against TNU in case 3.

Case 4: three charges injected to the LSEDUTs and due to the symmetric structure, there are six situations to be considered: <N1, N2, N3>, <N1, N2, N7>, <N1, N3, N4>, <N1, N3, N7>, <N2, N3, N4>, <N2, N3, N7>. We consider first the case of D=0, N2=0, N1=N3=1, (n2, p3, p7 are off and n4, p2, p5 are ON). If charges are injected to N1, N2, N3, they will lose their data and N2=1, N1=N3=0. In this situation, p3, n5, and p7 are ON, and n24, p2, p5, n4 are off; therefore, N4 is unstable and N1, N2, N3 cannot recover their data, but nodes N5, N7, N9, and N11 do not lose their data and have valid values. Therefore, N13, N14, and N15 do not lose their values and N16 and N17 have valid values, which implies that Q maintains its valid value and therefore, these soft errors cannot change the value of the proposed D-latch. The next case of triplet should be considered is <N1, N2, N7> being D=0, N2=0, N1=N7=1, and n24, n12, p5, and p2 are ON and p3, p15, n2, and n5 are off. If there is any charge injected to N1, N2, N7, and their values change to N2=1, N1=N7=0 as a consequence, p3, p15, n2 will be ON and n24, p5, n12, will be off and N3 will become unstable; however, this situation will not change the value of N3, and N12 because N4, and N11 are not affected by these charges. Since only N1 and N7 are affected and N3 and N11 are not affected, these soft errors can be filtered by the first stage of the CG-SIM, and the value of N13, N14, and N15 are valid. Therefore, Q has a valid value, which means

these charges injected do not affect the value of Q. For <N1, N3, N4>, <N1, N3, N7>, <N2, N3, N4>, and <N2, N3, N7> groups of nodes, the same analysis holds. As a result, the proposed D-latch is immune against TNU in case 4.

4.3.4 Immunity against QNU

In this section, we detail the immunity against QNU of the proposed D-latch in five cases, which is described as below:

Case 1: all four charges injected to the triple-level CG-SIM and none of the charges is affecting the LSEDUTs. This situation has three quadruplets of nodes to be analyzed <N13, N14, N16, Q>, <N13, N14, N15, N16>, <N13, N16, N17, Q>. In the <N13, N14, N16, Q> case, there is a temporary flip of state in N13, N14, N16, but these nodes can be recovered by the LSEDUTs which are not affected by the QNU and N1, N3, N5, N7, N9, and N11 have valid values. Thus, the value of N13 and N14 can be recovered and then, N16 can be recovered from N13 and N14. In the end, Q can be recovered through N16 and N17 after the temporary flip. The quadruplet <N13, N14, N16, Q> can recover from the QNU, and the two other quadruplets have the same analysis, which means that the proposed D-latch is self-recovered from QNUs in case 1.

Case 2: one node of LSEDUTs is affected by the charge injected, and three other charges are injected to the triple-level CG-SIM. As the proposed D-latch is symmetric, these situations should be considered: <N1, N13, N16, Q>, <N1, N13, N14, N16>, <N1, N14, N16, N17>, and <N1, N13, N14, N15>. When one charge is injected into an LSEDUT node, such as N1, the node can recover; then as LSEDUTs can be self-recovered, so do N1, N3, N5, N7, N9, and N11 having yet valid values, and even if the triple-level CG-SIM is affected by three charges injected to different nodes, Q can be recovered by the LSEDUTs. As a result, the proposed D-latch is immune and self-recoverable against QNU in case 2.

Case 3: two nodes of the LSEDUTs are affected by QNU, and two other charges affect the triple-level CG-SIM. For this case, these node quadruplets should be considered: <N1, N5, N13, N16>, <N1, N5, N16, N17>, <N1, N5, N14, N15>, and <N1, N5, N17, Q>. As the LSEDUT is not self-recoverable when charges are injected to N1 and N5, in this case, there is a soft error. This soft error can affect the value of N13 and when N14 is affected by the charge injected, they can change the value of N16. But, as the triple-level CG-SIM has six inputs and despite the fact that two of them lose their value, the four others keep their valid values, in this case, N3, N7, N9, and N11 do not lose their values and N17 has valid value; therefore, Q is not being affected by these soft errors. Moreover, in the case of <N1, N5, N16, N17>, a similar explanation holds

considering soft errors in N1 and N5. The value of N13 is affected by these soft errors and N13 is upset, but despite the soft errors in N16 and N17 and the potential effect on Q, this effect is temporary because N3, N7, N9, and N11 hold valid values, and therefore can recover the values of N16 and N17. The value of Q can be recovered by the last stage of the CG-SIM, which means that the output is not affected by QNU. In the cases <N1, N5, N14, N15>, and <N1, N5, N17, Q>, the analysis is the same and the value of Q is not affected by QNU. Therefore, QNU cannot induce a change of the value of Q in the proposed D-latch, which is immune against QNU in case 3.

Case 4: in this case, three charges affect the LSEDUTs and just one charge is affecting the triple-level CG-SIM. In this situation, the quadruplets of nodes <N1, N3, N5, N13>, and <N1, N5, N7, N13> should be analyzed. If three charges are injected into one LSEDUT, it cannot be self-recovered from the TNU. Therefore, there will be soft errors taking place in one LSEDUT. When N1, N3, and N5 lose their values, N13 is upset by QNU, but this soft error cannot change the value of N16 because N14 has a valid value. As a consequence, these soft errors cannot change the value of the output and the proposed D-latch which will remain immune against QNU in case 4.

Case 5: in this case, all of the charges are affecting the LSEDUTs. These lists of nodes can be considered for the analysis, <N1, N2, N3, N4>, <N1, N3, N7, N9>, and <N1, N3, N5, N7>. In this situation, the four charges can affect one LSEDUT, as <N1, N2, N3, N4> or three of them like <N1, N3, N5, N7>, or just two charges injected affect one LSEDUT like <N1, N3, N7, N9>. For the situation <N1, N3, N7, N9>, if two charges are affecting N1 and N3, they cannot recover by themselves and there are soft errors taking place in the LSEDUT. Also, N7 and N9 will have the same situation and they could not recover by themselves. This situation produces soft errors at the first stage of the triple-level CG-SIM and as N1, N3, N7, and N9 are upset, N14 upsets and loses its value. Nevertheless, these soft errors cannot change the value of N15 and N13 because N5 and N11 do not lose their values. The upset of N14 cannot change the value of N16, because N13 has the valid value. Consequently, Q is not affected by QNU. Other cases follow the same analysis and as a result, the proposed D-latch is immune against QNU in case 5.

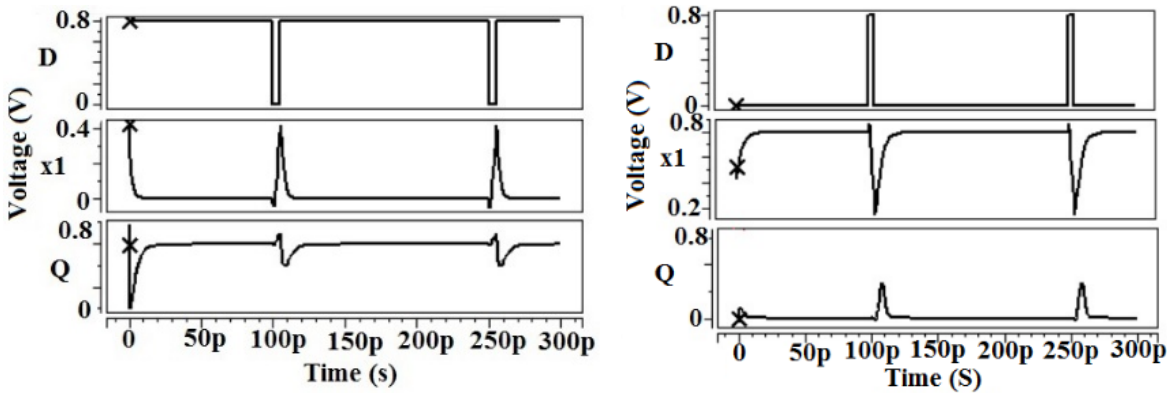
4.4 Simulation

In this section, the DICE [26], TPDICE-based D-latch [27], high performance SEU tolerant (HPST) latch [28], DNUCT [29], LSEDUT D-latch [25], QNUTL-CG D-latch [7], 4NUHL latch [30], and the proposed D-latch are simulated at 0.8 V supply voltage and 250 MHz frequencies at room temperature using Synopsys® HSPICE in 22 nm PTM technology. In this simulation, PMOS transistors have an aspect ratio W/L =

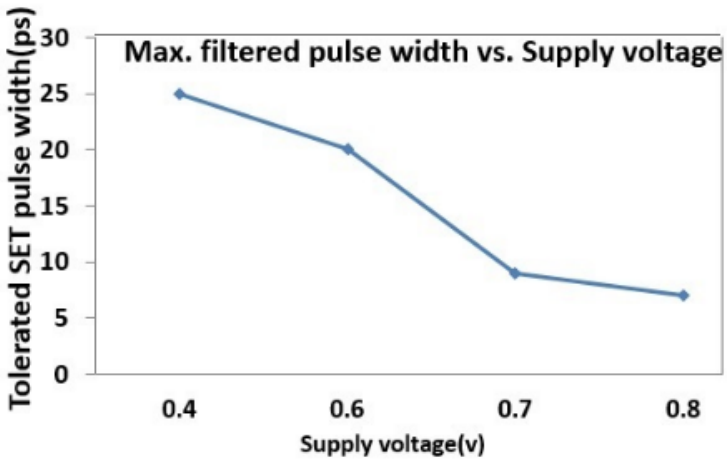
35 nm/22 nm, and NMOS transistors have an aspect ratio W/L = 24 nm/22 nm.

First, SET masking capability of the designed D-latch is tested. The proposed D-latch can filter undesirable pulses which are generated in the combinational digital circuit of previous D-latch stages. In the transparent mode, SET can be filtered by two clock-gating inverters in the direct path, which increases the delay but gives the extra feature to the proposed design. In Fig 4.3a and 4.3b, the input square positive and negative signals with 8 ps wide SET pulse at 0.8 V are shown demonstrating how this D-latch is designed to filter the SET pulse with the input signal in transparent mode (CLK=1), based on simulation on [29].

As the SET filtering depends on the supply voltage, the maximum width of SET pulses filtered by the proposed D-latch at different supply voltages is shown in Fig. 4.3c.



(a) (b)



(c)

Figure 4.3. (a) SET positive pulse filtering capability of the proposed D-latch; (b) SET negative pulse filtering capability of the proposed D-latch; (c) maximum pulse width of SET filtered by the proposed D-latch at various supply voltages.

4.4.1 Reliability comparison

One of the important test should be addressed is the evaluation of the proposed D-latch against SNU/DNU/TNU and QNU with a current transient (current source) simulating the charge injection given by the following mathematical expression [31]:

$$I = \frac{Q_{total}}{T\sqrt{\pi}} \sqrt{\frac{t}{T}} e^{-t/T} \tag{4.1}$$

In this simulation, T is the value of the time constant of the injected current charge, which is 0.3 ps. Q_{total} is the total charge injected being 50 fC in the worst case, which is large enough to prove immunity of the proposed D-latch against SNU/DNU/TNU and QNU [7].

For SNU simulation, one charge is injected to different nodes while the output node is monitored. When the output does not lose its logical value after this injection, it means it is immune against it. For DNU test, two charge injections are applied, three charge injections for TNU test, and four charge injections for QNU in different cases. As can be seen in Fig. 4.4, the output node does not change its value after SNUs, DNUs, and TNUs. Table 4.1 shows the key patterns of SNUs, DNUs, and TNUs used for the charge injection in Fig. 4.4. As can be seen, different key pattern injections of SNU, DNU, and TNU do not change the logical value of the output node, which means that the proposed D-latch is immune against SNUs, DNUs, and TNUs.

In Fig. 4.5, the simulation results of QNUs injection are shown. The pattern of injected QNUs is indicated in Table 4.2 in which “State” shows the value of the output node and “Time” shows the time of QNUs being injected into the proposed D-latch. As can be seen, the value of the output node does not change after the key patterns of QNUs are injected and proves that the proposed D-latch is immune against QNUs. But, this D-latch is not self-recoverable against QNUs.

Table 4.1. Key pattern of SNU, DNU, and TNU injections of the proposed D-latch in Fig.4.4.

Time (ns)	SNUs/ DNUs/ TNUs	State	Time (ns)	SNUs/ DNUs/ TNUs	State	Time (ns)	SNUs/ DNUs/ TNUs	State	Time (ns)	SNUs/ DNUs/ TNUs	State
5.15	N1	Q =1	16.0	Q	Q=0	26.8	N1, N16, N17	Q =1	36.0	N1, N13, N16	Q=0
5.2	N2	Q =1	16.2	N1, N2	Q=0	27.0	N1, N2, N13	Q =1	36.2	N1, N13, Q	Q=0
5.4	N13	Q =1	16.4	N1, N3	Q=0	27.2	N1, N2, N16	Q =1	36.4	N1, N16, N17	Q=0
5.5	N16	Q =1	16.6	N1, N4	Q=0	27.4	N1, N2, Q	Q =1	36.6	N1, N2, N13	Q=0
5.6	Q	Q =1	16.8	N2, N3	Q=0	27.6	N1, N3, N13	Q =1	36.8	N1, N2, N16	Q=0
5.7	N1, N2	Q =1	17.0	N2, N5	Q=0	27.8	N1, N3, Q	Q =1	37.0	N1, N2, Q	Q=0
5.8	N1, N3	Q =1	17.2	N2, N4	Q=0	28.0	N1, N3, N16	Q =1	37.2	N1, N3, N13	Q=0
5.9	N1, N4	Q =1	17.4	N1, Q	Q=0	28.2	N1, N2, N3	Q =1	37.4	N1, N3, Q	Q=0
6.0	N2, N3	Q =1	17.6	N13, Q	Q=0	28.4	N1, N2, N9	Q =1	37.6	N1, N3, N16	Q=0
6.2	N2, N5	Q =1	17.8	N1, N13	Q=0	28.6	N1, N3, N4	Q =1	37.8	N1, N2, N3	Q=0
6.4	N2, N4	Q =1	25.2	N13, N14, N16	Q =1	28.8	N1, N3, N9	Q =1	38.0	N1, N2, N9	Q=0
6.5	N1, Q	Q =1	25.4	N13, N14, N17	Q =1	29.0	N2, N3, N4	Q =1	38.2	N1, N3, N4	Q=0
6.6	N13, Q	Q =1	25.6	N13, N16, Q	Q =1	29.2	N13, N14, N15	Q =1	38.4	N13, N14, N16	Q=0
6.8	N1, N13	Q =1	25.8	N16, N17, Q	Q =1	29.4	N2, N3, N9	Q =1	38.6	N13, N14, N17	Q=0
15.2	N1	Q=0	26.0	N1, N17, Q	Q =1	35.2	N13, N16, Q	Q=0	38.8	N1, N3, N9	Q=0
15.4	N2	Q=0	26.2	N1, N13, N14	Q =1	35.4	N16, N17, Q	Q=0	39,0	N2, N3, N4	Q=0
15.6	N13	Q=0	26.4	N1, N13, N16	Q =1	35.6	N1, N17, Q	Q=0	39.2	N13, N14, N15	Q=0

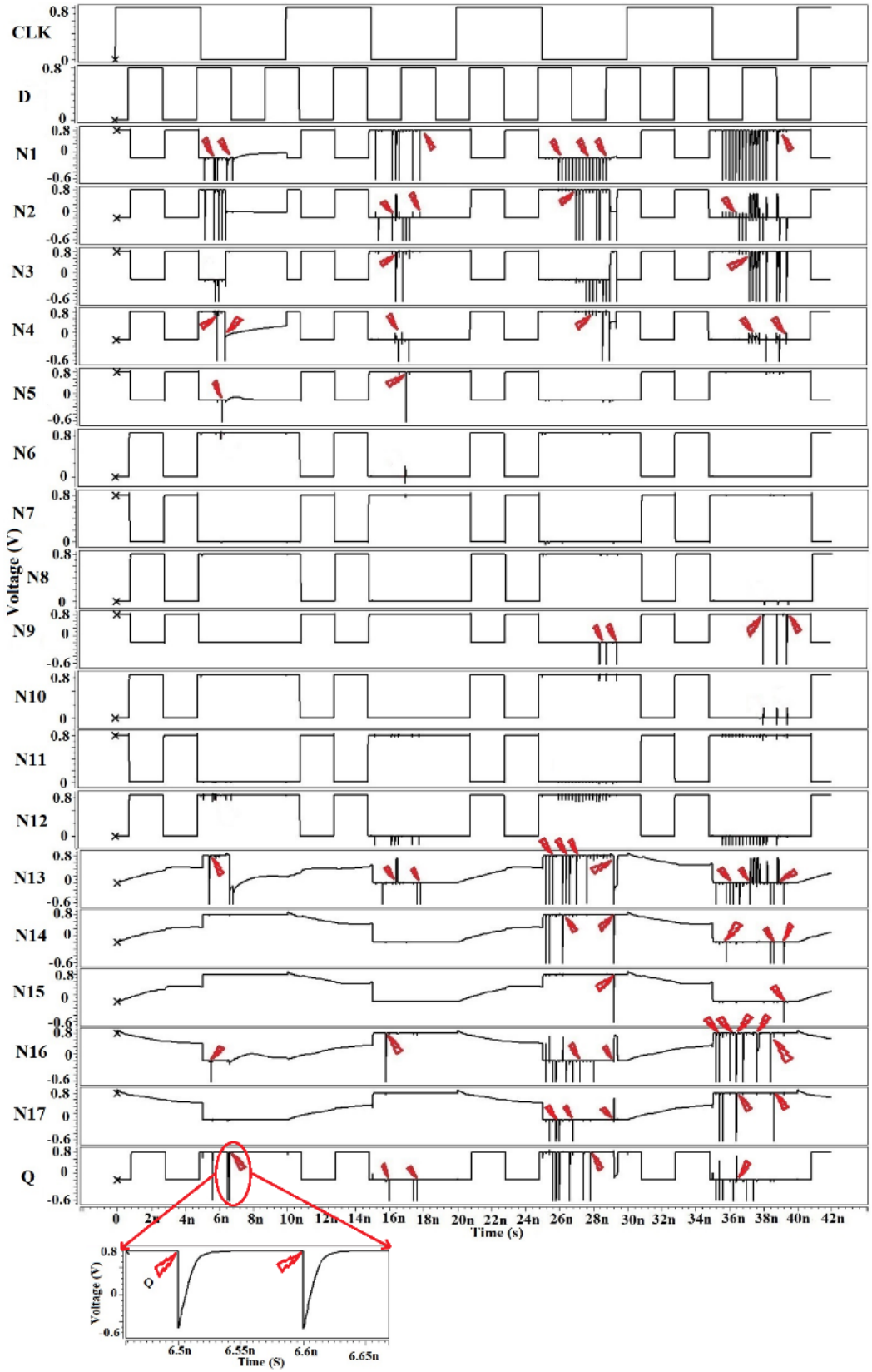


Figure 4.4. Simulation of the key patterns of SNU, DNU, and TNU injections for the proposed D-latch.

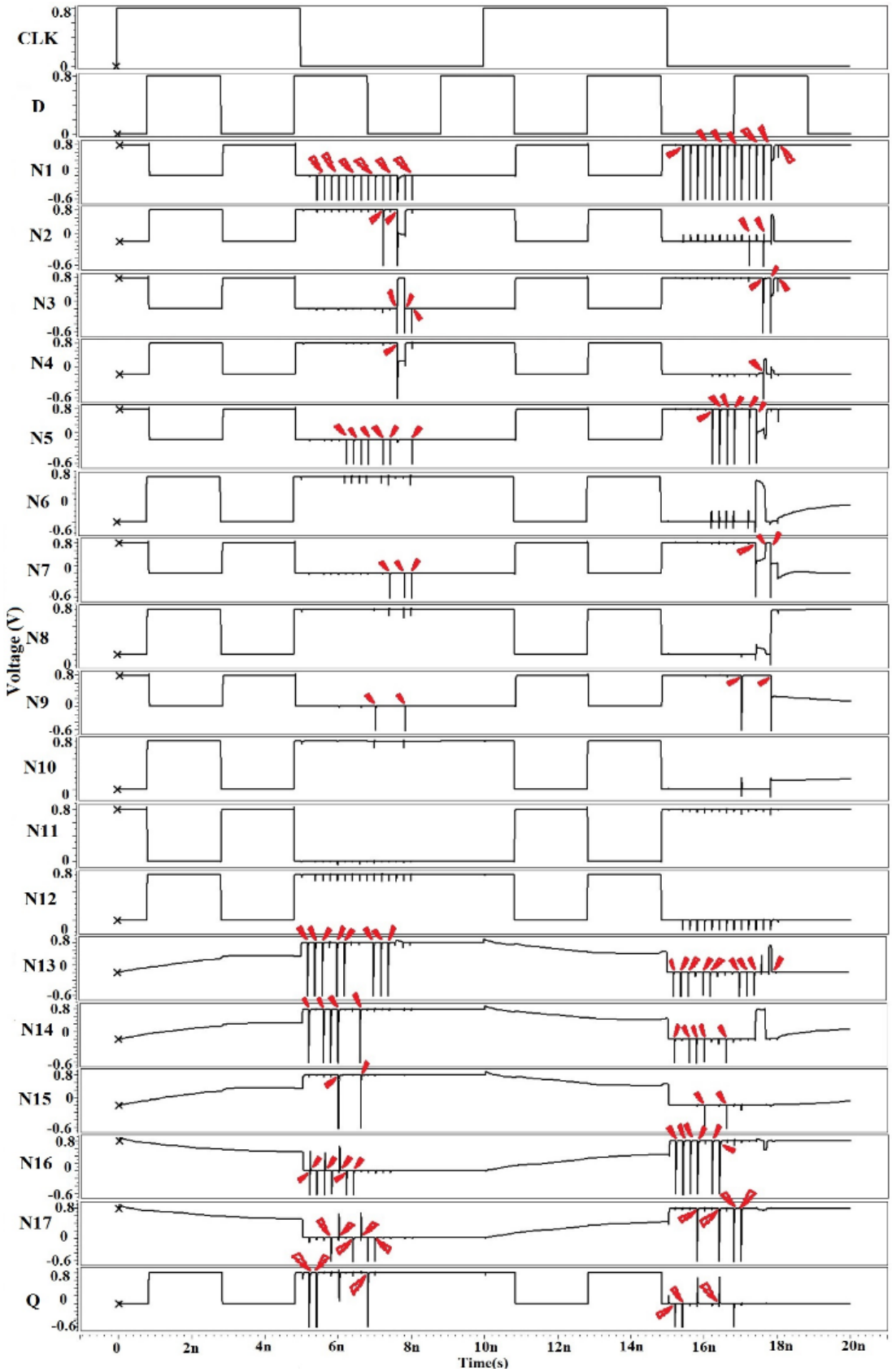


Figure 4.5. Simulation results of QNUs injected in the proposed D-latch

Table 4.2. Key patterns of QNUS injected in the proposed D-latch.

Time (ns)	QNUs	State	Time (ns)	QNUs	State	Time (ns)	QNUs	State
5.2	N13, N14, N16, Q	Q =1	7.2	N1, N2, N5, N13	Q =1	16.2	N1, N5, N13, N16	Q=0
5.4	N1, N13, N16, Q	Q =1	7.4	N1, N5, N7, N13	Q =1	16.4	N1, N5, N16, N17	Q=0
5.6	N1, N13, N14, N16	Q =1	7.6	N1, N2, N3, N4	Q =1	16.6	N1, N5, N14, N15	Q=0
5.8	N1, N14, N16, N17	Q =1	7.8	N1, N3, N7, N9	Q =1	16.8	N1, N5, N17, Q	Q=0
6.0	N1, N13, N14, N15	Q =1	8.0	N1, N3, N5, N7	Q =1	17.0	N1, N9, N13, N17	Q=0
6.2	N1, N5, N13, N16	Q =1	15.2	N13, N14, N16, Q	Q=0	17.2	N1, N2, N5, N13	Q=0
6.4	N1, N5, N16, N17	Q =1	15.4	N1, N13, N16, Q	Q=0	17.4	N1, N5, N7, N13	Q=0
6.6	N1, N5, N14, N15	Q =1	15.6	N1, N13, N14, N16	Q=0	17.6	N1, N2, N3, N4	Q=0
6.8	N1, N5, N17, Q	Q =1	15.8	N1, N14, N16, N17	Q=0	17.8	N1, N3, N7, N9	Q=0
7.0	N1, N9, N13, N17	Q =1	16.0	N1, N13, N14, N15	Q=0	18.0	N1, N3, N5, N7	Q=0

Table 4.3 summarizes the immunity against SNUs, DNUs, TNUs, QNUs, featuring a high impedance state at the output node, and SET filtering comparison between the proposed D-latch and previous hardened D-latches. The DICE, HPST D-latches are only immune against SNU, whereas the TPDICE-based D-latch, DNUCT, and the LSEDUT D-latch are just immune against SNU and DNU.

Moreover, the 4NUHL and QNUTL-CG D-latches present immunity against SNU, DNU, TNU, and QNU, but they are not capable of filtering SET. Besides, the proposed D-latch has full immunity against SNUs, DNUs, TNUs, and QNUs and it has two other beneficial features such as HIS insensitivity and SET filtering. Also, following this section, the simulation results of the process variations show that this design is more robust against (W/L) transistor aspect ratio and threshold voltage variability.

4.4.2 Cost comparison

To stablish a fair comparison, the previous hardened D-latches (DICE, HPST,

TPDICE-based D-latch, DNUCT, LSEDUT, 4NUHL, and QNUTL-CG D-latches) and the proposed D-latch are designed with the same PMOS and NMOS aspect ratios as stated at the beginning of Section 4.4, as the same strategy in [7]. Table 4.4 shows a comparison of D-latches related to area consumption, delays, power consumption, and PDP (Power-Delay Product), AOSF (ability of SET filtering), and minimum charge injections. These numbers are rounded.

As can be stressed out, the area penalty of the proposed D-latch is not unrestrained (especially compared to QNUTL-CG) and it provides better reliability. For example, DICE has 1 μm2 area consumption, but it has just immunity against SNU also is sensitive to high impedance state and cannot filter SET. The more recent D-latch, QNUTL-CG D-latch, is immune against SNU, DNU, TNU, and QNU, but it is not able to filter SET.

Another important parameter to be consigned is the (D-Q) delay and (CLK-Q) delay. As can be seen from Table 4.3, the two D-latches that can filter SET are the TPDICE-based D-latch and the proposed D-latch; this characteristic impacts on the delay, thus, the proposed D-latch does not feature the minimum delay (in the proposed D-latch, a Schmitt trigger inverter is not used as in the TPDICE-based D-latch because of its penalty on process variation and huge (D-Q) delay). Also, (D-Q) delay can be calculated just in the transparent mode because in the holding time mode, there is not any connection between input and D-latch. Moreover, the latch is working based on switching, therefore, the setup time for data should be calculated, which can be delay (D-Q) pulse to delay (clk-Q).

Table 4.3. Immunity against SNU, DNU, TNU, AND QNU, AND his insensitivity, and SET filtering of the proposed D-latches.

D-latch	Full Immune SNU	Full Immune DNU	Full Immune TNU	Full Immune QNU	HIS insensitive	Filtering SET
DICE [26]	✓	×	×	×	×	×
TPDICE based D-latch [27]	✓	✓	×	×	✓	✓
HPST [28]	✓	×	×	×	×	×
DNUCT [29]	✓	✓	×	×	✓	×
LSEDUT [25]	✓	✓	×	×	✓	×
QNUTL-CG [6]	✓	✓	✓	✓	✓	×
4NUHL [30]	✓	✓	✓	✓	✓	×
Proposed D-latch	✓	✓	✓	✓	✓	✓

Table 4.4. Comparative area of D-latches.

D-latch	Proposed D-latch	TPDICE-based	LSEDUT	DICE	QNUTL-CG	4NUHL	HPST	DNUCT
Area $(\mu m)^2$	4.6	2.1	2.1	0.9	3.9	3.3	0.94	3.1
Power consumption (μW)	0.5	1.0	3.0	0.74	0.5	4.3	0.18	0.53
(D-Q) Delay (ps)	8.3	11.8	0.56	18.2	0.53	0.48	0.48	0.53
(CLK-Q) Delay (ps)	4.47	9.8	0.65	21.62	0.62	0.57	0.56	0.63
Delay(set up data) (ps)	12.77	21.6	1.21	39.82	1.15	1.05	1.04	1.16
PDP $(10^{-18} \times W)$	4.27	12	1.7	13.4	0.3	2.1	0.09	0.28
AOSF	84.3%	67.8%	-	-	-	-	-	-
Qcrit (fc)	20	10	6	4	10	15	6	5

One of important parameter for benchmarking the proposed D-latch SET filtering is AOSF (ability of SET filtering), defined in [1]. This parameter is calculated from the ratio of maximum width of filtering SET divided by delay (D-Q) (in percentage). The better AOSF of the proposed D-latch compared to the TPDICE-based latch is due to the huge delay introduced by the Schmitt trigger (despite it features a better SET filtering).

Based on the reliability of the hardened D-latch against charge injections, the minimum charge injections that can produce SNU in different nodes of latches are calculated [32].

As the proposed D-latch is designed based on clock-gating C-elements and uses two different paths for transparent mode and holding time mode, the power consumption is much lower in comparison with the TPDICE-based D-latch, DICE, LSEDUT, DNUCT, 4NUHL D-latches, and features the same power consumption that QNUTL-CG, even if it has extra sub-circuit to filter SET.

4.4.3 Process variation

Due to the technology scaling race, process variability has become one challenging issue for integrated circuits [33]. In this section, we carry out a comparison of the impact on the gate delay and power consumption of the process variability induced by (W/L) and transistor threshold voltage fluctuations in the proposed D-latch and some of previous D-latches. For this comparison, Monte Carlo simulations with Gaussian

distribution are used to model (W/L) and threshold voltage variability [33]. The maximum deviations of the original value of (W/L) and threshold voltages are between 2% to 16% with 20 simulations [33]. These simulations are run for each of these deviations, and the effects of these variations are monitored on power consumption and delay.

In Fig. 4.6, the effect of threshold voltage variability on delay is shown. As can be seen, the threshold voltage variability has a lesser impact on the delay variation in the proposed D-latch compared with other existing hardened D-latches. The maximum standard deviations of gate delays are given in the insets for each D-latch. These numbers for the proposed D-latch, TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 0.0336, 0.035, 0.0407, 0.623, and 0.039, respectively. Furthermore, the maximum variance of the gate delay of the proposed D-latch, TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 0.0452, 0.046, 0.0534, 0.974, and 0.051, respectively. This comparison demonstrates that the delay of the proposed D-latch has less variation when threshold voltages of transistors are changed. The maximum standard deviation improvements of the gate delay of the proposed D-latch compared with TPDICE- based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 4%, 17.4%, 94.6%, and 13.8%, respectively. The maximum variance improvements of the gate delay of the proposed D-latch compared with TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 1.7%, 15.3%, 95%, and 11.3%, respectively.

In Fig. 4.7, the power consumption of the proposed D-latch, TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch is shown when the threshold voltages of the transistors are subjected to variability reproduced with Monte Carlo simulations. The maximum standard deviations of power consumption of the proposed D-latch, TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 0.0392, 0.17, 0.057, 0.159, and 0.051, respectively. The maximum variance of the power consumption of the proposed D-latch, TPDICE- based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 0.0563, 0.23, 0.0688, 0.214, and 0.071, respectively. The result of this comparison shows that the variance and standard deviation of the power consumption are minimum for the proposed D-latch. The maximum standard deviation improvements of the power consumption for the proposed D-latch compared with TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 76.9%, 31%, 75%, and 23%, respectively. The maximum variance improvements of the power consumption of the proposed D-latch compared with TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 75%, 18%, 73.6%, and 20.7%, respectively.

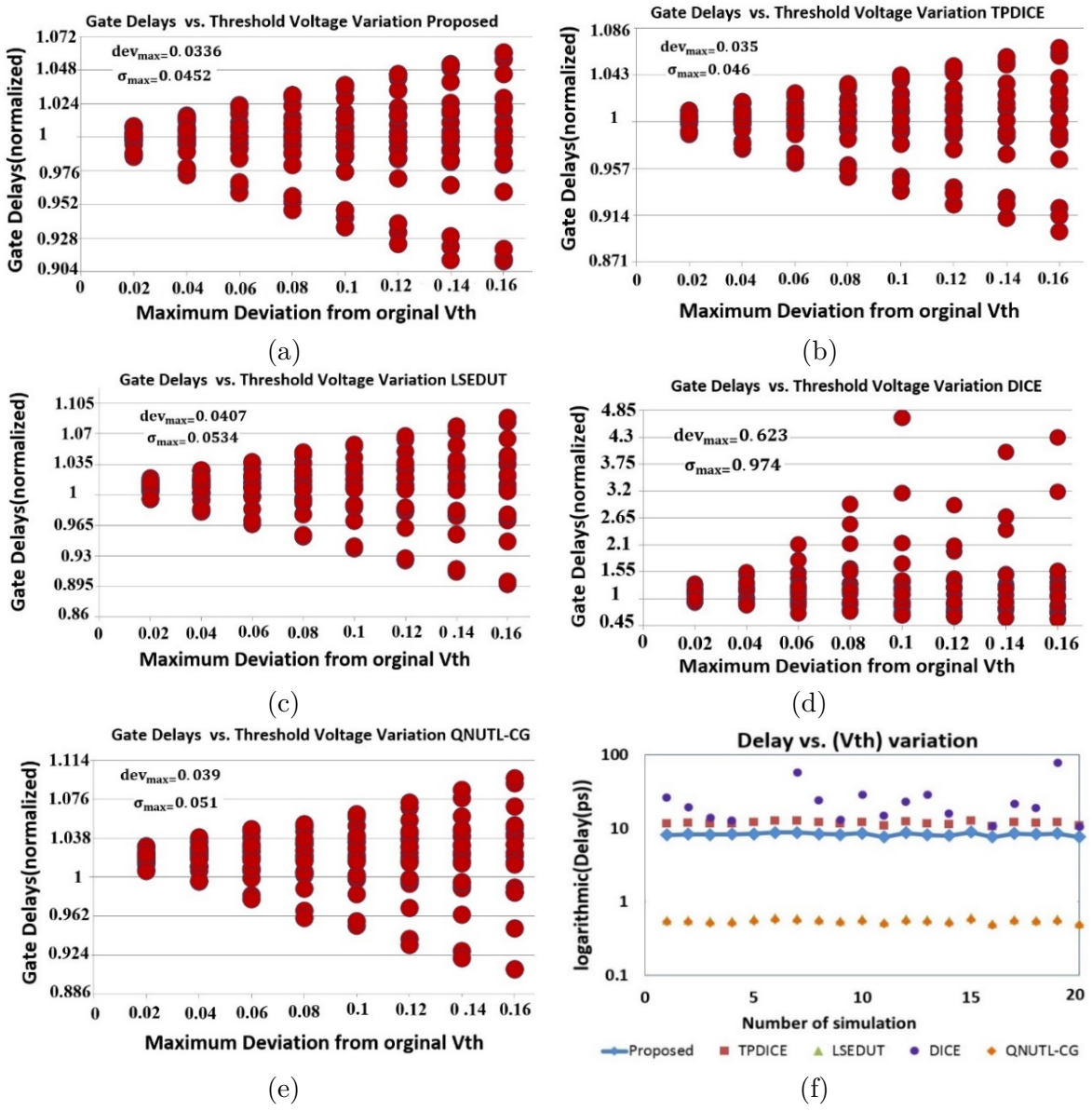


Figure 4.6. Threshold voltage variation effect on the D-latch delay: (a) proposed D-latch; (b) TPDICE-based D-latch; (c) LSEDUT latch; (d) DICE; (e) QNUTL-CG latch; (f) delay of D-latches with maximum deviation, 0.16, from original threshold voltage

The lower impact from process variation can be attributed to the non-active feedback loop in transparent mode, as the positive feedback loop increases the circuit sensitivity to parameters of process variations [34-35]. Also, to filter SET in the transmission mode, two inverters are applied in this proposed D-latch instead of Schmitt trigger circuit which is used in the TPDICE-based D-latch [27] (the Schmitt trigger inverter, due to the hysteresis property, impacts noticeably on parameters related to process variation). Also, the heavy use of stacked transistors decreases the impact of process variation parameters on delay and power consumption [3].

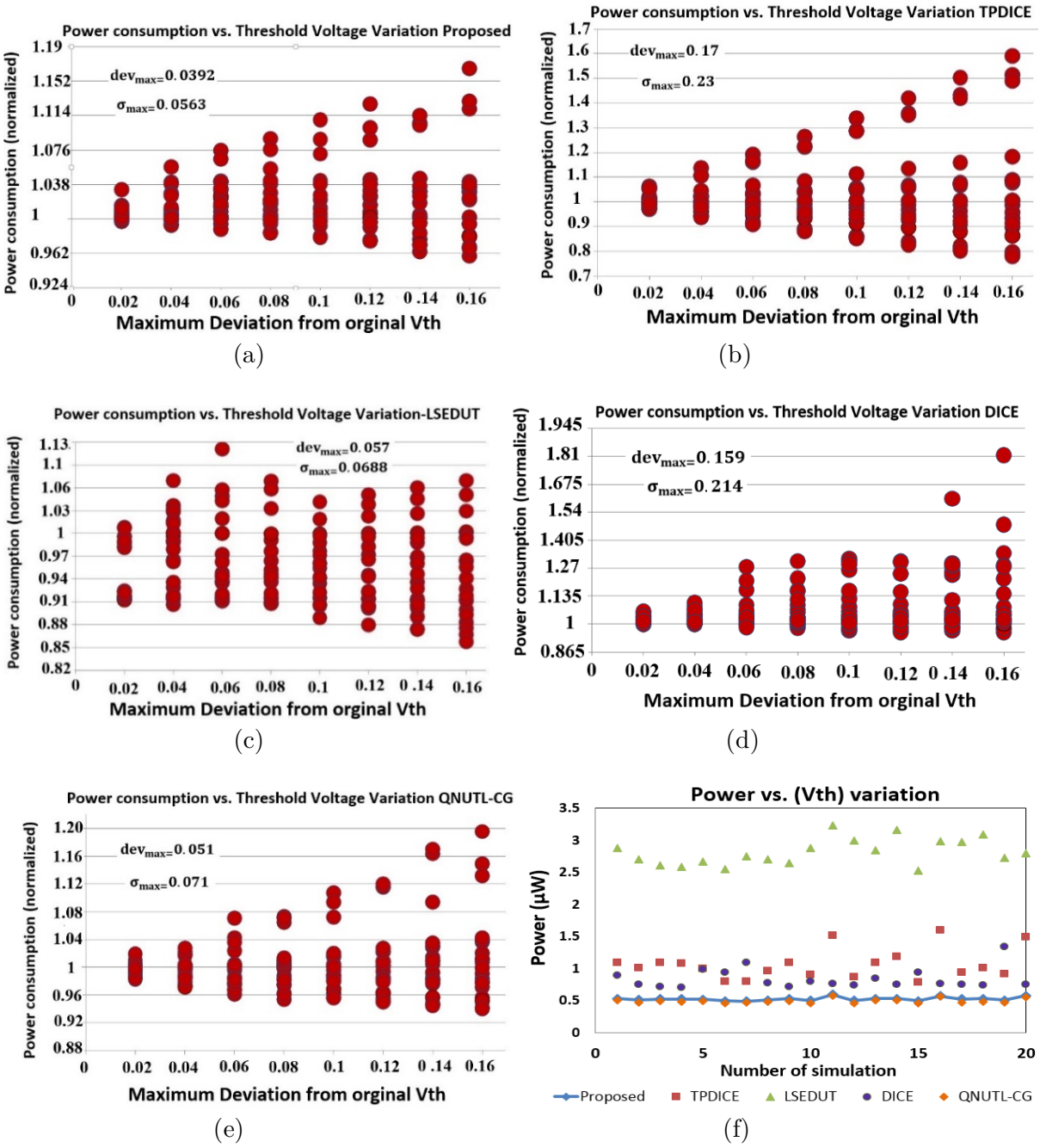


Figure 4.7. Threshold voltage variation effect on power consumption: (a) proposed D-latch (b) TPDICE-based D-latch (c) LSEDUT latch (d) DICE (e) QNUTL-CG latch (f) power consumption of D-latches with maximum deviation, 0.16, from original threshold voltage.

The other parameter seriously affected by process manufacturing variability is (W/L) transistor aspect ratio, which as in the case of the threshold voltage can be simulated by Monte Carlo methods with a Gaussian distribution. Results on the impact of this variability on the gate delay and power consumption are described next through Fig. 4.8 and 4.9.

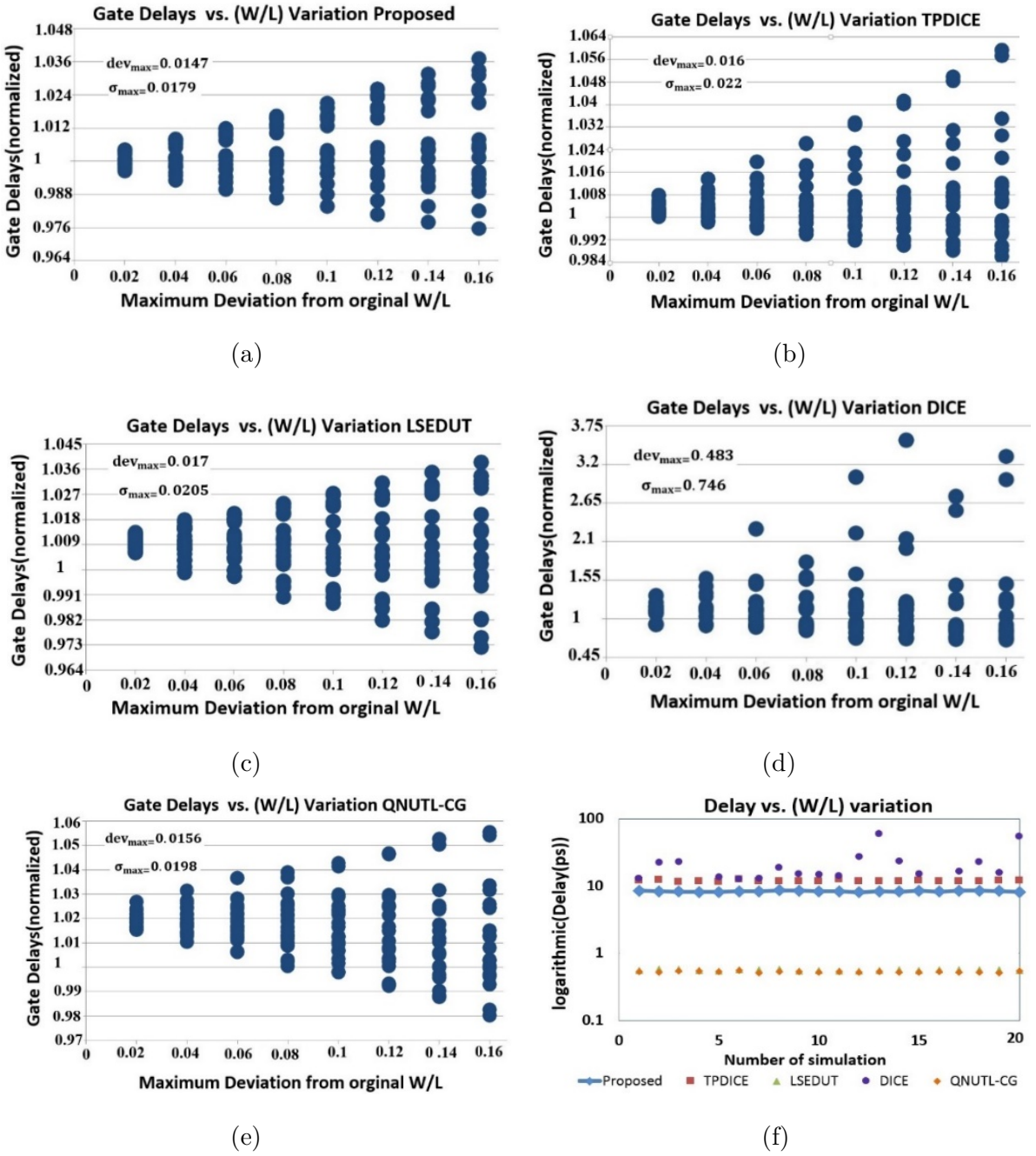


Figure 4.8. (W/L) variation effect on D-latch delay: (a) proposed D-latch; (b) TPDICE-based D-latch; (c) LSEDUT latch; (d) DICE; (e) QNUTL-CG latch; (f) delay of D-latches with maximum deviation, 0.16, from original W/L.

In Fig. 4.8, the gate delay variation of the proposed D-latch, TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch in regard to the maximum variability of the original W/L is shown. The lower gate delay variation of the proposed D-latch in comparison with those of TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch is worth mentioning. The maximum standard deviations of gate delay of the proposed D-latch, TPDICE-based D-latch, LSEDUT D-latch, DICE,

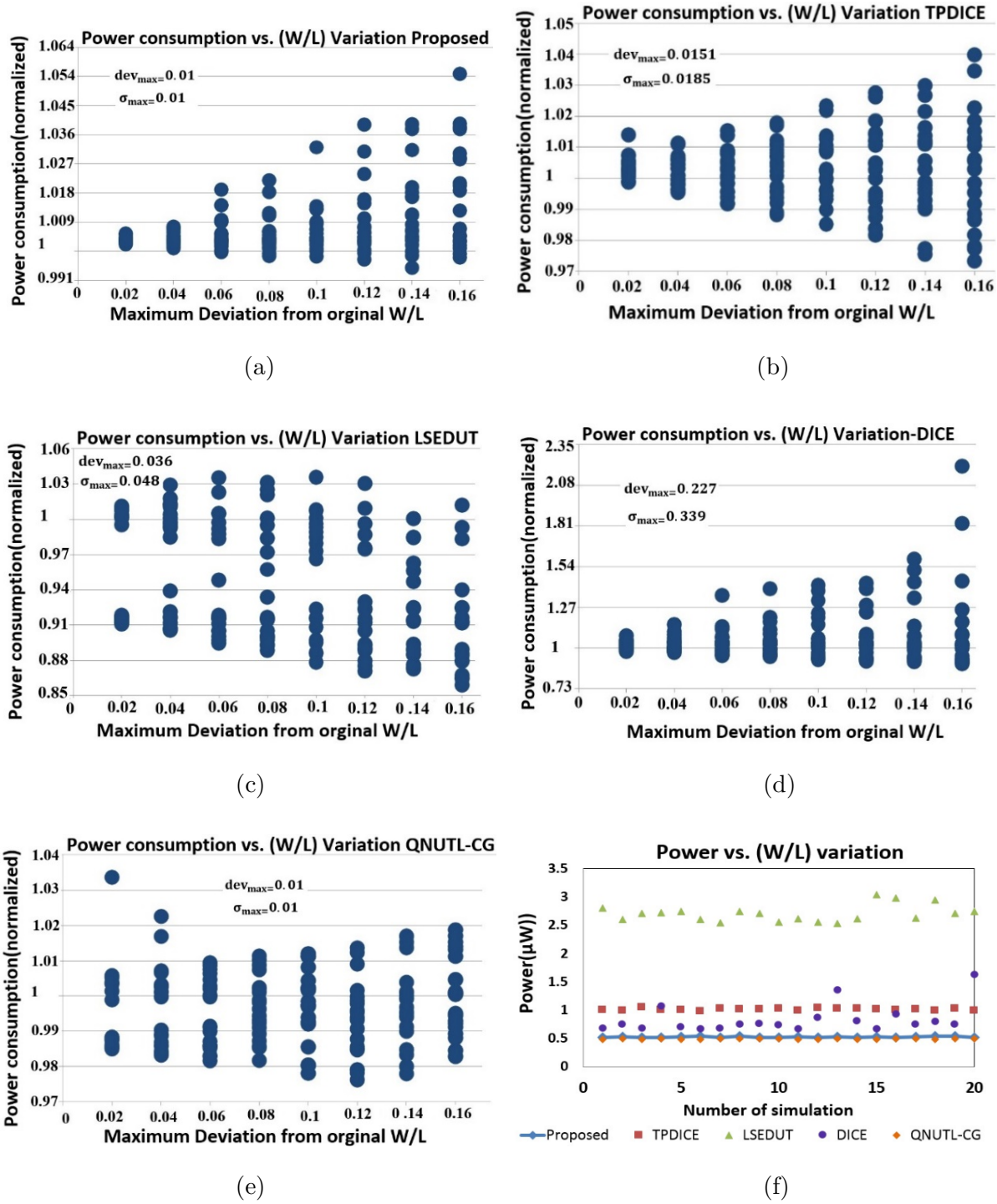


Figure 4-9. (W/L) variation effect on power consumption: (a) proposed D-latch; (b) TPDICE-based D-latch; (c) LSEDUT latch; (d) DICE; (e) QNUTL-CG latch; (f) power consumption of D-latches with maximum deviation, 0.16, from original W/L.

and QNUTL-CG D-latch are 0.0147, 0.016, 0.017, 0.483, and 0.0156, respectively.

Also, the maximum variance of gate delay of the proposed D-latch, TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 0.0179, 0.022, 0.0205,

0.746, and 0.0198, respectively. The maximum standard deviation improvements of the gate delay of the proposed D-latch compared with TPDICE- based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 8.1%, 13.5%, 96.9%, and 5.7%, respectively. The maximum variance improvements of gate delay of the proposed D-latch compared with the TPDICE- based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 18.6%, 12.6%, 97.6%, and 9.5%, respectively.

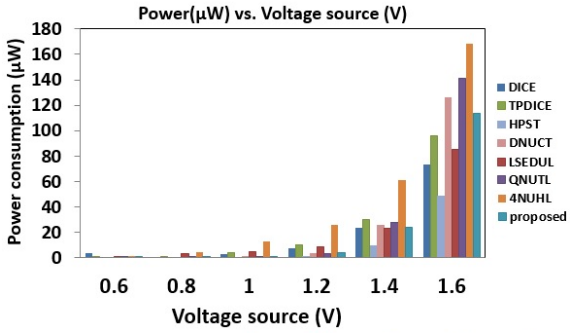
In Fig. 4.9, the power consumption variation as the result of (W/L) transistor variability of the proposed D-latch, TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch is shown. The maximum standard deviations of power consumption of the proposed D-latch, TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 0.01, 0.0151, 0.036, 0.227, and 0.01, respectively. The maximum variances of power consumption of the proposed D-latch, TPDICE-based D-latch, LSEDUT D-latch, DICE, and QNUTL-CG D-latch are 0.01, 0.0185, 0.048, 0.339, and 0.01, respectively. The result of this comparison shows that the variance and standard deviation of the power consumption are minimum for the proposed D-latch. The maximum standard deviation improvements of the power consumption of the proposed D- latch compared with TPDICE-based D-latch, LSEDUT D-latch, and DICE are 51%, 72%, 95.5%, respectively. The maximum variance improvements of the power consumption of the proposed D-latch compared with the TPDICE-based D-latch, LSEDUT D-latch, and DICE are 45.9%, 79%, and 97%, respectively. The maximum variance and standard deviation of proposed D-latch and QNUTL-CG D-latch present the same value.

4.4.4 PVT variations

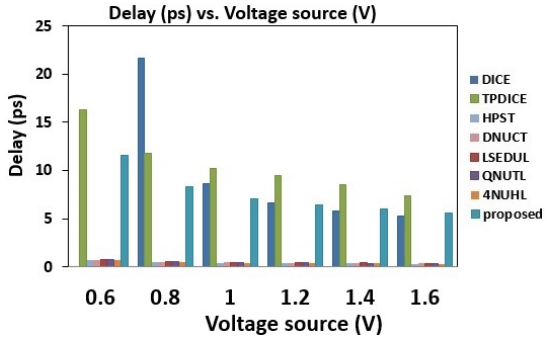
One additional parameter that should be considered to evaluate the performance of hardened D-latches is the impact of voltage and temperature (PVT) variations on the delay and power consumption. In this subsection the PVT variations impact of the proposed D-latch and previous D-latches are examined and benchmarked.

Figure 4.10 shows the impact of the variation of supply voltages (0.6 V-1.6 V) on the power consumption and delay (D-Q). In figure 4.10a, the power consumption rises by increasing the supply voltage. The reason is that by increasing the supply voltage, dynamic and static power increase (capacitors accumulate more charge and transistors drive more current [3]). Additionally, the delay of D-latches reduces due to the large current driven by the transistors, as shown in figure 4.10b.

In figure 4.11, the impact of temperature variation on the power consumption and delay (D-Q) is shown. The temperature variation has been evaluated in the industrial range from -40° C to 120° C. As the mobility of carrier reduces by rising temperature,

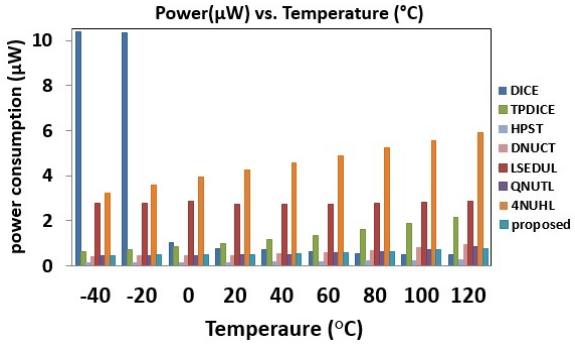


(a)

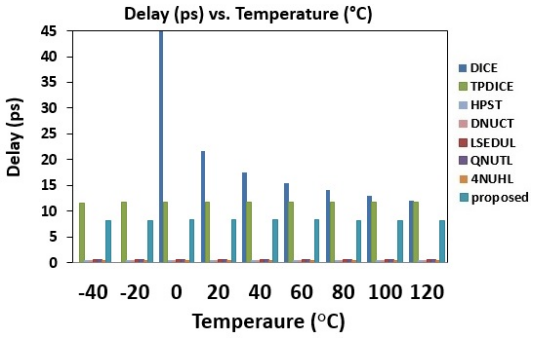


(b)

Figure 4.10. Impact of supply voltage variation on: (a) Power consumption; (b) delay.



(a)



(b)

Figure 4.11. Impacts of temperature variation on: (a) power consumption; (b) delay.

power consumption increases. But, the delay is not affected by the temperature expect for the case of DICE, since most of D-latches have one transmission gate from input to output in transparent mode. Two D-latches, TPDICE and proposed D-latch have more sub-circuits to filter SET, but their delays are not affected by temperature range. As can be seen in figure 4.11, the proposed D-latch is the less affected by the impact of temperature variation on power consumption and delay in comparison with other previous D-laches.

4.5 Conclusion

Scaling CMOS technology increases the demand for D-latch reliability to tackle harsh radiative environments. Under this premise, in this manuscript, a high reliability D-latch against temperature, process variation, and immunity against SNUs, DNUs, TNUs, and QNUs is presented. Moreover, the proposed D-latch has an additional feature with regard to the recently proposed QNUTL-CG D-latch (able to tolerate QNUs): it can mask SET in the input signal, without impacting on the power consumption (as compared with the QNUTL-CG D-latch). This lower power consumption with the extra SET masking feature and better process variation reliability is achieved by using clock-gating technology. Furthermore, compared with the QNUTL-CG D-latch, the improvements of the maximum standard deviation of the gate delay, which are the result of threshold voltage and (W/L) transistors variability of the proposed D-latch, are 13.8% and 5.7%, respectively and the improvement of the maximum standard deviation of power consumption, which is the result of threshold voltage variability of the proposed D-latch, is 23%. The improvements of the maximum variance of the gate delay, which are the result of threshold voltage and (W/L) transistors variability of the proposed D-latch are 11.3% and 9.5%, respectively and improvement of the maximum variance of power consumption, which is the result of threshold voltage variability of the proposed D-latch is 20.7%. Finally, the maximum standard deviation and variance of the power consumption induced by (W/L) transistor variability of the proposed D-latch are similar to QNUTL-CG D-latch. Furthermore, the additional benefits and high reliability do not come at a huge increase of the maximum value of area, power consumption, delay and PDP reached by the other hardened alternatives.

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Chapter 5

Rule-Based Design for Low-Cost Double-Node Upset Tolerant Self-Recoverable D-Latch

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Rule-Based Design for Low-Cost Double-Node Upset Tolerant Self-Recoverable D-Latch

Abstract: This paper presents a low-cost, self-recoverable, double-node upset tolerant latch aiming at nourishing the lack of these devices in the state of the art, especially featuring self-recoverability while maintaining a low-cost profile. Thus, this D-latch may be useful for high reliability and high-performance safety-critical applications as it can detect and recover faults happening during holding time in harsh radiation environments. The proposed D-latch design is based on a low-cost single event double-node upset tolerant latch and a rule-based double-node upset (DNU) tolerant latch which provides it with the self-recoverability against DNU, but paired with a low transistor count and high performance. Simulation waveforms support the achievements and demonstrate that this new D-latch is fully self-recoverable against double-node upset. In addition, the minimum improvement of the delay-power-area product of the proposed rule-based design for the low-cost DNU tolerant self-recoverable latch (RB-LDNUR) is 59%, compared with the latest DNU self-recoverable latch on the literature.

Index Terms: Delay-power-area product (DPAP), Double node upsets (DNU), High impedance state (HIS), Low cost single event double node upset tolerant (LSEDUT), Power-delay product (PDP), Single node upset (SNU), Soft error (SE).

5.1 Introduction

As CMOS technology is scaled down, the amount of charge needed to disturb the logic state of nodes of electronic circuits is dramatically reduced, primarily due to the low supply voltage and smaller capacitance of transistors. This fact is translated into an increasing vulnerability of the state of digital circuits to glitches formed by particle striking [1]. Therefore, increasing the reliability of integrated circuits for soft error (SE) tolerance or even SE self-recoverability has become a challenge of paramount importance [2].

The particle striking can affect the node state of memory cells, flip flops, and D-latches, which causes SEs. A SE occurring at one specific node is called single node upset (SNU). This phenomenon is responsible for the increasing investment in hardening D-latches against SNU [3-5]. Furthermore, the consequence of the nano scaling race, the probability of occurrence of a double node upset (DNU) increases. For example, it is more than twenty-five percent for technologies below the 45nm node [6], which redoubles the need to design D-latches that can handle DNU [7-10].

One of the approaches to increase the tolerance of D-latches against DNU is to use larger transistors for sensitive nodes, but even under this solution, some nodes can be upset by large charge injection [11]. Other approaches resort to layout technology making use of well isolation or extending the node space and guard ring to help tolerate DNU [7]. Thereby, the design of circuits becomes very complex. Many researchers are motivated to apply radiation hardening by design techniques (RHBD), in which C-elements, inverters, and Dual Interlocked storage Cell (DICE) [1], [12-15] are used. However, these D-latches cannot recover by themselves and present, at least, one pair of nodes unable to tolerate DNU [12], [13], [15], [16] or they are not optimized for power consumption or delay [10], [14].

This paper presents a novel and improved low-cost DNU-self-recoverable D-latch to meet the demand for reliable and low-cost circuits for harsh environments. This proposed D-latch is an improvement of the low-cost single-event double-node upset tolerant (LSEDUT) latch [12] based on the rule design for multiple nodes upset tolerant latch architecture [17], to confer it with self-recoverability. By using a different design approach, such as a clock-gating (CG) technique, this proposed D-latch has a lower transistor count, which results in lower power and area consumption. As there are separate paths for transparent mode and holding time, the delay also is minimum. SEU and DNU fault simulation results will show that this D-latch is not only immune against SEU and DNU, but the whole D-latch is self-recoverable against them.

The paper is structured as follows: section 5.3 focuses on reviewing previous self-

recoverable DNU and DNU tolerant D-latches. In section 5.3, the characteristics of the proposed D-latch are presented and the immunity against SNU and DNU is tested. In section 5.4, simulation methodology and comparative studies of robustness, power consumption, delay, area, and delay-power-area-product with previous hardened D-latches are discussed. Finally, the main conclusions derived from this work are summarized in Section 5.5.

5.2 State of the art: previous hardened latch designs

In this section, a review of self-recoverable DNU and DNU tolerant D-latches is presented. Previous hardened latch designs such as double-node charge sharing (DNCS) SEU tolerant latch [7], non-temporally hardened latch (NTHLTCH) [10], triple path dual-interlocked storage cell (TPDICE)-based latch [18], LSEDUT latch [12], DNU self-recoverable latch design for high performance and low power application (DNURHL) latch [19], and rule-based DNU tolerant latch (RDTL) [17] are analyzed.

5.2.1 DNCS-SEU tolerant latch

Figure 5.1a shows the structure of the DNCS SEU tolerant D-latch. This D-latch has some immunity constraints originating from the interlock between different nodes, such as N1 and N4. To illustrate this issue, as can be seen in figure 5.1a, N1 is the input of one C-element and N4 is the output of this C-element. Also, in the other C-element, N4 node becomes input and N1 is output, which stablishes one feedback path for these two nodes N1 and N4. Therefore, if the pair of nodes <N1, N4> has an upset, it will result in a high impedance in N5 and N2 nodes, and as the 3-input C-element has N1 upset, the output and inverter of output (Qb) will present high impedance. If at the output of the D-latch, a high impedance state (HIS) occurs, it yields that the D-latch does not have the ability to self-recover, and the upset at the latch can stay for the long term. This D-latch can experience upset by DNU in pairs such as <N2, N5>, <N3, N6>. Furthermore, this circuit is a pseudo-static D-latch and new data are written based on an overcoming process, which makes temporary competition between the driving output and the feedback inside, causing high leakage power consumption. Also, this D-latch presents a high delay from the input to the output node.

5.2.2 NTHLTCH

The structure of NTHLTCH D-latch is displayed in figure 5.1b. This D-latch is self-recoverable, but it is not cost effective in terms of silicon area and power consumption due to the use of nine C-elements and five inverters to ensure that it is immune against DNU and able to recover itself against DNU [19].

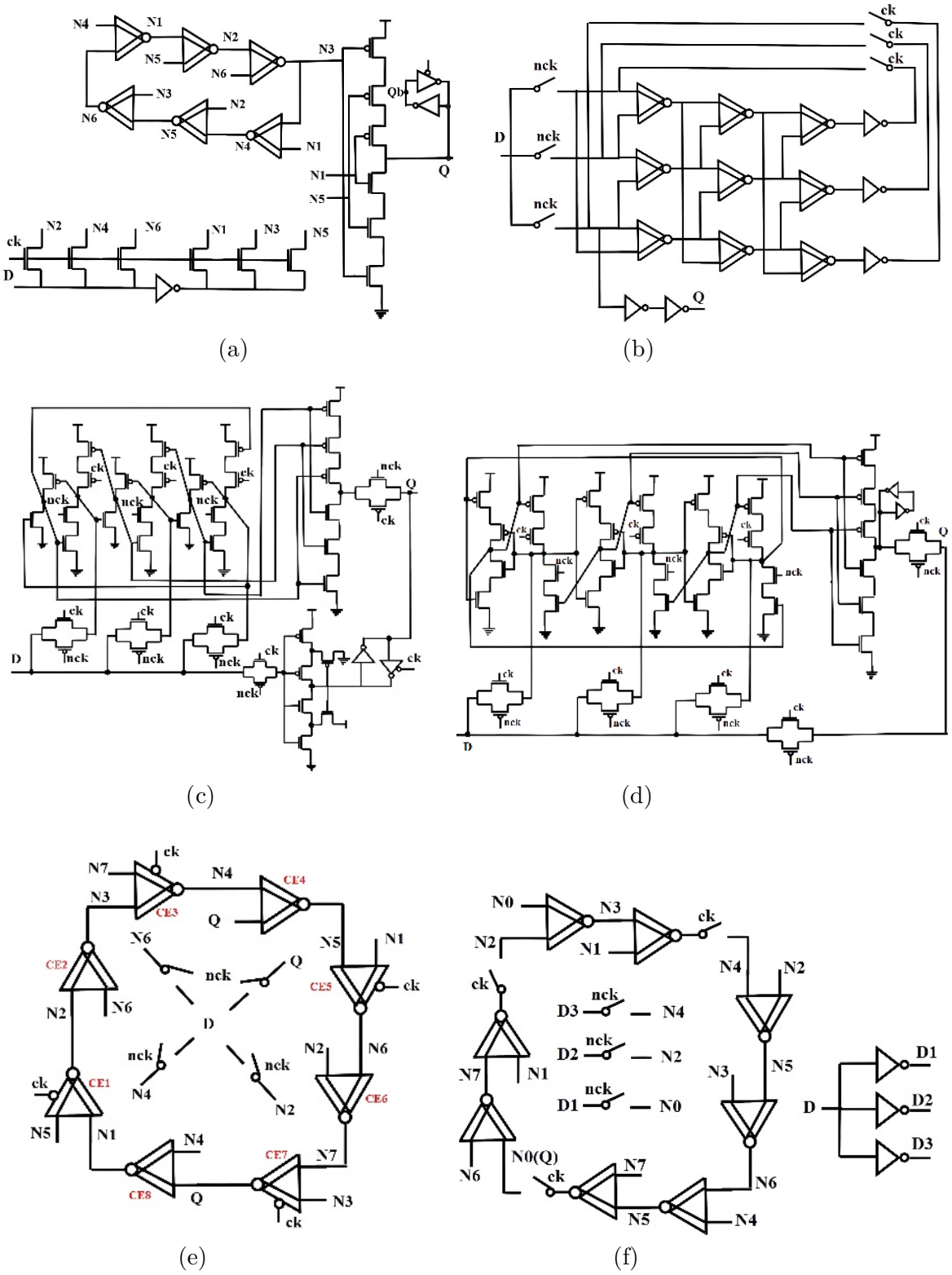


Figure 5.1. Previous hardened latch designs (a) DNCS-SEU tolerant latch; (b) NTHLTCH; (c) TPDICE-based latch; (d) LSEDUT latch; (e) DNURHL latch; (f) RDTL.

5.2.3 TPDICE-based D-latch

TPDICE-based D-latch is a hardened D-latch with immunity against single event transient (SET), SNU, DNU, and HIS insensitivity [18]. As figure 5.1c shows, this structure includes a TPDICE used for keeping the data in holding time, a three input C-element for filtering DNU, an embedded Schmitt trigger inverter for filtering the SET in the transparent path, and a keeper for avoiding HIS in the output node.

5.2.4 LSEDUT D-latch

Figure 5.1d shows the structure of the LSEDUT latch. This DNU tolerant D-latch is based on a TPDICE with full use of its interlocked node character to make it reliable for storing data. It has a keeper to avoid high impedance at the output node and two separate paths for holding time and transparent mode.

5.2.5 DNURHL D-latch

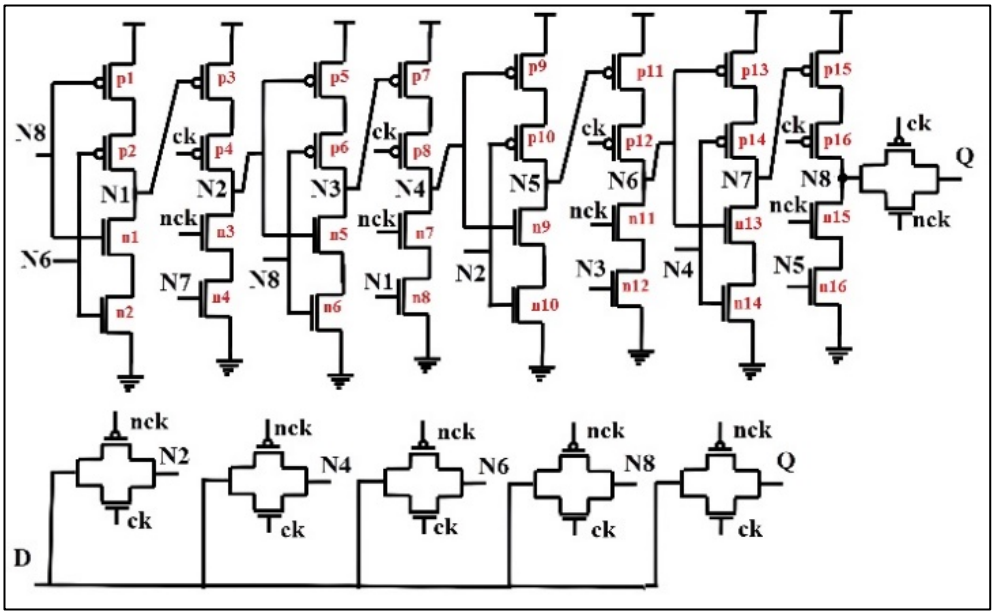
The DNURHL latch is DNU tolerant, however, due to the feedback architecture used, it is not fully recoverable. As figure 5.1e shows, it has pairs of input of C-elements, which makes improper feedback to the output of these C-elements: if there is any DNU at the input of these C-elements, their outputs will lose their data and it will result in an upset of the D-latch. These pair of input nodes of C-elements are, <N1, N5>, <N2, N6>, <N3, N7>, and <N4, Q>. This originated since node pair <N2, N6> is the input of two C-elements and if it is affected by charge injections, its upset can perturb the rest of the C-elements. A careful analysis shows that if N2 and N6 lose their value, N3 and N7 which are the output of C-elements (CE2) and CE6 will be affected, and their outputs lose their data. Therefore, two C-elements, CE3 and CE7, are affected and they lose their data. The <N1, N5>, <N3, N7>, and <N4, Q> pairs of nodes can experience the same upsets when a particle strikes two nodes of each of these pairs. The feedback of C-elements cannot recover their valid data because of the improper feedback mechanism. Consequently, the D-latch will be upset.

5.2.6 RDTL D-latch

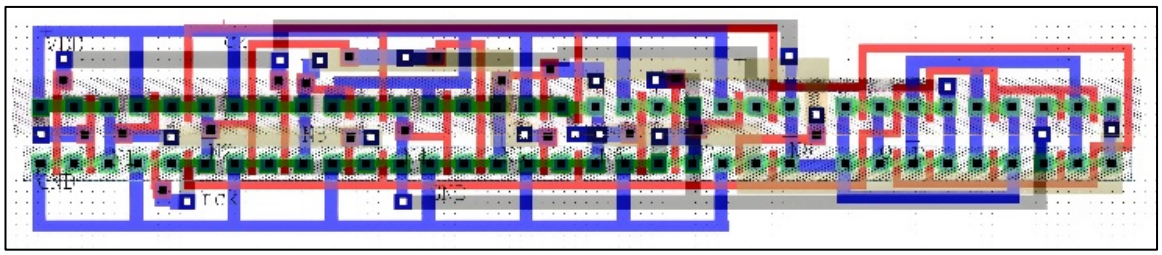
The DNURHL D-latch is not self-recoverable since the node pairs of C-element inputs are repeated, and these input pairs suffer from improper feedback to the output nodes of these C-elements. This problem is solved in RDTL (figure 5.1f), which is designed based on rule design so that the pairs of nodes of input C-elements are not repeated, presenting appropriate feedback in loops to become fully self-recoverable against DNU [17]. However, the RDTL, compared to the DNURHL latch, has more transmission gates and inverters, which introduces more area and power consumption penalty.

5.3 Proposed D-latch

The proposed D-latch is based on the LSEDUT and the RDTL latches, in which the number of transistors, power consumption, and area consumption are reduced. The structure of this latch consists of four 2-input C-elements, four input-split inverters, and six transmission gates. Also, each input of the proposed D-latch is connected to the four transistors, storing the input in more nodes to tolerate DNU and making this proposed D-latch self-recoverable against DNU. D, Q, ck, and nck are the input, output, clock, and inverted clock, respectively. Figure 5.2a shows the schematic of the proposed rule-based design for a low-cost DNU tolerant self-recoverable latch (referred to as RB-LDNUR) and figure 5.2b shows the layout of the proposed D-latch. When ck=1, the latch is in transparent mode and the input is connected to N2, N4, N6, N8, and Q. After the propagation of D input from 2-input C-elements, N1, N3, N5, and N7 are defined.



(a)



(b)

Figure 5.2. Proposed RB-LDNUR D-latch (a) schematic; (b) layout.

The output is driven by D, and N8 is not connected to the output directly targeting the reduction of the (D-Q) delay since N8 introduces more delay in the latch because it is connected to four gates of transistors (which introduces large capacitance in this node).

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When ck=0, the latch is in hold mode, N2, N4, N6, N8, and Q are disconnected from D, and Q is driven by N8. The interlocked feedback of the RB-LDNUR is active to retain robustly the data. These feedbacks are activated just during holding mode to save power.

When ck=0, the latch is in hold mode, N2, N4, N6, N8, and Q are disconnected from D, and Q is driven by N8. The interlocked feedback of the RB-LDNUR is active to retain robustly the data. These feedbacks are activated just during holding mode to save power.

The proposed D-latch structure is optimized in comparison with the DNURHL latch. Since the DNURHL latch consists of clock-gating 3-input C-elements, which are not applied in the proposed D-latch (the proposed design features 2-input C-elements), which optimizes area, power consumption, and transistor count. On the other hand, the RDTL latch has extra transmission gates and inverters in the feedback loop in comparison with the proposed D-latch, which reduces the transistor count of the new solution. In consequence, the power consumption and silicon area are also reduced. By applying the structure of the LSEDUT with the rule design of the RDTL, the proposed latch has larger interlocked feedback in holding time. By combining these two structures, the proposed D-latch is self-recoverable against DNU with fewer transistors. Also, in this structure, one transmission gate between Q and N8 is used for reducing the delay.

Following the rule design in [17], the proposed D-latch is immune against DNU, therefore, n=2, and d=2(n-1), where n is the number of nodes upset simultaneously in the D-latch, and d is the number of elements between Ni and Nj. To configure the proposed D-latch, assuming the Ni is the first node to one element, Nj is the second node, and i=(j-d-1) mod (4d). Therefore the pair of nodes entering different elements are as follows: <N1, N7>, <N2, N8>, <N3, N1>, <N4, N2>, <N5, N3>, <N6, N4>, <N7, N5>, <N8, N6>.

For evaluating the immunity against SNU, there are nine nodes and each of them can be affected by SNU. If N1 is affected by an SNU, a glitch will occur; in the case of

D=0, N2=0, and N1=N7=1 (p3 off and n8 ON), if the SNU occurs in N1, the value of N1=0 (p3 ON and n8 off), which makes N2 and N4 becomes unstable, but as N8 and N6 are not affected by SNU, N1 can be recovered by N8 and N6, then consequently, N2 and N4 can be stabilized by N1, which means N1 is self-recovered against SNU. This analysis can be applied to the whole of other nodes, which proves this latch is immune and self-recoverable against SNU.

For immunity against DNU, there are nine nodes in holding time making $C_2^9 = 36$ cases of node pairs. In the following, the different cases of DNU are evaluated based on the design of the hardened D-latch, but this DNU is independent of where the charge is injected into the D-latch. As the structure is symmetric, there are five cases to study: (1) <N1, N2>, <N2, N3>, <N3, N4>, <N4, N5>, <N5, N6>, <N6, N7>, <N7, N8>, <N8, N1>; (2) <N1, N3>, <N2, N4>, <N3, N5>, <N4, N6>, <N5, N7>, <N6, N8>, <N7, N1>, <N8, N2>; (3) <N1, N4>, <N2, N5>, <N3, N6>, <N4, N7>, <N5, N8>, <N6, N1>, <N7, N2>, <N8, N3>; (4) <N1, N5>, <N2, N6>, <N3, N7>, <N4, N8>; (5) <N1, Q>, <N2, Q>, <N3, Q>, <N4, Q>, <N5, Q>, <N6, Q>, <N7, Q>, <N8, Q>.

Case 1: <N1, N2> is affected by a DNU and perturbed by charge injection. As example D=N2=0 and N1=1; p3, n5, and n10 are off and n8, p5, and p10 are ON. If upset happens, N1=0 and N2=1, n8, p5, and p10 are off and p3, n5, and n10 are ON. But, N3 does not lose its value because N8 has valid data. As N8 and N6 have valid data, they can recover N1. Then, by recovering N1, p3 becomes off and N7 has valid data and can recover N2, which means <N1, N2> is immune and self-recoverable against DNU. Other pairs of this case can be analyzed similarly. As the result, the proposed RB-LDNUR D-latch is DNU-immune and self-recoverable in case 1.

Case 2: in this case, <N1, N3> is evaluated. Since N1 and N3 lose their value, there are weak instabilities in N2 and N4. But, as N6 and N8 have valid data, N1 can be recovered, and then N2 will be stable. The stability of N2 can help N3 to be recovered and N4 becomes stable. This explanation shows <N1, N3> is self-recoverable and immune against DNU. For other pair groups, the analysis against DNU is similar, thus they can be self-recover against DNU and this proposed D-latch is self-recoverable against DNU in case 2.

Case 3: in this case where <N1, N4> is affected by DNU, an upset happens. For example, D=N2=0, and N1=1; p3, n14, and n9 are off and n8, p9, and p14 are ON. If there are charges injected to N1 and N4, then N1=0 and N4=1, therefore, n8, p9, and p14 are off and p3, n14, and n9 are ON. N2 becomes weakly unstable. But, N5 does not lose its value. As N8 and N6 have a valid value, N1 can be recovered by N6, and N8 and N2 can be stable. Also, N4 can be recovered by N3 and N1. This explanation

demonstrates <N1, N4> is immune and self-recoverable against DNU. Other pairs of nodes can be analyzed similarly, thus they are also self-recoverable and DNU-immune. Therefore, this proposed RB-LDNUR D-latch can be self-recover from DNU in case 3.

Case 4: in this situation, <N1, N5> is affected by DNU. For this case, D=N2=0, and N1=N5=1, p11, and p3 are off; n8 and n16 are ON. If N1 and N5 are affected by DNU, N1=N5=0, p11 and p3 are ON; n8 and n16 are off. Then, N2 and N6 can be weakly unstable. But, N1 and N5 can be recovered by N8 and N4, respectively. Therefore, N2 and N6 become stable and the D-latch can become self-recoverable against DNU. Other pair groups recover themselves in the same way as <N1, N5>. Consequently, the proposed RB-LDNUR D-latch is self-recoverable in case 4.

Case 5: in this situation <N1, Q> is affected by DNU. As among nodes N1 to N8, just N1 is affected by DNU, this case is similar to SNU in nodes N1 to N8 because Q is not feedback to any other part of the RB-LDNUR latch. When N1 is affected by DNU, N2 and N4 become unstable, but N6 and N8 have valid data and N1 can be recovered by them. Then, N2 and N4 become stable. Also, Q can be recovered by N8. This analysis is valid for other pairs of nodes in this group. As the result, the proposed RB-LDNUR D-latch is immune and self-recoverable against DNU in case 5.

When D=1, the performance of the proposed RB-LDNUR D-latch is similar to the case when the input data is D=0. This structure is immune and self-recoverable against DNU. Therefore, the proposed RB-LDNUR D-latch is DNU-self-recoverable for all these key node pairs.

5.4 Simulation results

The proposed RB-LDNUR D-latch, DICE [20], DNCS SEU tolerant latch [7], DNUCT [21], NTHLTCH [10], TPDICE-based latch [17], LSEDUT latch [12], DNURHL [19], RDTL [17], RH-latch [22], FPADRL [23], LOCDNUTRL[24], HTNURE[25], LOCTNUTRL[24] are simulated at 0.8 V at room temperature using Synopsys® HSPICE in 22nm CMOS technology from PTM library [26]. For a fair comparison, PMOS transistors have an aspect ratio of W/L = 35 nm/22 nm, and NMOS transistors have an aspect ratio of W/L = 24 nm/22 nm.

In the error injection test, the proposed RB-LDNUR D-latch is evaluated against SNU and DNU by a current transient (current source) simulating the charge injection given by the following mathematical expression [27]:

$$I = \frac{Q_{total}}{T\sqrt{\pi}} \sqrt{\frac{t}{T}} e^{-t/T} \tag{5.1}$$

Where, T is the value of the time constant of the injected current charge, which is 0.1 ps and Q_{total} is the total charge injected being 20 fC in this test, which is large enough to prove immunity of the proposed RB-LDNUR D-latch against SNU/DNU [4].

The simulation results show that the operation of the proposed D-latch is similar to that of the traditional D-latch. Thus, in the transparent mode, the input is equal to the output, and in the holding mode, the output is equal to the input at the moment the clock becomes low level, as can be seen in figure 5.3.

For SNU simulation, to prove the self-recoverability of the proposed RB-LDNUR D-latch, one charge is injected into different nodes, such as internal nodes or Q. When the output and internal nodes do not lose their logical value after injections, which means they are self-recoverable against SNU.

As can be seen in figure 5.3, the key single nodes N1, N2, N8, and Q are injected by SNU, respectively. These key nodes are based on the different situations of SNU at the proposed RB-LDNUR latch, which analysis is mentioned above. The simulation results show that the output and other internal nodes do not lose their values after SNUs, which proves that the proposed RB-LDNUR D-latch is self-recoverable against SNU.

Based on different pairs of nodes in the DNU immunity of the proposed RB-LDNUR D-latch, the following tests are considered. Table 5.1 shows the key patterns of DNUs used for the charge injections in figure 5.4. As can be seen in this figure, different key pattern injections of DNU do not change the logical value of the internal nodes and output node, which means that the proposed RB-LDNUR D-latch is immune and self-recoverable against DNU. This table shows the precise time at which two charge injections are introduced at two different nodes. If after these injections the values of the nodes do not change, it means that they are self-recoverable against these DNUs.

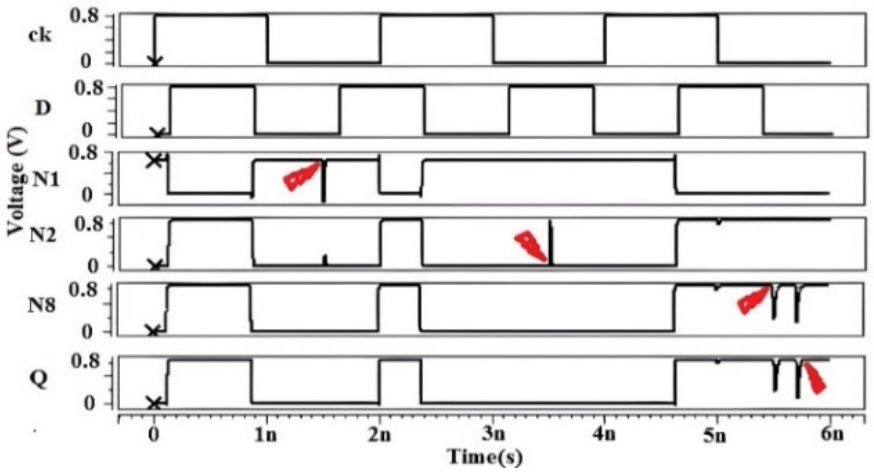


Figure 5.3. Simulation results of SNU injections to key single nodes of the proposed RB-LDNUR D-latch.

Table 5.1. Key pattern of DNU injections of the proposed RB-LDNUR latch in figure 5.4.

Time (ns)	SNUs/DNUs	State
1.2	N1, N2	Q =0
1.8	N1, N3	Q =0
3.2	N1, N4	Q =0
3.8	N1, N5	Q =0
5.8	N1, Q	Q =1

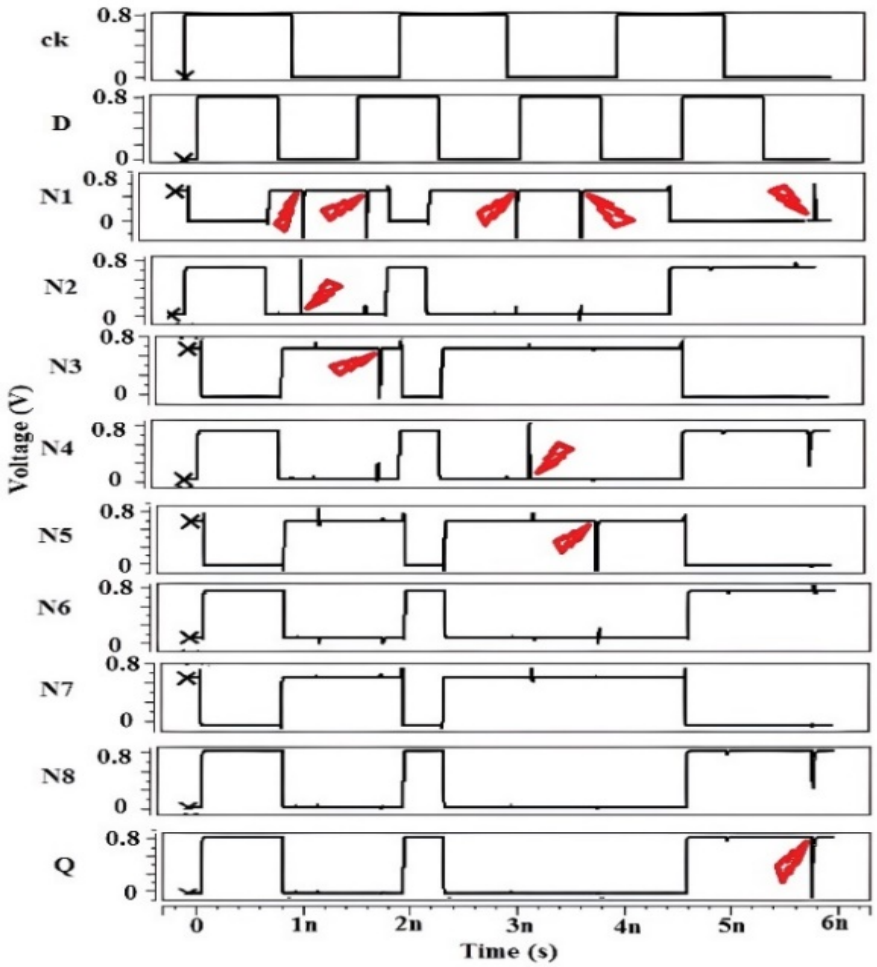


Figure 5.4. Simulation results of key patterns of DNU injections for the proposed RB-LDNUR latch.

Moreover, the output node has to maintain its value during these injections and as can be seen in figure 5.4, the Q value is stable during the whole of these DNUs.

Figure 5.5 shows the simulation waveforms for the proposed RB-LDNUR latch based on the pairs of nodes in table 5.2. These pairs of nodes are different internal nodes and the output node, Q. The results show that in all of the pairs of nodes, the proposed RB-LDNUR latch and all internal nodes can be self-recoverable from the DNU. Therefore, the output node is self-recoverable from every DNU at the proposed RB-LDNUR latch. For example at 1.2 ns in figure 5.5, the DNU injection occurs at N1 and Q nodes, when Q=0, as can be seen for this DNU test, the values of Q and N1 nodes are the same as before the injections.

In summary, the above explanation and simulation results demonstrate the reliability of the proposed RB-LDNUR latch against SNU/DNU injections and its self-recoverability.

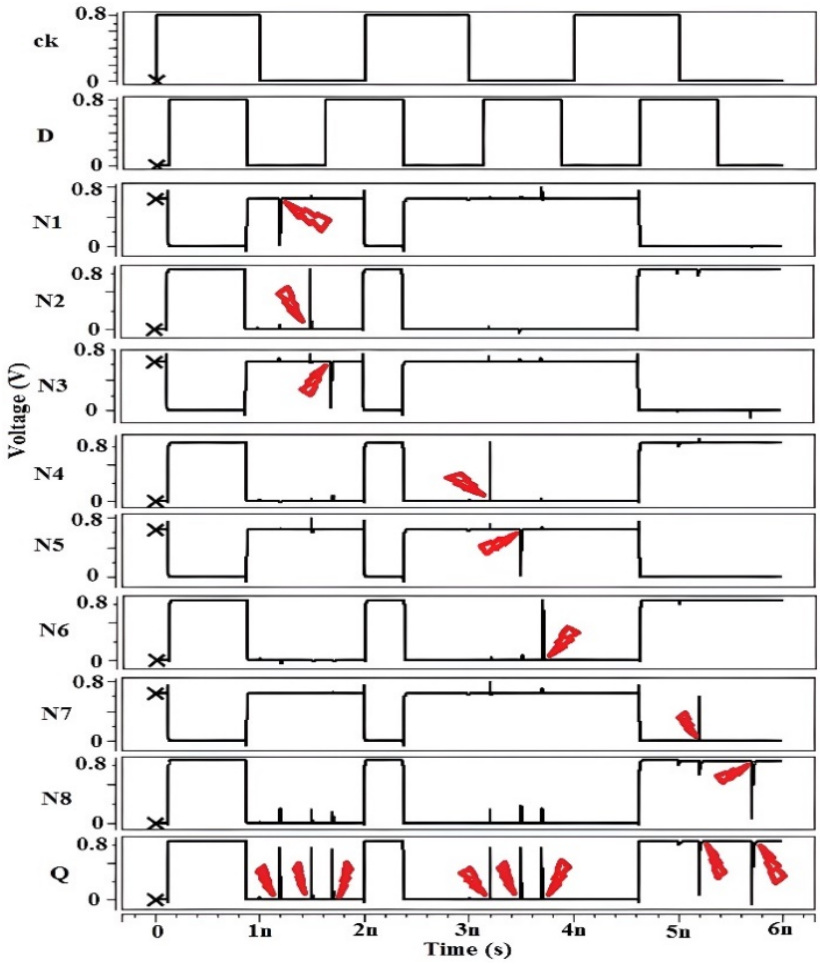


Figure 5.5. Simulation results of DNU injections to pairs related to the output node (Q) and other internal nodes of the proposed RB-LDNUR latch

Table 5.2. Pattern of DNU injections to pairs with output node (Q) and other nodes of the proposed RB-LDNUR latch.

Time (ns)	SNUs/DNUs	State
1.2	N1, Q	Q =0
1.5	N2, Q	Q =0
1.7	N3, Q	Q =0
3.2	N4, Q	Q =0
3.5	N5, Q	Q =0
3.7	N6, Q	Q =0
5.2	N7, Q	Q =1
5.7	N8, Q	Q =1

In table 5.3, there is a comparative summary of SNU, DNU immunity, HIS insensitivity, self-recoverability of the proposed RB-LDNUR latch and state-of-the-art SNU, DNU, and triple node upset (TNU) hardened D-latches, such as DICE, DNCS-SEU tolerant, DNUCT, NTHLTCH, TPDICE- based latch, LSEDUT, DNURHL, RDTL, RH-latch, FPADRL, LOCDNUTRL, HTNURE, LOCTNUTRL latches. DICE and DNCS-SEU tolerant latches are not fully immune against DNU. For self-recoverability, DICE can recover itself against SNU, but DNCS-SEU cannot recover itself against SNU. NTHLTCH is self-recoverable against DNU and it is fully immune against SNU and DNU, but it is not efficient in terms of cost. DNUCT, LSEDUT, and TPDICE-based latches and RH-latch are fully immune against SNU and DNU, but none of them are self-recoverable against DNU. The DNURHL latch is not fully immune against DNU because of improper feedback between pair nodes of 2-input C-elements and outputs of 2-input C-elements, causing the D-latch cannot recover its valid data when a pair nodes of 2-input C-elements are affected by DNU. The RDTL, FPADRL, and LOCDNUTRL latches are fully immune against SNU and DNU and can be self-recoverable, but it is not optimized for low-cost effectiveness. Also, HTNURE and LOCTNUTRL are TNU tolerant latches and self-recoverable against DNU, but still, they are not cost-efficient. Considering the proposed RB-LDNUR latch and applying the rule design of the RDTL latch and the structure of the LSEDUT latch, this new design is fully immune against SNU/DNU, can be self-recoverable, while maintaining a low-cost architecture. Moreover, as the proposed RB-LDNUR latch is HIS insensitive, it does not feature any driving ability during holding time.

Table 5.3. Immunity against SNU, DNU, HIS Insensitivity, and Self-Recoverability of the proposed RB-LDNUR and previous D-latches.

D-latch	FULL IMMUNE SNU	FULL IMMUNE DNU	SELF-RECOVERABILITY	HIS INSENSITIVE
DICE [20]	✓	×	✓	×
DNCS-SEU tolerant [7]	✓	×	×	✓
DNUCT [21]	✓	✓	×	✓
NTHLTCH D-latch [10]	✓	✓	✓	✓
TPDICE-based latch [18]	✓	✓	×	✓
LSEDUT latch [12]	✓	✓	×	✓
DNURHL latch [19]	✓	×	×	×
RDTL latch [17]	✓	✓	✓	✓
RH-latch [22]	✓	✓	×	✓
FPADRL [23]	✓	✓	✓	✓
LOCDNUTRL [24]	✓	✓	✓	✓
HTNURE[25]	✓	✓	✓	✓
LOCTNUTRL [24]	✓	✓	✓	✓
Proposed RB-LDNUR latch	✓	✓	✓	✓

Aiming at a quantitative comparison, the proposed RB-LDNUR latch and the mentioned hardened D-latches are simulated using the same PMOS and NMOS aspect ratios (transistors size), room temperature with 250 MHz input frequency at 0.8 V power supply in the 22nm CMOS technology. In the following simulation, a comparison of D-latch features related to area consumption, (D-Q) delay, average power consumption, PDP (power-delay product), transistors count, and DPAP (delay-power-area product) is presented. DPAP can be calculated by multiplying delay, power

consumption, and area. Area consumption can be calculated by silicon footprint extracted from the layout of the proposed RB-LDNUR latch and the mentioned hardened D-latches using L-EDIT Tanner software.

Table 5.4 presents the improvement percentage of proposed D-latch DPAP in comparison with all other mentioned D-latch alternatives, which is increased dramatically. The minimum percentage of improvement of DPAP of the proposed D-latch is 59% in comparison with DPAP of the best alternative (FPADRL D-latch) and the average improvement is 86.1%.

Table 5.4. Percentage improvement of DPAP proposed D-latch in comparison with other D-latches.

Features	Improvement
DICE	98.3%
DNCS-SEU tolerant	98.3%
DNUCT	76%
NTHLTCH D-latch	96%
TPDICE-based latch	99.1%
LSEDUT latch	94%
DNURHL latch	62%
RDTL latch	93%
RH-latch	64%
FPADRL	59%
LOCDNUTRL	97%
HTNURE	88%
LOCTNUTRL	95%

As shown in table 5.5, the lowest power consumption, area, delay, PDP, and DPAP are featured by the proposed RB-LDNUR D-latch in comparison with previous mentioned DNU/TNU tolerant D-latches. DICE and DNCS-SEU tolerant D-latches have the least number of transistors followed by the proposed D-latch, however, they are not fully immune against DNU and the DNCS-SEU latch is not self-recoverable

against SNU. Also, the area consumption in table 5.5, besides depending on the number of transistors, depends on the complexity of the layout of the D-latches. Because of that, even FPADRL has two transistors less than the proposed RB-LDNUR D-latch, but it does not feature lower area consumption in comparison to the proposed RB-LDNUR D-latch. Moreover, FPADRL in comparison with the proposed RB-LDNUR D-latch presents a higher power consumption because of its structure.

Table 5.5. Properties Comparative features of D-latches.

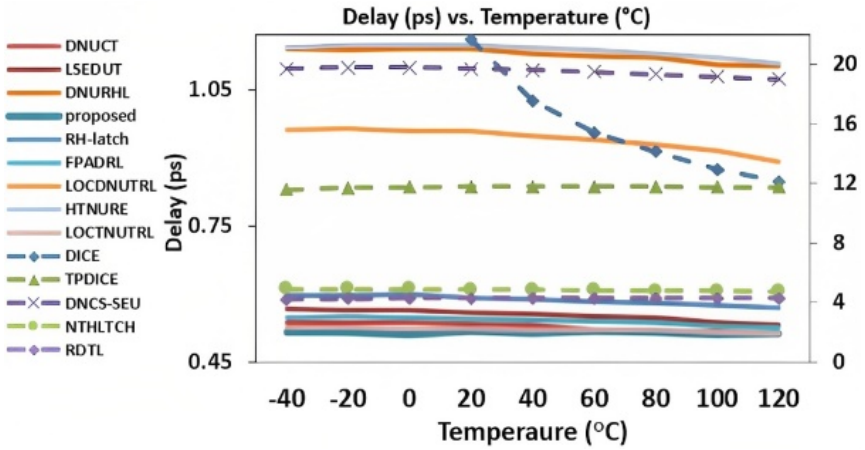
Features	POWER (μW)	DELAY (ps)	AREA (μm^2)	PDP ($10^{-18} \times W$)	TRANSISTOR COUNT	DPAP	Q_{crit} (fc)
DICE [20]*	0.74	18.20	0.90	13.40	18	12.10	1
DNCS-SEU tolerant [7]*	0.37	19.70	1.66	7.28	32	12.10	10
DNUCT [21]	0.53	0.56	3.10	0.28	70	0.87	5
NTHLTCH D-latch [10]	0.42	4.88	2.53	2.04	58	5.18	∞
TPDICE-based latch [18]	1.01	11.80	2.12	11.97	46	25.20	10
LSEDUT latch [12]	3.00	0.56	2.09	1.70	44	3.51	6
DNURHL latch [19]	0.26	1.14	1.85	0.30	48	0.55	8
RDTL latch [17]	0.35	4.28	1.99	1.48	50	2.98	∞
RH-latch [22]	0.53	0.56	1.99	0.29	36	0.58	5
FPADRL [23]	0.62	0.56	2.64	0.32	42	0.84	3
LOCDNUTRL [24]	3.16	0.95	2.24	3.01	44	6.74	2
HTNURE [25]	0.39	1.15	3.82	0.45	72	1.72	∞
LOCTNUTRL [24]	3.75	0.56	2.48	1.96	50	4.86	2
Proposed RB-LDNUR latch	0.24	0.56	1.57	0.14	44	0.21	∞

*Not DNU tolerant

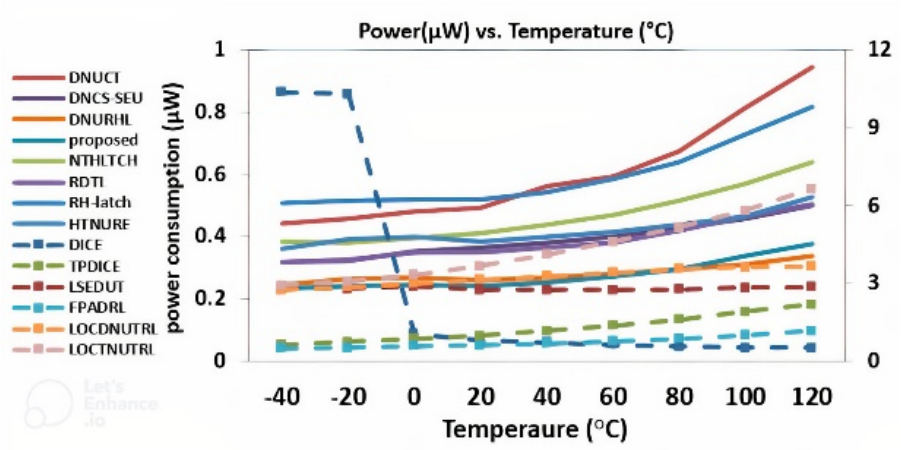
In the design of the proposed RB-LDNUR D-latch, the minimum (D-Q) delay is achieved by using a transmission gate between N8 and Q. Since the capacitor of N8 is large due to the four gates of transistors connected to this node. By separating the output node (Q) and N8, the delay is reduced considerably. By applying the LSEDUT latch structure, the number of transistors, power consumption, and area are reduced in comparison with DNURHL and RDTL structures containing 2-input C-elements and the clock gating 3-input C-elements. The minimum improvement of power consumption of the proposed latch is 7.7% in comparison with the best alternative (DNURHL latch); the minimum improvement of silicon area is 5.4% as compared with the best alternative (DNCS-SEU tolerant latch), except for DICE, and the minimum improvement of PDP is 50% in comparison with the best alternative (DNUCT latch). Based on the reliability of the hardened D-latch against charge injections, the minimum charge injections that can produce SNU in different nodes of latches are calculated [28]. Since the purpose of hardening the D-latch is increasing the value of Q_{crit} to tolerate SE, the minimum charge injections should be considered. This Q_{crit} is the minimum charge injection that can flip the value of the most sensitive D-latch nodes. As can be seen in table 5.5, the minimum charge injection that can change the value of proposed D-latch nodes is infinite, which means the proposed D-latch is full immune.

Process, voltage, and temperature (PVT) variation is considered for latches and flip-flops in nanotechnology [29-33]. Figure 5.6 and figure 5.7 show the temperature and voltage supply variation impact on the delay and power consumption of previous D-latches and the proposed D-latch. For a better comparison, both figure 5.6 and figure 5.7 include two different axes. The dashed lines with markers are adjusted by the secondary axes on the right side of the charts whereas the solid lines are adjusted by the axes on the left side of the charts.

In figure 5.6, for temperatures ranging between -40°C to 120°C, the power consumption and D-Q delay are monitored. In figure 5.6a, the delay is not affected by the temperature except for the case of DICE, since most of the mentioned D-latches have one transmission gate from input to output in transparent mode. The proposed D-latch features the minimum delay being its delay-temperature below the ones by its competitors. In figure 5.6b, by increasing the temperature, the carriers' mobility of the transistors decreases [34], which results in increased power consumption of D-latches, except for the DICE case. As can be seen in figure 5.6, the proposed D-latch is highly immune against the variation of temperature, approximately during the range of -40°C to 120°C, it maintains its minimum delay and power consumption.



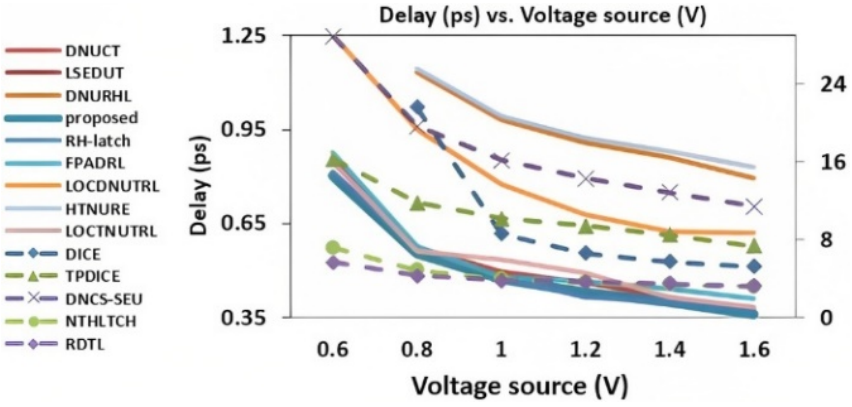
(a)



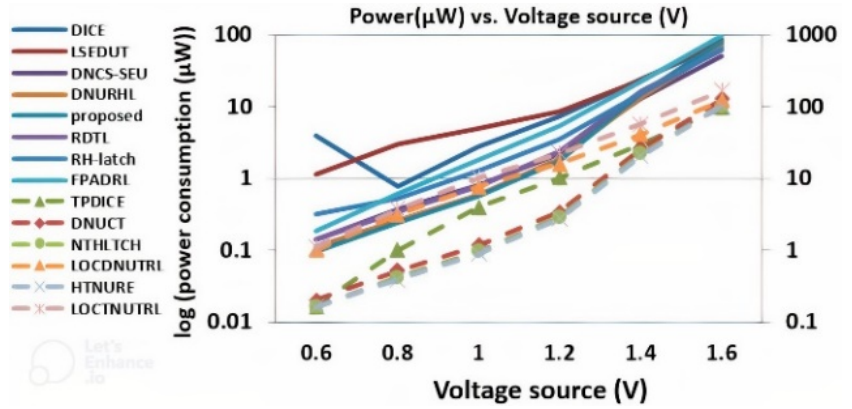
(b)

Figure 5.6. Impacts of temperature variation on: (a) delay; (b) power consumption.

Figure 5.7 shows the impact of the variation of supply voltages (0.6 V-1.6 V) on power consumption and delay (D-Q). In figure 5.7a, the delay of D-latches reduces due to the large current driven by the transistors, however, during the range of supply voltages (0.6 V-1.6 V), the proposed D-latch maintains its minimum value delay. Additionally, power consumption rises by increasing the supply voltage. The reason behind this must be sought in the fact that by increasing the supply voltage, dynamic and static power increase (capacitors accumulate more charge and transistors drive more current [34]), as shown in figure 5.7b in logarithmic scale. This figure shows that by increasing power consumption in the range of the supply voltages (0.6 V-1.6 V), the proposed D-latch maintains its minimum value of power consumption, which is translated into better performance in this range of supply voltage in comparison to its alternatives.



(a)



(b)

Figure 5.7. Impacts of supply voltage variation on: (a) delay; (b) power consumption.

5.5 Conclusion

Scaling CMOS technology boosts the demand for D-latch reliability. This paper proposes a low-cost, self-recoverable D-latch featuring immunity against SNUs and DNUs. Since most hardened DNU D-latches are not self-recoverable and low-cost, the proposed RB-LDNUR latch is conceived based on different rule designs and structures to achieve these purposes. Simulation results show that the proposed RB-LDNUR latch design is DNU self-recoverable and cost effective in comparison with other recently proposed DNU/TNU self-recoverable latch structures. The minimum improvement of power consumption is 7.7%, in comparison with the best alternative (DNURHL latch); the minimum improvement of silicon area is 5.4% when compared with the best alternative (DNCS-SEU tolerant latch, except for DICE which is not DNU tolerant),

the minimum improvement of PDP is 50% in comparison with the DNUCT latch. Finally, the minimum improvement of DPAP of the proposed D-latch in comparison with the FPADRL D-latch is 59% and compared with other mentioned D-latches, the average improvement is approximately 86.1%. Also, the temperature has little effect on the performance of the proposed D-latch and by changing the value of supply voltage, the proposed D-latch keeps its high performance compared with other mentioned previous D-latches.

DECLARATION OF COMPETING INTEREST

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Part III. Conclusions

Chapter 6

Conclusions and future work

6.1 Conclusions

This thesis has presented a comprehensive exploration of hardened D-latch designs for enhanced reliability and tolerance against various sources of perturbations in nano-scale IC technology. The outlined articles collectively contribute to advancing the field of fault tolerance in digital circuits, particularly focusing on single node upset (SNU) and quadruple node upset (QNU) scenarios.

Publication I established the foundation by addressing the challenges of low-cost hardening against single node upsets while maintaining high reliability under temperature and process variations. This article not only proposed innovative solutions but also critically evaluated and compared them with existing SNU-tolerant D-latch designs, showcasing the advancements made in this realm.

Publication II extended the scope to quadruple node upset (QNU) tolerance, introducing the High-Reliability Quadruple Node Upset (HRQNU) D-latch. The design emphasized its resilience against process variations and its ability to mask single event transients, thereby enhancing its robustness in real-world scenarios. The comprehensive analysis and comparison with prior QNU-tolerant D-latch designs highlighted its superior performance and potential for practical applications.

Publication III introduced a novel perspective by presenting a self-recoverable, double-node upset tolerant latch. This innovative approach, achieved through a combination of rule-based design and other techniques, opens avenues for multiple node upset (MNU) hardening, including the previously discussed QNU-tolerant D-latch. The proposed design showcases a balance between cost-effectiveness, reliability, and performance, contributing to the broader objective of fault tolerance in integrated circuits.

Collectively, the three publications underscore the significance of addressing various upset scenarios and process variations in modern digital circuitry. The innovative latch designs presented in this compendium highlight the ongoing efforts towards creating more resilient and reliable digital systems. As the field of nano-scale

IC technology continues to evolve, the insights and contributions of this thesis serve as a valuable resource for researchers and practitioners aiming to enhance the fault tolerance of digital circuits in the face of emerging challenges.

6.2 Future work

In the future work, building upon the foundation laid by the outlined thesis, there are several avenues for further exploration and enhancement in the realm of fault tolerance and robustness in nano-scale IC technology. Here are some potential directions for future research:

- Advanced Hardening Techniques: Investigate and develop more advanced hardening techniques that can provide even higher levels of tolerance against various sources of perturbations, including particle strikes, process variations, and temperature fluctuations. This could involve exploring novel circuit design strategies, utilizing emerging materials, or integrating intelligent error detection and correction mechanisms.
- Multi-Node Upset Hardening: Extend the research on multi-node upset (MNU) hardening, as introduced in Publication III. Further investigate and optimize the self-recoverable double-node upset tolerant latch design to accommodate a larger number of nodes. Develop techniques to effectively detect and recover from multiple simultaneous upsets, contributing to a comprehensive approach for MNU resilience.
- Integration with Other Circuit Blocks: Explore the integration of the proposed hardened latch designs into larger circuit blocks or systems, such as memory arrays, processors, or communication modules. Analyze the interactions and impacts of the hardened latches on overall system performance, power consumption, and reliability.
- Experimental Validation: Conduct extensive experimental validation and testing of the proposed latch designs using state-of-the-art nano-scale IC fabrication technologies. Evaluate their performance, reliability, and robustness through physical implementation and characterization in real-world environments. Compare the experimental results with simulation outcomes to validate the effectiveness of the designs.
- Dynamic Adaptation and Reconfiguration: Investigate adaptive and reconfigurable techniques that allow the latch designs to dynamically adjust their configurations based on changing environmental conditions or detected faults. Develop algorithms and control mechanisms that optimize the latch behavior in real-time, ensuring continuous operation in the presence of uncertainties.

- Application-Specific Design: Apply the hardened latch designs to specific application domains with stringent reliability requirements, such as aerospace, medical devices, or automotive systems. Tailor the designs to meet the unique challenges and constraints of these domains, considering factors like radiation exposure, temperature extremes, and real-time operation.
- Energy-Efficient Hardening: Explore techniques to achieve fault tolerance while minimizing power consumption. Investigate low-power design strategies that maintain the reliability of the latch designs without compromising energy efficiency, addressing the growing importance of power-aware computing.
- Security Considerations: Investigate potential security implications of the proposed latch designs. Analyze vulnerabilities and potential attack vectors that may arise due to the integration of hardening mechanisms. Develop countermeasures and techniques to enhance the security of the designs in addition to their fault tolerance capabilities.
- Collaborative Research: Collaborate with experts from other research disciplines, such as materials science, device physics, and system architecture, to leverage interdisciplinary knowledge and approaches in advancing fault tolerance and reliability in digital circuits.

By pursuing these avenues for future work, it will be possible to contribute to the ongoing advancement of fault tolerance in nano-scale IC technology, ultimately enhancing the resilience and robustness of digital circuits in the face of evolving challenges and emerging technologies.

Acronyms

4NUHL 4-Node-Upset completely Hardened Latch

AOSF Ability Of Set Filtering

CG Clock-Gating

CG-SIM CG Triple-level soft-error Interceptive Module

CLCT Circuit and Layout Combination Technique

CMOS Complementary Metal Oxide Semiconductor

DICE Dual Interlocked storage CEll

DNCS-SEU Double-Node Charge Sharing SEU

DNU Double Node Upset

DNUCT DNU Completely-Tolerant

DNURHL DNU self-Recoverable latch design for High performance and Low power application

DPAP Delay-Power-Area Product

ECC Error Correcting Codes

FERST Feedback redundant SEU/SET-tolerant latch

FPADRL Fully Polarity-Aware Double-node-upset-Resilient Latch

HIS High Impedance State

HPST High Performance SEU Tolerant

HTNURE Highly robust TNU self-REcoverable latch

LOCDNUTRL LOw-Cost DNU ToleRant Latch

LSEDUT Low-cost SEDU Tolerant

LSEH Low-cost and Soft Error Hardened

MEMU Multiple Event Multiple Upset

MNUs Multiple-Node Upsets

NTHLTCH Non-Temporally Hardened LaTCH

PDP Power-Delay Product

PVT Process, Voltage and Temperature

QNU Quadruple-Node Upsets

QNUTL-CG Clock Gating-based Quadruple-Node-Upset-Tolerant Latch

RB-LDNUR Rule-Based design for the Low-cost DNU tolerant self-Recoverable latch

RDTL Rule-based DNU Tolerant Latch

RH Radiation Hardened

RHBD Radiation Hardening By Design techniques

SE Soft Error

SEDU Single Event Double-Upset

SEMU Single Event Multiple Upsets

SEU Single Event Upset

SET Single Event Transient

SNU Single-Node Upset

STI embedded Schmitt Trigger Inverter

TMR Triple Modular Redundancy

TNU Triple Node Upset

TPDICE Triple Path DICE