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Research paper

Resonant hybrid flyback: A novel topology with wide voltage range for DC microgrid applications

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ABSTRACT

DC microgrids are becoming very popular due to the increasing deployment of distributed power generation systems. This presents new challenges for power converters, including how to achieve a wide range of input and output voltages in a small volume. State-of-the-art solutions include flyback-based and LLC-based converters. The first ones are bulky due to the large size of magnetic required to store the energy and their efficiency is limited by their capability to recycle the energy from parasitic elements. The second ones offer good efficiency but a limited range for input and output voltage, and may involve a large number of semiconductors. This paper studies the application of a novel topology, the asymmetrical half-bridge flyback, whose hybrid operation principle combines the advantages of forward and flyback converters while keeping a small number of switches. A design process to accomplish the outstanding requirements with the topology is presented. The theoretical analyses are supporter by a 240 W DC–DC prototype with an input range of 320 V–400 V and an output range of 5 V–24 V. A peak efficiency of 97.6 % is measured. The achieved power density of the converter is 65 W/inch^3 uncased. Finally, a comprehensive numerical comparison with the LLC and flyback converters in the state of the art is carried out to show the potential of the proposal.

1. Introduction

Microgrids are increasingly being deployed to make energy more affordable, reliable and sustainable, while reducing CO_2 emissions (Cui et al., 2023). In the state of the art, there are three types of microgrids depending on the voltages and currents used: AC and DC microgrids, and a mix of them, the so-called hybrid microgrids (Wang et al., 2020). DC microgrids present a number of advantages in comparison with the other approaches, e.g.: (1) A higher efficiency of the overall system thanks to the reduction of losses in different converters used for the DC loads, (2) better integration of DC storage systems as batteries or supercapacitors, DC supply sources as photovoltaic or fuel cells or DC loads such as LED lighting, (3) no need of frequency synchronization, unlike in the case of an AC bus and an AC generation system, like one based on wind energy (Cairoli and Dougal, 2013). Fig. 1 shows a general schematic of a DC microgrid.

However, despite these advantages, what will determine whether a DC microgrid is outperforming an AC microgrid is the number of DC loads, sources and storage systems which are working in the grid (Lotfi and Khodaei, 2017). Different values of voltages and currents that are used in these architectures are shown in Table 1. With the increase of DC loads (Lotfi and Khodaei, 2017), in addition to the DC nature of the storage systems and the incorporation of solar panels as DC source, DC microgrids are gaining more attention (Zhang et al., 2022). Table 1 shows the high range of voltages that are used in some examples on the devices of each block: sources, buses, loads and storage systems.

1.1. DC-DC converters

The key element enabling the wide use of DC microgrids is the DC–DC power converter, which is responsible for providing the required voltage and power values both from the sources or storage systems to DC bus and from the bus or storage systems to the loads (Sadaf et al., 2021). The development of DC microgrids entails the introduction of technologies such as fuel cells, storage systems, renewable energies or uninterruptible power supply systems, all of which imply new challenges to be overcome by power converters (Lakshmi and Hemamalini, 2018): (1) to be small enough to fit in domestic and not only in industrial environments (Schlenk et al., 2019), (2) to be able to work with large voltage ranges as can be seen in Table 1 and (3) to have a high operating efficiency in all conditions in order to achieve these objectives.

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Table 1
Examples of DC elements in a microgrid.

DC microgrid element	Voltage ratings	Current ratings	Power ratings
DC Sources			
Individual PV panels (Milenov et al., 2019)	20–100 V	–	75–300 W
DC Buses			
Data Center supplying (Arif and Hasan, 2018)	220 V, 380 V, 400 V	–	5 MW
Hybrid microgrid (Loh and Blaabjerg, 2011)	187.8–450 V	–	600–2100 W
Automotive application (Jones et al., 2019)	12 V, 48 V	–	2500–10000 W
PV, Battery and AC connection (Sun et al., 2011)	180–210 V	–	150–945 W
Onboard DC microgrid (Chen et al., 2023)	70–240 V	–	2000 W
DC Loads (Justo et al., 2013)			
Laptop computer	20 V	4.5 A	–
Cell phone	5 V	550 mA	–
Wireless phone	6.5 V	500 mA	–
Cable modems	12 V	750 mA	–
Variable speed drives (washers, dryer or air-condition)	380 V	–	465 W
DC Storage systems			
Supercapacitors (Fernando and Kularatna, 2015; Sanjeev et al., 2018)	12–48 V	–	–
Battery systems (Sasi and Jiji, 2020)	12–48 V	–	75–300 W

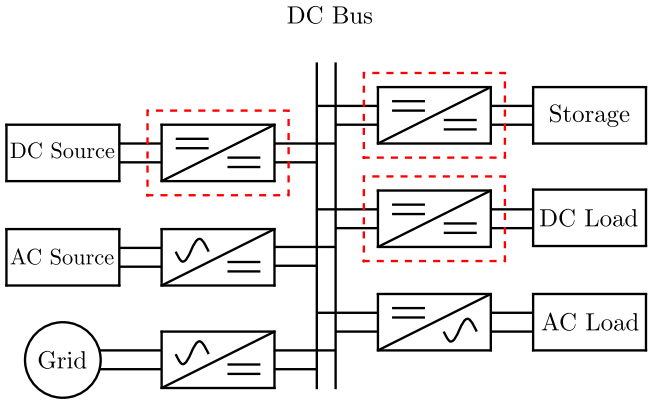


Fig. 1. General structure of a DC microgrid. The required DC–DC converters are highlighted.

Classic non-isolated converters, such as the Buck, Boost, Buck-Boost, Ćuk or Zeta, offer very competitive solutions suitable for these scenarios, as they are generally cheaper and simpler due to the need for fewer hardware components (Soedibyo et al., 2015; Dahale et al., 2017). Others offer higher performance by increasing the complexity (Marzang et al., 2022). However, these non-isolated converters have two disadvantages compared to isolated converters: they may not provide the required safety level and perform worse in terms of electromagnetic compatibility, which are the reasons behind the wide use of isolated converters (Alaql and Batarseh, 2019). Within this type of converter, the flyback is worth mentioning. This topology uses a coupled inductor as a storage element between the input and output, making it a bulky element. Furthermore, its efficiency is limited if the energy of the parasitic elements is not recycled, as is the case with the leakage inductance in the active clamp flyback (Huang et al., 2019; Alou et al., 2002). Beyond this topology, the LLC converter stands out (Cao et al., 2018). It presents a significant improvement in terms of efficiency, but to achieve large input and output voltage ranges, LLC-based topologies require extra power stages, making them more expensive and complex, sacrificing efficiency for the required dimensioning (Alaql and Batarseh, 2020; Alaql et al., 2020).

Due to the high growth in demand for DC–DC converters and the gap between requirements and state-of-the-art solutions, this paper contributes with a novel topology for these applications: the asymmetrical half-bridge flyback (AHBF). Thanks to its resonant behaviour, it combines advantages of flyback and forward conversion that prove to be beneficial in other topologies (Zhou et al., 2022). To this end, this work begins with a theoretical review of the latest knowledge of the topology, which exists thanks to its recent application in lower power applications as AC–DC wall adapters (Medina-Garcia et al., 2018). Secondly, a design method is described focused on having the most optimized dimensioning concerning volume and efficiency for DC microgrids. The manuscript proposes a more detailed loss analysis, together with a design scheme that aims to maximize the advantages of the topology in other working ranges, such as the hybrid flyback–forward power transfer and the soft switching behaviour (Huber and Jovanović, 2017; Garcia et al., 2018). Next, the outstanding performance of the topology is demonstrated with a prototype, showing its most suitable modulation scheme. Experimental results are then compared with those of converters based on flyback or LLC topologies to see the potential of the proposal. Finally, the most important conclusions of this work are drawn.

2. Proposed topology

A simplified schematic of the proposed topology, the asymmetrical half-bridge flyback (AHBF), is shown in Fig. 2. It consists of a transformer with its magnetizing inductance L_m which stores energy as in a standard flyback and a half-bridge (Q_1 and Q_2) that controls a resonant tank formed by L_r (which in practice is the leakage inductance of the transformer) and the capacitor C_r. The output is formed just by a single rectification diode, which can be replaced by a synchronous rectifier to obtain higher efficiency.

The presence of the transformer has a double advantage: on the one side, it provides the isolation that can be required for safety reasons. On the other side, it facilitates high voltage gain thanks to the turns ratio, which is very useful in these applications. The relation of the output and input voltage with the duty cycle, the turns ratio and the inductances is the one shown in Eq. (1) (Garcia et al., 2018). By choosing the right turns ratio, large voltage range can be achieved by fine control of the duty cycle (D).

$$V_o = D\frac{V_{in}}{N}\frac{L_m}{L_m + L_r} \tag{1}$$

The basic waveforms that describe the behaviour of the topology are shown in Fig. 3. They can be divided in the following phases:

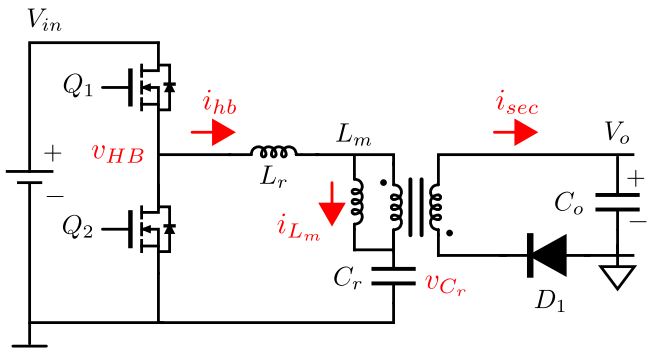


Fig. 2. Schematic of the asymmetrical half-bridge flyback. The main parameters for the topology modelling are highlighted.

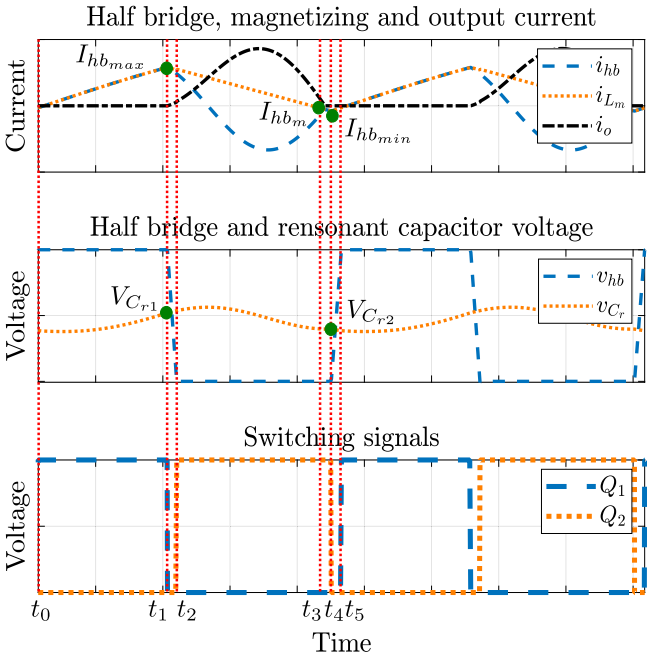


Fig. 3. Main waveforms of the asymmetrical HBF topology. Here the resonant behaviour of the topology can be seen. The graph points required in the theoretical modelling are highlighted, as well as the time periods into which the analysis is divided.

- **Operation phase 1** ($t_0 - t_1$). During this time, the energizing phase takes place. The switch Q_1 (the one in the high side) is switched on so the current flows across the resonant tank, charging both the transformer inductance and the capacitor C_r. It is done approximately in a linear way since the resonant frequency formed by L_m, L_r and C_r is lower than the working frequency. In the secondary side, the output rectifier is inversely biased, so there is no current through it, and therefore, there is no transmission of energy from input to output. At the end of this phase, the current in the resonant tank achieves its maximum value, $I_{hb_{max}}$.
- **Operation phase 2** ($t_1 - t_2$). In this short dead time, both switches are off. The transformer inductance which is still positive forces the current to flow through the body diode of the switch Q_2 since it is the only path it has. Thanks to this, the voltage in the half-bridge (v_{hb}) is ≈ 0 V before starting the following phase.
- **Operation phase 3** ($t_2 - t_4$). When the voltage v_{hb} is 0 V, the switch Q_2 in the low side of the half-bridge turns on with Zero Voltage Switching (ZVS) condition, reducing considerably the switching losses of the topology without the need of additional elements. Now, as the slope of the i_{L_m} current begins to decrease, the transformer voltage changes polarity. The diode in the secondary side starts conducting the current since it is forward biased, allowing the transfer of the energy. L_m is parallel to the output voltage, so its voltage value is fixed and there is a free resonance behaviour between L_r and C_r, with a frequency faster than the switching frequency. Therefore, as shown in Fig. 3, the output current has a sinusoidal waveform. At t_3, when the resonant current $i_{L_{hb}}$ reaches the value of the magnetizing current i_{L_m}, the output current reaches 0 A and can no longer flow through the rectifying diode, so no more power is sent to the output. The magnetizing current continues decreasing until it reaches a negative value $I_{hb_{min}}$.
- **Operation phase 4** ($t_4 - t_5$). In this last period, both switches are turned off, but current is forced to flow across the body diode of the Q_1 switch due to the inductance of the transformer. Thus, the voltage of the half-bridge will increase until it gets clamped to V_{in}. Due to this, when the cycle starts again with the operation phase 1, the voltage across the terminals of Q_1 is 0 V, allowing a ZVS in both transistors.

3. Design optimization

3.1. Losses model

The schematic of Fig. 2 is not realistic since it does not include the parasitic elements that cause losses. In Fig. 4 these elements are included. Switching components are modelled in terms of their resistance when current is flowing: R_{HS}, R_{LS} and R_{SR}. The same applies to the capacitors: the resistances $R_{C_{in}}$, R_{C_o} and R_{C_r} represent the parasitic equivalent series resistance (ESR) of the input, output and resonant capacitors. The transformer has two mechanisms of losses that are related between them. On the one side, the winding losses, produced by the electrical current flow. This is modelled by two parasitic resistances: R_p (on the primary side of the transformer) and R_s (on the secondary). R_p and R_s represent both the DC resistance of the copper wires, and the AC resistance that appears due to the skin and proximity effect caused by the frequency. On the other side, there are core losses produced by hysteresis during the process of magnetization and demagnetization and eddy currents across the ferromagnetic material. Finally, the last element of the losses model are the power losses related to the driving of the switching components due to the charging and discharging of their parasitic capacitors while they are turning on and off. The diode used in Fig. 2 is now replaced by a MOSFET to achieve synchronous rectification, which is the same approach used in the final prototype to improve the efficiency.

In short, there are 3 blocks of losses with different nature: conductive, magnetic and driving, distributed in 3 blocks of components: capacitors, switches and transformer. For the subsequent analysis, switching losses are considered to be zero due to soft switching (ZVS and ZCS). The losses in the leakage inductance are simplified by including them in the transformer losses, as they correspond to the same physical element in the prototype. This summary is shown in Table 2.

The driving losses and the conduction losses are applied to the three MOSFETs in the converter (Q_1, Q_2 and Q_{SR}). The losses in the transformer due to conduction are applied to both primary and secondary windings. Finally, conduction losses in the capacitors occur in the input capacitor, in the output capacitor and in the resonant capacitor.

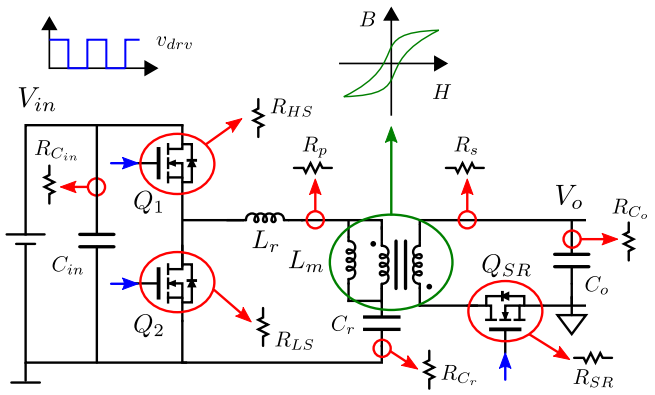


Fig. 4. Model of the asymmetrical half-bridge flyback with all the losses mechanisms.

Table 2
Summary of losses in the converter.

Power loss	Formula	Increases with:
Switching	$P_{sw} = 0$ (*ZVS* & *ZCS*)	–
Driving	$P_{drv} = V_{drv} \cdot f_{sw} \cdot Q_g/2$	$\uparrow f_{sw}$
Core	$P_c = P_v \cdot V_e$	$\uparrow f_{sw}$
Conduction MOSFETs	$P_{MOS} = R_{ds_{on}} \cdot I^2_{RMS_{MOS}}$	$\uparrow I_{RMS}$
Conduction Transformer	$P_t = R_{AC+DC} \cdot I^2_{RMS_t}$	$\uparrow R_{AC}$ $\uparrow I_{RMS}$
Conduction Capacitors	$P_{Cap} = ESR \cdot I^2_{RMS_{Cap}}$	$\uparrow I_{RMS}$

To calculate the conduction losses, it is necessary to know the RMS currents across each element in Fig. 4.

$$I_{RMS} = \sqrt{\frac{1}{T}\int_0^T i(t)^2\,dt} \tag{2}$$

Analysing the circuit in Fig. 2 in its different phases (Medina-Garcia et al., 2021a), the following temporal expressions are obtained:

$$i_{hb}(t) = \begin{cases} I_{hb_{max}} cos(\omega_1 t) + \dfrac{NV_o - V_{Cr2}}{Z_1} sin(\omega_1 t) & \text{if } t < t_1 \\ I_{hb_{min}} cos(\omega_2 t) + \dfrac{V_{Cr1}}{Z_2} sin(\omega_2 t) & \text{if } t_1 \le t < t_3 \\ I_{hb_m} - \dfrac{NV_o}{L_m} t & \text{if } t_3 \le t < t_4 \end{cases} \tag{3}$$

$$i_{L_m}(t) = \begin{cases} I_{hb_{max}} cos(\omega_1 t) + \dfrac{NV_o - V_{Cr2}}{Z_1} sin(\omega_1 t) & \text{if } t < t_1 \\ I_{hb_m} - \dfrac{NV_o}{L_m} t & \text{if } t_1 \le t < t_4 \end{cases} \tag{4}$$

$$i_{sec}(t) = \left(i_{L_m}(t) - i_{hb}(t)\right) N \tag{5}$$

Where:

$$\omega_1 = \frac{1}{\sqrt{(L_m + L_r)C_r}} \quad \& \quad Z_1 = \sqrt{\frac{L_m + L_r}{C_r}} \tag{6}$$

$$\omega_2 = \frac{1}{\sqrt{(L_r)C_r}} \quad \& \quad Z_2 = \sqrt{\frac{L_r}{C_r}} \tag{7}$$

This system of equations is transcendental, so the RMS can be obtained through numeric solutions. The qualitative waveforms of the currents are shown in Fig. 5.

Regarding the losses in the transformer, some approximations are made here to simplify the analysis. The core losses, which

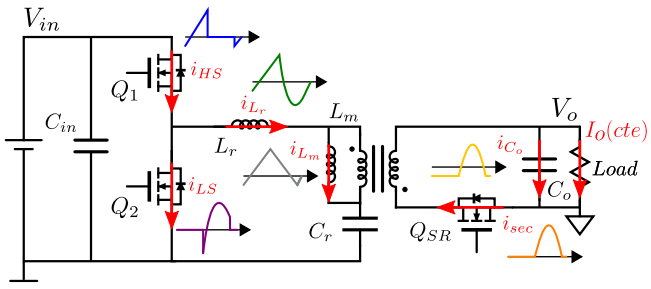


Fig. 5. Waveforms of the current across the elements of the converter.

Table 3
Target specifications.

Parameter	Value
Converter type	DC-DC
Input voltage ratings	320–400 V
Output voltage ratings	5–24 V
Max. output current	10 A
Max. output power @24 V	240 W
aa Max. switching frequency	250 kHz
Technology of switches	Si MOSFETs

are the product of the volumetric losses of the magnetic material and its total volume, are estimated with the manufacturer's tool for the material used: Ferroxcube Soft Ferrite Design Tool 2010. This makes it possible to estimate a precise volumetric loss with the non-sinusoidal shape of the magnetic flux, which is shown in Section 3.2. This gives a more accurate approximation than the Steinmetz equation (Yue et al., 2018). The winding resistances, and their dependence on the frequency, are calculated analytically in an approximate way using the Dowell solution (Szczerba et al., 2019), which gives a factor R_{ac}/R_{dc} depending on the skin and proximity effect, but neglecting the fringing effect on the air gap to avoid increasing excessively design time and complexity.

3.2. Parameter dimensioning

By using the losses model of the previous section, a prototype has been developed knowing how the selection of the parameters affects the final performance of the converter. The prototype is designed to meet the specifications in Table 3. In this case, the operation principle is similar to a buck converter, so it could be used to supply a load or a storage system from a DC bus or as a downstream DC–DC converter from an AC–DC converter connected to the conventional grid. The values are in accordance with those in Table 1.

The diagram in Fig. 6 shows the iterative flow of design to optimize the parameters of the converter in terms of volume and efficiency.

The first step is to select the turns ratio of the transformer. This determines the voltage stress of the switching devices and the resonant capacitor, delimiting the selection of them. Higher voltage devices mean more expensive and larger elements. In Fig. 7, the different values of voltage that the devices have to withstand is represented against different values of the turns ratio.

In addition, it is important to consider Eq. (1) since without the correct turns ratio it is impossible to achieve the desired voltage conversion by only changing the duty cycle.

Among those devices that can provide the required V_{DS}, the optimal one is selected considering its $R_{DS_{ON}}$, Q_G and C_{oss}. The ON resistance $R_{DS_{ON}}$ is going to determine the conduction losses. Besides this, the total gate charge Q_G determines driving losses. Finally, the ZVS condition depends on the output capacity C_{oss}.

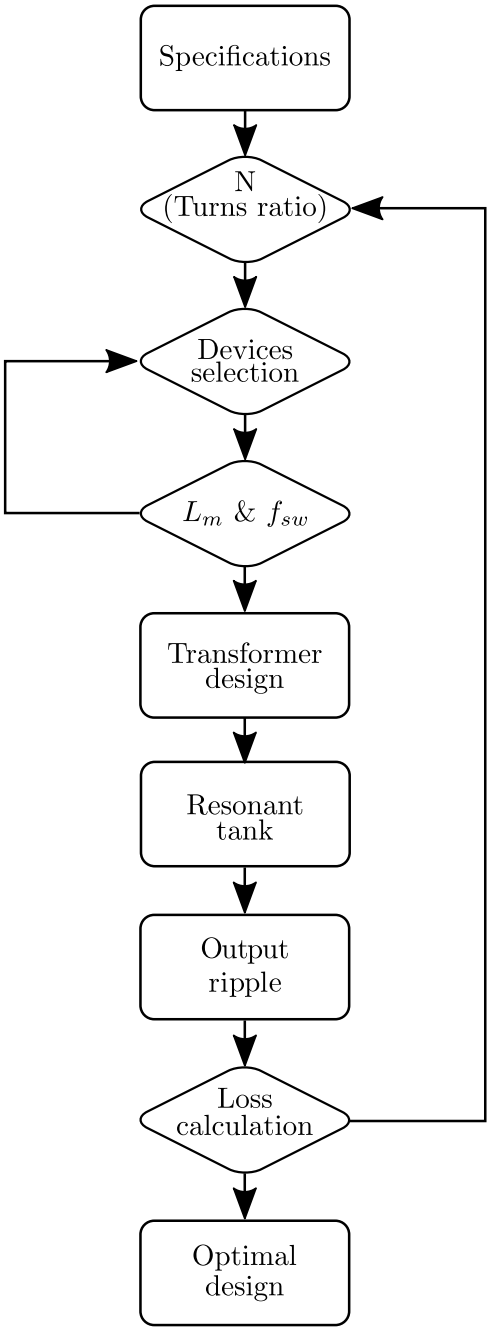


Fig. 6. Design flow diagram of the main elements of the converter.

Table 4
Semiconductor devices.

	IPD60R180C7	BSC037N08NS5
Device	Q_1, Q_2	SR (x2 in parallel)
$R_{DS_{ON}}$	180 mΩ	3.7 mΩ
Q_G	24 nC	46 nC
C_{oss}	18 pF	530 pF
$C_{o(er)}$	34 pF	581 pF
$C_{o(tr)}$	349 pF	932 pF
V_{ds}	650 V	80 V

For a turns ratio of $N = 8$, the chosen semiconductors with their characteristics are shown in Table 4.

In order to obtain a theoretical estimation of the needed working frequency, the circuit in Fig. 2 is analysed for the operation

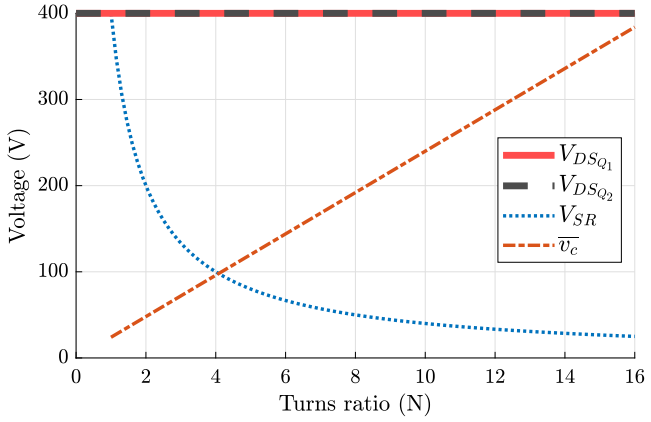


Fig. 7. Voltage stress of the half-bridge and SR MOSFETs and the resonant tank capacitor versus different values of the turns ratio in the worst case ($V_{in} = 400$ V).

phase 1, when the current across the magnetizing inductance is increasing from $I_{hb_{min}}$ to $I_{hb_{max}}$. Considering that the leakage inductance is smaller than the magnetizing inductance $L_m \gg L_r$, the voltage of the inductance is given by:

$$v_L = L_m \frac{\mathrm{d}i_{L_m}}{\mathrm{d}t_1} \tag{8}$$

In the desired operating state, the switching frequency must be much lower than the resonance frequency between the coil L_m and the capacitance C_r in order to approximate the current i_{L_m} to a straight line during the charging phase. Furthermore, it can be assumed that the capacitor voltage v_{C_r} is constant over time. With these two considerations, and expression (8), the value of the frequency can be obtained as follows:

$$f_{sw} = \frac{D\,(V_{in} - V_o N)}{I_{pp} L_m} \tag{9}$$

To determine the value of the peak to peak current required, the ZVS condition is used. The ZVS occurs when there is the sufficient amount of negative current to be able to discharge the energy stored in the parasitic capacitances of the switching elements (Kasper et al., 2016). This condition varies with the input voltage and is given by:

$$|I_{hb_{min}}| = V_{in}\sqrt{\frac{2C_{oss}}{L_m}} \tag{10}$$

Knowing the minimum value of current $I_{hb_{min}}$, the maximum value $I_{hb_{max}}$ can be obtained through the output current value (Medina-Garcia et al., 2018):

$$I_{hb_{max}} = \frac{2I_o}{N} - I_{hb_{min}} \tag{11}$$

Considering that $I_{pp} = I_{hb_{max}} - I_{hb_{min}}$, Eq. (9) can be solved using (10) and (11). In this way, it is possible to analyse how the needed switching frequency changes with the input voltage and the magnetizing inductance (Fig. 8). This allows the selection of a theoretical value of L_m suitable for the frequency range in which the converter is desired to operate, depending on the devices and controller used.

The other main element of the converter, together with the switching devices, is the transformer. The selected core is chosen to fit in size with the rest of the components, specially the output capacitors required to have the desired voltage ripple, since they are the largest components and the total volume is going to be dependent on them. For an appropriate design of the transformer,

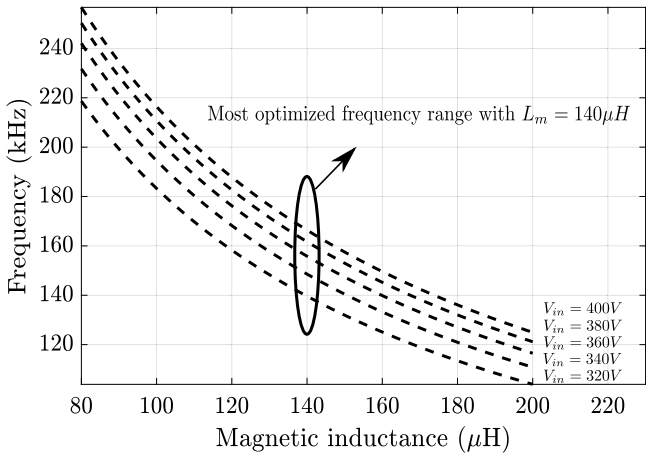


Fig. 8. Switching frequency versus variations of input voltage and magnetizing inductance for the highest output voltage ($V_o = 24$ V).

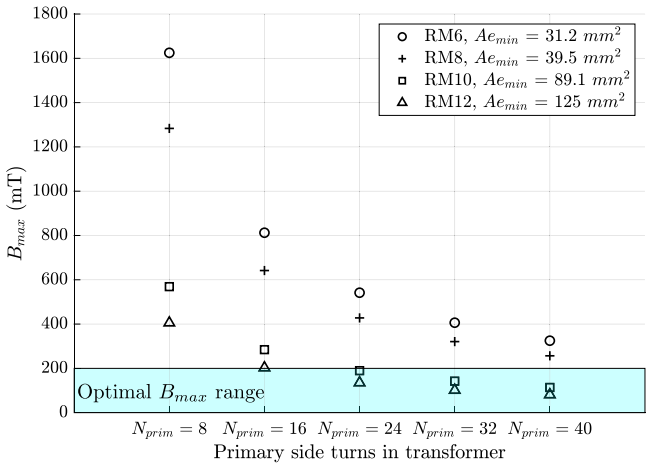


Fig. 9. B_{max} for different transformer's constructions. The shadowed zone represents the optimal range of B_{max}, avoiding too high values in the worst case ($V_{in} = 400$ V, $I_o = 10$ A).

a key variable is the maximum flux density B_{max}, since it is related with the possible saturation of the core and also with its losses. Using the formula (8) and the Faraday's law which correlates the magnetic field with the voltage applied in the primary side of the transformer, the B_{max} across the effective area of the core A_e can be obtained as follows:

$$B(t) = \frac{L_m}{N_{prim}A_e} i_{L_m}(t) \xrightarrow{max} B_{max} = \frac{L_m I_{hb_{max}}}{N_{prim}A_e} \tag{12}$$

There are two elements that define the core: the wires and the magnetic core. Their selection is intimately linked since there is a trade-off between conductive and magnetic losses. Choosing a bigger core allows having more room in the transformer's window for more copper, so less conduction losses occur and also decreases the value of B_{max} (Eq. (12)), reducing magnetic losses and avoiding core saturation. In the contrary, a bigger core volume is directly proportional to magnetic losses (Table 2), and takes more space in the converter, increasing its total volume. For this reason, the smallest core that allows a sufficiently small B_{max} but with the necessary space for copper has to be selected. In Fig. 9, some different values of B_{max} with different transformer constructions are compared. The turns of the primary side are determined by the turns ratio, as it has to be a multiple of it (in this case, 8) to have an exact value of turns in the secondary. Several shape cores are included in the graph of the RM Series Ferrite Cores.

Besides the shape, the core material is also a key parameter. The most suitable magnetic materials, according to expected temperature range and working frequency, are the 3C95 from Ferroxcube and the N95 from TDK. Table 5 presents the summary of the transformer specifications for the final design. This custom transformer is first handcrafted in the laboratory, and after initial tests an industrial prototype is obtained from Sumida Corporation.

The next step is to determine the resonant capacitor. When the time lapse to transfer the energy from primary to secondary (in the operation phase 3 from Fig. 3, T_{Q_2}) is minimum, the resonance time of the output current, caused between the elements L_r and C_r, must be short enough to complete approximately half a sine in order to achieve a Zero Current Switching (ZCS) behaviour in the secondary. This is very important in a step-down application, because the high currents flow through the secondary side of the topology.

The value of L_r, which is the leakage inductance of the transformer, can be estimated based on the transformer design, or measured if the transformer is available. The resonant tank capacity will be given by:

$$C_r < \left(\frac{T_{Q_2}}{\pi}\right)^2 \cdot \frac{1}{L_r} \tag{13}$$

The value of T_{Q_2} is calculated using the Eqs. (1) and (9) as follows:

$$D = \frac{T_{Q_1}}{T_{Q_1} + T_{Q_2}} \xrightarrow{(1)\ (9)} T_{Q_2} = \frac{I_{pp}L_m}{NV_o} \tag{14}$$

The worst case of study, shown in Fig. 10(a), is done considering the different values of output voltage, since it is independent of the input voltage. The value of the resonant capacitor must allow the discharge time to be met for all conditions, thus always reaching the ZCS. It may be lost if the resonant tank is not carefully dimensioned, this is shown in Fig. 10(b).

After dimensioning the converter, its currents are known, so the output ripple can be obtained. Fig. 11 shows the current across the output capacitor together with the output ripple.

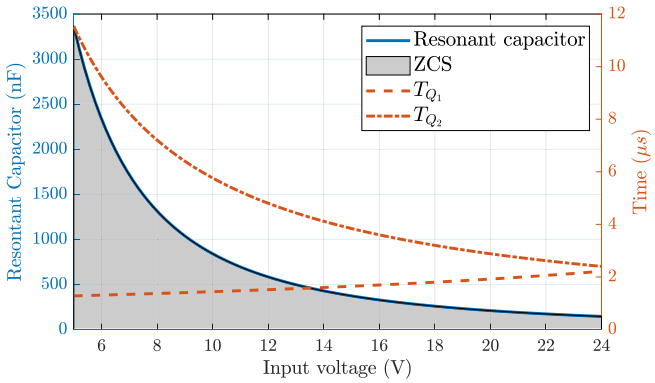
Output ripple depends on two parameters of the capacitor, its capacitance (C_o) and its equivalent series resistance (ESR), so both have to be considered for dimensioning. The resistive behaviour is particularly noticeable as shown in Fig. 11. The expression of the output ripple voltage can be approximated as:

$$\Delta V_o \approx \Delta V_o(C_o) + \Delta V_o(ESR) \approx \frac{I_o D}{f_{sw} C_o} + \Delta i_{C_o} ESR \tag{15}$$

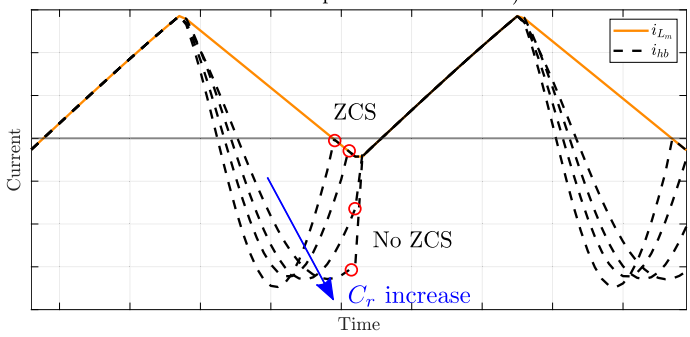
To keep the ripple small, the capacitance must be maximized and the ESR reduced. For this purpose, capacitors can be used in parallel, as shown in the final component list in Table 6.

Table 5
Transformer specifications.

Element	Value
Magnetic core type	RM10
Core material	3C95 (Ferroxcube)
Turns ratio	8
Np	24 turns (Litz 50 × 0.1 mm)
Ns	2 × 3 turns (TIW Litz 120 × 0.1 mm)
Interleaved structure	P-S-P
Primary inductance	140 µH @ 100 kHz
Leakage inductance	5.7 µH @ 100 kHz
Sumida part number	PS20-190



(a) C_r values for different V_o. The gray zone represents the values where ZCS is achieved. The selected value has to be suitable for the whole range, so the worst case is taken into account (maximum V_o, corresponding to the smallest value of T_{Q_2}, and so the shortest time available to complete the resonance).



(b) Effect of the resonant capacitor in the ZCS condition.

Fig. 10. Selection of the resonant capacitor.

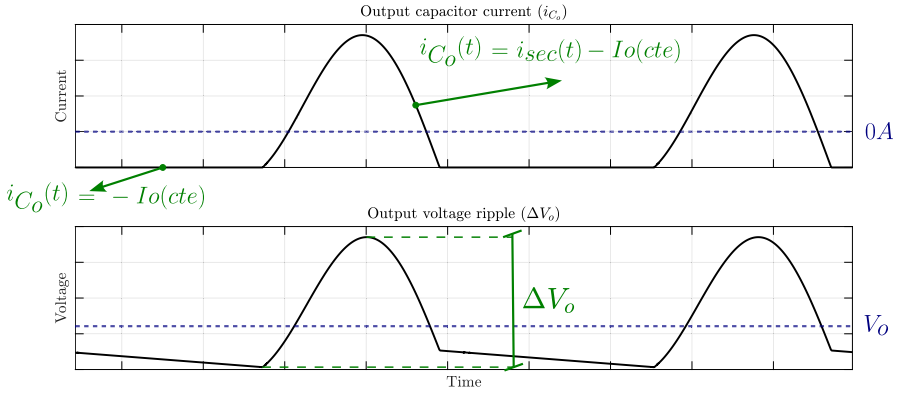


Fig. 11. Waveforms of the current and voltage at the terminals of the output capacitor.

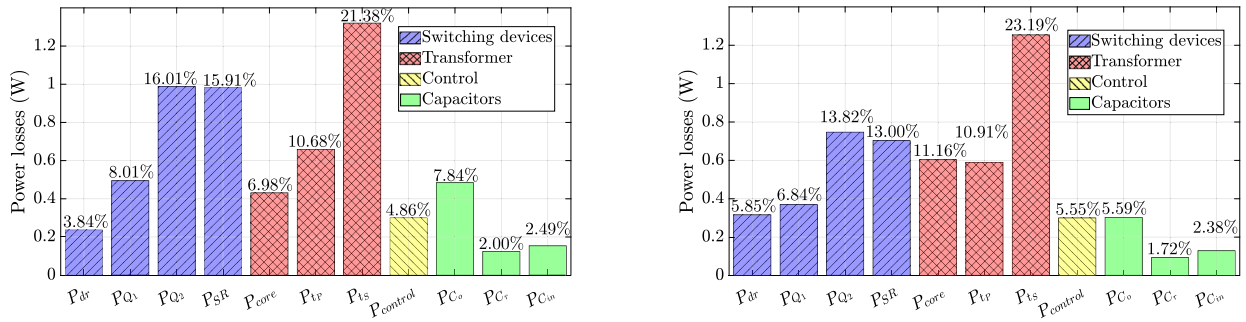
Finally, applying the losses model discussed before with the selected parameters, an estimate of the theoretical losses is obtained. This model can be recalculated by iteratively rescaling the parameters until the best desired estimation in terms of volume and efficiency is obtained. Table 6 shows the final values and chosen devices, together with the transformer in Table 5. Fig. 12 illustrates the loss estimation for these final parameters at maximum output power for $V_{in} = 320$ V (Fig. 12(a)) and $V_{in} = 400$ V (Fig. 12(b)). The losses are uniformly distributed across all elements over the entire voltage range.

Table 6
Parameters and components of the most optimized final design.

Parameter	Value
N	8
T_{Q_2}	2.5 µs
B_{max}	190 mT
C_r	110 nF
f_{sw} range	160–208 kHz
$I_{pp_{max}}$	3.29 A
ΔV_o @10 A	76 mV
Component	**Device**
HB MOSFETs	2xIPD60R180C7
SR MOSFETs	2x BSC037N08NS5
Input capacitance	1x (450 V/120 µF/150 mΩ)
Output capacitance	6x (35 V/470 µF/11 mΩ)

4. Experimental prototype

To demonstrate the potential of this topology, a prototype has been developed. The final design is carried out with the parameters and devices listed in Table 6. The final prototype is



(a) $V_{in} = 320$ V (b) $V_{in} = 400$ V

Fig. 12. Breakdown of theoretical losses of the 240 W AHBF prototype ($P_o = 240$ W).

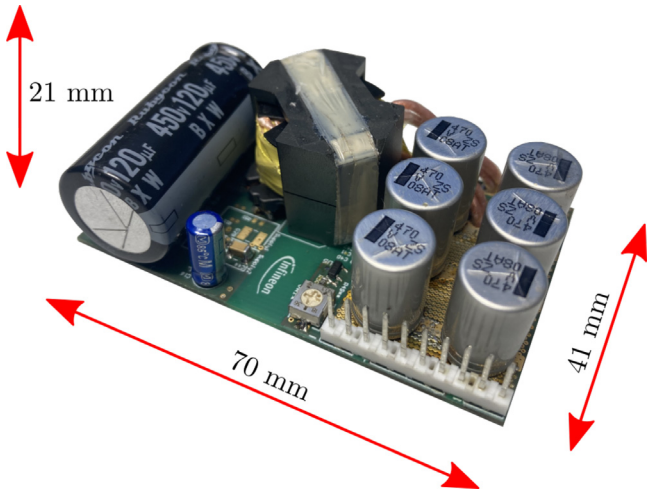


Fig. 13. Prototype built for experimental testing.

shown in Fig. 13, including both the power and control circuit. The circuit is built on a PCB with 2 oz of copper. The largest elements are the transformer and the input and output capacitors, so the dimensioning of these elements is crucial for achieving a small volume. In this case, the choice of an RM10 core results in the size of the converter being compact and suitable for microgrid applications.

4.1. Control method

The control is implemented in a modified version of the XDPS2201, a programmable controller from Infineon Technologies AG, on the basis of the modulation methods present in Medina-Garcia et al. (2021a). Fig. 14 shows a diagram of the control functions.

There are two different control modes that are switched at 50% load to maximize efficiency. The two modes are:

- **Continuous Resonant Mode (CRM)**. It is applied for high loads. The control is performed with complementary asymmetrical pulses in the high side Q_1 and low side Q_2 MOSFETs with dead time to avoid cross conduction and to achieve ZVS according to Eq. (10). V_{in} is measured to accomplish ZVS in all conditions. Using the voltage in shunt resistor R_s, peak current $I_{hb_{max}}$ is controlled considering the feedback coming from secondary side. The waveforms of this modulation are in Fig. 15(a).
- **Zero Voltage Resonant Valley Switching (ZV-RVS)**. This modulation is the discontinuous conduction mode for lighter loads, similar to a quasi-resonant flyback (Onay et al., 2018). First, a pulse is applied to the low side MOSFET Q_2, allowing the necessary negative current to achieve ZVS on the high side MOSFET Q_1. Following pulses are equivalent to the CRM mode. After that, unlike in the previous case, a waiting time T_w is applied in which there are no pulses and the transformer's current i_{L_m} reaches zero. The *ZCD* (Zero Crossing Detection) in Fig. 14, measured with an auxiliary winding of the transformer L_{aux}, gives the information to the controller about when the voltage on the half-bridge is zero. Thus, the cycle is always restarted with 0 V on the low side, so ZVS is achieved despite free oscillations during waiting time. Fig. 15(b) shows the behaviour of the topology with this modulation.

Eq. (16) shows how the output current I_o is affected by the control variables $I_{hb_{max}}$, $I_{hb_{min}}$, T and T_a in both control methods. Expression in ZV-RVS is the same that in the CRM case with the difference of a proportion $\frac{T_a}{T}$ which is the relation between the time while the transformer is actively energized T_a and the total period T.

$$I_o = \begin{cases} \dfrac{N(I_{hb_{max}} + I_{hb_{min}})}{2} & \text{CRM} \\ \dfrac{N(I_{hb_{max}} + I_{hb_{min}})}{2}\dfrac{T_a}{T} & \text{ZV-RVS} \end{cases} \tag{16}$$

4.2. Experimental results

To test the converter under different conditions, the output feedback is adjusted to obtain different values of output voltage. In Fig. 16 the efficiency versus load is shown for different working cases (Fig. 16(a): $V_o = 6$ V, Fig. 16(b): $V_o = 12$ V and Fig. 16(c): $V_o = 24$ V). The load excursion is swept from $I_o = 1$ A = 10% to $I_o = 10$ A = 100%. The experiment is carried out for different input voltages, from $V_{in} = 320$ V to $V_{in} = 400$ V. In the case of a very low output voltage, the input voltage starts with $V_{in} = 340$ V due to the need for a correct self supply of the control. With 24 V at the output, maximum power of $P_o = 240$ W is obtained. Graph 16 shows the highest efficiency in this case, for which the prototype is dimensioned. The losses are $P_{loss} = 5.78$ W at $V_{in} = 380$ V, resulting in a maximum efficiency of 97.59%. For lower voltage values in the output, the following maximum efficiencies are obtained at $V_{in} = 380$ V: for $P_o = 60$ W, losses are $P_{loss} = 5.28$ W and efficiency is 91.19%. For $P_o = 120$ W, losses are $P_{loss} = 3.91$ W and efficiency is 96.74%.

In the theoretical estimation made in the previous section, the losses obtained with $V_{in} = 400$ V and maximum output power were $P_{loss_{model}} = 5.41$ W, while the measured value is $P_{loss_{exp}} = 5.81$ W. With $V_{in} = 320$ V, the theoretical estimation was $P_{loss_{model}} = 6.17$ W and the measured value is $P_{loss_{exp}} =$

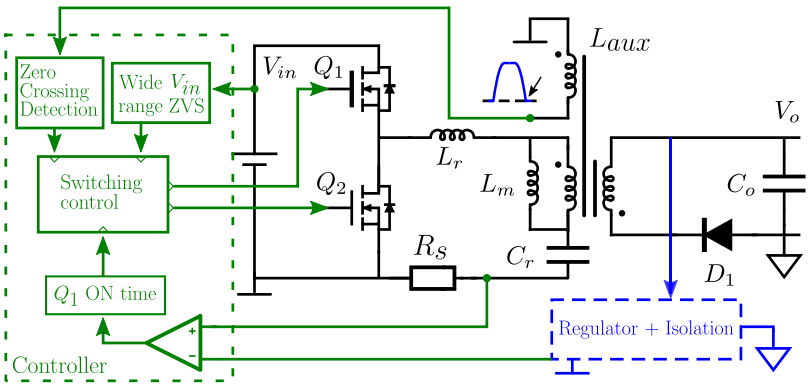
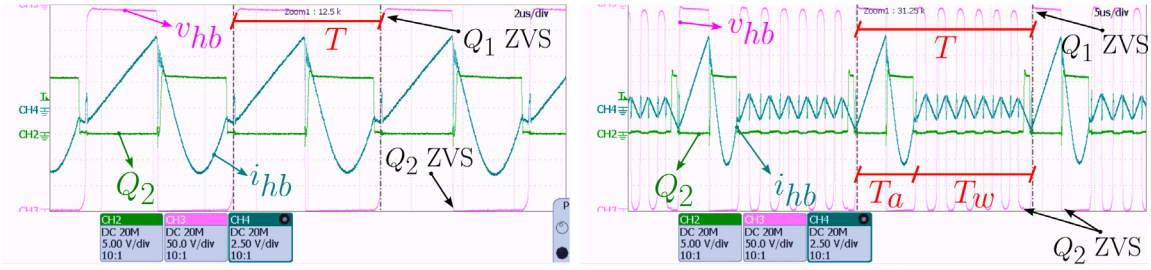
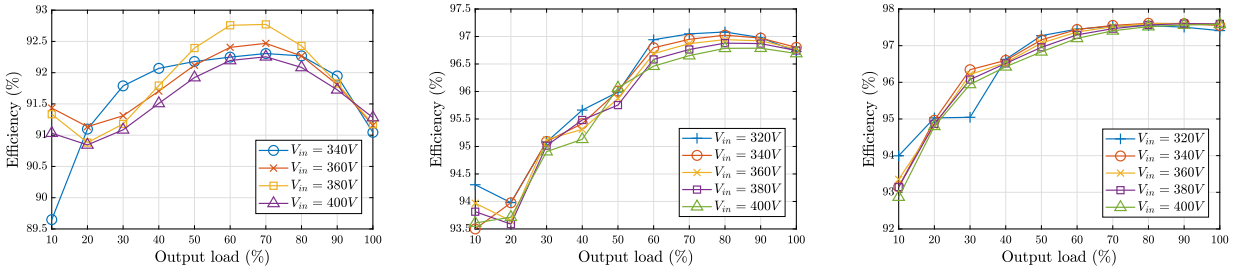


Fig. 14. Basic control diagram for the converter.



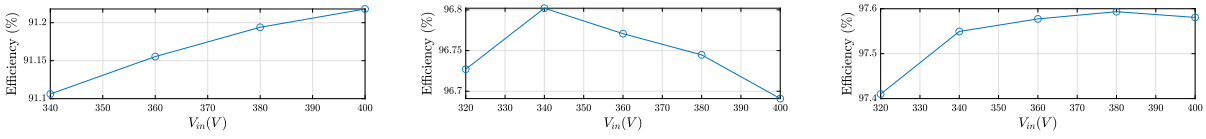
(a) CRM. $I_o = 10$ A. (b) ZV-RVS. $I_o = 3$ A.

Fig. 15. Actual waveforms of the converter measured for different output loads. $V_{in} = 380$ V, $V_o = 24$ V.



(a) $V_o = 6$ V (b) $V_o = 12$ V (c) $V_o = 24$ V

Fig. 16. Efficiencies vs load for different values of input and output voltages.



(a) $V_o = 6$ V (b) $V_o = 12$ V (c) $V_o = 24$ V

Fig. 17. Efficiency results for an input voltage sweep with $I_o = 10$ A.

6.22 W. The relative errors are respectively 7.39% and 0.81%, probably due to some mechanisms not considered in the analysis, as the resistance of the PCB tracks, the soldering connection of the components or the gap effect in the transformer. The latter mechanism is particularly important since the model is more accurate at lower input voltages, which indicates that loss mechanisms that increase with input voltage, and therefore frequency, such as magnetic losses, are underestimated.

To visualize how mildly the efficiency of the converter is affected by a variation of the input voltage, Fig. 17 shows a sweep of the input voltage for each output voltage case at 100% of load.

Finally, the ripple of the output voltage is measured for different conditions. It is observed that there is a big different between the CRM and the ZV-RVS, with the ripple being larger in the discontinuous mode, due to the discharge of the output capacitor because of the long waiting time between one set of pulses and the next (see Fig. 18). The experimental value differs slightly from the estimated theoretical value, possibly due to the simplification of parasitic elements in the calculation and measurement errors.

5. Comprehensive comparison of topologies

As stated in the introduction, in order to facilitate the large-scale deployment of DC microgrids, the power converters used

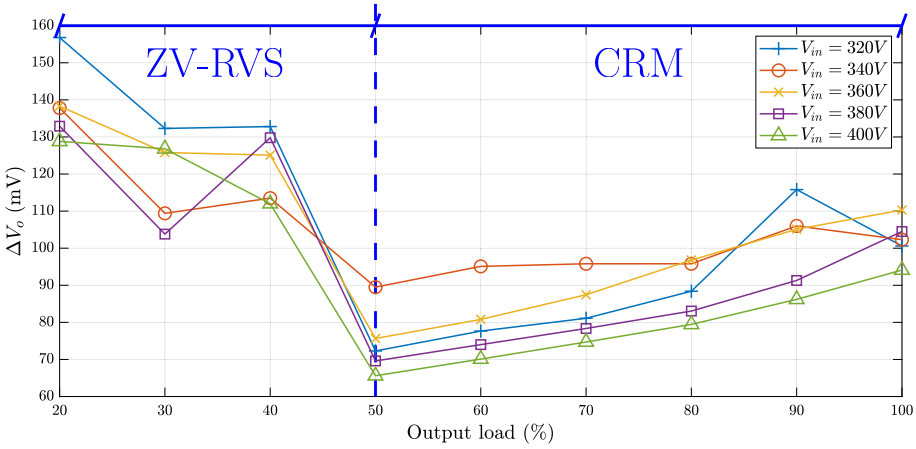


Fig. 18. Converter output voltage ripple for different operating points. $V_o = 24$ V. The difference by changing the modulation mode between CRM and RVS at 50% load is observed.

Table 7
Comprehensive comparison of different DC–DC topologies.

Converter	V_{in} rating	V_o rating	N° of switches	N° of diodes	N° of transformers' 2nd windings	Nominal power	Maximum efficiency	Soft switching
Proposed topology	320–400 V	5–24 V	3	0	1	240 W	97.6	Q_1–Q_2: ZVS Q_3: ZCS
Dual-bridge LLC (Sun et al., 2017a)	120–240 V	24 V	6	2	2	480 W	96.2	Q_1–Q_6: ZVS D_1–D_2: ZCS
Single-stage LLC (Kim et al., 2018)	127–380 V	16.5 V	4	0	2	60 W	96.17%[a]	Q_1: ZVS
MRC (Yang et al., 2018)	25–300 V	200 V	8	4	2	200 W	98.1	Q_1–Q_4: ZVS D_1–D_4: ZCS
LCLC (Chen et al., 2016)	250–400 V	12 V	4	0	2	500 W	97.9%	Q_1–Q_2: ZVS
2 transformers LLC (Hu et al., 2013)	25–100 V	210 V	6	8	2	250 W	98%	Q_1–Q_4: ZVS
Modified LLC (Sun et al., 2017b)	250–400 V	200 V	6	2	1	420 W	97	Q_1–Q_6: ZVS D_1–D_2: ZCS
EVLMG1-250WLLC (Hempt, 2021)	360–440 V	24 V	4	0	2	240 W	95	Q_1–Q_2: ZVS Q_3–Q_4: ZCS
CrCM Flyback (Pal et al., 2020)	120–375 V	10–50 V	1	1	1	100 W	92%[a]	–
Lossless snubber Flyback (Soltanzadeh and Yousefi, 2018)	120–190 V	24 V	2	7	1	240 W	91.3	Q_1–Q_2: ZCS D_2–D_5: ZCS D_6–D_7: ZVS
Active clamp Flyback (Yoo et al., 2017)	300–320 V	12 V	3	0	1	60 W	89.5%	–

[a]These efficiencies include an AC–DC step.

need to operate with wide voltage ranges to work in any condition, small enough to be used in the various possible applications, low cost to make them more attractive, and high efficiency to be able to reduce size and not waste energy.

A comparison is made with different state-of-the-art converters to demonstrate that this topology is a solid candidate in this field. The parameters to compare are: (1) the input and output voltage range, (2) the efficiency achieved, (3) the volume occupied by the converter and (4) the number of switches which are necessary as well as the transformer and inductive elements (they are going to determine the complexity and contribute to increase the cost). Regarding this last parameter, the number of windings in the secondary side are counted. They can be in the same transformer or in different ones.

Table 7 summarizes several state-of-the-art solutions which can be divided into two main groups. On the one hand, there are converters based on variants of the LLC, which exploits the resonance of a resonant tank to transmit energy: a dual-bridge LLC (Sun et al., 2017a), a single-stage LLC (Kim et al., 2018), a morphing multi-element resonant converter (MRC) (Yang et al., 2018), an LCLC (Chen et al., 2016), an LLC with two transformers (Hu et al., 2013) or a modified LLC with a secondary paralleled bidirectional switch (Sun et al., 2017b). These solutions require several additional elements that increase its price, volume and complexity to obtain a high voltage range. On the other hand, there are some examples of those based on flyback converters: a CrCM flyback (Pal et al., 2020), a flyback with double passive lossless snubber (Soltanzadeh and Yousefi, 2018) or an active clamp flyback (Yoo et al., 2017). In this case, the topologies are very limited in efficiency due to the absence or ineffectiveness of the recycling of leakage energy, and to the fact that all the energy transmitted from primary to secondary is stored exclusively in the transformer, which requires a larger volume. The hybrid flyback converter is proposed as a mixed solution, recycling the leakage energy of the transformer to reduce the storage in it, thus reducing its volume, but also allowing a wide voltage range with

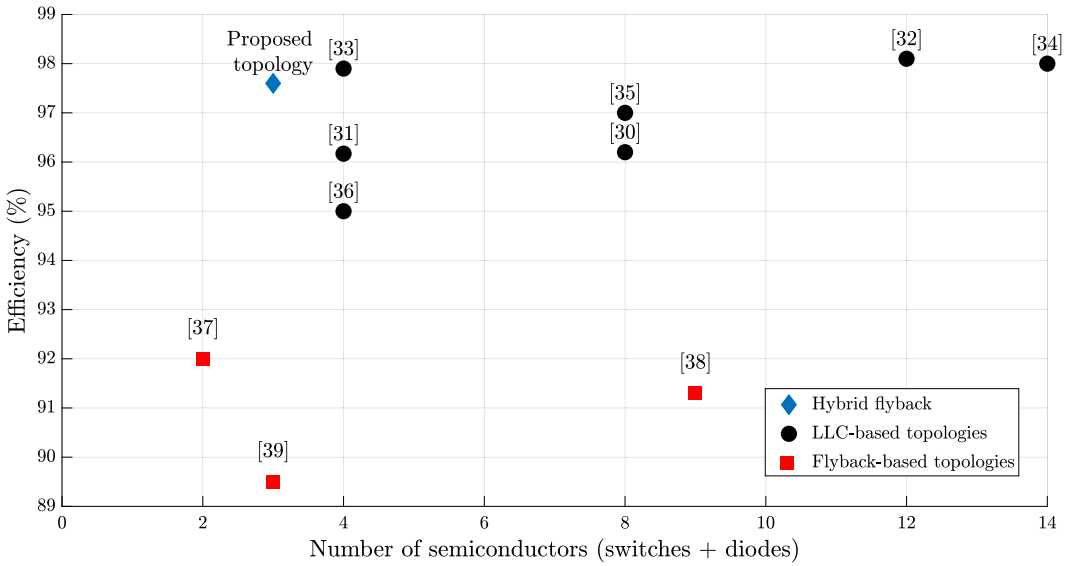


Fig. 19. Efficiency vs. number of semiconductors (switches + diodes) for each topology in Table 7.

few elements. Adding all the elements in the table that provide complexity (switches diodes and windings in transformer), the AHBF only has 4, compared to more than 6 in all the LLC cases, reaching up to 16 elements in the case of the LLC with double transformer. The 97.6% of efficiency remains above those based on flyback, and similar to the LLC solutions. In addition to its simplicity and high efficiency, a wide voltage range is permitted at both the input and output, which is not observed in the other solutions.

Fig. 19 shows the achieved efficiency vs. the number of required semiconductors for each converter in Table 7. For these power and voltage ranges, the proposed topology achieves values of efficiency comparable to LLC-based topologies with a number of elements comparable to flyback-based topologies.

To visualize the size reduction, the prototype can be compared to the EVLMG1-250WLLC since its volume data is available (Hempt, 2021). In the state-of-the-art solution, the volume is much higher (100 × 60 × 35 mm) than in the AHBF (70 × 41 × 21 mm), even though it has a lower efficiency and uses GaN semiconductors which are better for increasing efficiency and power density compared to the silicon used in this paper (Medina-Garcia et al., 2021b). Because of this, the power density of the AHBF is 65 W/inch^3, while in the LLC is 20 W/inch^3.

6. Conclusion

This paper proposes the asymmetrical hybrid flyback converter as a solution for the requirements of power converters for DC microgrids, satisfying the need for small size and high efficiency converters with wide voltage ranges. An iterative design process based on loss estimation is proposed to take the topology beyond its conventional use in very low power applications present in the state of the art, towards more generic and higher power applications to be used in a DC microgrid. Starting with the number of turns of the transformer, the rest of the devices and parameters are dimensioned analytically step by step: switching elements, frequency, magnetizing inductance, transformer and resonant capacitor. Once a first set of parameters is worked out and the losses determined, a theoretical value of the efficiency is estimated, allowing iterations to be performed until the most appropriate design in terms of efficiency and volume is obtained.

The theoretical design is empirically tested by making a prototype with an output power of $P_o = 240$ W, a power density of 65 W/inch^3, an input voltage range of $V_{in} = 320$ V–400 V, an output range of $V_o = 5$ V–24 V and a peak efficiency of 97.6%. These results are compared with other state-of-the-art solutions based on LLC and flyback converters for similar applications, and it is observed that there is a great improvement in terms of power density, efficiency, size, volume, voltage range and complexity. It is concluded that this novel topology is a great candidate for the new demands of DC microgrids.

CRediT authorship contribution statement

Juan Cruz-Cozar: Conceptualization, Methodology, Investigation, Validation, Software, Writing – original draft. **Alfredo Medina-Garcia:** Conceptualization, Methodology, Investigation, Software, Writing – review & editing. **Diego P. Morales:** Supervision, Funding acquisition, Writing – review & editing. **Noel Rodriguez:** Supervision, Funding acquisition, Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The data that has been used is confidential.

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