Synchronous rectifiers drain voltage overshoot reduction in PSFB converters

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***Abstract*— The requirements for the blocking voltage of the rectification devices on the secondary side of Phase Shift Full Bridge DC-DC converter topology are, by nature, higher than for other quasi-resonant or fully resonant topologies (DAB, LLC). This is especially aggravated in wide range operation converters and further increased by the rectifiers' drain voltage overshoot. Unlike other resonant topologies, the inductor at the output of the PSFB effectively decouples the capacitor bank from the rectification stage, which otherwise acts as a strong lossless snubber. Higher blocking voltage requirements for the rectification devices worsen their Figure of Merit, increasing their related losses and decreasing the overall efficiency of the converter. In this paper the main causes of the rectifiers drain voltage overshoots in PSFB are analyzed. Design guidelines for the mitigation of the different causes are introduced, as well as a novel modulation scheme for the overshoot reduction while the output filter operates in DCM, without penalties in performance, complexity or cost. A prototype of PSFB DCDC converter of 3300 W, with 400 V input to 54.5 V output nominal voltages, was designed and built to test the proposed solutions achieving a peak efficiency of 98.12 % at 50 % of load.**

***Index Terms*— Phase Shift Full Bridge, modulation technique, synchronous rectifier, drain voltage overshoot.**

I. INTRODUCTION

The Phase Shift Full Bridge (PSFB) is a buck derived isolated converter topology commonly used in medium to high power (one to several kW) DC-DC converter applications as a single stage or as the output stage of a full AC-DC converter. PSFB is commonly used with the input at high voltage (350 V to 450 V) and the output at low voltage (12 V to 60 V) and relatively high current for server, telecom and battery charging applications [1]. High output voltage designs are not common since the high-voltage (HV) requirements of the rectification devices on the secondary side make other alternatives more attractive [2]-[3].

Like other resonant or quasi-resonant topologies PSFB can achieve zero voltage switching (ZVS) on the primary side devices, nearly suppressing switching losses, which are especially high for HV devices in hard-switched converters [4]. ZVS enables higher efficiency, lower cost, higher power density or a combination of those.

Like other isolated topologies, the blocking voltage of the secondary side devices depends on the rectification stage configuration: it is two times the transformer reflected secondary voltage for center tapped and current doubler, or one time the transformer reflected secondary voltage for full bridge [5].

Unlike other resonant topologies, the output filter stage of the PSFB converter is composed, at least, of an inductor L_o and a bank of capacitors C_o. The inductor at the output effectively decouples the secondary side rectification devices from the output capacitance bank (Fig. 1). Therefore, the drain voltage of the secondary side devices is not as effectively clamped as in other converters such as LLC or DAB [6]-[8].

Moreover, the secondary reflected voltage of the transformer does not depend on the output voltage (V_o) and it is always necessarily higher than it. In the PSFB converter the output of the rectification stage is a square wave of duty cycle D_{eff}, with the amplitude of the transformer reflected voltage and the average value V_o. The reflected voltage is proportional to the transformer turns ratio and the input voltage, as expressed in (1) where V_E and V_D represents the amplitude of the output voltage of the rectification stage, and N_P and N_S respectively the primary and secondary turns of the main transformer.

$$V_o = \frac{N_S}{N_P} V_{in} D_{eff} = V_{in} \frac{D_{eff}}{n} = V_D D_{eff} = V_E D_{eff} \quad (1)$$

D_{eff} is necessarily less than or equal to one and, in practical converters, commonly much smaller, as the transformer turns ratio *n* is constrained by the input and output voltage range requirements: the converter should be capable of regulation at the minimum specified input voltage $V_{in,min}$ and maximum specified output voltage $V_{o,max}$.

Wide input voltage is required, for example, during hold-up time conditions [7], [9]-[11]. The power supply needs to maintain its output voltage during a time period of 20 ms (T_{hold}) after

the input AC line is lost. Hold-up operation is required in applications with demanding requirements on power supply continuity and reliability, such as sever power supply and telecommunication systems. This results in a minimum input voltage $V_{in,min}$ at the end of T_{hold}.

The wide regulation requirement makes PSFB converter not to be operated with its maximum duty in nominal state. Additionally, because of the time it takes to the current through the transformer to reverse polarity, part of the ideally available duty is lost (D_{loss}), which further constraints the maximum possible transformer turn ratio, the external resonant inductance and the leakage of the transformer, which should be conveniently dimensioned to reach the maximum power of the converter at the minimum specified input voltage (2)-(6). During the remaining duty, the so-called freewheeling (D_{frw}), the primary current recirculates without transferring energy to the output of the converter.

$$D_{loss} = 2F_{sw}\frac{(L_r+L_{lkg})}{V_{in}}\Delta iL_{r,1} \quad (2)$$

$$\Delta iL_{r,1} \approx \frac{2iL_{o,avg}}{n} \ , L_o \ in \ CCM \quad (3)$$

$$D_{loss,max} = 4F_{sw}\frac{(L_r+L_{lkg})}{V_{in,min}}\frac{iL_{o,avg,max}}{n} \quad (4)$$

$$D_{eff} + D_{frw} + D_{loss} = 1 \quad (5)$$

$$D_{frw} \geq 0 \xrightarrow{yields}$$

$$V_{in,min} \geq \left(nV_{o,max} + \frac{4F_{sw}(L_r+L_{lkg})iL_{o,avg,max}}{n}\right) \quad (6)$$

Any additional overshoot above the nominal blocking voltage (V_D and V_E) would require to further increase the maximum limits of the blocking voltage capabilities of the rectification devices (Fig. 2); or alternatively to use clamping or snubbering mechanisms that bring additional power losses, complexity and cost [12]-[13]. Furthermore, it is a common practice, in the design of switched mode power supplies (SMPS), to limit the maximum stress on the components (voltage, current, temperature) to a rated percentage of their safe maximum limits under any normal working conditions of the converter [14]. The rating percentage depends on the application, lifetime and reliability requirements, but 80 % is a common choice. For semiconductor devices the commonly rated parameters are the maximum drain voltage and the working temperature.

Because there is only a limited variety of voltage classes available in the market, increasing the blocking voltage may force the designer to go for a rather high voltage class where the available device technology has a worse figure of merit and could be further constrained to a limited $R_{DS,on}$ portfolio. A summary of the characteristics of two devices with similar $R_{DS,on}$ in Table I shows the influence of the blocking voltage in their characteristic charges and forward voltage drop, which ultimately affects the switching and conduction losses.

In PSFB converters several mechanisms induce or could induce the above mentioned secondary side rectifiers drain voltage overshoot [5], mostly not properly explored in the literature. In the following sections we analyze the most common causes, and provide design guidelines and control solutions for the reduction or suppression of the parasitic overshoots enabling high efficiency PSFB designs with the minimum possible secondary side voltage class devices. The rectification stage may have different configurations: center tapped, current doubler or full bridge; each of them having its advantages in different applications: low voltage, high current or high voltage outputs respectively [15]; however these alternatives have no major impact on the working principles of the converter and the solutions proposed here.

The rest of this document is organized as follows: in Section II a detailed analysis of the overshoot causes is conducted and previous literature is reviewed; in Section III a comprehensive analysis of the proposed overshoot reduction techniques are presented including a novel discontinuous conduction mode (DCM) control scheme; the study is confirmed by experimental results presented in Section IV; and finally, Section V presents a summary of conclusions out of this work.

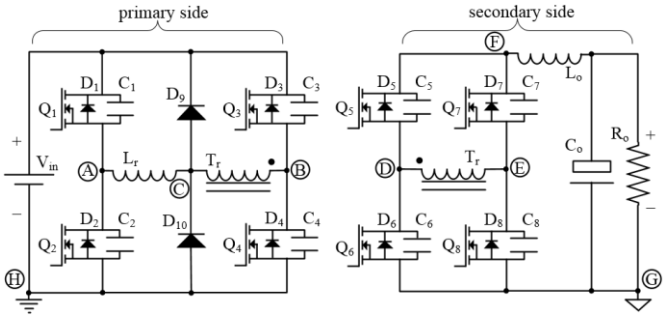


Fig. 1. Conventional phase shift full bridge DC/DC converter configuration with full bridge rectification and primary side clamping diodes.

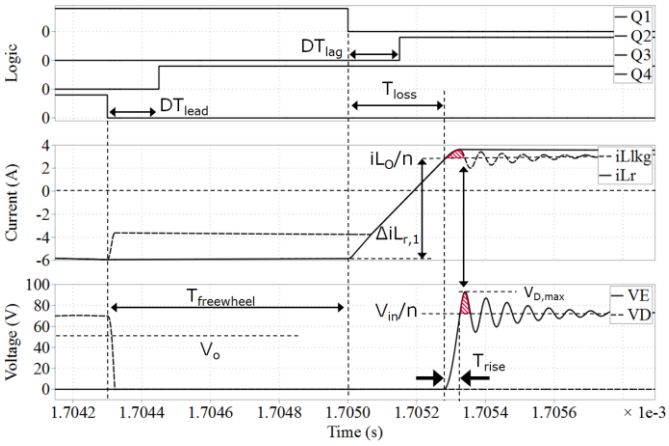


Fig. 2. Secondary side drain voltage overshoot increases the blocking voltage requirements for the rectification devices.

TABLE I
SI LV MOSFETS

	BSC093N15NS5	BSC098N10NS5
$V_{DS,max}$	150 V	100 V
$R_{DS,on,,max}$	9.3 mΩ @ 25 °C	9.8 mΩ @ 25 °C
Q_{oss}	91 nC	30 nC
Q_g	33 nC	22 nC
Q_{rr}	58 nC	73 nC
V_f	0.88 V	0.9 V

II. OVERSHOOT MECHANISMS ANALYSIS

A. COMMUTATION OVERSHOOT

The secondary side rectification devices are naturally commutated by the transformer reflected voltage, which is an effect of the primary side devices alternating the polarity of the voltage applied to the primary of the transformer. Thanks to that, the synchronous rectifiers (SRs) can be turned both on and off under ZVS conditions. They are, however, hard commutated and because certain body diode conduction is unavoidable in most practical cases, they require reverse recovery charge (Q_{rr}) for the diodes with the consequent additional related losses [16]-[17].

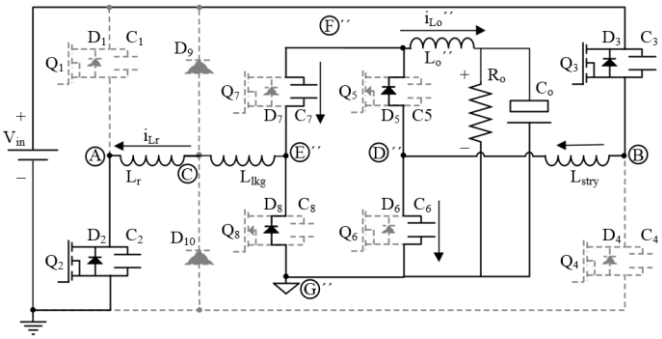


Fig. 3. Simplified equivalent circuit of the converter during the commutation of Q_6 and Q_7.

The energy required to charge the output capacitance (Q_{oss}) and Q_{rr} of the rectification devices during their commutation comes from the primary side through the transformer. Meanwhile, in the process of charge, all inductances appearing on the charging path (L_r, L_{lkg}, L_{stry}) (Fig. 3) store energy, which can be estimated by (7). That stored energy will subsequently cause a resonance together with the secondary side rectifier's output capacitance (C_{oss}) at the frequency given by (8) [5]. The energy of that resonance would cause a maximum peak voltage that can be calculated by (9)-(10). Subsequently the resonance energy will be partially lost in the resistive path as the resonance dampens or within other snubber, or clamping mechanisms [12].

$$\left.\begin{matrix} Q_{oss,5} = Q_{oss,6} = Q_{oss,7} = Q_{oss,8} = Q_{oss} \\ Q_{rr,5} = Q_{rr,6} = Q_{rr,7} = Q_{rr,8} = Q_{rr} \end{matrix}\right\} \xrightarrow{yields}$$

$$\left(\frac{iL_{r,com}^2}{2}L_r + \frac{iL_{lkg,com}^2}{2}L_{lkg}\right) = \frac{V_{in}}{n}(Q_{rr} + Q_{oss}), t_1 = \frac{\pi}{2\omega_1} \quad (7)$$

$$C_5 = C_6 = C_7 = C_8 = C_{SR} \xrightarrow{yields} \omega_1 = \frac{1}{\sqrt{2C_{SR}(L_{lkg}+L_r)}} \quad (8)$$

$$V_F(t) = V_E(t) = V_D(t) = V_{F,pk}(1 - \cos(t\omega_1)) \quad (9)$$

$$V_{F,pk} = \left(\frac{iL_{r,com}^2}{2Q_{oss}}L_r + \frac{iL_{lkg,com}^2}{2Q_{oss}}L_{lkg}\right) + \frac{V_{in}}{n}, t_2 = \frac{\pi}{\omega_1} \quad (10)$$

High frequency and high amplitude resonances can jeopardize driver and power switch integrity, and often cause electromagnetic interference (EMI) issues because of their high *dv/dt* and *di/dt* nature. The common mode (CM) noise of SMPS, which propagates in phase through both the power lines and returns from the ground, is mainly associated with high *dv/dt* nodes in the circuit and the parasitic capacitance between these nodes and ground. The CM noise characteristic of the converter is therefore determined by the voltage spectrum characteristics of the voltage pulsating nodes in the circuit [18]. The ringing is known to cause broadband EMI problems, the frequency of which is centered at the ringing frequency [19]-[20].

In [21] the analysis of the commutation resonance includes L_r, the parasitic capacitance and leakage of the transformer, the parasitic capacitance of the rectifier, and the capacitor of a snubber in a fifth-order model. This implies that the voltage ringing across the rectifiers should be a waveform including more than one frequency component. However, aside from the limited effectivity and applicability of the proposed method, the fact that only a small amount of the resonance could be cancelled probes the minor contribution of the other frequency components.

The traditional RC dampening snubber is not frequently used because of its large losses. Alternatively, an RCD snubber circuit limits the peak voltage of the resonance and its dampening with acceptable losses [22]-[23]. However, the design of the RCD network is not straightforward and requires a tradeoff between effectivity and power losses (11).

$$E_{RCD} \propto \left(\frac{V_{in}}{2n}(Q_{rr} + Q_{oss}) - \frac{V_{F,pk}}{2}Q_{oss}\right) \quad (11)$$

A comparison of considered "lossless" snubber circuits is presented in [12] and [24]. These circuits recover part of the clamped oscillation energy and consist entirely of a combination of passive components: diodes and capacitors. However, they are difficult to optimize for wide range converters: the resulting peak voltage overshoot depends on the effective duty of the converter. The best result is obtained with a combination of a diode and extra windings on the secondary side of the transformer, which complicates the manufacture of the magnetics and the layout of the board. The same working principle is applied with less complexity in [25] where the clamping diodes are placed on the primary side winding of the transformer.

An active clamp circuit on the secondary side consisting of an additional switch and a capacitor was proposed in [26]-[27]. While the solution seems promising, it has the added complexity of controlling an extra active switch in the converter. Furthermore, the related additional losses cannot be neglected: conduction and switching losses of the switch, and charge-discharge loss of the snubber capacitor. Another alternative snubber configuration is proposed in [28] where the additional switch is placed in the main path of the current at the output. However, the placement is not practical for converters with low voltage and high current outputs.

In [29]-[30] a regenerative Flyback converter replaces the resistor in an RCD snubber circuit thus recovering part of the energy. Additionally, this Flyback provides isolation and enables soft-start capability of the proposed bidirectional converter in [29]. The active regenerative snubber concept can be extended to other isolated or non-isolated topologies. In [31] a non-isolated buck converter feeds the clamped oscillation energy to the output of the converter. However, the conclusion in [30] is that the extra complexity does not justify the efficiency improvement considering that the traditional RCD snubber demonstrates to be far more effective reducing the voltage overshoot.

B. DCM OVERSHOOT

Under certain load conditions the average output current of the converter becomes lower or equal than half of the current ripple through L_o, which can be calculated with (12), where F_{sw} represents the switching frequency of the converter. In this scenario there are three main alternatives for the operation of the converter [17]:

- The output filter works naturally in DCM. This is the case of converters with passive rectification devices, like diodes, or not enabled active devices taking advantage of their intrinsic body diode.
- The output filter works in DCM but the SRs are enabled and driven in a similar manner to ideal diodes. This mode increases the efficiency of the converter, at least along certain load range where the additional driving losses are compensated by the reduction in forward voltage drop (Fig. 4).
- The output filter is forced to work in continuous conduction mode (CCM) when the active rectification devices are driven maintaining the same standard CCM modulation scheme along all load range.

$$\Delta I_{Lo,CCM} = V_o \frac{(1-D_{eff})}{2F_{sw}L_o} \quad (12)$$

A potential problem arises when the converter operates in any of the above mentioned DCM modes and L_o resonates back together with the output capacitance of the rectification devices. The maximum induced peak voltage of this resonance can be as high as twice the output voltage of the converter.

At the start of the resonance both the energy in L_o and the output capacitance of the rectifiers is zero (13). When the output capacitance of the rectifiers has been charged up to V_o, equal energy has been stored in L_o and the capacitors (14)-(15). Subsequently all the energy in L_o flows into the output capacitance of the devices (16).

$$E(t_0) = E_{Lo}(t_0) + E_{Csr,total}(t_0) = 0 \quad (13)$$

$$\omega_2 = \frac{1}{\sqrt{4C_{oss}L_o}} \ , \ t_1 = \frac{\pi}{2\omega_2} \ , \ t_2 = \frac{\pi}{\omega_2} \quad (14)$$

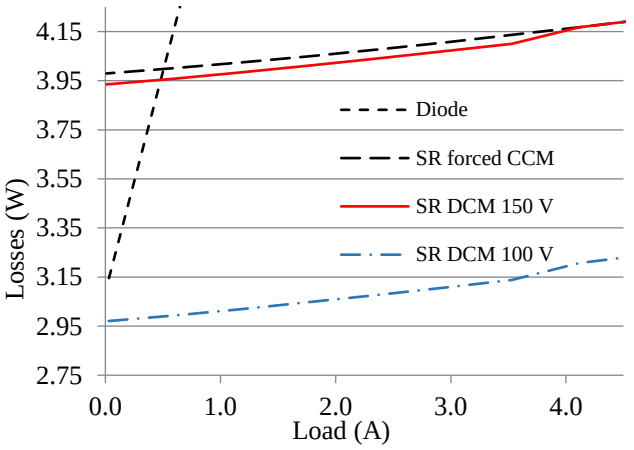


Fig. 4. Comparison of losses between the alternative operation modes of the SRs at light load. The estimated values account for the driving, switching and conduction losses of the SRs of the converter prototype in section IV.

$$E(t_1) = E_{Lo}(t_1) + E_{Csr,total}(t_1) = \frac{1}{2}L_o I_{Lo}^2 + \frac{1}{2}2Q_{oss}V_o \quad (15)$$

$$E(t_2) = E_{Lo(t_2)} + E_{Csr,total}(t_2) = 0 + 2Q_{oss}V_o \quad (16)$$

In a full bridge rectification stage configuration the peak voltage of the above mentioned DCM overshoot is blocked by two stacked devices and it is likely to be distributed near equally between them (considering all devices have near equal output capacitance) (17). For the center tapped or current doubler configurations the devices are anyhow dimensioned to block at least two times the transformer reflected voltage [5]. It follows that, in any of those scenarios the induced DCM resonance peak voltage is well under the blocking voltage limits for the secondary side devices already considered in normal working conditions.

$$\begin{cases} V_F(t) = 2V_o\,(1-\cos(t\omega_2)) \\ V_E(t) = V_D(t) = V_o\,(1-\cos(t\omega_2)) \end{cases}, V_{CB} = 0 \quad (17)$$

However, in the special case where the commutation of the rectification devices occurs in the middle of a DCM resonance, the voltage already stored in their C_{oss} effectively stacks on top of the transformer secondary reflected voltage, now likely exceeding the nominal blocking voltage limits (18). Additionally, the previously described commutation overshoot will also appear in a cumulative manner to this mechanism.

$$\begin{cases} V_E(t) = V_o\,(1-\cos(t\omega_2)) + \frac{V_{in}}{n} \\ V_D(t) = V_o\,(1-\cos(t\omega_2)) \end{cases}, V_{CB} = V_{in} \quad (18)$$

C. FORCED CCM OVERSHOOT

If the converter works in forced CCM but the active rectifiers happens to turn off while the current through L_o is flowing back against their intrinsic body diodes, the current path becomes blocked and the energy stored in L_o instead charges up the output capacitance of the devices (Fig. 5). Like in the previously described DCM overshoot scenario, the mechanism of these phenomena is a resonance between L_o and the output capacitance of the SRs. However, since in forced CCM the current through L_o becomes more negative than during DCM operation, there would be more energy stored at the start of the resonance (19). The induced drain voltage overshoot easily becomes large enough to reach the drain voltage breakdown limit of the rectification devices (20)-(21).

$$E_{Lo}(t_0) = \frac{1}{2}L_o I_{Lo}^2(t_0) \gg 0 \quad , \quad E_{Csr,total}(t_0) = 0 \quad (19)$$

$$E(t_2) = E_{Lo}(t_2) + E_{Csr,total}(t_2) = 0 + E_{Lo}(t_0) \quad (20)$$

$$\begin{cases} V_F(t) = \frac{L_o I_{Lo}^2(t_0)}{4Q_{oss}}\,(1-\cos(t\omega_2)) + \frac{V_{in}}{n} \ , \ V_{CB} = V_{in} \\ V_F(t) = \frac{L_o I_{Lo}^2(t_0)}{4Q_{oss}}\,(1-\cos(t\omega_2)) \ , \ V_{CB} = 0 \end{cases} \quad (21)$$

To avoid this problem it is required that the SRs always turn off while the current through L_o is positive (flowing towards the output of the converter), zero or nearly zero. The controller has to ensure that the transition from CCM to DCM operation happens before the output inductor current changes polarity or to ensure a proper turn off sequence when the converter operates in forced CCM.

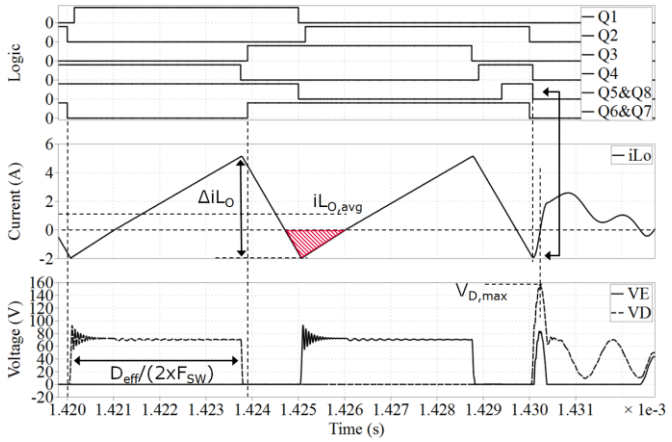


Fig. 5. Forced CCM. Induced drain voltage overshoot when the SRs are turned off while iL_o is lower than zero.

III. OVERSHOOT REDUCTION TECHNIQUES

A. COMMUTATION OVERSHOOT REDUCTION

The use of an external resonant inductance (L_r) in the primary side of PSFB, while increasing the component count, helps achieving ZVS in light to medium load conditions and thus increases the overall efficiency of the converter. Although it is possible to increase the leakage of the transformer for the same purpose, using an external resonant inductance on the primary side of the converter and placing clamping diodes between the transformer and L_r helps to reduce the secondary side rectifiers overshoot as well as reducing their switching/commutation related losses [25], [32]. The solution, previously reported in the literature, is analyzed in detail in this section.

It has been mathematically demonstrated in [33]-[34] that charging a capacitor inevitably causes energy losses. When charged through a resistive path the resistor dissipates energy equal to the one eventually stored (22)-(24). The analysis shows that a capacitor can be charged with only a modest energy loss in a series RLC circuit only if the source is disconnected after one half of a resonance cycle. Otherwise the remaining energy is dissipated during the dampening of the resonance and the energy loss becomes also equal to the stored. Their analysis is consistent with the formula for the estimation of switching losses in SRs in [35].

$$E_{sourced} = E_{stored} + E_{loss} = (2Q_{oss} + 2Q_{rr})\frac{V_{in}}{n} \quad (22)$$

$$E_{loss} = (Q_{oss} + 2Q_{rr})\frac{V_{in}}{n} \ , \quad E_{stored} = Q_{oss}\frac{V_{in}}{n} \quad (23)$$

$$P_{sw} = 2F_{sw}(Q_{oss} + 2Q_{rr})V_F \quad (24)$$

During the charge of Q_{rr} and Q_{oss} in the secondary side rectification devices an equal energy is stored in the inductances along the charging path (L_r, L_{lkg}, L_{stray}). It follows that the bigger L_r is in relation to the other inductances (L_{lkg} and L_{stray}) the more energy it stores comparatively. Due to the action of the primary side clamping diodes, the energy in L_r is actually recirculated on the primary side of the converter and does not contribute to the secondary side commutation resonance.

Additionally, an increase in the overall inductance along the charging path decreases the transformer and secondary side devices *di/dt* during the commutation, which is known to reduce Q_{rr} related losses in diodes [35]-[36].

Both of these mechanisms contribute to the reduction of Q_{oss} and Q_{rr} related losses in the SRs (25)-(26) as well as to the reduction of the commutation drain voltage overshoot, which can be estimated by (27)-(28), where $iL_{r,com}$ and $iL_{lkg,com}$ represents the current passing through the inductances at their peak during the first cycle of the resonance. The conduction loss of the clamping diodes E_{clmp} can be estimated from their average current, which is analyzed in the next section.

$$E(t_1) = \left(\frac{iL_{r,com}^2}{2}L_r + \frac{iL_{lkg,com}^2}{2}L_{lkg}\right) = (Q_{oss} + Q_{rr})\frac{V_{in}}{n} \ ,$$

$$t_1 = \frac{\pi}{2\omega_1} \quad (25)$$

$$E_{loss} = \frac{V_{in}}{n}\left(Q_{oss}\frac{L_{lkg}}{L_r} + Q_{rr}\left(1 + \frac{L_{lkg}}{L_r}\right)\right) + E_{clmp} \quad (26)$$

$$\omega_3 = \frac{1}{\sqrt{2C_{oss,sr}L_{lkg}}} \quad (27)$$

$$V_F(t) = \frac{iL_{lkg,com}^2 L_{lkg}}{2Q_{oss}}(1 - \cos(t\omega_3)) \quad (28)$$

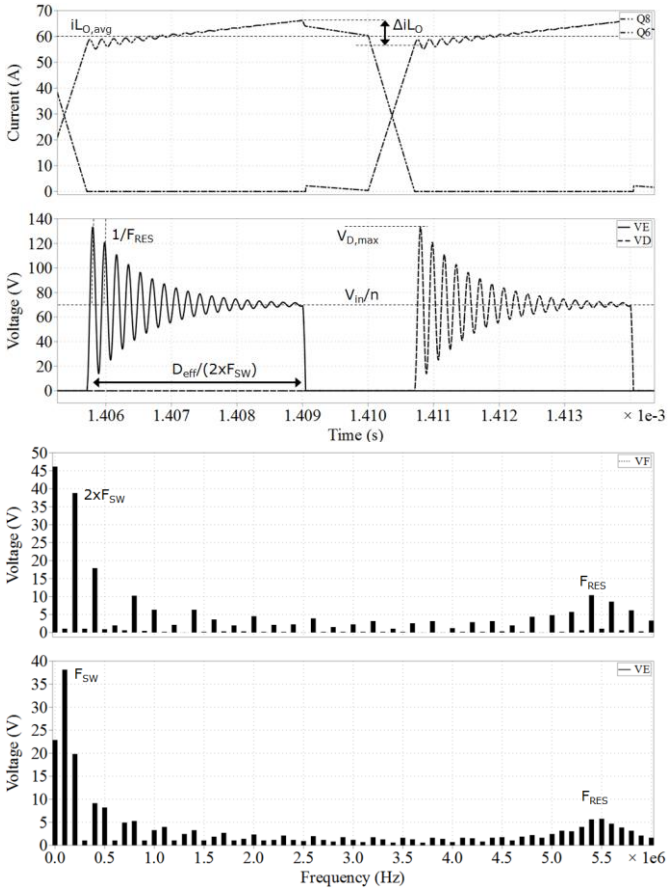


Fig. 6. Spectrum of SRs voltage and current without camping diodes on the primary side.

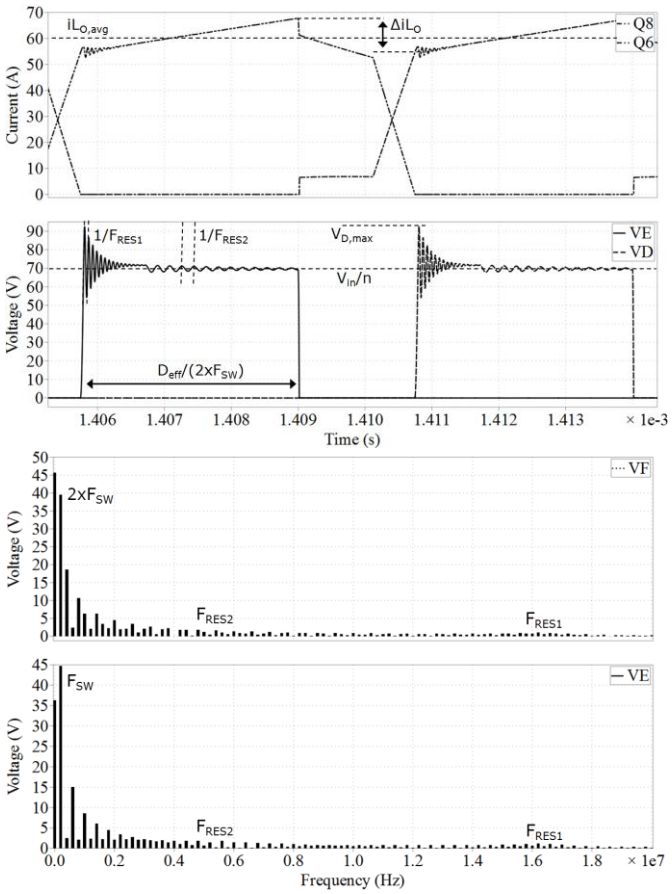


Fig. 7. Spectrum of SRs voltage and current with clamping diodes on the primary side and maximized ratio of L_r to L_{lkg}.

Fig. 6 and Fig. 7 compare the waveforms and the drain voltage spectrum of the secondary side rectifiers for two converters with the same total value of inductances in the commutation path (L_r plus L_{lkg}). Both converters are operating in the same conditions, however, the converter in Fig. 7 uses clamping diodes in the primary side and has maximized its ratio of L_r to L_{lkg}.

B. DCM OVERSHOOT SUPPRESSION

The output filter of the converter could be dimensioned in a way to ensure CCM or DCM in the boundary to CCM operation in all working conditions. This is however impractical in high efficiency converters, as it is difficult to design an efficient high value of inductance [2]. In this work we propose a solution to the induced DCM overshoot consisting of a novel modulation scheme, which does not constrain the converter design or its performance in any manner.

The key strategy is to use active rectification to overcome the DCM overshoot problem (Fig. 8). Switching on the devices prior or during the buildup time of the transformer secondary reflected voltage allows the output capacitance of the rectification devices to be discharged out from the DCM resonance energy (Fig. 9). The discharge of the precharged voltage limits the overshoot to that of a normal commutation, as in any other operating condition of the converter.

With the proposed modulation scheme the secondary side devices become hard switched. However, the switched voltage depends on the turn on instant during the resonance, which maximum amplitude was demonstrated to be V_o. This makes it difficult to estimate the related losses in a real application. The worst possible scenario can be estimated by (29).

$$P_{sw,DCM} = 2F_{sw}\left((Q_{oss} + 2Q_{rr})V_F + 2Q_{oss}V_o\right) \qquad (29)$$

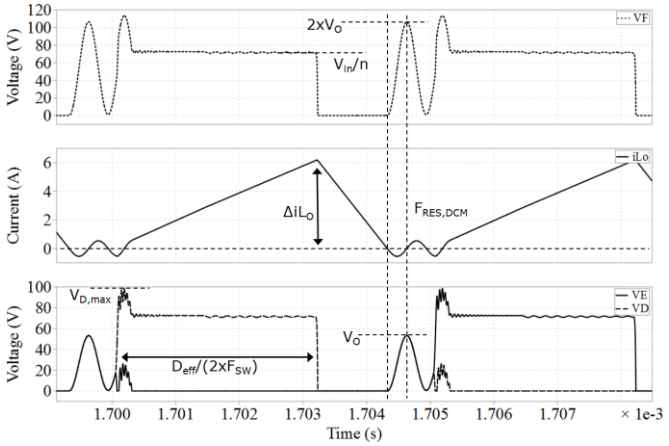


Fig. 8. Secondary side DCM overshoot where commutation occurs at the peak of L_o and C_{oss} resonance.

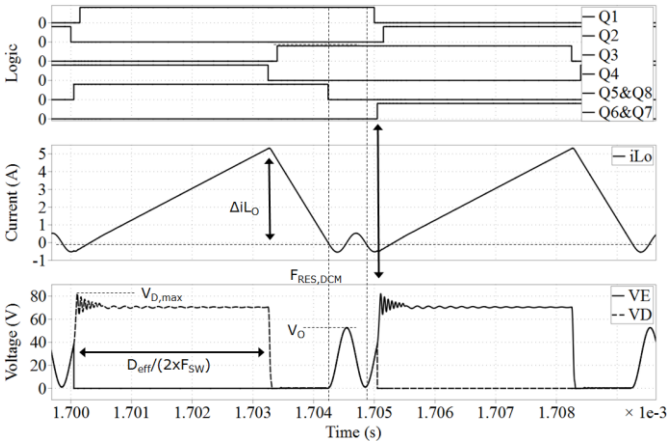


Fig. 9. Secondary side DCM overshoot where commutation occurs at the peak of L_o and C_{oss} resonance with the proposed modulation scheme applied.

IV. DCM PROPOSED MODULATION SCHEME

Fig. 10 shows the main driving signals and waveforms of a standard modulation scheme for PSFB in Tr-lead configuration [32] with external resonant inductance and clamping diodes in the primary side, as exemplified in Fig. 1. In Fig. 10, the converter operates at a load point where the output filter is working in CCM and where the secondary side SRs are enabled and driven with a standard CCM modulation. The so-called freewheeling time [t_3, t_5] is relatively long as it is the case for most practical designs with a wide input and/or output voltage range. Currents through L_r (iL_r) and through the transformer T_r (iT_r) differ due to the action of the clamping diodes D_9 and D_{10} diverting the L_r current after charging the secondary side rectifiers

Q_{oss} and Q_{rr} at the start and at the end of a power transfer ([t_1], [t_3], [t_7] and [t_{10}]).

Fig. 11 shows the main driving signals and waveforms of the proposed modulation scheme for the same converter in Fig. 1 while the output filter operates in DCM. In the example of Fig. 11 there is a single resonance period between the SR capacitance and L_o. In this scenario the stored voltage in C_{oss} is at its minimum value at the start of a new power transfer, which is the best possible case. However, the point within the resonance where the converter commutates varies depending on many factors (converter load, duty cycle, frequency of DCM resonance, etc.) that cannot be easily estimated or ensured by the controller. The solution we propose here is independent of the commutation point within the resonance, does not require additional measurements by the controller and can be tuned based on design parameters.

In the following we analyze the operation principle of the proposed DCM operation of the PSFB. Before the analysis some assumptions are made: 1) all diodes and switches are ideal; 2) all switches are MOSFETs with intrinsic anti-parallel body diode; 3) all capacitors and inductors are ideal; 4) C_1=C_2=C_3=C_4, C_5=C_6=C_7=C_8.

1) Mode 1 [t_2, t_3] [Fig. 12(a)] - D_{eff}

During this stage the power is being transferred from the primary to the secondary. A single secondary side rectification branch conducts while the complementary branch blocks the reflected voltage of the transformer.

The current through the external resonant inductance iL_r rises above the reflected primary side current of the transformer i_{Tr} due to the charge of the rectifier's Q_{oss} and Q_{rr} at the start of the power transfer (30)-(34). Thanks to the primary side clamping diodes, the additional energy stored in L_r is diverted and freewheels through Q_2 and D_{10} (35).

$$iL_r(t) = iL_r(t_2) + iL_{r,comm},\ t_2 < t < t_3 \quad (30)$$

$$iL_{r,comm} = \sqrt{\frac{2V_{in}}{n(L_r+L_{lkg})}(Q_{rr}+Q_{oss})} \quad (31)$$

$$\begin{cases} iL_r(t_2) = \frac{iL_{o,avg}-\frac{\Delta iL_o}{2}}{n} - \frac{D_{eff}V_{in}}{L_m 2F_{sw}}\ , CCM \\ iL_r(t_2) = iL_m(t_2) = -\frac{D_{eff}V_{in}}{L_m 2F_{sw}}\ ,\ DCM \end{cases} \quad (32)$$

$$iL_{Tr}(t) = \frac{iL_o(t)}{n} + \frac{iL_{r,comm}L_{lkg}}{(L_r+L_{lkg})}(1-\cos(t\omega_3)) + iL_m(t)\ ,\ t_2 < t < t_3 \quad (33)$$

$$\begin{cases} iL_o(t) = iL_o(t_2) + \frac{\left(\frac{V_{in}}{n}-V_o\right)}{L_o}t\ ,\ CCM \\ iL_o(t) = \frac{\left(\frac{V_{in}}{n}-V_o\right)}{L_o}t\ ,\ DCM \end{cases},\ t_2 < t < t_4 \quad (34)$$

$$iD_{10}(t) = iL_r(t) - iL_{Tr}(t),\ t_2 < t < t_3 \quad (35)$$

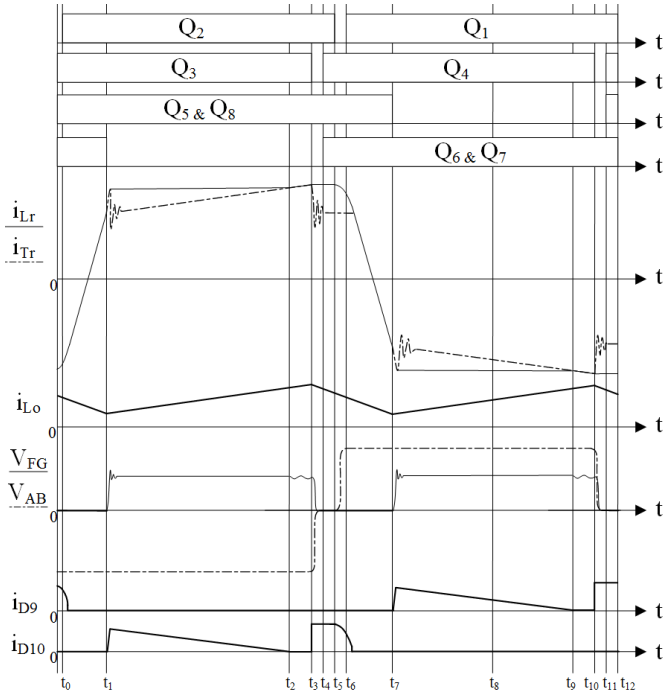


Fig. 10. Main signals in the circuit for the proposed forward operation of PSFB with output filter working in CCM

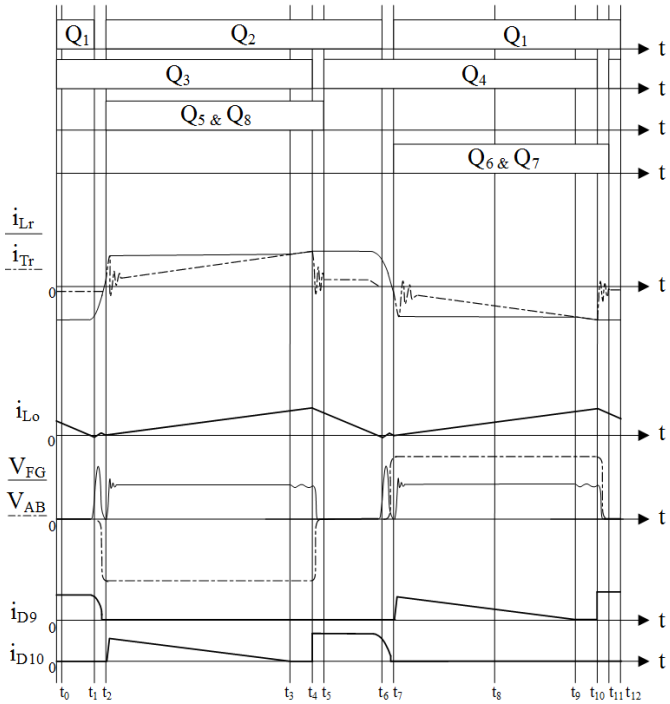


Fig. 11. Main signals in the circuit for the proposed forward operation of PSFB with the output filter working in DCM.

2) Mode 2 [t_3, t_4] [Fig. 12(b)] - D_{eff}

At t_3 the current through the external resonant inductance (iL_r) and through the primary side of transformer (iT_r) becomes equal and D_{10} stops conducting (36). The voltage at the node C (V_C) is no longer clamped to one of the primary side supply rails, as could be appreciated by the secondary reflected voltage

oscillations (V_F). Notice, however, that D_{10} does not necessarily stop conducting during the interval [t_2, t_4], it depends on the converter duty, peak value of iL_r and the slopes of iL_r and iT_r [25].

$$iL_r(t) = iL_{Tr}(t) = \frac{iL_o(t)}{n} + iL_m(t),\ t_3 < t < t_4 \quad (36)$$

The current through the output inductor (L_o) keeps rising, as so does the reflected primary current through the transformer. The external resonance inductor current iL_r equals that of the transformer and rises as well: L_r and the reflected output filter impedance effectively form a voltage divider, but since the reflected output impedance is much larger than L_r, as exemplified in (37)-(38), this effect can be normally neglected, especially in step down converters.

$$L_{o''} = L_o n^2 \quad (37)$$

$$N_P > N_S \xrightarrow{yields} L_{o''} \gg L_r \xrightarrow{yields} V_{in} = V_{BC} + V_{CA} \approx V_{BC} \quad (38)$$

3) Mode 3 [t_4, t_6] [Fig. 12(c), Fig. 12(f)] - $D_{freewheel}$

Q_3 turns off at t_4 forcing the current flowing through L_r and L_o to discharge C_4 and to charge C_3. Since V_{AB} decreases towards zero, so does the reflected transformer voltage V_{DE} forcing as well the discharge of Q_6 and Q_7 output capacitances (C_6 and C_7) on the secondary side. The discharging of C_6 and C_7 distributes iL_o between the secondary side rectification branches, not necessarily and, normally, not equally. Because part of iL_o does not pass through the secondary side of the transformer after this redistribution, the primary reflected iT_r decreases proportionally (39)-(40). However, iL_r remains nearly constant due to the action of D_{10} (41)-(42).

$$iL_{Tr}(t) = iL_{Tr}(t_4) - iL_{lkg,OFF}\ ,\ t_4 < t < t_6 \quad (39)$$

$$iL_{lkg,OFF} = \sqrt{\frac{V_{in}}{nL_{lkg}} 2Q_{oss}} \quad (40)$$

$$iL_r(t) \approx iL_r(t_4),\ t_4 < t < t_6 \quad (41)$$

$$iD_{10}(t) = iL_r(t) - iL_{Tr}(t),\ t_2 < t < t_3 \quad (42)$$

At some point during this interval C_4 is fully discharged and C_3 fully charged. The intrinsic body diode of Q_4 becomes then forward biased and carries all iT_r. Notice that the intrinsic body diode of Q_4 does not necessarily conduct before t_5, especially at light load conditions where the available energy for the transition is low, and most likely the case in Fig. 11 scenario where the output filter works in DCM. At t_5 Q_4 turns on and the channel of the device carries all the current iT_r.

On the secondary side C_6 and C_7 have become equally discharged and the intrinsic body diode of all the rectifier transistors conduct part of the output current, effectively shorting the transformer.

During this stage, the so-called freewheeling, the primary current recirculates through the two lower HV bridge devices (the two upper in the alternate polarity sequence) without actually transferring energy to the output of the converter. The secondary side devices continue sharing the output current (43)-(44), although most of it flows through D_5 and D_8.

$$iL_o(t) = iL_o(t_4) - \frac{\left(\frac{V_{in}}{n} - V_o\right)}{L_o} t\ ,\ t_4 < t < t_6 \quad (43)$$

$$iL_o(t_4) = iL_{o,pk} \quad (44)$$

In Fig. 11 Q_5 and Q_8 turn off at the start of the freewheeling stage. This simple approach, despite not being optimum in terms of efficiency, does not require the estimation or measurement of iL_o zero crossing and prevents the above mentioned forced CCM overshoot. Some other common alternative modulation schemes include [17]:

- Delaying the turn off of the SRs after the end of a power transfer by an estimated falling time of L_o current to zero.
- Sensing the current through L_o or through the SRs by the controller that turns off at zero crossing, perfectly mimicking the behavior of an ideal diode.

Near t_6, iL_o crosses zero and starts to flow back charging up all the secondary rectifiers output capacitance. Since the devices output capacitances are equal, charge and voltage will be equally distributed among all of them.

4) Mode 4 [t_6, t_7] [Fig. 12(g), Fig. 12(i)] - D_{loss}

Q_2 turns off at t_6 and the current flowing through L_r plus L_{lkg} charges C_2 and discharges C_1.

The resonance between L_o and the output capacitance of the SRs continues as could be observed in the V_F waveform in Fig. 11. The frequency of the oscillation depends on the value of those two components (45), relatively slow in comparison to the commutation overshoot phenomena. Due to this low frequency, the dampening effects of the circuit impedances are less noticeable.

$$iL_o(t) = \sqrt{\frac{4Q_{oss}V_o}{L_o}}(1 - \cos(t\omega_2))\ ,\ t_6 < t < t_7 \quad (45)$$

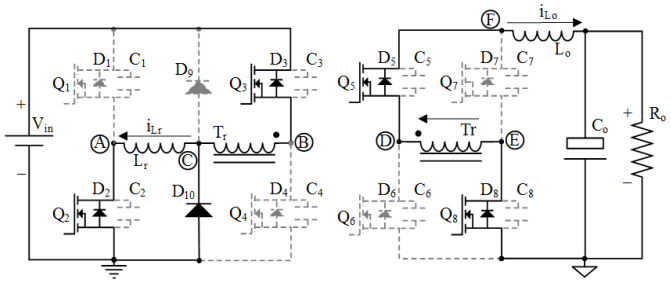
At certain point during this mode C_2 could become fully charged and C_1 fully discharged. If this occurs, the intrinsic body diode of Q_1 starts conducting the current through the external resonant inductor iL_r. Near t_7 Q_1 is turned on, ideally in ZVS conditions if there was enough energy stored in L_r prior to the transition. iL_r reverses polarity (46)-(48) and, since there is near zero reflected current, right after crossing the magnetizing current, the voltage starts to build up on the primary side of the transformer and, at the same time, on its secondary side.

$$iL_r(t) \approx iL_r(t_4) - \frac{V_{in}}{(L_r + L_{lkg})} t\ ,\ t_6 < t < t_7 \quad (46)$$

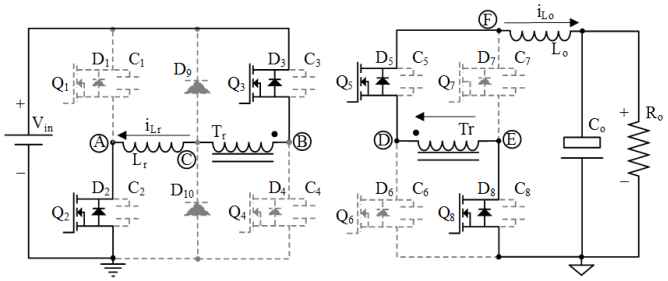
$$iL_{Tr}(t) = iL_r(t)\ ,\ t_x < t < t_7\ with\ t_6 < t_x \quad (47)$$

$$iD_{10}(t) = 0\ ,\ t_x < t \quad (48)$$

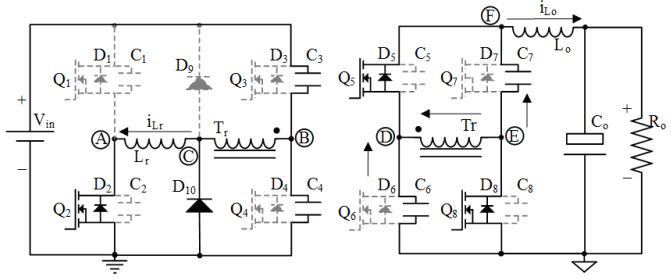
In Fig. 12(i), before the proposed solution is applied, the secondary side voltage builds up on top of the already precharged capacitances C_5 and C_8 (Fig. 8). However, in Fig. 12(i'), with the proposed modulation scheme, around t_7, while the voltage of transformer builds up, the secondary side rectifying branch about to conduct is turned on (Fig. 9). In this scenario Q_6 and Q_7 are hard switched and the energy of their output capacitances C_6 and C_7 is dissipated within these two devices. Subsequently V_F equals to the rising reflected voltage of the transformer V_{DE}.



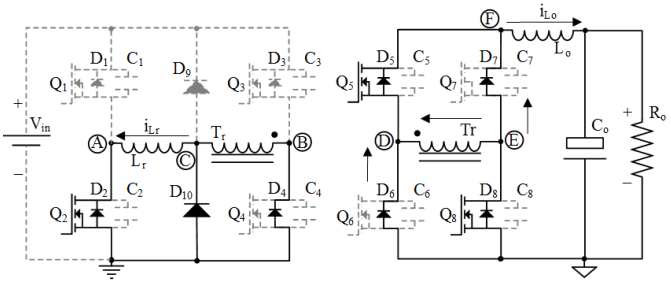
(a) [t_2, t_3]



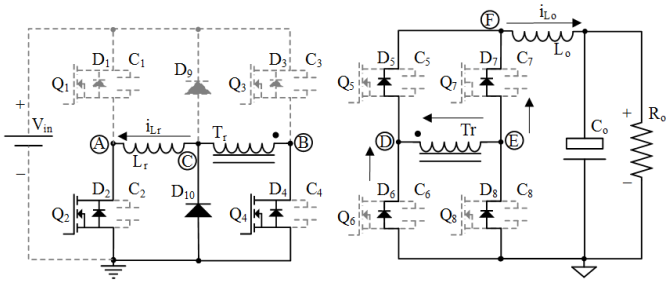
(b) [t_3,t_4]



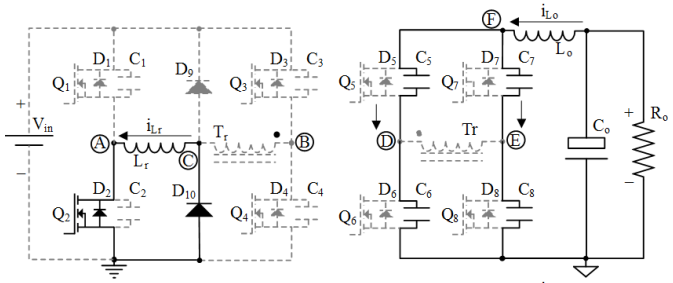
(c) [t_4]



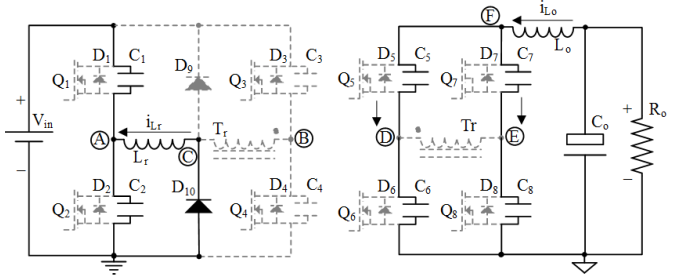
(d) [t_4, t_5]



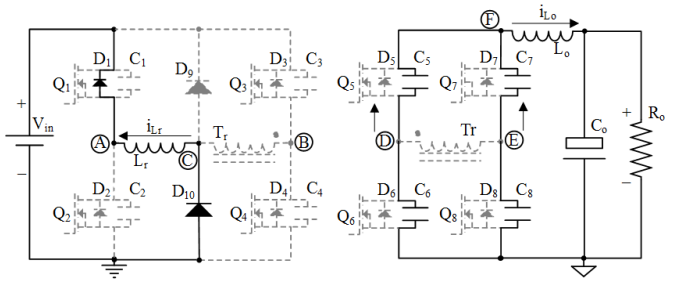
(e) [t_5]



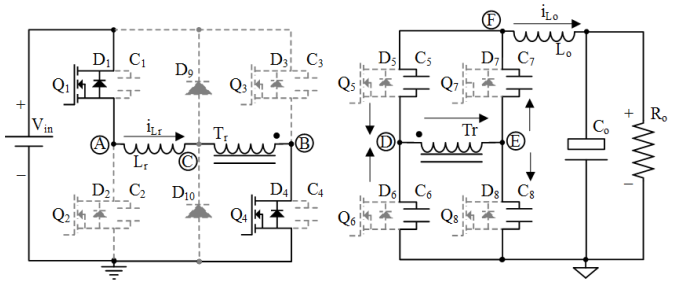
(f) [t_6]



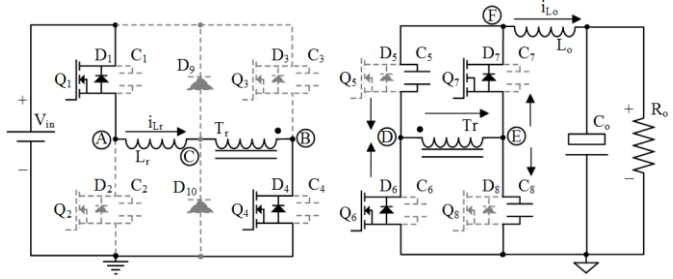
(g) [t_6, t_7]



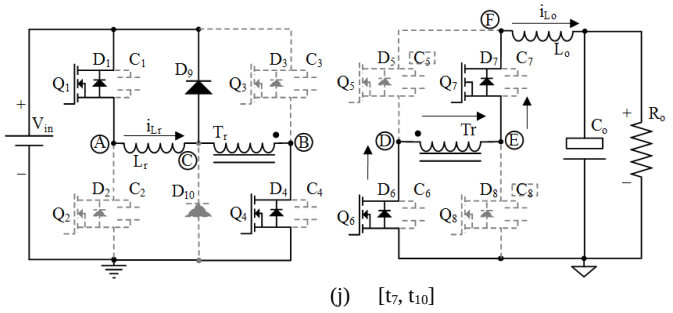
(h) [t_6, t_7]



(i) [t_7]



(i') [t_7] alternative



(j) [t_7, t_{10}]

Fig. 12. Operation modes for the proposed forward operation of PSFB in DCM

It is crucial for the effectivity of the solution that the switching on point of Q_6 and Q_7 falls within the building up time of the reflected voltage. The time constant of the rising time depends on L_r, leakage of transformer, stray inductances and output capacitance of the secondary side rectifying devices. The rising time can be estimated by (49) where C_{oss} accounts for C_5 and C_8.

$$T_{rise} = \pi\sqrt{(L_r + L_{lkg})2C_{oss}} \tag{49}$$

5) Mode 5 [t_7, t_{10}] [Fig. 12(j)] - D_{eff}

At some point after t_7 the output capacitances C_5 and C_8 are fully charged up to the nominal blocking voltage, and Q_6 and Q_7 conduct all the secondary side current in a new power transfer stage. Afterwards all the detailed sequence repeats but in the alternate polarity. On the primary side, like in mode 1, the difference between currents through L_r and the transformer flows through one of the clamping diodes: D_9.

A. INFLUENCE OF TIMING

Fig. 13 shows the effect of turning on the SRs too early while operating the converter in DCM: before the transformer voltage starts building up. The current through Lo grows negative (flowing against the rectifiers) prior to the start of a power transfer. Once the power transfer starts, the additional stored energy induces an overshoot potentially higher than the original scenario in Fig. 8, as more energy could have been unintentionally stored in L_o.

A late activation of the SR devices does not help either in the reduction of the maximum peak voltage of the drain overshoot. Fig. 13 also shows the effect of turning on short after that the transformer secondary reflected voltage has built up while the output filter works in DCM. The low frequency oscillation is clamped, but only after the prior high drain voltage overshoot.

The turn on instant for the SR ($t_{sr,on}$) can be referenced to the turn off instant of the primary side lagging leg ($t_{lagg,off}$) (50). The start of the voltage build up (T_{rise}) is delayed by the time it takes iL_r to reverse polarity, which can be calculated by (51)-(54). After this delay $T_{dly,on}$ the SR turn on instant should happen within the T_{rise} interval for an effective clamping of the DCM overshoot (Fig. 14). The minimum turn on time $t_{sr,on,min}$ and the maximum turn on time $t_{sr,on,max}$ for an effective reduction of the overshoot can be derived from the previous equations and calculated by (55)-(56).

$$(t_{lagg,off} + T_{dly,on}) < t_{sr,on} < (t_{lagg,off} + T_{dly,on} + T_{rise}) \tag{50}$$

$$T_{dly,on} = \frac{(iL_r(t_{lagg,off}) - iL_m(t_{lagg,off}))(L_r + L_{lkg})}{V_{in}} \tag{51}$$

$$iL_r(t_{lagg,off}) \approx \frac{iL_{o,pk}}{n} + iL_{m,pk} \tag{52}$$

$$iL_m(t_{lagg,off}) = iL_{m,pk} = \frac{V_{in}}{L_m}\frac{iL_{o,pk}L_o}{(V_{in} - V_o)} \tag{53}$$

$$iL_{o,pk} = \sqrt{\frac{iL_{o,avg}V_o(V_{in} - V_o)}{F_{sw}V_{in}L_o}} \tag{54}$$

$$t_{sr,on,min} = t_{lagg,off} + \sqrt{\frac{iL_{o,avg}V_o(V_{in} - V_o)}{F_{sw}V_{in}L_o}}\frac{(L_r + L_{lkg})}{V_{in}n} \tag{55}$$

$$t_{sr,on,max} = t_{lagg,off} + \sqrt{\frac{iL_{o,avg}V_o(V_{in} - V_o)}{F_{sw}V_{in}L_o}}\frac{(L_r + L_{lkg})}{V_{in}n} + \pi\sqrt{(L_r + L_{lkg})2C_{oss}} \tag{56}$$

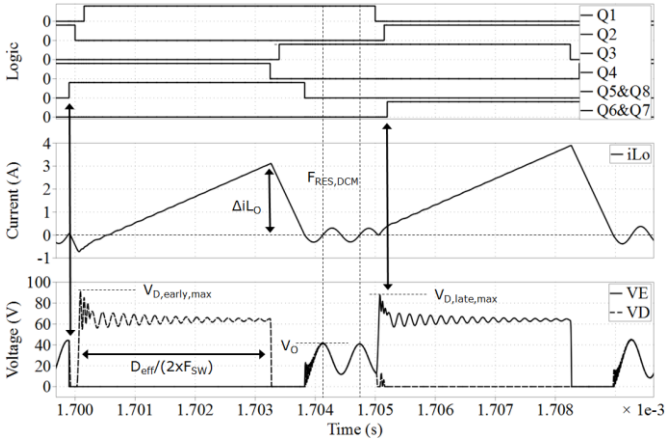


Fig. 13. Secondary side DCM overshoot with the proposed modulation scheme. SR has been turned on too early for the pulse in the left side. SR has been turned on too late for the pulse in the right side.

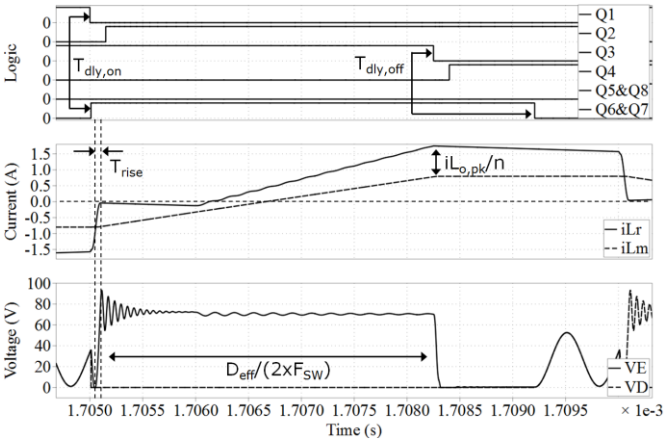


Fig. 14. Secondary side DCM overshoot with the proposed modulation scheme. SR has been turned on right at the start of the rising time T_{rise}.

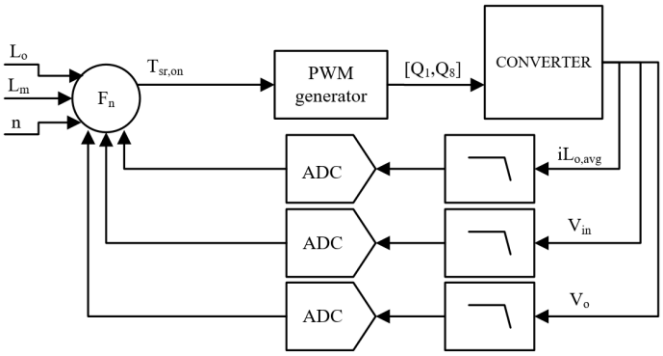


Fig. 15. Simplified control blocks for a possible implementations of $T_{sr,on}$ calculation in a PSFB controller.

Fig. 15 shows a proposal for the implementation of $T_{sr,on}$ in a controller. The voltages and currents through the converter are measurements typically available. Although, depending on the application, they can be considered constant ($V_{in,nominal}$, $V_{o,nominal}$) or estimated out from other of the measurements ($iL_{o,avg} \approx |iT_{r,avg}|n$). The rest of parameters, including converter inductances and turns ratio can be programmed as constants. The impact on the proposed implementation of the tolerances in the values of the converter's inductances and capacitances can be estimated with (55)-(56).

V.EXPERIMENTAL RESULTS

A 3300 W PSFB DC/DC converter (Fig. 16) was designed with the specifications given in Table II and built to test the proposed solutions and guidelines presented in this work. Table III and Table IV summarize the main components of the converter. The control was implemented with XMC™ 4200 ARM® Cortex®-M4 microcontroller from Infineon Technologies AG.

Fig. 16 Prototype of the 3300 W PSFB converter.

The output filter inductor L_o was designed for an optimal overall efficiency of the converter at 50 % load point while fulfilling space constraints, high power density and maintaining the output voltage ripple within specifications. Fig. 17 shows a summary of the estimation of losses for the output inductor within the load range of the converter. Table V is a summary of the estimation of losses for the main components of the converter. The distribution was estimated out of the measured efficiency of the real converter, thermographic captures, data from components manufacturer, finite element analysis (FEM), and circuit and numeric simulations.

Observe in Fig. 17 that the current ripple through the output inductor changes with the load due to the influence of the DC bias on the permeability of the material. The transition between CCM and DCM occurs at the point where the two lines ΔiL_o and iL_o cross each other, around a load of 8 A. The DCM threshold is relatively high, about 13 % of the load, because of the small value of the output inductance. Nevertheless, the controller of the prototype was adjusted to change between operating modes at 12 A (18 %) of load to ensure safe operation in all conditions (e.g. load jumps) and avoid risk of forced CCM overshoot. Thereafter DCM overshoot is likely to occur and had to be prevented by the proposed modulation scheme.

TABLE II
KEY PARAMETERS OF PROTOTYPE

Parameter	Value
Nominal input voltage	400 V
Input voltage range	360 V - 410 V
Nominal output voltage	54.5 V
Output voltage range	43 V - 60 V
Maximum output power	3300 W
Maximum output current	85 A
Switching frequency	100 kHz
Height of the converter	1 U (44.4 mm)
Transformer turns ratio (Np : Ns)	21:4
Magnetizing inductance (Lm)	750 µH
Resonant inductance (Lr)	11 µH
Output choke inductance (Lo)	9.8 µH

TABLE III
SI MOSFETS AND DIODES

	IPL60R075CFD7	BSC093N15NS5	IDP08E65D1
V_{ds}	600 V	150 V	650 V
$R_{DS,on,max}$	75 mΩ @ 25 °C	9.3 mΩ @ 25 °C	
$C_{oss(er)}$	96 pF	604 pF	
V_f	1 V	0.88 V	1.35 V
Q_{rr}	570 nC	58 nC	200 nC
Q_g	67 nC	33 nC	
Units	8 pieces	16 pieces	2 pieces

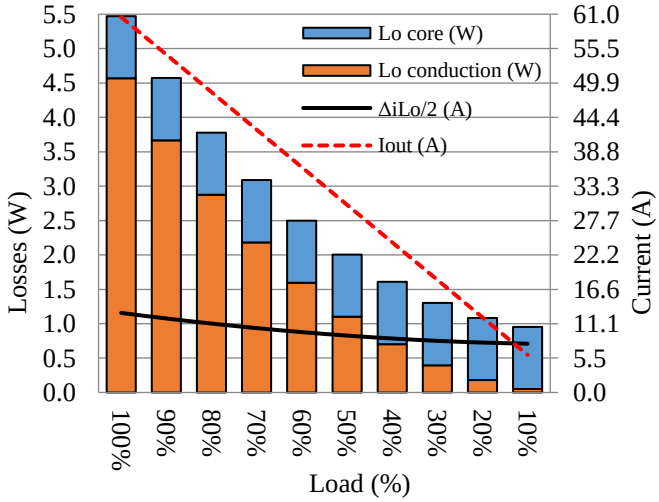


Fig. 17. Output inductor distribution of losses of the 3300 W PSFB prototype.

TABLE IV
MAGNETIC CORE SELECTION

	Core	Material	Manufacturer	Turns
Transformer	PQI 35/28	DMR95	DMEGC	21:4
L_r	PQI 35/28	DMR95	DMEGC	6
L_o	Toroid	HP 60 µ	Chang Sung	9

TABLE V
3300 W PSFB LOSSES BREAKDOWN

Loss contribution	100% power	50% power	20% power
Auxiliary circuitry	1.02 W	1.02 W	1.02 W
Fan	4.91 W	0.64 W	0.64 W
Transformer	30.17 W	10.95 W	5.45 W
Lr	2.98 W	1.00 W	0.26 W
Lo	5.47 W	2.01 W	1.08 W
Primary bridge	19.65 W	5.91 W	2.77 W
Secondary switching	7.30 W	6.38 W	5.81 W
Secondary conduction	11.32 W	2.53 W	0.42 W
Secondary driving	0.84 W	0.84 W	0.84 W
Clamping diodes	1.89 W	2.32 W	2.52 W
Capacitors	0.41 W	0.37 W	0.36 W
PCB conduction	7.60 W	1.92 W	0.32 W

A. WAVEFORMS

1) COMMUTATION OVERSHOOT

Since L_{lkg} and L_{stray} in the prototype are relatively small inductances, the commutation overshoot has high resonant frequency, low energy and dampens quickly. Fig. 18 shows a capture of the SR drain voltage overshoot at full load. Observe that the peak voltage is well below the rated limit for the 150 V of the secondary side devices in this design (limit would be 120 V at a standard 80 % rating). Devices with a maximum 120 V blocking voltage would be preferred on the secondary side since the improved Q_{oss} and Q_{rr} characteristics for the same $R_{DS,on}$ would further reduce commutation overshoot and losses [16] and would be still within their rated limits (96 V at a 80% rating). However, at the time of this work there were no available devices within that voltage class that could be used.

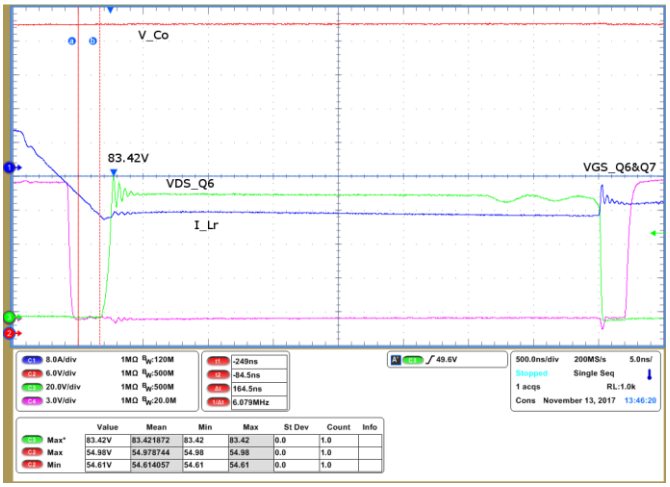


Fig. 18. SR overshoot at full load.

Besides, a weak snubber could be added to further reduce the peak voltage and/or improve the dampening of the commutation resonance without much of an impact on the losses.

2) DCM OVERSHOOT

In Fig. 19, during a load jump, the output filter of the converter goes into DCM during a few switching cycles whereas the controller did not apply the proposed DCM modulation scheme. It is worth to mention the difference between the drain voltage overshoot of the first three pulses compared to the last one: of lower frequency and higher energy, as caused by the resonance between Lo and the output capacitance of the SRs with L_o much larger than the leakage inductance of the transformer or other stray inductances in the commutation path.

Fig. 20 shows a deeper level of DCM operation of the output filter at very light load condition (no load start-up). A full resonance period is followed by the worst possible DCM overshoot scenario where a power transfer starts at the peak of charge of the output capacitances. It can be observed how the precharged energy stacks on top of the transformer reflected voltage.

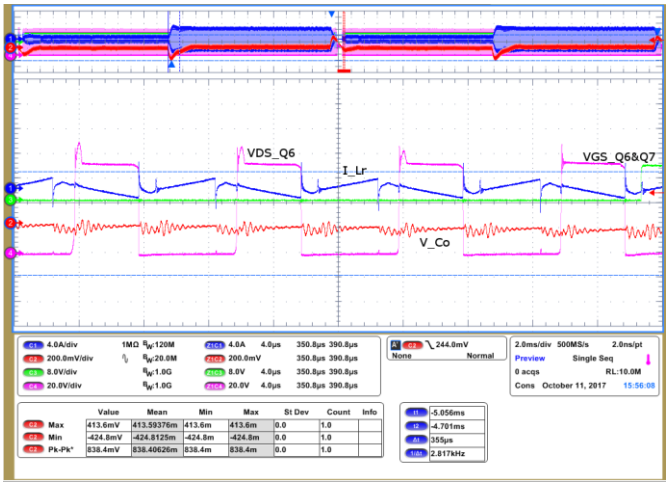


Fig. 19. SR DCM overshoot in a load jump without the proposed modulation scheme.

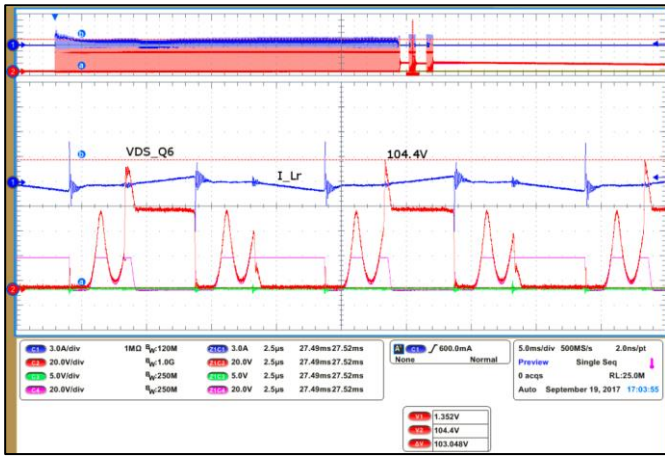


Fig. 20. SR drain voltage DCM overshoot at no load conditions without the proposed modulation scheme.

Fig. 21 shows a similar scenario to those in Fig. 19 and Fig. 20, but this time applying the proposed DCM modulation scheme. DCM resonance is visible before the transformer secondary side reflected voltage builds up, however, the drain voltage overshoot resembles that of Fig. 18 and it is much lower than the one in Fig. 19 and Fig. 20.These results confirm the analysis in section III.

3) INFLUENCE OF TIMING

Fig. 22 shows the effect of turning on the SRs too early, before the transformer voltage starts building up, while operating the converter in DCM.

Fig. 23 shows the effect of turning on short after that the transformer secondary reflected voltage has built up, while the output filter works in DCM. The low frequency oscillation is clamped, but only after the prior high drain voltage overshoot.

The results in Fig. 22 and Fig. 23 corroborate the analysis in section IV. A. The estimated T_{rise} for the prototype is approximately 740 ns, which can also be observed in Fig. 22.

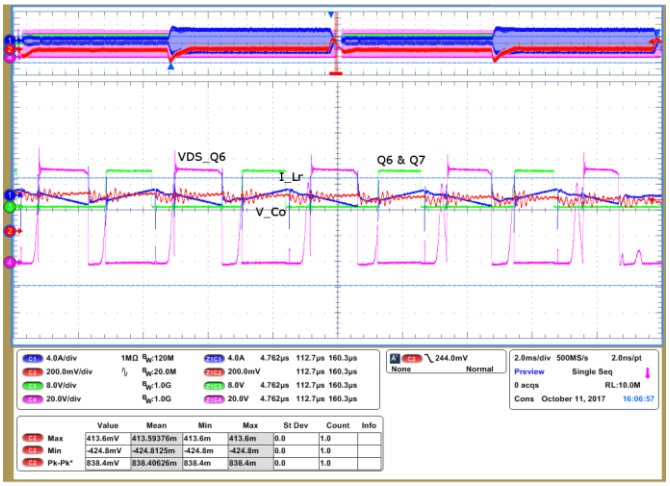


Fig. 21. SR drain voltage DCM overshoot in a load jump with the proposed modulation scheme.

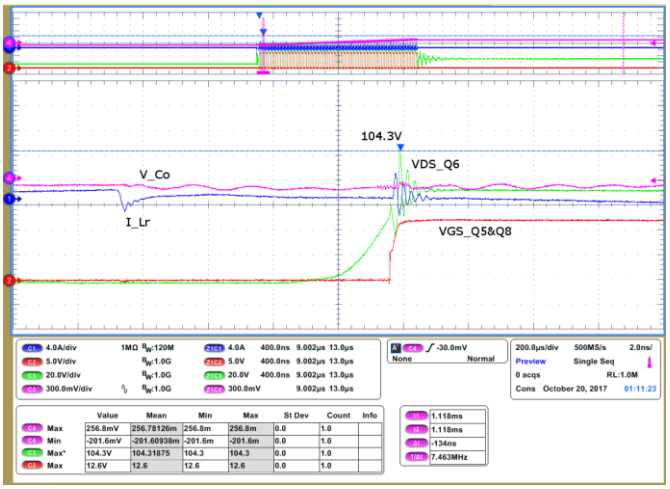


Fig. 22. SR drain voltage DCM overshoot when the devices turn on too early.

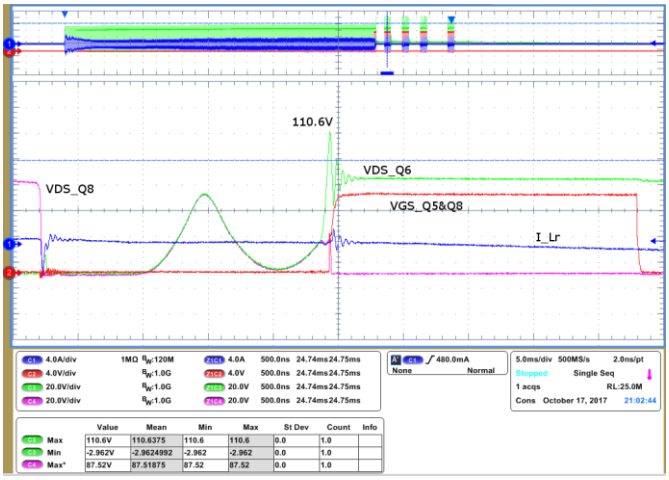


Fig. 23. SR drain voltage DCM overshoot when the device is activated too late.

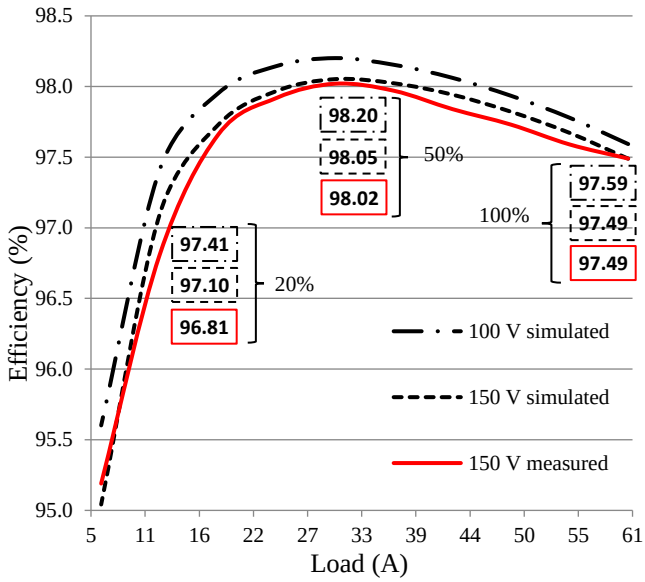


Fig. 24. Overall efficiency of the 3300 W PSFB converter. Auxiliary bias and fan were included in the measurements. Experimental and simulated results for the 150 V devices. Simulated results for the 100 V devices.

B. EFFICIENCY

The efficiency of the 3300 W PSFB prototype was measured at nominal input and output voltages along all the load range and plotted in Fig. 24. The experimental results are plotted together with simulated efficiencies for the 150 V devices and the 100 V devices of similar $R_{DS,on}$. The improved FoM of the 100 V technology has a noticeable impact along all the load range of the converter.

VI. CONCLUSION

One of the main disadvantages of the PSFB topology in comparison to other resonant topologies is the higher blocking voltage required for the SRs. This is especially detrimental in wide range operation converters and further aggravated by the SRs drain voltage overshoot. Unlike other resonant topologies, the

inductor at the output of the PSFB effectively decouples the capacitor bank from the rectification stage, which otherwise becomes a strong lossless snubber.

Traditionally the main criterion for the selection of the external resonant inductance has been the available energy for the ZVS of the HV primary side devices and the loss of duty cycle at full load. However, the analysis in this work demonstrates that, from the point of view of the overall performance of the system, the impact on the secondary side drain voltage overshoot and the reduction of the secondary side switching losses has to be taken into account for the dimensioning of the transformer's turns ratio *n* and the external inductance L_r.

In this work the main causes for the secondary side rectifiers drain voltage overshoot in PWM converters, specifically in PSFB converters, have been analyzed. Design guidelines and solutions for each of the scenarios, including a novel modulation scheme for the operation of PSFB with the output filter operating in DCM have been proposed. The proposed solution is based on an active rectification scheme switching on the devices prior or during the buildup time of the transformer secondary reflected voltage.

The proposed strategies enable the design of DCDC PSFB converters targeting high efficiency without penalties in reliability, complexity or cost. Lower blocking voltage requirements for the rectification devices improve their Figure of Merit, potentially reducing their related losses and increasing the overall efficiency of the converter.

A high efficiency DCDC PSFB converter prototype of 3300 W was designed and built to demonstrate the feasibility of the proposed solutions. The drain voltage overshoot has been proven to remain well within standard rated limits in all working conditions of the converter. The prototype achieved a peak efficiency of 98.12 % at nominal input and output voltages and 50 % of load. Overall, this work demonstrates that the PSFB can be a competitive alternative when building highly efficient and cost-competitive DC/DC converters.

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Synchronous rectifiers drain voltage overshoot reduction in PSFB converters

Dear Editor,

We would like to thank you for processing our contribution. We sincerely thank the editors and reviewers for the time and effort spent in reading and reviewing our manuscript and for the insightful comments. Below is a detailed response to each review comment. We hope that we correctly understood the implication of each comment and that our replies are appropriate and sufficient. Following their comments, we have introduced the suggested changes in the content and structure of the document. For the sake of clarity, we have highlighted in red only the major additions and changes to the previous version of the manuscript.

Sincerely yours,

Manuel Escudero Rodriguez on behalf of the authors

CO-EDITOR IN CHIEF COMMENTS

Mandatory changes are requested.

We appreciate the inputs from the reviewers and the fact that the highlighted the importance and potential usefulness of reducing the secondary side overshoot in PSFB converters. We hope to have covered all their concerns in the improved new version of the document.

Following are point-by-point answers to their comments (the reviewer's comments are in **bold**).

ASSOCIATE EDITOR COMMENTS

The paper needs some additions and should be reorganized considerably before being published.

We deeply appreciate the feedback to our work. Following the suggestions, we have made a substantial effort improving the content and the structure of the document. Some of the sections have been partially rewritten or rearranged with the purpose of improving the flow of the analysis and to facilitate the understanding of the manuscript to the readers.

REVIEWER 1 COMMENTS

This paper analyzes three mechanisms for rectifier voltage overshoot in phase-shifted full-bridge dc-dc converters, and proposes a new control scheme to address one of these mechanisms.

In the proposed scheme, applicable in DCM operation of the converter, the rectifier transistors are switched during the voltage commutation of the transformer, utilizing the DCM resonance energy to discharge the rectifier transistor output capacitances.

The revised manuscript is richer in technical content and addresses many of this reviewer's concerns. The authors' efforts in improving the manuscript are appreciated,

Thank you for emphasizing the value of our work. We hope to have covered all the remaining concerns in the improved new version of the document.

Following are point by point answers to your comments (the reviewer's comments are in **bold**).

However, one remaining (and important) concern is the sensitivity of the approach to timing. The authors do show an approach to computing the timing (Fig. 15), but this approach depends on the converter's component values (inductances, transformer turns ratio), which can themselves have variations (for e.g.: part-to-part manufacturing variations and tolerances). Hence, in the absence of any feedback mechanism to correct for such variations, the robustness of this timing approach cannot be guaranteed.

We acknowledge the reviewers concern. The turn on instant for the SR ($t_{sr,on}$) can be referenced to the turn off instant of the primary side lagging leg ($t_{lagg,off}$) (55). The start of the voltage build up (T_{rise}) is delayed by the time it takes iL_r to reverse polarity, which can be calculated by (56)-(59). After this delay $T_{dly,on}$ the SR turn on instant should happen within the T_{rise} interval for an effective clamping of the DCM overshoot.

$$T_{rise} = \pi\sqrt{(L_r + L_{lkg})2C_{oss}} \tag{54}$$

$$(t_{lagg,off} + T_{dly,on}) < t_{sr,on} < (t_{lagg,off} + T_{dly,on} + T_{rise}) \tag{55}$$

$$T_{dly,on} = \frac{(iL_r(t_{lagg,off}) - iL_m(t_{lagg,off}))(L_r + L_{lkg})}{V_{in}} \tag{56}$$

$$iL_r(t_{lagg,off}) \approx \frac{iL_{o,pk}}{n} + iL_{m,pk} \tag{57}$$

$$iL_m(t_{lagg,off}) = iL_{m,pk} = \frac{V_{in}}{L_m}\frac{iL_{o,pk}L_o}{(V_{in} - V_o)} \tag{58}$$

$$iL_{o,pk} = \sqrt{\frac{iL_{o,avg}V_o(V_{in}-V_o)}{F_{sw}V_{in}L_o}} \tag{59}$$

In summary, the secondary side rectifiers should be turned on after the $t_{sr,on,min}$ and before $t_{sr,on,max}$ (*a*)-(*c*). From the equations it is possible to estimate the impact of the tolerances in L_o, L_r, L_{lkg} and C_{oss}.

$$T_{dly,on} = \sqrt{\frac{iL_{o,avg}V_o(V_{in}-V_o)}{F_{sw}V_{in}L_o}}\frac{(L_r+L_{lkg})}{V_{in}n} \tag{a}$$

$$t_{sr,on,min} = t_{lagg,off} + \sqrt{\frac{iL_{o,avg}V_o(V_{in}-V_o)}{F_{sw}V_{in}L_o}}\frac{(L_r+L_{lkg})}{V_{in}n} \tag{b}$$

$$t_{sr,on,max} = t_{lagg,off} + \sqrt{\frac{iL_{o,avg}V_o(V_{in}-V_o)}{F_{sw}V_{in}L_o}}\frac{(L_r+L_{lkg})}{V_{in}n} + \pi\sqrt{(L_r + L_{lkg})2C_{oss}} \tag{c}$$

The A_L tolerance of the toroidal cores utilized for the realization of the output inductor is ±8 % in accordance to the manufacturer's datasheet. Considering the worst case deviation of 8 %, with all other values constant, the turn on window [$t_{sr,on,min}$, $t_{sr,on,max}$] is approximately delayed a 4 % of the nominal (the $T_{dly,on}$ is proportional to the square root of the inverse of L_o).

For the ferrite cores utilized for the realization of the resonant inductance, the tolerance of the initial permeability is ±25 % in accordance to the manufacturer's datasheet. The resonant inductance nominal value is 11µH which is realized with 6 turns. The effective length of the core l_e is 64.9 mm and the effective area A_e is 173.5 mm in accordance to the core set datasheet. The resulting gap is approximately 694 µm. This results in the effective permeability and the tolerance being dominated by the gap length, which makes it possible to manufacture a more repeatable value of inductance.

$$L_r = \frac{N^2\mu_e\mu_0A_e}{l_e} \xrightarrow{\text{yields}} \mu_e = 92.21 \tag{d}$$

$$\mu_e = \frac{\mu_i}{1+\mu_i\left(\frac{l_g}{l_i}\right)} \tag{e}$$

We can consider for the analysis a 10 % deviation in the resonant inductance value. With all other values constant the turn on window [$t_{sr,on,min}$, $t_{sr,on,max}$] is approximately delayed a 10 % and its length extended approximately 5 % of the nominal. The leakage of transformer L_{lkg} is much smaller than the external resonant inductance L_r. L_{lkg} is in the order of 0.5 µH whereas the nominal value of L_r is 11 µH. A 10 % deviation in L_{lkg} would have the same impact than a 0.45 % deviation in L_r.

In relation to the output capacitance of the secondary side rectifiers, we do not have data for the tolerances. From the typical 604 pF and maximum 803 pF values in the manufacturer's datasheet we can estimate a 33 % tolerance. We do not have statistical deviation data for the C_{oss}, therefore we cannot estimate the most probable scenario. A worst case would be all the capacitances deviated to their maximum. Consequently, we could expect a maximum deviation of 15 % in the duration of the turn on window (rise time is proportional to the square root of C_{oss}).

All the other values in the equations can be directly measured by the controller. Considering the worst case for all parameters deviation, the turn on window could be deviated, in this example, up to a 14.45 % and extended (or shrank) up to a 20 %. A ±15 % window around the nominal should be still within valid turn on times. For increased robustness there exists the possibility of trimming the nominal turn on time during production to account for the tolerances.

The authors would prefer to exclude this long analysis from the final version of the paper, which is already over-length. We have included an estimation of the Trise for the prototype in the experimental results section.

> *"The results in Fig. 22 and Fig. 23 corroborate the analysis in section IV. A. The estimated Trise for the prototype is approximately 740 ns, which can also be observed in Fig. 22."*

Moreover, we have included the two equations for the estimation of the minimum and maximum turn on times, which might be useful to make more obvious the impact of the component values and their deviations.

"The minimum turn on time $t_{sr,on,min}$ and the maximum turn on time $t_{sr,on,max}$ for an effective reduction of the overshoot can be derived from the previous equations and calculated by (60)-(61).

$$\left(t_{lagg,off} + T_{dly,on}\right) < t_{sr,on} < \left(t_{lagg,off} + T_{dly,on} + T_{rise}\right) \quad (55)$$

$$T_{dly,on} = \frac{\left(iL_r(t_{lagg,off}) - iL_m(t_{lagg,off})\right)(L_r + L_{lkg})}{V_{in}} \quad (56)$$

$$iL_r\left(t_{lagg,off}\right) \approx \frac{iL_{o,pk}}{n} + iL_{m,pk} \quad (57)$$

$$iL_m\left(t_{lagg,off}\right) = iL_{m,pk} = \frac{V_{in}}{L_m}\frac{iL_{o,pk}L_o}{(V_{in} - V_o)} \quad (58)$$

$$iL_{o,pk} = \sqrt{\frac{iL_{o,avg}V_o(V_{in} - V_o)}{F_{sw}V_{in}L_o}} \quad (59)$$

$$t_{sr,on,min} = t_{lagg,off} + \sqrt{\frac{iL_{o,avg}V_o(V_{in} - V_o)}{F_{sw}V_{in}L_o}}\frac{(L_r + L_{lkg})}{V_{in}n} \quad (60)$$

$$t_{sr,on,max} = t_{lagg,off} + \sqrt{\frac{iL_{o,avg}V_o(V_{in} - V_o)}{F_{sw}V_{in}L_o}}\frac{(L_r + L_{lkg})}{V_{in}n} + \pi\sqrt{(L_r + L_{lkg})2C_{oss}} \quad (61)$$

Fig. 15 shows a proposal for the implementation of $T_{sr,on}$ in a controller. The voltages and currents through the converter are measurements typically available. Although, depending on the application, they can be considered constant ($V_{in,nominal}$, $V_{o,nominal}$) or estimated out from other of the measurements ($iL_{o,avg} \approx |iT_{r,avg}|n$). The rest of parameters, including converter inductances and turns ratio can be programmed as constants. The impact in the proposed implementation of the tolerances in the values of the converter's inductances and capacitances can be estimated with (60)-(61)."

The problem becomes more severe when higher switching frequencies and lower reactive component values make the time interval shorter.

Thank you for the remark. The switching frequency of the prototype is an example of typical DC-DC converters for server and telecom applications. Evaluating in detail the consequences of increasing the switching frequency might require a new study.

As far as the tolerances remain within their percentages, a variation in the switching frequency does not have an influence in the previous analysis of tolerances. Certainly, for digital implementations the controller timer resolution could be a limiting point. For example, the resolution of the controller used in the implementation of the prototype is 12.5 ns. For higher switching frequencies, a controller with higher timer resolution would be recommended. We are aware of controllers, from the same series of the one used in the prototype, with timing resolutions down to 150 ps.

Moreover, for very high switching frequencies other variables may start having an influence, e.g. the driver's delay. In that scenario the principles of the solution for the DCM operation are still valid. However, the proposed implementations of the DCM algorithm might not be robust, and alternative implementations should be studied to apply the suggested principles. Alternatively, the design of the converter should be constrained to not operate in DCM or the voltage class of the rectifiers increased, with the consequent impact on the overall performance.

This concern would have been substantially mitigated if the proposed timing computation approach (Fig. 15) were implemented in the hardware. The authors are recommended to report these hardware results.

We understand the concerns of the reviewer. The impact of the component tolerances in the timings was already analyzed in the original document and in the previous answer. According to this analysis, a constant delay approach can be used as a simple and reliable implementation, which limits the computation effort of the controller with good performance. The performance of the constant delay was further proven in the experimental results.

Furthermore, the nominal turn on delay could be trimmed during production to account for the deviation in the inductances and capacitances. Additionally, we had provided the suggestion for a deterministic estimation of the delay times, which could be used as a starting point for alternative implementations.

REVIEWER 2 COMMENTS

This paper is a good contribution to the literature, especially as the phase shifted full bridge is a popular topology in many DC-DC converter applications. The paper needs some additions before being published.

Thank you for emphasizing the value of our work. We hope to have covered all the remaining concerns in the improved new version of the document.

Following are point by point answers to your comments (the reviewer's comments are in **bold**).

1. A full bridge secondary is described in this application- the rectification stage can be implemented in other ways, such as a current doubler where the inductance values are reasonably small and the transformer secondary winding is optimized. The authors have to at least include a discussion of a couple of secondary side SR implementations to validate the universality of the proposed scheme.

We thank the reviewer for this remark. The rectification stage may have different configurations, the most common in PSFB converters being center tapped, current doubler or full bridge. Although these alternatives have no major impact on the working principles of the converter they do have a major impact on the current and voltage stress over the secondary side devices and their related conduction and switching losses. The blocking voltage of the secondary side devices is two times the transformer reflected secondary voltage for center tapped and current doubler, or one time the transformer reflected secondary voltage for full bridge. However, the effective $R_{DS,(on)}$ is twice as big for full bridge rectification. Therefore, current doubler and center tapped rectifiers are the most appropriate for lower voltage and high current applications, whereas full bridge is the most common in converters for telecom applications (43.5 V- 59.5 V).

For the interest of the reviewer, simulations have been carried out for center-taped and current doubler rectifier configurations. Due to the over-length of the paper we prefer to exclude this analysis and further discussions. Nevertheless, we have included a paragraph in the new version of the manuscript to state that there is no significant impact on the analysis and the proposed solutions regarding the configuration of the rectification stage.

> *The rectification stage may have different configurations: center tapped, current doubler or full bridge; each of them having its advantages in different applications: low voltage, high current or high voltage outputs respectively* ***Error! Reference source not found.****; however these alternatives have no major impact on the working principles of the converter and the solutions proposed here.*

Figure *a* and Figure *b* compare the secondary side overshoot while the converter operates in DCM with center tapped configuration of the rectification stage, without (Figure *a*) and with (Figure *b*) the proposed modulation. The transformer turns ratio is 21:4:4, the input voltage of the converter is 380 V, and therefore the nominal blocking voltage for the rectifiers is approximately 145 V. While in Figure *a* the overshoot reaches up to 190 V, in the Figure *b* the peak voltage reaches up to 160 V. The converter in Figure *a* will require 250 V breakdown voltage class devices, while the converter in Figure *b* could use 200 V class devices.

Figure *c* (without the proposed modulation) and Figure *d* (when the proposed modulation is applied) compare the secondary side overshoot while the converter operates in DCM with current doubler configuration of the rectification stage. The transformer turns ratio is 21:8, the input voltage of the converter is 380 V, and therefore the nominal blocking voltage for the rectifiers is approximately 145 V. While in Figure *c* the overshoot reaches up to 171 V, in the Figure *d* the peak voltage reaches up to 160 V. The converter in Figure *a* will require 250 V breakdown voltage class devices, while the converter in Figure *b* could use 200 V class devices.

In the examples in Figure *a*, Figure *b*, Figure *c* and Figure *d* there was no additional snubber in place. In real hardware the oscillations will be dampened faster by high frequency impedances not modelled in the simulation. Alternatively, a weak dampening snubber could be used to improve the dampening without increasing notably the losses. However, a snubber it is not necessarily required with the proposed modulation scheme.

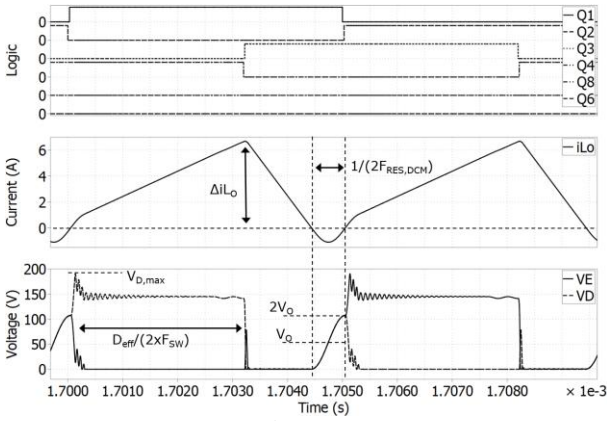

Figure *a*. Secondary side rectifiers overshoot operating in DCM with center tapped configuration.

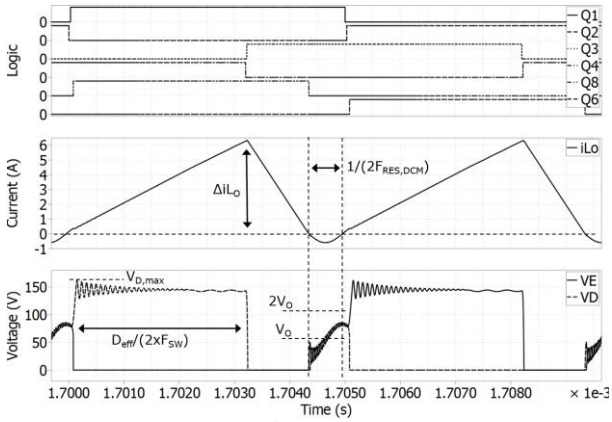

Figure *b*. Secondary side rectifiers overshoot operating in DCM with center tapped configuration and the proposed modulation scheme.

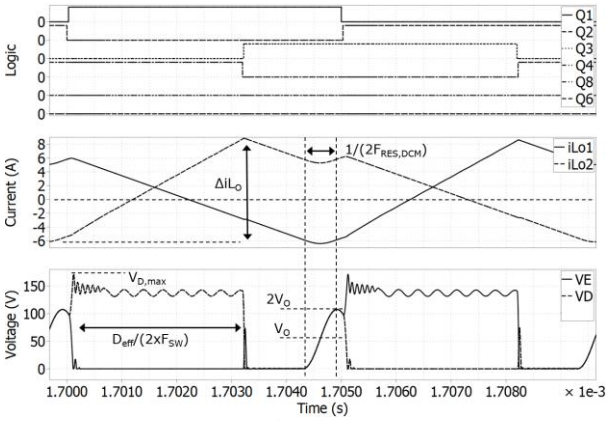

Figure *c*. Secondary side rectifier overshoot operating in DCM with current doubler configuration.

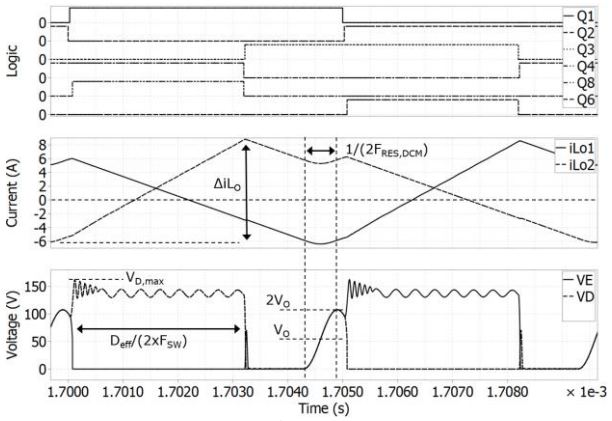

Figure *d*. Secondary side rectifier overshoot operating in DCM with current doubler configuration and the proposed modulation scheme.

It is also possible to get ZVS on the secondary side over a reasonable range of load with timing control.

In standard PSFB modulation schemes the secondary side rectifiers are zero voltage switched (ZVS) in all operating conditions of the converter. However, in our proposed modulation scheme the synchronous rectifiers could be hard-switched while operating in DCM to discharge their output capacitance prior to a power transfer.

The authors are not aware of other reported timing techniques for overcoming the analyzed DCM resonance overshoot. We kindly ask the reviewer, if possible, to provide references to the alternative solutions and help us to quote them in the manuscript.

2. The method of restricting the ring cycle in DCM to a minimal number and selecting the rise time/turn on parameters is a known method, done in commercial power supplies.

We thank the reviewer for this remark. According to the comment, the authors assume the reviewer might be possibly referring to two methods: valley switching and *dv/dt* control.

Regarding the valley switching technique, it is known to the authors, but it is not the solution proposed in this article. Moreover, we have our concerns to the valley switching being applicable to a fixed frequency PWM converter. Because the commutation of the secondary side rectifiers is driven by the reflected primary voltage, the valley switching would have to be controlled from the primary side full bridge.

The modulation scheme we propose in the article hard-switches the synchronous rectifiers during the commutation, therefore discharging the DCM resonance voltage prior to the end of the commutation and avoiding the voltages to stack up.

On the other hand, we understand that the reviewer reference to the rise time control may refer to the *dv/dt* control during the switching transitions. The rise time is not intentionally selected or controlled in our proposed solution. The rise time of the secondary side voltage is a consequence of the converter's design (L_r, L_{lkg}, C_{oss}). The proposed modulation scheme

takes advantage of the rise time to improve the robustness against the tolerances in the converter components with regard to the correct timing. However, the proposed modulation scheme does not constraint the components selection or require a specific raising time.

The authors need to expand the section on implementation to make the paper more useful:

a. The leakage inductance and C_{oss} of the part play an important role in controlling the timing. The C_{oss} varies with part type (Si/GaN/Superjunction etc) and also with voltage within the type. The authors need to explain how in production, a unit can handle variations in part, line and load, as this is a key aspect of how this technique can be used.

We acknowledge the reviewer's concern. We agree there are certain tolerances of C_{oss} within parts. The C_{oss} of interest for the proposed modulation scheme is the $C_{oss(tr)}$ or the equivalent time related capacitance, a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to the final blocking voltage. In the DCM resonance the voltage oscillates between zero and V_o, therefore, the voltage swing is fixed. Moreover, for MOSFETs the major nonlinearity of the capacitance happens in the depletion area, becoming nearly constant at higher voltages. The differences in $C_{oss(tr)}$ for variations in the final blocking voltage are negligible. For planar MOSFETs and Wide Band Gap devices the output capacitance exhibits less non-linearity along all the blocking voltages range. The $C_{oss(tr)}$ can be calculated like it is done for Superjunction MOSFETs.

In the following paragraphs, a time analysis of the on delay in the proposed solution is presented. This analysis includes a tolerance analysis not only on the switches parasitics, but also on the magnetic components.

The turn on instant for the SR ($t_{sr,on}$) can be referenced to the turn off instant of the primary side lagging leg ($t_{lagg,off}$) (55). The start of the voltage build up (T_{rise}) is delayed by the time it takes iL_r to reverse polarity, which can be calculated by (56)-(59). After this delay $T_{dly,on}$ the SR turn on instant should happen within the T_{rise} interval for an effective clamping of the DCM overshoot.

$$T_{rise} = \pi\sqrt{(L_r + L_{lkg})2C_{oss}} \tag{54}$$

$$(t_{lagg,off} + T_{dly,on}) < t_{sr,on} < (t_{lagg,off} + T_{dly,on} + T_{rise}) \tag{55}$$

$$T_{dly,on} = \frac{(iL_r(t_{lagg,off}) - iL_m(t_{lagg,off}))(L_r + L_{lkg})}{V_{in}} \tag{56}$$

$$iL_r(t_{lagg,off}) \approx \frac{iL_{o,pk}}{n} + iL_{m,pk} \tag{57}$$

$$iL_m(t_{lagg,off}) = iL_{m,pk} = \frac{V_{in}}{L_m}\frac{iL_{o,pk}L_o}{(V_{in} - V_o)} \tag{58}$$

$$iL_{o,pk} = \sqrt{\frac{iL_{o,avg}V_o(V_{in} - V_o)}{F_{sw}V_{in}L_o}} \tag{59}$$

In summary, the secondary side rectifiers should be turned on after the $t_{sr,on,min}$ and before $t_{sr,on,max}$ (*a*)-(*c*). From the equations it is possible to estimate the impact of the tolerances in L_o, L_r, L_{lkg} and C_{oss}.

$$T_{dly,on} = \sqrt{\frac{iL_{o,avg}V_o(V_{in} - V_o)}{F_{sw}V_{in}L_o}}\frac{(L_r + L_{lkg})}{V_{in}n} \tag{a}$$

$$t_{sr,on,min} = t_{lagg,off} + \sqrt{\frac{iL_{o,avg}V_o(V_{in} - V_o)}{F_{sw}V_{in}L_o}}\frac{(L_r + L_{lkg})}{V_{in}n} \tag{b}$$

$$t_{sr,on,max} = t_{lagg,off} + \sqrt{\frac{iL_{o,avg}V_o(V_{in} - V_o)}{F_{sw}V_{in}L_o}}\frac{(L_r + L_{lkg})}{V_{in}n} + \pi\sqrt{(L_r + L_{lkg})2C_{oss}} \tag{c}$$

The A_L tolerance of the toroidal cores utilized for the realization of the output inductor is ±8 % in accordance to the manufacturer datasheet. Considering the worst case deviation of 8 %, with all other values constant, the turn on window [$t_{sr,on,min}$, $t_{sr,on,max}$] is approximately delayed a 4 % of the nominal (the $T_{dly,on}$ is proportional to the square root of the inverse of L_o).

For the ferrite cores utilized for the realization of the resonant inductance, the tolerance of the initial permeability is ±25 % in accordance to the manufacturer datasheet. The resonant inductance nominal value is 11µH which is realized with 6 turns. The effective length of the core l_e is 64.9 mm and the effective area A_e is 173.5 mm in accordance to the core set datasheet. The resulting gap is approximately 694 µm. This results in the effective permeability and the tolerance being dominated by the gap length, which makes it possible to manufacture a more repeatable value of inductance.

$$L_r = \frac{N^2 \mu_e \mu_0 A_e}{l_e} \xrightarrow{\text{yields}} \mu_e = 92.21 \qquad (d)$$

$$\mu_e = \frac{\mu_i}{1+\mu_i\left(\frac{l_g}{l_i}\right)} \qquad (e)$$

We can consider for the analysis a 10 % deviation in the resonant inductance value. With all other values constant the turn on window [$t_{sr,on,min}$, $t_{sr,on,max}$] is approximately delayed a 10 % and its length extended approximately 5 % of the nominal. The leakage of transformer L_{lkg} is much smaller than the external resonant inductance L_r. L_{lkg} is in the order of 0.5 µH whereas the nominal value of L_r is 11 µH. A 10 % deviation in L_{lkg} would have the same impact than a 0.45 % deviation in L_r.

In relation to the nominal output capacitance of the secondary side rectifiers, we do not have data for the tolerances. For the devices in the prototype, from the manufacturers' datasheet values, typical 604 pF and maximum 803 pF, we can estimate a 33 % maximum variation. We do not have statistical deviation data for the C_{oss}, therefore we cannot estimate the most probable scenario. A worst case would be all the capacitances deviated to their maximum. Consequently we could expect a maximum deviation of 15 % in the duration of the turn on window (rise time is proportional to the square root of C_{oss}).

All the other values in the equations can be directly measured by the controller. Considering worst case for all parameters deviation the turn on window could be deviated, in this example, up to a 14.45 % and extended (or shrank) up to a 20 %. A 30 % window around the nominal should be still within valid turn on times. For increased robustness exists the possibility of trimming the nominal turn on time during production to account for the tolerances.

The authors would prefer to exclude this long analysis from the final version of the paper, which is already over-length. We have included the two equations for the estimation of the minimum and maximum turn on times, which might be useful to make more obvious the impact of the component values and their deviations.

"The minimum turn on time $t_{sr,on,min}$ and the maximum turn on time $t_{sr,on,max}$ for an effective reduction of the overshoot can be derived from the previous equations and calculated by (60)-(61).

$$\left(t_{lagg,off} + T_{dly,on}\right) < t_{sr,on} < \left(t_{lagg,off} + T_{dly,on} + T_{rise}\right) \qquad (55)$$

$$T_{dly,on} = \frac{\left(iL_r(t_{lagg,off}) - iL_m(t_{lagg,off})\right)(L_r + L_{lkg})}{V_{in}} \qquad (56)$$

$$iL_r\left(t_{lagg,off}\right) \approx \frac{iL_{o,pk}}{n} + iL_{m,pk} \qquad (57)$$

$$iL_m\left(t_{lagg,off}\right) = iL_{m,pk} = \frac{V_{in}}{L_m}\frac{iL_{o,pk}L_o}{(V_{in}-V_o)} \qquad (58)$$

$$iL_{o,pk} = \sqrt{\frac{iL_{o,avg}V_o(V_{in}-V_o)}{F_{sw}V_{in}L_o}} \qquad (59)$$

$$t_{sr,on,min} = t_{lagg,off} + \sqrt{\frac{iL_{o,avg}V_o(V_{in}-V_o)}{F_{sw}V_{in}L_o}}\frac{(L_r+L_{lkg})}{V_{in}n} \qquad (60)$$

$$t_{sr,on,max} = t_{lagg,off} + \sqrt{\frac{iL_{o,avg}V_o(V_{in}-V_o)}{F_{sw}V_{in}L_o}}\frac{(L_r+L_{lkg})}{V_{in}n} + \pi\sqrt{(L_r+L_{lkg})2C_{oss}} \quad (61)$$

Fig. 15 shows a proposal for the implementation of $T_{sr,on}$ in a controller. The voltages and currents through the converter are measurements typically available. Although, depending on the application, they can be considered constant ($V_{in,nominal}$, $V_{o,nominal}$) or estimated out from other of the measurements ($iL_{o,avg} \approx |iT_{r,avg}|n$). The rest of parameters, including converter inductances and turns ratio can be programmed as constants. The impact in the proposed implementation of the tolerances in the values of the converter's inductances and capacitances can be estimated with (60)-(61)."

b. Even with the improvements shown with the scheme, a secondary snubber may be needed to ensure that the part rating is controlled within limits. This has be discussed briefly in the final experimental results.

We thank the reviewer for this remark. In our experiments there was no need of a snubber to ensure the parts were operated within their rated limits. However, a weak snubber may improve the dampening of the commutation resonance without much of an impact on the losses. Therefore, following the recommendation of the reviewer the authors have added the next paragraph in the experimental results section.

"Besides, a weak snubber could be added to further reduce the peak voltage and/or improve the dampening of the commutation resonance without much of an impact on the losses."

3. Operating the inductor in DCM vs CCM and hard switched turn on of the secondary has an impact in high current applications. The savings from the proposed scheme is to select the right FET with a low enough rating, but the inductor size tradeoff and impact on output capacitors etc has to be discussed.

The authors agree with the reviewer as can be seen in the paper by the inclusion of an efficiency impact of the secondary side rectifiers in hard-switching conditions. The DCM modulation is only required at light load operating conditions where the average output current is lower than half the output inductance ripple. At higher loads and output currents, the converter can have a standard operation (ZVS operation of secondary side).

We understand that the reviewer might be referring to hard-commutation of the synchronous rectifiers, however, the proposed modulation hard-switches the SRs but the commutation, like in standard rectification schemes, always happens from the reflected primary side voltage and through the inductances in the path L_r, L_{lkg} and L_{stry}.

The output inductor design criteria is briefly discussed hereafter. The output filter inductor selection is constrained by the output current ripple and the maximum output voltage ripple requirements. The output current ripple can be calculated with the equation (*f*), which has an impact on the *rms* losses the output capacitors (*f*)-(*h*). The maximum output voltage ripple is also a function of the total amount of output capacitance and its parasitic equivalent resistance (*i*)-(*g*).

$$\Delta IL_o \approx \frac{T}{2}\frac{\left(\frac{V_{in}}{n}-V_o\right)D_{eff}}{L_o} \quad (f)$$

$$iC_o \approx \frac{\left(\frac{V_{in}}{n}-V_o\right)}{L_o}t - \frac{\Delta IL_o}{2} \;,\; t \in \left[0, D_{eff}\frac{T}{2}\right] \quad (g)$$

$$iC_o \approx \frac{\Delta IL_o}{2} - \frac{V_o\left(t-D_{eff}\frac{T}{2}\right)}{L_o} \;,\; t \in \left[D_{eff}\frac{T}{2}, \frac{T}{2}\right] \quad (h)$$

$$vC_{o,ripple} = C_{o,ESR}iC_o + \int_0^t \frac{iC_o}{C_o}dt + V_{o,ripple}\Big|_{t=0} \quad (i)$$

$$VC_{o,ripple,min} = \frac{(V_o n - V_{in})\left(16{C_o}^2{C_{o,ESR}}^2 + {D_{eff}}^2T^2\right)}{32C_oL_on} \quad (f)$$

$$VC_{o,ripple,max} = \frac{V_o\left(16{C_o}^2{C_{o,ESR}}^2 + {D_{eff}}^2T^2 - 2D_{eff}T^2 + T^2\right)}{32C_oL_o} \quad (g)$$

The L_o value also impacts other *rms* currents through the converter. Additionally, a side effect of L_o value is the available energy for the ZVS transitions on the primary side of the converter. In a simplified model, not considering the effect of the primary side clamping diodes, because $I_{p,lead}$ increases and $I_{p,lag}$ decreases for bigger output current ripples (Figure e), the ZVS range of the lagging leg is extended for larger values of L_o (Figure f). However, considering also the effect of the clamping diodes in the lagging position, both $I_{p,lead}$ and $I_{p,lag}$ increase for bigger output current ripples, and the ZVS range of the lagging leg can be further extended with smaller values of L_o (Figure *g*).

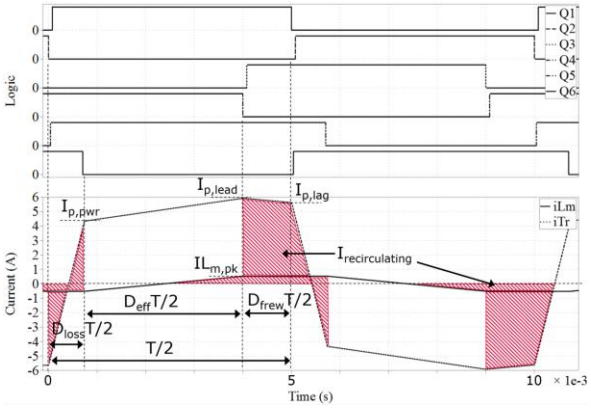

Figure *e*. Primary side current and PWM control signals of a simplified model of PSFB converter.

Figure *e*, *f*, *g*, *h* and *i* analyze the influence of the output inductor selection in another prototype of converter, a PSFB 1.4 kW for server applications. The values of inductances and the ZVS energies will differ from the prototype presented in the paper. However, the outcome of the analysis is equally valid for other designs.

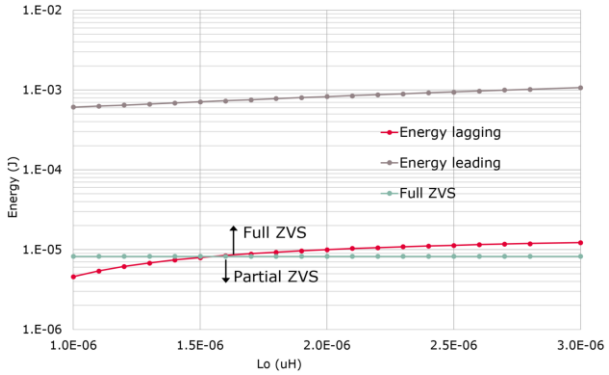

Figure *f*. Available energy for the ZVS transitions depending on the value of the output inductor Lo without clamping diodes. At 10 % of load.

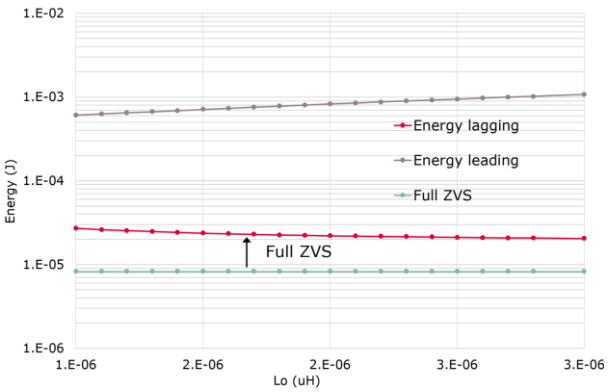

Figure *g*. Available energy for the ZVS transitions depending on the value of the output inductor Lo with clamping diodes. At 10 % of load.

In the realization of L_o a low permeability core is preferred because maintains a more stable value of inductance along the load and the core losses are normally lower. For a given core geometry and core material the core losses and copper losses can be balanced adjusting the number of turns and the number of parallel wires. However, the available winding room in the core limits the possible combinations. In the Figure h and i we compare the effect of only changing the number of turns in the output choke of the reference design: 1.88 µH corresponds to the five turns of five parallel wires of the prototype; 2.70 µH corresponds to six turns and five parallel wires; 1.20 µH corresponds to four turns and five wires; and 3.68 µH to seven turns and five wires. Although for the estimation of losses in Figure h and i the number of wires or their diameter has not been adjusted the impact on the conduction losses is already visible because of the variations in winding length.

The selection of a small inductance at the output of the converter and its impact in the DCM operation of the converter at light loads was already justified in the original document.

"The output filter of the converter could be dimensioned in a way to ensure CCM or DCM in the boundary to CCM operation in all working conditions. This is however impractical in high efficiency converters, as it is difficult to design an efficient high value of inductance ***Error! Reference source not found.****. In this work we propose a solution to the induced DCM overshoot consisting of a novel modulation scheme, which does not constrain the converter design or its performance in any manner."*

The authors consider that a thorough analysis of the constraints, the performance and recommendations for the design of the output inductor of a PSFB converter requires a long discussion and is out of scope of this paper.

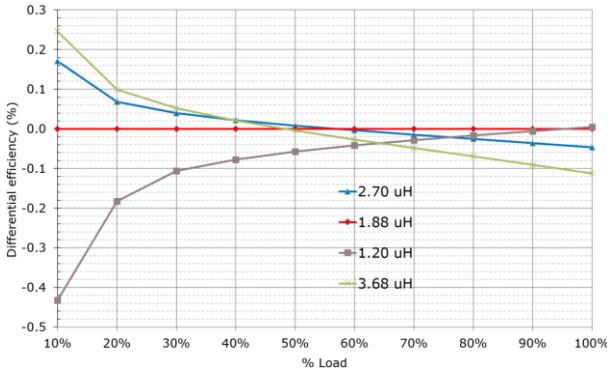

Figure *h*. Performance comparison for different number of turns of the output inductor. Differential efficiency.

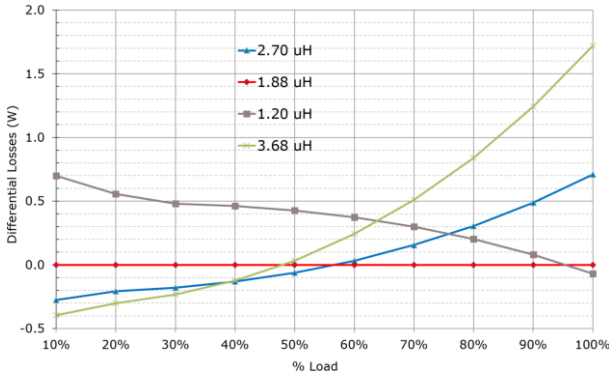

Figure *i*. Performance comparison for different number of turns of the output inductor. Differential losses.

There are advantages to the proposed scheme with better devices. One can run at higher frequencies, and use low capacitance devices that do not penalize the efficiency impact. For future work, a comparison with GaN secondaries may be an interesting topic for development and implementation.

We agree with the reviewer that the switching frequency of the converter can be increased with lower Q_{rr} and Q_{oss} devices. However, for a high efficiency design the output choke will be dimensioned in accordance to the switching frequency of the converter, with a smaller core and proportionally lower inductance. Therefore, is more than likely that the converter will also operate in DCM at a higher frequency, high efficiency design. In consequence, the proposed modulation scheme for the operation of PSFB in DCM would be equally useful.

Moreover, the other overshoot causes and their countermeasures are equally applicable independently of the switching frequency.

Alternatively, the lower Q_{oss} and the lower or zero Q_{rr} of Wide Band Gap devices could potentially increase the performance of the converter maintaining the current switching frequency range (similar to the prototype in the paper). However, they could also have some drawbacks because of the increase forward voltage drop in the third quadrant operation. As the reviewer points out, it is worth to be analyzed in within future, separate works.

The paper does not present new theoretical concepts but is a useful contribution to practicing engineers with a well-known topology. However, as the implementation makes the key difference in this paper, more details on the algorithm and control implementation must be provided for making the paper useful to practicing engineers.

We thank the reviewer for this remark. We consider we have contributed with the analysis of several concepts we are not aware being previously reported in the literature:

- The impact of the clamping diodes and the dimensioning of the external resonant inductance on the secondary side overshoot, the secondary side switching losses and the overall efficiency of the converter.
- Forced CCM overshoot and related reliability issues.
- DCM resonance causing drain voltage overshoot during the commutation of the rectification stage. Traditionally PSFB has been dimensioned with high output inductance. Therefore most of the previous works we are aware of focus in the CCM operation.
- Proposal and analysis of a new modulation scheme overcoming the DCM resonance induced overshoot without constraints in the design or additional components required.
- Proposal of an implementation of the novel DCM modulation scheme.

We agree with the reviewer that the implementation is of interest for practicing engineers. Therefore, as an example, two alternative implementations have been proposed, and recommended because of their simplicity and not requiring any additional component not commonly present in a standard converter. The authors consider that the main points of interest of the article are the analysis of the several overshoot phenomena and the proposed solutions for each of the scenarios, potentially enabling the best possible voltage class for the synchronous rectifiers, and consequently improved overall performance. Moreover, due to the current length of the paper we consider that the implementation approaches are already reasonably well detailed.

REVIEWER 3 COMMENTS

The paper proposes voltage overshoot reduction scheme. It has potential to be applied in many applications which uses PSFB converter.

Thank you for emphasizing the value of our work. Following are point by point answers to your comments (the reviewer's comments are in **bold**).

The paper proposes voltage overshoot reduction scheme. It is important and practical issue. However, the paper does not present clear analysis and comparison which makes readers difficult to follow. In addition, in this revision, the author just added many analysis which results in huge number of paper. Author should provide proper analysis but that does not mean 'many analysis'. Author should provide concise, clear, and essential contents. The paper should be reorganized considerably

Following the recommendation of the reviewer the authors have done an important effort to enhance the structure and content of the paper, improving the clarity and flow of the analysis.

The introduction has been partially reordered and rewritten. The EMI discussion has been moved to the analysis of the commutation overshoot. The ZVS energy discussion of the HV primary side bridge has been removed. The switching losses analysis, which was previously disperse between sections, has been integrated together. The main changes have been marked in red in the new version of the document. After the modifications and additions suggested by the reviewers the final length of the paper was reduced in nearly one page.

We sincerely believe the new version of the paper is clearer and can be better understood.