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In this manuscript we present a new 3D memristor simulator based on circuit breakers (CBs). Previous simulators are 2D; therefore, it means a step forward in the description of memristor operation and the resistive switching processes. The CBs can be switched between different resistance values depending on the voltage between their terminals or on the CB temperature. By means of these mechanisms, that reflect the physics and chemistry involved in the operation of memristors, we are able to reproduce experimental data obtained in h-BN memristors and describe the conductive nanofilament formation and rupture that make the device operate. Moreover, we can reproduce reset processes where the current versus voltage curve presents several steps (partial nanofilament rupture). We can also describe defect regions in the dielectric (our simulation domain), allowing the study of pristine dielectrics and the corresponding resistive switching operation.

The particularities of 2D materials (the case for the dielectric of our devices, hexagonal boron nitride) have been considered in the simulator and they helped to understand the operation and experimental measurements of our devices.

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Title: 3D simulation of conductive nanofilaments in multilayer h-BN memristors via a circuit breaker approach

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Abstract:

A 3D simulation of conductive nanofilaments (CNF) in multilayer hexagonal-BN memristors is performed. To do so, a simulation tool based on circuit breakers is developed including for the first time a 3D resistive network. The circuit breakers employed can be modeled with two, three and four resistance states; in addition, a series resistance and a module to account for quantum effects, by means of the quantum point contact model, are also included. Finally, to describe real dielectric situations, regions with a high defect density are modeled with a great variety of geometrical shapes to consider their influence in the resistive switching (RS) process. The simulator has been tuned with measurements of h-BN memristive devices, fabricated with chemical-vapour-deposition grown h-BN layers, that were electrically and physically characterized. We show the formation of CNFs that produce filamentary charge conduction in our devices. Moreover, the simulation tool is employed to describe partial filament rupture in reset processes and show the low dependence of the set voltage on the device area, that is seen experimentally.

Index Terms — Memristor, resistive switching, 2D materials, simulation, circuit breaker, variability, defects

I.-Introduction

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Memristive devices are being intensively studied in the Academia and industry in the last decade [Chua1976, Corinto2015, Lanza2022]. These devices show a great potential both for standalone and embedded non-volatile memory applications [Pan2014, Lanza2019, Ielmini2015, Lee2015, Spiga2020]; in fact, they have already been incorporated in different industrial products [Lanza2022]. Their features make them fit the market needs (in general, as storage-class memory) and they are CMOS fabrication technology compatible (some memristive devices have a $4F^2$ footprint, where "F" is the minimum technology half-pitch) [Spiga2020].

Although memristor-based non-volatile memory applications are the most commercially advanced [Yang2020, Chou2020, Chou2018], these devices play an important role in other fields such as neuromorphic computing [Yu2011, Ambrogio2018, Merolla2014, Alibart2013, Zhu2023, Sebastian2020, Roldan2022, Prezioso2015, Zidan2018, Hui2021]. The neuromorphic engineering approach [Mead1989] allows the acceleration of matrix-vector multiplication (a key operation in Artificial Intelligence (AI) algorithms) that can be implemented through memristive device crossbar arrays [Lanza2022, Sebastian2020]. This approach can get over some of the hurdles of von Neumann's bottleneck, that are linked to the constant data movement between the memory and the processor. Memristive devices, in this neuromorphic computing context, mimic biological synapses to permit the fabrication of hardware neural networks [Yu2011, Ambrogio2018, Roldan2022, Merolla2014, Alibart2013, Prezioso2015, Zhu2023, Dalgaty2021, Zidan2018]. In this respect, due to the inherent

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redundancy of neural circuits, the device requirements do not need to be as strict as in non-volatile memory applications since AI methodologies allow a greater margin of variability and endurance [Sebastian2020].

Resistive switching memristors are fabricated with a thin layer of dielectric sandwiched between metal electrodes; their electrical and thermal features are closely linked to the materials employed. Different authors have described switching and charge conduction making use of the dynamics of metallic ions, oxygen vacancies and other defects, whose concentration evolves with time in the device active part [Aldana2020a, Menzel2017, Dirkmann2018, Bocquet2014, Aldana2020b, Menzel2015, Funck2021]. In particular, for filamentary conduction, the formation and destruction of CNFs is a stochastic process that leads to cycle-to-cycle (C2C) variability [Perez2019, Mikhaylov2021, Ielmini2015, Roldan2023, Lee2015]. This inherent variability (in addition to device-to-device (D2D) variability [Perez2019]) has to be minimized for memory applications; however, it could be beneficial in some cases for deep neural network training to avoid overfitting [Romero-Zaliz2021]. Variability is key for hardware cryptography (an entropy source that allows the fabrication of physical unclonable functions and random number generators) [Carboni2019, Pazos2023, Wei2016, Chen2015b, Lanza2021]. C2C variability is linked to CNFs morphological changes in each RS cycle, where the CF is created (set process) and ruptured (reset process) successively [Aldana2020a, Menzel2017, Dirkmann2018, Menzel2015, Funck2021]. The device C2C and D2D variability, and switching dynamics can be tackled from different simulation and modeling approaches such as: kinetic Monte Carlo (kMC) simulation [Vandelli2015, Aldana2020a, Dirkmann2018, Aldana2020b,

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Guy2015]; advanced statistical modeling [Roldan2019, Alonso2021] and compact modeling (for circuit simulation and design) [Huang2013, González-Cordero2017, Chen2015a, Corinto2015, Guan2012, Huang2017, Jiang2016, Roldan2021]. A different approach, although complementary, is based on RRAM simulation by means of circuit breakers (CB) [Lee2015, Chang2009, Lee2011, Chae2008, Brivio2017, Maldonado2022, Roldan2022b]. These CB-based simulators are bidimensional; nevertheless, a 3D approach is needed if CNFs (in case of filamentary operation) are to be described correctly, see in Ref. [Aldana2018] a study on the appropriateness of a 3D description in comparison with a 2D approach based on a kMC simulation tool. CB-based simulation poses a numerical technique in between kMC and compact modeling for circuit simulation in what is refereed to complexity, although it allows a reasonable description of variability and current versus voltage curves.

In this work we present a 3D CB-based simulator that can describe the CNF evolution (that facilitates RS operation) and the charge transport in the filamentary operation regime. Apart from common features for these CB-based simulation tools [Lee2015, Chang2009, Lee2011, Chae2008, Brivio2017], we include quantum effects implemented through the quantum point contact model, the use of circuit breakers with four conductivity stages and a device series resistance. We also consider 3D regions of different shapes within the simulator domain to model dielectric zones with high defect density formed at the fabrication stage that evolve as the RS unfolds. This latter feature is hardly ever taken into consideration in simulation tools.

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We have tuned our simulator making use of experimental measurements from hexagonal boron-nitride memristive devices [Lanza2021b] that we have fabricated. The devices characterized here have been studied previously [Roldan2022, Acal2023], physical and electrical experimental characterization was employed. Devices with some similarities in the layer stack were also analyzed from different viewpoints [Pan2017]. All these works were purely experimental. In this work we present an analysis where a strong simulation approach was introduced. The 3D modeling employed was implemented by means of a new CB-based simulator that allows to assess different physical effects on the RS operation and the role of high defect density regions in the dielectric on device variability and reliability.

It is important to draw attention to the fact that there exist different physical characterization techniques to visualize conductive nanofilaments [Li2017, Knot2022, Knot2023]. They are based on the use of Conductive Atomic Force Microscopy (C-AFM) and Transmission Electron Microscopy (TEM). These techniques allow outstanding analyses that give us information about the CNF composition, size, shape, charge transport features, etc. This information can be used in the development of models and simulation tools. They are also important for the model and simulator calibration, in addition to electrical measurements. Once the simulators are tuned, they can complement C-AFM and TEM by providing an exact map of the temperature and the electric field in the simulation domain (usually the dielectric, although it could include the electrodes), the progress in the CNF formation, the influence of high defect density regions on RS, quantum effects, and charge transport processes.

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The measurements have been correctly fitted and different operational particularities have been explained in full. In particular, in section II, we introduce the fabrication and measurement details; the simulator description is presented in section III and the results and discussion is given in section IV. Finally, the main conclusions are drawn in section V.

II.-Device fabrication and measurement setup

The memristive devices used in our study have been introduced previously [Roldan2022]. The electrodes are made of a bilayer of 40 nm Au/10 nm Ti thick (E-beam evaporation is employed). The bottom electrode is deposited on a Si wafer, with 300nm SiO_2 on top the Si. Then, a h-BN multilayer (18 layers approximately, see Figures 1a and 1b) film was placed on top of the bottom electrode by wet transfer from a Cu foil where it was grown by chemical vapor deposition. In Figure 1c RS I-V curves are shown. They are obtained with a B1500A Keysight semiconductor parameter analyzer and a probe station (Karl Suss); Ramped Voltage Stress (RVS) is used for the measurement of long RS series with consecutive set and reset cycles. RS operation is filamentary [Roldan2022].

In Figures 1d and 1e we plot the set and reset parameters, the Low and High Resistance States (LRS/HRS) are plotted in Figure 1f. It is clear that the resistance ratio (R_{HRS}/R_{LRS}) allows non-volatile memory applications (see the cumulative distribution functions of R_{HRS} and R_{LRS} in the inset in Figure 1f, a reasonable variability is obtained).

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It is interesting to highlight that CVD grown polycrystalline h-BN multilayers, as the one employed here, work well for RS devices since it includes insulating 2D layered regions and clusters of defects that are more conducting (these clusters of defects may be related to lattice distortions that propagate from one layer to another [Shi2018, Pan2017]). Other options, such as exfoliated h-BN, do not exhibit RS [Hattori2015].

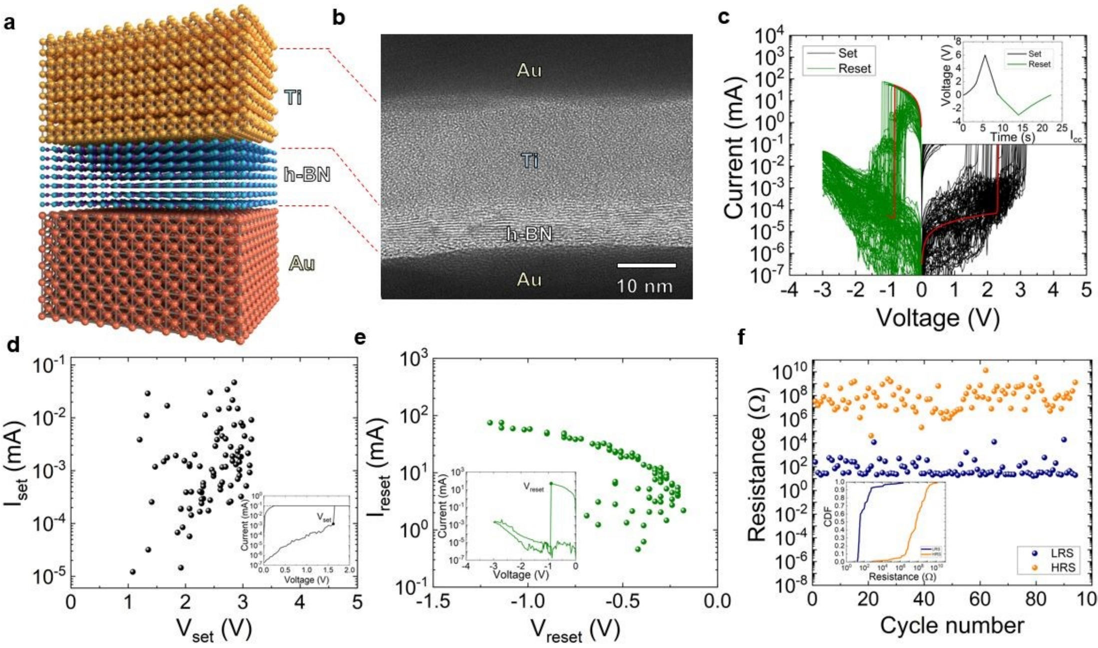

Figure 1. **a** Device layer scheme, **b** Cross-section TEM image of the dielectric and surrounding layers in the device stack. In the h-BN dielectric, we have approximately 18 layers that were transferred from Cu foils. **c** Current versus voltage measured in the ramped voltage stress operation regime, see the voltage versus time signal in the inset. **d** Set current versus set voltage for the curves shown in c; the set point definition is shown in the inset. **e** Reset current versus voltage for the I-V curves in c, in the inset it is shown the criterion established to define the reset voltage. **f** HRS and LRS resistance values versus cycle number in the resistive switching series obtained in figure c (the data are read at 0.1 V). Inset: cumulative distribution function (CDF) of the HRS and LRS resistance values.

III.-Simulator description

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The simulation tool we developed, based on CBs, allows the analysis of RRAM RS, charge conduction and variability. CNF creation and destruction can be modeled to describe both unipolar and bipolar device operation. A 3D approach is followed, and therefore, it means a step forward with respect to 2D CB tools [Lee2015, Chang2009, Lee2011, Chae2008, Brivio2017, Maldonado2022] (see Figure 2a). Following the simulation scheme unfolded in [Maldonado2022], CBs with several conductance levels are included (Figure 2b). Quantum effects in the charge conduction are considered by means of the Quantum Point Contact (QPC) model [Miranda2010, Roldan2018], also the effects of metal pads and electrodes are included through a series resistance [Maldonado2021] (Figure 2a).

The particularities of the h-BN dielectric are considered by utilizing two types of CB resistance values: in-plane CBs, represented in blue in Figure 2a, that account for charge conduction in the BN layers and out-of-plane CBs (red ones) that represent charge conduction in the dielectric vertical direction. The resistance values are described as plotted in Figure 2b, selecting two, three or four levels. In whatever case, the red CBs are scaled with respect to the blue ones due to the different nature of the transport in a h-BN plane or in the perpendicular direction of the multilayer stack (c-axis).

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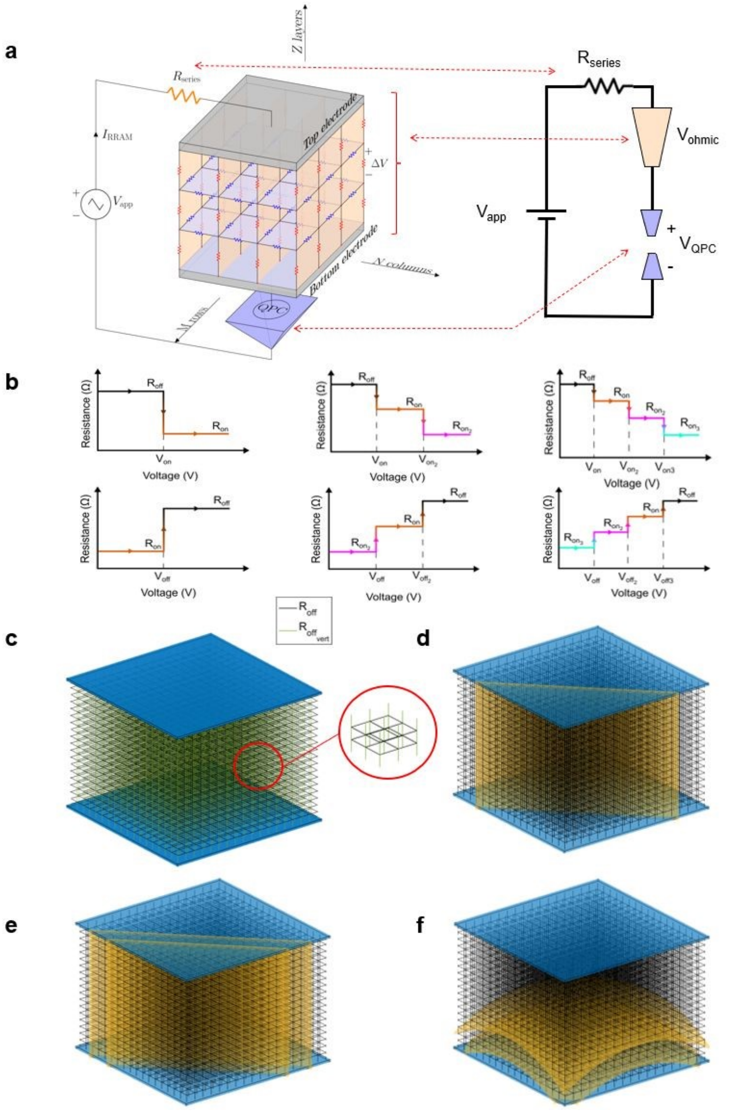

Figure 2. **a** Schematics of the 3D CB network diagram that depicts the internal electric circuitry included in the simulator to model the device. The horizontal CBs symbolize B vacancies embedded within the percolation path. The CBs are differentiated by blue and red colors, describing conduction in the h-BN layers (with lower associated resistances) and in the perpendicular direction of the BN planes (corresponding to much higher resistance in our model). The top and bottom electrodes are connected to an external voltage source. The model includes a series resistance that accounts for the metal pads and electrode resistances, it is obviously in series with the resistance network the represents the dielectric. Quantum effects related to potential barriers along the charge conduction path are taken into consideration by means of the QPC model. A single module for the QPC model is employed in series with the resistance network. **b** The CB internal resistance values for the set (or forming) process is categorized into two levels (R_{off} and R_{on}), three levels (R_{off}, R_{on}, and R_{on2}) and four levels (R_{off}, R_{on}, R_{on2}, and R_{on3}). Similarly, for the reset process, the CB internal resistance structure is described for two, three or four levels. **c** Schematic of the 3D CB network incorporating two types of CBs to address the resistivity in-layer and out-layer in the h-BN. In this case, the horizontal CBs are represented in black, while the vertical CBs are denoted in green to better visualized them. **d** 3D CB network including a 2D vertical plane (in yellow) to model a region with a higher defect density, **e** 3D vertical plane and **f** a 3D curved plane in the CB domain to represent regions of different shape with a higher defect density.

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At the beginning of the simulation (corresponding to a pristine dielectric), we can select the probability of having some CBs in the low resistance values (in case of two levels, the R_{on} value) in all the dielectric volume. In addition, we can define a 3D region, described by its geometrical equation, where the probability of having defects is higher than in the rest of the dielectric (this is modeled by increasing the CB probability of being in the low resistance value at the beginning of the simulation). Within the regions selected, determining a certain geometry (a single plane, Figure 2d, a thick plane Figure 2e, including several layers of CBs; a curve surface of different thickness, Figure 2f), the initial probability can be changed (usually higher) with respect to the rest of the dielectric. This assumption can help to consider different pristine dielectrics or changes along a switching cycle series, and, therefore, direct the CNF formation through this region. If we consider three or four resistance levels for each CB, we can also select between other low resistance levels (R_{on}, R_{on2}, R_{on3}) as the CNF is getting formed along a set or forming process. The CB high-resistance component represents a defect-free dielectric region where charge transport is not enhanced by any means and the h-BN works as an ideal dielectric. The CB low-resistance component could be associated with the presence of a Ti atom inside the h-BN stack. Ti^{X+} ions move toward the cathode across the dielectric leading to CNF formation through the h-BN multilayer. These CNFs short the electrodes and strongly reduce the device resistance. The ions are expected to diffuse preferentially at locations where the lower density of the material and the larger density of B and N vacancies favor their migration. Under negative bias (the bottom electrode is assumed to be always

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grounded) Ti^{X+} ions may diffuse back to their original positions leading to the CNF rupture, i.e., a reset event [Pan2017, Roldan2022].

The switching between the CB resistance values is performed when V_{on} (also V_{on1} and V_{on2}) or V_{off} (also V_{off1} and V_{off2}) are overpassed (see Figure 2b). Additionally, a fully thermal simulation can be performed by controlling the CB switching through temperature calculations, as described in [Maldonado2022, Video].

IV.-Results and discussion

We have simulated the devices described in section II. A 18x18x18 matrix of resistors was employed since the 6nm-thick dielectric consist of 18 layers approximately of h-BN [Roldan2022, Zhu2023]. We have employed a two-value CB resistance model, although higher complexities are allowed in the simulation tool (see Figure 2b). As a reference, the scale between the values of the blue (in-plane CBs), see Figure 2a, and red (out-plane CBs, higher resistance) resistances assumed in the simulation was 10. In this case, the best fit of the experimental curve was performed (blue curve, Figure 3a and 3b). For a scale factor of 20 the green curve for the set I-V curve is obtained (Figure 3a and 3b). We have also included for the sake of comparison a simulation where no distinction between the horizontal and vertical CBs is assumed (orange curve corresponding to CBs with equal resistance values). In this latter case a much different I-V curve is obtained.

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Due to the h-BN material structure a distinction between in-plane and out-of-plane CBs is needed.

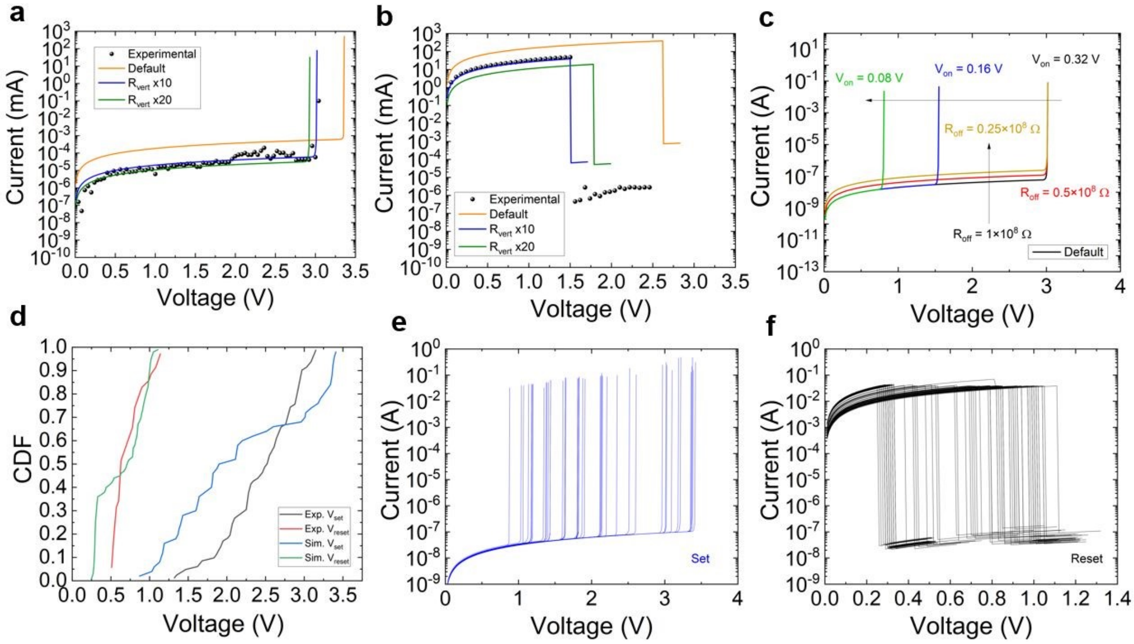

Figure 3. **a** Current versus voltage absolute value curve of simulated data (solid lines) and experimental data (black symbols) for a set process and **b** for a reset process. An 18×18×18 resistor array was employed to obtain this simulation using CBs with two resistance levels: $R_{off} = 1 \times 10^8\ \Omega$ and $R_{on} = 0.5\ \Omega$. The model parameters in relation to Figure 2 are: $V_{off} = 0.195$ V and $V_{on} = 0.32$ V. A 10 scale factor was employed between horizontal (lower) and vertical (higher) resistances. This corresponds to the blue line, a scale factor of 20 was used in the green line. The default curve (orange) stands for CBs with similar resistance values for the vertical and horizontal directions. **c** Simulated current versus voltage set curves. The model parameter employed were those of panel a, for the default curve. Other curves obtained by changing some of the model parameters are shown for comparison, to assess their influence in the simulation tool. **d** CDFs for the experimental (c) and simulated (panels e and f) set and reset voltage (absolute value) points extracted from the I-V curves. **e (f)** simulated set (reset) cycles obtained for different probabilities for the defect density included in the geometry described in Figure 2e (a thick plane). The simulation parameters are the same as in Figure 3a and 3b. Voltage absolute values were considered for the reset processes.

The fitting of I-V experimental curves is shown in Figure 3a-3b. Some simulated curves are shown in Figure 3c for different model parameters. See how the current level and the set voltage depend on the model parameters. A comparison between the set and reset voltages CDFs obtained from experimental and simulated curves is given in Figure 3d. The

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group of simulated curves is obtained by changing the thickness of the geometry shown in Figure 2e, and the probability linked to the CBs within this geometry in the low resistance state at the beginning of the simulation (see Figures 3e and 3f where the group of simulated I-V curves is shown). In spite of the approximations performed in the modeling implemented in the simulator, the curve fitting is reasonable (Figure 3d). In this respect the cycle-to-cycle variability can be described with our simulation tool.

In Figure 4a we have plotted a simulated set current versus voltage. Different points have been marked along the curve in order to follow the CNF evolution. The low resistance value circuit breakers (R_{on}) are shown in red in Figures 4b-e (assuming two resistance values CBs); these panels correspond to the simulation points shown in symbols in Figure 4a. Notice how the CNF is formed as the set process unfolds till (in Figure 4e) it shorts the electrodes and constitutes a fully-formed conduction path. The latter points (2-4) correspond to the sudden current rise that is seen both in simulated and experimental curves close to the set point, where a positive feedback process linked to the CNF formation is triggered [Aldana2020a].

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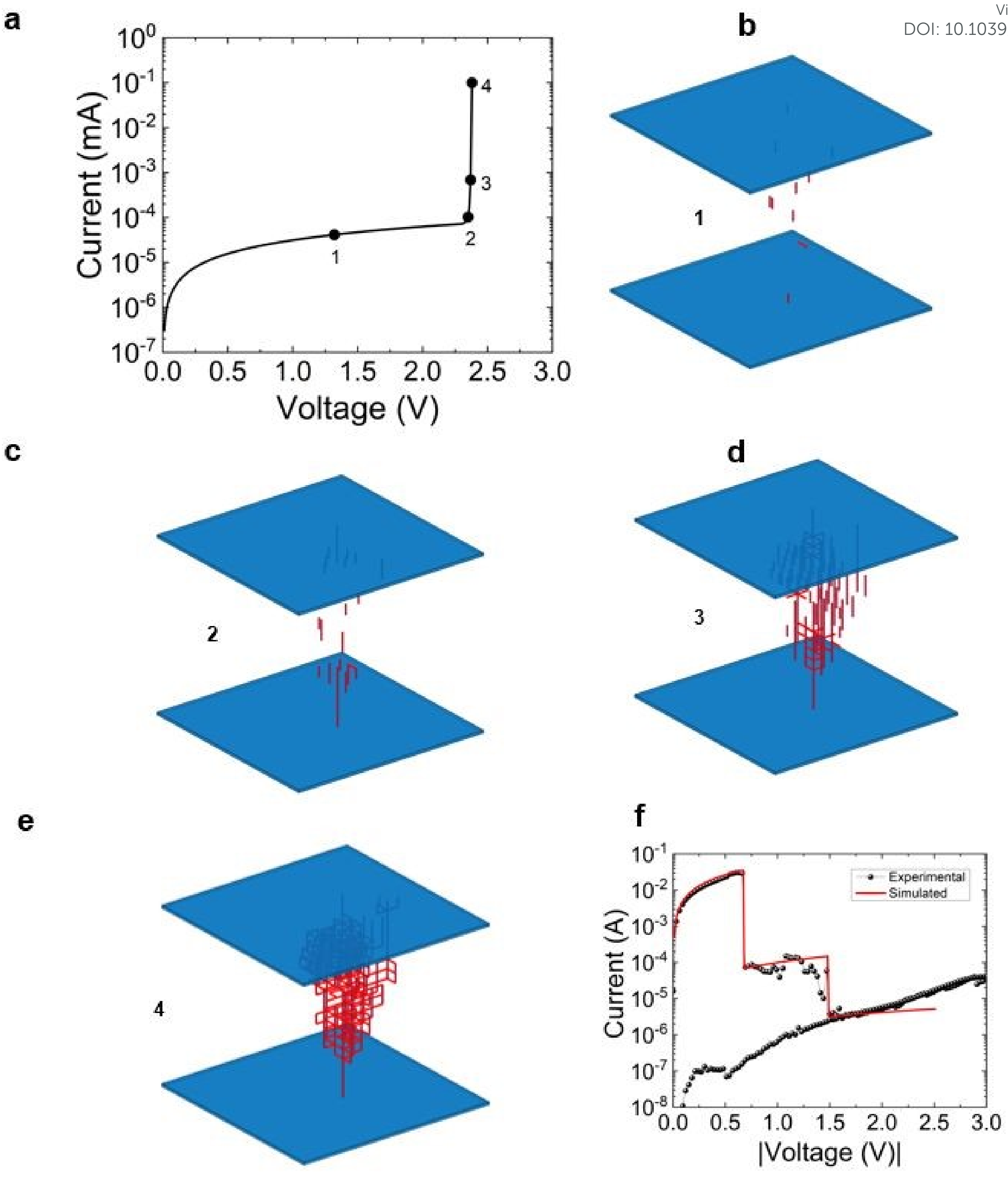

Figure 4. **a** Simulated current versus voltage in a set process. See different points along the I-V that corresponds to different CNF formation stages (the CNFs are plotted in panels **b-e**) An 18×18×18 network was employed to obtain this simulation using CBs with two resistance levels: R_{off} = 65.5 × 10^6 Ω, R_{on} = 0.24 Ω. The model parameters in relation with Figure 2 are: V_{off} = 0.11 V, V_{on} = 0.25 V. A 10 scale factor was employed between horizontal (lower) and vertical (higher) resistances. **f** Simulated and experimental current versus voltage in a set process. A clear stepped curve is seen due to the partial CNF rupture along the reset process.

Some of the experimental curves measured present a stepped-like shape (see Figure 4f) due to a CNF rupture in several stages. Our simulator can reproduce this behavior. In this respect, a single CNF could be broken in steps, or two CNFs (formed in a previous set event) can go through a reset process and get broken at different times. Experimental and simulated curves are shown in Figure 4f to illustrate this effect.

The simulator can also be used to study large area devices. For instance, 100 nm x 100 nm area devices are simulated maintaining the number of CBs per nanometer that corresponds to the description of the h-BN layers of the dielectric described above. In this respect, millions of CBs are taken into consideration (see Figures 5a and 5b for plots of a large area device simulation CB network). In this case, big matrix processing acceleration techniques have been implemented. In Figure 5c we have shown arbitrary I-V curves simulated for devices with different areas. In this case no regions of high defect density were assumed. The probability of finding CBs in the low resistance value at the beginning of the simulation (1% in these examples) was the same in all cases; notice that a different random distribution is generated at the start of each simulation. We have scaled the I-V curves by a factor $\text{Area}_{\text{smallest\_area\_simulated}}/\text{Area}_{\text{actual\_device\_area}}$ in order to fairly compare the curves taking into consideration the purely resistive network we have employed to model the device. It is seen that, although the current curves are close together, the set voltage varies in each of the device areas employed. This parameter depends on the initial random distribution of low resistance CBs. We have plotted the set voltage versus device area in Figure 5d, it can be seen that as the area increases the set voltage decreases. This effect is linked to the higher probability (for the higher area devices) of finding a pre-formed subpath with the random initial

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CB configuration to let the CNF be created. As can be seen, as the area increases, the set voltage reduction saturates, as it is expected for devices where charge conduction is based on filamentary switching (Figure 5d).

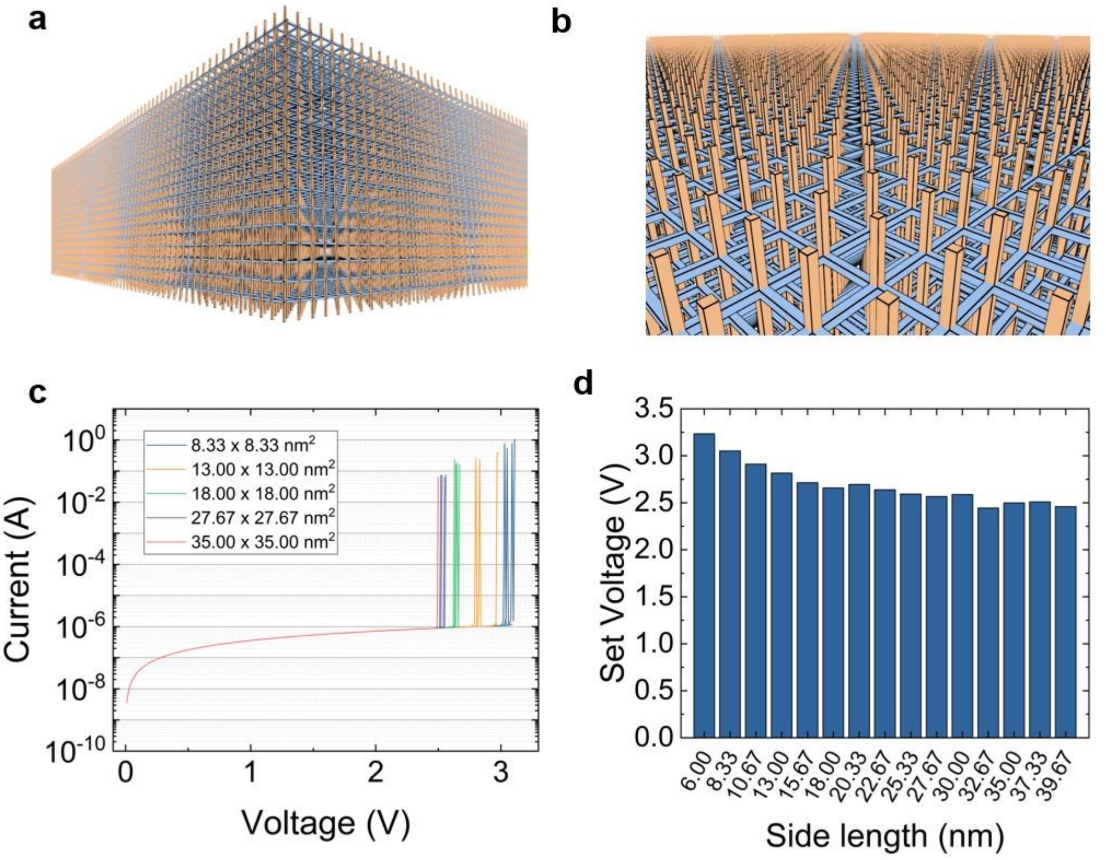

Figure 5. **a** Resistance network corresponding to a great area (100 nm x 100 nm) device. **b** Resistance network corresponding to a great area (100 nm x 100 nm) device (zoomed-in view). **c** Several simulated set I-V curves for different device areas (the current values are scaled with respect to the lowest area shown in the plot, i.e. (8.33 nm x 8.33 nm)). **d** Set voltage versus device side length (assuming a device square area obtained as (side length)^2).

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V.-CONCLUSIONS

A 3D simulation tool based on CBs is developed for the first time to describe RS in multilayer h-BN memristors. It is based on CBs that can be modeled with two, three and four resistance states; in addition, a series resistance and a module to account for quantum effects. The simulator has been tuned with measurements of h-BN memristive devices. The influence of the model parameters has been shown in the simulator tuning process. We also show the CNF formation that accounts for filamentary charge conduction in our devices, explaining the current abrupt change when the set event takes place. In doing so, the particularities of the material have been taken into consideration. Moreover, the simulation tool is employed to describe partial filament rupture in reset processes. Finally, the dependence of the set voltage with the device area is described by means of simulations with a massive number of CBs.

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VI. - ACKNOWLEDGMENTS

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Data available on request from the authors. The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflict of Interest

There are no conflicts of interest to declare.

References

View Article Online
DOI: 10.1039/D3MH01834B

[Acal2023] C. Acal, D. Maldonado, A. M. Aguilera, K. Zhu, M. Lanza, J. B. Roldán, “Holistic variability analysis in resistive switching memories using a two-dimensional variability coefficient”, ACS Applied Materials & Interfaces, 15, 15, 19102–19110, 2023.

[Aldana2018] S. Aldana, P. García-Fernández, R. Romero-Zaliz, F. Jiménez-Molinos, F. Gómez-Campos, J.B. Roldán, "Analysis of conductive filament density in resistive RAMs, a 3D Kinetic Monte Carlo approach", Journal of Vacuum Science and Technology B, 36, p. 62201, 2018.

[Aldana2020a] S. Aldana, P. García-Fernández, R. Romero-Zaliz, M.B. González, F. Jiménez-Molinos, F. Gómez-Campos, F. Campabadal, J.B. Roldán, "Resistive Switching in HfO2 based valence change memories, a comprehensive 3D kinetic Monte Carlo approach", Journal of Physics D: Applied Physics, in press53, 225106, 2020.

[Aldana2020b] S. Aldana, E. Pérez, F. Jimenez-Molinos, C. Wenger, J.B. Roldán, "Kinetic Monte Carlo analysis of data retention in Al:HfO2-based resistive random access memories", Semiconductor Science and Technology, 35, 115012, 2020.

[Alibart2013] F. Alibart, E. Zamanidoost, D.B. Strukov, “Pattern classification by memristive crossbar circuits using ex situ and in situ training”, Nature Communications, 4, p. 2072 (2013).

[Alonso2021] F.J. Alonso, D. Maldonado, A.M. Aguilera, J. B. Roldan, "Memristor variability and stochastic physical properties modeling from a multivariate time series approach", Chaos, Solitons & Fractals, 143, 110461, 2021.

[Ambrogio2018] S. Ambrogio, et al., “Equivalent-accuracy accelerated neural-network training using analogue memory”, Nature, 558, 60–67, 2018.

[Brivio2017] S. Brivio, S. Spiga, “Stochastic circuit breaker network model for bipolar resistance switching memories”, Journal of Computational Electronics, 16, pp.1154–1166, 2017.

[Bocquet2014] Bocquet M, Deleruyelle D, Aziza H, Muller C, Portal J-M, Cabout T and Jalaguier E, “Robust compact model for bipolar oxide-based resistive switching memories”, IEEE Trans. Electron Devices, 61, pp. 674–81, 2014.

[Carboni2019] R. Carboni, D. Ielmini, “Stochastic Memory Devices for Security and Computing”, Advanced Electronic Materials, 5, p. 1900198, 2019.

[Chae2008] S.C. Chae, J.S. Lee, S. Kim, S.B. Lee, S.H. Chang, C. Liu, B. Kahng, H. Shin, D.W. Kim, C.U. Jung, S. Seo, M.J. Lee, T.W. Noh, “Random circuit breaker network model for unipolar resistance switching”, Advanced Materials, 20, pp.1154–1159, 2008.

[Chang2009] S.H. Chang, J.S. Lee, S.C. Chae, S.B. Lee, C. Liu, B. Kahng, D.W. Kim, T.W. Noh, “Occurrence of both unipolar memory and threshold resistance switching in a NiO film”, Phys. Rev. Lett. 102, 026801, 2009.

View Article Online
DOI: 10.1039/D3MH01834B

[Chen2015a] P. Chen and S. Yu, "Compact Modeling of RRAM Devices and Its Applications in 1T1R and 1S1R Array Design" IEEE Transactions on Electron Devices, vol. 62, no. 12, pp. 4022-4028, Dec. 2015.

[Chen2015b] A. Chen, "Utilizing the variability of resistive random access memory to implement reconfigurable physical unclonable functions", IEEE Electron Device Lett., vol. 36, no. 2, pp. 138-140, Feb. 2015.

[Chou2018] C.-C. Chou et al., "An N40 256K×44 embedded RRAM macro with SL-precharge SA and low-voltage current limiter to improve read and write performance," in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), 2018.

[Chou2020] C.-C. Chou et al., "A 22nm 96K×144 RRAM macro with a self-tracking reference and a low ripple charge pump to achieve a configurable read window and a wide operating voltage range," in Proc. IEEE Symp. VLSI Circuits, 2020.

[Chua1976] Chua, Leon O., and Sung Mo Kang. "Memristive devices and systems." Proceedings of the IEEE 64.2 (1976): 209-223.

[Corinto2015] F. Corinto, P. P. Civalleri, L. O. Chua. "A theoretical approach to memristor devices", IEEE Journal on Emerging and Selected Topics in Circuits and Systems 5.2, 123-132, 2015.

[Dalgaty2021] T. Dalgaty, N. Castellani, C. Turck et al., "In situ learning using intrinsic memristor variability via Markov chain Monte Carlo sampling", Nature Electronics, 4, 151–161, 2021.

[Dirkmann2018] S. Dirkmann, J. Kaiser, C. Wenger, T. Mussenbrock, "Filament Growth and Resistive Switching in Hafnium Oxide Memristive Devices", ACS applied materials & interfaces, 10(17), 14857-14868, 2018.

[Funck2021] C. Funck, S Menzel, "Comprehensive model of electron conduction in oxide-based memristive devices", ACS Applied electronic materials, 3, 3674-3692, 2021.

[González-Cordero2017] G. González-Cordero, M.B. González, H. García, F. Campabadal, S. Dueñas,, H. Castán, F. Jiménez-Molinos, J.B. Roldán, "A physically based model for resistive memories including a detailed temperature and variability description", Microelectronic Engineering, 178, pp. 26-29, 2017.

[González-Cordero2019] G. González-Cordero, M. Pedro, J. Martin-Martinez, M.B. González, F. Jiménez-Molinos, F. Campabadal, N. Nafría, J.B. Roldán. (2019). Analysis of resistive switching processes in TiN/Ti/HfO2/W devices to mimic electronic synapses in neuromorphic circuits. Solid State Electronics, Volume 157, July 2019, Pages 25-33. DOI: 10.1016/j.sse.2019.04.001

[Guan2012] X. Guan, S. Yu, and H.-S. Philip Wong, "A SPICE Compact Model of Metal Oxide Resistive Switching Memory With Variations," Electron Device Letters, IEEE, vol.33, no.10, pp.1405,1407, Oct. 2012.

[Guy2015] J. Guy, G. Molas, P. Blaise, M. Bernard, A. Roule, G. Le Carval, V. Delaye, A. Toffoli, G. Ghibaudo, F. Clermidy, B. De Salvo, L. Perniola, "Investigation of Forming, SET, and Data Retention of Conductive-Bridge Random-Access Memory

View Article Online
DOI: 10.1039/D3MH01834B

for Stack Optimization", IEEE Transactions on Electron Devices, 62(11), pp. 3482-3489, 2015.

[Hattori2015] Y. Hattori, T. Taniguchi, K. Watanabe, K. Nagashio, "Layer-by-layer dielectricbreakdown of hexagonal boron nitride", ACS Nano, 9, 916, 2015.

[Huang2013] Huang, P., Liu, X. Y., Chen, B., Li, H. T., Wang, Y. J., Deng, Y. X., … Kang, J. F., "A Physics-Based Compact Model of Metal-Oxide-Based RRAM DC and AC Operations", IEEE Transactions on Electron Devices, 60(12), 4090–4097, 2013.

[Huang2017] Huang, P., Zhu, D., Chen, S., Zhou, Z., Chen, Z., Gao, B., … Kang, J., "Compact Model of HfOX-Based Electronic Synaptic Devices for Neuromorphic Computing", IEEE Transactions on Electron Devices, 64(2), 614–621, 2017.

[Hui2021] F. Hui, P. Liu, S. A. Hodge, T. Carey, C. Wen, F. Torrisi, D. Thanuja L. Galhena, F. Tomarchio, Y. Lin, E. Moreno, J. B. Roldan, E. Koren, A. C. Ferrari, M. Lanza, "In-situ Observation of Low-Power Nano-Synaptic Response in Graphene Oxide using Conductive Atomic Force Microscopy", Small, 2101100, 1-8, 2021.

[Ielmini2015] D. Ielmini, R. Waser. "Resistive Switching: From Fundamentals of Nanoionic Redox Processes to Memristive Device Applications", Wiley-VCH, 2015.

[Jiang2016] Z. Jiang, Y. Wu, S. Yu, Member, L. Yang, K. Song, Z. Karim, H.-S. P. Wong, "A Compact Model for Metal–Oxide Resistive Random Access Memory With Experiment Verification", IEEE Transactions on Electron Devices, vol. 63, no. 5, pp. 1884-1892, May 2016.

[Kim2014] K. Kim, S.J. Yoon, W.Y. Choi, "Dual random circuit breaker network model with equivalent thermal circuit network", Applied Physics Express, 7, 024203, 2014.

[Knot2022] A.C. Khot, T.D. Dongale, K.A. Nirmal, J.H. Sung, H.J. Lee, R.D. Nikam, and T.G. Kim, "Amorphous Boron Nitride Memristive Device for High-Density Memory and Neuromorphic Computing Applications", ACS Applied Materials & Interfaces, 14 (8), 10546-10557, 2022.

[Knot2023] A.C. Khot, T.D. Dongale, K.A. Nirmal, J.K. Deepthi, S.S. Sutar, T.G. Kim, "2D Ti3C2Tx MXene-derived self-assembled 3D TiO2 nanoflowers for nonvolatile memory and synaptic learning applications", Journal of Materials Science & Technology, 150, 1-10, 2023.

[Lanza2019] M. Lanza, H.-S. P. Wong, E. Pop, D. Ielmini, D. Strukov, B.C. Regan, L. Larcher, M.A. Villena, J.J. Yang, L. Goux, A. Belmonte, Y. Yang, F. M. Puglisi, J. Kang, B. Magyari-Köpe, E. Yalon, A. Kenyon, M. Buckwell, A. Mehonic, A. Shluger, H. Li, T.-H. Hou, B. Hudec, D. Akinwande, R. Ge, S. Ambrogio, J.B. Roldan, E. Miranda, J. Suñe, K.L. Pey, X. Wu, N. Raghavan, E. Wu, W.D. Lu, G. Navarro, W. Zhang, H. Wu, R. Li, A. Holleitner, U. Wurstbauer, M. Lemme, M. Liu, S. Long, Q. Liu, H. Lv, A. Padovani, P. Pavan, I. Valov, X. Jing, T. Han, K. Zhu, S. Chen, F. Hui, Y. Shi, "Recommended methods to study resistive switching devices", Advanced Electronics Materials, 5, 1800143, 2019.

View Article Online
DOI: 10.1039/D3MH01834B

[Lanza2021] C. Wen, X. Li, T. Zanotti, F. M. Puglisi, Y. Shi, F. Saiz, A. Antidormi, S. Roche, W. Zheng, X. Liang, J. Hu, S. Duhm, J. B. Roldan, T. Wu, V. Chen, E. Pop, B. Garrido, K. Zhu, F. Hui, M. Lanza, "Advanced data encryption using two-dimensional materials", Advanced Materials, 2100185, 1-12, 2021.

[Lanza2021b] M. Lanza, Y. Shi, F. Palumbo, F. Aguirre, S. Boyeras, B. Yuan, E. Yalon, E. Moreno, T. Wu, J. B. Roldan, "Temperature of conductive nanofilaments in hexagonal boron nitride based memristors showing threshold resistive switching", Advanced Electronics Materials, 2100580, 2021.

[Lanza2022] Mario Lanza, Abu Sebastian, Wei D. Lu, Manuel Le Gallo, Meng-Fan Chang, Deji Akinwande, Francesco M. Puglisi, Husam N. Alshareef, Ming Liu, Juan B. Roldan, "Memristive technologies for data storage, computation, encryption and radio-frequency communication", Science, 376, 6597, eabj9979, pp. 1-13, 2022.

[Larcher2015] F.M. Puglisi, P. Pavan, L. Larcher, A. Padovani, "Statistical analysis of random telegraph noise in HfO2-based RRAM devices in LRS", Solid-State Electronics, 113, 132-137, 2015.

[Lee2011] S.B. Lee, J.S. Lee, S.H. Chang, H.K. Yoo, B.S. Kang, B. Kahng, M.J. Lee, C.J. Kim, T.W. Noh, "Interface-modified random circuit breaker network model applicable to both bipolar and unipolar resistance switching", Appl. Phys. Lett. 98(3), 033502, 2011.

[Lee2015] J. S. Lee, S. Lee, T.W. Noh, "Resistive switching phenomena: A review of statistical physics approaches", Applied Physics Reviews, 2, 031303, 2015.

[Li2017] Y. Li, S. Long, Q. Liu, H. Lv, M. Liu, "Resistive Switching Performance Improvement via Modulating Nanoscale Conductive Filament, Involving the Application of Two-Dimensional Layered Materials", Small 13, 1604306, 2017.

[Menzel2015] S. Menzel, P. Kaupmann, R. Waser, "Understanding filamentary growth in electrochemical metallization memory cells using kinetic Monte Carlo simulations", Nanoscale, 7, 12673, 2015.

[Menzel2017] von Witzleben, M., Fleck, K., Funck, C., Baumkötter, B., Zuric, M., Idt, A., Breuer, T., Waser, R., Böttger, U., Menzel, S., "Investigation of the Impact of High Temperatures on the Switching Kinetics of Redox-Based Resistive Switching Cells using a High-Speed Nanoheater", Adv. Electron. Mater. 2017, 3, 1700294. https://doi.org/10.1002/aelm.201700294

[Maldonado2021] D. Maldonado, F. Aguirre, G. González-Cordero, A.M. Roldán, M.B. González, F. Jiménez-Molinos, F. Campabadal, E. Miranda, J.B. Roldán, "Experimental study of the series resistance effect and its impact on the compact modeling of the conduction characteristics of HfO2-based resistive switching memories", Journal of Applied Physics, 130, 054503, 2021.

[Maldonado2022] D. Maldonado, F. M. Gomez-Campos, M.B. González, A.M. Roldán, F. Jiménez-Molinos, F. Campabadal, E. Miranda, J.B. Roldán, "Comprehensive study on unipolar RRAM charge conduction and stochastic features, a simulation approach", Journal of Physics D: Applied Physics, 55, 155104, 2022.

View Article Online
DOI: 10.1039/D3MH01834B

[Mead1989] C. Mead and M. Ismail, “Analog VLSI Implementation of Neural Systems”, Springer, 1989.

[Merolla2014] P. A. Merolla, J. V. Arthur, R. Alvarez-Icaza, A. S. Cassidy, J. Sawada, F. Akopyan, B.L. Jackson, N. Imam, C. Guo, Y. Nakamura, B. Brezzo, I. Vo, S.K. Esser, R. Appuswamy, B. Taba, A Amir, M.D. Flickner, W.P. Risk, R. Manohar, D. S. Modha, “A million spiking-neuron integrated circuit with a scalable communication network and interface”, Science 345, pp. 668-673, (2014).

[Mikhaylov2021] A.N. Mikhaylov, D.V. Guseinov, A.I. Belov, D.S. Korolev, V.A. Shishmakova, M.N. Koryazhkina, D.O. Filatov, O.N. Gorshkov, D. Maldonado, F.J. Alonso, J.B. Roldán, A.V. Krichigin, N.V. Agudov, A.A. Dubkov, A. Carollo, B. Spagnolo, "Stochastic Resonance in a Metal-Oxide Memristive Device", Chaos, Solitons & Fractals, 2021.

[Miranda2010] E. Miranda, C. Walczyk, C. Wenger, and T. Schroeder, Model for the resistive switching effect in HfO2 MIM structures based on the transmission properties of narrow constrictions, IEEE Electron Device Lett 31, 609, 2010.

[Pan2014] F. Pan, S. Gao, C. Chen, C. Song, F. Zeng, "Recent progress in resistive random access memories: materials, switching mechanisms and performance", Materials Science and Engineering, 83, pp. 1-59, 2014.

[Pan2017] C. Pan, Y. Ji, N. Xiao, F. Hui, K. Tang, Y. Guo, X. Xie, F. M. Puglisi, L. Larcher, E. Miranda, L. Jiang, Y. Shi, I. Valov, P. C. McIntyre, R. Waser, and M. Lanza “Coexistence of Grain-Boundaries-Assisted bipolar and threshold resistive switching in multilayer hexagonal Boron Nitride”, Advanced Functional Materials, 27, 1604811, 2017.

[Pazos2023] S. Pazos, T. Becker, M. A. Villena, W. Zheng, Y. Shen, Y. Yuan, O. Alharbi, K. Zhu, J. B. Roldán, G. Wirth, F. Palumbo, M. Lanza, “Hardware implementation of a true random number generator integrating a hexagonal boron nitride memristor with a commercial microcontroller”, Advanced Functional Materials, in press, 2023.

[Perez2019] E. Pérez, D. Maldonado, C. Acal, J.E. Ruiz-Castro, F.J. Alonso, A.M. Aguilera, F. Jiménez-Molinos, Ch. Wenger, J.B. Roldán, "Analysis of the statistics of device-to-device and cycle-to-cycle variability in TiN/Ti/Al:HfO2/TiN RRAMs", Microelectronics Engineering, 214, pp. 104-109, 2019.

[Picos2015] R. Picos, J.B. Roldán, M.M. Al Chawa, P. García-Fernández, F. Jiménez-Molinos y E. García-Moreno, "Semiempirical Modeling of Reset Transitions in Unipolar Resistive-Switching based Memristors", Radioengineering Journal, 24, pp. 420-424, 2015.

[Prezioso2015] M. Prezioso, F. Merrikh-Bayat, B. D. Hoskins, G. C. Adam, K. K. Likharev, D. B. Strukov “Training and operation of an integrated neuromorphic network based on metal-oxide memristors”, Nature 521, pp. 61-64 (2015).

[Roldan2018] J.B. Roldán, E. Miranda, G. González-Cordero, P. García-Fernández, R. Romero-Zaliz, P. González-Rodelas, A. M. Aguilera, M.B. González, F. Jiménez-

DOI: 10.1039/D3MH01834B

Molinos, “Multivariate analysis and extraction of parameters in resistive RAMs using the Quantum Point Contact model”, Journal of Applied Physics, 123, 014501, 2018.

[Roldan2019] J.B. Roldán, F.J. Alonso, A.M. Aguilera, D. Maldonado, M. Lanza, “Time series statistical analysis: a powerful tool to evaluate the variability of resistive switching memories”, Journal of Applied Physics, 125, 174504, 2019.

[Roldan2021] J. B. Roldán, G. González-Cordero, R. Picos, E. Miranda, F. Palumbo, F. Jiménez-Molinos, E. Moreno, D. Maldonado, S. B. Baldomá, M. Moner Al Chawa, C. de Benito, S. G. Stavrinides, J. Suñé, L. O. Chua, “On the Thermal Models for Resistive Random Access Memory Circuit Simulation”, Nanomaterials, 11, 1261, 2021.

[Roldan2022] J. B. Roldan, D. Maldonado, C. Aguilera-Pedregosa, E. Moreno, F. Aguirre, R. Romero-Zaliz, A. García-Vico, Y. Shen, M. Lanza, Y. Yuan, M. Lanza, "Spiking neural networks based on two-dimensional materials", npj 2D Materials and Applications, 6, 63, 2022.

[Roldan2022b] J. B. Roldan, D. Maldonado, C. Aguilera-Pedregosa, F. J. Alonso, Y. Xiao, Y. Shen, W. Zheng, Y. Yuan, M. Lanza, "Modeling the variability of Au/Ti/h-BN/Au memristive devices", IEEE Transactions on Electron Devices, 70, 4, 1533-1539, 2022.

[Roldan2023] J.B. Roldán, E. Miranda, D. Maldonado, A.N. Mikhaylov, N.V. Agudov, A.A. Dubkov, M. N. Koryazhkina, M.B. González, M.A. Villena, S. Poblador, M. Saludes-Tapia, R. Picos, F. Jiménez-Molinos, S. G. Stavrinides, E. Salvador, F.J. Alonso, F. Campabadal, B. Spagnolo, M. Lanza, L.O. Chua, “Variability in resistive memories”, Advanced Intelligent Systems, in press, 2023.

[Romero-Zaliz2021] R. Romero-Zaliz, E. Perez, F. Jiménez-Molinos, C. Wenger, J.B. Roldán, “Study of quantized hardware deep neural networks based on resistive switching devices, conventional versus convolutional approaches”, Electronics, 10, 346, 2021.

[Ruiz-Castro2021] J. E. Ruiz-Castro, C. Acal, A.M. Aguilera, J. B. Roldan, "A Complex Model Via Phase-Type Distributions to Study Random Telegraph Noise in Resistive Memories", Mathematics, 9, 390, 2021.

[Sebastian2020] A. Sebastian, M. Le Gallo, R Khaddam-Aljameh et al., “Memory devices and applications for in-memory computing”, Nature nanotechnology 15, 529–544, 2020.

[Spiga2020] S. Spiga, A. Sebastian, D. Querlioz, B. Rajendran, “Memristive devices for brain-inspired computing”, Elsevier, 2020.

[Shi2018] Y. Shi et al., “Electronic synapses made of layered two-dimensional materials”, Nature Electronics, 1, 458–465, 2018.

[Vandelli2011] L. Vandelli, A. Padovani, L. Larcher, G. Broglia, G. Ori, M. Montorsi, P. Pavan, “Comprehensive physical modeling of forming and switching operations in HfO2 RRAM devices”, IEEE International Electron Devices Meeting, pp. 17-5, 2011.

View Article Online
DOI: 10.1039/D3MH01834B

[Vandelli2015] A. Padovani, Member, IEEE, L. Larcher, Member, IEEE, O. Pirrotta, L. Vandelli, G. Bersuker, Member, IEEE, “Microscopic Modeling of HfO x RRAM Operations: From Forming to Switching”, IEEE Transactions on Electron Devices, 62(6), pp. 1998-2006, 2015.

[Video] https://youtu.be/Ksivb2vHtv4

[Wei2016] Z. Wei et al., "True random number generator using current difference based on a fractional stochastic model in 40-nm embedded ReRAM," 2016 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, pp. 4.8.1-4.8.4, 2016. DOI: 10.1109/IEDM.2016.7838349

[Yang2020] C.-F. Yang et al., “Industrially applicable read disturb model and performance on Mega-bit 28nm embedded RRAM,” in Proc. IEEE Symp. VLSI Technol., 2020.

[Yu2011] S. Yu, Y. Wu, R. Jeyasingh, D. Kuzum, H.-S. Wong, “An electronic synapse device based on metal oxide resistive switching memory for neuromorphic computation”, IEEE Trans. Electron Devices, 58 (8), pp. 2729–2737, 2011. doi: 10.1109/TED.2011.2147791.

[Zhu2023] K. Zhu, S. Pazos, F. Aguirre, Y. Shen, Y. Yuan, W. Zheng, O. Alharbi, M. A. Villena, B. Fang, X. Li, A. Milozzi, M. Farronato, M. Muñoz-Rojo, T, Wang, R. Li, H. Fariborzi, J. B. Roldan, G. Benstetter, X. Zhang, H. Alshareef, T. Grasser, H. Wu, D. Ielmini, M. Lanza, “Hybrid 2D/CMOS microchips for memristive applications”, Nature, 618, 57–62, 2023.

[Zidan2018] M. A. Zidan, J. P. Strachan and W. D. Lu, “The future of electronics based on memristive systems”, Nature Electronics, 1, 22-29, 2018.