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Graphene-on-Silicon Hybrid Field-Effect Transistors

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The combination of graphene and silicon in hybrid electronic devices has attracted increasing attention over the last decade. Here, a unique technology of graphene-on-silicon heterostructures as solution-gated transistors for bioelectronics applications is presented. The proposed graphene-on-silicon field-effect transistors (GoSFETs) are fabricated by exploiting various conformations of channel doping and dimensions. The fabricated devices demonstrate hybrid behavior with features specific to both graphene and silicon, which are rationalized via a comprehensive physics-based compact model which is purposely implemented and validated against measured data. The developed theory corroborates that the device hybrid behavior can be explained in terms of two independent silicon and graphene carrier transport channels, which are, however, strongly electrostatically coupled. Although GoSFET transconductance and carrier mobility are found to be lower than in conventional silicon or graphene field-effect transistors, it is observed that the combination of both materials within the hybrid channel contributes uniquely to the electrical response. Specifically, it is found that the graphene sheet acts as a shield for the silicon channel, giving rise to a nonuniform potential distribution along it, which impacts the transport, especially at the subthreshold region, due to non-negligible diffusion current.

1. Introduction

Silicon has been the cornerstone of micro- and nanoelectronics for the last half a century, with silicon-based field-effect transistors (SiFETs) evolving from rudimentary and bulky into sub 3 nm dimensions.[1,2] This continuous downsizing has brought numerous advantages but also relevant challenges, coming hand-in-hand with the conception of novel and varied applications.[3–6] Among them, biosensing and bioelectronic applications have been successfully explored [7,8], e.g., employing functionalized specific biomarkers on SiFETs surface, enabling selective label-free detection.[9,10] Silicon has also been utilized for numerous in vitro recordings of electrogenic cells (cardiac or neural) or even in vivo mapping of the whole brain.[11,12] However, it is known to be a bioresorbable material that degrades over time once immersed in saline, thus, suffering from a limited operation time for in vivo applications.[13,14]

While silicon still dominates the industrial semiconductor scene, a new material has emerged rather recently, transforming materials science: graphene. Accompanied by other two-dimensional (2D) materials, graphene has already opened new prospects in modern nanoelectronic applications[15–18] and also holds a great promise for bio- and neuro-applications due to its extraordinary conductivity and good biocompatibility.[19–21] In particular, graphene-based FETs (GFETs) and microelectrode arrays (MEAs), both rigid and flexible, have been reported to successfully interface with electrogenic cells

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as well as live tissues.[22–24] However, the absence of a bandgap on graphene results in large "off" state currents, and the effect of a non-negligible quantum capacitance limiting effective out-of-plane electrical coupling to the biomolecules or electrostatic potentials created by the cells.[25]

In this work, we propose to merge silicon and graphene FETs, creating a so-called Graphene-on-Silicon FET (GoSFET). In particular, we aimed to leverage the advantages of both materials in a unique device, seeking its application in biosensing and bioelectronics. For this purpose, we investigated the GoSFET performance when it is electrically gated via an electrolyte.

Graphene has already been combined with: i) other 2D materials in numerous and varied heterostructures (e.g., with molybdenum disulfide (MoS_2),[26,27]) with weak van der Waals forces controlling the interaction, as well as ii) with silicon, where a significantly more relevant interaction arises resulting in a hybrid channel. In this latter case, the hybrid channel has already been exploited, for example, to demonstrate ultrasensitive and fast photoresponse;[28,29] or radiofrequency devices,[30] where the bare silicon substrate without an insulating layer was used passively.

In our work, on the contrary, we go a step further with both graphene and silicon channels contributing to the active charge transfer, seeking to build a more robust device with: i) a high on/off conductance ratio due to silicon, and ii) a high conductivity, transconductance, and environmental stability due to graphene. Our experimental findings reveal a hybrid behavior, indeed, although the combination of both channel materials results in poorer performance of the hybrid device than what would be expected from the advantages of the isolated materials.[31–33]

Nonetheless, the resulting structures can be exploited for complex biosensing where graphene and silicon are functionalized for the detection of separate analytes within one substance, which turns relevant the investigation of the potential sensing performance of these hybrid devices. To this aim, we have performed electrical transport characterization of the GoSFETs, including a statistical analysis to comprehend the feasibility of these devices for this targeted application.

In order to reach a deeper understanding of the working principles of the hybrid electrolyte-gated device, the GoSFETs are fabricated in different layouts with varying material-width proportions. Concomitantly, we pursue to rationalize the results and shed light on the charge transfer phenomena by developing a comprehensive physics-based model of GoSFETs that comprises the electrostatics and the charge transport description of the heterostructure. The estimated electrical properties of the electrolyte-gated GoSFETs model correlate very well with the experimental results, evidencing that the placement of graphene directly on top of the silicon results in a strong screening effect (of the electrolyte gate) that produces a heavy non-uniform charge distribution along the silicon channel, which eventually impacts and explains the GoSFET performance.

2. Results and Discussion

2.1. Experimental

The graphene-on-silicon field-effect transistors consist of a conventional SiFET where the top-gate metal-insulator interface is substituted by a graphene sheet, which is in turn electrostatically controlled by a reference electrode immersed into an electrolyte solution placed on top of the graphene channel. A schematic depiction of the fabricated GoSFET can be found in **Figure 1**a. The graphene is laterally contacted with metal stacks of Ti/Au, which are on top of the highly doped drain and source edges of the silicon channel forming the drain (V_D) and source (V_S) electrodes. The electrostatic modulation of the carrier concentration in both graphene and silicon channels is achieved via liquid gating (V_{LG}).

We fabricate four wafers with arrays of 32 GoSFET chips, each of them featuring an array of 14 transistors. To study the interaction between channel material layers, we use different layouts defining the size of the Si and graphene channels. In some cases, graphene has precisely the same size as silicon, while in other samples, it is up to 20 times narrower (see Table S1, Supporting Information). As a base for the device fabrication, we use mildly p-doped SOI wafers ($\rho \approx$ 14–18.9 Ωcm). First, we employ a thermally grown SiO_2 hard mask prepatterned utilizing photolithography and CHF_3 plasma etching for silicon nanoribbons formation. Then, following the silicon etching in a solution of tetramethylammonium hydroxide (TMAH), drain-source regions on half of the devices are doped with arsenic and another half with boron. The resulting inversion- (n^+–p–n^+) and accumulation- (p^+–p–p^+) mode SiFETs are contacted by metallization using the TiN and Al compound

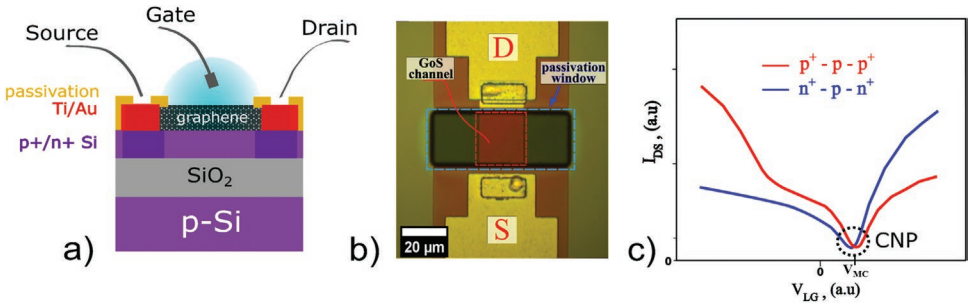

Figure 1. a) Cross-sectional schematic of the GoSFET device. Silicon is color-coded in violet (or dark violet for high-doped regions), metal in red, and passivation in yellow. b) Optical photograph of the GoSFET channel (red dashed line), with passivation window (blue dashed line). Passivated feedlines (yellow) on top of the mesa structure (red) contact the combined channel from the bottom and top part of the photograph. c) Illustrative comparison of $I_{DS} - V_{LG}$ characteristics for two kinds of GoSFET devices explored in this work, p^+–p–p^+ (red) and n^+–p–n^+ (blue), where the charge neutrality point (CNP) and minimum current-voltage (V_{MC}) of the hybrid silicon-graphene channel are highlighted.

(small squares on the feedlines from the top and bottom part of Figure 1b). Then, Ti/Au metallization of the whole feedlines is performed. Next, the CVD-grown graphene is transferred onto the Si substrate using the "fishing" technique, and it is patterned with oxygen plasma before a second metallization. Once graphene is sandwiched with the second metallization, its contact resistance is expected to be ≈5.3 kΩ·μm (with standard deviation (SD), SD = 1.55 kΩ μm), as previously reported for the same fabrication technology of graphene transistors.[32] For fabricated silicon nanowires, the typical contact resistance lies in the range of 32.1 kΩ μm (SD = 11.9 kΩ μm).[34] Therefore, can arise a question of an immense imbalance between graphene and silicon contact resistances in the resulting GoSFET structures. However, the impact of contact resistances imbalance on the electrical measurements is expected to be negligible because of the significant difference (two-three orders of magnitude) between the magnitude of the channel and contact resistivities in our devices, as we discuss later during electrical analysis.

At the final fabrication step, the devices are passivated so that only the channel is in direct contact with the liquid electrolyte. An illustrative view of the cross-section of the fabricated devices can be found in Figure 1a. At the same time, Figure 1b shows an optical photograph of an original GoSFET after the passivation, with a visible window opening in the middle.

A first comparison of the discovered similarities and differences between p^+–p–p^+ and n^+–p–n^+ based GoSFETs can be realized from their illustrative typical *I*–*V* transfer characteristics (plotted on the same linear scale) shown in Figure 1c.

The minimum conductivity point, namely the charge neutrality point (CNP), occurs for a positive gate voltage (V_{MC}), which indeed is quite similar in both structures. The origin of V_{MC} has been reported in the case of isolated graphene on top of a SiO_2-substrate in Ref. [35]: it is due to a weak *n*-doping caused by adsorbates or adsorbates attachment to silanol (SiOH) groups at the graphene/SiO_2 interface.

In addition, we observe that both structures show a rapid increase in the current for an applied potential on the opposite sides of V_{MC}. For accumulation GoSFETs, this occurs under voltages $V_{LG} < V_{MC}$, similar to the on-state of p^+–p–p^+ SiFETs, while in the case of inversion GoSFETs, the current rises under voltages $V_{LG} > V_{MC}$, witnessing the n^+–p–n^+ SiFET base of this type of the devices. This is later confirmed by the theoretical model. So in both cases, it is observed that hybridized transistors combine typical unipolar silicon behavior with ambipolar graphene. Thus, to discuss further experimental results, we introduce two regions in the characteristics as graphene-like and silicon-like parts **Figure 2**a,d. But one still has to keep in mind that the channel current in these devices is never contributed solely to graphene or silicon but as a result of their combination. This discussion is later completed and spelled out in Sections 2.3 and 2.4, where a physics-based model of the hybrid GoSFET is developed and exploited to analyze the contribution of graphene and silicon current into the particular shape of the

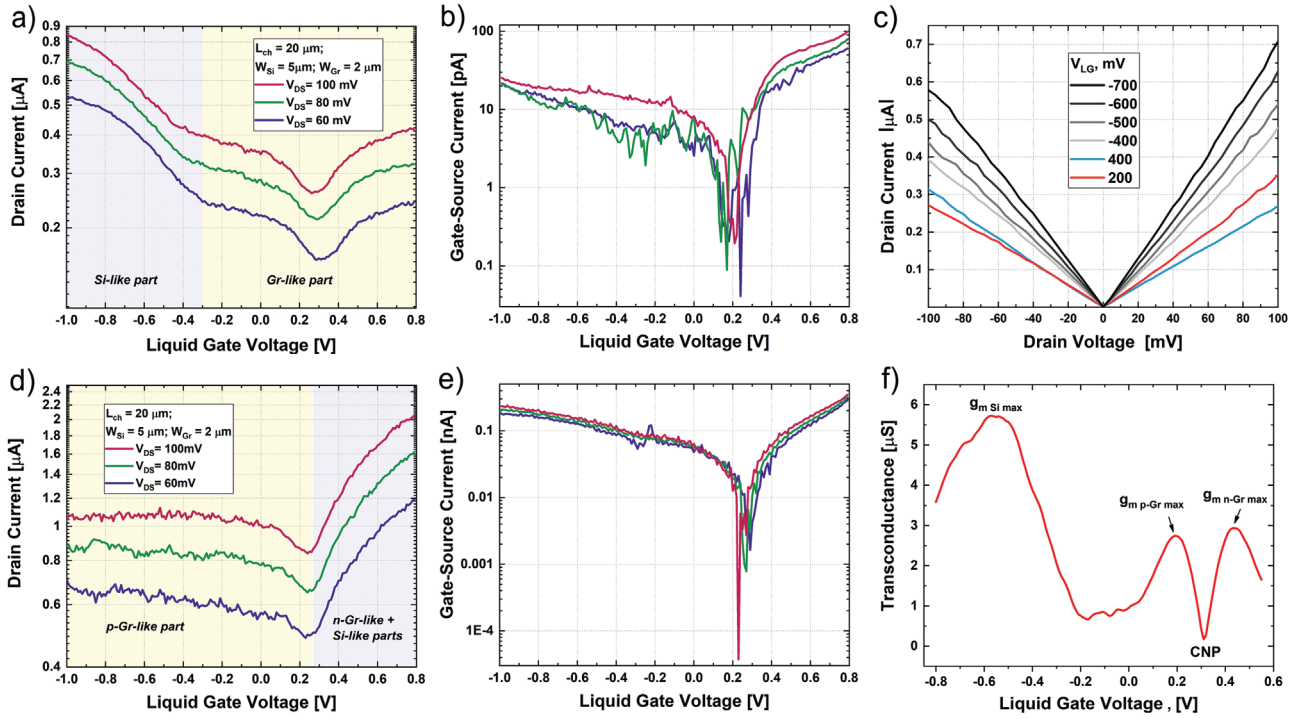

Figure 2. a) Transfer characteristics I_{DS}-V_{LG} of a p^+–p–p^+ GoSFET under different drain bias voltages and b) leakage gate current $I_{GS} - V_{LG}$ with corresponding color labeling. c) Output characteristics $|I_{DS}|$-V_{DS} of the same device, with red and blue colors representing current in the linear part of the hole and electron conduction of graphene. The gradual change of the current level in the linear part of the silicon conductive region is shown in shades of black. d) Transfer I_{DS} - V_{LG} characteristics of n^+ – p – n^+ based GoSFET under various drain voltages, and e) corresponding leakage current $I_{GS} - V_{LG}$. f) Typical transconductance curve for p+ – p – p+ devices in absolute value. Here $g_{m\ Si\ max}$ indicates the transconductance maximum of the silicon-like part of the channel; $g_{m\ p\text{-}Gr\ max}$ is the transconductance maximum for hole carriers in graphene-like behavior, and $g_{m\ n\text{-}Gr\ max}$ for electrons.

transfer characteristics. Indeed, from the model, we corroborate that graphene and silicon channels are electrostatically coupled, and the particular shape of transfer curves is thus a combination of the transport of both materials that, however, cannot be strictly conceived into graphene and silicon currents.

The experimental transfer curves of GoSFETs are obtained by sweeping the liquid gate voltage V_{LG} while the bias voltage V_{DS} between drain-source electrodes is fixed at 100 mV. The resulting current (Figures 2a,d) for both structures shows a low on/off current ratio, i.e., the hybrid channel cannot be properly switched off, which, in principle, evidences the impact of graphene, although we will later reveal from the theoretical model some non-obvious transport nuances in the hybrid channel.

Together with the experimental I_{DS}–V_{LG} characteristics, we demonstrate that the leakage current for GoSFETs (Figures 2b,e) is lying in the range of hundreds of pico-amps, which are negligibly small values compared to the drain-to-source currents. Besides, Figure 2c shows the output characteristics of the accumulation mode GoSFET in which the drain-source current $|I_{DS}|$ is recorded as a function of drain-source voltage V_{DS} in the regions of both graphene-like (V_{LG} = 200 mV and 400 mV) and silicon-like parts (V_{LG} from –700 to –400 mV), evidencing a linear behavior.

Next, we extract the device performance for p$^+$–p–p+-based devices, including the transconductance and mobility, for a set of 20 transistors. The transconductance defines the change in current as a response to change in gate potential, which is the essence of any liquid-gated biosensor; hence it is an important figure-of-merit for GoSFET biosensors. A typical transconductance curve ($g_m = dI_D/dV_{LG}$) for p$^+$–p–p$^+$ heterostructures can be found in Figure 2f. Here it is worth to notice, that we conceptually connect the g_m peaks to a particular transport regime of the hybrid $I_{DS} - V_{LG}$ characteristic in Figure 2a. In contrast, the transconductance itself is not directly explainable in terms of one of the channel materials but as the combined effect of both (see Section 2.3.) This is done in order to analyze the GoSFETs performance, where the two regions with graphene-like and silicon-like behavior are compared.

The silicon-like part of I–V characteristics demonstrates an average maximum transconductance, normalized over the bias voltage (V_{DS}), in the range of 51.4 µS V^{-1}, with a standard deviation of SD = 51.8 µS V^{-1}. For the graphene-like behavior, the transconductance was estimated separately for both types of carriers. Thus, the attained mean value of the bias normalized hole transconductance maximum is 20.1 µS V^{-1} (SD = 22.7 µS V^{-1}), while for electrons, its value is somewhat higher, 33.6 µS V^{-1} (SD = 41.5 µS V^{-1}). Chartboxes with the statistical data for graphene-like and silicon-like maximum transconductance are provided in **Figure 3**a (where some data points are missing since, for some of the devices, it was not possible to extract the transconductance maximum due to the noise. In both cases, the values are significantly lower than those achieved in conventional GFETs or SiFETs.[31–33]

Furthermore, we show that the maximum transconductance of GoSFETs has a particular dependency on the channel geometry (Figures S2-S4, Supporting Information). A somewhat positive correlation can be tracked between transconductance at the silicon-like behavior part and silicon width in Figure S2a, Supporting Information. Also, it should be noted that, for graphene-like behavior, both hole and electron transconductances also have a positive trend across silicon width (Figures S3-S4, Supporting Information). Besides, a positive correlation can be observed between n-graphene and the width-to-length silicon ratio (Figure S4b, Supporting Information). These dependencies are indirect evidence of the hybrid nature of the CNP vertex, what with more details explained later in Section 2.3.

In addition to the transconductance analysis, we estimate the carrier mobility for the graphene-like part of the channel from the DC measurements:[32]

$$\mu = \frac{L}{W} \cdot \frac{g_m}{C_{int} V_{DS}} \tag{1}$$

where L and W are the channel length and width, respectively, and C_{int} represents the interface capacitance.

The average value of graphene-like hole region maximum mobility is 15.4 cm^2 V^{-1} s^{-1} (SD = 13.8 µS V^{-1}), while the electron region of the characteristics shows a higher value, 23.1 cm^2 V^{-1} s^{-1} (SD = 17.9 µS V^{-1}). In both cases, to extract the maximum mobility, the interface capacitance was assumed to be $C_{int} \approx$ 2.1 µF cm^{-2}, according to the theoretical model (see Section 2.2). Chartboxes of maximum mobility values for all measured transistors can be found in Figure 3. Since W/L ratio is used to calculate carrier mobility, the final values are inde-

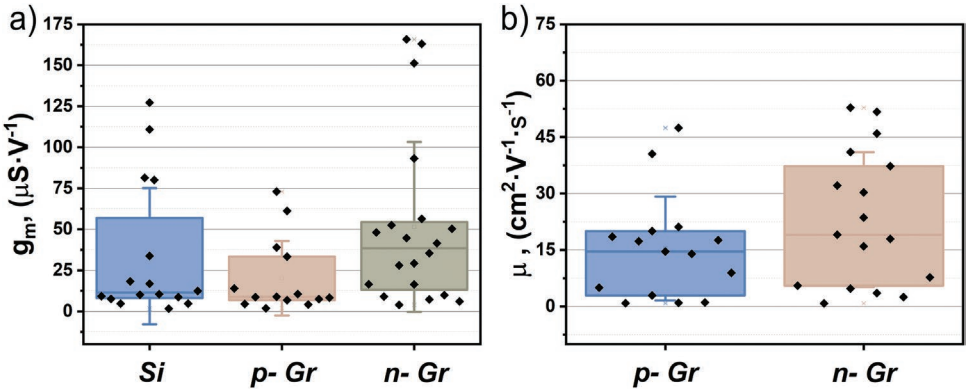

Figure 3. a) Transconductance maximum statistics from a set of p$^+$ – p – p$^+$ transistors. b) Hole and electron maximum mobility comparison, estimated for the graphene-like part of the characteristics of GoSFETs.

Table 1. Mobility of Accumulation-Mode GoS and Some Representative 2D Materials at 300 K.

Material	μ^e, cm^2 V^{-1} s^{-1}	μ^h, cm^2 V^{-1} s^{-1}	ref
GoS	23.1	15.4	this work
Graphene	7.8×10^3	6.2×10^3	[36]
MoS_2	200	152	[37]
WS_2	120	210	[37]

pendent of channel geometry (see Figures S5-S6, Supporting Information). As well as for the transconductance, GoSFETs graphene-like part carrier mobility is significantly lower compared to conventional devices.[31–33] In **Table 1**, we compare the carriers' mobility of GoSFETs to the carriers' mobility in electrolyte-gated graphene and two other 2D materials such as molybdenum disulfide (MoS_2) and tungsten disulfide (WS_2) that are often used for fabrication of hybrid devices.

As we already mentioned at the beginning of the subsection, an immense imbalance between the contact resistance of the channel materials can be observed. However, due to the low mobility of the graphene channel, we can safely assume that the impact of metal-graphene contact resistance in the overall graphene current is negligible. This aspect is particularly relevant as the analysis proposed in the following subsection did not consider significant differences in the contact properties of the graphene and silicon channels. While this assumption is common in silicon-metal contacts (which have been technologically optimized for decades and currently do not impact the silicon transport characteristics), in the case of graphene, the state-of-the-art metal-graphene contact resistances are far from being optimal and constitute crucial and undesirable elements degrading the performance of graphene devices. However, because of the low graphene mobility observed in our fabricated devices, in the order of tens of cm^2/Vs (see Figure 3b), the graphene channel resistivity is quite high, in the order of hundreds of kΩ·µm, which is two/three orders of magnitude higher than the expected edge-contact resistivity; allowing to neglect them in the graphene transport and disregard any differences between silicon and graphene currents arising from the contact resistances dissimilarities.[38–43]

Nevertheless, the contact resistance imbalance still can contribute to the rapid degrading that was revealed and tracked within several rounds of measurements for some of the devices. We studied the degradation process via consecutive I_{DS}-V_{GS} measurements (inset in **Figure 4**) and transferred them into the evolution of the transconductance maximum according to the first I_{DS}-V_{GS} sweep (Figure 4).

The upgoing trend in the first measurements can be explained by the elimination of the remnants of fabrication residues adhered to the channel material's surface. Then, the transconductance is gradually degraded for both, graphene-like and silicon-like regions, until graphene-like transconductance becomes undetectable (at this point, the CNP cannot be identified). Our assumption is that graphene is degrading, and once it gets fused, the overall device performance declines. Experimentally we show this behavior via Raman spectroscopy of the graphene surface before and after degradation. The Raman spectra on the newly fabricated GoSFETs demonstrate strongly pronounced G and 2D band signals originating from the monolayer graphene (blue line in **Figure 5**a). Simultaneously, Raman spectra acquired from the degraded devices produce only minor signs of the G band peak, while the 2D band peak is almost completely vanished (yellow line in Figure 5a). From the gained spectra for both cases, we managed to develop footprints of the graphene with weighting factors for each pixel (Figure 5b,c).

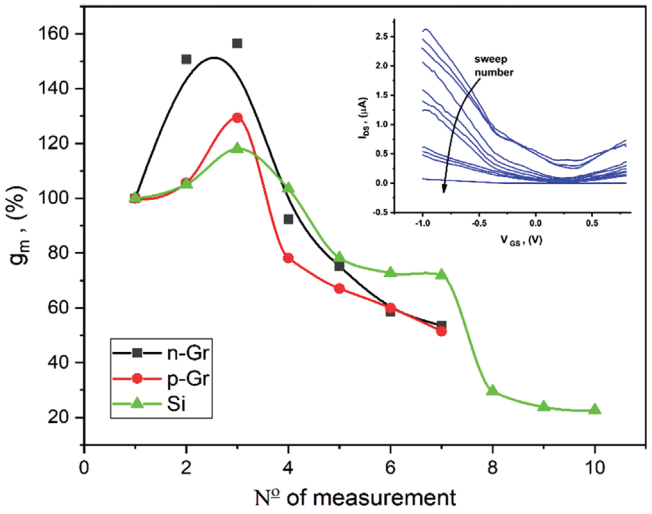

Figure 4. Extracted transconductance versus the number of measurements demonstrating gradual degradation of the device and corresponding *I–V* measurements taken under 100 mV bias (inset). Here silicon-like transconductance is color-coded in green, while graphene-like electron and hole transconductance are color-coded in black and red, respectively. Results are displayed as a percentage ratio of the transconductance achieved in the first sweep.

The intensity ratio I_D/I_G of the fitted Gaussians for D and G peaks lies mostly below 1 (blue regions in Figure 5b), indicating good quality low-defect graphene in the working device; on the other hand, the device degraded after many measurements cycles featuring I_D/I_G ratio >2 indicating the presence of numerous defects in the material [44,45], and even a transformation of the graphene layer into scattered carbon clusters (yellow regions in Figure 5c), which is indicative of destructed graphene.

Since the quick degradation is not observed in conventional liquid-gated GFETs, we assume that the doping of the silicon substrate can potentially play a significant role in the graphene degradation observed in GoSFETs. It is well known that the bonding between graphene and various substrates is typically mediated by relatively weak van der Waals forces.[46,47] At the same time, p-type doping of the silicon with boron results in an excess of positively charged carriers (holes) in the silicon. Hypothetically, this can affect the adhesion of graphene to the substrate by reducing the number of available bonding sites on the silicon interface hence reducing the adhesion and favoring partial detachment of the graphene from the substrate. This poor adhesion and the associated detachment in the presence of dissolved oxygen in the electrolyte, reported as an origin of leakage current in GFETs [45], can result in reduced graphene stability, integrity, and subsequent performance degradation. The work considers the graphene electrochemical window, used reference electrodes, and electrolytes. Besides, in regular conditions, graphene serves as an excellent barrier material

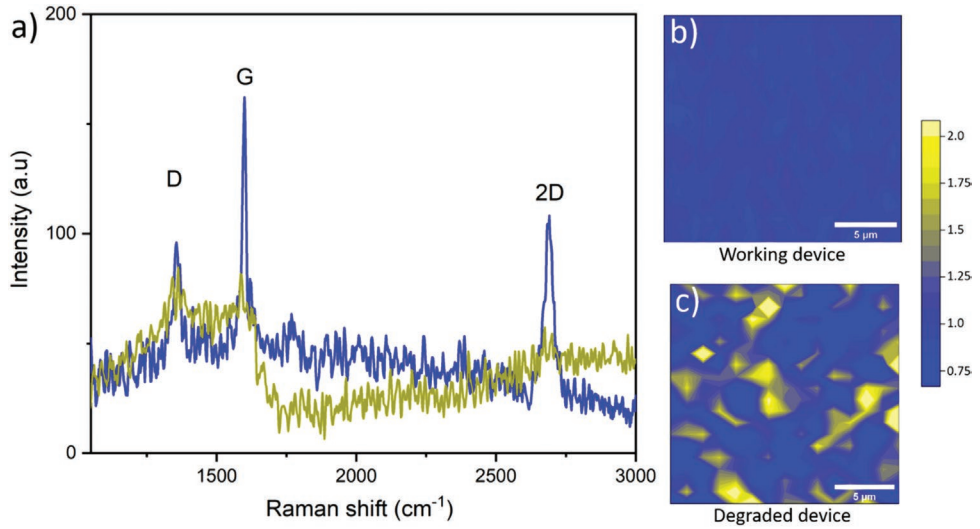

Figure 5. Raman spectra of graphene on GoSFETs a) before (blue curve), and after performance degradation (yellow curve) and corresponding graphene channel footprints b,c) of the intensity ratio ID/IG of the fitted Gaussians for D and G peaks. The measured area is 20 µm × 20 µm, scale bars: 5 µm.

for protecting substrate, preventing its oxidation/degradation. For graphene poorly attached to the silicon surface, the underlying silicon may contact to the buffer solution. This may promote certain electrochemical reactions that would lead to the graphene degradation. Therefore, the substrate doping effect on graphene adhesion and further strategies to overcome this challenge should be next stages of the study. One of the possible solutions could be the fabrication of an additional 5 nm SiO_2 isolating layer between graphene and silicon channels that would guarantee a reasonable adhesion between materials and prevent silicon from interaction with a liquid.

2.2. Electrostatics of Liquid-Gated GoSFETs

To rationalize the experimental measurements and give insights into the physics at play, we have implemented a comprehensive physics-based electrical model of GoSFETs. The model reproduces to an excellent agreement (maximum average relative error of 7.5%) with the experimental electrical readouts and provides an in-depth description of the device's electrical behavior supporting the interpretation of the measurements.

As already mentioned in the experimental section, the electrostatic modulation of the carrier concentration in the hybrid GoSFET channel is achieved via the reference electrode (V_{LG}) immersed into the aqueous solution. To understand the dependence of the carrier density in graphene and silicon with the reference electrode potential, we first deal with the charge distribution at the graphene/electrolyte interface.[48] In particular, it is crucial to properly model the capacitance at such an interface to accurately relate the charge carrier density induced in graphene and silicon with the electrode potential. The interfacial capacitance can be split into three contributions, as represented in the equivalent capacitive circuit of GoSFETs shown in **Figure 6**a: a double layer capacitance (C_{DL}), a Stern capacitance (C_{Stern}), and a gap capacitance (C_{gap}). C_{DL} accounts for the electrical double layer that appears at the electrolyte/graphene interface[49] and ranges from a few µF/cm^2 to a few hundred of µF/cm^2 depending on the metal electrodes or the ionic concentration of the electrolyte.[49,50] C_{Stern} models the region depleted of ionic charges close to the surface [51–53], with values also varying among tens of µF/cm^2.[54] Finally, C_{gap} considers the hydrophobic nature of the graphene surface and the consequent changes in the electrolyte close to it:[55] as demonstrated by molecular dynamics simulations,[53] the density of water decreases strongly at the surface resulting in a so-called hydrophobic gap between the solid and the electrolyte. In this gap, the effective dielectric constant is smaller than in bulk water, resulting in a significant potential drop at the interface. A hydrophobic gap of 0.31 nm and a relative dielectric constant of 1 is considered,[31,32] resulting in $C_{gap} \approx 2.1$ µF cm^{-2}.

The series combination of C_{DL}, C_{Stern}, and C_{gap} results in an equivalent interfacial capacitance (C_{int}) which is dominated by C_{gap}, with a capacitance value around one order of magnitude lower than C_{DL} and C_{Stern} given that the ionic concentration, i_0, is at least 10 mM. Thus, the electrode-electrolyte-hydrophobic gap heterostructure acts as an effective capacitance $C_{int} = (C_{DL}^{-1} + C_{Stern}^{-1} + C_{gap}^{-1})^{-1} \approx C_{gap}$, where an effective potential, $-\Psi_0$, drops across the electrolyte/graphene interface,[32] resulting in an effective gating $V_G = V_{LG} + \Psi_0$. The potential Ψ_0, according to the site-binding theory,[56] is dependent on pH, ionic concentration, the density of surface ionizable sites, and dissociation constants.[57,58] Here Ψ_0 is considered as a gate offset bias as the electrolyte characteristics are not modified during the experimental measurements.

The next region in the device heterostructure is the graphene-silicon interface. To model it, we consider the formation of an interfacial silicon-graphene dipole layer within an equilibrium separation distance, $t_{eq} = 0.6$ nm[43,59] and a relative dielectric constant of 1 (resulting in $C_{dip} \approx 1.5$ µF cm^{-2}). In this regard, the 1D electrostatics is analyzed by solving the Gauss' law (see Methods) across the electrode-electrolyte-hydrophobic gap-graphene-dipole layer-silicon heterostructure shown in Figure 6b. The electrostatics of the GoSFET is then described

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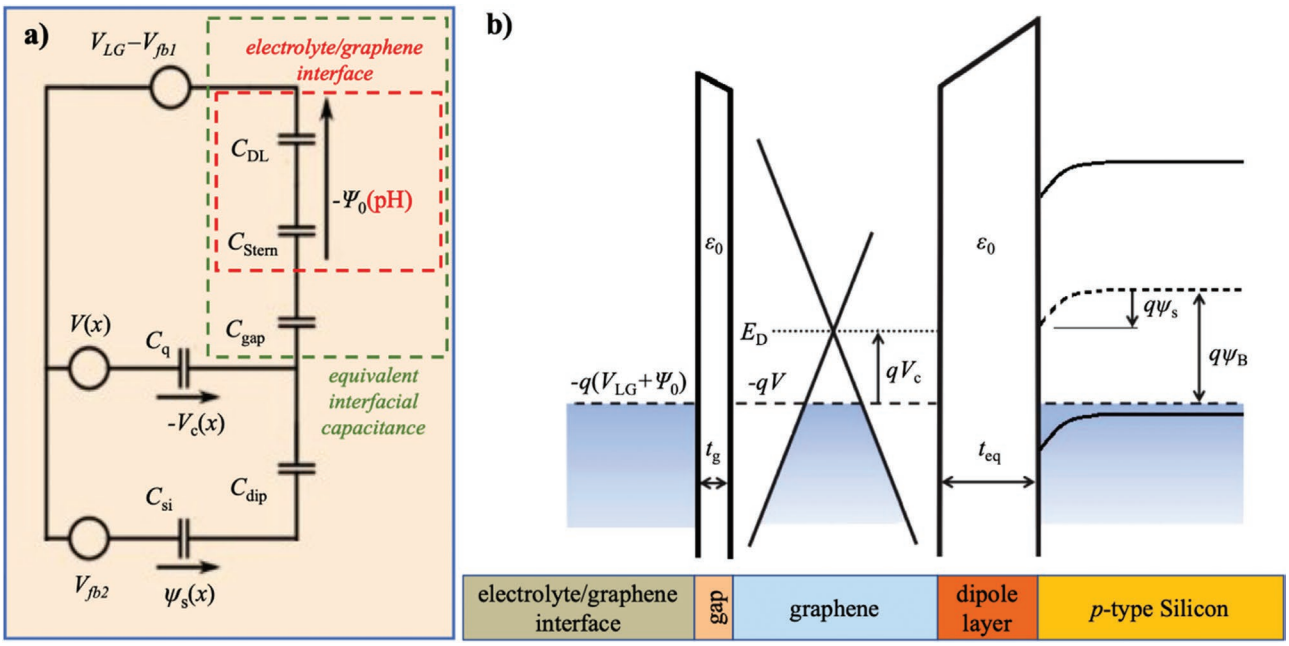

Figure 6. a) Equivalent capacitive circuit of an electrolyte-gated GoSFET. b) Sketch of the band diagram of the electrolyte-hydrophobic gap-graphene-dipole layer-silicon heterostructure in equilibrium (V_{LG} = 0 V). At the graphene channel, $E_D = -q(V\text{-}V_c)$ is the Dirac energy, $-qV$ is the graphene Fermi level, and V_c is the graphene chemical potential. At the silicon channel, $q\psi_B$ is the difference between the Fermi level and the intrinsic Fermi level; and ψ_s is the surface potential.

using the equivalent capacitive circuit depicted in Figure 6a, where $C_q = \partial Q_{net}/\partial V_c$ represents the quantum capacitance of graphene,[60] while $C_{si} = -\partial Q_{si}/\partial \psi_s$ is the intrinsic silicon capacitance,[61] accounting for the 2D and 3D finite density of states of graphene and silicon, respectively.

A study of the gate voltage dependence of the relevant capacitances of the accumulation and inversion GoSFETs is addressed in (Figure S8b and Figure S10b, Supporting Information). It is worth noting that Equation (2) (see Methods) resembles the electrostatics of a dual-gated GFET[62] where the role of the top (back) insulator is played by the hydrophobic gap (dipole layer) and the effective top (back) gate voltage is $V_{LG} + \Psi_0 - V_{fb1}$ ($\psi_s + V_{fb2}$). In addition, Equation (2) solves the electrostatics of a common SiFET[61] but gated by the graphene potential $V\text{-}V_c$ and substituting the insulator with a dipole layer. This way, the electrostatics of a hybrid GoSFET can be understood as the self-consistent solution of both GFET and SiFET devices. The analytical equations used to solve Equation (2) can be found in Note S1, Supporting Information.

2.3. Drift-Diffusion Transport Along the Graphene-Silicon Channels

Given that the length of the fabricated devices ranges from 5 to 20 µm, it is reasonable to assume that the mean free path of carriers is much shorter than the channel length, and the drift-diffusion theory is the appropriate framework to describe the electrical transport. In this regard, the drain current can be written in the form $I_{DS} = WQ_t(x)\mu(x)\mathrm{d}V(x)/\mathrm{d}x$, where W is the gate width; Q_t is the mobile charge density; and μ is the carrier mobility. We assume that graphene and silicon behave as two independent transport channels, i.e., the flow of current or tunneling between the inversion (accumulation) channel formed at the silicon surface and at the graphene sheet is negligible in comparison with the longitudinal current along each of them.

In graphene, ambipolar Q_t can be expressed as a quadratic polynomial dependent on the chemical potential V_c,[63,64] while symmetrical electron and hole mobility are considered independent of the applied electric field, carrier density, or temperature. On the other hand, Q_t in silicon arises from the inversion in the $n^+ - p - n^+$ GoSFET (or accumulation in the $p^+ - p - p^+$ GoSFET) channel charge density; with mobility $\mu_{e,Si}$ ($\mu_{h,Si}$) for electrons (holes). Analytical expressions for the calculation of the graphene and silicon currents for both inversion/accumulation regimes of GoSFETs are provided in Note S2, Supporting Information.

2.4. Theoretical Interpretation of Experimental Data

We exploited the implemented model to explain the physics at play in the experimental device realizations. For this purpose, we employed the electrical and physical parameters collected in **Table 2** as extracted for the $p^+ - p - p^+$ GoSFET. In particular, the experimental device of choice comprised a 20 µm-long and 2 µm-wide graphene sheet covered on top with the electrolyte, with an offset voltage V_{fb1} = 0.3 V, i.e., it is *p*-type in equilibrium. Notably, the residual charge density reaches 1.7×10^{13} cm^{-2}, and the mobility is low (μ_g = 10 cm^2 Vs^{-1}), meaning that the graphene sheet is highly contaminated and the carriers suffer from frequent scattering. The former can be produced by charged impurities and a highly corrugated silicon surface,[65,66] while the latter might be due to a high residual carrier concentration in the channel,[67] remote phonons, and

Table 2. p^+–p–p^+ GoSFET model parameters.

Graphene		Silicon			
L (µm)	20	L (µm)	20	C_{DL} (µF cm^{-2})	23
W_g (µm)	2	W_s (µm)	2	C_{Stern} (µF cm^{-2})	20
V_{fb1} (V)	0.3	V_{fb2}–V_D (V)	–0.23	C_{gap} (µF cm^{-2})	2.86
μ_g (cm^2 Vs^{-1})	10	$\mu_{h,Si}$ (cm^2 Vs^{-1})	400	C_{dip} (µF cm^{-2})	1.48
σ_{pud}/q (cm^{-2})[a)]	1.7×10^{13}	N_A (cm^{-3})	4×10^{15}	T (K)	300

[a)] σ_{pud} is the residual charge density due to electron-hole puddles (see Note S2, Supporting Information).

the high electrostatic coupling given that the graphene sheet is sandwiched between the silicon surface charge and the electrical double layer originated at the electrolyte interface.[68] The silicon channel has equal dimensions (20 µm-long and 2 µm-wide), and it consists of a *p*-type substrate with acceptor concentration $N_A = 4 \times 10^{15}$ cm^{-3} and hole mobility of $\mu_{h,Si} = 400$ cm^2 Vs^{-1}. The electrolyte is a 1xPBS, so a C_{DL} of 23 µF cm^{-2} is assumed (calculated from site-binding theory[57]), while C_{Stern} of 20 µF cm^{-2} was taken.[54]

Figure 7a shows the simulated transfer characteristics of the accumulation GoSFET together with the experimental measurements. The model is able to reproduce to an excellent agreement the experimental results (maximum average relative error of 7.5%) with the shape of the experimental data showing a hybrid behavior where the point of minimum conductivity (V_{MC}) is highlighted. Some deviation between the simulated and measured data is observed around $V_{LG} \sim -0.5$ V. Specifically, we observe from measurements a more pronounced change in the current at such gate voltage. This deviation is originated from a theoretical overestimation of the transport charge density. This issue is thoroughly commented in Note S3, Supporting Information, but it does not significantly affect the explanation of the physical operation of the device.

The contributions of graphene and silicon channels to the theoretical current of the p^+ – p – p^+ GoSFET for $V_{DS} = -0.1$ V are shown in Figure 7b. The minimum conductivity of the accumulation GoSFET occurs at a gate bias $V_{MC} = 0.26$ V. As can be expected, the current at the graphene channel ($I_{DS,G}$) is hardly modulated by the gate voltage due to the high residual concentration (the mobile charge in graphene is hardly tunable in the vicinity of the Dirac voltage in this scenario). In Figure 7c the modulation of the graphene electrostatic potential at the drain and source edges are shown. At the Dirac voltage, half of the graphene channel is filled with electrons and half is filled with holes, meaning that the Fermi level crosses the Dirac energy at the middle of the graphene channel. For liquid gate voltage higher and lower than CNP voltage, the flow of electrons and holes, respectively, becomes predominant.[69–72]

The silicon-based charge carriers, on the contrary, are considerably modulated by the gate voltage, and therefore they are the main responsible of the overall behavior observed in the

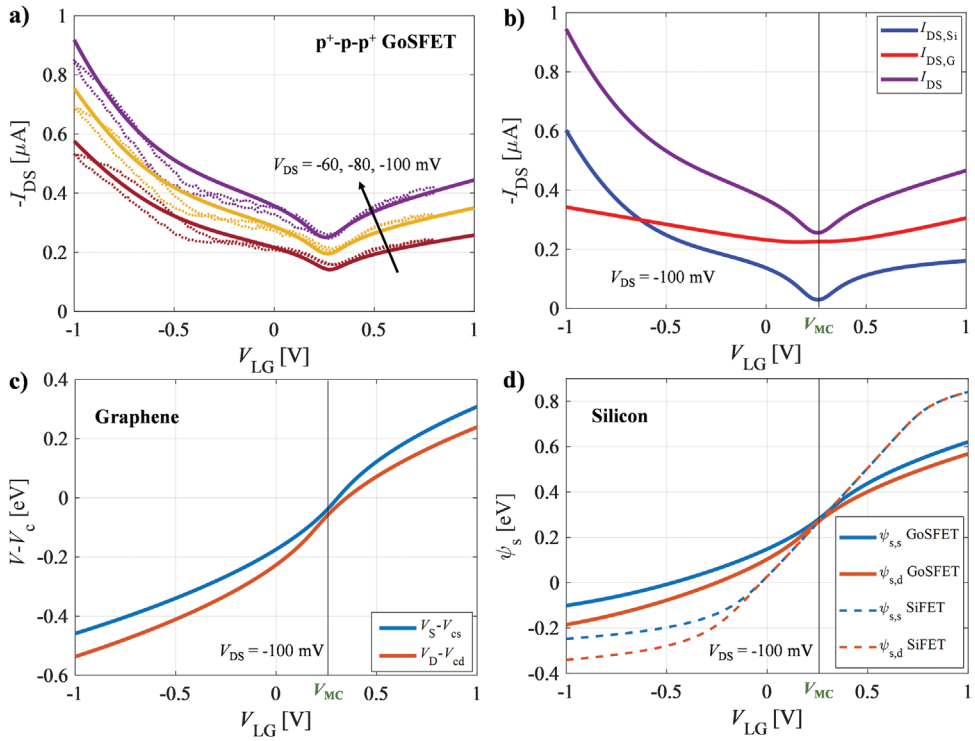

Figure 7. a) Transfer characteristics of the accumulation p^+–p–p^+ GoSFET described in Table 2 for three different drain biases. Simulations are plotted with solid lines and experimentally measured data (forward and backward sweeps) with dots. b) Theoretical drain current of the accumulation GoSFET for $V_{DS} = -0.1$ V (purple) split into the graphene (red) and silicon (blue) current contributions. A vertical black solid line marks the gate bias that achieves the minimum conductivity, labeled as V_{MC}. c) Modulation of the graphene electrostatic potential V-$V_c = E_D/q$ at the source (blue) and drain (orange) ends with a drain voltage of $V_{DS} = -0.1$ V. d) Modulation of the silicon surface potential at the source (blue) and drain (orange) edges in the accumulation of a GoSFET (solid lines) and a SiFET (dashed lines) with $V_{DS} = -0.1$ V.

current of the GoSFET (Figure 7b). Indeed, the vertex of the V-shaped transfer curve of the GoSFET is mainly produced by the current flowing through the silicon channel (Figure 7b). The surface potentials at the drain ($\psi_{s,d}$) and source ($\psi_{s,s}$) edges of the accumulation GoSFET (solid lines) are shown together with these quantities for a SiFET counterpart. According to Figure 7d, $\psi_{s,d}$ and $\psi_{s,s}$ get close at V_{MC}, meaning that the transport charge can be considered uniform along the channel, therefore, minimizing the diffusion component of the current. For $-0.5\ V < V_{LG} < V_{MC}$ and $V_{LG} > V_{MC}$, the surface potentials start to split and thus, both diffusion and drift currents increase. Finally, for $V_{LG} < -0.5$ V, when $\psi_s < 0$ holes accumulate in the channel, showing a large increment in the drift current (see details in Note S3, Supporting Information). The surface potentials of a SiFET without considering the graphene layer (shown in Figure 7d for comparison), exhibit the usual behavior of an accumulation SiFET. In this case, when $\psi_{s,d}$ and $\psi_{s,s} > 0$, they are almost identical and the diffusion current is negligible. For $\psi_s < 0$, the channel enters in accumulation and the surface potentials start to separate, therefore, increasing drift and diffusion currents.

A complete analysis of the inversion $n^+ - p - n^+$ GoSFET is also provided in Note S4, Supporting Information. It must be highlighted that the same parameters collected in Table 2 have been used for the inversion $n^+ - p - n^+$ GoSFET, except the values of the mobilities ($\mu_g = 40\ cm^2\ Vs^{-1}$; $\mu_{e,Si} = 225\ cm^2\ Vs^{-1}$), the residual charge density due to electron-hole puddles ($\sigma_{pud}/q = 5.4 \times 10^{12}\ cm^{-2}$) and the offset bias ($V_{fb2} - V_D = -0.41$ V) and the agreement between simulation and measurements is excellent (maximum average relative error of 6%) even though each type of GoSFET (accumulation and inversion) shows a quite different transfer characteristic shape (Figure 1c).

3. Conclusions

Graphene-on-silicon field effect transistors have been fabricated, exploiting a novel hybrid technology and demonstrating a unique behavior where both channel materials contribute to electronic transport. In spite of the fact that GoSFETs transconductance and carrier mobility are significantly lower compared to the conventional GFETs and SiFETs, the resulting structures can be utilized as a biosensor where eventually graphene and silicon can be functionalized for complex analytics separately. A comprehensive physics-based compact model has been purposely implemented evidencing that, contrary to the behavior registered in a conventional SiFET (which is controlled by a constant gate potential along the channel), the GoSFET is characterized by a non-uniform spatial graphene-silicon interaction that impacts the silicon conductivity. This strong electrostatic coupling between carriers in both channels is captured in our theoretical analysis and results in the presence of a non-negligible diffusion current in the subthreshold region. Due to this nonuniform gating effect caused by the graphene layer, the current in the silicon channel in a GoSFET can hardly be switched off.

4. Experimental Section

Device fabrication: Graphene-on-Silicon heterostructures were fabricated on <100> 4-inch silicon-on-insulator (SOI) wafers provided by SOITEC, France. The active silicon layer was 50 nm thick with 145 nm of buried oxide. In the first step, the thermal oxidation of the top silicon layer in the dry oxygen atmosphere was performed (940 °C, 45 min.). Then utilizing e-beam photolithography, the SiO_2 hard mask was patterned by anisotropic reactive ion etching (RIE) in CHF_3 plasma. The finite silicon nanoribbon shape was transferred to the active silicon layer by dipping wafers into a 5% TMAH water solution at 80 °C for 15 s. After stripping off the hard mask with 1% HF (3 min 30 sec), to create good ohmic contacts, ion implantation of drain-source terminals is carried out. Depending on the structure, boron (6 keV, $10^{15}\ cm^{-2}$) and arsenic (8 keV, $10^{14}\ cm^{-2}$) were used to get highly doped regions p- or n-type, correspondingly. Then, wafers are annealed for dopant activation: 5 s at 1000 °C for boron and 30 s at 950 °C for arsenic implantation. The fabrication layouts of GoSFETs are designed with the possible back gate control. For this reason, we performed etching through the buried oxide by a buffered oxide etch (BOE) for 70 seconds. As a protecting layer pre-patterned, AZ 5214 E photoresist was used. Metallization of the silicon part of the transistors was done in two steps. First, the stack of 5 nm TiN and 200 nm of Al were deposited onto drain-source contacts with the subsequent annealing in forming gas atmosphere (N_2:H_2 = 10:1 at 450 °C for 1 min.). This step is essential for the creation of good ohmic contact with the structure. After, metallization of feedlines by 10 nm Ti and 60 nm Au compound was carried out. Finally, after creating inversion ($n^+ - p - n^+$) or accumulation ($p^+ - p - p^+$) mode SiFETs, we go to the graphene part of the technology. A monolayer of CVD-grown graphene used in this study was provided by Graphenea, Spain. For "fishing" technique transfer, we used a PMMA photoresist as support to transfer graphene on top of the wafers. The PMMA residues are removed by subsequent immersion of the wafers into hot acetone and propanol (60 °C, 1 h. each). Next, patterning of graphene was done using oxygen plasma (1 min., 100 W). Then, the second metallization with another Ti/Au (10 nm/60 nm) stack is performed to sandwich graphene. In the last step, each wafer is covered by polyimide for passivation. After photolithography, the passivation layer is annealed and wafers are diced onto chips.

Characterization: After fabrication stage, devices were fastened to the chip carriers and encapsulated. Characterization was carried out utilizing a Keithley 4200 SCS semiconductor parameter analyzer. The gate potential (V_{LG}) was swept against Ag/AgCl pellet electrode from –1 V to 0.8 V. For the liquid gating, a physiologically close 150 mM phosphide buffer solution (PBS) with pH 7.4 was used. The drain-source potential (V_{DS}) was altered from 20 mV to 100 mV or from 50 mV to 500 mV with steps of 20 mV or 50 mV respectively.

Raman Spectroscopy: Confocal Raman spectroscopy for GoSFETs was performed using a Witec 300 Alpha R equipped with a Mitutoyo M Plan Apo SL 100×/0.55 objective. The spectra were taken with an excitation laser wavelength of 532 nm and power of 0.3 mW before the objective to avoid damage to the sample. As a laser source applied through a 100 µm single-mode glass fiber a single-mode frequency-doubled Nd:YAG laser was used. The excitation line was isolated from the Raman signal via an edge filter. As a pinhole for Raman confocality served 50 µm multimode fiberglass. Additionally, Raman setup was equipped with Newton Andor EMCCD camera with 1600×200 pixels and a holographic grating of 600 lines per mm. The data processing was performed by cluster analysis and non-negative matrix factorization.

Electrostatics of the GoSFET: 1D electrostatics across the electrode-electrolyte-hydrophobic gap-graphene-dipole layer-silicon heterostructure:

$$\begin{cases} Q_{net}(x) = -C_{int}\left(V_{LG} + \Psi_0 - V_{fb1} + V_c(x) - V(x)\right) - C_{dip}\left(V_{fb2} + \Psi_s(x) + V_c(x) - V(x)\right) \\ Q_{si}(x) = -C_{dip}\left(V(x) - V_c(x) - V_{fb2} - \Psi_s(x)\right) \end{cases} \quad (2)$$

where Q_{net} is the graphene overall net sheet charge density; Q_{si} is the charge induced in the silicon channel; V is the graphene quasi-Fermi level and must fulfill the boundary conditions: (i) $V(x = 0) = V_S$ (source voltage) at the source end; (ii) $V(x = L) = V_D$ (drain voltage) at the drain edge, where x is the transport direction and L is the gate length; V_c is the graphene chemical potential (related to the shift of the Fermi level with respect to the Dirac energy[62,73]); and ψ_s is the silicon surface potential.[61] Furthermore, $V_{fb1} = \Phi_m - \Phi_g - Q_{d1}/C_{int}$ and $V_{fb2} = \Phi_g - \Phi_{si} - Q_{d2}/C_{dip} + V_D$ are the flat-band voltages that comprise metal (Φ_m) and graphene (Φ_g) work-functions; possible additional charges (Q_{d1} and Q_{d2}) due to impurities, doping, etc., at the electrolyte-graphene interface and the graphene-silicon interface; the silicon work-function defined $\Phi_{si} = \chi_{si} + E_G/(2q) + \psi_B$, where χ_{si} and E_G are the silicon electron affinity and band gap; and $\psi_B = (k_BT/q)\ln[N_A/n_i]$ is the difference between the Fermi level and the intrinsic Fermi potentials at the silicon channel[61] (with k_B is the Boltzmann constant, T is the temperature, q is the electron elementary charge, N_A the acceptor concentration at the p-type silicon substrate and n_i the silicon intrinsic carrier concentration). Finally, the last term of V_{fb2} embraces the V_D dependence of the shift of the Dirac voltage of graphene due to traps at the graphene-silicon interface.[74] As aforementioned, since the electrolyte properties are not modified, Ψ_0 is constant in Equation (2) and could be incorporated into V_{fb1} as a correction of the flat-band condition.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

M. Fomin: Investigation, Formal analysis, Data Curation, Writing – Original Draft. F. Pasadas: Methodology, Theory, and Interpretation, Writing – Original Draft. E. G. Marin, A. Medina-Rull, F. G. Ruiz, A. Godoy: Methodology, Theory, and Interpretation, Writing – Review & Editing. I. Zadorozhnyi: Investigation, Supervision. G. Beltramo: Investigation, F. Brings: Supervision. S. Vitusevich: Supervision. A. Offenhaeusser: Supervision. D. Kireev: Conceptualization, Investigation, Writing – Review & Editing, Supervision.

Data Availability Statement

The data and the Verilog-A compact model that support the findings of this study are available from the corresponding authors upon reasonable request.

Keywords

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