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RESEARCH ARTICLE

Rule-Based Design for Low-Cost Double-Node Upset Tolerant Self-Recoverable D-Latch

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ABSTRACT This paper presents a low-cost, self-recoverable, double-node upset tolerant latch aiming at nourishing the lack of these devices in the state of the art, especially featuring self-recoverability while maintaining a low-cost profile. Thus, this D-latch may be useful for high reliability and high-performance safety-critical applications as it can detect and recover faults happening during holding time in harsh radiation environments. The proposed D-latch design is based on a low-cost single event double-node upset tolerant latch and a rule-based double-node upset (DNU) tolerant latch which provides it with the self-recoverability against DNU, but paired with a low transistor count and high performance. Simulation waveforms support the achievements and demonstrate that this new D-latch is fully self-recoverable against double-node upset. In addition, the minimum improvement of the delay-power-area product of the proposed rule-based design for the low-cost DNU tolerant self-recoverable latch (RB-LDNUR) is 59%, compared with the latest DNU self-recoverable latch on the literature.

INDEX TERMS Delay-power-area product (DPAP), double node upsets (DNU), high impedance state (HIS), low cost single event double node upset tolerant (LSEDUT), power-delay product (PDP), single node upset (SNU), soft error (SE).

I. INTRODUCTION

As CMOS technology is scaled down, the amount of charge needed to disturb the logic state of nodes of electronic circuits is dramatically reduced, primarily due to the low supply voltage and smaller capacitance of transistors. This fact is translated into an increasing vulnerability of the state of digital circuits to glitches formed by particle striking [1]. Therefore, increasing the reliability of integrated circuits for soft error (SE) tolerance or even SE self-recoverability has become a challenge of paramount importance [2].

The particle striking can affect the node state of memory cells, flip flops, and D-latches, which causes SEs. A SE occurring at one specific node is called single node upset (SNU). This phenomenon is responsible for the increasing investment in hardening D-latches against SNU [3], [4], [5].

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Furthermore, the consequence of the nano scaling race, the probability of occurrence of a double node upset (DNU) increases. For example, it is more than twenty-five percent for technologies below the 45nm node [6], which redoubles the need to design D-latches that can handle DNU [7], [8], [9], [10].

One of the approaches to increase the tolerance of D-latches against DNU is to use larger transistors for sensitive nodes, but even under this solution, some nodes can be upset by large charge injection [11]. Other approaches resort to layout technology making use of well isolation or extending the node space and guard ring to help tolerate DNU [7]. Thereby, the design of circuits becomes very complex. Many researchers are motivated to apply radiation hardening by design techniques (RHBD), in which C-elements, inverters, and Dual Interlocked storage Cell (DICE) [1], [12], [13], [14], [15] are used. However, these D-latches cannot recover by themselves and present, at least,

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one pair of nodes unable to tolerate DNU [12], [13], [15], [16] or they are not optimized for power consumption or delay [10], [14].

This paper presents a novel and improved low-cost DNU-self-recoverable D-latch to meet the demand for reliable and low-cost circuits for harsh environments. This proposed D-latch is an improvement of the low-cost single-event double-node upset tolerant (LSEDUT) latch [12] based on the rule design for multiple nodes upset tolerant latch architecture [17], to confer it with self-recoverability. By using a different design approach, such as a clock-gating (CG) technique, this proposed D-latch has a lower transistor count, which results in lower power and area consumption. As there are separate paths for transparent mode and holding time, the delay also is minimum. SEU and DNU fault simulation results will show that this D-latch is not only immune against SEU and DNU, but the whole D-latch is self-recoverable against them.

The paper is structured as follows: section II focuses on reviewing previous self-recoverable DNU and DNU tolerant D-latches. In section III, the characteristics of the proposed D-latch are presented and the immunity against SNU and DNU is tested. In section IV, simulation methodology and comparative studies of robustness, power consumption, delay, area, and delay-power-area-product with previous hardened D-latches are discussed. Finally, the main conclusions derived from this work are summarized in Section V.

II. STATE OF THE ART: PREVIOUS HARDENED LATCH DESIGNS

In this section, a review of self-recoverable DNU and DNU tolerant D-latches is presented. Previous hardened latch designs such as double-node charge sharing (DNCS) SEU tolerant latch [7], non-temporally hardened latch (NTHLTCH) [10], triple path dual-interlocked storage cell (TPDICE)-based latch [18], LSEDUT latch [12], DNU self-recoverable latch design for high performance and low power application (DNURHL) latch [19], and rule-based DNU tolerant latch (RDTL) [17] are analyzed.

A. DNCS-SEU TOLERANT LATCH

Figure 1(a) shows the structure of the DNCS SEU tolerant D-latch. This D-latch has some immunity constraints originating from the interlock between different nodes, such as N1 and N4. To illustrate this issue, as can be seen in figure 1(a), N1 is the input of one C-element and N4 is the output of this C-element. Also, in the other C-element, N4 node becomes input and N1 is output, which stablishes one feedback path for these two nodes N1 and N4. Therefore, if the pair of nodes <N1, N4> has an upset, it will result in a high impedance in N5 and N2 nodes, and as the 3-input C-element has N1 upset, the output and inverter of output (Qb) will present high impedance. If at the output of the D-latch, a high impedance state (HIS) occurs, it yields that the D-latch does not have the ability to self-recover, and the upset at the latch can stay for the long term. This D-latch can experience upset by DNU in pairs such as <N2, N5>, <N3, N6>. Furthermore, this circuit is a pseudo-static D-latch and new data are written based on an overcoming process, which makes temporary competition between the driving output and the feedback inside, causing high leakage power consumption. Also, this D-latch presents a high delay from the input to the output node.

B. NTHLTCH

The structure of NTHLTCH D-latch is displayed in figure 1(b). This D-latch is self-recoverable, but it is not cost effective in terms of silicon area and power consumption due to the use of nine C-elements and five inverters to ensure that it is immune against DNU and able to recover itself against DNU [19].

C. TPDICE-BASED D-LATCH

TPDICE-based D-latch is a hardened D-latch with immunity against single event transient (SET), SNU, DNU, and HIS insensitivity [18]. As figure 1(c) shows, this structure includes a TPDICE used for keeping the data in holding time, a three input C-element for filtering DNU, an embedded Schmitt trigger inverter for filtering the SET in the transparent path, and a keeper for avoiding HIS in the output node.

D. LSEDUT D-LATCH

Figure 1(d) shows the structure of the LSEDUT latch. This DNU tolerant D-latch is based on a TPDICE with full use of its interlocked node character to make it reliable for storing data. It has a keeper to avoid high impedance at the output node and two separate paths for holding time and transparent mode.

E. DNURHL LATCH

The DNURHL latch is DNU tolerant, however, due to the feedback architecture used, it is not fully recoverable. As figure 1(e) shows, it has pairs of input of C-elements, which makes improper feedback to the output of these C-elements: if there is any DNU at the input of these C-elements, their outputs will lose their data and it will result in an upset of the D-latch. These pair of input nodes of C-elements are, <N1, N5>, <N2, N6>, <N3, N7>, and <N4, Q>. This originated since node pair <N2, N6> is the input of two C-elements and if it is affected by charge injections, its upset can perturb the rest of the C-elements. A careful analysis shows that if N2 and N6 lose their value, N3 and N7 which are the output of C-elements (CE2) and CE6 will be affected, and their outputs lose their data. Therefore, two C-elements, CE3 and CE7, are affected and they lose their data. The <N1, N5>, <N3, N7>, and <N4, Q> pairs of nodes can experience the same upsets when a particle strikes two nodes of each of these pairs. The feedback of C-elements cannot recover their valid data because of the improper feedback mechanism. Consequently, the D-latch will be upset.

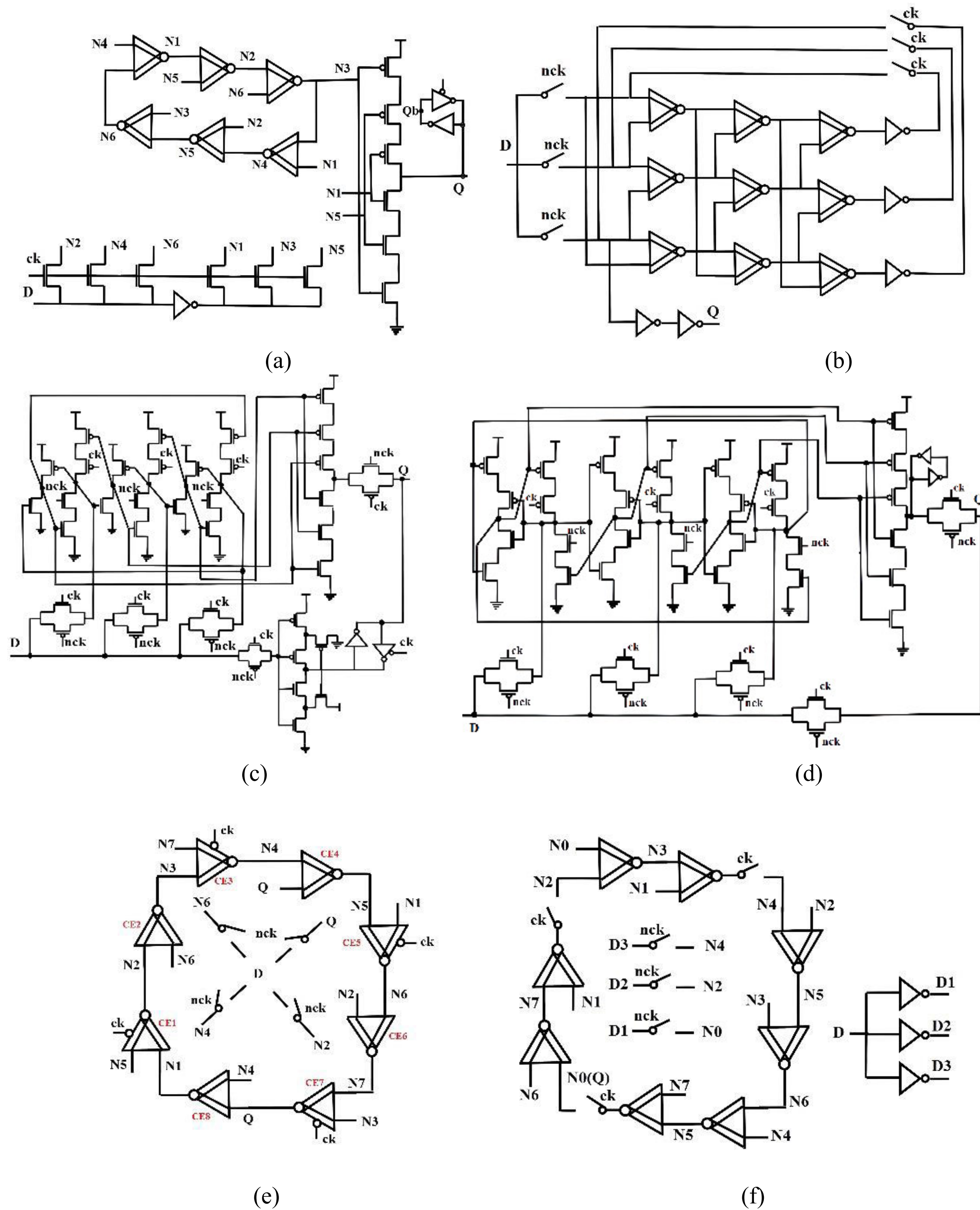

FIGURE 1. Previous hardened latch designs (a) DNCS-SEU tolerant latch, (b) NTHLTCH, (c) TPDICE-based latch, (d) LSEDUT latch, (e) DNURHL latch, (f) RDTL.

F. RDTL LATCH

The DNURHL D-latch is not self-recoverable since the node pairs of C-element inputs are repeated, and these input pairs suffer from improper feedback to the output nodes of these C-elements. This problem is solved in RDTL (figure 1(f)), which is designed based on rule design so that the pairs of nodes of input C-elements are not repeated, presenting appropriate feedback in loops to become fully self-recoverable against DNU [17]. However, the RDTL, in comparison with the DNURHL latch, has more transmission gates and inverters, which introduces more area and power consumption penalty.

III. PROPOSED D-LATCH

The proposed D-latch is based on the LSEDUT and the RDTL latches, in which the number of transistors, power consumption, and area consumption are reduced. The structure of this latch consists of four 2-input C-elements, four

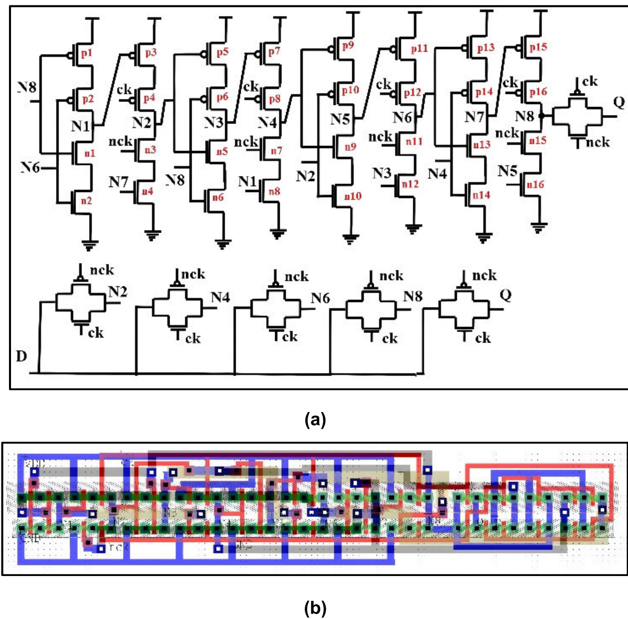

FIGURE 2. Proposed RB-LDNUR D-latch (a) schematic, (b) layout.

input-split inverters, and six transmission gates. Also, each input of the proposed D-latch is connected to the four transistors, storing the input in more nodes to tolerate DNU and making this proposed D-latch self-recoverable against DNU. D, Q, ck, and nck are the input, output, clock, and inverted clock, respectively. Figure 2(a) shows the schematic of the proposed rule-based design for a low-cost DNU tolerant self-recoverable latch (referred to as RB-LDNUR) and figure 2(b) shows the layout of the proposed D-latch. When ck = 1, the latch is in transparent mode and the input is connected to N2, N4, N6, N8, and Q. After the propagation of D input from 2-input C-elements, N1, N3, N5, and N7 are defined. The output is driven by D, and N8 is not connected to the output directly targeting the reduction of the (D-Q) delay since N8 introduces more delay in the latch because it is connected to four gates of transistors (which introduces large capacitance in this node).

When ck = 0, the latch is in hold mode, N2, N4, N6, N8, and Q are disconnected from D, and Q is driven by N8. The interlocked feedback of the RB-LDNUR is active to retain robustly the data. These feedbacks are activated just during holding mode to save power.

The proposed D-latch structure is optimized in comparison with the DNURHL latch. Since the DNURHL latch consists of clock-gating 3-input C-elements, which are not applied in the proposed D-latch (the proposed design features 2-input C-elements), which optimizes area, power consumption, and transistor count. On the other hand, the RDTL latch has extra transmission gates and inverters in the feedback loop in comparison with the proposed D-latch, which reduces the transistor count of the new solution. In consequence, the power consumption and silicon area are also reduced. By applying the structure of the LSEDUT with the rule design of the RDTL, the proposed latch has larger interlocked feedback in holding time. By combining these two structures, the proposed D-latch is self-recoverable against DNU with fewer transistors. Also, in this structure, one transmission gate between Q and N8 is used for reducing the delay.

Following the rule design in [17], the proposed D-latch is immune against DNU, therefore, n = 2, and d = 2(n-1), where n is the number of nodes upset simultaneously in the D-latch, and d is the number of elements between Ni and Nj. To configure the proposed D-latch, assuming the Ni is the first node to one element, Nj is the second node, and i = (j-d-1) mod (4d). Therefore the pair of nodes entering different elements are as follows: <N1, N7>, <N2, N8>, <N3, N1>, <N4, N2>, <N5, N3>, <N6, N4>, <N7, N5>, <N8, N6>.

For evaluating the immunity against SNU, there are nine nodes and each of them can be affected by SNU. If N1 is affected by an SNU, a glitch will occur; in the case of D = 0, N2 = 0, and N1 = N7 = 1 (p3 off and n8 ON), if the SNU occurs in N1, the value of N1 = 0 (p3 ON and n8 off), which makes N2 and N4 becomes unstable, but as N8 and N6 are not affected by SNU, N1 can be recovered by N8 and N6, then consequently, N2 and N4 can be stabilized by N1, which means N1 is self-recovered against SNU. This analysis can be applied to the whole of other nodes, which proves this latch is immune and self-recoverable against SNU.

For immunity against DNU, there are nine nodes in holding time making $C_2^9 = 36$ cases of node pairs. In the following, the different cases of DNU are evaluated based on the design of the hardened D-latch, but this DNU is independent of where the charge is injected into the D-latch. As the structure is symmetric, there are five cases to study: (1) <N1, N2>, <N2, N3>, <N3, N4>, <N4, N5>, <N5, N6>, <N6, N7>, <N7, N8>, <N8, N1>; (2) <N1, N3>, <N2, N4>, <N3, N5>, <N4, N6>, <N5, N7>, <N6, N8>, <N7, N1>, <N8, N2>; (3) <N1, N4>, <N2, N5>, <N3, N6>, <N4, N7>, <N5, N8>, <N6, N1>, <N7, N2>, <N8, N3>; (4) <N1, N5>, <N2, N6>, <N3, N7>, <N4, N8>; (5) <N1, Q>, <N2, Q>, <N3, Q>, <N4, Q>, <N5, Q>, <N6, Q>, <N7, Q>, <N8, Q>.

Case 1: <N1, N2> is affected by a DNU and perturbed by charge injection. As example D = N2 = 0 and N1 = 1; p3, n5, and n10 are off and n8, p5, and p10 are ON. If upset happens, N1 = 0 and N2 = 1, n8, p5, and p10 are off and p3, n5, and n10 are ON. But, N3 does not lose its value because N8 has valid data. As N8 and N6 have valid data, they can recover N1. Then, by recovering N1, p3 becomes off and N7 has valid data and can recover N2, which means <N1, N2> is immune and self-recoverable against DNU. Other pairs of this case can be analyzed similarly. As the result, the proposed RB-LDNUR D-latch is DNU-immune and self-recoverable in case 1.

Case 2: in this case, <N1, N3> is evaluated. Since N1 and N3 lose their value, there are weak instabilities in N2 and N4. But, as N6 and N8 have valid data, N1 can be recovered, and then N2 will be stable. The stability of N2 can help N3 to be recovered and N4 becomes stable. This explanation shows <N1, N3> is self-recoverable and immune against DNU.

For other pair groups, the analysis against DNU is similar, thus they can be self-recover against DNU and this proposed D-latch is self-recoverable against DNU in case 2.

Case 3: in this case where <N1, N4> is affected by DNU, an upset happens. For example, D = N2 = 0, and N1 = 1; p3, n14, and n9 are off and n8, p9, and p14 are ON. If there are charges injected to N1 and N4, then N1 = 0 and N4 = 1, therefore, n8, p9, and p14 are off and p3, n14, and n9 are ON. N2 becomes weakly unstable. But, N5 does not lose its value. As N8 and N6 have a valid value, N1 can be recovered by N6, and N8 and N2 can be stable. Also, N4 can be recovered by N3 and N1. This explanation demonstrates <N1, N4> is immune and self-recoverable against DNU. Other pairs of nodes can be analyzed similarly, thus they are also self-recoverable and DNU-immune. Therefore, this proposed RB-LDNUR D-latch can be self-recover from DNU in case 3.

Case 4: in this situation, <N1, N5> is affected by DNU. For this case, D = N2 = 0, and N1 = N5 = 1, p11, and p3 are off; n8 and n16 are ON. If N1 and N5 are affected by DNU, N1 = N5 = 0, p11 and p3 are ON; n8 and n16 are off. Then, N2 and N6 can be weakly unstable. But, N1 and N5 can be recovered by N8 and N4, respectively. Therefore, N2 and N6 become stable and the D-latch can become self-recoverable against DNU. Other pair groups recover themselves in the same way as <N1, N5>. Consequently, the proposed RB-LDNUR D-latch is self-recoverable in case 4.

Case 5: in this situation <N1, Q> is affected by DNU. As among nodes N1 to N8, just N1 is affected by DNU, this case is similar to SNU in nodes N1 to N8 because Q is not feedback to any other part of the RB-LDNUR latch. When N1 is affected by DNU, N2 and N4 become unstable, but N6 and N8 have valid data and N1 can be recovered by them. Then, N2 and N4 become stable. Also, Q can be recovered by N8. This analysis is valid for other pairs of nodes in this group. As the result, the proposed RB-LDNUR D-latch is immune and self-recoverable against DNU in case 5.

When D = 1, the performance of the proposed RB-LDNUR D-latch is similar to the case when the input data is D = 0. This structure is immune and self-recoverable against DNU. Therefore, the proposed RB-LDNUR D-latch is DNU-self-recoverable for all these key node pairs.

IV. SIMULATION RESULTS

The proposed RB-LDNUR D-latch, DICE [20], DNCS SEU tolerant latch [7], DNUCT [21], NTHLTCH [10], TPDICE-based latch [17], LSEDUT latch [12], DNURHL [19], RDTL [17], RH-latch [22], FPADRL [23], LOCDNUTRL [24], HTNURE [25], LOCTNUTRL [24] are simulated at 0.8 V at room temperature using Synopsys® HSPICE in 22nm CMOS technology from PTM library [26]. For a fair comparison, PMOS transistors have an aspect ratio of W/L = 35 nm/22 nm, and NMOS transistors have an aspect ratio of W/L = 24 nm/22 nm.

In the error injection test, the proposed RB-LDNUR D-latch is evaluated against SNU and DNU by a current transient (current source) simulating the charge injection given

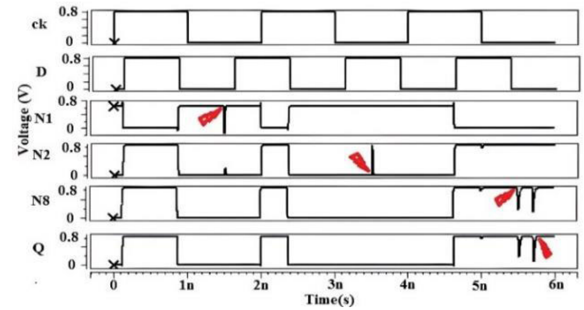

FIGURE 3. Simulation results of SNU injections to key single nodes of the proposed RB-LDNUR D-latch.

by the following mathematical expression [27]:

$$I = \frac{Q_{total}}{T\sqrt{\pi}}\sqrt{\frac{t}{T}}e^{-t/T} \tag{1}$$

where, T is the value of the time constant of the injected current charge, which is 0.1 ps and Q_{total} is the total charge injected being 20 fC in this test, which is large enough to prove immunity of the proposed RB-LDNUR D-latch against SNU/DNU [4].

The simulation results show that the operation of the proposed D-latch is similar to that of the traditional D-latch. Thus, in the transparent mode, the input is equal to the output, and in the holding mode, the output is equal to the input at the moment the clock becomes low level, as can be seen in figure 3.

For SNU simulation, to prove the self-recoverability of the proposed RB-LDNUR D-latch, one charge is injected into different nodes, such as internal nodes or Q. When the output and internal nodes do not lose their logical value after injections, which means they are self-recoverable against SNU.

As can be seen in figure 3, the key single nodes N1, N2, N8, and Q are injected by SNU, respectively. These key nodes are based on the different situations of SNU at the proposed RB-LDNUR latch, which analysis is mentioned above. The simulation results show that the output and other internal nodes do not lose their values after SNUs, which proves that the proposed RB-LDNUR D-latch is self-recoverable against SNU.

Based on different pairs of nodes in the DNU immunity of the proposed RB-LDNUR D-latch, the following tests are considered. Table 1 shows the key patterns of DNUs used for the charge injections in figure 4. As can be seen in this figure, different key pattern injections of DNU do not change the logical value of the internal nodes and output node, which means that the proposed RB-LDNUR D-latch is immune and self-recoverable against DNU. This table shows the precise time at which two charge injections are introduced at two different nodes. If after these injections the values of the nodes do not change, it means that they are self-recoverable against these DNUs. Moreover, the output node has to maintain its value during these injections and as can be seen in figure 4, the Q value is stable during the whole of these DNUs.

TABLE 1. Key pattern of DNU injections of the proposed RB-LDNUR latch in figure 4.

Time (ns)	SNUs/DNUs	State
1.2	N1, N2	Q =0
1.8	N1, N3	Q =0
3.2	N1, N4	Q =0
3.8	N1, N5	Q =0
5.8	N1, Q	Q =1

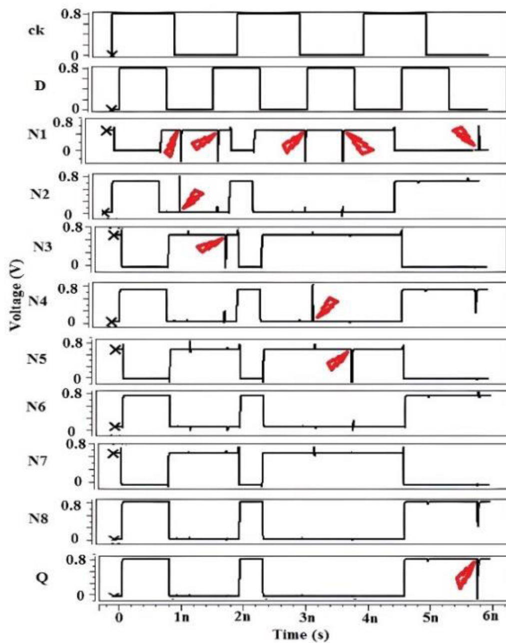

FIGURE 4. Simulation results of key patterns of DNU injections for the proposed RB-LDNUR latch.

Figure 5 shows the simulation waveforms for the proposed RB-LDNUR latch based on the pairs of nodes in table 2. These pairs of nodes are different internal nodes and the output node, Q. The results show that in all of the pairs of nodes, the proposed RB-LDNUR latch and all internal nodes can be self-recoverable from the DNU. Therefore, the output node is self-recoverable from every DNU at the proposed RB-LDNUR latch. For example at 1.2 ns in figure 5, the DNU injection occurs at N1 and Q nodes, when $Q = 0$, as can be seen for this DNU test, the values of Q and N1 nodes are the same as before the injections.

In summary, the above explanation and simulation results demonstrate the reliability of the proposed RB-LDNUR latch against SNU/DNU injections and its self-recoverability.

In table 3, there is a comparative summary of SNU, DNU immunity, HIS insensitivity, self-recoverability of the proposed RB-LDNUR latch and state-of-the-art SNU, DNU, and triple node upset (TNU) hardened D-latches, such as DICE, DNCS-SEU tolerant, DNUCT, NTHLTCH, TPDICE- based latch, LSEDUT, DNURHL, RDTL, RH-latch, FPADRL, LOCDNUTRL, HTNURE, LOCTNUTRL latches. DICE and DNCS-SEU tolerant latches are not fully immune against DNU. For self-recoverability, DICE can recover itself against SNU, but DNCS-SEU cannot recover itself against SNU. NTHLTCH is self-recoverable against DNU and it is fully immune against SNU and DNU, but it is not efficient in terms of cost. DNUCT, LSEDUT, and TPDICE-based latches and RH-latch are fully immune against SNU and DNU, but none of them are self-recoverable against DNU. The DNURHL latch is not fully immune against DNU because of improper feedback between pair nodes of 2-input C-elements and outputs of 2-input C-elements, causing the D-latch cannot recover its valid data when a pair nodes of 2-input C-elements are affected by DNU. The RDTL, FPADRL, and LOCDNUTRL latches are fully immune against SNU and

TABLE 2. Pattern of DNU injections to pairs with output node (Q) and other nodes of the proposed RB-LDNUR latch.

Time (ns)	SNUs/DNUs	State
1.2	N1, Q	Q =0
1.5	N2, Q	Q =0
1.7	N3, Q	Q =0
3.2	N4, Q	Q =0
3.5	N5, Q	Q =0
3.7	N6, Q	Q =0
5.2	N7, Q	Q =1
5.7	N8, Q	Q =1

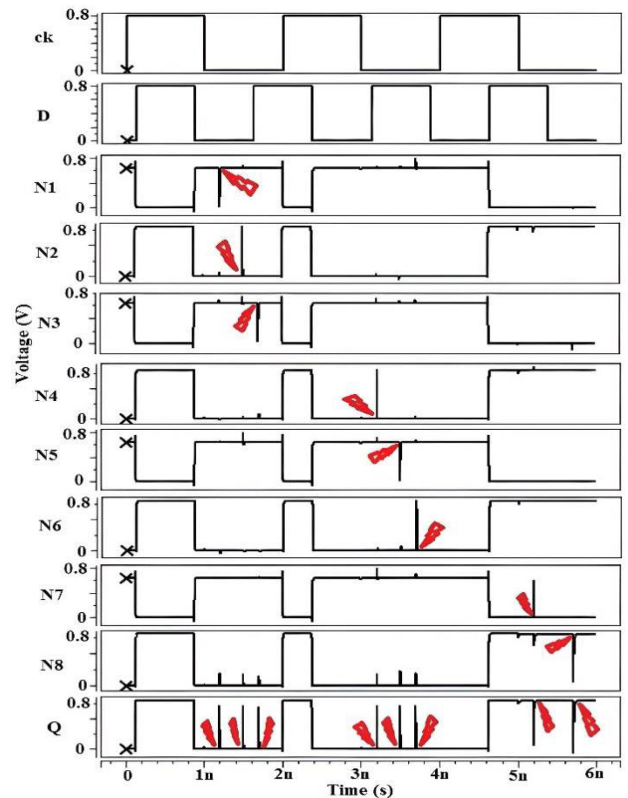

FIGURE 5. Simulation results of DNU injections to pairs related to the output node (Q) and other internal nodes of the proposed RB-LDNUR latch.

TABLE 3. Immunity against SNU, DNU, HIS insensitivity, and self-recoverability of the proposed RB-LDNUR and previous D-latches.

D-latch	Full Immune SNU	Full Immune DNU	Self-recoverability	HIS insensitive
DICE [20]	✓	×	✓	×
DNCS-SEU tolerant [7]	✓	×	×	✓
DNUCT [21]	✓	✓	×	✓
NTHLTCH D-latch [10]	✓	✓	✓	✓
TPDICE-based latch [18]	✓	✓	×	✓
LSEDUT latch [12]	✓	✓	×	✓
DNURHL latch [19]	✓	×	×	×
RDTL latch [17]	✓	✓	✓	✓
RH-latch [22]	✓	✓	×	✓
FPADRL [23]	✓	✓	✓	✓
LOCDNUTRL [24]	✓	✓	✓	✓
HTNURE[25]	✓	✓	✓	✓
LOCTNUTRL [24]	✓	✓	✓	✓
Proposed RB-LDNUR latch	✓	✓	✓	✓

DNU and can be self-recoverable, but it is not optimized for low-cost effectiveness. Also, HTNURE and LOCTNUTRL are TNU tolerant latches and self-recoverable against DNU, but still, they are not cost-efficient. Considering the proposed RB-LDNUR latch and applying the rule design of the RDTL latch and the structure of the LSEDUT latch, this new design is fully immune against SNU/DNU, can be self-recoverable, while maintaining a low-cost architecture. Moreover, as the proposed RB-LDNUR latch is HIS insensitive, it does not feature any driving ability during holding time.

Aiming at a quantitative comparison, the proposed RB-LDNUR latch and the mentioned hardened D-latches are simulated using the same PMOS and NMOS aspect ratios (transistors size), room temperature with 250 MHz input frequency at 0.8 V power supply in the 22nm CMOS technology. In the following simulation, a comparison of D-latch features related to area consumption, (D-Q) delay, average power consumption, PDP (power-delay product), transistors count, and DPAP (delay-power-area product) is presented. DPAP can be calculated by multiplying delay, power consumption, and area. Area consumption can be calculated by silicon footprint extracted from the layout of the proposed RB-LDNUR latch and the mentioned hardened D-latches using L-EDIT Tanner software.

Table 4 presents the improvement percentage of proposed D-latch DPAP in comparison with all other mentioned D-latch alternatives, which is increased dramatically. The minimum percentage of improvement of DPAP of the proposed D-latch is 59% in comparison with DPAP of the best alternative (FPADRL D-latch) and the average improvement is 86.1%.

As shown in table 5, the lowest power consumption, area, delay, PDP, and DPAP are featured by the proposed RB-LDNUR D-latch in comparison with previous mentioned DNU/TNU tolerant D-latches. DICE and DNCS-SEU tolerant D-latches have the least number of transistors followed

TABLE 4. Percentage improvement of DPAP proposed D-latch in comparison with other D-latches.

Features	Improvement
DICE	98.3%
DNCS-SEU tolerant	98.3%
DNUCT	76%
NTHLTCH D-latch	96%
TPDICE-based latch	99.1%
LSEDUT latch	94%
DNURHL latch	62%
RDTL latch	93%
RH-latch	64%
FPADRL	59%
LOCDNUTRL	97%
HTNURE	88%
LOCTNUTRL	95%

by the proposed D-latch, however, they are not fully immune against DNU and the DNCS-SEU latch is not self-recoverable against SNU. Also, the area consumption in table 5, besides depending on the number of transistors, depends on the complexity of the layout of the D-latches. Because of that, even FPADRL has two transistors less than the proposed RB-LDNUR D-latch, but it does not feature lower area consumption in comparison to the proposed RB-LDNUR D-latch. Moreover, FPADRL in comparison with the proposed RB-LDNUR D-latch presents a higher power consumption because of its structure.

In the design of the proposed RB-LDNUR D-latch, the minimum (D-Q) delay is achieved by using a transmission gate between N8 and Q. Since the capacitor of N8 is large due to the four gates of transistors connected to this node. By separating the output node (Q) and N8, the delay is reduced considerably. By applying the LSEDUT latch structure, the

TABLE 5. Properties comparative features of D-latches.

Features	POWER (μW)	DELAY (ps)	AREA (μm^2)	PDP ($10^{-18} \times W$)	TRANSISTOR COUNT	DPAP	$Q_{crit}(fc)$
DICE [20]*	0.74	18.20	0.90	13.40	18	12.10	1
DNCS-SEU tolerant [7]*	0.37	19.70	1.66	7.28	32	12.10	10
DNUCT [21]	0.53	0.56	3.10	0.28	70	0.87	5
NTHLTCH D-latch [10]	0.42	4.88	2.53	2.04	58	5.18	∞
TPDICE-based latch [18]	1.01	11.80	2.12	11.97	46	25.20	10
LSEDUT latch [12]	3.00	0.56	2.09	1.70	44	3.51	6
DNURHL latch [19]	0.26	1.14	1.85	0.30	48	0.55	8
RDTL latch [17]	0.35	4.28	1.99	1.48	50	2.98	∞
RH-latch [22]	0.53	0.56	1.99	0.29	36	0.58	5
FPADRL [23]	0.62	0.56	2.64	0.32	42	0.84	3
LOCDNUTRL [24]	3.16	0.95	2.24	3.01	44	6.74	2
HTNURE [25]	0.39	1.15	3.82	0.45	72	1.72	∞
LOCTNUTRL [24]	3.75	0.56	2.48	1.96	50	4.86	2
Proposed RB-LDNUR latch	0.24	0.56	1.57	0.14	44	0.21	∞

*Not DNU tolerant

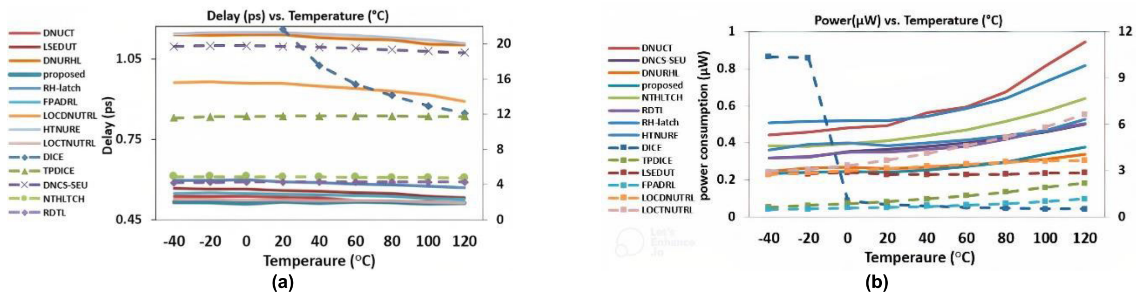

FIGURE 6. Impacts of temperature variation on: (a) Delay (b) Power consumption.

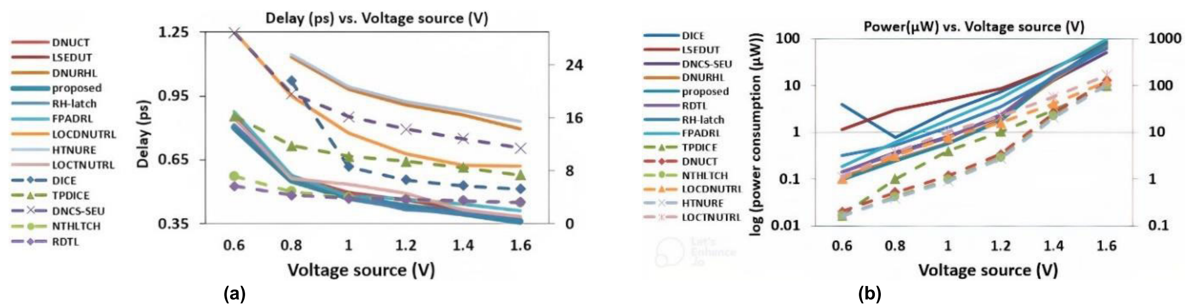

FIGURE 7. Impacts of supply voltage variation on: (a) Delay (b) Power consumption.

number of transistors, power consumption, and area are reduced in comparison with DNURHL and RDTL structures containing 2-input C-elements and the clock gating 3-input C-elements. The minimum improvement of power consumption of the proposed latch is 7.7% in comparison with the best alternative (DNURHL latch); the minimum improvement of silicon area is 5.4% as compared with the best alternative (DNCS-SEU tolerant latch), except for DICE, and the minimum improvement of PDP is 50% in comparison with the best alternative (DNUCT latch). Based on the reliability of the hardened D-latch against charge injections, the minimum charge injections that can produce SNU in different nodes of latches are calculated [28]. Since the purpose of hardening the D-latch is increasing the value of Q_{crit} to tolerate SE, the minimum charge injections should be considered. This Q_{crit} is the minimum charge injection that can flip the value of the most sensitive D-latch nodes. As can be seen in table 5, the minimum charge injection that can change the value of proposed D-latch nodes is infinite, which means the proposed D-latch is full immune.

Process, voltage, and temperature (PVT) variation is considered for latches and flip-flops in nanotechnology [29], [30], [31], [32], [33]. Figure 6 and figure 7 show the temperature and voltage supply variation impact on the delay and power consumption of previous D-latches and the proposed D-latch. For a better comparison, both figure 6 and figure 7 include two different axes. The dashed lines with markers are adjusted by the secondary axes on the right side

of the charts whereas the solid lines are adjusted by the axes on the left side of the charts.

In figure 6, for temperatures ranging between −40°C to 120°C, the power consumption and D-Q delay are monitored. In figure 6 (a), the delay is not affected by the temperature except for the case of DICE, since most of the mentioned D-latches have one transmission gate from input to output in transparent mode. The proposed D-latch features the minimum delay being its delay-temperature below the ones by its competitors. In figure 6 (b), by increasing the temperature, the carriers' mobility of the transistors decreases [15], which results in increased power consumption of D-latches, except for the DICE case. As can be seen in figure 6, the proposed D-latch is highly immune against the variation of temperature, approximately during the range of −40°C to 120°C, it maintains its minimum delay and power consumption.

Figure 7 shows the impact of the variation of supply voltages (0.6 V-1.6 V) on power consumption and delay (D-Q). In figure 7 (a), the delay of D-latches reduces due to the large current driven by the transistors, however, during the range of supply voltages (0.6 V-1.6 V), the proposed D-latch maintains its minimum value delay. Additionally, power consumption rises by increasing the supply voltage. The reason behind this must be sought in the fact that by increasing the supply voltage, dynamic and static power increase (capacitors accumulate more charge and transistors drive more current [15]), as shown in figure 7 (b) in logarithmic scale. This figure shows that by increasing power consumption in the range of the supply voltages (0.6 V-1.6 V), the proposed D-latch maintains its minimum value of power consumption, which is translated into better performance in this range of supply voltage in comparison to its alternatives.

V. CONCLUSION

Scaling CMOS technology boosts the demand for D-latch reliability. This paper proposes a low-cost, self-recoverable D-latch featuring immunity against SNUs and DNUs. Since most hardened DNU D-latches are not self-recoverable and low-cost, the proposed RB-LDNUR latch is conceived based on different rule designs and structures to achieve these purposes. Simulation results show that the proposed RB-LDNUR latch design is DNU self-recoverable and cost effective in comparison with other recently proposed DNU/TNU self-recoverable latch structures. The minimum improvement of power consumption is 7.7%, in comparison with the best alternative (DNURHL latch); the minimum improvement of silicon area is 5.4% when compared with the best alternative (DNCS-SEU tolerant latch, except for DICE which is not DNU tolerant), the minimum improvement of PDP is 50% in comparison with the DNUCT latch. Finally, the minimum improvement of DPAP of the proposed D-latch in comparison with the FPADRL D-latch is 59% and compared with other mentioned D-latches, the average improvement is approximately 86.1%. Also, the temperature has little effect on the performance of the proposed D-latch and by changing the value of supply voltage, the proposed D-latch keeps its high performance compared with other mentioned previous D-latches.

DECLARATION OF COMPETING INTEREST

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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