NEW APPROACHES FOR CONTROLLING A RESONANT HALF-BRIDGE FLYBACK CONVERTER WITH WIDE VOLTAGE OPERATION RANGE

UNIVERSIDAD DE GRANADA

DOCTORAL THESIS

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CONTENT

Acknowledgement 8

Abstract 9

1. Introduciton 10

1.1. Thesis objectives 11

1.2. Document organization 12

2. Thermals limits versus power density and converter transfer function 13

2.1. Thermal limits 13

2.2. Transfer function of the power stage 15

2.3. References 17

3. Publication 1: Asymmetrical flyback converter in high density SMPS 18

3.1. Introduction 19

3.2. Multi-objective optimization 19

3.3. Asymmetrical PWM flyback 20

3.3.1. Topology 20

3.3.2. Operation phases 21

3.3.3. Energy storage 22

3.4. Dimensioning and control of the converter 23

3.4.1. Safe and efficient operation 23

3.4.2. Duty cycle and output voltage 23

3.4.3. Output load effect 23

3.4.4. Asymmetrical PWM flyback control method 24

3.4.5. Transformer dimensioning 24

3.5. Experimental results 25

3.6. Conclusions 26

3.7. References 26

4. Publication 2: Resonant Hybrid Flyback, a New Topology for High Density

Power Adaptors 27
4.1. Introduction 28
4.2. Asymmetrical Duty Cycle Flyback 29
4.2.1. Topology 29
4.2.2. Resonant Operation Phases 30
4.3. Asymmetrical Duty Cycle Flyback Control Methods 32
4.3.1. Duty Cycle and Output Voltage 32
4.3.2. Considerations for ZVS Operation 32
4.3.3. Proposed Resonant Operation 33
4.3.4. Understanding the Energy Storage 33
4.3.5. Magnetizing Current Displacement 35
4.3.6. Overpower Capability 36
4.4. Experimental Results 37
4.5. Discussion 40
4.6. Conclusions 40
4.7. References 41
5. Publication 3: Advanced control methods for Asymmetrical Half-bridge Flyback 43
5.1. Introduction 44
5.2. Topology 45
5.3. Continuous resonant mode (CRM) operation 46
5.3.1. Equations 47
5.3.2. Low output current operation 50
5.3.3. Low output voltage operation 50
5.3.4. Low input voltage operation 51
5.3.5. Limitations of the CRM control method. 54
5.4. Zero voltage resonant valley switching (ZV-RVS) mode 54
5.4.1. ZV-RVS mode, output current and control. 56
5.4.2. Optimum mode and operation point. 56

5.5. Practical prototype 58
5.6. Conclusions 61
5.7. Acknowledgment 62
5.8. References 62
6. Publication 4: Study of WBG switches benefits on Asymmetrical Half-bridge Flyback Converter 65
6.1. Introduction 66
6.2. Asymmetrical HB flyback topology 67
6.3. Switches and its parasitic elements effects 68
6.3.1. Required negative current (I_n) for ZVS operation 68
6.3.2. Practical switches example 69
6.4. Other considerations 72
6.5. Experimental prototype 73
6.6. Conclusions 74
6.7. References: 74
7. Publication 5: A high-efficiency isolated wide voltage range DC-DC converter using WBG devices 76
7.1. Introduction 77
7.2. Energy processing in power converters 79
7.2.1. Proposed topology 79
7.2.2. General design guidelines for AHB flyback 80
7.3. Estimation of the converter efficiency 82
7.4. Prototype 86
7.5. Conclusions 90
7.6. References 91
8. Results and conclusions 93
8.1. Results 93

8.2. Conclusions 93
8.3. Future work 94
9. Apendix 95
9.1. Patents 95
9.1.1. US11005378B2: Operating a flyback converter using a signal indicative of a resonant tank current of the flyback converter 95
9.1.2. DE102017110927A1: Flyback converter control, flyback converter and method of operating the flyback converter 95
9.1.3. US10797582B1: Cross conduction protection in a voltage converter 95
9.1.4. US10892687B2: Asymmetric power converter, power converters, and operating power converters 96

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A lo largo de la vida muchas personas pasan al lado, otras caminan junto a ti, pero sólo algunas te ayudan a caminar.

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ABSTRACT

Currently, adaptors and chargers are evolving towards a universal DC power source. The introduction of the USB-PD and USB-PD EPR standards define the path for such universalization. This way, they open the door to extend the usage of such adaptors for most of the rechargeable battery-based devices, from mobile phones to e-bikes.

A truly universal adaptor needs to support high output power, which normally results in bigger size and weight. Overcoming these disadvantages, in combination with the USB-PD requirements, is the major driving factor of the current developments in the field. The investigation targets of this work has been defined within such context.

Current flyback based converters show limited efficiency and size to achieve such targets. Forward converters, such as LLC converter, has limited input to output voltage range and need additional power stages to achieve the required range.

The proposed topology to be investigated, “asymmetrical half-bridge flyback converter”, is one of the most promising converter topologies to achieve the given goals, mainly due to the hybrid flyback-forward nature of the converter presented by first time within the context of this work.

The boundary conditions to achieve the maximum power density are described. An analysis of the proposed converter topology to probe its suitability for high power density is presented. Innovative control methods are proposed, especially to address low power conditions and wide input and output voltage range operation. Finally, the advantages of wide band gap devices applied to the converter are analyzed.

The investigation has been backup with simulation and several hardware prototypes that show outstanding results in terms of efficiency, power density and wide voltage range operation.

This research work has been carried out in cooperation with Infineon Technologies AG, most of the practical investigations has been carried out in its facilities at its headquarters in Neubiberg, Germany.

1. INTRODUCTION

Close frame power supplies without forced cooling are known as adaptors. They pose especial challenge in terms of size due to the fact that the heat, generated internally, is only dissipated by the surface of the electronics container.

Such adaptors used in telecommunication and lighting equipment are subject to several normative in terms of efficiency, power factor, electromagnetic compatibility (EMC) and safety.

Additionally selling factors such as, reliability, size, weight or efficiency are desired by the manufacturers to make their product more attractive.

All this factors set the requirements and development trends of the adaptors.

Regarding normative, the European standard EN61000-3-2, based on the international IEC 61000-3-2, limits the amount of harmonic currents introducing distortion for the mains voltage for equipment up to 16A per phase. This standard defines in a great manner the architecture of the power converters, in particular the defined power factor requirements, for lighting over 25W and for telecommunication equipment over 75 W, shape the architecture to be adopted. In many cases, when power factor needs to be provided, two converter stages are used.

In adaptor for telecommunication equipment, for power levels under 75W, a single stage flyback is very common. For power level over 75W, dual stage is very common, mostly PFC boost followed by LLC converter or PFC boost followed by flyback converter, being this second one more suitable for variable output voltage.

For lighting power supplies, power factor correction needs to be provided over 25 W. Figure 1-1 shows the dominating topology used in the 2 mentioned fields depending of the output power.

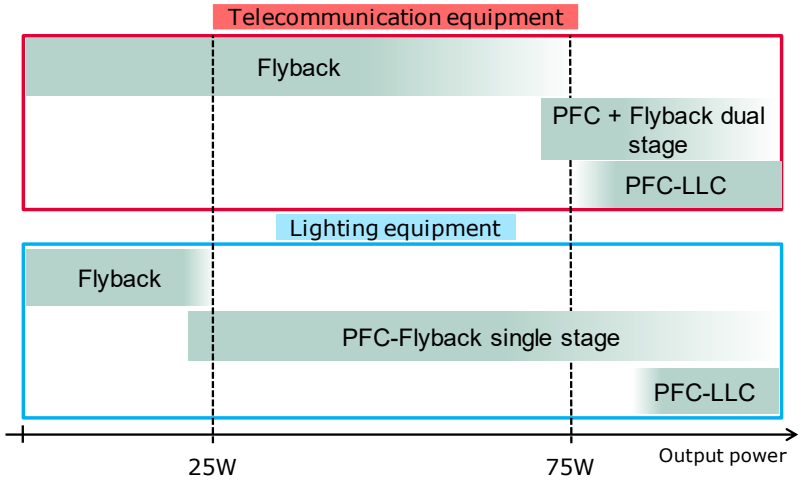

Figure 1-1: Dominant power supply architecture versus output power for lighting and telecommunication equipment.

Flyback converter has the advantage of wide input to output voltage range but it suffer from lower efficiency and bigger transformer size compared to forward converter like the LLC. On the other hand forward converters benefits from high efficiency but lack of wide input to output range.

At the starting date of this work most of the solutions for USB-PD applications were flyback based due to the wide input and output voltage range required. For the input, universal voltage range (100Vac to 264Vac) is required and USB-PD (5V to 20V) for the output.

Further development of the USB-PD standard led to the USB-PD EPR (extended power range) which defines output voltages from 5V to 48V.

The current work aims at improving the efficiency and power density of adaptors and chargers existing at the starting date of this thesis. To achieve such target, this study will focus on the asymmetrical half-bridge flyback converter topology.

Such converter as it will be described in following chapters behaves as a hybrid flyback-forward converter which enjoys the benefits of both types.

The basic schematic of a single stage adaptor based on such topology is shown in Figure 1-2.

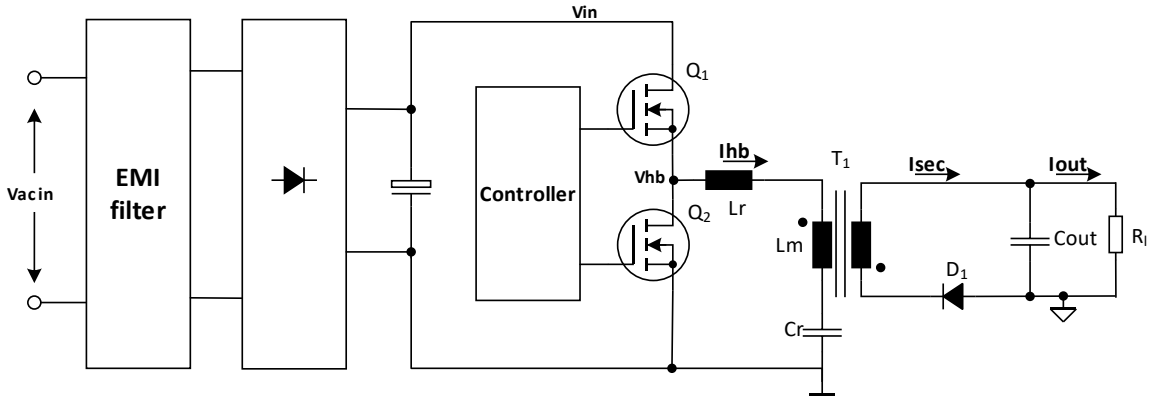

Figure 1-2: Simplified AC-DC adaptor based on the asymmetrical half-bridge flyback converter

Such topology has been chosen due to its known advantages due to zero voltage switching and zero current switching characteristics but mainly due to its hybrid flyback-forward nature.

The asymmetrical half-bridge flyback has been studied in several papers but it has not been used in adaptors due to the limitation of the available control methods to fulfill the requirements.

This work will analyze the limits of power density in power supplies without force cooling. It will study the proposed topology, present innovative new control methods and evaluate its benefits. Furthermore wide band gap (WBG) switches will be used and its performance will be compared with traditional silicon devices. The proposed control methods and the theoretical analysis will be verified on real converter prototypes.

1.1. Thesis objectives

The objectives of the thesis have been defined in the investigation plan presented before starting this work. They are based on the asymmetrical half-bridge flyback converter topology. The main focus of this work are points 3 and 8 which are less developed compare to the rest.

1. Understanding the thermal requirements to achieve the given power density
2. Theoretical analysis of the converter, transfer function, operation modes, etc.
3. To develop the required control algorithms/methods for the different operation modes

4. Dimensioning of the converter to achieve optimum performance over the whole operating range in terms of minimum power dissipation
5. To develop a hardware prototype to verify the theoretical analysis
6. Control algorithms implementation and validation
7. Validation of the prototype considering final application requirements in terms of: efficiency, size, standby power, EMI, protections, load step response, etc.
8. To study the benefits and challenges of using GaN technology to further push efficiency and size reduction of the converter

The organization of the following sections, including the 5 related publications (3 of them in journals with impact index), tries to follow the defined objectives.

1.2. Document organization

The following sections of this work are organized according to the targets described in section 1.1, corresponding to the targets defined in the investigation plan.

Charter 2 analyzes and present the thermal limits for adaptors where non-forced ventilation is available. As well, it introduce the transfer function of the converter.

Chapters 3 to 7 presents 5 different manuscripts publications, every publication proves the results with real converter prototypes:

Chapter 3 present the converter, the operation phases and a first view to the converter dimensioning.

Chapter 4 introduces control methods for different input voltages and introduce the concept of hybrid nature of the converter forward-flyback.

Chapter 5 presents innovative new control methods for low power or low output voltage of the converter. It analyzes the limits of the converter such as operation with low input voltage.

Chapter 6 analyze and compares theoretically and experimentally the behavior of 3 different switches technologies used in the adaptor, silicon (Si), silicon-carbide (SiC) and Galium Nitride (GaN).

Chapter 7 present an AHB flyback converter based on GaN, the design optimization process and analyze the losses in the different components, the results are shown in a very high-density design (112W/inch^3) with outstanding efficiency of 98%.

Finally, chapter 8 presents the conclusion of this work.

2. THERMALS LIMITS VERSUS POWER DENSITY AND CONVERTER TRANSFER FUNCTION

2.1. Thermal limits

The thermal requirements of adaptors are typically defined by the maximum surface temperature. Limited surface hotspots maybe allowed.

Since there is no forced cooling, the only forms of heat dissipation in the adaptor are natural convection of the surrounding air and radiation of the surfaces, this limits in a great manner the amount of heat that the adaptor can dissipate. Other factors can further affect the amount of dissipated heat are for example: the shape of the adaptor, the orientation or placement. Further details about such factor can be found in [1].

Typical values for the surface temperature of the adaptor are 70°C; in more conservative designs only 60°C are allowed under an ambient temperature of 25°C.

In other to have an idea about the power density that we can achieve given a maximum constant surface temperature, it is necessary to fix some of the various degrees of freedom. For this reason we will assume a cubic shape of the adaptor, with upper and lower faces perpendicular to the gravitation field and suspended in free air at 25°C, in such way that the internal heat can be dissipated by radiation and air convection around the cube.

In [2] we find the equations that defines the amount of power that the defined cube can dissipate, this will be described in the following paragraphs.

The power dissipated by radiation is defined by the Stefan-Boltzmann law, which relates the energy flux emitted by an ideal radiator (or blackbody) to the fourth power of the absolute temperature, see equation (2-1):

$$P = \in \sigma A(T_s^4 - T_a^4) \tag{2-1}$$

Where $\in$ is the emissivity factor of the radiating material, σ the Stefan-Boltzmann constant, A the radiating surface area and T_s and T_a the surface and ambient temperatures respectively.

The power dissipated by convection can be calculated from the Nusselt number (Nu), which provides a relation of convective and conductive heat transfer, the thermal conductivity of the air and the area which dissipate the heat. Due to the different positions of the cube surfaces in the fluid (air in this case) the Nusselt number needs to be calculated for the case of the upper, bottom and lateral cube surfaces.

The power dissipated by a surface respond to equation (2-2):

$$P = \mathrm{Nu}(T_s - T_a)k\frac{A}{L} \tag{2-2}$$

Where L is the surface length and k is the thermal conductivity of the air.

For vertical surfaces, we can calculate Nu using equations (4.33) in [2], for the upper surface, we can use equations (4.25) and (4.39) and for the bottom surface we can use (4.40).

Adding the power dissipated by radiation and convection, we can calculate the total amount of power that the cube can dissipate under the described conditions. This is shown in Figure

2-1 where additional surface temperatures has been added to get a better overview.

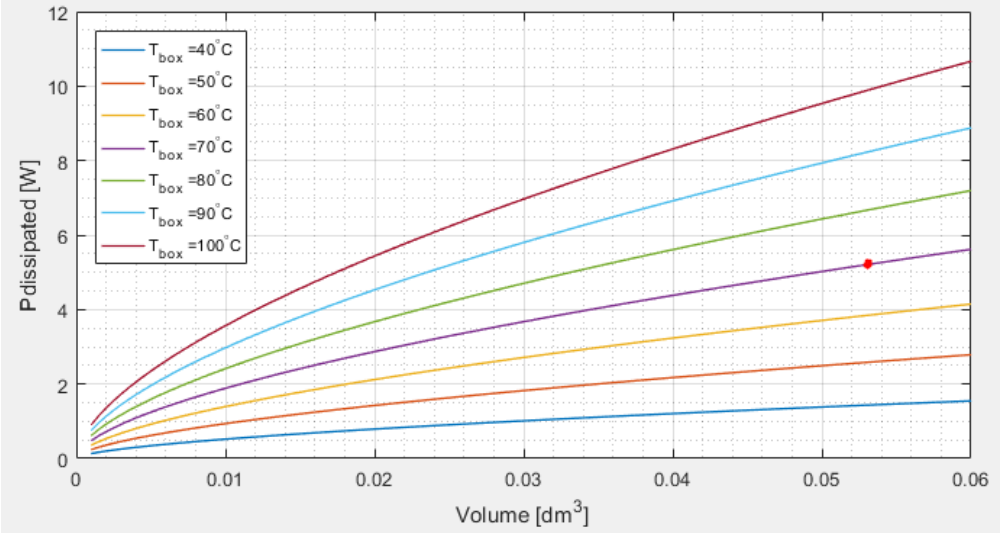

Figure 2-1: Power dissipated by a cube with constant surface temperature vs. its volume.

For a given nominal power (P_n) of an adaptor that would fit in the cube, we can calculate the corresponding power density and efficiency required to match the power losses.

$$P_{den} = \frac{P_n}{V} \tag{2-3}$$

$$\eta = \frac{P_n}{P_n + P_{loss}(V)} \tag{2-4}$$

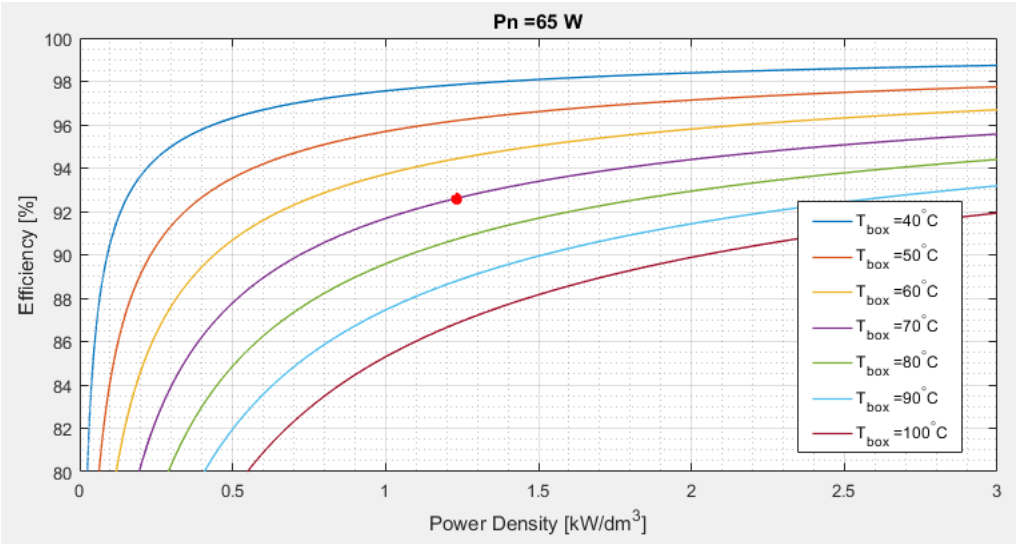

Figure 2-2: Efficiency required by a cubic 65W adaptor vs. its power density for different surface temperatures (red point indicates 1.23 KW/dm^3 = 20W/inch^3)

For every point of the curves in Figure 2-1, we can calculate the power density and the efficiency matching the power dissipated. This way we obtain the relation of the efficiency required for a given power density.

Figure 2-2 shows the case for a 65W adaptor, the point marked in red shows that for 20W/inch^3 an efficiency of at least 92.5% is required, this represents a reasonable target compare to state of the art solutions.

For the case of 240 W nominal power we can redraw Figure 2-2 and obtain Figure 2-4.

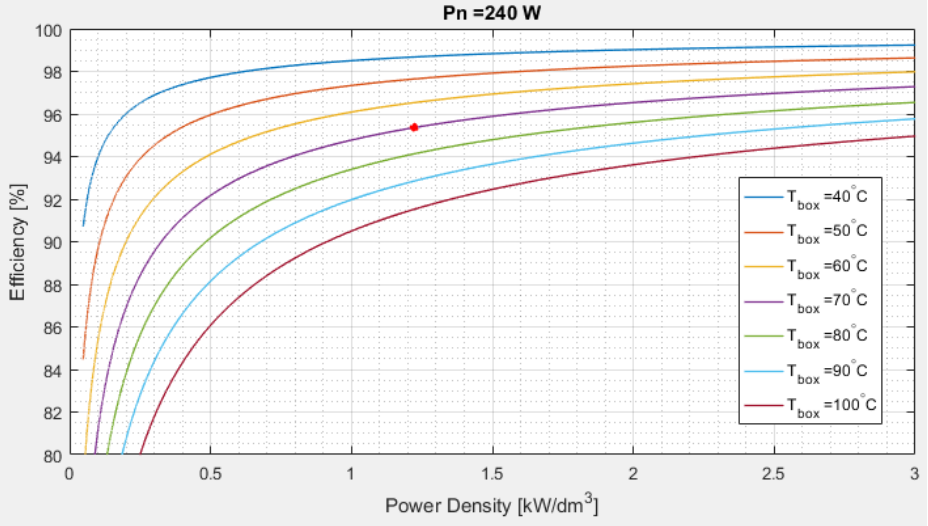

Figure 2-3: Efficiency required by a cubic 240W adaptor vs. its power density for different surface temperatures (red point indicates 1.23 Kw/dm^3 = 20W/inch^3)

It can now observed that to obtain the same power density we had in the case of 65W, we need an efficiency over 95%. This can be explained by the increase of the volume compare with the increase of the surface of a cube, power of 2 vs. power of 3 respectively.

It is important to mention that the obtained figures, dissipated power, power density and efficiency, are only indicative due to the various factors affecting the final temperature of the adaptor, but they provide a first reference point for further steps.

2.2. Transfer function of the power stage

The transfer function of the power converter can be different depending on the control methods used (CCM, DCM, etc) and the defined input and output variables of the plant.

There are existing studies about the transfer function of the asymmetrical half-bridge converter. The results will be reviewed in this chapter but no further analysis will be done as they are beyond the scope of this work.

In [3] the average state space equations are presented. The control method assume no dead times between the switches of the half bridge therefore an ideal PWM with duty cycle (D) is applied to the power stage providing an output voltage (V_{out}).

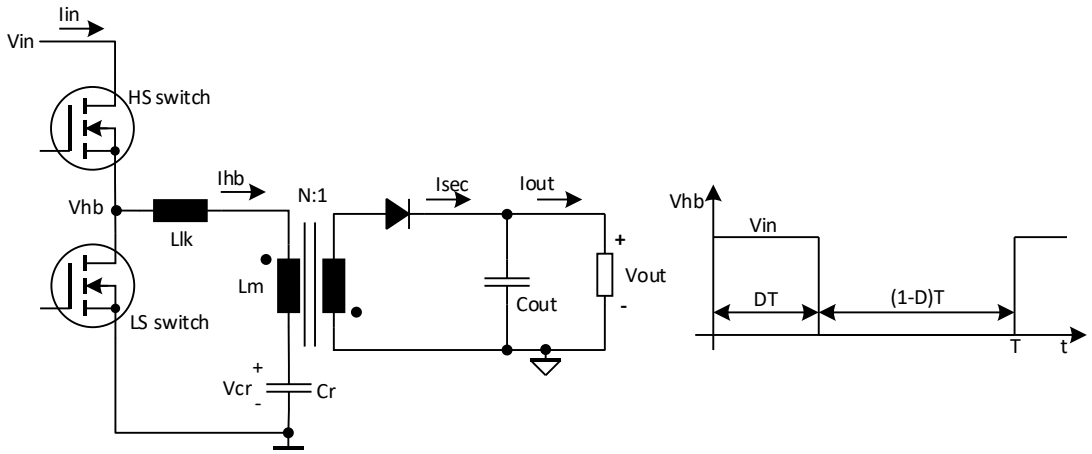

Figure 2-4: Converter stage and signals used to define the transfer function, input: D, output: Vout

The defined input for the transfer function is the duty cycle (D), and the output is the converter output voltage (V_{out}).

From the state space equations, a small model is extracted that will define the frequency response of the converter.

An example of the frequency response of the plant for a converter dimensioned for 20V output wide input range is shown in Figure 2-5.

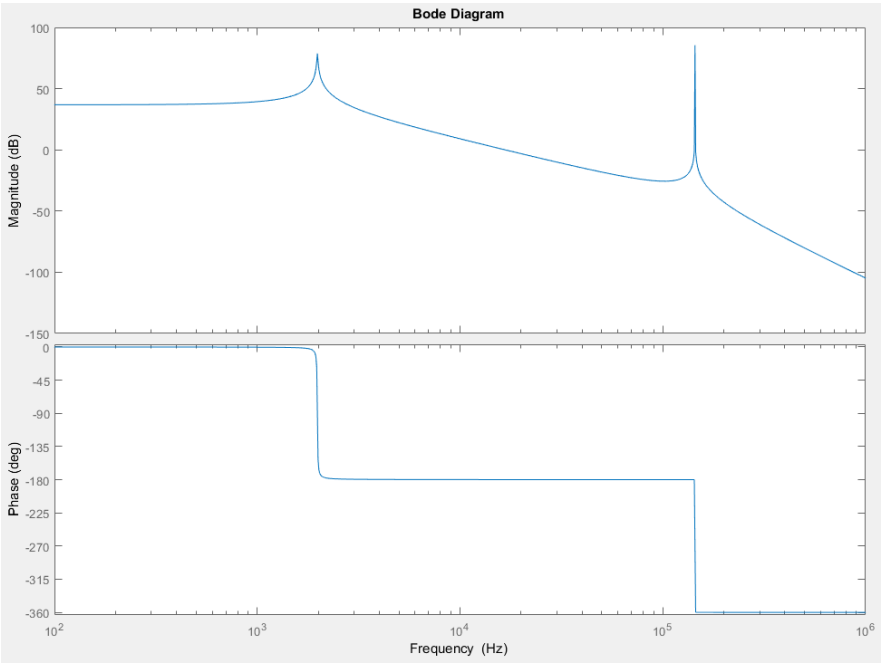

Figure 2-5: Frequency response of the transfer function $V_{out}(D)$ of a converter.

(V_{out} = 20V, R_l = 10Ω, C_{out} = 1000µH, C_r = 0.8 µC, N = 2.83, L_m = 51µH, L_{lk} = 1.1µH)

The response is similar to resonant buck converter, with two pair of conjugate poles as shown in (2-5), this is mainly because the analyzed topology has the nature of an isolated buck, further details can be found in [3].

$$\frac{V_{out}}{D} = \frac{A}{(s^2 + Bs + C)(s^2 + Ds + E)} \tag{2-5}$$

2.3. References

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[2] Handbook of heat transfer, editors, W.M. Rohsenow, J.P. Hartnett, Y.I. Cho, 3rd edition, Publisher: McGraw-Hill, New York, 1998.

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3. PUBLICATION 1: ASYMMETRICAL FLYBACK CONVERTER IN HIGH DENSITY SMPS

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ASYMMETRICAL FLYBACK CONVERTER IN HIGH DENSITY SMPS

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Abstract: In recent years the number of electronic devices, such as mobile phones, tablets, laptops, etc., have increased dramatically. The need for a versatile adapter which can be used for several devices, with high efficiency and minimum size to ensure minimal waste of energy and electronic parts, is highly desired.

An innovative USB-PD adaptor, based on the asymmetrical PWM flyback topology will be proposed, which is able to supply 65W, has peak efficiency close to 95% and a minimum of 93% at full load over input voltage and a power density of 20W/inch^3 cased. The topology selection, dimensioning and control method will be explained in this paper, and measurement results on a prototype will be presented.

3.1. Introduction

The typical state-of-the-art solution for USB-PD adaptors consists of two power stages in order to resolve the wide input (90V to 265V) and output voltage (5V to 20V) ranges, where the second stage is typically a buck converter. Employing two stages however, will most often result in a more expensive and bulky solution than single stage concepts.

The potential of reducing the adaptor size is also limited by the maximum losses that are generated by the adaptor in any given operating point. In a power adaptor where the heat is only dissipated passively, the maximum allowed surface temperature will determine the minimum allowed efficiency at full load, which is typically the worst case operating point.

In this paper a very compact and highly efficient, single stage solution, based on an asymmetrical PWM flyback converter addressing those challenges will be presented.

3.2. Multi-objective optimization

In order to identify the best suited topology for a high density adaptor, several different concepts have been comparatively evaluated by means of a multi-objective optimization, which considers all available degrees of freedom in the design of each concept. As a result, an

efficiency vs. power density (η-ρ) Pareto front is calculated for each topology (cf. Figure 3-1), indicating the achievable trade-off between the performance and dimensions. The considered topologies include:

1. PFC flyback with secondary side power pulsation buffer;
2. Flyback converter with a fixed output voltage and subsequent buck converter
3. Flyback converter with wide output voltage range
4. Cascaded asymmetrical PWM flyback where the primary side consists of two cascaded half-bridges Flyback
5. Asymmetrical PWM flyback converter

As shown in Figure 3-1, based on the optimization results, the asymmetrical PWM flyback concept is identified as the most promising candidate.

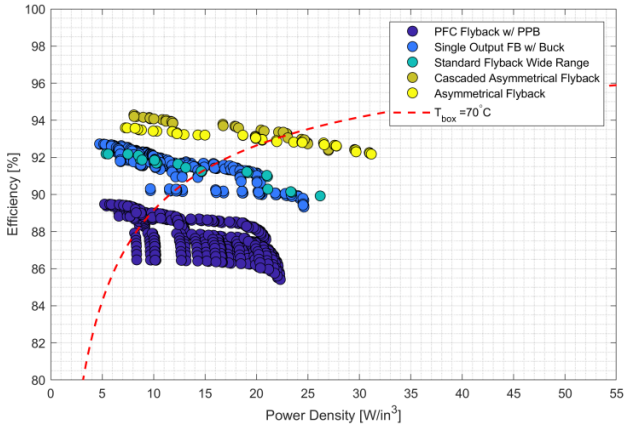

Figure 3-1: Multi-objective optimization results of several different adaptor concepts for full load (P_{out} = 65W), V_{out} = 20V and low line (V_{in} = 90Vac) operation. Additionally, also the thermal limit line is shown, which defines the minimum efficiency required for a given power density in order to keep the surface temperature of the adaptor below 70°C.

3.3. Asymmetrical PWM flyback

3.3.1. Topology

To achieve an outstanding power density, a combination of the right topology, dimensioning

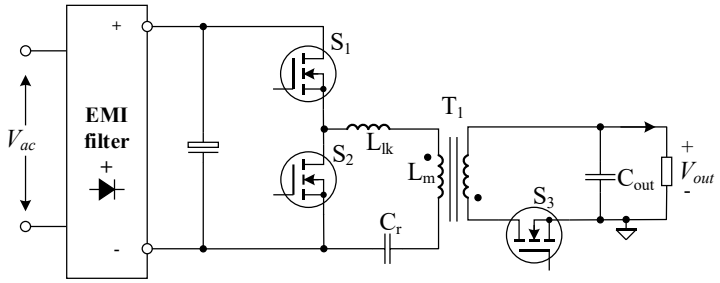

Figure 3-2: Asymmetrical PWM flyback with synchronous rectification

and advanced control techniques have to be used. In particular the presented topology of the asymmetric PWM flyback, see Figure 3-2, can achieve ZVS and secondary ZCS which helps to reduce the losses in parasitic elements and maximize efficiency, additionally a synchronous rectification will be used in the secondary side to further boost efficiency.

It is important to notice the LC tank driven by the half bridge; it is formed by a series capacitor and the transformer leakage inductance (or external inductance plus leakage inductance).

Please note that the same converter can also be realized by connecting the resonant capacitor Cr and primary of the transformer between positive node and middle point of the half bridge. That would result in similar operation but with the roles of the LS switch and the HS switch inverted.

3.3.2. Operation phases

The operation phases of the asymmetrical PWM flyback can be divided in 4 parts:

1. Energy taking phase
2. Dead time 1
3. Energy transfer phase
4. Dead time 2

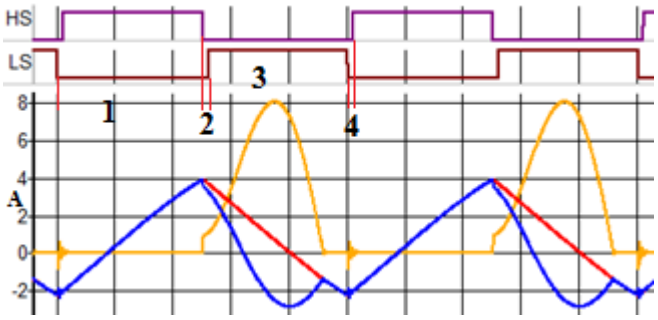

Figure 3-3: Typical waveform of the Asymmetrical PWM flyback (blue: LC tank current, red: magnetizing current, yellow: secondary current)

Phase 1:

During the energy taking phase the high switch is ON and low switch OFF, the current increases in the transformer and resonant capacitor Cr gets charged, the secondary diode is polarized inversely hence no energy is transmitted to the secondary side.

Phase 2:

In this phase both switching are off. The flowing current in the transformer inductance will force the half bridge middle point to drop until the body diode of the lower mosfets clamp the voltage.

Phase 3:

During the energy transfer phase, the low side is switched ON with ZVS condition, the high side switch is OFF, the voltage in the transformer has reversed and the secondary diode starts conducting. The energy stored in the primary transformer and resonant capacitor is transferred to the output. Due to LC tank formed by the transformer leakage inductance and the resonant

capacitor, the secondary current follows a sine wave with period defined by both elements Llk and Cr.

Phase 4:

In the last phase both transistors will be OFF and the negative current in the transformer will force the half bridge middle point to increase its voltage. That will lead to phase 1 with ZVS condition for the high side switch.

3.3.3. Energy storage

It is worth to mention why this topology can reduce the size of the transformer compare to a standard or active clamp flyback under similar conditions.

While in a standard flyback the transformer has to store all the energy in the transformer before it releases to the secondary side, in the asymmetrical flyback converter the energy to be transfer to the secondary side is shared between the resonant capacitor and the transformer.

As explained in the operation phases, in phase 3 the energy of the capacitor is transferred to the secondary in a forward mode and the magnetizing energy of the transformer as in a standard flyback.

When the converter is running in stable operation, the average voltage of the resonant capacitor is approximately the output voltage multiplied by the turn ratio of the transformer.

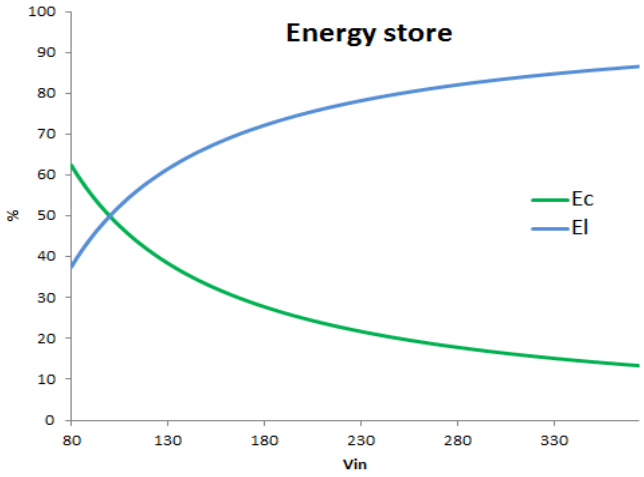

Figure 3-4: Energy sharing between transformer and resonant capacitor over input voltage.

Depending on the input voltage, the sharing of the energy between the capacitor and the transformer changes.

It is obvious that the size required by the resonant capacitor is almost neglectable.

At higher input voltage more energy is transferred from the transformer to the output, but the peak of the flux is constant as the increase of frequency compensates for it, as typically observed in flyback converter.

This phenomenon explains why the asymmetric PWM flyback is, as confirmed by the Multi-objective optimization in section 3.2, uses smaller transformer and therefore is the most promising topology for high-density adapters.

3.4. Dimensioning and control of the converter

3.4.1. Safe and efficient operation

For proper and reliable operation of the converter when using Mosfets as switches, we need to ensure that independent of the input and output voltage and output load no body diode cross conduction happens, meaning that one Mosfet of the half bridge is switched ON while the body diode of the other is still conducting, that would result in a current spike through the bridge due to the diode reverse recovery time. Therefore we need to ensure that the magnetizing current of the transformer oscillate around zero.

On other hand, to maximize efficiency we need to ensure zero voltage switching (ZVS) on the switching devices to avoid losses on their parasitic output capacitance and secondary side zero current switching (ZCS) to avoid loses due to the secondary leakage inductance.

3.4.2. Duty cycle and output voltage

Assuming negligible dead times, we can define the duty cycle as expressed by equation (3-1):

$$D = \frac{T_{hs}}{T_{hs} + T_{ls}} \tag{3-1}$$

Where Ths is the ON time of the high side switch and T_{ls} is the ON time of the low side switch in Figure 3-2.

The proposed topology provides an output voltage proportional to the duty cycle, according to (3-2):

$$V_{out} = D\frac{V_{in}}{n}\frac{L_m}{L_m + L_{lk}} \tag{3-2}$$

Ideally we would not need to compensate for output load changes but in reality we need to compensate for energy transfer losses and variations of the duty cycle due to the dead times.

3.4.3. Output load effect

No load operation

At no load operation, if no burst mode is implemented we will circulate energy but we will

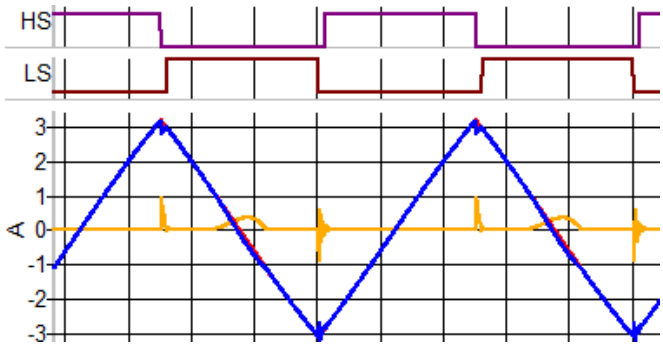

Figure 3-5: No load operation waveforms, blue: tank current, red: magnetizing current, Orange: transformer secondary current.

not transfer it to the output, see Figure 3-5.

In this case ZVS operation is ensured as the magnetizing current of the transformer will oscillate around zero.

Operation under load conditions

If we maintain a fix duty cycle and connect a load at the output (Figure 3-3), the magnetizing current of the transformer will be shifted up, due to the output current being reflected in the primary side. The amount is given by equation (3-3).

$$\Delta I_{mag} = \frac{I_{out}}{n} \tag{3-3}$$

The dimensioning of the converter needs to ensure not only that the magnetizing current stays around zero but as well that it goes negative enough to ensure ZVS operation is achieved considering the parasitic capacitance connected to the middle point of the bridge. Additionally proper dead times have to be implemented.

3.4.4. Asymmetrical PWM flyback control method

As shown by equation (3-2) the output voltage is proportional to the duty cycle. That allows controlling the output voltage easily.

But in order to regulate the output voltage and maintain efficiency the proposed control method is based on keeping the energy transfer time (LS switch ON) constant, to a value being equal or slightly above half of the resonant period formed by Cr and the primary leakage inductance (and eventually an external series inductance, if present), and regulate the input voltage and load by modulating the on time of the high side switch.

Normally, for variable output voltage, such condition is guaranteed only at the maximum output voltage, which is the case where maximum efficiency is required.

1. The advantages of the proposed control method are:
2. Zero current switching (ZCS) in the secondary, which avoids possible losses in the secondary side snubber due to non-zero current in the secondary leakage inductance
3. It makes the job of the synchronous rectifier easier and avoid late switch off

It results in an output current waveform, which has lower RMS value compared to other topologies, such as standard flyback or active clamp flyback, reducing in this way resistive loses. See Figure 3-3.

3.4.5. Transformer dimensioning

In order to ensure the wide range operation requirements, we can start our design by looking at two factors:

1. Absolute input voltage range (Vin_max)
2. Secondary mosfets voltage rating (Vds_max)

To have a safe operation the transformer ratio (n) need to be bigger than:

$$n > \frac{V_{in\_max}}{V_{ds\_max}} \tag{3-4}$$

but on other hand, to be able to regulate, the maximum output voltage reflected in the primary

has to be below the minimum input voltage:

$$n * V_{out\_max} < V_{in\_min} \tag{3-5}$$

It is desired to keep the value of n in the low range to avoid high RMS secondary currents at low input voltages.

Once the transformer ratio is selected considering the equations (3-4) and (3-5), we can calculate the duty cycle for a given input and output voltage:

$$D \approx \frac{n * V_{out}}{V_{in}} \tag{3-6}$$

In the next step, we need to ensure sufficient magnetizing current:

$$I_{mag\_pp} > \frac{2 * I_{out\_max}}{n} \tag{3-7}$$

And add a margin to ensure ZVS considering parasitic capacitances associated to the half bridge middle point. Such current margin will allow overpower capability required in most cases.

In the next step we need to consider the desired operating frequency range to determine the transformer primary inductance. Since the proposed control method fix the time of the low side switch and regulate with the high side ON time the resulting frequency range will variate with the input and output as indicated in equation (3-8):

$$L = \frac{D(V_{in} - nV_{out})}{FI_{mag\_pp}} \tag{3-8}$$

where F is the desired switching frequency and D is the duty cycle, which can be obtain from equation (3-2).

For a wide input range converter we should consider the corner cases to limit the minimum and maximum operation frequency once we fix the inductance value.

3.5. Experimental results

A 65W prototype (Figure 3-6) using 500V/140mOhm Infineon MOSFETs has been

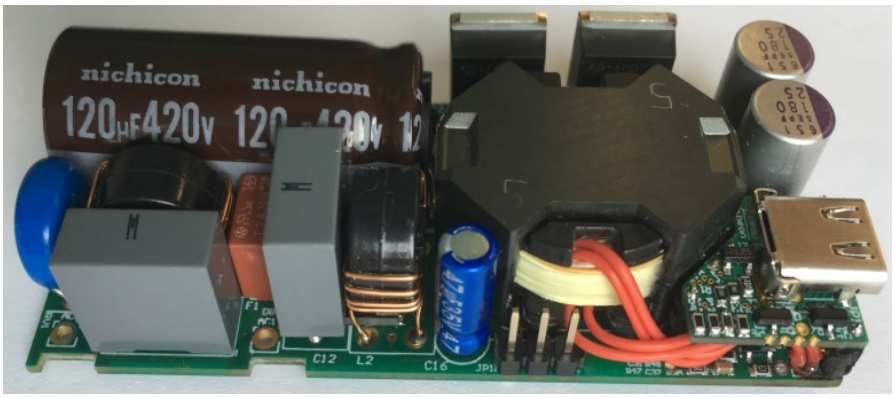

Figure 3-6: USB-PD 65W prototype (27w/inch^3 uncase, 20w/inch^3 cased)

developed. It supports USB-PD with different output voltage profiles ranging from 5V/3A to 20V/3.25A. The operation frequency varies from 100 kHz to 220 kHz depending on the input voltage. The maximum efficiency achieved was 94.8%, please refer to Figure 3-7.

3.6. Conclusions

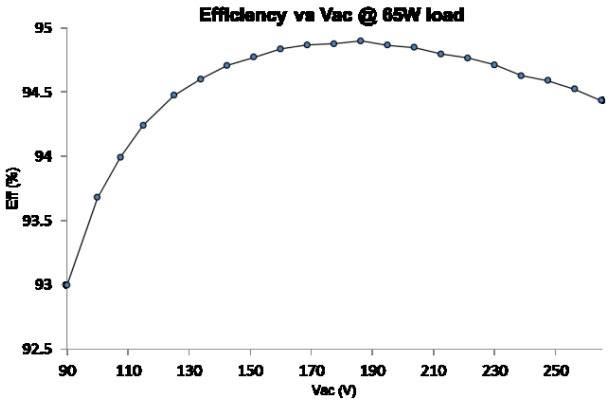

Figure 3-7: Full load efficiency over input voltage

The proposed asymmetric PWM flyback concept has been identified as the most promising topology for highly efficient and very compact USB-PD adaptors, due to its forward energy transfer capability compare to standard flyback where the transformer has to store all the energy. The proposed control method and topology dimensioning ensure on one hand high efficiency, due to guarantee ZVS and ZCS operation, and on the other hand an easy controllability of the output voltage. The performance has been demonstrated with a 65W prototype which achieves a minimum efficiency of 93% at full load and low line operation.

3.7. References

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4. Publication 2: Resonant Hybrid Flyback, a New Topology for High Density Power Adaptors

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RESONANT HYBRID FLYBACK, A NEW TOPOLOGY FOR HIGH DENSITY POWER ADAPTORS

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Abstract: In this article, an innovative power adaptor based on the asymmetrical pulse width modulation (PWM) flyback topology will be presented. Its benefits compared to other state-of-the-art topologies, such as the active clamp flyback, are analyzed in detail. It will also describe the control methods to achieve high efficiency and power density using zero-voltage switching (ZVS) and zero-current switching (ZCS) techniques over the full range of the input voltage and the output load, providing comprehensive guidelines for the practical design. Finally, we demonstrate the convenience of the proposed design methods with a 65 W adaptor prototype achieving a peak efficiency of close to 95% and a minimum efficiency of 93.4% at full load over the range of the input voltage, as well as a world-class power density of 22 W/inch^3 cased.

Keywords: adaptor; flyback; power density; efficiency; MOSFET; GaN

4.1. Introduction

In recent years, the amount of highly portable electronic devices—such as mobile phones, tablets, laptops, etc.—has increased significantly to satisfy social needs, communication needs, and enable access to a large variety of cloud-based services. Simultaneously, the need for power adaptors with high efficiency, to ensure minimal waste of energy, and minimally-sized electronic parts is highly desired to satisfy the portability premise [1].

Power adaptors must feature a wide input voltage range, typically ranging from 90 Vac to 264 Vac, and passive cooling. For low-power converters in which power factor correction is not required, flyback or flyback-based converters are preferably used due to their capability to handle a wide input to output voltage ratios [2]-[3]. Additionally, the potential for reducing the adaptor size is limited by the maximum losses that are generated at any given operating point. For a power adaptor where the heat is only dissipated passively, the maximum allowed surface temperature will determine the minimum allowed efficiency at full load and the minimum input voltage, which is typically the operating point characterized by a worst-case condition.

In a traditional flyback converter, the transformer acts as an energy storage element resulting in a larger transformer compared to forward topologies. This limits the maximum achievable power density. Over the years, increasing the switching frequency has been used to reduce the transformer size. Nevertheless, as the frequency increases, the energy losses in the parasitic elements (mainly transformer leakage inductance) and output metal-oxide-semiconductor

field-effect transistor (MOSFET) capacitance become more significant. To overcome the issues related to higher switching frequencies, different variants of the flyback topology have become popular, all of which aim to recycle the energy of the parasitic elements, with the active clamp flyback being the most well-known variant in either complementary or non-complementary versions [4]-[5]. However, the original challenge related to the size of the transformer still remains: The energy to be transferred to the secondary side first has to be stored in the transformer.

In recent years, new transistor technologies allowing higher switching frequencies have become popular. Examples of these are silicon carbide and GaN MOSFETs [6]-[8]. The use of these new switches in active clamp flybacks seems to be able to solve both of the major limitations of high power density adaptors: Recycling energy from the parasitic elements while reducing the transformer size. Nevertheless, the higher switching frequencies are not exempt from problems. Faster switching frequencies raise a new challenge: To fulfill conductive or radiated electromagnetic interference (EMI) regulations, such as EN55022. Another limitation of this solution is the higher cost of special devices in a market where the total system cost is very sensitive.

The creatively titled asymmetrical duty cycle flyback converter is a hybrid between a flyback and a forward converter [9]-[10] that addresses the major problems related to high-density adaptors while using moderate switching frequencies. In this paper, a solution based on such a converter, and the control methods that ensure zero voltage switch (ZVS) and zero current switch (ZCS) over line and load will be presented.

4.2. Asymmetrical Duty Cycle Flyback

4.2.1. Topology

The general schematic of the asymmetrical duty cycle flyback converter is presented in Figure 4-1, including the elements needed in an adaptor, such as the EMI filter and the input rectifier [9]. It is important to note here the capacitor (*Cr*) is in series with the transformer, which is the major difference with respect to the traditional flyback and will make the converter behave as a hybrid flyback and a forward converter.

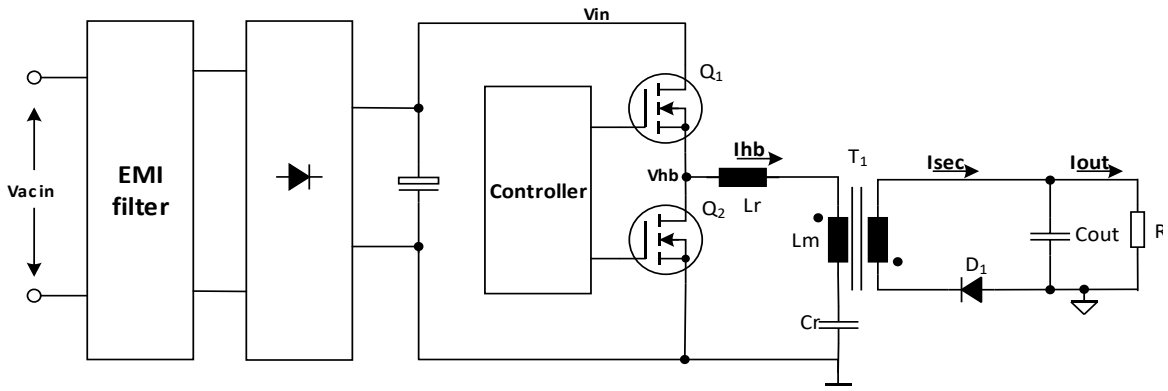


Figure 4-1: Simplified adaptor schematic of an asymmetric pulse width modulation (PWM) half-bridge (HB) flyback.

To achieve outstanding power density, a combination of the right topology, dimensioning, and advanced control techniques have to be used. In particular, the presented topology with the right control method can achieve ZVS and secondary ZCS under all conditions of input

voltages and output current. Moreover, it recycles the energy of the transformer leakage inductance, which helps to reduce the losses and maximize efficiency. To further boost efficiency, synchronous rectification can be used in the secondary side.

The power circuit in the primary is realized by an LC tank driven by a half-bridge similar to an LLC converter. The resonant inductor *Lr* represents the series inductance, *Lr* being either the transformer leakage inductance or the leakage inductance plus an external inductor. It is worth mentioning that the converter can also be implemented by connecting the resonant capacitor *Cr* and the primary side of the power transformer between the positive node and the middle point of the half-bridge. This would result in a similar operation, but with the roles of the switch Q1 and Q2 inverted. A second resonant circuit is formed by *Lr* + *Lm* and *Cr*.

4.2.2. Resonant Operation Phases

The operation phases of the resonant asymmetrical duty cycle flyback can be divided into six phases as schematized in Figure 4-2:

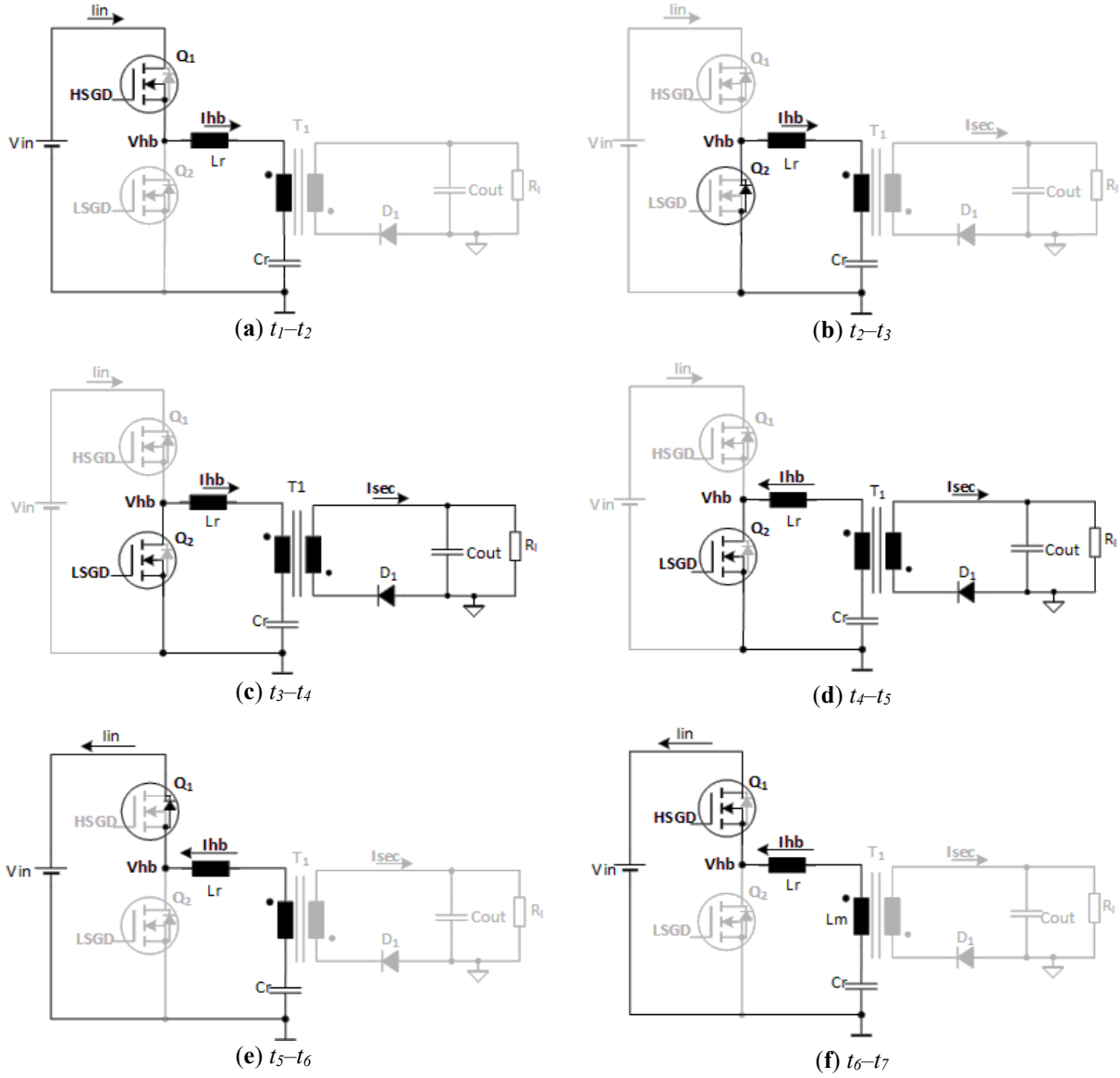


Figure 4-2: Asymmetric flyback converter operation phases.

Phase 1, t_1 to t_2: During this phase, the Q_1 switch is on and the Q_2 switch is off. The current increases in the transformer and the voltage in the resonant capacitor *Cr* increases; both elements store energy. The secondary diode D_1 is biased inversely hence no energy is transferred to the secondary side.

Phase 2, t_2 to t_3: In this phase, both switches Q_1 and Q_2 are off. The current in the transformer T_1 will force the half-bridge middle point V_{hb} to drop until the body diode of Q_2 MOSFET clamps the voltage. The primary side of the transformer now has the same voltage as the capacitor C_r.

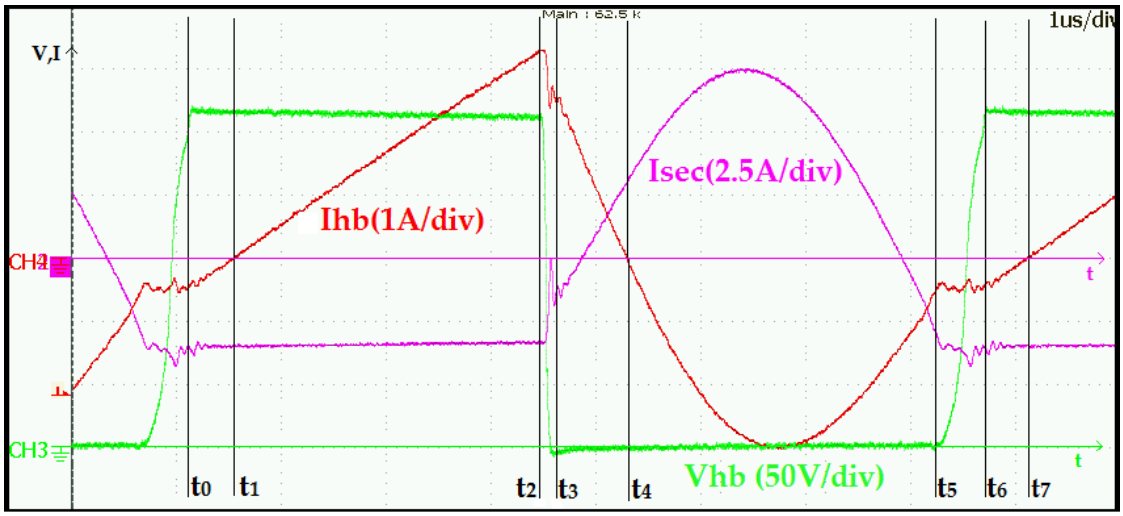


Figure 4-3: Resonant asymmetric flyback converter waveforms, Ihb: tank current, Vhb: half bridge middle point voltage, Isec: secondary transformer current.

Phase 3, t_3 to t_4: During this phase the Q_1 switch is off and Q_2 is switched on under the ZVS condition; the secondary voltage is now equal to the voltage across the capacitor C_r divided by the turns ratio. The current starts flowing through D_1 and the energy stored in the capacitor and the transformer is transferred to the output. Due to the LC tank formed by the L_r (transformer leakage inductance) and the resonant capacitor, the current in the secondary follows a sine wave with the period defined by the resonant frequency of those elements (see Figure 4-3). The current in the primary is the sum of the magnetizing current plus the reflected secondary current. The current in the resonant tank is still positive, mainly driven from the transformer T_1 magnetizing inductance, and flows into the resonant capacitor C_r, charging it further.

Phase 4, t_4 to t_5: This phase is a continuation of the previous one. The Q_1 switch is off and Q_2 is switched on; the energy is still being transferred to the secondary side but the resonant tank current inverts its direction driven by the voltage in the resonant capacitor C_r. The energy of the resonant capacitor is not only transferred to the secondary side but also contributes to bringing the magnetizing current of the transformer T_1 to a negative level as long as Q_2 is on.

Phase 5, t_5 to t_6: In this phase, both switches Q_1 and Q_2 are off. The negative current induced in the transformer during the previous phase will force the half-bridge middle point V_{hb} to increase its voltage until it is clamped by the body diode of Q_1.

Phase 6, t_6 to t_7: Similarly to phase 1, Q_1 is switched on with the ZVS condition and Q_2 is switched off, but the current in the transformer resonant tank is still negative, meaning that the excess of energy in the tank will be sent back to the input.

4.3. Asymmetrical Duty Cycle Flyback Control Methods

4.3.1. Duty Cycle and Output Voltage

Assuming negligible dead times, we can define the duty cycle as expressed by the Equation (4-1):

$$D = \frac{T_{Q1}}{T_{Q1} + T_{Q2}} \tag{4-1}$$

where T_{Q1} is the ON time of the Q_1 switch and T_{Q2} is the ON time of the Q_2 switch in Figure 4-1.

As described in detail in [11]-[12], the proposed topology provides an output voltage proportional to the duty cycle, according to:

$$V_{out} = D \frac{V_{in}}{N} \frac{L_m}{L_m + L_{lk}} \tag{4-2}$$

where n represents the winding ratio between the primary and the secondary of the transformer.

Equation (4-2) shows that the output voltage is independent of the output current due to the fact that components without loss are assumed. However, in a real converter, it is necessary to compensate for energy losses in non-ideal components (i.e. capacitor ESR) and variations of the effective duty cycle due to the dead times.

4.3.2. Considerations for ZVS Operation

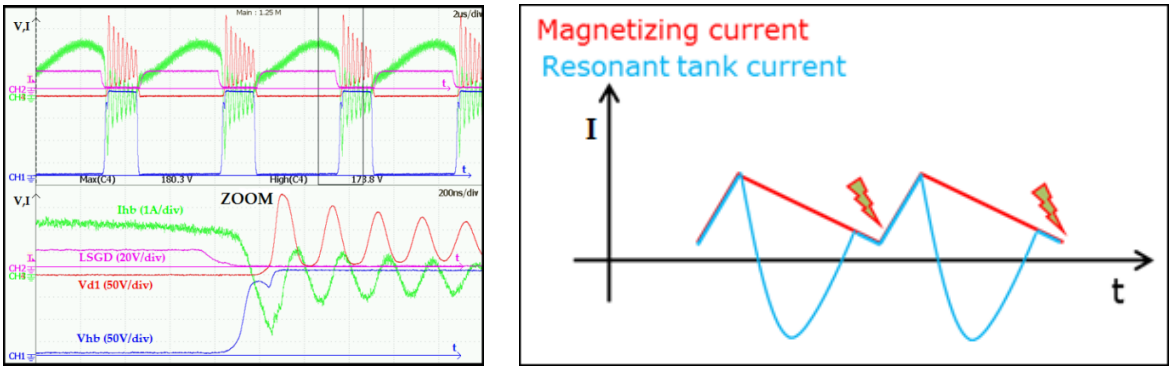
In order to achieve the ZVS condition before the MOSFETs are switched on, the right polarity of the tank current as well as sufficient energy in the tank are needed to turn the V_{hb} around and ensure ZVS. Not doing so will create hard switching, undesired oscillations and, in the worst case, body diode cross conduction.

There are different ways to achieve ZVS, either using the energy in *Lr*, *Lm* or both. Due to the current flowing though *Lr* and Lm at t_2 (see Figure 4-3), it is easy to achieve ZVS for Q_2. For Q1, ZVS can be achieved by:

1. Ensuring that enough current flows through the *Lr*. However this solution is compromising: Due to the sharp *di/dt* on the secondary leakage inductance, the voltage across D_1 will oscillate resulting in higher voltage requirements and in high EMI.
2. Ensuring that enough current flows through the magnetizing inductance, due to the larger value of *Lm* compared to *Lr*. This is the preferred way to ensure ZVS. Furthermore, oscillations in the output can be avoided if the secondary current is zero (ZCS) (*Isec* @ t_5 in Figure 4-3).

Figure 4-4b shows that the use of a too-high switching frequency, or high inductance, does not allow the transformer magnetizing current to reverse its polarity when Q2 is switched off. This condition forces the tank current to flow through the body diode of Q2. When Q1 is switched on, a high current will flow through the half-bridge due to the reverse recovery time

of the diode, eventually damaging the MOSFETs.



(a) (b)

Figure 4-4: Undesired conditions for ZVS operation: (a) ZVS is achieved with Lr, large oscillations are observed in D1 voltage due to secondary leakage inductance (b) tank current polarity does not allow ZVS operation and leads to body diode cross-conduction when Q1 is switched on.

4.3.3. Proposed Resonant Operation

Taking into account all the considerations previously described, the proposed control method is based on keeping the energy transfer time (T_t) constant (t_3 to t_5 in Figure 4-3), and approximately equal to a value around half of the resonant period of circuit formed by *Cr* and *Lr*. The regulation of the converter is then achieved by modulating the on time of the high side switch (Q_1) (t_0 to t_2 in Figure 4-3). This method is illustrated in detail in Section 3.5.

This approach with the proper dimensioning of the topology [9] has the following advantages:

1. Zero current switching (ZCS) in the secondary side, which avoids losses in the secondary side snubber due to the non-zero current in the secondary leakage inductance.
2. It allows an easier drive of the synchronous rectifier because it avoids late switch off, i.e., as happened in CCM-operated flyback converters [6].
3. It avoids double SR (synchronous rectifier) pulses as can happen in active clamp flyback converters [3].
4. It results in an output current waveform that has a lower RMS (root mean square) value compared to other topologies, such as standard flyback or active clamp flyback converters, by reducing resistive losses (as shown in Figure 4-3).

4.3.4. Understanding the Energy Storage

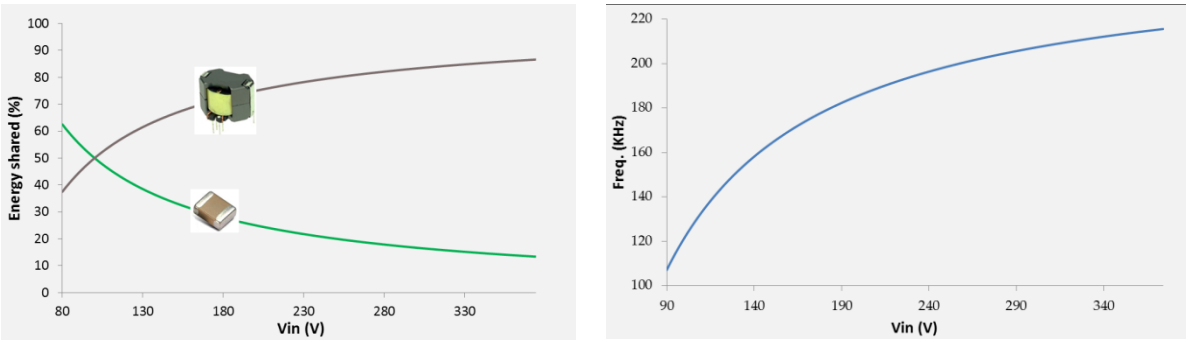
Looking at the energy stored during the charging phase helps to understand why this topology allows a reduction of the size of the transformer compared to a standard or active clamp flyback converter when the same switching frequency is used. While in a standard flyback or ACF (Active Clamp Flyback) all the energy has to be stored in the transformer before releasing it to the secondary side, in the asymmetrical flyback converter, the energy stored is shared between the resonant capacitor and the transformer, resulting in a more relaxed transformer requirement and therefore a smaller size.

Under the condition that the charge time is very small compared to the resonant period ($t_c \ll 2\pi\sqrt{(L_m + L_r)C_r}$), the increment of stored energy in the resonant capacitor (C_r) and the

transformer primary inductance ($L_{lk} + L_m$) depends on the voltage shared between both of them during the charge phase; this is shown in Figure 4-2a, considering that the average voltage across the resonant capacitor is proportional to the output voltage as indicated in (4-3).

$$V_{cr\_avg} = NV_{out} \tag{4-3}$$

It easy to note that the percentage of energy shared depends on the input voltage as shown in Figure 4-5a.



(a) (b)

Figure 4-5: (a) Percentage of energy stored during the charge phase of the converter over V_{in}, V_{cr} = 50 V; (b) switching frequency of the resonant converter over Vin using the proposed control method.

It can be observed in Figure 4-3 that the power taken from the input source, under the condition $t_c \ll 2\pi\sqrt{(L_m + L_r)C_r}$, can be calculated by the Equation (4-4):

$$P_{in} = \frac{1}{T}\int_{t_0}^{t_6} V_{in}\, I_{in}(t)dt = \frac{V_{in}(I_{hb\_h} + I_{hb\_l})}{2T} t_c \tag{4-4}$$

where I_{hb_h} and I_{hb_l} are the $I_{hb}(t)$ currents at t_0 and t_2, see Figure 4-3, and T is the period from t_0 to t_6.

On the other hand, with the same approximation, the charge (t_c) and discharge ($t_d = T_t$) times of the transformer can be determined by the voltage applied to the transformer during each phase:

$$t_c = \frac{I_{hb\_pp} L_p}{V_{in} - NV_{out}} \tag{4-5}$$

$$t_d = \frac{I_{hb\_pp} L_p}{NV_{out}} \tag{4-6}$$

where $I_{hb\_pp} = I_{hb\_h} - I_{hb\_l}$.

Neglecting dead times, the period T can be extracted by adding tc and td. By replacing T and t_c in Equation (4-4), the following expression for the input power can be derived:

$$P_{in} = \frac{NV_{out}(I_{hb\_h} + I_{hb\_l})}{2} \tag{4-7}$$

Assuming an ideal system with no losses, where all the energy taken from the input is transferred to the output ($P_{in} = P_{out}$), I_{out} can be calculated as follows:

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{N\left(I_{hb\_h} + I_{hb\_l}\right)}{2} \tag{4-8}$$

Equation (4-8) shows that for the given control method the output current is independent of the input and output voltages.

From Figure 4-5 it can be observed that for the higher input voltages the portion of power transferred from the resonant capacitor is lower; this means that the transformer always stores the same amount of energy (same I_{hb_h} and I_{hb_l} over the input voltage) but it transfers more power because of the higher switching frequencies. This is different behavior compared to a standard flyback converter or an ACF converter where the transformer is the only element storing the energy. Here, the frequency decreases with lower input voltages and the transformer is forced to store more energy leading to higher core flux and losses.

4.3.5. Magnetizing Current Displacement

With the proposed control method, where T_t is kept constant and therefore $I_{hb\_pp} = I_{hb\_h} - I_{hb\_l}$, Equation (4-8) demonstrates the shift of the transformer T_1 magnetizing current due to the output current.

Under the conditions of a constant output voltage (constant duty cycle) and zero output current, the equivalent circuit is a half-bridge driving an LC tank formed by the transformer primary inductance ($L_r + L_m$) and C_r (no secondary elements involved). The amount of I_{hb} peak to peak depends only on the applied frequency or T_t. The converter only circulates energy: No energy is transferred to the secondary side.

As the output current increases, the reflected current of the secondary side appears in the primary side, as shown in Figure 4-3 from t_3 to t_5. If the output voltage is constant, the reflected current shifts the magnetizing current up by approximately a factor of $2I_{out}/N$, where N is the transformer turns ratio.

$$I_{hb\_h} = I_{hb\_pp} + \frac{2I_{out}}{N} \tag{4-9}$$

The magnetizing current can be used to estimate the average output current or to control it independently of the input and output voltages, i.e., by measuring the middle point of the increasing current ramp during Q_1 on time, t_0 to t_2 in Figure 4-3.

Figure 4-6 shows actual measurements of the effect of the input voltage and the output current on the magnetizing current. In particular, Figure 4-6a,b show that the peak current of the tank circuit is independent of the input voltage and has the same peak value because the output load is the same, 0.6 A. Figure 4-6c,d show the same effect with a load of 3.25 A. The value of I_{hb} peak current is given by Equation (4-9).

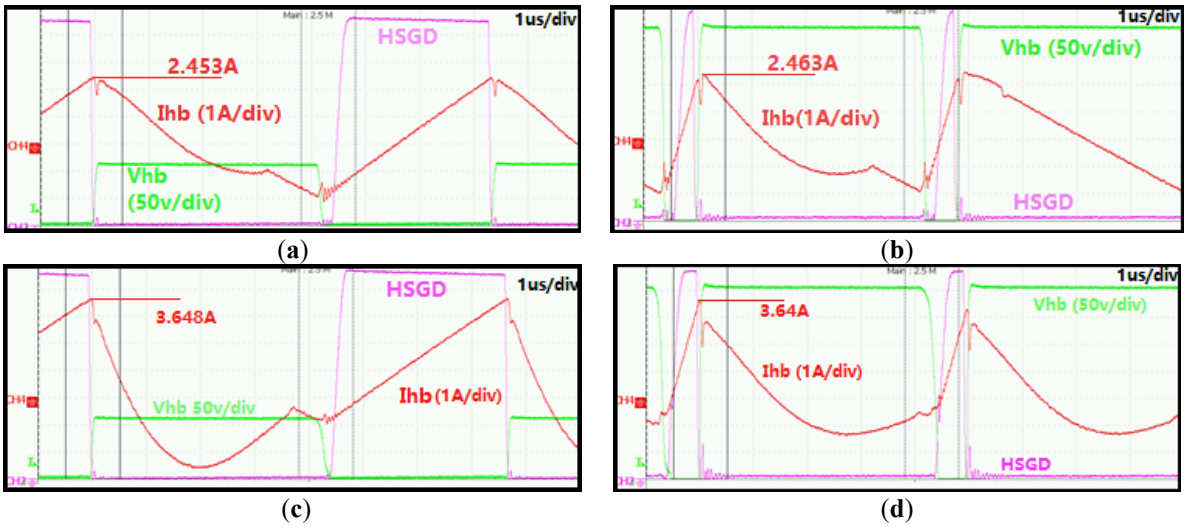


Figure 4-6: Converter waveforms under different input voltages and load conditions, in this case the turns ratio N is 2.4: (a) V_{in}: 110 V, Iload: 0.6 A; (b) V_{in}: 360 V, Iload: 0.6 A; (c) V_{in}: 110 V, Iload: 3.25A; (d) V_{in}: 360 V, I_{load}: 3.25 A.

4.3.6. Overpower Capability

Until this point the description of the behavior of the converter has been based on the assumption of a very small variation of the resonant capacitor voltage. Without the previous approximation $t_c \ll 2\pi\sqrt{(L_m + L_r)C_r}$, the primary current during the charge time is not linear but sinusoidal with a resonance period given by:

$$T_{res} = 2\pi\sqrt{(L_m + L_r)C_r} \tag{4-10}$$

Under heavy load conditions, where longer charge times are required, it can be observed that the percentage of energy accumulated by the capacitor is even larger compared with the approximation previously used of small t_c time. Figure 4-7 shows the magnetizing current and

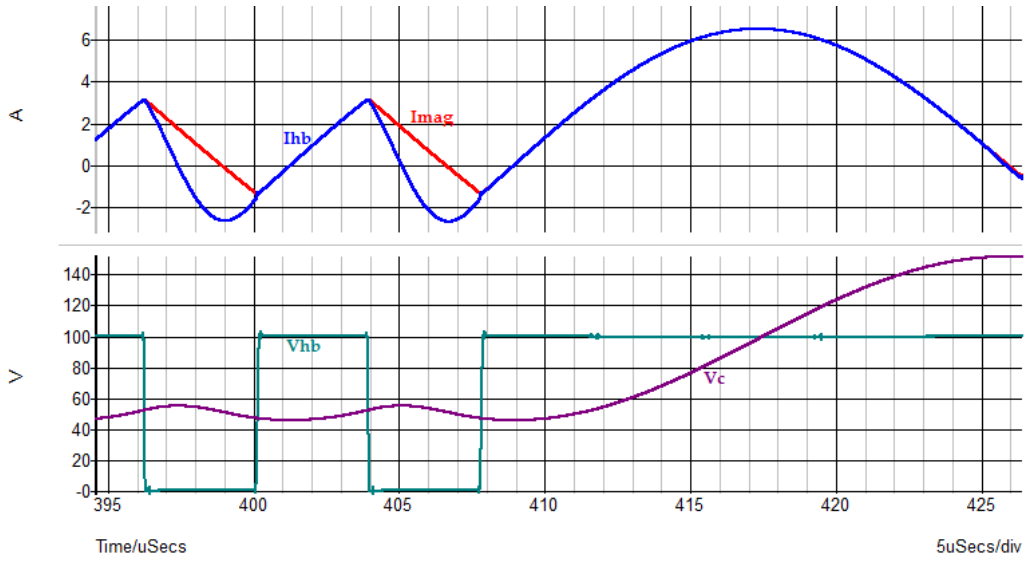


Figure 4-7: Primary waveforms over time with long charge time.

resonant capacitor voltage over time, and Figure 4-8 shows the stored energy of each element over time.

Such behavior can be used to provide a considerable amount of overpower, often required in adaptors without the risk of saturating the transformer as can happen in standard flyback or active clamp flyback (ACF) converters.

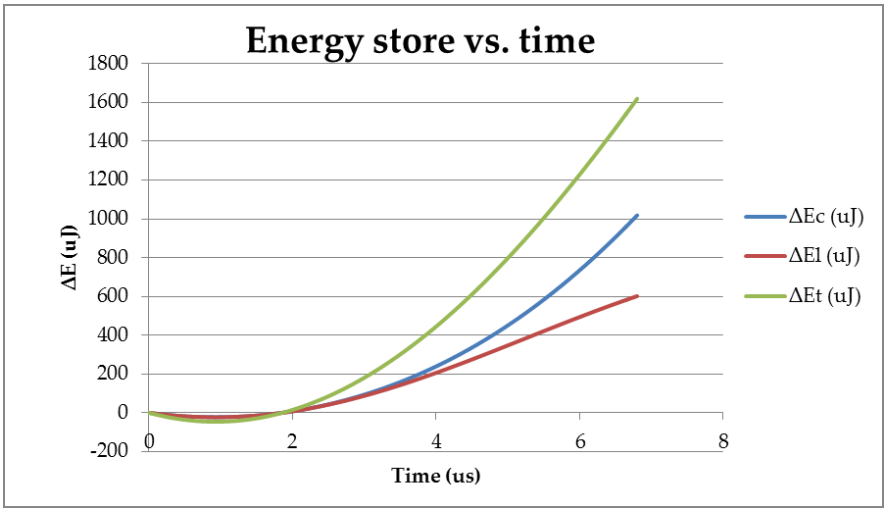


Figure 4-8: Energy stored in the transformer magnetizing inductance and resonant capacitor over time. ΔEc: increment of energy in the resonant capacitor, ΔEl: increment of energy in the primary inductance, ΔEt: total increment of energy in the resonant tank.

4.4. Experimental Results

To demonstrate the high efficiency and power density that this topology can achieve, a 65W

prototype converter was built. The converter specifications are shown in Table 4-1.

Table 4-1: Converter target specifications

Parameter	Value
Max output current	3.25 A
Output voltage	20 V
Input voltage	90–264 Vac
Power density	>20 w/inch^3
Efficiency full load	>93%
EMC	EN55022 class B

The dimensioning of the converter was determined according to [11] and the feedback network was determined considering [13]. A synchronous rectifier was used on the secondary side in order to further boost the efficiency. The MOSFETs used in this experiment are shown in Table 4-2. To maximize the efficiency, the primary side switches were selected with a low $R_{ds(on)}$ and a low output capacitance $C_{o(tr)}$ to allow a ZVS with a minimum circulating current. Since the half-bridge transistor's body diode clamps the V_{hb}, there was no need for a very high voltage rating of these elements as in a standard flyback converter or ACF converter. For the control, a programmable digital controller from Infineon was used.

Table 4-2: MOSFETs characteristics

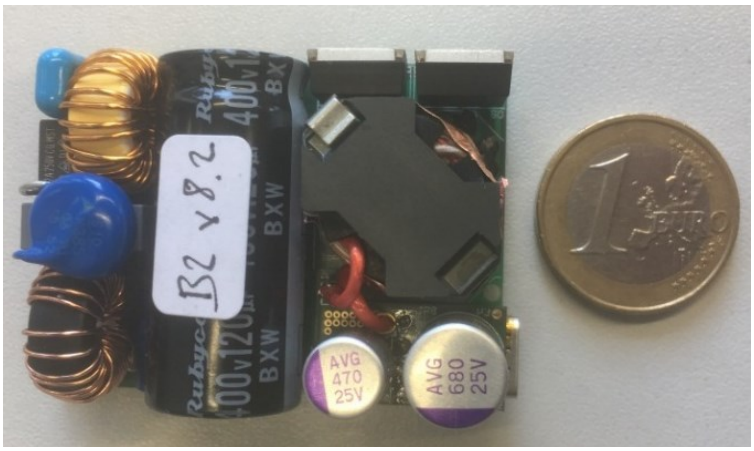
Parameter	HB Mosfets	SR Mosfet
Manufacturer	Infineon	Infineon
Reference	IPP50R140CP	BSC093N15NS5
$R_{ds(on)}$	140 mOhm	9.3 mOhm
$V_{ds\ max}$	500 V	150 V
$C_{o(tr)}$	230 pF	604 pF
Q_{gs}	48 nC	14 nC

The transformer was implemented using an RM8 core. The specifications are shown in Table 4-3:

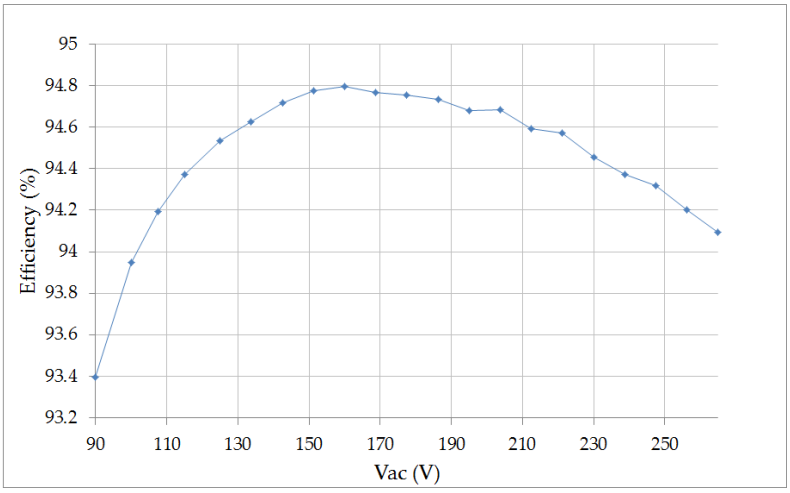
Table 4-3: Transformer specifications

Parameter	HB Mosfets
Core type	RM8
Core material	3C95
Lm	52uH
Llk	1.7uH
Np	18 turns (Litz 40 × 0.1 mm)
Ns	7 turns (TIW Litz 70 × 0.1 mm)
Winding interleaving	P-S-P

The dimensions of the final converter (see Figure 4-9a) were 51.5 × 38 × 19 mm, achieving a power density of 29 W/inch^3. The prototype achieved a minimum efficiency of 93.4 at a 90 Vac input and a 65 W load measured at the board connectors.



(**a**)



(**b**)

Figure 4-9: (a) Asymmetric flyback converter prototype, (b) full load efficiency versus input voltage range.

The frequency of operation ranged from approximately 100 KHz at 90 V_{ac} to 200 KHz at 264 V_{ac}.

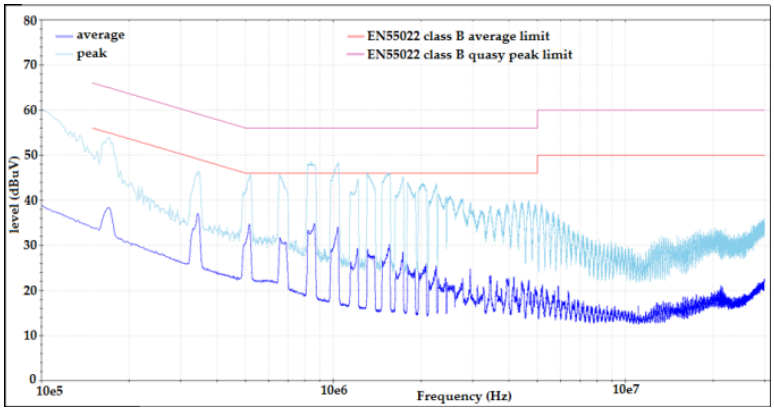
The equipment used for measurements is listed in Table 4-4:

Table 4-4: List of equipment used for measurements

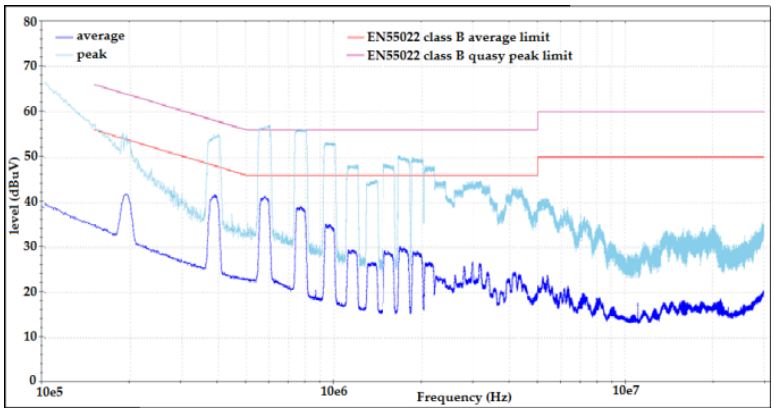
Parameter	HB Mosfets
AC source	Chroma 61505
Programmable load	Chroma 63202
Power analyzer	Yokogawa WT500
Spectrum analyzer	Rohde&Schwarz HMS-X
Oscilloscope	Yokogawa DLM6054

Figure 4-10 shows the EMI results, demonstrating the benefits of this topology and the used

control method.



(a)



(b)

Figure 4-10: EMI results for average, dark blue and peak, light blue values. Upper limit: quasi peak, lower limit: average. (a) Result at 115 V_{ac}, full load and (b) result at 230 V_{ac}, full load.

4.5. Discussion

The outstanding efficiency and EMI performance of the asymmetrical duty cycle flyback converter were proven. The proposed converter and its control method, including ZVS and ZCS over load and line, enable the future study of the benefits of using faster switching devices and higher switching frequencies. This could result in the reduction of the transformer size, and the extension of the input voltage range to further reduce the bulk capacitor or to increase the leakage inductance to achieve EMI requirements at higher switching frequencies.

When used in a DC-to-DC stage and with the proper design, it can achieve efficiency levels close to an LLC converter but with the benefit of the wider voltage range, meaning that in some cases the replacement may be possible and beneficial.

4.6. Conclusions

The proposed asymmetric flyback with the presented control method is a promising topology for highly efficient and very compact adaptors. These features were achieved due to its forward energy transfer capability, compared to standard flyback or ACF [14], where the transformer

has to store all the energy. The proposed control method and topology recycle the energy of the most critical parasitic elements and ensure ZVS and ZCS over load and line. Even with the use of slow devices (with respect to GaN), the efficiency is high and the EMI, due to slow voltage slew rates, easily fulfills commercial requirements.

The performance was demonstrated with a 65W prototype that achieves a minimum efficiency of 93.4% and a peak of 94.8% at full load over the range of Vac input voltage, satisfying the EN55022 class B requirements.

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5. PUBLICATION 3: ADVANCED CONTROL METHODS FOR ASYMMETRICAL HALF-BRIDGE FLYBACK

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ADVANCED CONTROL METHODS FOR ASYMMETRICAL HALF-BRIDGE FLYBACK

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Abstract: In this article, a power converter based on an asymmetrical half-bridge flyback topology is analyzed and optimized for small form factor and fast-charging power adaptors. Two resonant control methods, taking advantage of the forward and flyback characteristics of the converter, as well as the benefits of each of them depending of the operation point are discussed. The analysis is nourished with the equivalent circuits in each phase of operation and the equations that define them. Particularly innovative is the proposed zero voltage resonant valley switching (ZV-RVS) control method for the mentioned converter; in this case it is operated similarly to a flyback converter, allowing safe output voltage ramp up, which is one of the challenges that has limited the usage of this topology up to now. The manuscript also describes how to achieve high efficiency and power density using zero-voltage switching (ZVS) and zero-current switching (ZCS) techniques over the full range of the input voltage and the output load. Finally, the advantages of the proposed control methods are demonstrated in a 65 W adaptor prototype achieving a peak efficiency over 94.6% and an efficiency of 93.8% @ Vac ≥ 100V at full load over the range of the input voltage, as well as a world-class power density of 35 W/inch^3 uncased.

Index Terms: Adaptor, efficiency, flyback, MOSFET, power density

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5.1. Introduction

Portable electronic devices offer every day more processing capabilities, new features and longer battery lifetime. Additionally, bigger screen sizes are becoming popular. All these features require batteries with higher energy capacity. Under such scenario, fast charging technologies are being developed to compensate the longer charging time required; those include new batteries, charging modes, and communication protocols between charger and the portable device to provide variable output voltage, i.e. quick charge, USB-PD [1], etc. These standards allow, as well, the reuse of the power adaptors for different devices and ensure minimal waste of electronics [2], but rise an additional challenge when they are compared to fix voltage adaptors.

One key feature to enable fast charging is that the adaptor must be able to provide a higher

power level, however its size and weight increase with the amount of power that the charger can provide. This increase of size and weight is contradictory with the portability offered by the devices themselves. This contradiction is driving the search for new solutions that are able to keep the adaptor size reasonable but to increase the amount of power that it can provide; this kind of solutions are known as high power density adaptors.

The potential of reducing the adaptor size is limited not only by the size of the individual components, but as well by the maximum losses that are generated at any given operating point. In contrast to other solutions, the heat of adaptors for portable applications is only dissipated by the case surface with passive cooling. The maximum surface temperature is usually determined by the minimum efficiency at full load [3]. Typically this occurs at the minimum input voltage: 100Vac for universal input range 100Vac to 240Vac.

The flyback topology, and its derivatives, is one of the most suitable topologies to overcome the wide input to output voltage range; it is the dominating topology for adaptors below 75W where no power factor correction (PFC) is required [4]-[5]. In a traditional flyback converter [6], the transformer acts as a pure energy storage element resulting in a larger transformer size when it is compared to forward topologies [7]. This limits the maximum achievable power density. In recent years, the emerging wide bandgap devices, such as GaN or SiC [8]-[10], allow higher operation frequencies. This has enabled the active clamp flyback (ACF), in its complementary and non-complementary versions [11]-[14], in combination with these new devices, to reduce the transformer size by increasing the frequency since it is able to recycle the energy of the parasitic elements. Nevertheless, the higher switching frequencies are not exempt from problems. The frequency increase is linked to the usage of wide band gap devices. Faster switching frequencies raise new challenges, i.e. fulfilling conductive or radiated electromagnetic interference (EMI) regulations, such as EN55022 [15].

The asymmetrical half-bridge flyback (AHB) has been proposed in several publications [16]-[19] as a topology able to boost efficiency by recycling the energy of the parasitic elements and, reduce the transformer size due to its hybrid properties as flyback and forward converter. However, the proposed control methods do not address the challenges that arise during power up, due to wide output voltages or lower efficiency at low output currents.

In this paper, a detailed analysis of the AHB flyback and its equations will be performed, two control methods will be analyzed to overcome the challenges that arise from high power density and wide output voltage. Furthermore, the control methods introduced will ensure optimum usage of the topology in all operation points.

5.2. Topology

The general schematic of the asymmetrical half-bridge flyback converter is presented in Figure 5-1, including the elements needed in an adaptor, such as the EMI filter and the input rectifier. The circuit shows a half-bridge in the primary side connected to a capacitor (C_r) in series with the transformer. This is similar to an LLC converter [20], showing the resonant nature of the converter. On the other hand, the secondary side, with a single diode, is similar to a flyback converter.

Of particular interest is the auxiliary winding L_{aux}, that will provide additional information used in the presented control methods. This winding will be used to detect when the magnetizing current reaches zero through the connection to the controller input ZCD (zero crossing detection).

Aiming to provide outstanding power density, the presented control methods for this

topology ensure ZVS and ZCS in the secondary under all conditions, enabling in this way higher switching frequency [21] and therefore a size reduction of the magnetic components. Moreover, this topology recycles the energy of the transformer leakage inductance, which helps to reduce the losses and maximize efficiency. To further boost efficiency, synchronous rectification can be used in the secondary side [22]-[24].

5.3. Continuous resonant mode (CRM) operation

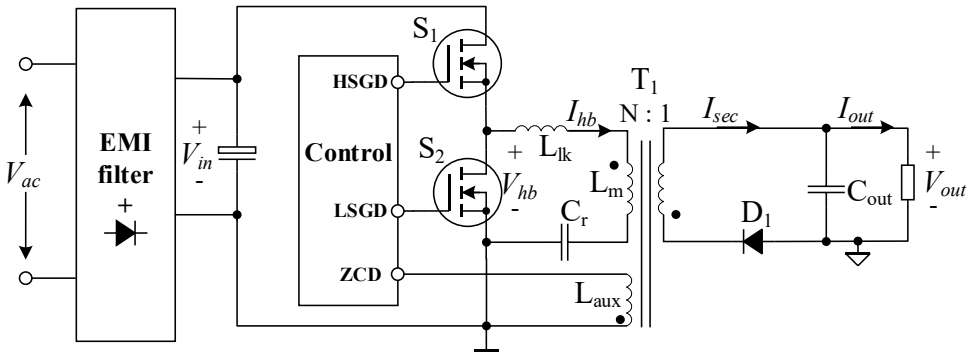


Figure 5-1: Simplified typical adaptor schematic with AHB flyback stage.

Continuous Resonant Mode (CRM) is a control method consisting in turning on the switches in a complementary way with dead times in between to avoid cross conduction. In this mode, there is always a voltage applied to the primary winding of the transformer, except for small dead times.

The ON time of the high side switch S1, Figure 5-1, can be time controlled [25] or peak current controlled [26]. Peak current control is more suitable as it ensures that the output current can be limited and undesired effects such as body diode cross conduction can be avoided [27]-[29].

5.3.1. Equations

An example of CRM mode waveforms in steady state is shown in Figure 5-2.

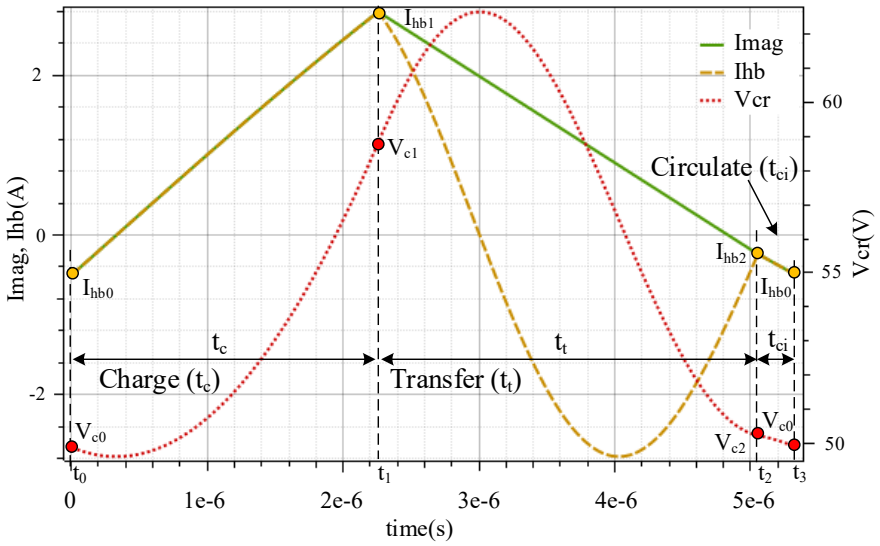


Figure 5-2: Hybrid flyback CRM steady state waveforms (conditions L_m = 51.5µH, L_{lk} = 1.5µH, N = 2.8, C_r = 300nF, V_{in} = 130V, V_{out} = 20V, I_{out} = 3.25A).

In such case, three different phases of operation are identified corresponding to the time intervals, t_0-t_1 (phase 1), t_1-t_2 (phase 2) and t_2-t_3 (phase 3). Depending on the conditions, phases 2 and 3 may change the order or appear more than one time; these situations will be discussed later in section 5.3.2.

For a pure theoretical study, ideal components with no parasitic elements will be considered and dead times in the half-bridge are assumed to be zero.

The 3 phases shown in Figure 5-2 can be named according to the effect that they have in the converter as charge, transfer and circulate phase. In the following paragraphs, the equivalent circuit and equations are presented:

Phase 1, *charge*, from t_0 to t_1: High side switch ON, low side switch OFF.

The equivalent circuit is shown in Figure 5-3. In this phase, the input voltage is connected to the LC tank formed by the primary inductance (L_p, $L_p = L_{lk} + L_m$) and the resonant capacitor (C_r).

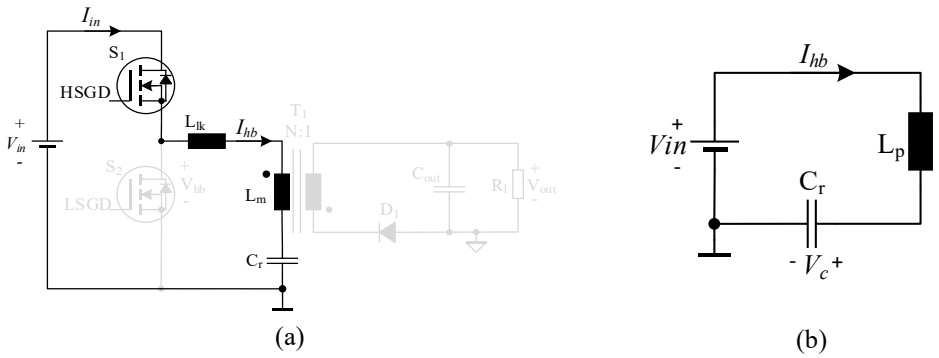


Figure 5-3: Phase 1, charge: (a) Active elements (b) Equivalent circuit.

With the previously described considerations, the equations that define the current in the loop and the voltage of the resonant capacitor are given by (5-1) and (5-2).

$$i_{hb}(t) = I_{hb0}\cos(w_p t) + \frac{V_{in}-V_{c0}}{Z_p}\sin(w_p t) \tag{5-1}$$

$$v_c(t) = (V_{c0}-V_{in})\cos(w_p t) + I_{hb0}Z_p \sin(w_p t) + V_{in} \tag{5-2}$$

Being $w_p = 1/\sqrt{L_p C_r}$ and $Z_p = \sqrt{L_p/C_r}$, I_{hbo} represents I_{hb} at $t = t_0$.

Phase 2, *transfer*, from t_1 to t_2: High side switch OFF, low side switch ON and $I_{mag} \neq I_{hb}$. (Being I_{mag} the current that represents the magnetizing current of the transformer)

During this phase, the equivalent circuit is shown in Figure 5-4. C_{out} is considered large

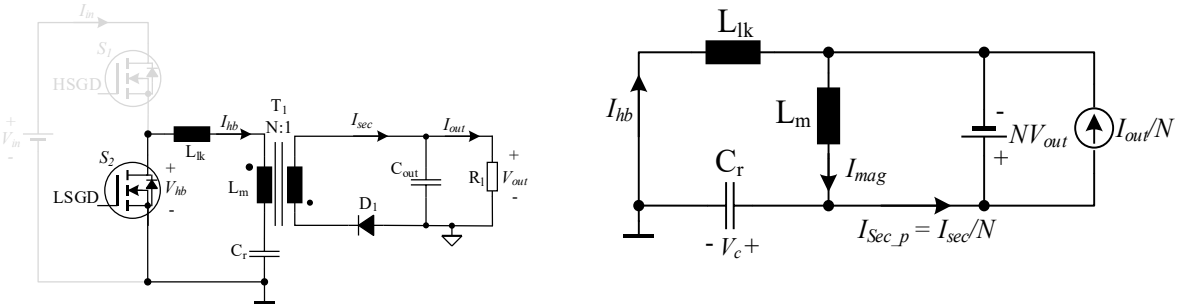


Figure 5-4: Phase 2, transfer: (a) Active elements (b) Equivalent circuit.

enough, this allows us representing it as a constant voltage source of value NV_{out} in the equivalent circuit related to the primary side. During this phase of operation, three reactive elements which energy is changing, L_m, L_{lk} and C_r, are dominating the characteristics of the circuit:

1. The energy of the magnetizing inductance Lm is absorbed by the output capacitor, in this case represented by NVout.
2. The LC tank formed by Llk and Cr is left free to oscillate and their energy flows to the output capacitor too.

The addition of the current from both tanks defines the output current Isec. The reflected secondary side current (to primary side) can be defined as Isec_p = Isec / N.

The equations describing the electrical magnitudes in this phase are given by (5-3) to (5-6):

$$i_{hb}(t) = I_{hb1}\cos(w_1 t) + \frac{NV_{out}-V_{c1}}{Z_1}\sin(w_1 t) \tag{5-3}$$

$$v_c(t) = (V_{c1}-NV_{out})\cos(w_1 t) + I_{hb1}Z_1 \sin(w_1 t) + NV_{out} \tag{5-4}$$

$$i_{lm}(t) = I_{hb1} - \frac{NV_{out}}{L_m}t \tag{5-5}$$

$$i_{sec\_p}(t) = i_{mag}(t) - i_{hb}(t) \tag{5-6}$$

Where $w_1 = 1/\sqrt{L_{lk}C_r}$ and $Z_1 = \sqrt{L_{lk}/C_r}$. I_{hb1} represents I_{hb} at $t = t_1$.

Phase 3, *circulate*, from t_2 to t_3: High side switch OFF, low side switch ON and $I_{mag} = I_{hb}$, see Figure 5-5.

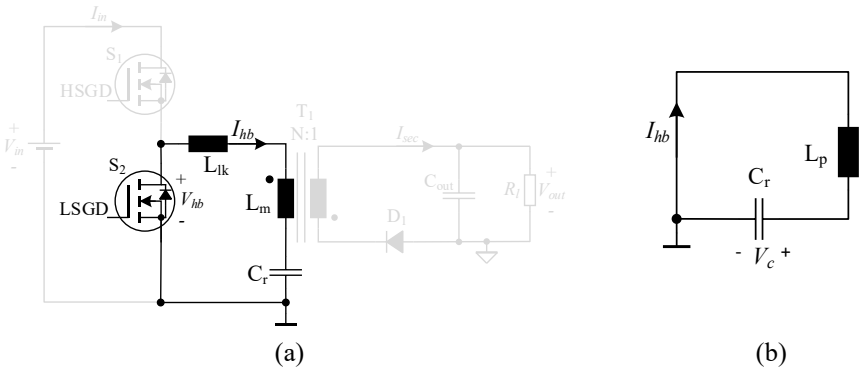


Figure 5-5: Phase 3, circulate: (a) Active elements (b) Equivalent circuit.

This phase starts when I_{hb} current is equal to I_{mag}, meaning that I_{sec} reaches and stays at 0A (ZCS) since the output diode blocks the current. In this phase, the low side switch is kept ON ensuring that I_{hb} gets negative. The negative current in L_p allows having ZVS at the next turn on of the high side switch. If devices with body diode are used, i.e. MOSFET, special care needs to be taken in order to ensure that I_{hb} is negative when the high side switch turns ON in the next cycle. Otherwise an undesired effect called body diode cross conduction will result into a high spike of current through the half-bridge due to the body diode turn off delay of the low side switch [29].

The equations defining this phase are (5-7) and (5-8).

$$i_{hb}(t) = I_{hb2}\cos(w_p t) + \frac{V_{c2}}{Z_p}\sin(w_p t) \tag{5-7}$$

$$v_c(t) = V_{c2}\cos(w_p t) + I_{hb2}Z_p \sin(w_p t) \tag{5-8}$$

Considering a steady state the following system of equations can be derived:

$$I_{hb1} = I_{hb0}\cos(w_p t_c) + \frac{V_{in}-V_{c0}}{Z_p}\sin(w_p t_c) \tag{5-9}$$

$$V_{c1} = (V_{c0}-V_{in})\cos(w_p t_c) + I_{hb0}Z_p \sin(w_p t_c) + V_{in} \tag{5-10}$$

$$I_{hb2} = I_{hb1}\cos(w_1 t_t) + \frac{NV_{out}-V_{c1}}{Z_1}\sin(w_1 t_t) \tag{5-11}$$

$$V_{c2} = (V_{c1}-NV_{out})\cos(w_1 t_t) + I_{hb1}Z_1 \sin(w_1 t_t) + NV_{out} \tag{5-12}$$

$$I_{hb2} = I_{hb1} - \frac{NV_{out}}{L_m}t_t \tag{5-13}$$

Where

$$I_{hb0} = I_{hb2}\cos(w_p t_f) + \frac{V_{c2}}{Z_p}\sin(w_p t_f) \quad (5\text{-}14)$$

$$V_{c0} = V_{c2}\cos(w_p t_f) + I_{hb2} Z_p \sin(w_p t_f) \quad (5\text{-}15)$$

And I_{hb2} represents I_{hb} at $t = t_2$.

5.3.2. Low output current operation

As the output current decreases, the order and number of the previously shown phases change. Figure 5-6 shows the waveforms of the previous circuit example under 1A of load and 20V output.

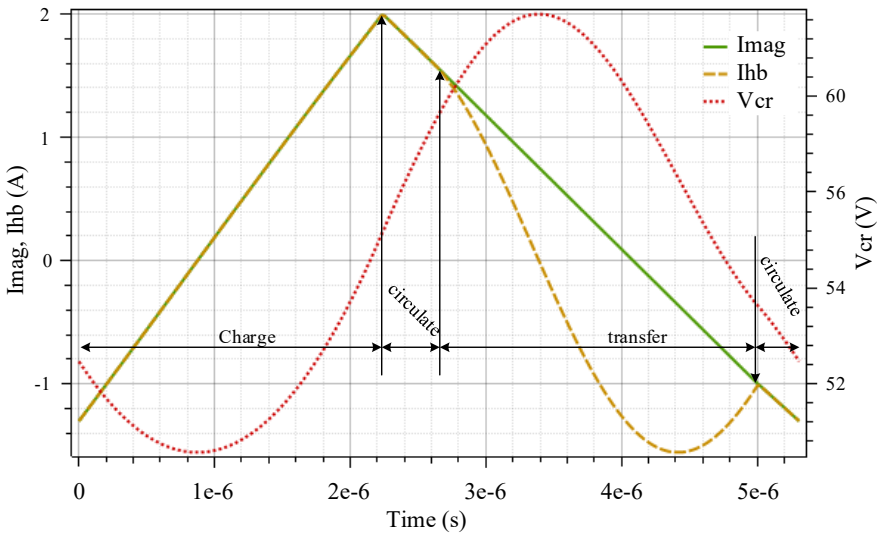


Figure 5-6: CRM steady state waveforms under 1A output current and 20V (L_p = 53µH, L_{lk} = 1.5µH, N = 2.8, C_r = 300nF, V_{in} = 130V and V_{out} = 20V).

A lower output current leads to a higher negative I_{hb} current, therefore the voltage in the resonant capacitor at the end of the charge phase has a value lower than the reflected output voltage NV_{out}, this leads, during the low side switch turn on, to a circulating phase followed by transfer and circulating phase again. In the case of no load condition, the magnetizing average current would be zero and the half-bridge would just drive an LC circuit circulating energy. Consequently, at low output current, the resulting efficiency of the converter using this control method is expected to be low due to the amount of circulating energy compared to the energy transferred to the secondary side.

5.3.3. Low output voltage operation

In CRM mode, lower output voltages can be provided by decreasing the duty cycle defined as $T_{hs}/(T_{hs} + T_{ls})$, where T_{hs} and T_{ls} are the ON times of the high side and low side switches respectively. Under these conditions, the resonance seen during the energy transfer phase may not match the ON time of the low side switch T_{ls}. In this case, where T_{ls} is longer comparable to previous examples, several resonant cycles of the LC tank formed by L_{lk} and C_r may occur; this is illustrated in Figure 5-7.

Another important aspect to consider is the synchronous rectification in the secondary side

[22]-[24], present in almost every modern high-density adaptor to increase the efficiency. In CRM mode, the shape of the secondary current (I_{sec_p}), during T_{ls}, may vary depending on the damping factor due to the equivalent series electrical resistance of the circuit as shown in Figure 5-7. The equivalent series resistance R_{esr} includes the effect of the switches ON resistance (R_{on}), PCB tracks, transformer cables, etc. Figure 5-7 shows two examples for different R_{on} values,

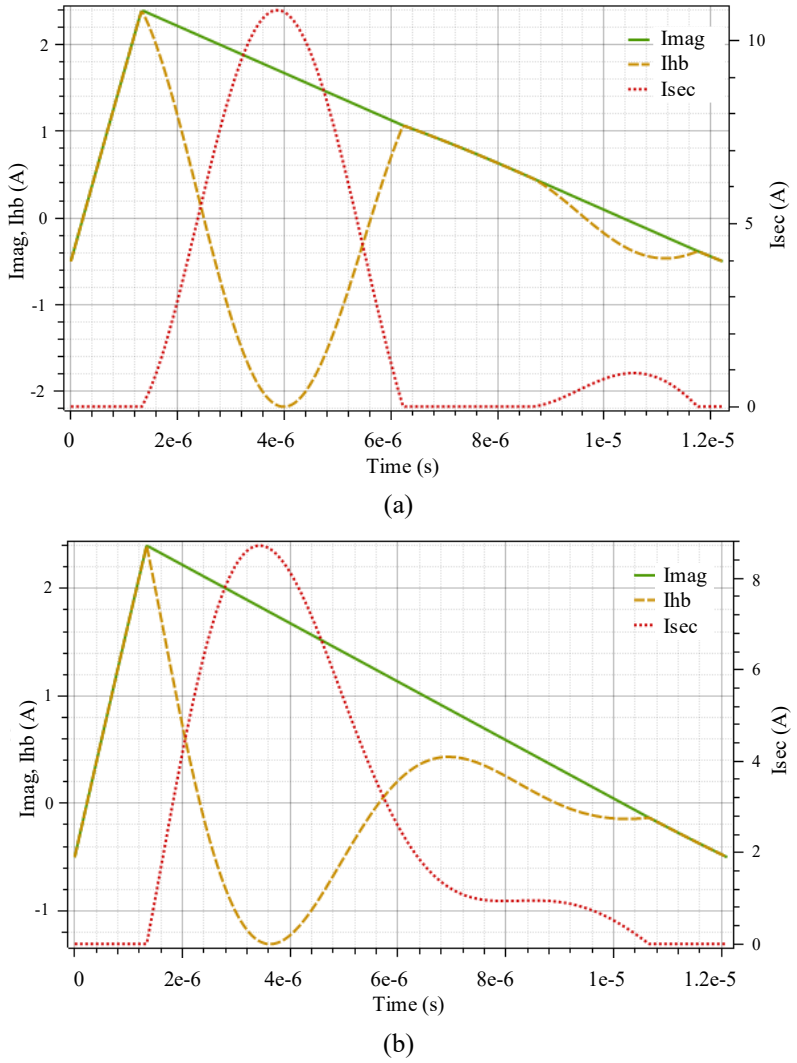


Figure 5-7: Damping effect on the waveforms shape for low output voltage (Vout = 5V). a) I_{sec_p} with 2 pulses, series resistance R_{esr}: 0.2 Ω, b) I_{sec_p} with single pulse, series resistance R_{esr}: 1 Ω

in Figure 5-7a R_{on} = 0.2 Ω and Figure 5-7b R_{on} = 1 Ω.

In Figure 5-7a the output current reaches zero amperes and rises again; typically, SR controllers activate the associated switch only during the first pulse and not during the second, affecting this way the efficiency. If synchronous rectification is used in combination with CRM control method for low output voltage, the operation in Figure 5-7b is preferred, due to single current pulse in the secondary but it will have a negative impact on the efficiency.

5.3.4. Low input voltage operation

During low input voltage operation, the required T_{hs} to reach certain amount of peak current is longer. The current I_{hb}, which has a sinusoidal shape (5-1), may reach its maximum and start decreasing during the charge phase, meaning that peak current control cannot be used since I_{hb}

may not reach the desired peak value; ON time control may be used in this case or combined with peak current control. Under these conditions, I_{hb}, during the charge phase, cannot be approximated by a linear function, therefore, the approximations presented in [27] are no longer valid. This operation condition is shown in Figure 5-8. As the current I_{hb} decreases, the energy stored in the magnetizing inductance of the transformer decreases, besides this, the energy stored in the capacitor increases further. This differs from the energy portion shared between the resonant capacitor and the magnetizing inductance presented in [27] under linear

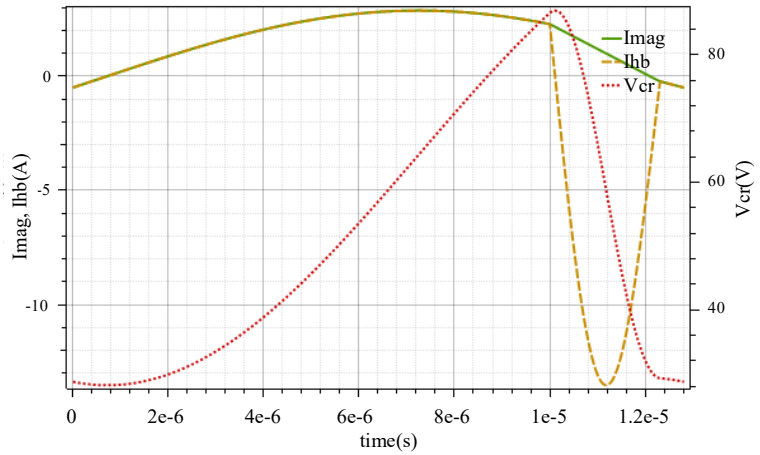


Figure 5-8: Sinusoidal shaped current Ihb during charge time at low input voltage (V_{in} = 63V).

approximation of the current I_{hb}. In this situation, much more energy is stored in the resonant capacitor compared to the energy stored in the magnetizing inductance.

To understand further the behavior of the converter, the system of equations presented by (5-9) to (5-15) needs to be solved. Since the transfer time variable (T_t) appears in (5-13) and, as well, within the argument of a trigonometrical functions in (5-11) and (5-12), the system is transcendental and cannot be solved symbolically. To disclose the limits of the converter at low input voltage, where the linear approximations of I_{hb} are no longer valid, the same numerical iterative method mentioned in section 5.3.1 will be used.

The numerical solution will consider practical conditions required for a proper operation:

1. At the end of the cycle (t_3 in Figure 5-2) $I_{hb} = I_{mag}$ to have secondary ZCS
2. At the end of the cycle I_{mag} needs to be negative to achieve ZVS
3. V_{out} is constant and the amplitude I_{mag} (peak to peak value) is kept constant

The solution is presented in Figure 5-9, it shows the relation between the output current (y axis) and input voltage (x axis) for different values of I_{hb_p} (parameter). It can be observed that a given I_{hb_p} current allows higher output current at lower V_{in}. The left part of the plot (lower values of the input voltage), where the lines start to curve up, shows the limit of the linear approximation of the sinusoidal shaped current I_{hb} described in [27]. Nevertheless, from a practical point of view, the approximation is accurate down to relatively low input voltages.

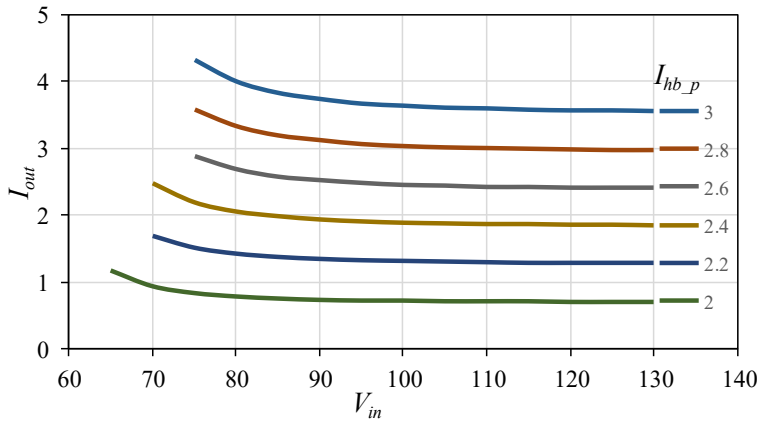


Figure 5-9: I_{out} as a function of V_{in} for different I_{hb} peak currents showing the limits of linear approximation for I_{hb}

For dimensioning of a practical converter, it is desired to know the value of the minimum operating input voltage. Such voltage can be chosen as the minimum one to ensure peak current control of I_{hb}, meaning that I_{hb} does not have negative slope. That is the peak of the sine wave during the charge phase. This is shown in Figure 5-10.

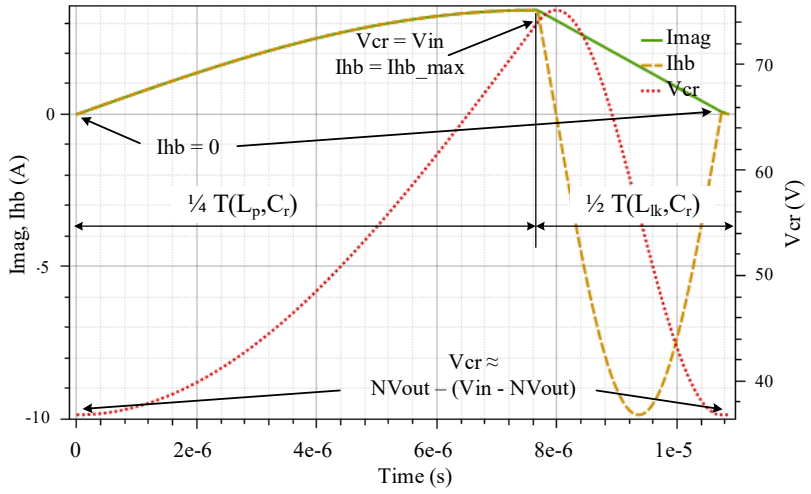


Figure 5-10: Converter waveforms showing the limit of peak current (I_{hb_p}) control.

Considering the results shown in Figure 5-9, a conservative approximation of the required I_{hb} peak current can be calculated using equation (5-20) as proposed in [27].

With a few practical approximations, we can calculate the minimum input voltage required to reach the desired I_{hb} peak:

1. Assuming zero magnetizing negative current, we can reduce (5-1) to (5-16) and the peak of I_{hb} to (5-17).

$$i_{hb}(t)=\frac{V_{in}-V_{c0}}{Z_p}\sin(w_p t) \tag{5-16}$$

$$I_{hb\_max}=\frac{V_{in}-V_{c0}}{Z_p} \tag{5-17}$$

2. If the transfer phase (see section 5.3.1) duration is approximately equal to ½ resonant period of the tank formed by L_{lk} and C_r (T_r), the initial voltage in the resonant capacitor can by calculated by (5-18).

$$V_{c0} = NV_{out}-(V_{in}-NV_{out}) \tag{5-18}$$

$$V_{in\_min}= NV_{out}+\left(\frac{I_{out}}{N}\right)\sqrt{L_p/C_r} \tag{5-19}$$

Replacing the required peak current I_{hb_max} from (5-20) and V_{c0} from (5-18) in (5-17), we obtain the approximate minimum input voltage required for peak current control (5-19).

5.3.5. Limitations of the CRM control method.

CRM (continuous resonant mode) control method provides the best efficiency at high output current; however, at low output current, the excessive circulating current impacts negatively on the efficiency, this is due to the fact that T_t is fix to achieve resonant operation introducing in this way high negative currents. Furthermore, at low output voltage, double pulse in the secondary current, as seen in Figure 5-7a, may be observed, leading to loss of ZCS in the secondary and undesired ringing. Additionally, if a synchronous rectifier (SR) is used, a loss of efficiency may occur since the SR controller may only be triggered during the first pulse of the secondary current.

However, the most challenging drawback from a practical point of view is that the current I_{hb} may not reach a negative value at the end of the cycle (t_3 in Figure 5-2), especially during ramp up of the output voltage from zero. If MOSFETs are used as switches, there is risk of body diode cross conduction [27]-[29].

To overcome those limitations, an alternative control method will be proposed, this control method will be presented in the next section.

5.4. Zero voltage resonant valley switching (ZV-RVS) mode

Zero Voltage Resonant Valley Switching mode [30] is a control method that operates the converter using waiting times (both switches OFF) until the transformer is demagnetized. It is synchronized to the valleys as a traditional quasi-resonant flyback [6], which allows the converter to reduce the frequency and it ensures zero voltage switching in all switches. This mode solves the weakness of the previously analyzed CRM control method, especially during start up with low output voltage since it ensures no body diode cross conduction and keeps the magnetizing current under control, i.e. transformer demagnetization.

Figure 5-11 shows the result of a simulation of the proposed control method ZV-RVS. The PWM pattern is shown in the upper part of the figure, where HS and LS signals indicate which switch is active over time. The PWM consists of three pulses synchronized with the zero crossing detection (ZCD) signal, see Figure 5-1, which indicates the demagnetization of the transformer and subsequent zero crossing of the magnetizing current. This signal is commonly used in quasi-resonant flyback converters [6].

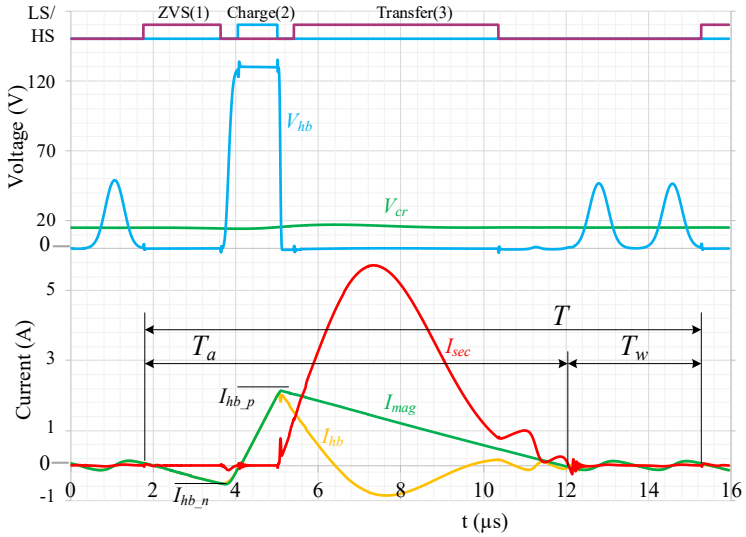


Figure 5-11: Simulated ZV-RVS waveforms with 2nd valley operation. T_a is the period with forced magnetizing current and T_w is the period of free oscillation.

The function of the three pulses and the waiting time is the following:

1. *ZVS* pulse (1): it is applied on the low side (LS) switch when V_{hb} reaches zero (detected through the ZCD signal). This pulse is used to induce a small amount of I_{hb} negative current in the transformer. After the LS turns off the induced current forces V_{hb} to increase, allowing ZVS for the next pulse.
2. *Charge* pulse (2): this pulse is applied on the high side (HS) switch. During this pulse the current I_{hb} gets positive and the energy taken from the input is stored in the primary inductance and the resonant capacitor.
3. *Transfer* pulse (3): This last pulse, in the low side switch, will transfer the stored energy to the secondary side, the energy of the resonant capacitor is transferred in forward mode through the transformer. To achieve resonance, the proposed length of this pulse is T_r. Once this pulse is finished the remaining magnetizing current, if any, will be transferred to the output or the resonant capacitor.
4. Waiting time (T_w): during this time the remaining energy in the magnetizing inductance flows to the output capacitor (and/or the resonant capacitor); the transformer magnetizing inductance is discharged and the system oscillates freely.

Special attention needs to be paid to the transfer pulse. In the proposed ZV-RVS mode, the transfer pulse should be shorter than the demagnetization time of the transformer to allow free oscillations once the magnetizing current reaches zero, avoiding therefore driving unnecessary negative magnetizing current. These oscillations are similar to those occurring in standard flyback converters [6]. The next *ZVS* pulse can be synchronized to any valley controlling this way the switching frequency [31].

The control of the output current can be easily carried out using peak current (I_{hb_p}) control during the charge phase, and ON time modulation for the other two phases: transfer and ZVS.

It is worth mentioning that this control method outperforms other alternatives since it ensures no body diode cross conduction, allows frequency control, zero voltage switching in all cases, uses forward mode energy transfer, and it maximizes the efficiency, due to the absence of extra circulating energy, compared to CRM mode.

5.4.1. ZV-RVS mode, output current and control.

The output current in CRM mode under linear approximation of I_{hb} is similar to the one of a buck converter operating in CCM mode:

$$I_{out} = \frac{N(I_{hb\_p}+I_{hb\_n})}{2} \tag{5-20}$$

This is analyzed in detail in [27]. Having a look to the waveforms shown in Figure 5-11 for ZV-RVS mode it can be observed that, without considering the pause interval T_w, the magnetizing current, I_{hb}, has the same triangular shape as it has for CRM mode. Therefore, we can approximate the output current taking into account the duty cycle (T_a/T) shown in (5-21).

$$I_{out} = \frac{N(I_{hb\_p}+I_{hb\_n})}{2}\frac{T_a}{T} \tag{5-21}$$

T_a represents the time where the magnetizing current is present (not freely oscillating), see Figure 5-11.

Similar to a standard flyback, with this method we have two degrees of freedom to control the output current, namely I_{mag} peak current (I_{hb_p}) and valley number selection (or waiting time T_w). The valley number will introduce a waiting time where no power is transferred. This method allows reducing circulating current present in CRM control method, achieving in this way a higher efficiency at low output current.

5.4.2. Optimum mode and operation point.

Two major factors need to be considered to achieve optimum efficiency; on the one hand, conductive losses due to resistive elements and magnetic losses due to flux in the transformer, on the other hand, for its known benefits, resonant operation may be desired [27]. The presented control methods offer several degrees of freedom to provide the desired output affecting those two factors. In the next section the operation modes will be analyzed in regard to the switching frequency (F_{sw}) and magnetizing peak current to better understand which conditions provide the best efficiency.

Equations in [27] will be used to extract the relation between the peak current and the switching frequency for the two control methods.

In ZV-RVS mode, T_a can be calculated as (5-22). By replacing T_a in (5-23), the relation between I_{hb_p} and T_w or T ($T=T_a+T_w$) is obtained.

$$T_a = (I_{hb\_p} - I_{hb\_n}) L_p \left(\frac{1}{V_{in} - NV_{out}} + \frac{1}{NV_{out}} \right) \quad (5\text{-}22)$$

$$I_{out} = \frac{N(I_{hb\_p} + I_{hb\_n})}{2} \frac{T_a}{T_a + T_w} \quad (5\text{-}23)$$

In CRM mode the relation between the switching frequency and the peak current can be expressed as (5-24).

$$F_{sw} = \frac{NV_{out}(V_{in} - NV_{out})}{\left(2I_{hb\_p} - {}^{2I_{out}}/_{N}\right) L_p V_{in}} \quad (5\text{-}24)$$

An example of the operation modes and their conditions, for a given V_{in} and V_{out}, is represented in Figure 5-12. The solid lines represent pairs of combinations I_{hb_p}/F_{sw} which satisfy equation (5-23) for ZV-RVS, and the dashed lines, pairs that fulfill (5-24) for CRM, both cases for a given output current. The circles on the solid lines represent the discrete values (NT_{osc}) of T_w for valley switching (T_{osc} is the period of the valleys in ZV-RVS).

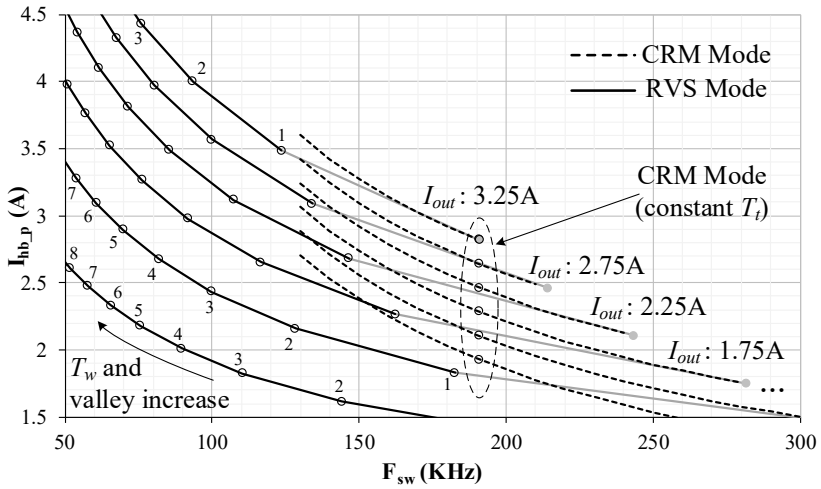


Figure 5-12: Example of operation mode and conditions for different I_{out} under fix V_{in} and V_{out}. Conditions V_{in}=140V, V_{out}: 20V, N=2.8, I_{hb_n}=-0.5A, L_p=53uH and T_{osc}=1.8us.

If resonant operation is desired, additional restrictions appear when choosing the operation conditions:

In ZV-RVS mode, resonant operation can be achieved without driving excess of negative current by selecting the switching frequency which fulfils (5-25).

$$I_{hb\_p} \geq \frac{NV_{out}}{L_p} T_t \quad (5\text{-}25)$$

In CRM mode there is a single frequency which achieves resonant operation with minimum peak current given by (5-26).

$$F_{sw}=\frac{V_{in}-NV_{out}}{T_t V_{in}} \quad (5\text{-}26)$$

At low output voltage only ZV-RVS mode is preferred to avoid several resonance cycles that appear in the case that CRM mode is used. This has been explained in section 5.3.3.

The conductive losses increase with the peak current I_{hb_p}, and the magnetic losses are related to each pair (I_{hb_p}, F_{sw}). The optimum operation point depends on the final components and system dimensioning. Configurable digital controllers are very suitable for this purpose.

5.5. Practical prototype

To demonstrate the high efficiency and power density that this topology can achieve, a 65W prototype converter was built. The converter specifications are shown in Table 5-1

Table 5-1: Converter specifications

PARAMETER	VALUE
Output voltage	USB-PD 5V-20V
Nominal output current	3.25A
Input voltage	90Vac – 264Vac
Power density uncased	35 w/inch3
Efficiency full load	>93.8% @ Vac ≥ 100Vac
EMC	EN55022 class B

The dimensioning of the converter [32] has targeted maximizing the efficiency at low input voltage and maximum load, this helps minimizing the maximum power loss at any given operation point. A synchronous rectifier was used in the secondary side in order to further boost the efficiency. The regulator is placed in the secondary side and feedbacks to the primary controller through an opto-coupler [33], providing the electrical isolation required in such kind of applications. The MOSFETs used in the experimental prototype and their characteristics are shown in Table 5-2

Table 5-2: Mosfet used in the converter

Parameter	LS Mosfet	HS Mosfet	SR Mosfet
Company	Infineon	Infineon	Infineon
Reference	IPI50R140CP	IPD60R180C7	BSC093N15S5
Rds(on)	140 mΩ	180 mΩ	9.3 mΩ
Vds_max	500 V	600 V	150V
Co(tr)	230 pF	349 pF	604 pF
Qgs	48 nC	24 nC	14 nC

To reduce the circulating current Ihb required to achieve ZVS and maximize efficiency, the primary side switches were selected with a low output capacitance Coss and low Rds(on). Since the half-bridge transistor's body diodes clamp the voltage in the bridge middle point Vhb, the maximum Vds voltage rating required by the primary MOSFETS is limited to the AC wave peak voltage. This is a major advantage compared to a standard flyback converter or active

clamp flyback (ACF) converter where additional reflected voltage and spikes need to be consider. This lower voltage seen across the transformer primary and secondary is another advantage for EMI and primary to secondary safety distances compared to ACF.

The transformer was implemented using an RM8 core for size reduction. The specifications are shown in Table 5-3

Table 5-3: Transformer specifications

Parameter	LS Mosfet
Core type	RM8
Core material	PC95
Lm	52µH
Llk	1.7µH
Np	17 turns (Litz 40x0.1 mm)
Ns	6 turns (TIW Litz 120x0.08 mm)
Winding structure	P-S-P

Both discussed control methods, CRM and ZV-RVS, were implemented in a programmable digital controller from Infineon Technologies AG.

Figure 5-13 shows the converter efficiency for the two control modes versus output current, for 100Vac and 240Vac.

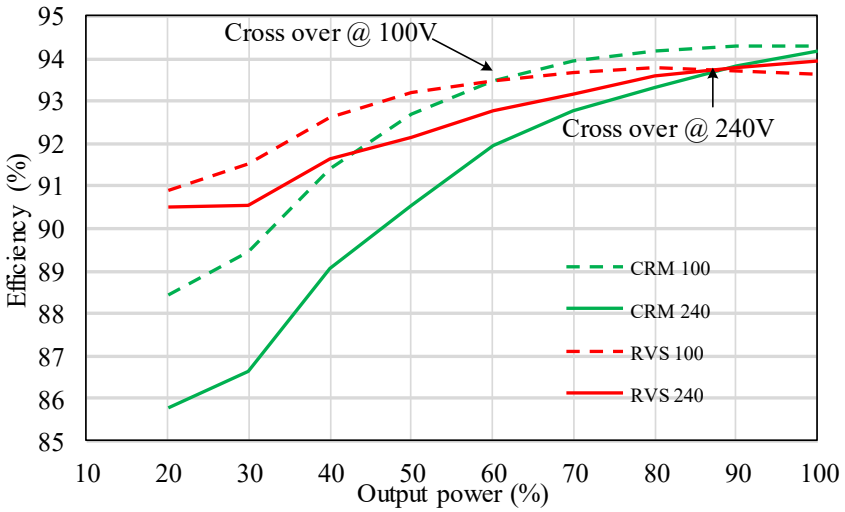


Figure 5-13: Converter efficiency vs. load at $100V_{ac}$ and $240V_{ac}$ input voltage using CRM and RVS mode. Output voltage 20V.

It can be observed, as explained, that RVS is preferred for low output current and CRM mode for higher output currents

Using both modes, the total efficiency can be optimized.

An actual waveform of the RVS mode is shown in Figure 5-14.

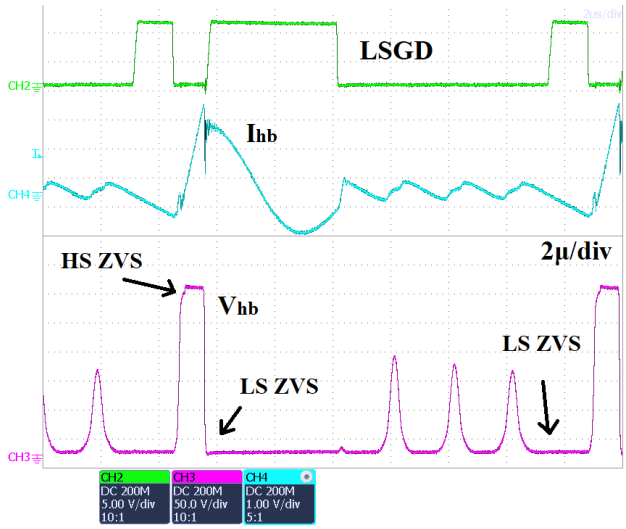
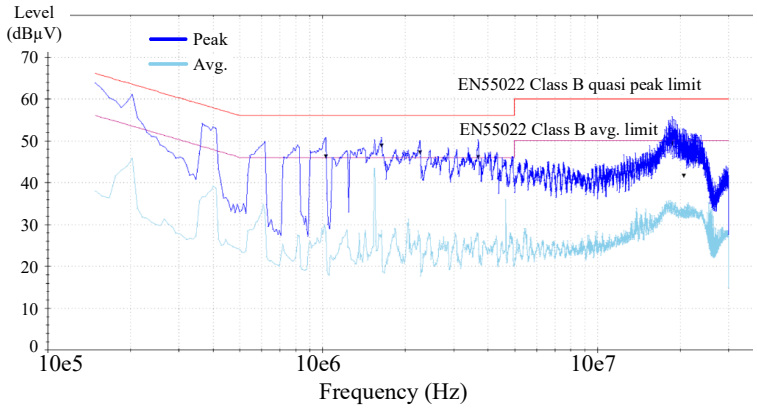
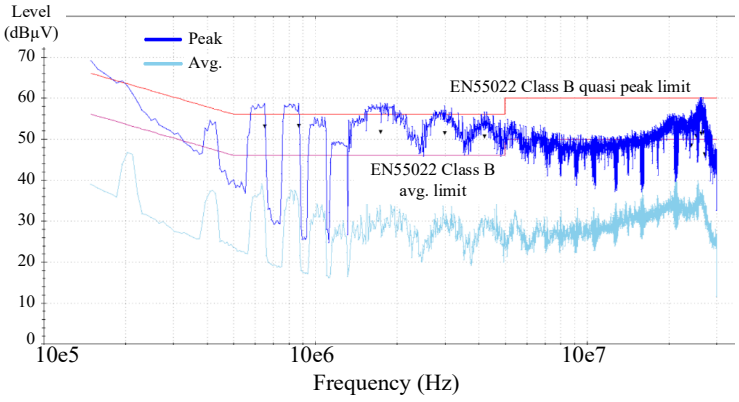


Figure 5-14: Actual waveforms of the converter prototype during ZV-RVS operation measured with scope Yokogawa DLM6054. Operations conditions: V_{ac} = 230V, V_{out} = 12V.

The EMI results at 115Vac and 230Vac are shown in Figure 5-15. They fulfill the required normative EN55022 [15] for average and quasi peak limits.



(a)



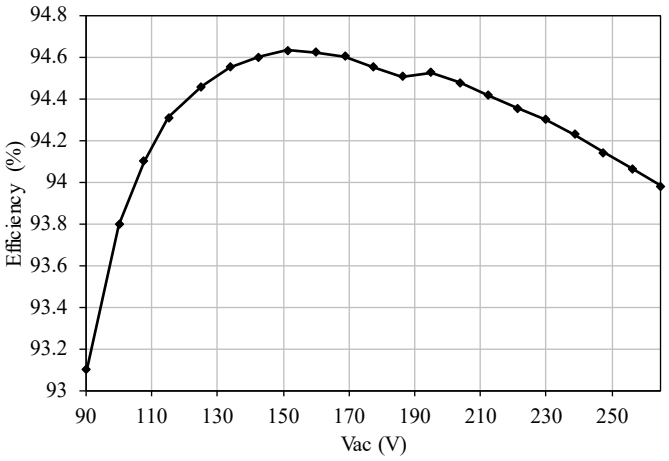
(b)

Figure 5-15: Conductive EMI results, average and peak values. a) V_{ac} = 115 V, full load and b) V_{ac} = 230 V, full load.

It can be seen how the proposed method achieve ZVS, or in worst case partial ZVS, for both switches as explained in section 5.4. After the transfer pulse, V_{hb} oscillates similarly to a standard flyback converter. This operation mode solves the issue of the high circulating current that leads to low efficiency at low output current seen in Figure 5-13.

The size of the final converter, see Figure 5-16a, is 43.3 × 37 × 19 mm, achieving an uncased power density of 2.13W/cm^3 (35 W/inch^3). The prototype achieved a minimum efficiency of 93.1% at a 90Vac/50Hz input and a 65 W load measured at the board connectors, see Figure 5-16b.

(a)



(b)

Figure 5-16: (a) Asymmetric HB flyback prototype, (b) full load efficiency versus input voltage range, including bridge rectifier and EMI filter.

The frequency of operation ranged from approximately 140 KHz at 90 V_{ac} to 240 KHz at 264 V_{ac}.

5.6. Conclusions

In the previous sections, two different control methods have been presented and analyzed for AHB flyback converter. It is important to sum up the nature of both control methods:

1. CRM is a typical operation mode of forward converters, i.e. a buck converter. The duty cycle defines the output voltage. In CRM mode, the converter can operate in absence of

load without losing the control of the output voltage, meaning that energy is just circulated but not transferred.

2. In ZV-RVS mode, the converter is operated similar to a flyback converter. The PWM used in this control method guarantees always zero voltage switching (ZVS) and minimizes the circulating energy. It can also perform valley switching, reducing this way the switching frequency to improve the efficiency.

The dual control mode proposed in this work, makes the best use of the converter due to its hybrid nature forward/flyback in terms of wide input/output voltage range, low output current operation and maximum efficiency. Additionally, it ensures that the output current and/or voltage are easy to control. The two reviewed control methods are suited as an improvement of the well-known CCM and DCM modes. The selected topology in combination with the two described control methods enables high power density (35W/inch^3) and high full load efficiency, above 93.1% over input voltage, using Silicon MOSFETs as switches. Under DC input voltage excluding the rectifier and EMI filter losses, an efficiency of 96.3% peak has been achieved. Additionally, the newly proposed ZV-RVS mode solves the weakness of the CRM mode for low output current, low output voltage and converter start up. It ensures the demagnetization of the transformer and avoids body diode cross conduction issues and therefore enables a safe start-up. The results have been demonstrated with a fully functional 65W prototype.

5.7. Acknowledgment

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6. PUBLICATION 4: STUDY OF WBG SWITCHES BENEFITS ON ASYMMETRICAL HALF-BRIDGE FLYBACK CONVERTER

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STUDY OF WBG SWITCHES BENEFITS ON ASYMMETRICAL HALF-BRIDGE FLYBACK CONVERTER

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Abstract: Recent market trends are shaping the direction of power adaptors development. On the one hand, USB-PD standard [1] that allows the reuse of power adaptors for multiple devices, thus reducing the electronic waste generated [2]; on the other hand, fast battery charging features for mobile devices bring the need for higher adaptor power levels, resulting in bigger adaptor size. To reduce the size of the adaptor, a recent market trend drives the development of high-power density adaptors.

In this paper, an USB-PD adaptor based on the asymmetrical Half-Bridge (AHB) flyback converter [3]-[7] using wide band gap (WBG) devices will be presented. The behavior and advantages of WBG devices will be analyzed and compared to traditional Silicon switches.

The theoretical analysis will be completed with experimental results of a 65W adaptor prototype using GaN devices, achieving with a peak efficiency over 95.5% and a minimum efficiency of 93.4% at full load over the input voltage range while reaching and a power density of 1.92 w/cm3 (31.5 w/inch3) uncased.

6.1. Introduction

Flyback converters are the state of the art for wide input (90Vac to 264Vac) to output (5V to 20V) voltage range converters used in USB-PD compatible adaptors. The potential of reducing the adaptor size is limited, not only by the components size, but also by the maximum losses that are generated by the converter at any given operating point. In a power adaptor where the heat is only dissipated passively, the maximum allowed surface temperature will determine the minimum allowed efficiency at full load, which is typically the worst-case operating point [8].

To overcome these issues, different variants of flyback converters [9] are becoming popular.

In this work, a converter based on an asymmetrical Half-bridge flyback topology using WBG devices will be presented.

The AHB flyback has been analyzed in several previous works. The benefits in terms of zero voltage switching (ZVS) and zero current switching (ZCS), as well as its merit to achieve a small size has been widely described [3]-[7]. Compared to the traditional flyback converter, it is able to recover the energy of the transformer leakage inductance. Other works have analyzed the benefits synchronous rectification in the secondary side [10]-[11].

In the following sections, the advantages of WBG devices in the switching behavior and its impact on the final converter efficiency will be analyzed. The behavior of SiC and GaN devices will be shown and compared to traditional silicon switches.

6.2. Asymmetrical HB flyback topology

The AHB flyback converter circuit is shown in Figure 6-1. The converter control method and its different operation phases had been the focus of previous works [4]-[7]. The output voltage can be controlled by modulating the duty cycle of V_{hb}. Equation (6-1) shows the relation of input to output voltage.

$$V_{out} = D \frac{V_{in}}{\mathrm{N}} \frac{\mathrm{L_m}}{\mathrm{L_m} + \mathrm{L_{lk}}} \tag{6-1}$$

Where D is the on-time of the high side (T_{hs}) divided by the period (T) and N the transformer

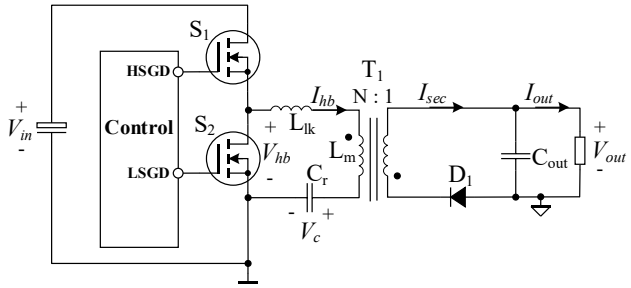


Figure 6-1: Schematic of the asymmetrical half-bridge flyback converter.

turns ratio primary to secondary.

With the right dimensioning ZVS and ZCS, can achieved. That helps to reduce the losses in

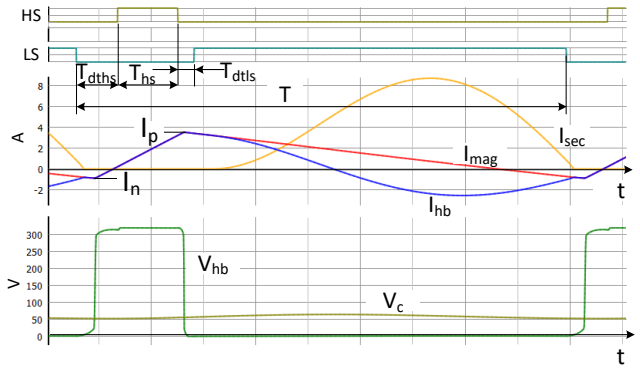


Figure 6-2: Asymmetrical HB flyback waveforms under full load conditions showing significant dead times required to achieve ZVS.

parasitic elements and to maximize efficiency. Typically, resonant operation is desired. This can be achieved when the on-time of the low side switch (T_{ls}) matches to ½ of the resonant period formed by L_{lk} and C_r [7].

For the following analysis, the most interesting operation point is the one at maximum output current. Figure 6-2 shows a simulation of the converter under such conditions.

As explained in [6], the DC value of the magnetizing current (I_{mag}) is equal to I_{out}/N. This leads to the worst case of minimum absolute value of I_n. On the other hand, I_n needs to be sufficient to achieve ZVS when the HS switch turns on.

Synchronous rectification (SR) can be used in the secondary side to boost efficiency [10]-[11]. In such a case, the parasitic output capacitance of the SR switch, reflected to the primary side, needs to be considered.

The value of I_n and the dead times (T_{dtls}, T_{dths}) required to achieve ZVS will impact the efficiency of the converter. This will be explained in detail in the next sections.

Higher frequencies are desired to further reduce the converter size, to achieve that, short dead times and ZVS are the key features. Small parasitic capacitances associated to the switching nodes allow ZVS and reduced dead times, therefore, GaNs and SiCs are very suitable devices to serve this purpose.

6.3. Switches and its parasitic elements effects

There are three major parameters of the switches that affect the efficiency: $R_{ds(on)}$, $C_{o(er)}$ and $C_{o(tr)}$. The first one has a direct impact on the resistive losses. $C_{o(er)}$ affects directly the amount of negative current (I_n) required to achieve ZVS and $C_{o(tr)}$ affects the dead times; as no power is transfer during dead times the loss of usable time needs to be compensated with higher peak current (I_p) which results in higher conductive and magnetic losses. As explained before, these effects become especially important at full load where the amount of negative current reaches its minimum in absolute value and results therefore in longer dead times. Obviously, these restrictions appear as long as ZVS is desired to be maintained. If hard switching is allowed such restrictions would not apply, but loses due to hard-switching and other undesired negative effects will appear, i.e. EMI or SR V_{ds} overshoot.

6.3.1. Required negative current (I_n) for ZVS operation

In order to achieve ZVS, the primary inductance has to store an amount of energy equal to the energy stored in the parasitic capacitance associated to the half-bridge (HB) node. Considering only the parasitic capacitance of the primary switches, the amount of negative current is given by (6-2). For the sake of simplicity the use of same switches for HS and LS it will be assumed.

$$|I_n| = V_{in}\sqrt{2C_{o(er)}/L_p} \tag{6-2}$$

Furthermore, the time required to achieve ZVS depends on the $C_{o(tr)}$ value if only the parasitic elements from the primary switches are considered. Assuming that the primary inductance of the transformer provides a constant current equal to I_n, the dead time required between LS turn off and HS turn on can be estimated as shown in (6-3).

$$t_{dths} = \frac{2V_{in}C_{o(tr)}}{|I_n|} = C_{o(tr)}\sqrt{\frac{2L_p}{C_{o(er)}}} \tag{6-3}$$

The dead time for the LS switch can be calculated as shown in (6-4).

$$t_{dtls} = \frac{2V_{in}C_{o(tr)}}{I_p} \tag{6-4}$$

In the following, the impact on the peak current due to the negative current and the dead times will be estimated. From [7] the relation between peak currents and output power, Equation (6-5), is known.

$$P_{out} = \frac{V_{in}(I_p + I_n)}{2T}t_c \tag{6-5}$$

Where T can be expressed as $T = t_c + t_d + t_{dths} + t_{dtls}$. From (6-5) the required I_p can be calculated as shown in (6-6).

$$I_p = \frac{2I_{out}(1 + t_{dt}/T_a)}{N} - I_n \tag{6-6}$$

Where $t_{dt} = t_{dths} + t_{dtls}$ and $T_a = t_c + t_d$ and can be expressed as shown in equation (6-7).

$$T_a = \frac{(I_p - I_n)L_pV_{in}}{NV_{out}(V_{in} - NV_{out})} \tag{6-7}$$

Substituting (6-7) in (6-5) the relation between I_p and t_{dt} can be we found as a second order equation (6-8).

$$I_p = \frac{2I_{out}}{N}\left[1 + \frac{t_{dt}(I_p - I_n)L_pV_{in}}{NV_{out}(V_{in} - NV_{out})}\right] - I_n \tag{6-8}$$

The resulting switching frequency of the converter can be expressed as shown in (6-9).

$$F_{sw} = \frac{1}{T_a + t_{dt}} \tag{6-9}$$

6.3.2. Practical switches example

Let's have a look to different switches and its characteristics (Table 6-1) in order to evaluate the impact on the converter under ZVS conditions.

Table 6-1: Different switches to be studied

Part number	Technology	$V_{ds\ max}$ (V)	Typ $R_{ds(on)}$	$C_{o(er)}$ (pF)	$C_{o(tr)}$ (pF)
IGO60R070D1	GAN	600	55	80	102
IGT60R190D1S	GAN	600	140	32	40
IMZA65R072M1H	SiC	650	72	98	129
IMW65R107M1H	SiC	650	107	66	87
IPL60R065C7	Si	600	56	101	1050
IPP60R180C7	Si	600	155	34	349

Using the equations from section 6.3.1 and considering a practical converter design, i.e. L_p= 53uH, N = 2.83, V_{in} = 320V and I_{out} = 3.25A, the next values of the required I_n and T_{dls} can be calculated, see Table 6-2.

Table 6-2: negative current and dead time required for ZVS

Part number	$\|I_n\|$ min for ZVS	T_{dtls}
IGO60R070D1	0.55A	117ns
IGT60R190D1S	0.35A	73ns
IMZA65R072M1H	0.61A	134ns
IMW65R107M1H	0.5A	110ns
IPL60R065C7	0.62A	1075ns
IPP60R180C7	0.36A	616ns

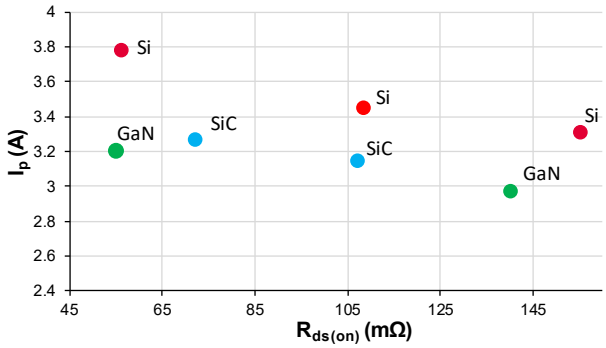


Figure 6-3: Example of the required I_p vs. R_{ds}(on) for different devices and technologies.

The necessary current I_p can be estimated by iterating over equation (6-8) since the resulting I_p will influence T_{dths}, T_{dtls} and T_a. The result for the selected switches is show in Figure 6-3. $R_{ds(on)}$ is used in the x-axis since it is the major figure of merit of the switches.

In Figure 6-3 it can be seen that, for the given example, GaN offers the optimum solution with a minimum peak current for the same output power, followed by SiC and then Si. Lower I_p will enable lower conductive and magnetic loses. Typically, the lower operating frequency,

due to higher peak-to-peak current, does not compensate the losses due to higher magnetizing flux.

To further understand the impact of the output capacitance (C_{oss}) for different input voltages, three of the switches, with similar (although not equal) $R_{ds(on)}$, have been selected: IGT60R190D1S, IMW65R107M1H and IPP60R180C7. Figure 6-4 illustrates the necessary I_{hb}

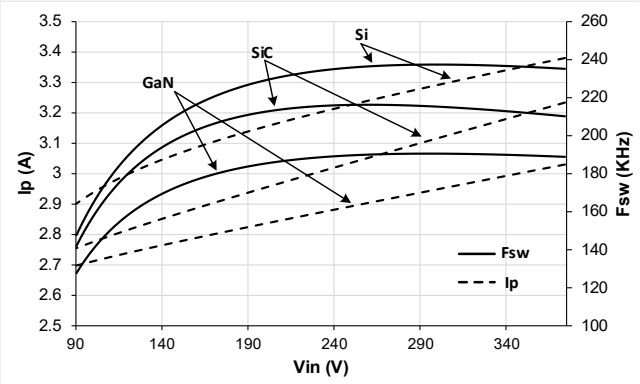


Figure 6-4: Example of required I_p to achieve ZVS and resulting F_{sw} versus input voltage (V_{in}).

peak current (I_p) and switching frequency (F_{sw}) required for the previously given practical example. It can be observed that the GaN requires significant lower I_p current to achieve the same output power, this difference becomes even more visible for higher input voltages. SiC devices follow GaN devices closely (keep in mind that the selected SiC device has a lower $R_{ds(on)}$ and therefore higher C_{oss}). Additionally, compared to Si switches, the selected SiC and GaN switches have lower conductive loses due to the slightly lower $R_{ds(on)}$. The lower C_{oss} results in smaller dead times enabling higher switching frequencies.

In terms of efficiency, it is desired to work with a lower peak current and a slightly higher frequency. The peak current affects the conductive loses and the magnetic core losses, while the frequency only affects the magnetic losses. This efficiency tendency will be shown comparing the difference devices on the same converter prototype under the same conditions.

Figure 6-5 shows real measurements of the waveforms for Si, SiC and GaN. The used

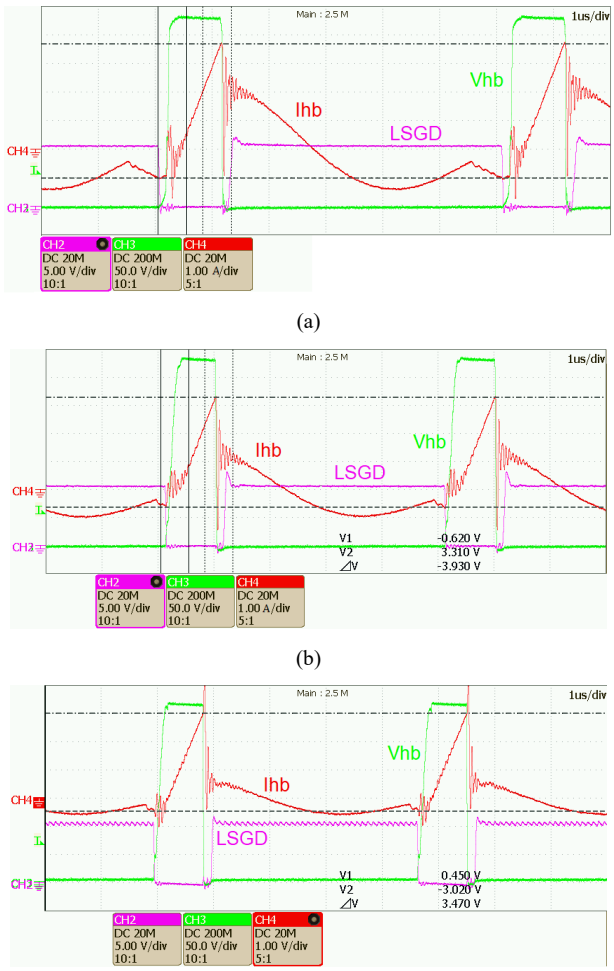


Figure 6-5: Example of practical waveforms on the same converter under the same conditions, a) Si: IPP60R180C7, b) SiC: IMW65R107M1H c) GaN: IGT60R190D1S.

prototype had the following parameters and operating point: L_p= 53uH, N = 2.53, V_{out} = 20V and I_{out} = 3.25A. The higher peak current required by Si switches in order to achieve ZVS can be seen. As previously described, the additional capacitance associated to the HB node increases the required peak current (and results in lower F_{sw}). The peak currents were I_p = 3.69A, I_p = 3.31A and I_p = 3.02A for the Si, SiC and GaN cases respectively. The adaptor efficiency under these conditions has been 94.5% in the case of Si, 94.9% using SiC and 95.1% with GaN.

6.4. Other considerations

In the previous section, the impact of the switches output capacitance on the operation of the converter has been analyzed. To better understand the effect of the primary switches, any other parasitic capacitances associated to the HB node have been excluded. In a practical case, the intertwining capacitance and output capacitance of the synchronous rectification MOSFET in the secondary side, if present, will increase the capacitance associated to the HB node.

Another beneficial effect of using WBG devices is the so called “dip” effect, which has been deeply analyzed in the next publication [12]. This effect helps reducing the RMS currents, especially in the secondary side, and increasing in this way the efficiency in comparison to Si.

Regarding the $R_{ds(on)}$, SiC devices show considerably less dependency on temperature compared to GaN or Si, see Figure 6-6. This will give an advantage to SiC, especially in applications with working temperatures above 25°C, i.e. high-density adaptors. This is especially helpful at low input voltage due to higher conductive loses.

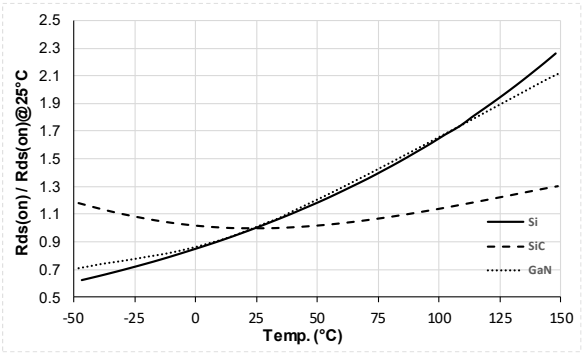


Figure 6-6: Normalized $R_{ds(on)}$ versus temperature for different switches technologies.

6.5. Experimental prototype

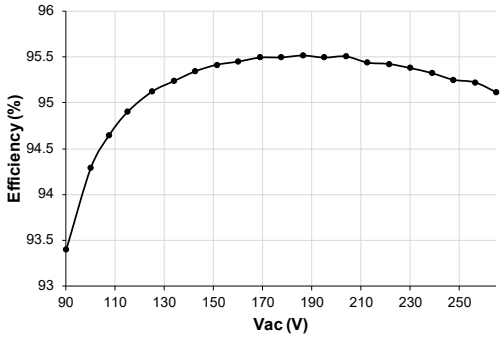
To demonstrate the capability of WBG devices to increase the performance of the asymmetrical half-bridge flyback, a 65W prototype (see Figure 6-7a) using 600V/190mOhm GaNs has been developed. The achieved power density is 1.92W/cm^3 (31.5W/inch^3) uncased. It supports USB-PD standard with output voltage profiles from 5V/3.25A to 20V/3.25A. The operation frequency varies from 140 kHz to 300 kHz depending on the input voltage. The achieved peak efficiency is 95.5% as shown in Figure 6-7b.

The key parameters of the converter are shown in Table 6-3.

Table 6-3: Transformer and switches information

Parameter	Manufacturer	Value
Core type	TDK	X20/8.25
Core material	TDK	PC95
Lp		53uH
Np/Ns		3
SR Mosfet	Infineon	BSC093N15
HB switch	Infineon	IGI60F1414A1L

(a)



(b)

Figure 6-7: a) Asymmetrical HB flyback prototype using GaNs. b) Total converter efficiency vs. input voltage (V_{ac})

6.6. Conclusions

The asymmetric HB flyback converter can achieve ZVS and secondary ZCS allowing an increase of the switching frequency. The presented converter in combination with WBG switches has been identified as the most promising topology for highly efficient and very compact USB-PD adaptors. GaN switches (with their extremely low C_{oss}) and SiC switches (with their $R_{ds(on)}$ dependency on temperature) can achieve similar power densities. From the three analyzed technologies, GaN, due to its low C_{oss}, allows shorter dead times and can easily achieve ZVS, therefore it is the most suitable for higher switching frequencies. The performance has been demonstrated with a 65W prototype that achieves a minimum efficiency of 93.4% at full load and 90Vac and a peak efficiency of 95.5%.

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7. PUBLICATION 5: A HIGH-EFFICIENCY ISOLATED WIDE VOLTAGE RANGE DC-DC CONVERTER USING WBG DEVICES

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A HIGH-EFFICIENCY ISOLATED WIDE VOLTAGE RANGE DC-DC CONVERTER USING WBG DEVICES

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ABSTRACT: The recent release of the standard USB-PD 3.1 [1] specifies variable output voltages from 5 V to 48 V featuring a step forward towards a universal adaptor but rising new challenges for the converter topologies used up to now. In such applications, a first AC-DC stage is followed by a DC-DC stage. In this paper, emerging WBG technologies are applied to the asymmetrical half-bridge flyback topology, demonstrating the potential of such combination as a wide voltage range DC-DC stage. Its suitability for high-density and high-efficiency USB-PD Extended Power Range (EPR) and battery charger applications is discussed. The impact of different switching technologies, silicon and wide band gap, is analyzed. A general method to dimension the converter is presented and an iterative process is used to evaluate the theoretical efficiency under different conditions and switching devices. Finally, the advantages of the presented converter using Gallium Nitride (GaN) devices are demonstrated in a 240 W DC-DC prototype. It achieves a full load efficiency of 98%, and it is able to deliver an output voltage from 5 V to 48 V with input voltage range from 120 V to 420 V, as well an outstanding power density of 112 W/inch^3 uncased.

Index terms: GaN, Adaptor, USB-PD EPR, Power density, Battery charger

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7.1. Introduction

Recent trends push existing AC-DC adaptors towards a universal power supply capable of being used for many different purposes, from charging smartphones or tables to laptops, e-bikes or power tools. One major standard in this direction is the recent publication of the USB-PD Extended Power Range (EPR) [1], which defines adaptors with output voltage ranging from 5 V to 48 V and up to 240 W. Furthermore, to ensure the acceptance of such universal power adaptor, a reduce size and limited weight is desired. Lastly, to allow the usage of any adaptor

worldwide, universal input voltage range (100 Vac to 240 Vac) is an expected characteristic. The new USB-PD specification, combined with wide input and output voltage ranges, bring additional challenge to achieve very high power density and efficiency [2] for the topologies and architectures used in converters up to now.

Possible solutions in this application include PFC followed by a flyback-based converters [3] - [8], see Figure 7-1a, they are extremely flexible in terms of input and output voltage range, but they are very bulky due to its transformer size. LLC based converters [9], [10] can be very small and efficient but they are very limited in terms of input and output voltage range. They are the preferred solution for high power and fixed output voltage and are typically combined with a Power Factor Correction (PFC) boost converter as first stage.

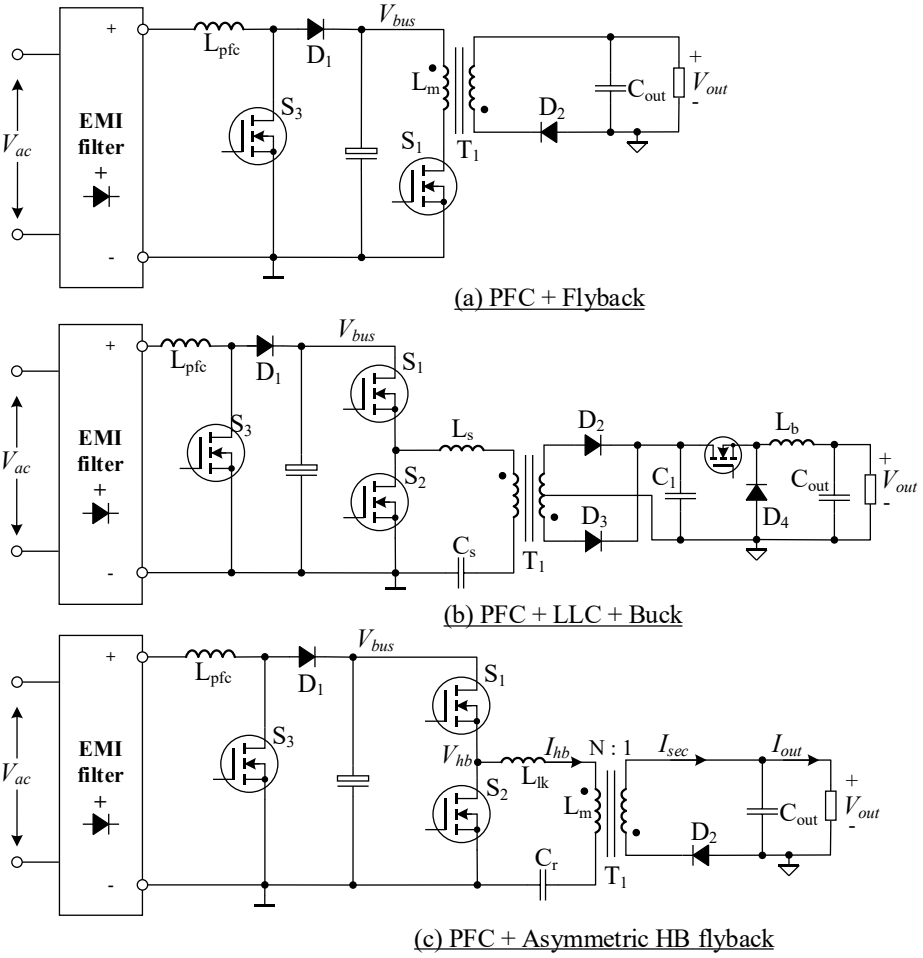


Figure 7-1: Suitable architectures for the discussed applications. Proposed solution (c): Boost PFC (AC-DC stage) followed by AHB converter (DC-DC stage).

If the LLC topology is used, wide output voltage can be achieved adding an additional downstream buck stage. However, a three-stage converter configuration (PFC + LLC + Buck, Figure 7-1b), will lead to a bulky and expensive converter.

This paper proposes a PFC followed by an asymmetrical half-bridge flyback (AHB) topology, also known as Hybrid Flyback [11], using GaN devices, see Figure 7-1c.

The combination achieves optimum performance in terms of wide voltage range, small size, high efficiency and low number of components for the DC-DC stage thanks to the figure of merit $R_{dson}C_{o(tr)}$ of wide band gap switches and the characteristics of the topology.

This manuscript is organized as follows: firstly, a theoretical review of the AHB topology is carried out. Secondly, general design rules and an estimation of the efficiency with a numerical iteration method is shown. Afterwards the prototype used to demonstrate the analytical results is presented as a base for the conclusions of the paper.

7.2. Energy processing in power converters

In some non-isolated converters, a percentage of the energy is transferred directly from the input to the output and does not need to be stored in reactive elements, but the rest of energy needs to be processed, meaning that it has to be stored and released by reactive elements [12] – [15]. Examples of that are buck or boost converters where the current flows directly from the input to the output during certain phase of the operation without processing the energy [12], [13].

An analogue operation to direct energy transfer is observed in isolated converters when the energy is transferred in forward mode through the transformer [16]. This effect avoids energy storage in magnetics components, which is typically more expensive in terms of efficiency and size than capacitive energy storage [17].

With the previous considerations, and to ensure the best efficiency and minimum size, different characteristics are desired in power converters:

1. In isolated converters: maximize energy transfer in forward mode. In non-isolated converters: maximize direct energy transfer.
2. When energy is stored in magnetic components, higher frequencies help to reduce the size.
3. Zero voltage switching (ZVS) and zero current switching (ZCS) techniques to minimize switching losses, especially if high switching frequencies (F_{sw}) are used.
4. Lowest possible RMS currents to reduce conduction losses.
5. In general, minimum number of elements involved in the energy transfer process.

For the design of the converter, the above characteristics must be balanced to achieve an optimal design for the given requirements.

7.2.1. Proposed topology

In AC-DC applications where a PFC (Power Factor Correction) [18] is required, a dual stage approach is typically used, consisting of a PFC boost converter followed by a DC-DC stage with isolation. Example of such applications are USB-PD, battery chargers or AC-DC adaptors.

Due to its hybrid nature forward/flyback [19], the asymmetrical half-bridge flyback is very appropriate for such applications and can fulfill the previously listed desired characteristics in an optimal way, making it especially suitable for high-density designs.

In order to demonstrate the potential size reduction of this topology, an example converter acting as DC-DC stage is dimensioned to provide 5 V to 48 V output and 5 A, with a turns-ratio N (primary to secondary) of 4.2 and a V_{bus} voltage of 380 V. Under these conditions, approximately 53% (NV_{out_max}/V_{bus}) of the energy is stored in the capacitor and transferred in a forward mode, resulting in less magnetic energy storage and therefore, smaller transformer compared to any flyback converter, where 100% of the energy is stored in the transformer. This is explained in more detail in [19], [20].

In the next section, some general design rules will be presented and the loss mechanism in the different elements will be analyzed to obtain an estimation of the efficiency.

7.2.2. General design guidelines for AHB flyback

An example of the converter target requirements is shown in Table 7-1.

Table 7-1: Desired AHB flyback converter characteristics

Parameter	Value
Input voltage range	120 V to 420 V (Vout dependent)
Output voltage range	5 V to 48 V
Maximum output current	5 A
Efficiency	Max@full load @ V_{in} = 380 V
Power density	>50 W/inch^3

In high power density adaptors, it is desired to minimize the amount of power dissipated at any load, typically the worst case occurs at full load. This means that the efficiency needs to be optimized for the highest output power: 48 V/5 A at the given input voltage of 380 V. An accurate analytical model that finds such optimum point is complex, especially due to the multiple possible magnetics designs and their losses model complexity. Therefore, an iterative process over different component choices can further help to find the optimal dimensioning.

Based on the operation principle explained in [19] and [21], the next general design steps can be applied:

The turns-ratio (N) is the most important parameter in the design of this converter. It affects the secondary RMS currents and the reverse voltage to withstand by the output rectifier. A good starting point is to target 45% to 55% duty cycle at the nominal input voltage (V_{in_nom}) and maximum output voltage (V_{out_max}) to calculate N.

$$D \approx \frac{NV_{out\_max}}{V_{in\_nom}} \tag{7-1}$$

Using D = 53%, a turns-ratio of approximately 4.2 is obtained from (7-1). Using (7-2) the maximum reverse voltage in the secondary rectifier (V_{ds_SRmax}) can be calculated, which is especially important if a synchronous rectification switch is used to improve the efficiency, as in this case [22] - [24].

$$V_{ds\_SRmax} \approx \frac{V_{in\_max}}{N} \tag{7-2}$$

With the given maximum input voltage (V_{in_max}) of 420 V (worst case), 100 V is obtained from (7-2).

In the next step, the maximum (I_{hbh}) and the minimum (I_{hbl}) magnetizing current need to be estimated. The relation between the desired output current (I_{out}) and the current in the half-bridge can be approximated by (7-3) [19]:

$$I_{out} = \frac{N\left(I_{hb_h} + I_{hb_l}\right)}{2} \tag{7-3}$$

I_{hbl} is set to the minimum required negative current to achieve ZVS under full load conditions. This allows minimizing the peak-to-peak current (I_{hb_pp}). Its value depends on the C_{oss} of the used switches and the transformer primary inductance. Not only the primary switches C_{oss} (C_{oss_hs} and C_{oss_ls}) needs to be considered but as well, the C_{oss} of the synchronous rectification switch (C_{oss_SR}) in the secondary side [21] - [23], if present. The total primary equivalent capacitance (C_{p_eq}) to achieve ZVS is shown in (7-4).

$$C_{p\_eq} = \frac{C_{oss\_SR}}{N^2} + C_{oss\_hs} + C_{oss\_ls} \tag{7-4}$$

Based on experience, a good starting point is to use 20% to 25 % of I_{hbh} if Si MOSFETs are used and 15% in case of GaNs devices. Taking I_{hbl} = 15% of I_{hbh}, I_{hbh} =2.8 A and I_{hbl} = 0.42 A will be obtained.

In a next step, using the obtained value of I_{hbl}, the exact value of the transformer inductance ($L_p = L_{lk} + L_m$) can be calculated.

Assuming small variations of the resonant capacitor voltage (V_{cr}), the charge (T_c) and discharge (T_d) times (7-5) and (7-6) of the magnetizing transformer current can be used to obtain the switching period (T) from (7-7) [21]:

$$T_c = \frac{L_p}{V_{in} - V_{cr}} I_{hb\_pp} = \frac{L_p}{V_{in} - NV_{out}} I_{hb\_pp} \tag{7-5}$$

$$T_d = \frac{L_p}{V_{cr}} I_{hb\_pp} = \frac{L_p}{NV_{out}} I_{hb\_pp} \tag{7-6}$$

$$T = I_{hb\_pp} L_p \frac{V_{in}}{(V_{in} - NV_{out})NV_{out}} \tag{7-7}$$

Equation (7-7) shows that the switching frequency ($F_{sw} = 1/T$) increases with higher input voltage (V_{in}). Based on the frequency range of the transformer magnetic core, the desired operating frequency is set to 250 kHz at the nominal input and output voltage. This way L_p = 117 µH is obtained.

Knowing L_p, the exact value of the required negative current to achieve ZVS can be calculated by matching the energy in L_p and to the parasitic capacitance associated to the half-bridge node (C_{p_eq}) for the worst case (V_{in_max}), this is shown in (7-8).

$$\frac{1}{2} L_p I_{hbl}^2 > C_{p\_eq}(V_{in\_max}) V_{in\_max}^2 \tag{7-8}$$

On the other hand, the negative current needs to be compensated with positive peak current as indicated by (7-3), therefore devices with lowest C_{oss} (and in particular low $C_{o(tr)}$ as explained in [25]) are desired. High peak-to-peak current (I_{hb_pp}) not only affects the amount of conductive losses but as well increases the magnetic losses.

To reduce conductive losses, switches with low R_{dson} and C_{oss} are desired. On the other hand, power switches show a dependency of the output capacitance C_{oss} with R_{dson}. Therefore, a tradeoff between both parameters needs to be achieved when choosing the devices. Considering the previous statements, Figure 7-2 shows that wide bandgap devices, particularly those based on GaN technology [26], [27], are the closest to an ideal switch (zero ON resistance (R_{dson}) and parasitic capacitance $C_{o(tr)}$) and therefore the most suitable for this application.

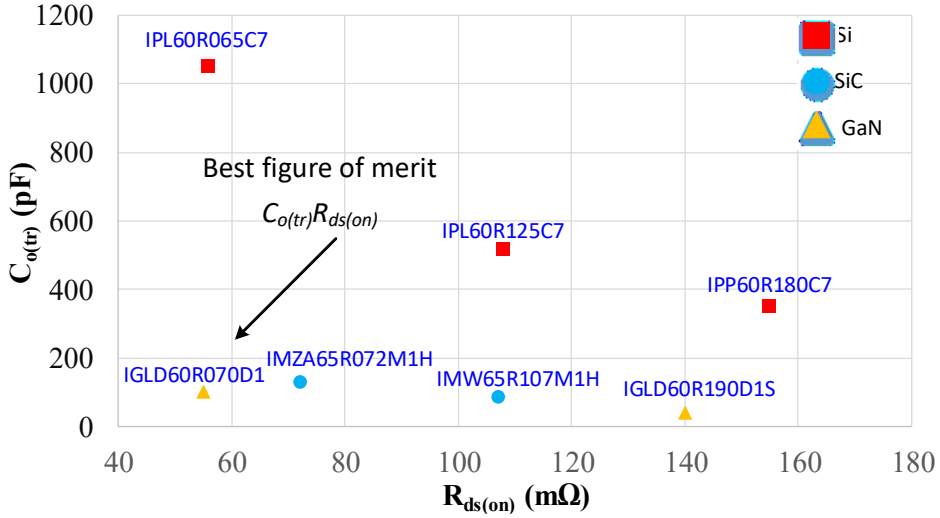


Figure 7-2: $C_{o(tr)}$ vs. $R_{ds(on)}$ parameters for different switches and technologies. GaN devices show the best figure $R_{ds(on)}C_{o(tr)}$.

The dependency of the losses with the required negative magnetizing current to achieved ZVS is complex to calculate. As described in [21], the temporal equations of the system do not have a numeric solution, therefore simulation can provide the value of the RMS and peak-to-peak currents to calculate conduction and magnetic losses respectively.

The transformer design requires a tradeoff between copper and magnetic losses, typically, the peak to peak flux needs to be selected according to the switching frequency. As example of design, the peak to peak flux is chosen to 200 mT and the peak flux to around 175 mT, avoiding high values which increase magnetic losses and the risk of saturation. A core type EQ25 has been selected due to its small size and low profile. As calculated previously, the primary to secondary turns-ratio is 21:5 and the chosen ferrite material is 3C95 due to its low losses over temperature for the given operating (F_{sw}).

Finally, to minimize the RMS value of the currents at full load, the resonant capacitor (C_r) is adjusted to match the discharge time (ON time of the LS switch: T_{ls}) considering the transformer leakage inductance (L_{lk}), as shown in (7-9). The resulting waveforms would be similar to those in Figure 7-3.

$$T_{ls} \approx \pi\sqrt{C_r L_{lk}} \tag{7-9}$$

7.3. Estimation of the converter efficiency

Assuming perfect ZVS and ZCS conditions, and therefore neglecting switching losses, the total losses of the converter consist of conductive losses in the different resistive elements,

magnetic losses in the core of the transformer and control and driving losses. To calculate the first ones, the RMS currents and the resistance of each element are needed. For the second ones the volumetric losses and core size are required. The losses due to control and driving are estimated to be approximate 0.5 W.

The RMS values of the different elements can be extracted from simulations. Figure 7-3 shows the simulated waveforms of the converter in steady state under the conditions: V_{in} = 380 V and V_{out} = 48 V / I_{out} = 5 A. I_{mag} represents the transformer magnetizing current and I_{hb} and

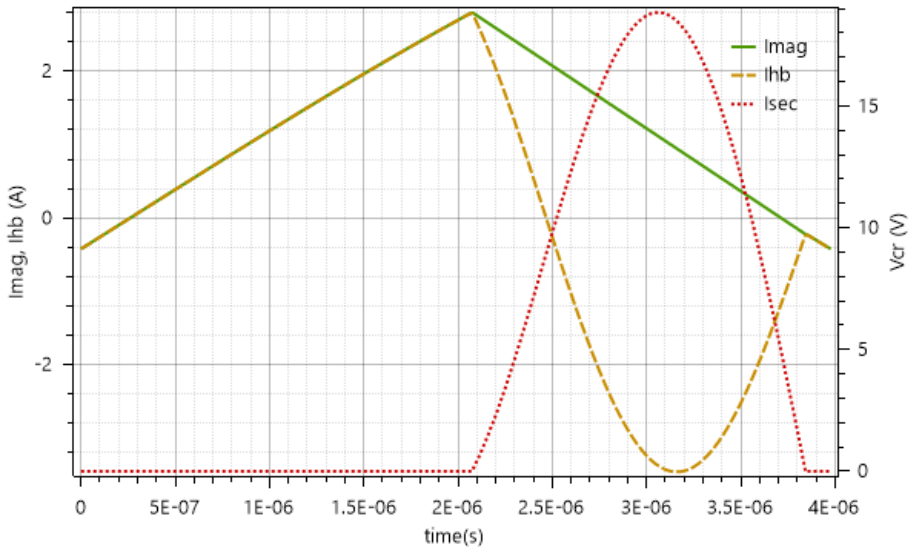


Figure 7-3: Simulated waveforms under the conditions: V_{in} = 380 V, V_{out} = 48 V, I_{out} = 5 A.

I_{sec} the primary and secondary transformer currents respectively, both represented in Figure 7-1.

To estimate the magnetic losses, the magnetic field (B) induced by the magnetizing current (I_{mag}) needs to be calculated as shown in (7-10), being A_e the effective area of the core.

$$B(t) = \frac{I_{mag}(t) L_p}{A_e N} \tag{7-10}$$

The volumetric losses can be calculated using vendor specific tools or ferrite datasheet. When available, the Steinmetz coefficients and sinusoidal approximation can be used. The magnetic losses given in datasheet are typically based on homogenous distribution of the magnetic flux in a ring core, therefore an extra of 20% losses is added for non-homogenous distribution in specific ferrite core. Table 7-2 shows the loss breakdown in the different components under the simulated conditions shown in Figure 7-3.

Table 7-2: Loss breakdown @380Vin

Element	Irms/Flux	Rds(on)	Ploss
Input capacitor	0.926 A	250 mΩ	0.214 W
HS switch	1.137 A	190 mΩ	0.245 W
LS switch	1.578 A	190 mΩ	0.473 W
Shunt resistor	1.137 A	90 mΩ	0.116 W
Transformer primary	1.946 A	100 mΩ	0.378 W
Transformer secondary	8.85 A	5 mΩ	0.392 W
Magnetic core	-24 to 173 mT	3C95	0.775 W
SR	8.85 A	15 mΩ	1.175 W
Output capacitor	7.16 A	10 mΩ	0.512 W
Controller & driving	-	-	0.5 W
Efficiency			**4.78 W => 98.04%**

To better understand and optimize the converter, a numerical method has been developed. It iterates over the equations that define the converter [21] and extracts the currents required to calculate the resistive and magnetic losses under different conditions.

Figure 7-4a shows the efficiency over the input voltage and Figure 7-4b shows the loss breakdown over input voltage ranging from 300 V to 500 V obtained with this method. The listed elements are: input capacitor (C_{in}), transformer primary winding (T_{prim}), high side switch (HS_sw), current sense resistor (R_{shunt}), low side switch (LS_sw), transformer secondary winding (T_{sec}),

synchronous rectifier switch (SR_sw), output capacitor (C_{out}) and transformer core (Core)

It is clearly seen how the resistive losses dominate at low input voltage whereas magnetics

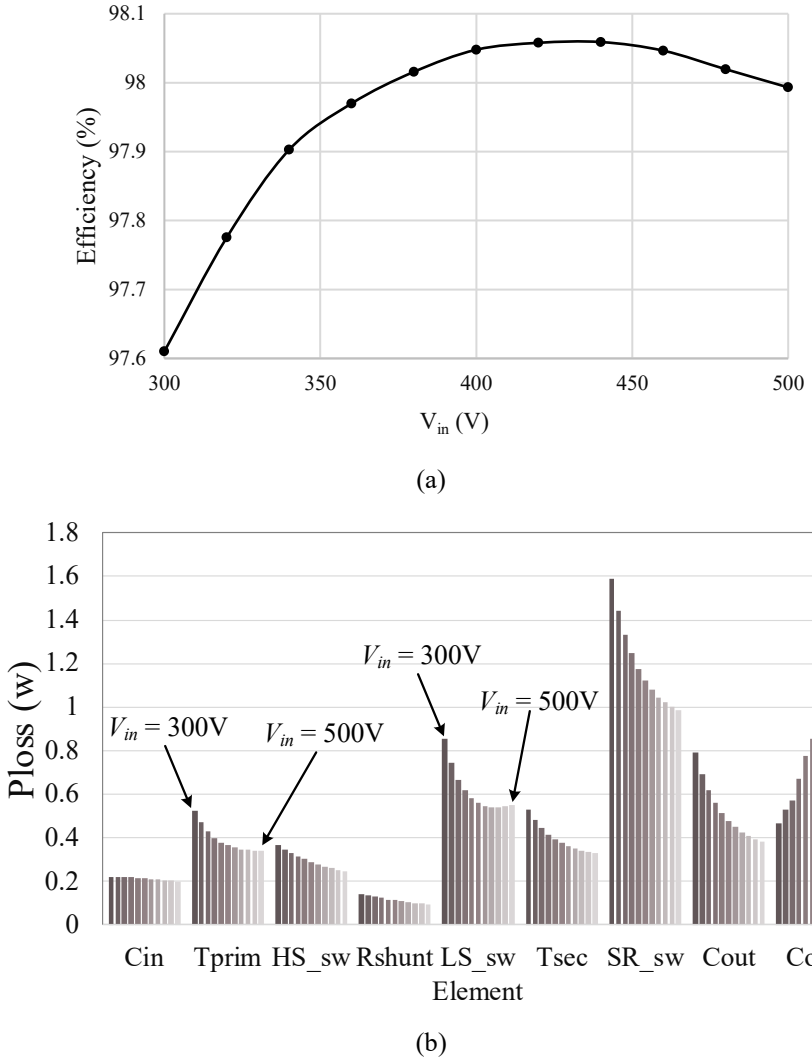


Figure 7-4: (a) Calculated efficiency vs. input voltage, (b) components loss breakdown for different input voltages (V_{in}).

losses in the core are dominant at higher input voltage due to the frequency increase and higher magnetizing current required to achieve ZVS.

The same method is used to evaluate different switches and input voltages to estimate the efficiency. Such method complements the general design rules explained before and helps finding the optimal design. Figure 7-5 shows the superior performance of the GaN devices compared to Silicon for the reasons previously explained.

7.4. Prototype

Finally, a prototype has been built to support the theory. The dimensioning has been done accordingly to the presented guidelines and design optimization process to fulfill the requirements given in Table 7-1. The devices used in the final design are shown in Table 7-3.

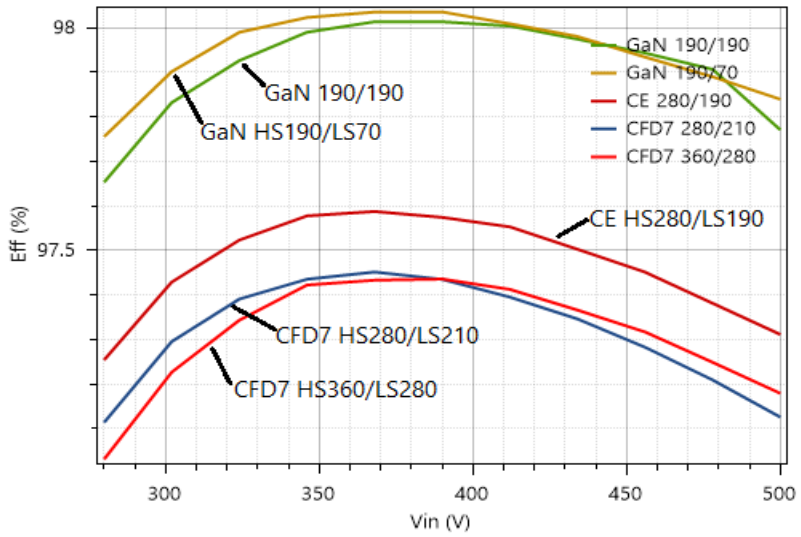


Figure 7-5: Calculated efficiency vs. input voltage for different devices and technologies (GaN and Si: CFD7 and CE) from Infineon.

Table 7-3: Main components of the converter prototype

Element	Characteristics	Part number
Controller	AHB controller	XDPS2201 (modified)
Input capacitor	450V/47uF	450BXW47MEFR16X25
HS GaN	190mΩ/600V	IGLD60R190D1
LS GaN	190mΩ/600V	IGLD60R190D1
SR Mosfet	9.3mΩ/150V	BSC093N15NS5
Output capacitor	3x330uF/50V	A750MW337M1HAAE020
SR Mosfet	9.3mΩ/150V	BSC093N15NS5

Table 7-4 shows the transformer construction details.

Table 7-4: Transformer specification

Element	VALUE
Core type	EQ25 (16mm height)
Core material	3C95
Lm	120 uH
Llk	3 uH
Np	21 turns (Litz 40 × 0.1 mm)
Ns	5 turns (TIW Litz 120 × 0.1 mm)
Winding interleaving	P-S-P

Figure 7-6 shows a picture of the prototype and Figure 7-7 the measured efficiency at full load vs. input voltage, the measured efficiency follows the same pattern as the simulated efficiency in Figure 7-4. The primary signal waveforms are shown in Figure 7-8 where ZVS

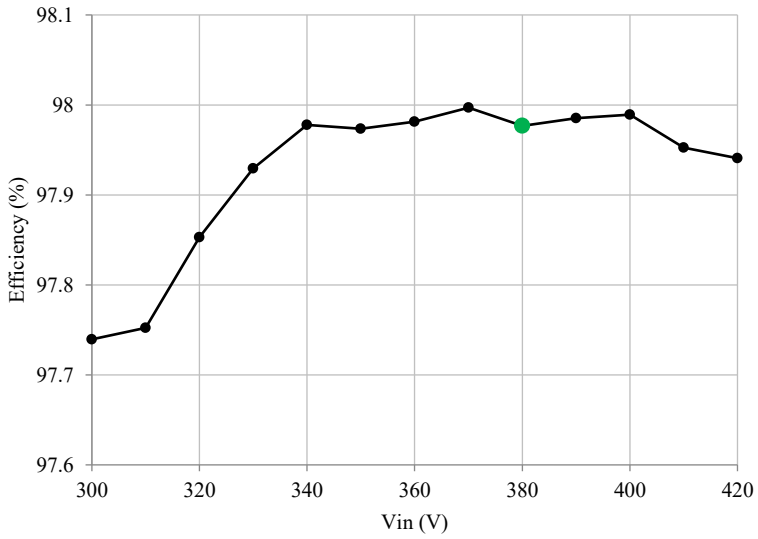
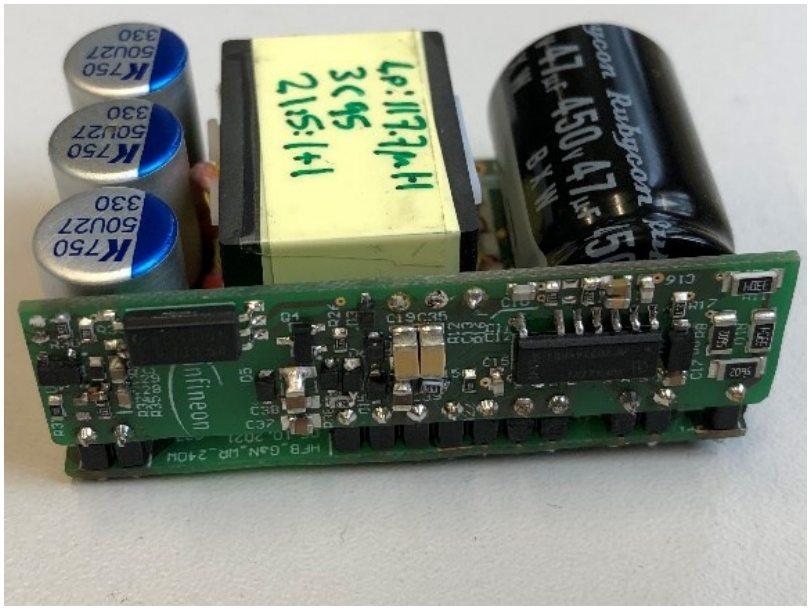


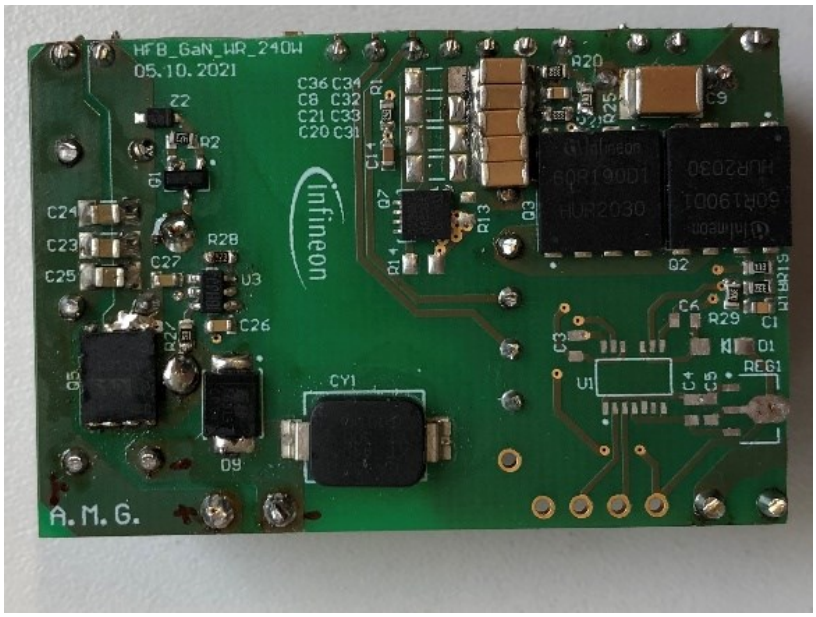
Figure 7-6: Full load (48 V / 5 A) efficiency versus input voltage, green dot mark the nominal input voltage.

can be observed.

Figure 7-9 shows the thermal behavior at full load under 380V input. As expected from the loss breakdown it can be observed that the SR MOSFET is the hottest device in the design.



(a)



(b)

Figure 7-7: Top and back side view of the 240 W DC-DC GaN prototype. Size: 51x36x19 mm, power density: 112 W/inch^3.

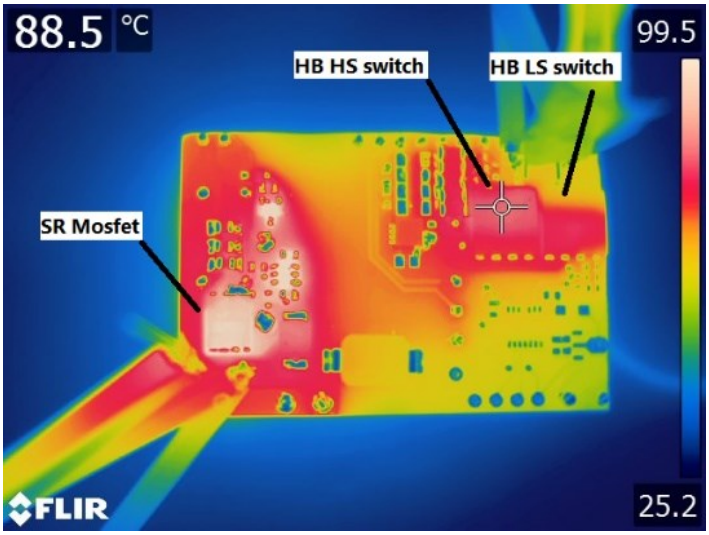


Figure 7-8: Thermal picture of the components side at 380 V input voltage.

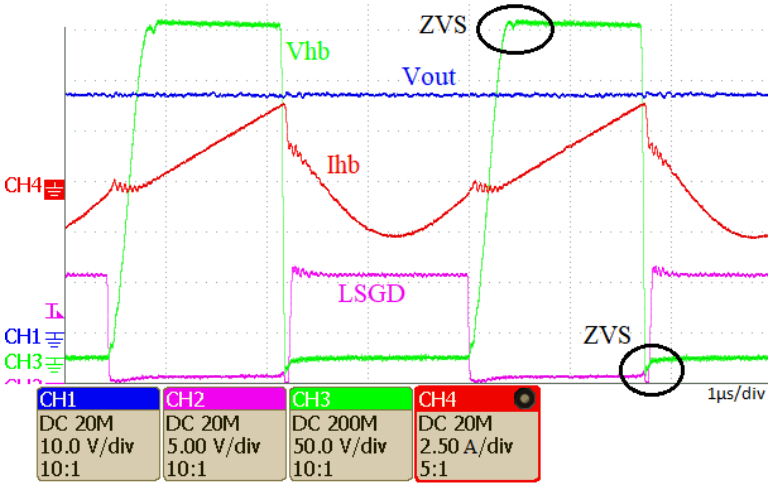


Figure 7-9: Full load oscilloscope waveforms showing Vhb ZVS operation.

Finally, Figure 7-10 and Figure 7-11 show the efficiency versus output voltage and load respectively. Different control methods are applied depending on the output conditions (forced

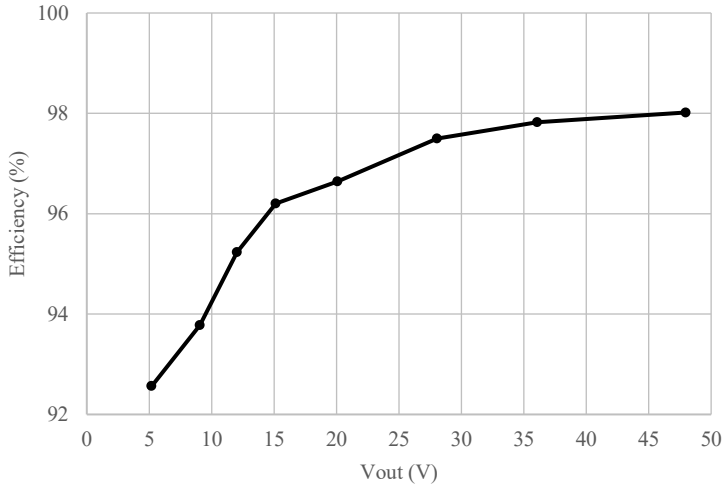


Figure 7-10: Efficiency versus output voltage for I_{out} = 5 A.

CCM at heavy load and DCM at light load) as explained in [21].

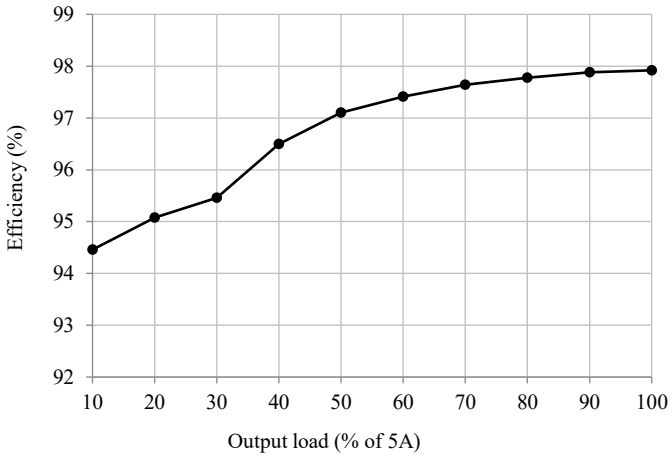


Figure 7-11: Efficiency vs. load @48 V output 380 V input.

7.5. Conclusions

A GaN-based Asymmetrical Half-Bridge Fyback converter has been proposed as an isolated second-stage DC-DC converter for USB-PD EPR and battery chargers applications. The proposed topology combined with GaN switches technology achieves outstanding characteristics for such applications: high efficiency, high power density and wide output voltage range. A general method for dimensioning the converter has been presented and the results of a computational iterative method to optimize the final design has been shown.

The efficiency (98%) and power density (6.88 W/cm^3 or 112 W/inch^3) provided by the converter, thanks to the forward energy transfer mode, outperforms many other state-of-the-art

topologies. Furthermore, the capabilities to provide wide input and output voltage range, thanks to the flyback energy transfer mode, makes the converter the optimal choice for battery charger and USB-PD EPR applications.

Wide band gap devices and in particularly GaNs, due to its low C_{oss} enabling low circulating current, are especially suitable for this topology. They can provide higher efficiency and a better performance than Si based devices.

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8. RESULTS AND CONCLUSIONS

8.1. Results

In this work the thermal limits for adaptors, where no forced ventilation is available, has been presented in 2.1. The relation between power density and efficiency has been shown, setting this way the basics for the targets to be achieved.

The proposed topology, asymmetrical half-bridge flyback, has been analyzed. The transfer function for the case of PWM duty cycle control and the temporal equations for the different phases of operation has been reviewed in 2.2 and 5.3.1 respectively.

A novel view of the converter behavior shows its hybrid forward-flyback nature, the dependency with the input voltage is studied in 3.3.3.

Different dimensioning procedures and considerations are described along this work in 3.4, 4.3.2, 5.3.3 and 7.2.2.

Novel control methods for wide input and output voltage operation are disclosed in 5.4, the proposed control methods ensue ZVS and ZCS and therefore are very suitable for high switching frequency operation.

Three different switches technologies, silicon (Si), silicon-carbide (SiC) and Gallium-Nitride (GaN) are applied to the converter and its behavior is analyzed and compared in 6, the results are verified in a converter prototype.

Finally in 7 a full performance prototype using GaN devices is presented and the losses in the different elements is analyzed for different input voltages, the prototype achieves 98% efficiency and a power density of 112W/inch^3, as well wide input and output voltage range is demonstrated, showing the full potential of the proposed solution.

8.2. Conclusions

In contrast with other existing type of power adaptors, USB-PD adaptors enable the reusability and universality that a power source requires for multiple devices, avoiding this way big amount of electronic waste. Enabling such power supply is a necessary step forward to protect our environment.

To avoid limiting such universal usage there is a tendency to increase the output power, in other cases the desired for higher output power could come from the target application needs, such as fast chargers. But, with increasing output power, the small size and lightweight selling feature is at risk.

This work has settled the basics to enable the asymmetrical half-bridge flyback topology as a first choice to fulfill the high efficiency and power density and, in many cases, cost, desired for USB-PD power adaptors. This has been demonstrated by several prototypes presented over this work.

Related to this converter, Infineon has filed several patents where the author of this work is inventor or co-inventor. Several commercial solutions are, at present time, available in the market. Example of that is *Anker 737 Charger GaNPrime 120W* which uses the hybrid flyback Infineon controller combined with GaN technology to provide outstanding performance.

8.3. Future work

In this work, the asymmetrical hybrid flyback converter has been deeply studied in its linear operation area and the proposed control methods are based on the approximation for such linear operation. Further studies could focus on understanding the nonlinear region, especially under low input voltage operation described in 5.3.4.

Software tools for dimensioning the converter would be required to simplify and better understanding the optimum operation of the converter.

Performance under higher switching frequencies is another open field to explore where wide-band-gap devices and specially GaN can show its benefits compare to silicon, under this conditions the magnetics components behavior is as well of interest.

In section 7, an outstanding 240W prototype has been shown, which most likely outperforms, in efficiency and power density, all the state of the art converter available today. Nevertheless it is believed that with increasing output power other converter will perform better due to lower RMS currents, such as LLC or phase shift full bridge (although they may not provide such wide input and output voltage range operation). Therefore the limit for higher power range where asymmetric half-bridge flyback is of interest compare to other converter types is still unclear.

9. APENDIX

9.1. Patents

In the next section a list of related patents from Infineon Technologies are listed, in all of them the Author of this work is inventor or co-inventor.

9.1.1. US11005378B2: Operating a flyback converter using a signal indicative of a resonant tank current of the flyback converter

File date: 20-June-2019

Granted date: 11-May-2021

Inventor(s): Alfredo Medina Garcia

Abstract:

Power converter controllers, flyback converters and methods are provided which use a resonant tank current of the flyback converter as a measure for an output current of the flyback converter. A power converter controller includes a control logic circuit that is configured to use, as a measure of an output current of the flyback converter, the resonant tank current indicated by the signal at a time in a phase where there is no reflected current to the primary side of the flyback converter.

9.1.2. DE102017110927A1: Flyback converter control, flyback converter and method of operating the flyback converter

File date: 19-Max-2017

Granted date: pending

Inventor(s): Alfredo Medina Garcia, Pierrick Ausseresse, Dr. Jörg Peter Oehmen

Abstract:

Flyback converters and related methods are provided. In one implementation, an on-time of a flyback converter low side switch is maintained substantially at a resonant half resonance period defined by a leakage inductance of a flyback converter and a capacitance value of a capacitor coupled to a primary winding of the transformer. Other methods, controls, and flyback converters are also provided.

9.1.3. US10797582B1: Cross conduction protection in a voltage converter

File date: 14-May-2019

Granted date: 6-October-2020

Inventor(s): Alfredo Medina Garcia, Pierrick Ausseresse

Abstract:

An apparatus comprises: a voltage converter, a first switch, a second switch, and a controller. The voltage converter includes a combination of a primary winding and an auxiliary primary winding magnetically coupled to a secondary winding. The auxiliary primary winding is operable to generate a feedback voltage signal. The secondary winding is operable to receive energy from the primary winding to produce an output voltage to power a load. The controller controls switching operation of the first switch and the second switch to control a flow of current through the primary winding. The controller is further operable to: i) via a feedback voltage signal from the auxiliary primary winding, monitor a flow of current through a body diode of the second switch, and ii) control subsequent activation of the first switch to an ON state based on the monitored flow of current through the body diode of the second switch.

9.1.4. US10892687B2: Asymmetric power converter, power converters, and operating power converters

File date: 26-September-2019

Granted date: 12-January-2021

Inventor(s): Alfredo Medina Garcia, Marc Fahlenkamp

Abstract:

Power converter controller, asymmetric power converter and method for operating a power converter. Power converter controllers, power converters and method are provided. In some configurations, first and second primary side switches of the power converter are controlled, in each switching cycle such that first a first switch is closed, then a second switch is closed and then again a first switch is closed.