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Compact Modeling Technology for the Simulation of Integrated Circuits Based on Graphene Field-Effect Transistors

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The progress made toward the definition of a modular compact modeling technology for graphene field-effect transistors (GFETs) that enables the electrical analysis of arbitrary GFET-based integrated circuits is reported. A set of primary models embracing the main physical principles defines the ideal GFET response under DC, transient (time domain), AC (frequency domain), and noise (frequency domain) analysis. Another set of secondary models accounts for the GFET non-idealities, such as extrinsic-, short-channel-, trapping/detrapping-, self-heating-, and non-quasi static-effects, which can have a significant impact under static and/or dynamic operation. At both device and circuit levels, significant consistency is demonstrated between the simulation output and experimental data for relevant operating conditions. Additionally, a perspective of the challenges during the scale up of the GFET modeling technology toward higher technology readiness levels while drawing a collaborative scenario among fabrication technology groups, modeling groups, and circuit designers, is provided.

1. Introduction

By combining graphene devices with interconnects and other components, innumerable circuits can be designed for analog and radio-frequency (RF) applications,[1] preferably in the form of an integrated circuit (IC). The graphene-based circuits could be integrated with the silicon CMOS IC to increase the IC functionality. A possible realization of a hybrid graphene–silicon IC could consist of a silicon platform that would implement digital circuits according to the CMOS process. In addition to the silicon platform, a graphene platform (e.g., based on graphene transistor technology) for making RF functions exploiting the unique properties of graphene could be fabricated, combining the best of two technologies in a single IC (**Figure 1**a).[2] The graphene platform could be monolithically integrated on a convenient substrate (Figure 1b) such as silicon carbide[3] or a flexible polymer[4] to exploit the functionality of graphene in specific applications.[5] Regardless of the choice between hybrid or monolithic, a compact modeling technology for the graphene platform is required to make predictions of the electrical behavior of arbitrary circuits for DC, transient (time domain), AC (frequency domain), and noise (frequency domain) analysis. Every type of analysis requires a tailored set of models that capture the physics involved in a consistent way with experimental measurements for the relevant device operating conditions, which form the basis for a technology computer aided design (TCAD). Moreover, the mathematical complexity of the models should be kept low because multiple devices could be involved in a simulation. A TCAD tool is required during manufacturing to make the circuit design-fabrication cycle more efficient.

In this study, we present the progress made toward the definition of a modular compact modeling technology for the graphene field-effect transistor (GFET), which is considered as the building block of the graphene platform in the IC. For a circuit simulation to be realistic, various non-idealities must be modeled at the device level. They include the effect caused by the parasitic network (parasitic resistances, capacitances, and inductances) associated to the contact pads and interconnections, as well as the effect of extrinsic resistances (contact and gate resistance), which significantly reduce the expected device performance. Additionally, the effect of the charges trapped/detrapped in the dielectric materials and interfaces must be included, which are related with the observed time-dependent drift of the operating bias point. In contrast, as short-channel length devices are needed to upscale the RF performance of graphene devices and circuits, short-channel effects (SCE) must be properly accounted by considering the 2D electrostatics and velocity saturation effect. It is also important to consider the

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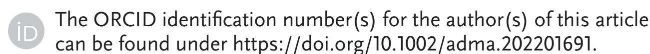
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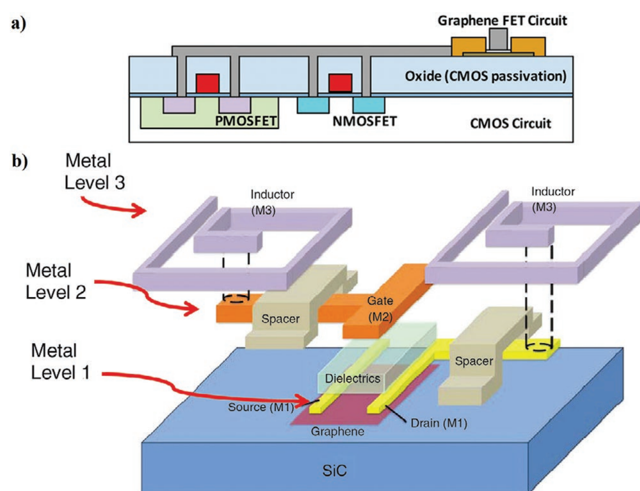

Figure 1. a) Schematic cross section of a hybrid IC combining silicon and graphene platforms, where the former implements the digital part of the mixed-signal circuit and the latter implements the RF part. Reproduced with permission.[2] Copyright 2016, ACS. b) A wafer-scale graphene circuit in which all circuit components, including GFET and inductors, are monolithically integrated on a single silicon carbide wafer. Reproduced with permission.[6] Copyright 2012, Elsevier.

self-heating effects (SHE) at high fields that might produce an important reduction of the drain current. In addition, if the excitation frequency is close or above the device intrinsic cutoff frequency, the effect of carrier inertia should be considered, which requires a non-quasi-static (NQS) model. For the noise, the relevant physics must be collected into an appropriate compact model to obtain the noise indicators at the circuit level. This requires an analysis of the different noise sources and their dependence on the substrate, dielectric environment, as well as contact technology. A deep understanding of the mechanisms of local noise propagation to terminal currents and voltages is necessary. At high-frequency (HF) range, a careful analysis of the coupling mechanisms between the channel and the gate(s) is required. These efforts are relevant because figures of merit are limited by noise.

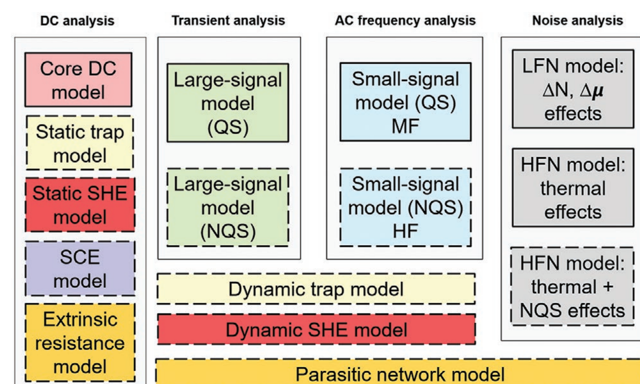

Figure 2. Modular compact modeling GFET technology presented in this study. The primary models describing the ideal device are represented by black solid lines, whereas the secondary models describing the device non-idealities are represented by black dashed lines. Acronyms used – SHE: self-heating effects, SCE: short-channel effects, QS: quasi-static, NQS: non-quasi-static, MF: medium frequency, HF: high frequency, LFN: low-frequency noise, HFN: high-frequency noise.

A set of models capturing the relevant physics is needed to deal with the different types of electrical analysis, which forms the basis for a compact modeling technology targeting the simulation of ICs based on GFETs. As shown in **Figure 2**, they can be categorized into primary models defining the ideal device response and secondary models accounting for non-ideal effects to provide the necessary refinement to perform realistic circuit simulations. An in-depth explanation of relevant model details and main results for each type of analysis will be given along the Sections of the manuscript, namely DC (Section 2), transient (Section 3), AC (Section 4), and noise analysis (Section 5). In addition, we have benchmarked each model with experimental results to demonstrate its predictive capability.

2. DC Analysis

Here, a model accounting for the DC behavior of GFETs is presented. Section 2.1 introduces the intrinsic GFET core DC model, which is based on the Poisson's equation coupled with a drift-diffusion current equation, the former describing the device electrostatics (Section 2.1.1) and the latter describing the electron transport along the graphene channel (Section 2.1.2). In Section 2.2, various non-ideal effects affecting the operation of a GFET are added to the intrinsic model; thus, their inclusion is proven to be necessary to get consistency with experimental results from real devices. Those encompass charges trapped in the dielectric materials and interfaces (Section 2.2.1), SHE (Section 2.2.2), and SCE (Section 2.2.3). Finally, some relevant analytical models for the contact resistance, which can be used toward extending the intrinsic model with the obtained values of this parameter, have been presented (Section 2.2.4).

2.1. Core DC Model

Here, we present the model for the electrostatics of a four-terminal GFET in Section 2.1.1, which sets the basis for the later formulation of a drain current model in Section 2.1.2.

2.1.1. Electrostatics of a Four-Terminal FET

Let us consider a general GFET as that depicted in **Figure 3**a. The graphene sheet under the electric control of the gate electrodes plays the role of the active channel. The electrostatic modulation of the carrier concentration in the 2D channel is achieved via a double-gate stack consisting of top- and back-gate dielectrics and corresponding metal gates (Figure 3b). The graphene sheet is contacted with both a drain and source terminal; carrier transport is produced between both terminals when a non-zero bias is applied. The direction of current transport defines the longitudinal direction (y). The transversal direction (x) goes from the top gate to the bottom gate, whereas the z-direction goes across the width of the device (W), where W is sufficiently large such that the transistor can be considered uniform along the z axis. The electrostatics of the GFET

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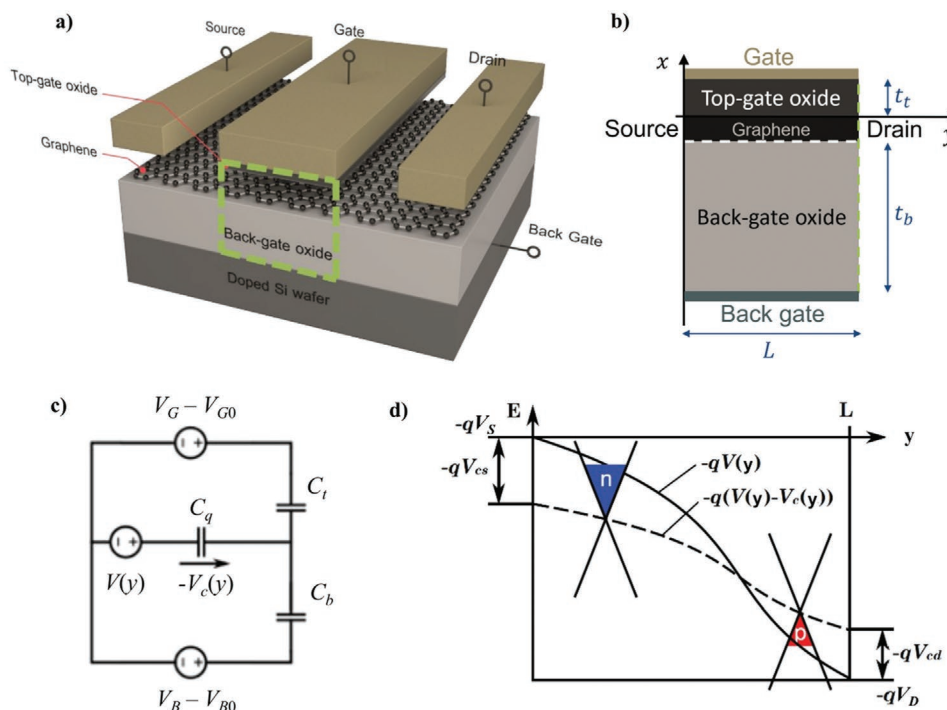

Figure 3. a) Schematic depiction of a four-terminal GFET. b) Cross section of the GFET and the domain where the Poisson's equation is evaluated to solve the electrostatics. This area corresponds to the dashed rectangle in (a). c) Equivalent capacitive circuit of the GFET. d) Schematic of the band diagram of the intrinsic device:[7,8] Energy, E, versus longitudinal position, y. The quasi-Fermi level $E_F = -qV(y)$ and the Dirac energy $E_D = -q\psi(y) = -q(V(y) - V_c(y))$ are shown. When the quasi-Fermi level is located at the Dirac energy, the dubbed Dirac point or charge neutrality point is reached. V_D and V_S are the drain and source biases, respectively; V_{cd} and V_{cs} are the channel potentials at the drain and source sides, respectively. Two Dirac cones illustrate the mixed n/p-type channel of this example. a) Reproduced with permission.[9] Copyright 2016, IOP. d) Reproduced with permission.[8] Copyright 2014, IEEE.

can be evaluated by applying the Poisson's equation across its structure

$$\nabla \cdot [\varepsilon(x,y)\nabla\psi(x,y,T)] = \rho_{\text{free}}(x,y,T) \tag{1}$$

where T is the temperature, ε is the permittivity, ψ is the electrostatic potential, and ρ_{free} is the free charge density. Considering a 1D approximation for the GFET electrostatics along a transversal cut, the following charge-balance equation, which can be represented by the equivalent capacitive circuit shown in Figure 3c, can be obtained:[10,11]

$$\begin{aligned} Q_{\text{net}}(y,T) = &-C_t(V_G - V_{G0} - V(y,T) + V_c(y,T)) \\ &- C_b(V_B - V_{B0} - V(y,T) + V_c(y,T)) \end{aligned} \tag{2}$$

where $Q_{\text{net}}(y,T) = q[p(y,T) - n(y,T)]$ is the net sheet charge density; q is the elementary charge; p and n are the hole and electron carrier densities, respectively. $C_t = \varepsilon_t/t_t$ ($C_b = \varepsilon_b/t_b$) is the top- (back-) oxide capacitance per unit area, with ε_t (ε_b) being the top (back) dielectric constant and t_t (t_b) the top- (back-) oxide thickness. The top (back) overdrive voltage is $V_G - V_{G0}$ ($V_B - V_{B0}$), where V_G (V_B) is the top- (back-) gate potential, and V_{G0} (V_{B0}) comprises the work-function difference between the top (back) gate and the graphene channel as well as the effect of additional fixed charge owing to impurities or doping. Because of the presence of non-negligible contact resistances in GFETs (Section 2.2.4), the intrinsic source and drain potentials (V_S and V_D at the active channel edges) cannot be shorted to reference in practice; therefore, we adopted a general formulation where none of the terminals are grounded. Thus, the GFET is driven by terminal voltages defined with respect to some arbitrary reference point. $V(y,T)$ is the quasi-Fermi level along the graphene channel, that is, the electrochemical potential, and it must fulfill the following boundary conditions: 1) $V(y = 0,T) = V_S$ and 2) $V(y = L,T) = V_D$ at the source and drain edge-sides, respectively, where L is the gate length. $V(y,T)$ is assumed to be the same for both electrons and holes because the generation/recombination times for carriers in graphene are very short (1-100 ps);[12–14] therefore, electron and hole quasi-Fermi levels do not deviate significantly from each other.[7] $V_c(y,T)$ represents the position-dependent chemical potential, that is, the shift of the Dirac potential ($\psi(y, T)$) with respect to the quasi-Fermi level. Figure 3d shows a scheme of the electrostatic, electrochemical, and chemical potentials along the channel at an arbitrary bias. Electron and hole concentrations can be calculated as a function of $V_c(y,T)$ using the following equations, which are a result of the density of states of graphene (deduced from its linear dispersion relation), where the electronic states are occupied according to the Fermi–Dirac statistics:

$$\begin{aligned} p(y,T) &= \frac{\Delta^2}{2\pi(\hbar v_F)^2} + \frac{2}{\pi}\left(\frac{k_B T}{\hbar v_F}\right)^2 \mathfrak{F}_1\left[\frac{qV_c(y,T)}{k_B T}\right] \\ n(y,T) &= \frac{\Delta^2}{2\pi(\hbar v_F)^2} + \frac{2}{\pi}\left(\frac{k_B T}{\hbar v_F}\right)^2 \mathfrak{F}_1\left[-\frac{qV_c(y,T)}{k_B T}\right] \end{aligned} \tag{3}$$

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where Δ is the amplitude of the electrostatic potential inhomogeneity that causes the electron–hole puddles;[15] $\mathfrak{F}_1$ is the Fermi–Dirac integral of first-order; k_B is the Boltzmann constant, $\hbar$ is the reduced Planck constant, and $v_F = \sqrt{3}a\gamma_0/2\hbar$ is the Fermi velocity; where a = 2.49 Å is the graphene lattice constant[16] and γ_0 = 3.16 eV is the interlayer coupling.[17] The term $\Delta^2/(2\pi(\hbar v_F)^2)$ accounts for the contribution of the puddles to the carrier concentration. The net sheet charge density and the quantum capacitance of graphene, which is defined as $C_q(y,T) = \partial Q_{net}/\partial V_c$, result in[8]

$$Q_{net}(y,T) = \frac{2q(k_BT)^2}{\pi(\hbar v_F)^2}\left\{\mathfrak{F}_1\left[\frac{qV_c(y,T)}{k_BT}\right] - \mathfrak{F}_1\left[-\frac{qV_c(y,T)}{k_BT}\right]\right\}$$
$$C_q(y,T) = \frac{2q^2k_BT}{\pi(\hbar v_F)^2}\ln\left[2\left(1+\cosh\left[\frac{qV_c(y,T)}{k_BT}\right]\right)\right] \tag{4}$$

$V_c(y,T)$ could be calculated as a function of the terminal biases (V_G, V_B, V_D, V_S) from Equations (2) and (4). However, this formulation is not convenient for a compact model compatible with circuit simulators. Using a square-root-based approximation for C_q,[18] it is possible to get an implicit expression for V_c that can be written in terms of elemental functions, which is more suitable for compact modeling purposes

$$C_q(y,T) \approx kc_1\sqrt{1+(V_c/c_1)^2}$$
$$Q_{net} = \int_0^{V_c} C_q(\tilde{V})d\tilde{V} = \frac{kc_1}{2}\left[V_c\sqrt{1+(V_c/c_1)^2} + c_1\text{asinh}(V_c/c_1)\right] \tag{5}$$

where $k = 2q^3/(\pi(\hbar v_F)^2)$ and $c_1 = (k_BT/q)\ln(4)$.

The chemical potentials at the source $V_{cs} = V_c(0,T)|_{V=V_S}$ and drain $V_{cd} = V_c(L,T)|_{V=V_D}$ side-edges are the relevant quantities required to calculate the drain current. They can be easily determined by implementing the Verilog-A algorithm reported in refs. [8, 19] which allows the circuit simulator to solve Equations (2) and (5), favoring a circuit-compatible model.

2.1.2. Drain Current Model

Here, we deal with the development of a compact model for the GFET drain current. For such purpose, we assumed that the drift-diffusion theory is applicable. That implies that the carrier mean free path (MFP) is significantly shorter than L. The MFP is related to the graphene quality and values below 100 nm have been reported at room temperature.[15] Electrons and holes in graphene tend to present mobilities in the same order of magnitude in both experiments and simulations.[20–22] Here, we assume an equal mobility for both types of carriers for simplicity, but the models could be easily extended for non-equal mobilities. The drain current of a GFET according to the drift-diffusion theory can then be evaluated as

$$I_{DS} = qW\rho_{sh}(y,T)\mu(y,T)\frac{\partial V(y,T)}{\partial y} \tag{6}$$

where $\rho_{sh}(y,T) = p(y,T) + n(y,T)$ is the transport carrier sheet density and $\mu(y,T)$ is the field-dependent carrier mobility that reads as[9]

$$\mu(y,T) = \frac{\mu_{LF}}{\sqrt[\beta]{1+\left(\frac{\mu_{LF}}{v_{sat}(y,T)}\left|\frac{\partial\psi(0,y,T)}{\partial y}\right|\right)^\beta}} \tag{7}$$

where β is a parameter of the model describing how sharp the transition between low- and high-field mobilities is and μ_{LF} refers to the low-field carrier mobility. Saturation velocity $v_{sat}(y,T)$ is limited by optical phonon scattering according to the following equation:[23,24]

$$v_{sat}(y,T) = \frac{2\Omega}{\pi\sqrt{\pi\rho_{sh}(y,T)}}\frac{1}{N_{OP}(T)+1}\sqrt{1-\frac{\Omega^2}{4\pi v_F^2\rho_{sh}(y,T)}}$$
$$N_{OP}(T) = \frac{1}{\exp\left(\frac{\hbar\Omega}{k_BT}\right)-1} \tag{8}$$

where $N_{OP}(T)$ and $\hbar\Omega$ are the optical phonon occupation and energy, respectively. Low-field mobility and saturation velocity strongly depend on the dielectric materials surrounding the graphene layer, namely on the substrate and top-gate insulator used for the specific GFET geometry. These parameters depend on various scattering mechanisms that drive the carrier transport.

To obtain an explicit expression for Equation (6) in terms of the chemical potential, V_c, the following simplifications are needed: 1) under the condition of identical electron and hole mobilities, $\rho_{sh}(y,T)$ is approximated to its second-order Taylor expansion[8,18]

$$\rho_{sh}(y,T) \approx \frac{\Delta^2}{\pi(\hbar v_F)^2} + \frac{\pi(k_BT)^2}{3(\hbar v_F)^2} + \frac{q^2V_c^2(y,T)}{\pi(\hbar v_F)^2} \tag{9}$$

2) A soft-saturation model (β = 1) is adopted. This value is consistent with numerical studies of electronic transport based on the Monte Carlo simulations;[25] 3) v_{sat} is assumed to be constant ($v_{sat,0}$), instead of using Equation (8). This is because the implementation of Equation (8) together with (2) has been found to produce some artifacts that can result in harmonic distortion when large-signal transient simulations are performed. Considering all the simplifications, the following closed-form drain current equation is achieved:

$$I_{DS} = \frac{W\mu_{LF}}{L_{eff}}\left\{\frac{k}{2}\left(\frac{kc_1V_c(c_1^2+2V_c+4c_2)\sqrt{1+(V_c/c_1)^2}}{8(C_t+C_b)} - \frac{kc_1^2(c_1^2-4c_2)\text{asinh}(V_c/c_1)}{8(C_t+C_b)} + \frac{V_c^3}{3} + c_2V_c\right)\right\}_{V_{cs}}^{V_{cd}} \tag{10}$$

where $c_2 = (\pi k_BT)^2/3q^2 + \Delta^2/q^2$. An effective electrical length, L_{eff}, incorporating velocity saturation effects can be defined as

$$L_{eff} = L + \frac{1}{C_t+C_b}\frac{\mu_{LF}}{v_{sat,0}}\{Q_{net}\}_{V_{cs}}^{V_{cd}} \tag{11}$$

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2.2. Non-Ideal Effects for Enhancing the Prediction Capability of the Core DC Model

To achieve high-yield technology generations as well as reproducible electrical device characteristics toward exploiting GFETs at a circuit level, the trap mechanisms taking place within the device should be understood. Traps are material- or energetic-dependent imperfections within the channel or its surroundings, for example, interfaces and oxide, able to capture and release carriers at different rates. Fast capture occurs within the channel and interfaces close to it, whereas the release of these trapped carriers is fast in the channel region and slow at the interfaces. In contrast, traps within the oxide region far from the channel have slow capture and emission time constants.[26] Graphene channels and their associated interfaces have been optimized toward a significant reduction of traps and defects in transistor architectures, for example, through passivation[27,28] and/or encapsulation techniques.[29,30] However, gate oxide has been a major issue in graphene transistors as well as in other emerging[26] and mature[31] FET technologies owing to scalability limitations;[26] thus, deep oxide (border) traps still affect the device performance.[32–35] High-κ insulators, such as HfO_2 and Al_2O_3, as well as layered 2D insulators, such as hexagonal boron nitride (hBN), have been used to fabricate high-performance GFETs.[36,37] Trap-related phenomena in the aforementioned bulk high-κ oxides have been observed and studied in silicon devices[38] as well as in emerging transistor technologies.[39] hBN has been suggested as the optimal dielectric for GFETs owing to the good lattice matching between the 2D channel and the 2D dielectric and minimized dangling bonds.[40–42] However, in addition to the low-κ of hBN ($\kappa \approx 3$–4),[40,43] which limits the equivalent oxide thickness scalability,[26] causing wafer-scale integration issues,[36] few works have reported on HF GFETs with hBN as the true gate oxide,[29,44,45] which exhibit poor HF performance, in stark contrast to GFETs with high-κ oxides.[46–52] Furthermore, in contrast to the demonstrated low density of interface traps in hBN/graphene interfaces,[29,41] the temperature- and field-dependent carrier capture and emission processes owing to border traps within this 2D dielectric in 2D FETs,[26] specifically in GFETs, are not yet understood despite the recent characterization efforts.[53–55] A correct description of trap-related effects and their impact on the static and dynamic performance of graphene transistors can reveal true features of a corresponding technology.[34,35,56–58] The impact of traps on the transfer device characteristics is described by the static trap model module presented in Section 2.2.1, whereas the dynamic aspects of traps are introduced in Section 3.3.1 to complete the discussion.

The upscaling of RF performance in GFETs can be achieved by the progressive reduction of the channel length. When analyzing a short-channel GFET, velocity saturation is an important factor, but 2D electrostatics should also be considered. The strong electric fields caused at high bias affect the charge distribution along the graphene channel; thus, the 2D electrostatics across the plane perpendicular to graphene must be analyzed. Therefore, we developed a model that solves the 2D Poisson's equation coupled with the drift-diffusion equation, which includes the velocity saturation effect, to consider SCE effectively. In contrast, power dissipation in the graphene channel imperfectly spread out of the device increases its temperature,[59–61] triggering SHE. Temperature strongly affects charge transport through carrier concentration and saturation velocity. SHE and SCE will be modeled in Sections 2.2.2 and 2.2.3, respectively.

Finally, in Section 2.2.4, we studied the bias-dependent contact resistance, which embraces the phenomena at the metal–graphene (MG) interface as well as the junction formed between the graphene layer under the metal electrode and the graphene channel.

2.2.1. Static Trap Model

The actual performance of GFETs can be revealed by a device model correctly describing the hysteresis in both trap-affected and trap-reduced scenarios. In the literature, graphene transistor models including trap-effects have been reported;[34,58] however, their use has been limited either to observe the impact of the traps on the transport properties within a specific trap-affected scenario (forward bias sweep)[34] or without considering drain-to-source voltage dependence of the traps.[58] Next, we describe our model[35] that overcomes the latter issues.

The density of trap centers in a high-κ device, including GFETs, is higher in the gated region because all types of traps are present, that is, material, interface, and border traps. Hence, the modeling approach reviewed next focuses on this specific device region. A high-κ oxide has been considered without loss of generality, that is, trapping mechanisms in 2D oxides are qualitatively similar to the ones in 3D oxides but differ in temperature and vertical field dependence. Trapping mechanisms in ungated regions can be implicitly included in scattering-related parameters.

Figure 4a shows a schematic cross-section of a top-gated graphene transistor with high-κ oxide where trap centers are pointed out (top), and a sketch of the conduction band at a given V_{GS} in the linear regime is also illustrated (bottom). At a hypothetical state of the traps not affecting the device performance, that is, a trap-free state, the traps under the gate are empty; thus, the field lines emitted from the gate contact affect the channel carriers directly (cf. Figure 4b). Notably, a trap-free state is not possible in real conditions. However, a reduced impact of the charged traps on the I–V characteristics, that is, minimum hysteresis window, can be obtained by controlling the measurement conditions with sophisticated characterization techniques, for example, pulsed measurements.[32,35,56] In this study, the latter scenario is considered as a trap-reduced device performance. In a more practical scenario, the traps within the oxide are filled up so that the electrical field lines from the gate end on the traps, causing the channel potential to be shielded from the gate (cf. Figure 4c) and impacting the transport conditions, that is, the operating bias point is shifted leading to a hysteretic device performance. Herein, the latter is named as a trap-affected performance.

To reproduce and understand the impact of traps on critical device figures of merit toward using the devices in circuits, a compact model describing the behavior of trap-affected and trap-reduced device performance accurately is required. The former characteristics can be obtained with a staircase characterization

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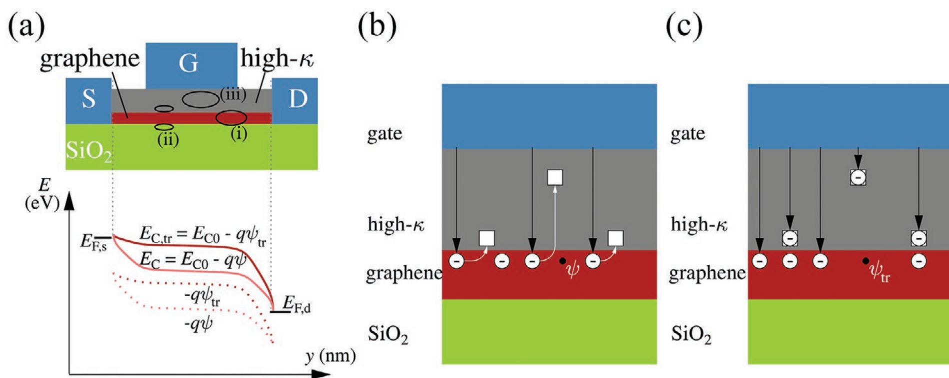

Figure 4. a) Top: schematic cross section of a GFET indicating (i) channel, (ii) interface, and (iii) deep oxide traps. Bottom: sketch of the conduction energy band and channel potential under trap-free (E_C,ψ) and trap-affected ($E_{C,tr}$,ψ_{tr}) conditions. b,c) Schematic representations of the gated device region showing traps (squares) and carriers (circles) under trap-free (b) and trap-affected (c) conditions.

whereas an opposing-pulse technique can be used for the latter as shown in ref. [35]. Forward (increasing extrinsic, $V_{GS,e}$) and backward (decreasing $V_{GS,e}$) sweeps are applied in both characterization approaches to show a hysteresis window in the transfer characteristics. An analytical I–V compact model based on Equations (2) and (6),[10] under the condition of one active gate, has been used to describe the experimental data of GFETs by considering the impact of traps on the net charge within the graphene channel. The electrostatic equation of a practical one-gate GFET yields a net charge, $Q_{net,tr}(y,T)$, description with the impact of traps given as[35]

$$Q_{net,tr}(y,T) = -C_t[V_G - V_{G0} - V(y,T) + V_c(y,T)] + qN_{tr} \tag{12}$$

where $N_{tr} = C_t(DV_{tr} - (K_{tr}V_{DS})/2)/q$ is the trap density with the trap-induced potential term $DV_{tr} - (K_{tr}V_{DS})/2$. DV_{tr} and K_{tr} are the phenomenological model parameters accounting for the shift of V_{Dirac} owing to traps impact and the V_{DS} dependence of this shift, respectively. The Dirac voltage, considering both the trap-reduced and trap-affected scenarios, is calculated by considering straightforward conditions such as $Q_{net,tr}(y,T) \rightarrow 0$ at the charge neutrality point (CNP) as well as an average channel potential over the channel, that is, $V(y,T) \approx V_{DS}/2$ at similar bias conditions, which yields[35]

$$V_{Dirac} \approx \begin{cases} V_{G0} + \dfrac{V_{DS}}{2}, & \text{trap-reduced} \\ V_{G0} - DV_{tr} + \dfrac{(K_{tr}+1)V_{DS}}{2}, & \text{trap-affected} \end{cases} \tag{13}$$

To reproduce the traps impact on the performance, the net charge expression in the model should account the corresponding scenario, that is, Equation (2) for the trap-reduced characteristics and Equation (12) for the trap-affected characteristics. Notably, the V_{DS}-dependence of a trap-affected Dirac voltage owing to hot-carriers[32,62] has been considered in this model,[35] which is an innovation with respect to other compact models including the impact of traps but neglecting such important effect.[58]

Both trap-affected and trap-reduced experimental transfer characteristics of a back-gated GFET technology with a gate width of 2 × 12 µm and a gate length of 300 nm (fabrication details in ref. [63]), obtained via staircase sweep and an opposing sweep characterization, respectively,[35] have been correctly described by the model in the p-type region, as shown in **Figure 5**a,b (model parameters are listed in Table II of ref. [35]). The hole dominant branch of the experimental data has been selected as the reference in the symmetric model, around V_{Dirac}, because better RF-related figures of merit are reported in this operation regime for this technology, in contrast to the n-type region.[35,64]

The model is valid for various V_{DS} values, from low to higher ones, at different trap-affected states (Figures 2 and

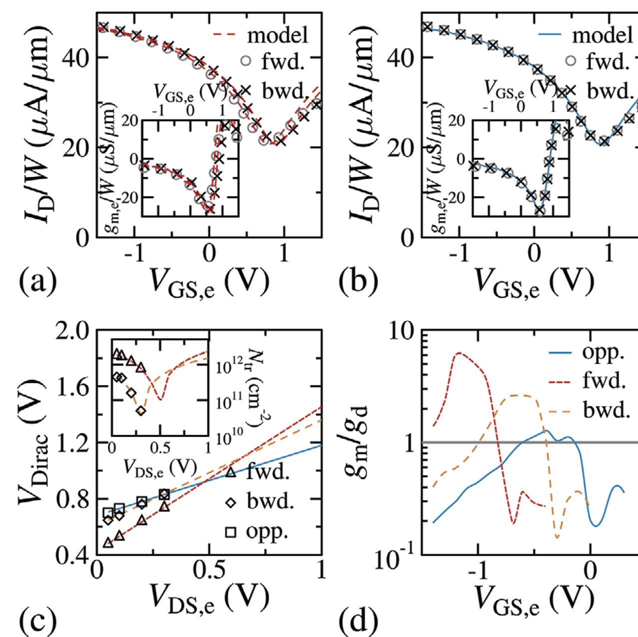

Figure 5. a,b) Experimental (markers) and modeling (lines) data of a 300 nm-long GFET: transfer characteristics with forward and backward sweeps showing trap-affected (a) and trap-reduced (b) behavior at V_{DS} = 0.3 V. Insets: transconductance plots at similar bias and conditions. c) V_{DS}-dependence of the Dirac voltage under different conditions. Inset: absolute value of the trap density for different V_{DS}. d) Intrinsic transistor gain at V_{DS} = −1 V. a–d) Adapted with permission.[35] Copyright 2020, IEEE.

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3 in ref. [35]), as indicated by the correct V_{DS}-dependence of V_{Dirac} observed in Figure 5c. The lower slope of the trap-reduced V_{Dirac} versus V_{DS} plot (≈1/2) with respect to the one obtained for the trap-affected data (≈(K_{tr} + 1)/2) suggests a trap-induced overestimation of V_{Dirac} at high fields, in contrast to a reproducible performance with the traps impact highly suppressed, that is, trap-reduced data. This is a crucial insight to be considered for the GFET performance in circuit applications.

Additionally, the trap density of the studied device is obtained for the different measurement sweeps from experimental data (see ref. [35] for the procedure) and the model parameters. The model can describe the V_{DS} dependence of N_{tr}, as shown in the inset of Figure 5c. Trapping and detrapping mechanisms can be elucidated from the curves for voltages lower and higher than the minimum point, respectively, which corresponds to a change of polarity of the trap-induced potential term. For instance, as indicated by the model curve, trapping processes are active for the forward staircase sweep at 0.3 V < V_{DS} < 0.5 V, whereas traps are enabled by the release of previous trapped carriers for the backward sweep case at the same bias range, as suggested by the increase of N_{tr} for the model curve. A correct description of N_{tr} at different biases, such as the one obtained with this model, enables the obtaining of improved insights in the device physics, for example, on low-frequency noise (LFN) characterization of GFETs.[64]

The intrinsic gain, $A_{v,i} = g_m/g_{ds}$, calculated from both the intrinsic transconductance ($g_m = \partial I_{DS}/\partial V_G$) and output conductance ($g_{ds} = \partial I_{DS}/\partial V_D$), has been shown with the model calibrated with trap-affected and trap-reduced data (cf. Figure 5d) of the device under study.[35] The result indicates higher $A_{v,i}$ and different V_{GS} dependence of this parameter for the trap-affected data than in the trap-reduced scenario. This is attributed to the trap-induced shielding of the channel potential because the changes of the current with respect to the different applied voltages, that is, g_m and g_{ds}, are affected differently depending on the traps state (measurement history). In addition to the experimental observations at different scenarios,[35] this model has shown the largely overlooked impact of traps on the performance of the graphene transistor. The approach used here enables a correct description of reproducible (trap-reduced) characteristics at room temperature toward exploiting such features in GFET-based circuit applications.

2.2.2. Static Self-Heating Model

Source-to-drain current within the graphene channel generates energy by the Joule effect, which can increase the temperature of the device considerably if the heat is not properly dissipated. The increase in graphene temperature, T, with respect to the ambient temperature, T_A, can be expressed as

$$T - T_A = \Re_{th} P_{dis} \tag{14}$$

where $P_{dis} = |I_{DS} V_{DS}|$ corresponds to the power dissipated in the graphene channel and $\Re_{th}$ is the effective thermal resistance, which embraces all the paths through which the heat can be dissipated out of the channel. $\Re_{th}$ can be estimated according to the methodology proposed in refs. [23, 65]. The method considers the combined effect produced by the graphene/dielectric interface, dielectric layer, and substrate thermal conductance. The thermal conductance contributed by the contacts is neglected.

To demonstrate the impact of SHE, we simulated the device described in ref. [51] assuming a high thermal resistance of 3×10^4 K W^{-1}. **Figure 6**a shows the temperature distribution as a function of the bias. Temperatures can reach high values at

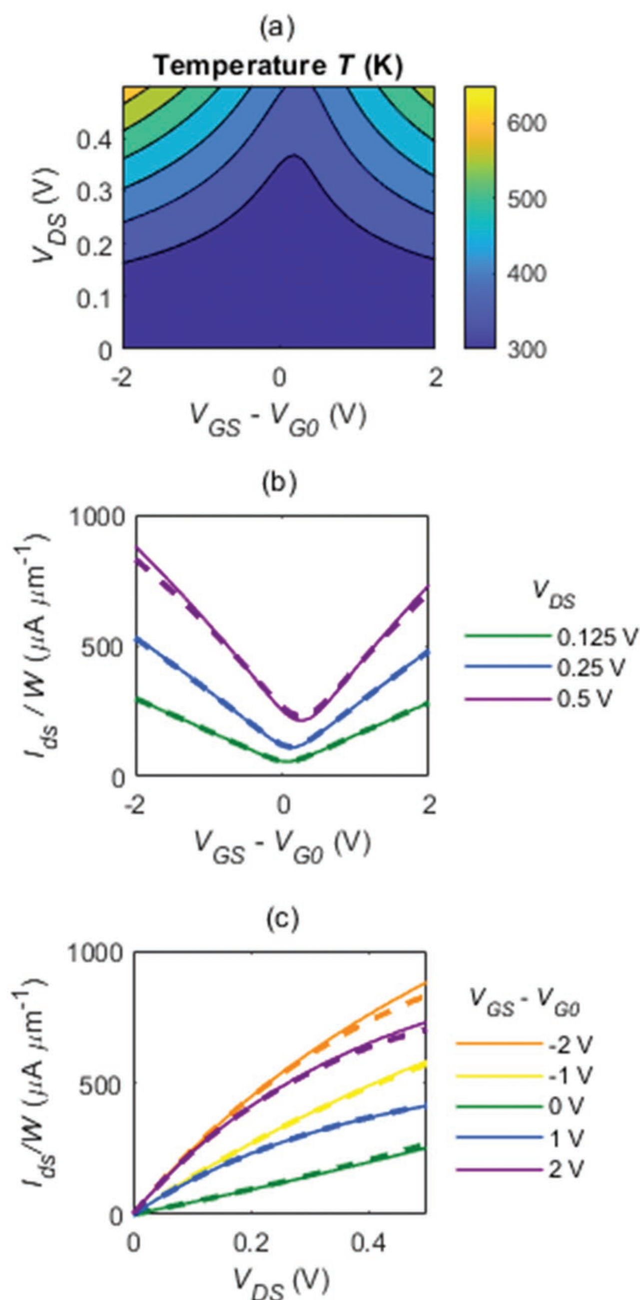

Figure 6. a) Temperature distribution as a function of the intrinsic bias voltage for a self-heated GFET. b) Transfer characteristics and c) output characteristics of a GFET at 300 K non-affected by SHE (solid) and affected by SHE (dashed).

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large supply biases, in the order of the temperatures estimated for similar GFETs.[66] Moreover, experimental observations show that self-heating can increase the temperatures of graphene significantly when thermal resistances are large (e.g., with thin insulators).[67] The transfer and output characteristics either neglecting SHE (solid lines) or considering SHE (dashed lines) are presented in Figure 6b,c. From the figure, it can be observed that temperature affects the drain current in different ways. The drain current increases in polarizations near V_{Dirac}, whereas it decreases for large gate voltages. Near V_{Dirac}, the increase in drain current is caused by a higher thermal carrier concentration. However, the temperature reduces carrier mobility and saturation velocity, whose effect dominates for biases far from V_{Dirac}. Moreover, current tends to saturate because of self-heating.[24] Despite the current saturation, Section 3.3.2 shows that the performance of the SHE-affected device observed in DC does not imply an improvement in the RF figures of merit, as the actual AC small-signal output conductance is larger than the one observed at DC.

2.2.3. Short-Channel Model

To study the performance of short-channel GFET, we developed a numerical model that aims to find the self-consistent solution of the 2D Poisson's equation (Equation (1)) in the domain represented in Figure 3a and the current continuity equation (Equation (6)). In addition to velocity saturation, this model accounts for the 2D electrostatics to consider SCE. Because Equation (6) assumes a drift-diffusion scheme, the short-channel model is valid when the GFET operates in this transport regime. Hence, the model cannot be applied to the pure ballistic regime.[68] This implies that the considered channel lengths should be significantly greater than the MFP of carriers in graphene, which is in the 10–100 nm range.[15,69,70]

We thoroughly studied SCE for the reference device reported in ref. [51] by varying the channel length. **Figure 7** compares the compact model of Section 2.1 (solid lines) with the self-consistent model, which considers 2D electrostatics (symbols). The figure shows the chemical potential and *I–V* curves for

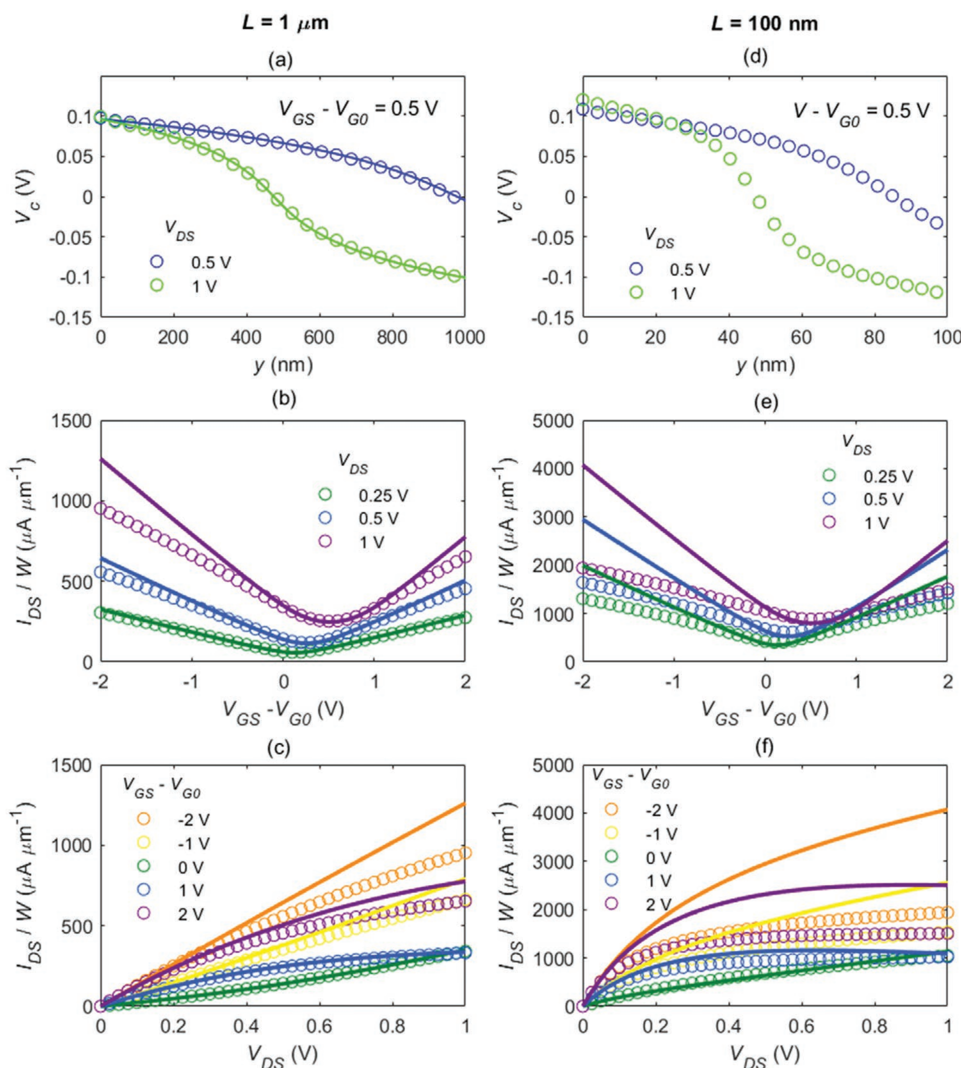

Figure 7. a–f) Comparison between the compact model (solid lines) and the numerical model that accounts for SCE (circles) for a 1 µm-long channel GFET (a–c) and a 100 nm-long channel GFET (d–f). a,d) Chemical potential along the channel. b,e) Transfer characteristics. c,f) Output characteristics.

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the cases of channel lengths of 1 μm, where both models give similar results, and 100 nm where models clearly diverge. The results of the short-channel device indicate that SCE imply a redistribution of carriers caused by 2D electrostatic effects:[9] carrier concentration close to source and drain edges increases as compared with the long device, as can be observed in the chemical potential distribution along the channel shown in Figure 7a,d. Additionally, the chemical potential slope becomes steeper, and the CNP (defined by the condition $V_c = 0$) is slightly displaced toward the middle of the channel.[9]

Figure 7 also shows the differences between the compact model and the self-consistent model in predicting the transfer (Figure 7b,e) and output curves (Figure 7c,f). As for the 1 μm-long GFET, the differences between both models mainly come from the velocity saturation effect, where $v_{sat,0}$ is kept constant in the compact model whereas it follows the more complex model described by Equation (8) in the self-consistent model. However, the predicted trends are analogous. In contrast, the predictions of both methods differ considerably for the 100 nm-long GFET. For this case, a significant degradation in the transconductance can be observed, which has a direct impact on the RF performance scaling.

2.2.4. Metal–Graphene Contact Resistance

Although GFET has emerged as a promising device for analog/RF applications, the contact resistance (R_c) embracing the phenomena arising at the interface between graphene and source/drain metal electrodes remains a major limiting factor that affects the electronic transport properties.[71–80] For RF electronic applications, it is a relevant issue with a strong impact on figures of merit such as the maximum frequency of oscillation (f_{max}), intrinsic cut-off frequency (f_T), and $A_{v,i}$.[9,81,82] Despite the considerable number of experimental and theoretical studies, the origin of R_c is still unclear owing to the multiple intrinsic and extrinsic factors affecting it, namely the nature of metals (chemisorbed or physisorbed), geometry of the contact (planar or edge), number of graphene layers, as well as impact of the fabrication process and bias. Therefore, a broad range of experimental values of R_c have been reported in the literature even though the same contact metal has been considered.[83–93] In a metal–semiconductor junction (Schottky contact), a potential barrier (Schottky barrier) is formed at the interface. In an ideal case, the Schottky barrier height is given by the difference between the metal work function and the semiconductor electron affinity (Schottky–Mott approach). For conventional (3D) semiconductors, a Schottky contact can be turned into an Ohmic contact by lowering the Schottky barrier height with opportune metal choice or lowering the barrier thickness sufficiently, in the order of few nanometers, by heavily doping the semiconductor. Therefore, electrons can go through the barrier driven by the quantum tunneling effect. However, for MG junction, the difference between the dimensional nature of the metal (3D) and graphene (2D) as well as the strong influence of the contact metal and the impact of the device fabrication details on the graphene properties hinder its description by the conventional Schottky–Mott picture. Furthermore, graphene zero energy bandgap prevents the formation of conventional Schottky contact and its small density of states near the Dirac point strongly limits the current injection from the metal.[94]

When a finite metal electrode is deposited to cover part of a graphene sheet as in the GFET contact shown in **Figure 8**a, the following electrostatic effects appear: 1) there is a charge transfer through the interface producing a doping of the graphene underneath, which is characterized by a significant shift ΔE_m of the graphene Fermi level with respect to its Dirac point. This is owing to the small density of states near the Dirac energy. Not only the difference between metal and graphene work functions should be considered in the process, but also the type of chemical interaction at the surface, namely physisorption or chemisorption.[96,97] 2) A potential step is established between graphene under the metal and the graphene channel,[98,99] which is produced by a charge transfer between the two graphene regions. As shown in Figure 8a, the potential step is characterized by an effective length, λ, and energy shifts ΔE_m and ΔE_g in the graphene under the metal and graphene channel, respectively. In the limit where the contact length is larger than the transfer length, L_T, which is defined as the effective contact length contributing to the injection of carriers in graphene, there is a current crowding effect indicative of

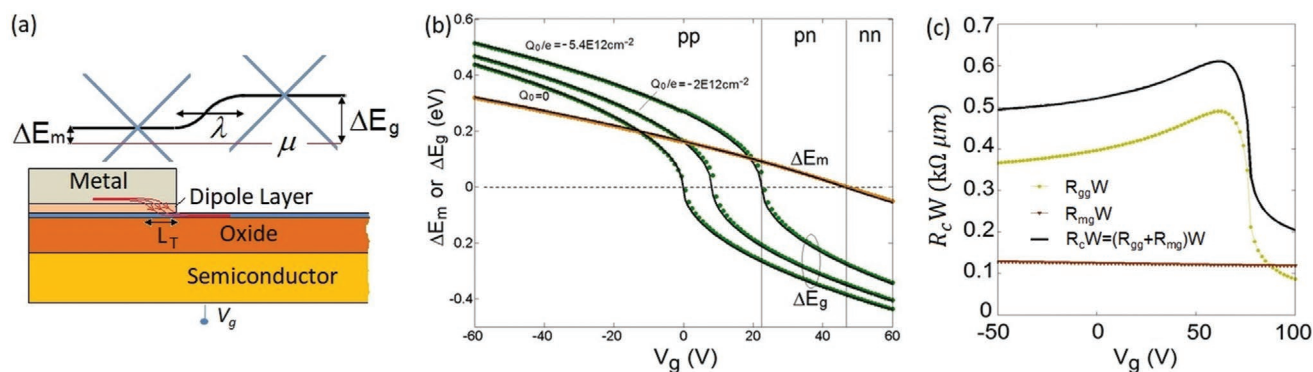

Figure 8. a) Sketch of the MG contact on a back-gate structure and the corresponding potential step formed between graphene under the metal and graphene in the channel. The red lines denote the current crowding effects near the contact edge. b) Graphene Fermi level shifts with respect to the Dirac point for different values of doping (Q_0/q), with palladium as a metal contact. c) Predicted R_c and its components, R_{mg} and R_{gg}, considering titanium as a metal. a–c) Reproduced with permission.[95] Copyright 2015, IOP Publishing.

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an R_c dependence on the contact width instead of the contact area.[100,101] Evidence of the current crowding has been reported by photocurrent spectroscopy experiment for graphene–gold contact.[102]

Apart from the abovementioned electrostatics, several theoretical studies have been conducted to understand both intrinsic and extrinsic factors in controlling the values of R_c in graphene-based devices. We can classify the theoretical studies as: 1) ab initio calculations[87,91,103–109] and 2) analytical models.[78,95,96,101] The ab initio calculations have helped to comprehend the nature of the MG interface at the microscopic level and to suggest ways to engineer contact resistance. For example, they have been useful to explain the spread of R_c measurements as due to uncontrolled graphene doping and/or the chemistry of the interface. However, these types of models have an extremely high computational cost. In contrast, for the analytical models, as proposed in ref. [101] the transport in the MG junction is described as carrier injection from metal to graphene underneath with probability $\mathcal{T}_{mg}$ followed by injection to the graphene channel with probability $\mathcal{T}_{gg}$. The conductance of MG contact is expressed in terms of the conduction modes in graphene and the transmission probabilities following the Landauer approach. However, in this model, the mechanism of $\mathcal{T}_{mg}$ is ambiguous and it does not consider the 3D and 2D nature of the metal electrode and graphene sheet, respectively. To solve this issue, a theoretical model of carrier transport considering the dimensional nature has been developed in ref. [95]. The physical model is based on the Bardeen transfer Hamiltonian (BTH) method for the calculation of the resistance, R_{mg}, between the metal and graphene underneath and on the Landauer approach to calculate the resistance, R_{gg}, arising at the potential step across the junction formed between the graphene under the metal and the graphene channel. The total contact resistance can be calculated as $R_c = R_{mg} + R_{gg}$. Here, the gate voltage dependence of ΔE_m and ΔE_g, in a standard back-gate GFET configuration, is conveniently solved using a 1D model, as illustrated in Figure 8b, where palladium was assumed as the metal electrode. These two quantities are key factors to determine R_c as a function of the gate voltage. Different types of junctions could be developed depending on the back-gate bias, namely pp-type, pn-type, and nn-type junctions. By assuming a chemical doping of the graphene channel $Q_0/q = -5.4 \times 10^{12}$ cm^{-2}, the transitions from pp- to pn-type at $V_G \approx 23$ V and from pn- to nn-type at $V_G \approx 46$ V were captured in accordance with reported measurements.[101] Moreover, by combining the BTH method for calculating the specific contact resistivity,[96] ρ_c, with the transmission line model,[110] the simple analytical expression

$$R_{mg}(\Delta E_m) = \frac{\sqrt{\rho_c R_{sh}^{m}}\coth\left(\frac{L_c}{L_T}\right)}{W_c} \tag{15}$$

is found; thus, its gate voltage dependence for arbitrary metals is predicted. Here, R_{sh}^{m} is the sheet resistance of graphene under the metal; L_c and W_c are the contact dimensions. Additionally, R_{gg} strictly depends on the effective length, λ, of the potential step that builds up between the graphene under the metal and the graphene channel, which can be calculated as

$$R_{gg}^{-1}(\Delta E_m, \Delta E_g) = 2e^2 W_c (h\pi)^{-1} \int_{-k_F}^{k_F} \mathcal{T}_{gg} dk_y \tag{16}$$

where $k_F = \min(|\Delta E_m|, |\Delta E_g|)/\hbar v_F$ and $\mathcal{T}_{gg}$ is the transmission probability of Dirac fermions across the potential step given by Cayssol et al.[98] According to this model, depending on the metal electrode and a possible chemical doping of the graphene channel, the two components of R_c could be either similar in magnitude or of very different orders. It has been established that R_{gg} is the dominant component for nickel and titanium electrodes, whereas there is a competition between both components for palladium. For illustrative purposes, the breakdown of R_c in its two components for a titanium-contacted GFET is reproduced in Figure 8c.

Recently, a physical model of R_c in titanium-contacted graphene-based FETs[78] has been developed considering an interfacial layer including oxidized Ti and polymethyl methacrylate residues at the Ti–G interface from the processing conditions of the contact. The study indicates that R_c is highly dependent on the properties of the interfacial layer. Similar to ref. [101] R_c is calculated as

$$R_c^{-1} \propto \int_{-\infty}^{\infty} dE_1 G(qE_1 - \Delta E_m, t_1) \int_{-\infty}^{\infty} dE_2 G(qE_2 - \Delta E_g, t_2) \int_{-k_F}^{k_F} dk_y \mathcal{T}_{total} \tag{17}$$

where

$$\mathcal{T}_{total} = \mathcal{T}_{mg}\mathcal{T}_{gg} / [1 - (1 - \mathcal{T}_{mg})(1 - \mathcal{T}_{gg})] \tag{18}$$

is the total carrier transmission probability and the Gaussian functions $G(E, t)$ with effectives broadening t_1 and t_2 have been considered to get a more realistic model. Parameter t_1 considers the coupling between the metal and the quasi-bound graphene states underneath; t_2 is a parameter embedding information of the random disorder potential in the graphene channel, which depends on the minimum sheet carrier concentration.

The probability of carrier transmission through the potential is given in ref. [98]. The carrier transmission, $\mathcal{T}_{mg}$, through Ti–TiO_x–graphene interface depends on the tunneling mechanisms and it has been modeled based on quantum-mechanical tunneling theory using the WKB approximation.

The above comprehensive physics-based calculation of R_c can be used as a confident reference for the values of this parameter in a device model. For compact modeling approaches, however, R_c in GFETs has been either extracted from experimental data-based methodologies[75–77,79] (cf. Section 4.2.3) or been considered as a model parameter whose value is obtained by fitting the experimental *I–V* curves (cf. Section 3.2). Furthermore, parameter extraction techniques based on test-structures or analysis of transport experimental data[81,89,111,112] have been developed toward obtaining an immediate R_c value. Further details of these extraction methodologies are provided in Section 4.2.3.

3. Transient Analysis

When a time-varying signal is applied to a GFET terminal, the dynamic operation of the device is strongly influenced by

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internal capacitive effects. Therefore, it is necessary to develop a large-signal model of intrinsic GFET capacitances. Various capacitive models for general FETs have been developed over the years. Basically, they can be categorized into two groups: 1) Meyer-like[113] and 2) charge-based capacitance models. The advantages and shortcomings of both model groups applied to conventional FETs have been widely discussed and implemented in circuit simulators.[114,115]

Meyer-like models are widely used in incumbent technologies because of their simplicity and fast computation. They assume that the intrinsic capacitances are reciprocal (i.e., $C_{ij} = C_{ji}$). Notably, this hypothesis might give unphysical results when dealing with some class of circuits (such as switched capacitor filters); furthermore, earlier models based on this assumption could not ensure charge conservation.[116,117]

Conversely, the charge-based models ensure both charge conservation and non-reciprocity of intrinsic capacitances in a FET. Owing to some corrections assembled by Ward and Dutton,[118] the charge-conservation issue was solved by introducing a capacitive matrix, which adds a bit of complexity. In refs. [11, 119–121] we have provided graphs of bias-dependent C_{dg} and C_{gd} for graphene- and MoS_2-based FETs, showing that the reciprocity of capacitances in emergent 2D technologies cannot be assumed for all transistor operation regimes. However, most of the GFET capacitance models reported so far rely on the Meyer's reciprocity assumption without evaluating the implications of adopting it.[122–126] Therefore, a comparison of the RF performance prediction between the Meyer-like models against a charge-based approach is provided in ref. [119] indicating that significant errors could arise.

Considering all the aforementioned, we presented a large-signal model for the GFET elsewhere and summarized it in Section 3.1.[11,127] Thereafter, to illustrate the working of the model, we have presented the dynamic response of several circuits exploiting the graphene ambipolarity in Section 3.2. Later in Section 3.3, we considered significant non-ideal effects that must be modeled to enhance the predictive capability of the large-signal model. The effects include the impact of the trapped charges in Section 3.3.1 and the NQS effects owing to carrier inertia in Section 3.3.2. Dynamic SHE will be treated in the context of small-signal analysis later in Section 4.2.2. As for the large-signal case, dynamic SHE would need some adaptation, which is not yet investigated. Finally, to account for the impact of parasitic elements when a transient circuit analysis is performed, a parasitic network model of the GFET should be considered in the simulation. That will be discussed in the context of AC analysis in Section 4.2.3.

3.1. Large-Signal Model

Assuming a quasi-static (QS) operation, the entering terminal currents in the time domain can be expressed by considering that the charges per unit area at any time controlled by the time-varying terminal voltages, ($v_G(t)$, $v_B(t)$, $v_D(t)$, and $v_S(t)$), are identical to those found if DC voltages (V_G, V_B, V_D, and V_S) were used.

$$i_m(t) = \frac{dQ_m}{dt} + I_m \tag{19}$$

where m stands for G, D, S, and B which denote the top gate, drain, source, and back gate, respectively. The possible leakage current through the top and back insulators is neglected, that is, $I_G = I_B = 0$. In addition, to guarantee charge conservation, $I_D = -I_S = I_{DS}$, where I_{DS} is calculated according to Equation (10). A four-terminal FET can be modeled using a set of 16 intrinsic capacitances, including 4 self-capacitances and 12 transcapacitances. The capacitance matrix is formed by these capacitances, where each element, C_{ij}, describes the dependence of the charge at terminal i with respect to a varying voltage applied to terminal j, assuming that the voltage at any other terminal remains constant. Therefore, Equation (19) can be written as

$$\begin{bmatrix} i_G \\ i_D \\ i_S \\ i_B \end{bmatrix} = \begin{bmatrix} C_{gg} & -C_{gd} & -C_{gs} & -C_{gb} \\ -C_{dg} & C_{dd} & -C_{ds} & -C_{db} \\ -C_{sg} & -C_{sd} & C_{ss} & -C_{sb} \\ -C_{bg} & -C_{bd} & -C_{bs} & C_{bb} \end{bmatrix} \begin{bmatrix} dv_G/dt \\ dv_D/dt \\ dv_S/dt \\ dv_B/dt \end{bmatrix} + \begin{bmatrix} 0 \\ I_{DS} \\ -I_{DS} \\ 0 \end{bmatrix} \tag{20}$$

$$C_{ij} = -\frac{\partial Q_i}{\partial V_j},\ i \neq j;\ C_{ij} = \frac{\partial Q_i}{\partial V_j},\ i = j. \qquad i, j = \text{G, D, S, B}$$

Each row must sum to zero for the matrix to be reference-independent, and each column must sum to zero for the device description to be charge-conservative.[128] Notably, only 9 out of the 16 intrinsic capacitances are independent. In addition, we can take advantage of the relations between top- and back-gate capacitances,[11,129] namely $C_{bd} = C_{gd}\ (C_b/C_t)$; $C_{bs} = C_{gs}\ (C_b/C_t)$; $C_{db} = C_{dg}\ (C_b/C_t)$; $C_{sb} = C_{sg}\ (C_b/C_t)$; $C_{gg} = -C_{bg}(C_t/C_b) + C_tWL$; $C_{bg} = C_{gb} = -C_{bb}(C_t/C_b) + C_tWL$; reducing the independent set of intrinsic capacitances of a four-terminal GFET to only four; for instance, C_{gs}, C_{gd}, C_{dg}, and C_{sd}.

Considering all the aforementioned, the modeling of the dynamic response of a GFET requires a charge model relating the terminal charges to the terminal voltages. From the electrostatics given in Equation (2), the following relations are derived:[11]

$$Q_G + Q_B = -W\int_0^L Q_{net}(y)dy; \begin{cases} Q_G = Q_0 - \dfrac{C_tW}{C_t + C_b}\displaystyle\int_0^L Q_{net}(y)dy \\ -Q_B = Q_0 + \dfrac{C_bW}{C_t + C_b}\displaystyle\int_0^L Q_{net}(y)dy \end{cases} \tag{21}$$

where $Q_0 = WLC_tC_b(V_G - V_{G0} - V_B + V_{B0})/(C_t + C_b)$. The charge controlled by the drain and source terminals is calculated based on the Ward–Dutton linear charge partition scheme, which guarantees charge conservation[118]

$$\begin{aligned} Q_D &= W\int_0^L \frac{y}{L} Q_{net}(y)dy \\ Q_S &= -(Q_G + Q_B + Q_D) = W\int_0^L (1 - \frac{y}{L}) Q_{net}(y)dy \end{aligned} \tag{22}$$

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Both terminal charges and intrinsic capacitances can conveniently be written using V_c as the integration variable, as it was done to model I_{DS} (cf. Section 2.1.2). Because I_{DS} is the same at any point y in the channel (by considering compensated generation/recombination processes), the equations required to evaluate the terminal charges and intrinsic capacitances are obtained from the drift-diffusion transport model as follows:

$$dy = \frac{\mu_{LF} W}{I_{DS}} \rho_{sh}(V_c) \frac{dV}{dV_c} dV_c - \frac{\mu_{LF}}{v_{sat}} \frac{d\psi}{dV_c} |dV_c|$$
$$y = \frac{\mu_{LF} W}{I_{DS}} \left(\int_{V_{cs}}^{V_c} \rho_{sh}(V_c) \frac{dV}{dV_c} dV_c \right) - \frac{\mu_{LF}}{v_{sat}} \left| \int_{V_{cs}}^{V_c} \frac{d\psi}{dV_c} dV_c \right| \tag{23}$$

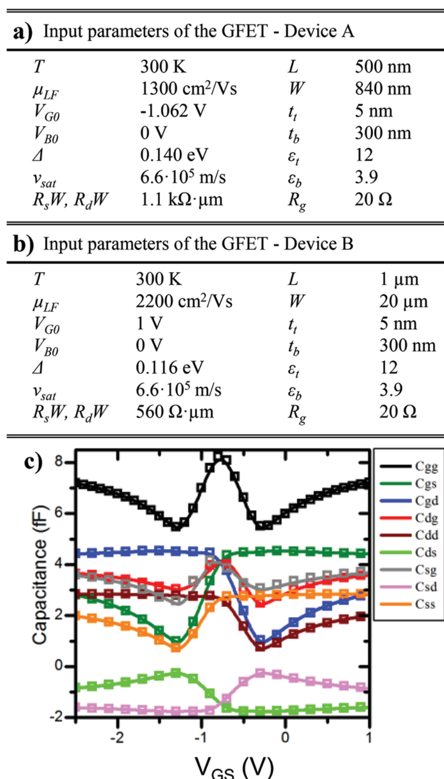
where $\frac{dV}{dV_c} = 1 + \frac{d\psi}{dV_c} = 1 + \frac{C_q(V_c)}{C_t + C_b}$

The drain current model presented in Section 2.1.2 is combined with the charge-based compact intrinsic capacitance description as shown in Equation (20) to assemble a large-signal model of GFETs. The modeling approach presented here has been validated against numerical simulations (**Figure 9**c)[11] as well as with experimental data from fabricated GFETs.[127]

3.2. Dynamic Response of GFET-Based RF Applications

To demonstrate the predictive capabilities of the large-signal model presented,[127] we consider various exemplary circuits, namely: the frequency doubler and the subharmonic mixer.[130,131] The GFET used in each of the circuits is referred as device A and B (with their corresponding parameters given in Figure 9a,b), respectively. In Figure 9c, a set of independent intrinsic capacitances for the device A is plotted as a function of the gate voltage, showing a clear non-linear behavior of the GFET around the Dirac voltage. It can be observed that the Meyer's reciprocity does not hold.[11]

A graphene-based frequency doubler leverages the quadratic-like transfer characteristic (I_{DS} vs $V_{GS,e}$ curve) of a GFET. If such a transfer characteristic is not perfectly parabolic and/or symmetric, which is the practical case, the output voltage contains the doubled frequency and other higher-order harmonics, resulting in harmonic distortion. As for device A configured in the topology depicted in Figure 9d, with the nearly symmetric transfer characteristic around V_{Dirac} = –1.15 V shown in



a) Input parameters of the GFET - Device A

T	300 K	L	500 nm
μ_{LF}	1300 cm²/Vs	W	840 nm
V_{G0}	-1.062 V	t_t	5 nm
V_{B0}	0 V	t_b	300 nm
Δ	0.140 eV	ε_t	12
v_{sat}	6.6·10⁵ m/s	ε_b	3.9
R_sW, R_dW	1.1 kΩ·µm	R_g	20 Ω

b) Input parameters of the GFET - Device B

T	300 K	L	1 µm
μ_{LF}	2200 cm²/Vs	W	20 µm
V_{G0}	1 V	t_t	5 nm
V_{B0}	0 V	t_b	300 nm
Δ	0.116 eV	ε_t	12
v_{sat}	6.6·10⁵ m/s	ε_b	3.9
R_sW, R_dW	560 Ω·µm	R_g	20 Ω

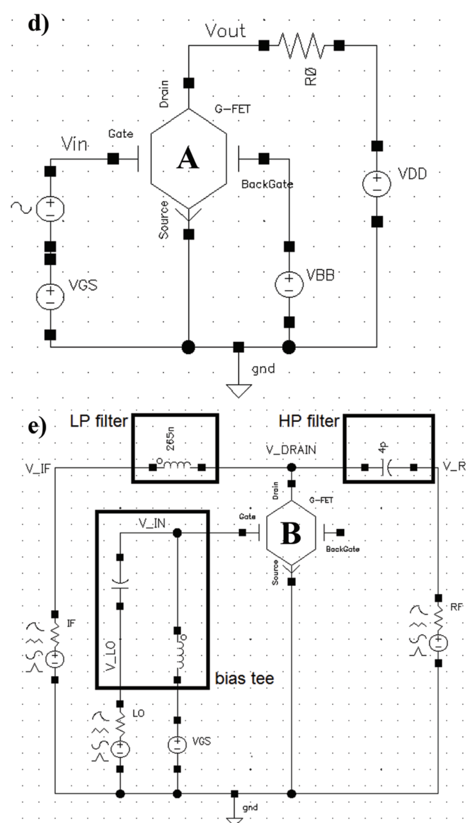


Figure 9. a,b) Input parameters used to describe the GFETs reported by Wang et al.[130] (Device A) (a) and Habibpour et al.[131] (Device B) (b). Contact resistances, R_d and R_s, have been considered bias-independent. R_g is the gate resistance. c) Compact model (solid lines) and numerical (symbols) calculation of the intrinsic capacitances versus V_{GS} for Device A at V_{DS} = 1 V. d) Schematic circuit of a GFET-based frequency doubler based on Device A.[130] e) Schematic circuit of a subharmonic resistive GFET mixer based on Device B.[131] A bias tee is used for setting the DC bias point. The characteristic impedance is 50 Ω. c) Reproduced with permission.[11] Copyright 2016, IEEE. d,e) Reproduced with permission.[127] Copyright 2016, IEEE.

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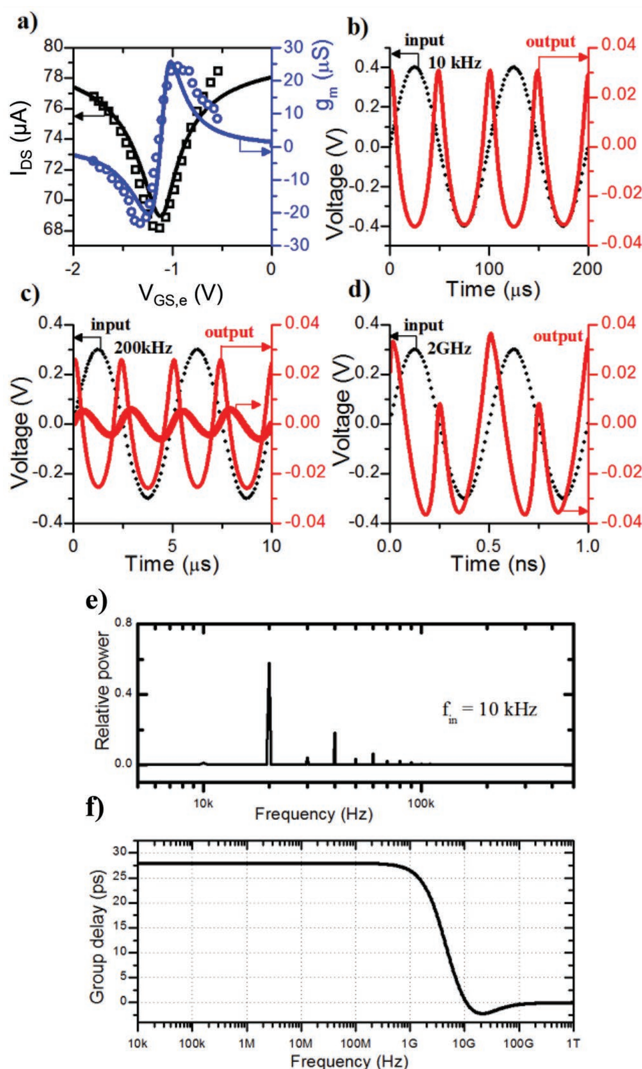

Figure 10. a) Experimental measurements (symbols) and simulations (solid lines) of the DC transfer characteristics and the extrinsic transconductance of a GFET-based frequency doubler.[130] The device is biased at $V_{DS,e} = 1$ V, $V_{BS,e} = 40$ V, and $V_{GS,e} = -1.15$ V. b) Input and output waveforms considering an input frequency of $f_{in} = 10$ kHz and amplitude $A = 400$ mV. c) Input and output waveforms considering an input frequency of $f_{in} =$ 200 kHz and amplitude of $A = 300$ mV. A thicker solid line shows the output waveform when a parasitic capacitance ($C_{pad} = 600$ pF) is placed between the drain/source and the back gate, considering the effect of the electrode pads. d) Input and output waveforms considering an input frequency of $f_{in} = 2$ GHz and amplitude of $A = 300$ mV. e) Power spectrum obtained via Fourier transforming the output signal shown in (b). f) Group delay versus frequency of the GFET-based frequency doubler. a–f) Reproduced with permission.[127] Copyright 2016, IEEE.

Figure 10a, the output waveforms after considering different input frequencies are shown in Figure 10b–d. For the input signal with amplitude A and lowest frequency, $f_{in} = 10$ kHz, the output waveform consists of the doubled frequency with amplitude $\approx A/10$, with a clear distortion coming from other higher order harmonics (Figure 10b). A Fourier transform of such waveform is shown in Figure 10e, revealing that 60% of the output RF power is concentrated at the doubled frequency of 20 kHz.

When the input signal is increased up to $f_{in} = 200$ kHz and beyond, a significant decay of the output signal amplitude was observed in the experiment,[130] with a voltage gain of $\approx A/100$ likely because of the presence of a parasitic capacitance (estimated in $C_{pad} = 600$ pF) between the GFET source-drain terminals and its back gate. When including the C_{pad}, the predicted output waveform is similar to that in the experiment for an input frequency of 200 kHz (Figure 10c). If the input frequency is increased further to 2 GHz, as shown in Figure 10d, the output waveform displays the doubled frequency, although with a greater distortion because the group delay is not constant with the frequency according to Figure 10f, indicating that the phase is not linear with the frequency.

Furthermore, with the use of a single GFET (Figure 9e), a subharmonic mixer can be designed to take advantage of the device non-linearity. This way, the device is fed with two different frequencies (the local oscillator, LO, signal at f_{LO} and the RF signal at f_{RF}) and a mixture of several frequencies appears at the output port, including both original input frequencies; the sum of the input frequencies; the difference between the input frequencies; the intermediate frequency (IF), f_{IF}; and other intermodulations.[132] According to the graphene-based mixer topology shown in Figure 9e, the LO signal and DC bias are applied to the gate port through a bias-tee, whereas the RF signal is applied to the drain of the GFET through a high-pass filter, and the IF is extracted with a low-pass filter, both assumed with cut-off frequencies of 800 and 30 MHz, respectively.

The drain-to-source resistance, $R_{DS} = V_{DS,e}/I_{DS}$, versus the gate bias is shown in **Figure 11**a. To reach subharmonic operation, the device is biased at $V_{GS,e} = V_{Dirac} = 1$ V through a bias tee. In contrast, Figure 11b shows the mixer IF output power versus the RF input power, where a near constant conversion loss rate of ≈ 25 dB is obtained. The transient evolution of the signal collected at the drain is shown in Figure 11c, as well as the signal collected at the IF port (Figure 11d), which oscillates as expected at $f_{IF} = |f_{RF} - 2f_{LO}| = 20$ MHz given that $f_{LO} = 1.01$ GHz and $f_{RF} = 2$ GHz. Finally, the spectrum of the signal collected at the drain is presented in Figure 11e, with an output power of ≈ -49 dBm. Lower levels of odd harmonics are observed as well, which are attributed to the non-perfect symmetry of R_{DS} versus $V_{GS,e}$.

3.3. Non-Ideal Effects for Enhancing the Large-Signal Model Prediction Capability

A brief description of the dynamic trap-related phenomenon in GFETs is presented in Section 3.3.1. The implementation of this module into the GFET modeling framework presented in this work is still an ongoing effort; hence, the corresponding subsection should be considered a useful guide for approaching this development. A systematic study on NQS effects in GFETs is provided in Section 3.3.2.

3.3.1. Dynamic Trap Model

Trapping and detrapping dynamic processes in MOS-like transistors can be characterized by their corresponding capture and

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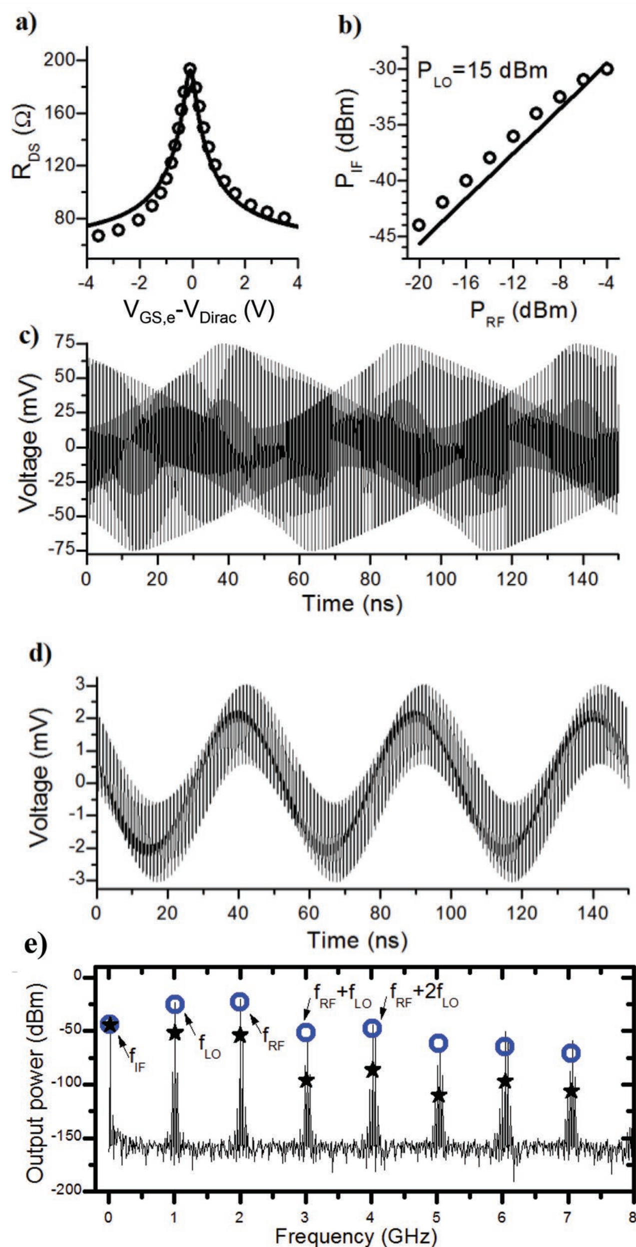

Figure 11. a) Drain-to-source resistance, R_{DS}, versus the overdrive gate voltage, with $R_{DS} = R_d + R_s + R_{ch}$, where R_{ch} is the channel resistance, and R_d and R_s are the extrinsic contact resistances at the drain and source sides, respectively. Solid lines correspond to simulations and the symbols to the experimental results.[131] b) IF output power as a function of the RF input power. The device is biased at the Dirac voltage $V_{GS,e} = V_{Dirac}$ and $P_{LO} = 15$ dBm. c) Transient evolution of the signal collected at the drain at $V_{GS,e} = V_{Dirac}$. The following conditions have been assumed: $P_{LO} = 15$ dBm and $f_{LO} = 1.01$ GHz; $P_{RF} = -20$ dBm and $f_{RF} = 2$ GHz. d) Transient evolution of the IF signal collected at the IF port under the same conditions as in (c). The separation between peaks is 50 ns, which corresponds to $f_{IF} = |f_{RF} - 2f_{LO}| = 20$ MHz. e) Simulated spectrum (solid lines) of the signal collected at the drain (shown in (c)) and the measured power peaks (blue circles) reported in ref. [131]. The stars correspond to the simulation results of power peaks of the signal collected at the IF port (shown in (d)). a–e) Reproduced with permission.[127] Copyright 2016, IEEE.

emission time constants, τ_c and τ_e, respectively. These phenomena can occur over a wide time span depending on the location of the traps centers within the device (cf. Section 2.2.1), as well as on the bias and temperature conditions.[133,134] In devices with high-κ oxides, for example, GFETs, the dynamic performance is strongly affected by the capture and release of carriers,[35,135,136] mainly located at the gate oxide and channel interfaces, because the trap-induced shift of the channel potential modify the bias conditions (transfer curve hysteresis) to achieve specific dynamic characteristics.[35,136] Additionally, trapping phenomena have an impact on the device measurement history, that is, on the initial state of shielding of the channel potential from the gate-source voltage. This impact could not be reduced by a technology-dependent quiescent time approach,[51,81] if either τ_c or τ_e (or a combination of both) is larger than the quiescent pulse duration. Hence, the dynamic modeling approach for graphene transistors should consider the trap time constants for a correct description and projection of the device performance. Furthermore, a reliable compact model considering a description for trap mechanisms can aid the technology development by revealing the device dynamic performance affected by traps under different pulse biasing conditions, as demonstrated in other emerging technologies.[137,138] The latter can be immediately exploited in specific application scenarios, for example, high-speed GFET-based modulators designs,[139,140] and it can be boosted by an accurate modeling of the dependence of the trap-affected/reduced device performance on the pulse biasing conditions.

Trap dynamics in graphene transistors have been systematically characterized[141,142] using silicon technology-based models[143] yielding the traps activation energy distributions and trap time constant distributions of the capture and emission processes. Individual values of trap-related time constants have been experimentally characterized in different GFET technologies ranging from few nanoseconds to the order of few hours.[32,33,144–146] Trap time constants have been obtained by fitting the transient current response over specific non-quiescent conditions with constant pulse widths using empirical exponential models.[32,33,144,145] A capture process is usually related to such extracted trap time constants in these cases; hence, the emission time constants are ignored. Studies with different pulse duration reveal both τ_c and τ_e, as demonstrated in ref. [146] where the latter is obtained with pulses larger than the time required for an apparent initial steady-state of the current.

Currently, physics-based models for τ_c and τ_e in GFETs have not been reported in the literature. However, previously developed high-κ dielectric MOS-models of oxide traps, for example, a non-radiative multiphonon model[147] (already applied to other 2D transistor technologies),[148] can be adapted to GFETs because statistical similarities between trapping processes in the latter and in incumbent technologies have already been observed.[141,142] This model predicts τ_c and τ_e as a function of the position and energy of the trap, applied bias, and temperature.

A numerical device simulation solution, enabled by the drift-diffusion-based description of transport in graphene transistors,[149,150] can be developed by considering the trap-assisted phenomena, including $\tau_{c/e}$-dependent capture and emission rates, in both the Poisson's equation and the

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continuity equation[151,152] as already implemented in other drift-diffusion-based simulators describing different transistor technologies.[152–155] In contrast, an immediate approach to adapt the compact graphene transistor model considering traps in a static regime described in Section 2.2.1 for the dynamic description can be conducted by defining the trap density N_{tr} in Equation (12) in terms of the steady-state trap density $N_{\mathrm{tr,ss}}$ along with τ_{c} or τ_{e}, as implemented previously in a different compact model.[156] The challenging characterization of $N_{\mathrm{tr,ss}}$ has been overcome in ref. [156] using an empirical function depending on the vertical fields and some fitting parameters. An improvement of the compact GFET model discussed in this work (cf. Section 2.1), including the dependence of both lateral and vertical fields as well as τ_{c} and τ_{e} in the definition of N_{tr} is left for future studies. Alternatively, for circuit design purposes, a practical approach considering an adjunct trap network, as demonstrated in studies of emerging transistor technologies,[58,137,138,157] with different time constants defined by RC networks can be an option to include directly in the compact model the impact of the different capture and emission trapping processes within the device.[39,137,138]

3.3.2. Non-Quasi-Static Large-Signal Model

Depending on the input frequency of the time-varying signal, two operating regimes can be distinguished, QS and NQS. In the QS regime, the fluctuation of the varying terminal voltages is sufficiently slow such that the channel charge can follow the voltage variations. This regime applies whenever the transition time for the voltage to change is larger than the transit time of the carriers from source to drain. Contrarily, the NQS regime where carrier inertia effects are important should be considered. When dealing with circuit simulations, assuming a QS regime is not appropriate for long-channel GFETs operating at HFs or when the load capacitance is extremely small.[128,158] Applications of QS approach could result in important errors when predicting phase margins or the stability of wideband amplifiers.[159]

A straightforward approach for modeling a transistor at speeds where the QS regime breaks down involves splitting the channel length in many shorter sections; thus, the QS approach still holds within each section.[128,160,161] To track the breakdown of the QS regime, we consider the frequency-dependent admittance $y_{\mathrm{m}} = y_{\mathrm{dg}} - y_{\mathrm{gd}}$ as a convenient indicator of the electrical gate control on the transistor channel over frequency. Thus, a decrease of $|y_{\mathrm{m}}|$ is interpreted as the loss of the gate control over the channel charge because of the significant carrier inertia originated at HF.[128,162] Considering the 1 µm-long prototype GFET described in **Figure 12**a, a simulation of normalized $|y_{\mathrm{m}}|$ from the QS model is shown in **Figure 13**f. The selected bias to perform the calculation is $V_{\mathrm{G}} = 1.5$ V, $V_{\mathrm{D}} = 1$ V, and $V_{\mathrm{B}} = V_{\mathrm{S}} = 0$ V. The result is compared with that obtained after connecting 20 identical GFETs of length $L/20 = 50$ nm in series (sharing all the same gate, as shown in the inset of Figure 13f), where the array effectively allows the capture of NQS effects. At medium frequencies, both approaches, QS and NQS, predict the same normalized $|y_{\mathrm{m}}|$. However, the upward-going magnitude of normalized $|y_{\mathrm{m}}|$ predicted by the QS model for the 1 µm-long GFET working at HF is clearly unrealistic, as it

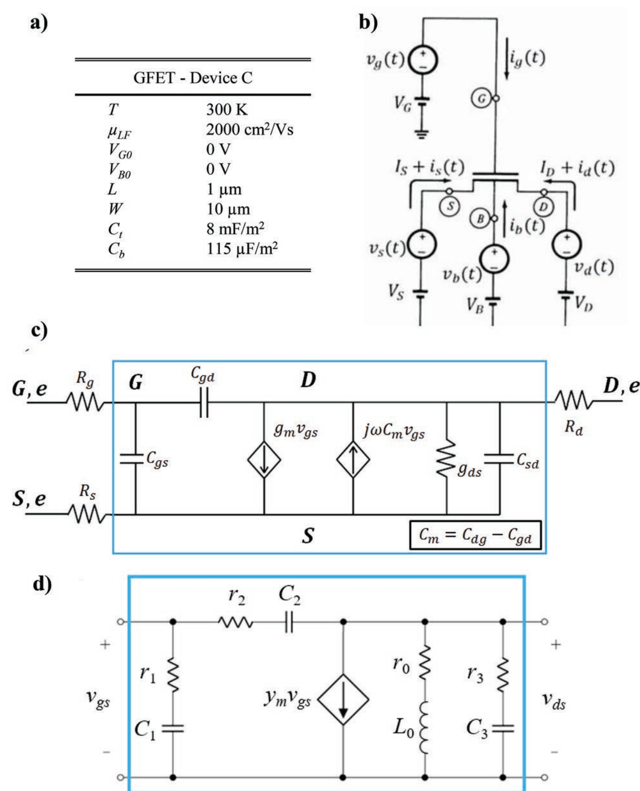

Figure 12. a) Input parameters used to describe a prototype GFET. b) Schematic of a four-terminal FET operating under small-signal regime showing the terminal DC and AC voltages as well as currents. To guarantee charge conservation, the sum of the terminal currents must be zero; thus, $I_{\mathrm{D}} = -I_{\mathrm{S}}$, where the DC top- and back-gate currents are $I_{\mathrm{G}} = I_{\mathrm{B}} = 0$; and $i_{\mathrm{g}}(t) + i_{\mathrm{b}}(t) + i_{\mathrm{d}}(t) + i_{\mathrm{s}}(t) = 0$. c) QS charge-based small-signal model suited to three-terminal GFETs. The equivalent circuit of the intrinsic device is framed in blue. d) Equivalent circuit of a GFET in two-port configuration describing the first-order NQS behavior using lumped elements. b,d) Reproduced with permission.[162] Copyright 2020, IEEE. c) Reproduced with permission.[119] Copyright 2017, IEEE.

suggests an enhancement in the forward gate-to-drain action. This behavior results contrary to the expectation that, at such frequencies, control of the gate on the drain current is gradually lost due to the carrier inertia in the graphene channel. These predictions for GFETs are in qualitative agreement with the NQS studies that have been conducted for conventional silicon-based MOSFETs.[128,159]

4. AC Analysis

When considering analog and RF electronic applications, FET terminals are polarized with a DC bias over which a time-varying voltage is superimposed (Figure 12b). If the voltage amplitude is sufficiently small, the resulting AC components of terminal currents and charges can be linearly related to the AC voltage.[128] Therefore, the non-linear FET can be treated as a linear circuit formed by lumped elements, known as the FET small-signal equivalent circuit. In Section 4.1, we derive a small-signal equivalent circuit for the GFET assuming that the QS hypothesis is valid in the medium frequency range. Later in Section 4.2, we

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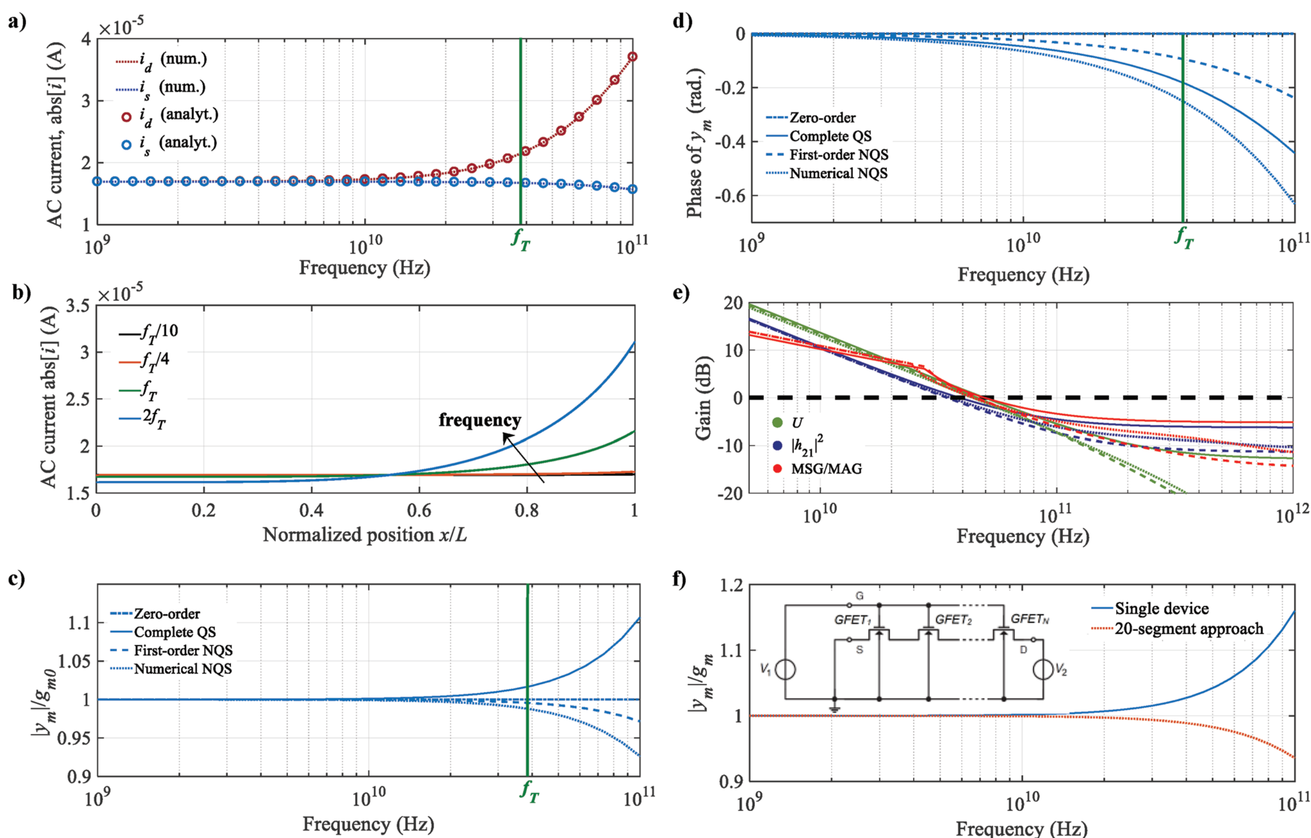

Figure 13. a) Modulus of the AC current at the drain (i_d) and source (i_s) edges computed in analytical (symbols) and numerical (dotted line) ways. The former is computed by truncating the modified Bessel functions of the first kind to $n = 10$ (ref. [162]). b) Modulus of the AC current along the normalized position in the channel for different frequencies. c) Normalized magnitude and d) phase of $y_m = y_{dg} - y_{gd}$ versus frequency at $V_G = 1.5$ V, $V_D = 1$ V, $V_B = V_S = 0$ V. Four types of models are considered: zero-order model (dashed-dotted lines); charge-based QS model described in Section 4.1 (solid line); first-order NQS model described in Section 4.2 (dashed lines); numerical NQS model (dotted line). e) Small-signal current gain (h_{21}), unilateral power gain (U, Mason's invariant),[165] and maximum stable gain/maximum available gain (MSG/MAG) versus frequency of the GFET under test predicted by the QS (solid lines), first-order NQS (dashed lines), and numerical NQS (dotted lines) models. The RF figures of merit f_T and f_{max} are obtained when the gains are reduced to unity (0 dB). f) Normalized magnitude of y_m versus frequency under the operating bias point $V_G = 1.5$ V, $V_D = 1$ V, $V_B = V_S = 0$ V for a single 1 µm-length GFET compared against a two-port configuration of a cascade of 20 GFETs, 50 nm-length each, connected in series. (inset) Schematics of the multisegment approach applied to a GFET. a–f) Reproduced with permission.[162] Copyright 2020, IEEE.

introduce some important non-ideal effects. Specifically, the small-signal model derivation has been extended to cover the NQS regime at HF in Section 4.2.1. A brief review of the dynamic self-heating model in GFETs is presented in Section 4.2.2. Finally, in Section 4.2.3, we discuss a procedure adapted to GFETs to go from the extrinsic to the intrinsic AC frequency response, which requires a model for the parasitic network that should include the effect of the contact pads, metal interconnections, and substrate.

4.1. Quasi-Static Small-Signal Model

Currently, many small-signal models proposed for GFETs have been directly imported from Meyer-like capacitance models.[123,124,126,163,164] They assume that the intrinsic capacitances are reciprocal, which has been proven to result in inaccuracies when predicting the RF figures of merit, as demonstrated in ref. [119] for GFETs. Moreover, these models do not ensure charge conservation, which is crucial not only for accurate device modeling and circuit simulation, but also for proper parameter extraction. To ensure both capacitance reciprocity and charge conservation, the charge-based small-signal model shown in Figure 12c is adopted, where the intrinsic part has been framed in blue. We considered a three-terminal GFET configuration, where the back gate is considered AC disconnected ($i_B(t) = 0$). The small-signal parameters including g_m, g_{ds}, and a set of independent capacitances, including C_{gd}, C_{gs}, C_{sd}, and C_{dg}, are calculated according to the procedure described in Section 3.1. The intrinsic model must be augmented with the extrinsic resistances, R_d and R_s, after linearization around the operating bias point, and the gate resistance, R_g (Figure 12c), if the extrinsic RF performance is intended.

The small-signal model parameters could be either extracted by applying a direct methodology based on S-parameter

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measurements[119] or numerically computed with a DC simulator (optionally including SCE and/or SHE), allowing the prediction of RF performance for different embodiments of GFETs at arbitrary bias.[24,120,150]

4.2. Non-Ideal Effects for Enhancing the Prediction Capability of the Small-Signal Model

Here, we present a set of secondary models to enhance the prediction capability of the small-signal model presented in Section 4.1 by including some relevant non-idealities. We first describe an NQS small-signal model suitable for HF simulations in Section 4.2.1. Thereafter, a dynamic SHE model, developed in the context of small-signal analysis, is presented in Section 4.2.2. Finally, a parasitic network model that considers the effect of contact pads, metal interconnections, and the substrate is discussed in Section 4.2.3.

4.2.1. Non-Quasi-Static Small-Signal Model

Here, we discuss ways for expanding the frequency range that can be reached with the small-signal model while keeping the accuracy to acceptable levels. Therefore, NQS effects arising at HF should be incorporated into the model. A small-signal NQS model can be derived from the analytical solution of the drift-diffusion equation coupled with the continuity equation, which can be expressed in terms of the modified Bessel functions of the first kind.[162] The model can be conveniently simplified to provide an equivalent circuit of lumped elements that can be used in circuit simulators. For instance, if second- and higher-order terms in ω (angular frequency) are neglected in the GFET ω-dependent admittances, a first-order NQS equivalent circuit of the GFET can be obtained (Figure 12d), which is fully described by the following bias-dependent small-signal parameters:[162]

$$
\begin{aligned}
&C_1 = g_{m0}(\gamma\tau_4 - \tau_2); C_2 = g_{m0}\tau_2; C_3 = g_{ds0}\tau_3(1-\gamma) \\
&r_1 = \tau_1/C_1; r_2 = \tau_1/C_2; r_3 = \tau_1/C_3 \\
&L_0 = \tau_1/g_{ds0}; r_0 = 1/g_{ds0}; y_m = g_{m0}/(1+j\omega\tau_1)
\end{aligned}
\tag{24}
$$

where:

$$
\begin{aligned}
&g_{m0} = -\mu_{LF}\frac{W}{L}\frac{k^2}{2(C_t+C_b)}(\mathrm{sgn}[V_{cd0}]h_{GD}V_{cd0}^3 - \mathrm{sgn}[V_{cs0}]h_{GS}V_{cs0}^3) \\
&g_{ds0} = \mu_{LF}\frac{W}{L}\frac{k^2}{2(C_t+C_b)}(h_{GD}+h_{BD})|V_{cd0}|^3 \\
&V_{cx0} = \frac{(C_t+C_b) - \sqrt{(C_t+C_b)^2 \pm 2k[C_t(V_G - V_{G0} - V_X) + C_b(V_B - V_{B0} - V_X)]}}{\pm k} \\
&h_{GX} = -\frac{C_t}{(-C_t - C_b \pm kV_{cx0})}; h_{BX} = \frac{C_b}{C_t}h_{GX}
\end{aligned}
\tag{25}
$$

where the positive (negative) sign applies when $C_t[V_G - V_{G0} - V_X] + C_b[V_B - V_{B0} - V_X] < 0(>0)$ and the subscript X stands for drain (D) and source (S). The time constants τ_1, τ_2, τ_3, and τ_4 from Equation (24) are

$$
\begin{aligned}
&\tau_1 = -\frac{D'}{12}\frac{V_{cd0}^4 V_{cs0}^4}{V_{cd0}^2 + V_{cs0}^2} \\
&\tau_2 = \frac{D'(V_{cd0}^6 - 3V_{cd0}^2V_{cs0}^4 + 2V_{cs0}^6)}{24\quad h_{GD}V_{cd0}^3 - h_{GS}V_{cs0}^3}h_{GD}V_{cd0}^3 \\
&\tau_3 = -\frac{D'}{24}(V_{cd0}^6 - 3V_{cd0}^2V_{cs0}^4 + 2V_{cs0}^6) \\
&\tau_4 = \frac{D'}{24}\frac{(V_{cd0}^2 - V_{cs0}^2)^2}{h_{GD}V_{cd0}^3 - h_{GS}V_{cs0}^3}\left(h_{GD}V_{cd0}^3(V_{cd0}^2 + 2V_{cs0}^2) + h_{GS}V_{cs0}^3(2V_{cd0}^2 + 2V_{cs0}^2)\right) \\
&D' = \mathrm{sgn}[V_{cd0}]\mu_{LF}W^2k^3/(2I_{DS0}^2(C_t+C_b)) \\
&I_{DS0} = \mu_{LF}Wk^2(\mathrm{sgn}[V_{cd0}]V_{cd0}^4 - \mathrm{sgn}[V_{cs0}]V_{cs0}^4)/(8L(C_t+C_b))
\end{aligned}
\tag{26}
$$

with $\gamma = C_t/(C_t + C_b)$.

Because of the simplifications made in the model derivation, the selected bias point should be placed far enough from the Dirac voltage for the device to operate in the linear region. The assumption is $V_{cx0}^2 \gg (\pi k_B T/(\sqrt{3}q))^2 + 2q\Delta^2/(k\pi(\hbar v_F)^2)$. Although it is certainly a limitation of the model, the approach is useful for the important usage of GFET as an amplifier. In addition, the expressions shown in Equations (25) and (26) consider $k|V_{cx0}| \gg (C_t + C_b)$. The opposite case, $(k|V_{cx,0}| \ll (C_t + C_b))$, is provided in ref. [162].

To demonstrate the impact of NQS effects on the RF performance of GFETs, we considered the device described in Figure 12a. It consists of a double-gated topology with 10 nm-Al_2O_3 and 300 nm-SiO_2 dielectrics at the top and back gate stacks, respectively. Figure 13a shows the absolute value of the small-signal current at the drain (i_d) and source (i_s) edges for several frequencies, as well as the calculated f_T (=38.8 GHz). Both i_d and i_s have been computed both in an analytical and numerical way through the evaluation of the modified Bessel functions of the first kind.[162] The analytical case consists of truncating the function to a tenth order. According to Figure 13a, $|i_d|$ and $|i_s|$ show same value for frequencies lower than $\approx f_T/4$, which agrees with the QS assumption and with the behavior of silicon-based FETs operating at medium frequency.[128] For frequencies higher than $f_T/4$, $|i_d|$ and $|i_s|$ differ from the QS value adopting different values, which indicates that the channel charge in the graphene layer cannot follow the voltage variations for such frequencies.

Figure 13b shows the modulus of the AC current, $|i|$, along the normalized channel length for different frequencies. The solid orange line shown in Figure 13b corresponds to the frequency of $f_T/4$, which has been chosen to delimit the QS and NQS regimes.[128] For frequencies lower than $f_T/4$, for example, $f_T/10$, the AC current is approximately the same along the channel length, which is consistent with the QS approximation. However, for frequencies higher than $f_T/4$, for example, f_T or $2f_T$, the carriers do not have enough time to move from drain to source in a signal period, resulting in a departure of i from the QS value, which is in accordance with the behavior observed in Figure 13a.

Figure 13c,d shows the normalized magnitude and phase of $y_m = y_{dg} - y_{gd}$. It is observed that from the zero-order model to the first-order, the NQS model produces a significant improvement in the region of validity (where we have assumed here that the numerical solution provides the reference solution). This is because y_m contains a right-half-plane zero for this zero-order model[119] in contrast to the

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left-half-plane pole in y_m for the first-order NQS model (Equation (24)). The upward-going magnitude predicted by the QS model at HF is unrealistic, although the phase of y_m is predicted better by the QS model than the first-order NQS model; therefore, a higher order correction would be needed if the phase of y_m is crucial for the targeted range of frequency according to the intended application. This discussion as well as results shown in Figure 13c,d is in qualitative agreement with the NQS studies conducted for conventional silicon-based MOSFETs.[128,159]

The frequency dependence of the current and power gains predicted by the different models, namely $|h_{21}|^2$, U, and MSG/MAG, are shown in Figure 13e. Differences between the QS and NQS model predictions are not significant below f_T, but the QS model overpredicts the gain for frequencies higher than f_T, highlighting the importance of including the NQS effects.

4.2.2. Dynamic Self-Heating Model

The equations we have presented so far to describe the drain current include a dependence on the bias point and the temperature. To analyze the impact of self-heating on HF performance, the dependence of the small-signal parameters on temperature must be studied. Here, we present a model valid for AC input voltages, assuming that the GFET presents a complex thermal impedance, Z_{th}, that depends on the angular frequency, ω (=$2\pi f$), and on the different thermal paths through which the power, P_{dis}, is dissipated from the graphene channel. This heat crosses the different device thermal boundaries defined by the interfaces between the materials. Z_{th} can be represented by various thermal RC networks characterized by the values of thermal resistances, $\Re_{th,i}$, and thermal frequencies, $f_{th,i}$, as follows:

$$Z_{th}(\omega) = \sum_i \frac{\Re_{th,i}}{1 + j\dfrac{\omega}{2\pi f_{th,i}}} \tag{27}$$

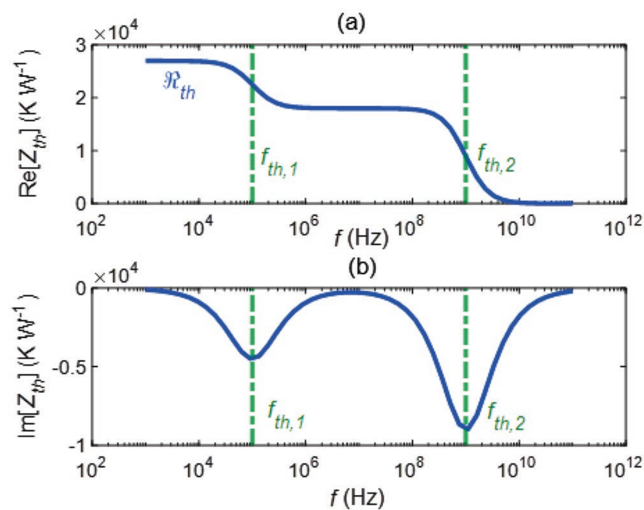

Figure 14. Complex thermal impedance of the graphene transistor showing two poles, each one corresponding to a heat dissipation path. a) Real part and b) imaginary part as a function of the applied frequency.

The sum of all thermal resistances gives the total thermal resistance, which causes the increase of graphene temperature owing to DC self-heating, as addressed in Section 2.2.2

$$\Re_{th} = \sum_i \Re_{th,i} \tag{28}$$

Figure 14 shows the real and imaginary parts of $Z_{th}(\omega)$ for the simple case of two thermal *RC* networks in series (two poles), one at a thermal frequency of $f_{th,1}$ = 1 kHz and the other at $f_{th,2}$ = 1 GHz. The thermal frequencies highly depend on the specific GFET technology because they are a function of the heat dissipation paths. Although they have been arbitrarily chosen to illustrate dynamic SHE, they could be observed in the frequency range between ≈5 and 10 MHz according to experimental measurements performed elsewhere.[54,146]

Following the temperature-dependent two-port network approach developed by Rinaldi[166] and assuming no leakage current through the gate oxides, the small-signal parameters are modified according to the following equations:

$$\begin{aligned} y_{gg}(\omega) &= y_{gg,T}(\omega) \\ y_{gd}(\omega) &= y_{gd,T}(\omega) \\ y_{dg}(\omega) &= \frac{y_{dg,T}(\omega) + cZ_{th}(\omega) y_{gg,T}(\omega) V_{GS}}{1 - cZ_{th}(\omega) V_{DS}} \\ y_{dd}(\omega) &= \frac{y_{dd,T}(\omega) + cZ_{th}(\omega)\left(y_{gd,T}(\omega) V_{GS} + I_{DS}\right)}{1 - cZ_{th}(\omega) V_{DS}} \end{aligned} \tag{29}$$

where $c = \partial I_{DS}/\partial T$ is a coefficient describing the rate of change of the current with respect to the temperature and $y_{ij,T}(\omega)$ are the small-signal parameters calculated by the QS approximation at a constant temperature, that is, assuming that the frequency is sufficiently high so the device temperature cannot follow the rapid oscillations of the electrical signal.

Figure 15 shows the simulated intrinsic small-signal parameters, $y_{dg}(\omega)$ and $y_{dd}(\omega)$, for the device described in ref. [51] at selected bias points as a function of the frequency, and assuming a two-pole thermal impedance as that presented in Figure 14. Above the thermal frequencies, $f_{th,1}$ and $f_{th,2}$, the thermal impedance is $Z_{th}(\omega) \approx 0$; therefore, the small-signal parameters are equal to the values at a constant temperature $y_{ij}(\omega) \approx y_{ij,T}(\omega)$. On the contrary, for very low frequencies, the graphene temperature can follow the oscillation of the electrical signal. Notably, it is very important to consider the SHE in HF performance calculation, as the QS approximation directly applied to the DC current curves assumes that the temperature varies with the bias point.

4.2.3. Parasitic Network Model

Generally, the parasitic network plays a significant role in determining the GFET performance. For on-wafer RF FETs, it is determined by the contact pads, metal interconnections, and the substrate.[167] **Figure 16**a shows the complete GFET circuit with the parasitic network connected to the intrinsic FET

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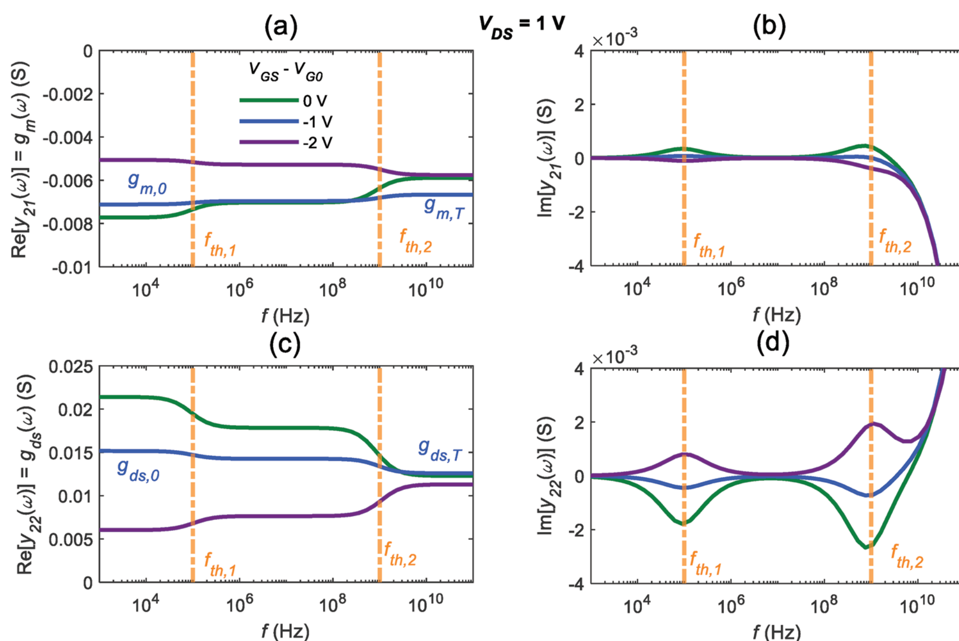
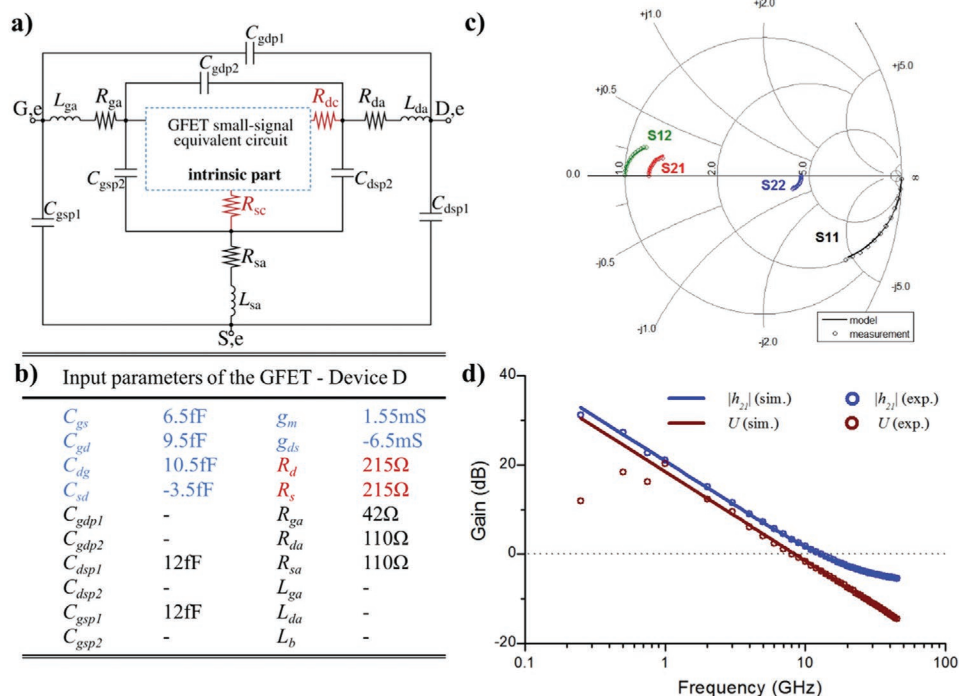


Figure 15. Small-signal parameters affected by SHE at the biases V_{DS} = 1 V, $V_{GS} - V_{G0}$ = 0, –1, and – 2 V. a) Real part and b) imaginary part of y_{dg}. c) Real part and d) imaginary part of y_{dd}.

equivalent circuit discussed previously, as well as the contact resistances.[168]

To obtain information on internal physical mechanisms in fabricated devices for a given intrinsic model parameter to be validated for a correct description of the GFET RF performance, de-embedding techniques should be applied to remove the effect of the parasitic network. This can be done by characterizing dummy test structures developed ad hoc, which are



b) Input parameters of the GFET - Device D

C_{gs}	6.5fF	g_m	1.55mS
C_{gd}	9.5fF	g_{ds}	-6.5mS
C_{dg}	10.5fF	R_d	215Ω
C_{sd}	-3.5fF	R_s	215Ω
C_{gdp1}	-	R_{ga}	42Ω
C_{gdp2}	-	R_{da}	110Ω
C_{dsp1}	12fF	R_{sa}	110Ω
C_{dsp2}	-	L_{ga}	-
C_{gsp1}	12fF	L_{da}	-
C_{gsp2}	-	L_b	-

Figure 16. a) Typical topology of the small-signal equivalent circuit for an RF GFET. b) Parameters of the equivalent circuit for describing the experimental GFET reported in ref. [119]. c) S-parameter measurements (circles) and simulations (lines) for the applied bias $V_{GS,e}$ = 0.2 V and $V_{DS,e}$ = 1 V. d) RF performance of the experimental GFET. Measured (symbols) and simulated (solid line) small-signal current gain ($|h_{21}|$) and Mason's invariant (U) plotted versus frequency. a–d) Reproduced with permission.[119] Copyright 2017, IEEE.

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usually fabricated on the same wafer as the device under test. The common de-embedding procedure involves measuring the S-parameters of "open," "short," and "thru" test structures and applying a mathematical procedure to subtract the effect of certain elements of the parasitic network. Therefore, the small-signal parameters of the intrinsic FET can be isolated from the de-embedded S-parameters. However, the contact resistances, R_s and R_d, cannot be de-embedded in Schottky-like transistors such as 2DM-based FETs; therefore, the parasitic resistances extracted by this method are R_{sa} and R_{da} (cf. Figure 16a). As a result, R_s and R_d should be extracted separately, for example, using the transfer length method technique or an adapted Y-function-based method.[169] The first one involves the fabrication and characterization of back-gated devices with different channel lengths whereas the second one is a more general approach because it can be applied to individual devices regardless the gate architecture. Once the values of R_s and R_d are known, their impact can be removed from the dynamic characteristics by following a matrix algebra process as shown elsewhere.[168]

The outer parasitic capacitances (parasitic inductances) in Figure 16a, namely C_{gsp1}, C_{gdp1}, and C_{dsp1} (L_{ga}, L_{da}, and L_{sa}), correspond to the electrostatic couplings (magnetic inductances) of the access layout pads. These capacitive (inductive) effects are related to the "open" ("short") test structure; hence, their values can be directly measured and/or removed from the device using the de-embedding method. In contrast, a special dedicated "open-pad-dummy" (also called "mute") structure[112,170,171] with identical layout as the active device, including the gate fingers, is required to extract and/or remove the inner parasitic capacitances, C_{gsp2}, C_{gdp2}, and C_{dsp2}. These parameters are associated to the electrostatic couplings between gate-to-source and gate-to-drain metal interconnect fingers (also identified as extrinsic fringing capacitances) and finger overlaps capacitance effects owing to gates wider than the channel as well as to a spurious coupling between feed and connecting lines in a finger layout. Notably, for practical purposes, for example, the design of a functional GFET-based RF circuit, the unavoidable inner parasitics should be considered. In addition to the experimental characterization via the HF admittance parameters of the test structures,[112,170,171] the C_{xxp2} values have been obtained in the literature using numerical device simulations (of the dummy structure)[172–174] as well as with compact model fitting for a correct description of measurements.[24,119,175,176] Models embracing these parasitics in GFETs are still missing in the literature. A possible approach for the correct description of effects embraced by C_{xxp2} is the conformal mapping technique,[177] accounting for the fringing fields and the solution of the parallel plate capacitances within the layout as suggested in studies of other FET technologies.[161,178,179]

Figure 16b shows the intrinsic small-signal parameters (blue color), parasitic network parameters (black color), and contact resistances (red color) describing the experimental GFET reported elsewhere.[119] The de-embedding procedure described in refs. [167, 170, 180] involving "open" test structures, has been implemented to eliminate the contribution of the parasitic network. From the de-embedded S-parameters, the intrinsic elements have been obtained through the extraction methodology proposed in ref. [119]. As a novelty, the method considers R_s and R_d as a part of the (augmented) intrinsic GFET model; therefore, they can be extracted on equal footing with the rest of small-signal intrinsic parameters. Measured and modeled S-parameters at V_{GS} = 0.2 V and V_{DS} = 1 V plotted together in Figure 16c are in good agreement. In addition, Figure 16d shows the experimental extrinsic current gain ($|h_{21}|$) and extrinsic Mason's invariant (U), both obtained from the S-parameters measurements shown in Figure 16c, compared to the simulated ones obtained from the small-signal model (Figure 16a,b).

5. Noise Analysis

Graphene-based FETs have proven to be excellent contestants for forthcoming RF applications owing to graphene's exceptional characteristics that can ensure high speed performance.[181] In such circuits, noise can either be in the form of LFN below the corner frequency f_c or high-frequency noise (HFN) above the aforementioned frequency; thus, it is a crucial figure of merit.[161] LFN can deteriorate the performance of RF circuits by being up-converted to phase noise[182–185] and it can downgrade the sensitivity of chemical–biological sensors[186,187] or optoelectronic devices.[188] Conversely, HFN can be very critical for the sensitivity of an RF system and the signal-to-noise ratio at the RF regime.[189] Thus, both LFN and HFN should be investigated thoroughly and modeled correctly.

There are three major mechanisms responsible for the generation of LFN in transistors: i) carrier number fluctuation effect (ΔN),[190–193] ii) mobility fluctuation effect ($\Delta\mu$),[194] and iii) contact resistance contribution (ΔR).[161] ($\Delta\mu$ $k_B T$ ΔN is formed by trapping/detrapping mechanism near the oxide interface. Each individual carrier that gets captured and then released by an active trap within a few $k_B T$ from the Fermi level creates random telegraph noise (RTN),[191] which demonstrates Lorentzian shape in frequency domain. Although experimental RTN has not been observed in GFETs, which could be because of the large area of the devices under test, the superposition of the Lorentzian spectra results in $1/f$ noise in longer-gated channels, where the number of slow near-interfacial and border traps is adequate, if the distribution of their time constants is uniform on the logarithmic axis.[190,191]

Moreover, a thermally activated process is assumed for the trapping/detrapping mechanism for ΔN $1/f$ noise, where the time constants follow a non-radiative multiphonon model.[190,191]

Fluctuations of the carrier mobility are responsible for the generation of $\Delta\mu$ model, which is described by the empirical Hooge expression, and contact resistance can also contribute to LFN (ΔR).[161]

Regarding CMOS processes, a number of analytical models are available in the literature, which mostly refer to the ΔN effect and consider a uniform channel. They are valid only in the linear region of operation and result in a squared transconductance-to-current ratio) $(g_m/I_{DS})^2$ trend of normalized output noise (S_{ID}/I^2_{DS}). Several recent works have indicated the same mechanisms (ΔN, $\Delta\mu$, ΔR) responsible for the genesis of $1/f$ noise in GFETs.[64,195–203] Moreover, Δ N prevails as the number of graphene layers reduce, whereas $\Delta\mu$ is dominant in multilayer

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devices.[198] The same studies depict an M-shape dependence of normalized 1/*f* noise data versus effective gate voltage ($V_{GEFF} = V_{G(B)S} - V_{G(B)0}$). Although most of the 1/*f* noise models in GFETs are derived based on the simplified approach of uniform channel mentioned before,[196–201] we recently proposed a complete physics-based compact model,[64,202] which accounts for all the non-homogeneities as well as velocity saturation effect, that can affect 1/*f* noise in GFETs (Section 5.1). Additionally, a complete 1/*f* noise parameters extraction procedure has been introduced.[64,203] The model gives accurate results capturing both the M-shape dependence and the reduction of 1/f noise at high electric fields owing to the velocity saturation mechanism[64,203] when validated with data from fabricated devices.[63] The aforementioned experiments present a slightly ideal 1/*f* behavior (cf. Figure 4 in ref. [64]).

Moreover, the study of variability issues in currently immature GFET technologies is very critical for the transition to large-scale wafer fabrication and eventually to massive applications production. 1/*f* noise statistical deviation is a significant variable and it should be investigated thoroughly. Although LFN variance has been adequately researched in CMOS devices following empirical,[204] simplified,[205] or complete approaches,[206] there is a lack of studies regarding GFETs. Recently, we designed a complete physics-based compact model[207] describing the bias dependence of the 1/*f* noise variance in GFETs accurately when compared to experimental data (Section 5.1).[208]

For HFN modeling in GFETs, very few studies have been reported. They are mainly based on simple long-channel approaches, straightforwardly adapted from CMOS, and neither do they focus on the bias dependence of noise, nor do they consider the degenerate nature of graphene.[175,209–211] Thus, we developed a novel physics-based compact model that accurately describes HFN drain current spectral density (S_{ID}) for various operating conditions including the derivations in the velocity saturation effect and graphene's degeneracy (Section 5.2).[212] Two short channel GFETs have been measured[63] in HF range to extract intrinsic S_{ID} after appropriate de-embedding as well as R_g and R_c elimination procedures. The experimental data precisely validate the proposed model for a wide V_{GS} span without using any fitting parameters and S_{ID} increases toward higher-carrier densities until it saturates, similarly to MOSFETs.[213] The model is also derived for the non-degenerate case, where a significant overestimation of measurements is revealed, indicating that the degenerate nature of graphene significantly reduces HFN. In addition, noise excess factor γ, a crucial figure of merit of noise performance in RF circuits,[214] is first examined in GFETs and presented in ref. [212].

In general, the noise models presented in Section 5 are extracted based on a methodology of dividing the device channel in very small slices where each one of them is a local noise source; all these local noise sources are considered uncorrelated and thus the integration of the local power spectral densities from source to drain results in the total channel noise.[64,189,202,203,207] Thereafter, the final compact expressions are obtained considering the chemical potential-based *I*–*V* model proposed in Equations (1)–(11) of Section 2.1. All the models are implemented in Verilog-A; thus, they can be easily integrated in circuit simulators.

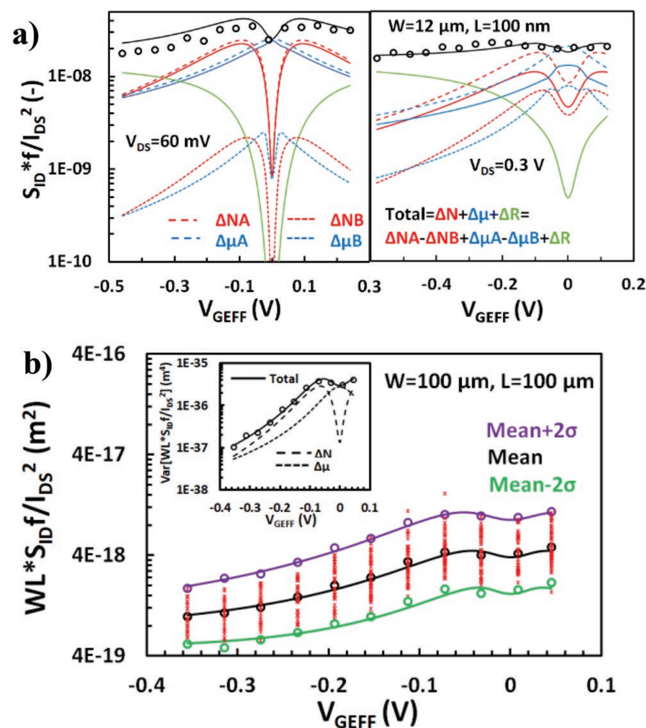

Figure 17. a) Drain current noise divided by squared drain current $S_{ID}\,f/I^2_{DS}$, referred to 1 Hz, versus gate voltage overdrive $V_{GEFF} = V_G - V_{G0}$ at low $V_{DS} = 60$ mV in left subplot and high $V_{DS} = 0.3$ V in right subplot for a $W/L = 12$ µm/100 nm GFET. Data are shown with markers whereas different noise contributors are depicted with solid, dashed, and dotted lines as well as with different colors. b) Normalized 1/*f* noise $WLS_{IDf}f/I^2_{DS}$ versus V_{GEFF}, for a 100 µm/100 µm GFET at $V_{DS} = 50$ mV. Measured noise from all available samples: star markers, measured ln-mean noise, and its ±2-sigma deviation: open circle markers, mean and ±2-sigma deviation model: lines. (mean data and model: black, +2-sigma deviation data and model: purple, −2-sigma deviation data and model: green). Inset illustrates the variance of normalized 1/*f* noise Var [$WLS_{ID}f/I^2_{DS}$] versus V_{GEFF}, for the same GFET. Markers: data, solid lines: total model, dashed lines: individual contributions (ΔN, $\Delta\mu$). a) Reproduced with permission.[64] Copyright 2019, ACS. b) Reproduced with permission.[207] Copyright 2020, Royal Society of Chemistry.

5.1. Low-Frequency Noise Model

The proposed 1/*f* noise model's compact expressions are presented in Equations (S1)–(S5), Supporting Information.[64,202] The precise performance of the model is verified in **Figure 17**a, where normalized 1/*f* noise $S_{ID}\,f/I^2_{DS}$ is shown versus V_{GEFF} for a $W/L = 12$ µm/100 nm short-channel GFET with round markers representing the measurements and lines the different contributors of the model. More specifically, ΔN and $\Delta\mu$ effects are illustrated with solid lines and they are calculated by the subtraction of long-channel terms, ΔNA and $\Delta\mu A$ (dashed lines),[202] with the velocity saturation related terms, ΔNB and $\Delta\mu B$ (dotted lines), respectively;[64] ΔN terms are denoted in red, $\Delta\mu$ are denoted in blue, and ΔR are denoted in green. Evidently, ΔN is responsible for the M-shape whereas $\Delta\mu$ presents a Λ-shape and contributes near CNP. In the left subplot, the low $V_{DS} = 60$ mV regime is depicted and it is clear that the long-channel terms are dominant there, whereas the velocity

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saturation related ones are negligible owing to the low electric field value. On the contrary, the higher $V_{DS} = 0.3$ V region shown in the right subplot confirms that as the electric field is heightened, velocity saturation effect becomes significant; thus, ΔN and $\Delta \mu$ mechanisms and consequently total $1/f$ noise are reduced. The experimental data confirm the above theoretical findings, which are of outstanding significance because the unavoidable usage of high-speed short-channel devices in graphene RF circuits makes it vital to model their LFN.

Regarding the $1/f$ noise variance model, Equations (S6)–(S10), Supporting Information, are derived and presented.[207] $WLS_{ID} f / I^2_{DS}$ $1/f$ noise versus V_{GEFF} for a long-channel solution-gated $W/L = 100$ μm/100 μm GFET is shown in Figure 17b. Mean $1/f$ noise data are depicted with black markers whereas the solid lines, accounting for the mean $1/f$ noise model, fit these data precisely. $1/f$ noise data from all the samples are shown with small red markers. For the validation of $1/f$ noise statistical model,[207] $\pm 2\sigma$ standard deviation of normalized $1/f$ noise are also presented both for the model and experimental data with purple ($+2\sigma$) and green (-2σ) solid lines and markers, respectively. The proposed statistical $1/f$ noise model captures the dispersion of the data and its bias dependence accurately,[207] and the general picture reveals the consistency between the mean value and variance $1/f$ noise models. The inset of Figure 17b shows the variance of normalized $1/f$ noise Var $[WLS_{ID} f / I^2_{DS}]$ versus V_{GEFF} for the same GFET, where the agreement of the total model (solid lines) versus data (markers) is consistent. Notably, the variance contributions, ΔN and $\Delta \mu$, shown with dashed and dotted lines, respectively, behave similarly as in the mean value $1/f$ noise case. Therefore, the ΔN model provides an M-shape to $1/f$ noise variance as it did for its mean value, whereas the $\Delta \mu$ model follows a Λ-shape, contributing to $1/f$ noise variance mainly at CNP, as it was the case for mean value 1/f noise.[207] Another important observation is that $1/f$ noise statistical dispersion in GFETs is not related with I–V quantities but it is caused by the deviations of the physical parameters of ΔN and $\Delta \mu$ mechanisms, which are the number of traps, n_{tr}, and the Hooge parameter, α_H, respectively.[207]

5.2. High-Frequency Noise Model

The HFN S_{ID}, model is accurately defined in Equations (S11)–(S14), Supporting Information.[212] Contrary to the LFN, where velocity saturation effect has been shown to decrease noise under high electric field conditions (cf. Figure 17a), it has an opposite additive effect on HFN.[209] HFN measurements have been conducted at $f = 1$ GHz, which forces the GFETs under test to operate at the QS regime as their extrinsic f_T is higher than $f = 1$ GHz.[63] Therefore, S_{ID} is frequency-independent under such operating conditions and the attention is concentrated on its bias-dependence. **Figure 18**a presents intrinsic measured S_{ID} versus V_{GS} at $V_{DS} = 0.5$ V for a $W/L = 24$ μm/200 nm (EG5) GFET in the left and a $W/L = 24$ μm/300 nm (EG8) one in the right subplot, respectively, with markers, whereas the complete model is depicted with solid lines. V_{GS} extends from high p- to high n-type carrier densities' area but the maximum g_m, recorded in the p-type regime,[211,212] leads the attention to this specific region. Owing to the direct relation of g_m with S_{ID},[212] the latter

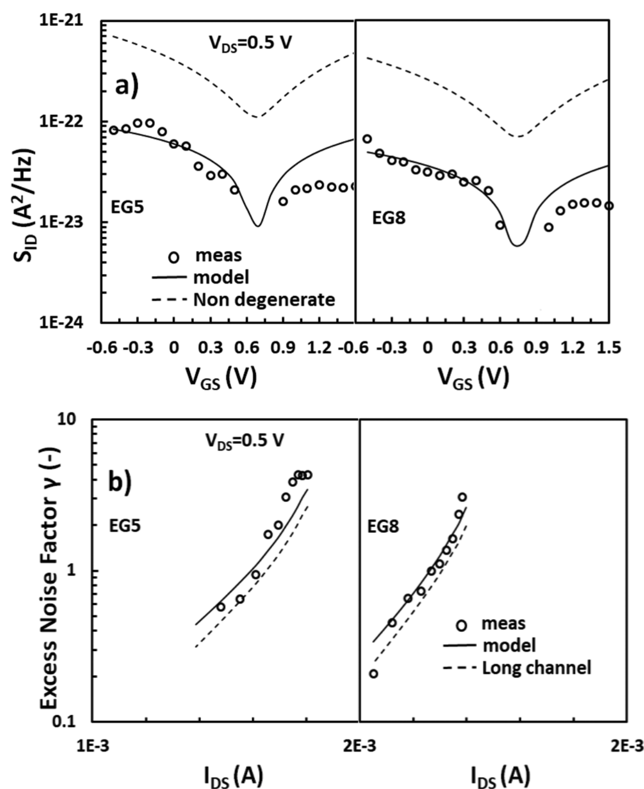

Figure 18. a) Channel thermal noise, S_{ID}, at 1 GHz versus V_{GS} and b) noise excess factor γ versus I_{DS} for short channel GFETs with W = 24 μm and L = 200 nm (EG5-left subplots), L = 300 nm (EG8-right subplots), respectively at V_{DS} = 0.5 V. markers: measured, solid lines: model, dashed lines: non-degenerate model in (a) and long channel model in (b). a,b) Reproduced with permission.[212] Copyright 2021, IEEE.

is also higher there; thus, the model, which presents a symmetric behavior, accurately follows the experiments in the p-type regime. Non-degenerate models are also demonstrated with dashed lines for both devices and they overestimate the experiments almost one order of magnitude, indicating that using HFN CMOS models in GFETs is not accurate. As mentioned earlier, excess noise factor, γ, is first examined thoroughly in GFETs in ref. [212]. Figure 18b illustrated both experimental (markers) and simulated (lines) γ for EG5 in the left and EG8 in the right subplot, respectively, at $V_{DS} = 0.5$ V versus I_{DS}, which is now confined in the p-type region where the specific study is focused, as detailed earlier. The validation of the model with the measurements is reliable. A long-channel case is also shown with dashed lines after ignoring the velocity saturation effect, which results in a quite significant underestimation of γ. In addition to S_{ID}, which dominates above corner frequency f_c, the potential fluctuations within the channel are coupled with the gate through gate oxide capacitance resulting in induced gate noise, S_{IG}, and its correlation with channel noise S_{IGID}, both important at frequencies close or above f_T at NQS regime.[161,189] These two terms increase with frequency because S_{IG} is proportional to f^2 whereas S_{IGID} is proportional to f. Although there are some simple long-channel approaches to model the above two contributions, they are not valid in the NQS region of operation. Currently, our model predicts a frequency independent S_{ID} (white noise) that is valid for frequencies sufficiently below f_T, whereas S_{IG} and S_{IGID}

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have a very small effect there. The characterization and compact modeling of S_{IG} and S_{IGID} are of critical importance for HFN at higher frequencies; this task is an ongoing research.

6. Conclusions

We have provided an updated report on the progress made toward the development of a modular compact modeling technology allowing DC, transient, AC, and noise analysis of arbitrary GFET-based circuits. The models have a strong physical basis and consider some non-idealities that have proven to impact in static and/or dynamic operation. The non-idealities include extrinsic-, short-channel-, trapping/detrapping-, self-heating-, and NQS-effects. The models have been validated against experimental results for the relevant operating conditions up to frequencies of some tens of GHz. We estimate that the presented modeling technology's readiness level (TRL) is four (validation in laboratory environment). To push the technology toward higher TRLs, more efforts are needed in different directions. First, there are some relevant physics discussed along the manuscript that deserve further modeling and/or experimental validation, such as: 1) trapping/detrapping mechanisms under dynamic operation, 2) SHE at frequencies below and close to the thermal frequency, 3) NQS effects at frequencies near and beyond the cut-off frequency, and 4) HFN including the gate-induced noise and its correlation with channel noise at frequencies close or beyond the cut-off frequency in the NQS regime. Second, moving to higher TRLs requires the successful application of state-of-the-art modeling technology to ICs working in a relevant/operational environment toward the improvement and strengthening of the GFET technology by a constant feedback between fabrication technology groups, modeling groups, and circuit designers. That requires a more systematic characterization of RF building blocks such as frequency multipliers, mixers, and low-noise amplifiers, to mention a few. This would allow the full demonstration of the consistency between simulation and experiment for the relevant operation conditions. Finally, statistical variability in device characteristics is an important aspect that should be addressed in future investigations, which is critical for the transition to the large-scale wafer fabrication and eventually to massive applications production.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

2D materials, compact modeling, graphene, hybrid integrated circuits, monolithic integrated circuits, radio-frequency, transistors

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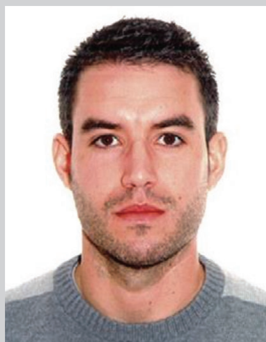

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