APPLIED RESEARCH

A High-Efficiency Isolated Wide Voltage Range DC-DC Converter Using WBG Devices

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ABSTRACT The recent release of the standard USB-PD 3.1 specifies variable output voltages from 5 V to 48 V featuring a step forward towards a universal adaptor but rising new challenges for the converter topologies used up to now. In such applications, a first AC-DC stage is followed by a DC-DC stage. In this paper, emerging WBG technologies are applied to the asymmetrical half-bridge flyback topology, demonstrating the potential of such combination as a wide voltage range DC-DC stage. Its suitability for high-density and high-efficiency USB-PD Extended Power Range (EPR) and battery charger applications is discussed. The impact of different switching technologies, silicon and wide band gap, is analyzed. A general method to dimension the converter is presented and an iterative process is used to evaluate the theoretical efficiency under different conditions and switching devices. Finally, the advantages of the presented converter using Gallium Nitride (GaN) devices are demonstrated in a 240 W DC-DC prototype. It achieves a full load efficiency of 98%, and it is able to deliver an output voltage from 5 V to 48 V with input voltage range from 120 V to 420 V, as well an outstanding power density of 112 W/inch^3 uncased.

INDEX TERMS GaN, adaptor, USB-PD EPR, power density, battery charger.

I. INTRODUCTION

Recent trends push existing AC-DC adaptors towards a universal power supply capable of being used for many different purposes, from charging smartphones or tables to laptops, e-bikes or power tools. One major standard in this direction is the recent publication of the USB-PD Extended Power Range (EPR) [1], which defines adaptors with output voltage ranging from 5 V to 48 V and up to 240 W. Furthermore, to ensure the acceptance of such universal power adaptor, a reduce size and limited weight is desired. Lastly, to allow the usage of any adaptor worldwide, universal input voltage range (100 Vac to 240 Vac) is an expected characteristic. The new USB-PD specification, combined with wide input and output voltage ranges, bring additional challenge to achieve

very high power density and efficiency [2] for the topologies and architectures used in converters up to now.

Possible solutions in this application include PFC followed by a flyback-based converters [3], [4], [5], [6], [8], see Fig. 1.a, they are extremely flexible in terms of input and output voltage range, but they are very bulky due to its transformer size. LLC based converters [9], [10] can be very small and efficient but they are very limited in terms of input and output voltage range. They are the preferred solution for high power and fixed output voltage and are typically combined with a Power Factor Correction (PFC) boost converter as first stage.

If the LLC topology is used, wide output voltage can be achieved adding an additional downstream buck stage. However, a three-stage converter configuration (PFC + LLC + Buck, Fig. 1.b), will lead to a bulky and expensive converter.
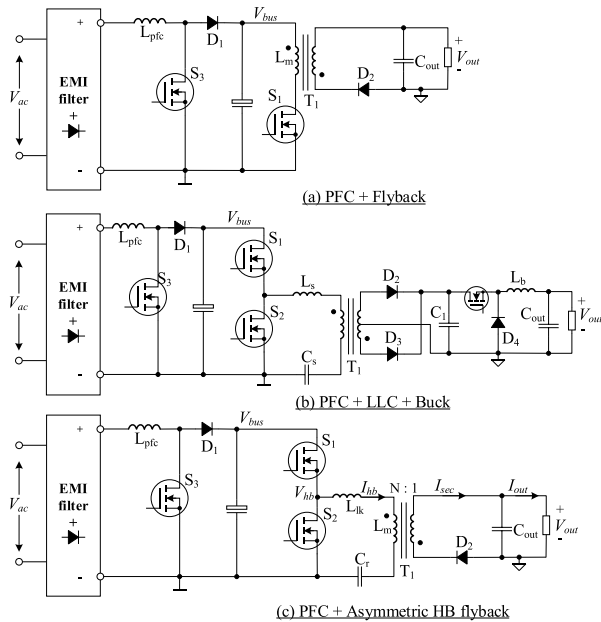
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FIGURE 1. Suitable architectures for the discussed applications. Proposed solution (c): Boost PFC (AC-DC stage) followed by AHB converter (DC-DC stage).

This paper proposes a PFC followed by an asymmetrical half-bridge flyback (AHB) topology, also known as Hybrid Flyback [11], using GaN devices, see Fig. 1.c.

The combination achieves optimum performance in terms of wide voltage range, small size, high efficiency and low number of components for the DC-DC stage thanks to the figure of merit $R_{dson}C_{o(tr)}$ of wide band gap switches and the characteristics of the topology.

This manuscript is organized as follows: firstly, a theoretical review of the AHB topology is carried out. Secondly, general design rules and an estimation of the efficiency with a numerical iteration method is shown. Afterwards the prototype used to demonstrate the analytical results is presented as a base for the conclusions of the paper.

II. ENERGY PROCESSING IN POWER CONVERTERS

In some non-isolated converters, a percentage of the energy is transferred directly from the input to the output and does not need to be stored in reactive elements, but the rest of energy needs to be processed, meaning that it has to be stored and released by reactive elements [12], [13], [14], [15]. Examples of that are buck or boost converters where the current flows directly from the input to the output during certain phase of the operation without processing the energy [12], [13].

An analogue operation to direct energy transfer is observed in isolated converters when the energy is transferred in forward mode through the transformer [16]. This effect avoids energy storage in magnetics components, which is typically more expensive in terms of efficiency and size than capacitive energy storage [17].

With the previous considerations, and to ensure the best efficiency and minimum size, different characteristics are desired in power converters:

1) In isolated converters: maximize energy transfer in forward mode. In non-isolated converters: maximize direct energy transfer.
2) When energy is stored in magnetic components, higher frequencies help to reduce the size.
3) Zero voltage switching (ZVS) and zero current switching (ZCS) techniques to minimize switching losses, especially if high switching frequencies (F_{sw}) are used.
4) Lowest possible RMS currents to reduce conduction losses.
5) In general, minimum number of elements involved in the energy transfer process.

For the design of the converter, the above characteristics must be balanced to achieve an optimal design for the given requirements.

A. PROPOSED TOPOGY

In AC-DC applications where a PFC (Power Factor Correction) [18] is required, a dual stage approach is typically used, consisting of a PFC boost converter followed by a DC-DC stage with isolation. Example of such applications are USB-PD, battery chargers or AC-DC adaptors.

Due to its hybrid nature forward/flyback [19], the asymmetrical half-bridge flyback is very appropriate for such applications and can fulfill the previously listed desired characteristics in an optimal way, making it especially suitable for high-density designs.

In order to demonstrate the potential size reduction of this topology, an example converter acting as DC-DC stage is dimensioned to provide 5 V to 48 V output and 5 A, with a turns-ratio N (primary to secondary) of 4.2 and a V_{bus} voltage of 380 V. Under these conditions, approximately 53% (NV_{out_max}/V_{bus}) of the energy is stored in the capacitor and transferred in a forward mode, resulting in less magnetic energy storage and therefore, smaller transformer compared to any flyback converter, where 100% of the energy is stored in the transformer. This is explained in more detail in [19] and [20].

In the next section, some general design rules will be presented and the loss mechanism in the different elements will be analyzed to obtain an estimation of the efficiency.

B. GENERAL DESIGN GUIDELINES FOR AHB FLYBACK

An example of the converter target requirements is shown in Table 1.

In high power density adaptors, it is desired to minimize the amount of power dissipated at any load, typically the worst case occurs at full load. This means that the efficiency needs to be optimized for the highest output power: 48 V/5 A at the given input voltage of 380 V. An accurate analytical model that finds such optimum point is complex, especially due to the multiple possible magnetics designs and their losses model complexity. Therefore, an iterative process

TABLE 1. Desired AHB flyback converter characteristics.

Parameter	Value
Input voltage range	120 V to 420 V (Vout dependent)
Output voltage range	5 V to 48 V
Maximum output current	5 A
Efficiency	Max@full load @ V_{in} = 380 V
Power density	>50 W/inch^3

over different component choices can further help to find the optimal dimensioning.

Based on the operation principle explained in [19] and [21], the next general design steps can be applied:

The turns-ratio (N) is the most important parameter in the design of this converter. It affects the secondary RMS currents and the reverse voltage to withstand by the output rectifier. A good starting point is to target 45% to 55% duty cycle at the nominal input voltage (V_{in_nom}) and maximum output voltage (V_{out_max}) to calculate N.

$$D \approx \frac{N V_{out\_max}}{V_{in\_nom}} \quad (1)$$

Using D = 53%, a turns-ratio of approximately 4.2 is obtained from (1). Using (2) the maximum reverse voltage in the secondary rectifier (V_{ds_SRmax}) can be calculated, which is especially important if a synchronous rectification switch is used to improve the efficiency, as in this case [22], [23], [24].

$$V_{ds\_SRmax} \approx \frac{V_{in\_max}}{N} \quad (2)$$

With the given maximum input voltage (V_{in_max}) of 420 V (worst case), 100 V is obtained from (2).

In the next step, the maximum (I_{hbh}) and the minimum (I_{hbl}) magnetizing current need to be estimated. The relation between the desired output current (I_{out}) and the current in the half-bridge can be approximated by (3) [19]:

$$I_{out} = \frac{N \left(I_{hb_h} + I_{hb_l} \right)}{2} \quad (3)$$

I_{hbl} is set to the minimum required negative current to achieve ZVS under full load conditions. This allows minimizing the peak-to-peak current (I_{hb_pp}). Its value depends on the C_{oss} of the used switches and the transformer primary inductance. Not only the primary switches C_{oss} (C_{oss_hs} and C_{oss_ls}) needs to be considered but as well, the C_{oss} of the synchronous rectification switch (C_{oss_SR}) in the secondary side [21], [22], [23], if present. The total primary equivalent capacitance (C_{p_eq}) to achieve ZVS is shown in (4).

$$C_{p\_eq} = \frac{C_{oss\_SR}}{N^2} + C_{oss\_hs} + C_{oss\_ls} \quad (4)$$

Based on experience, a good starting point is to use 20% to 25 % of I_{hbh} if Si MOSFETs are used and 15% in case of GaNs devices. Taking I_{hbl} = 15% of I_{hbh}, I_{hbh} =2.8 A and I_{hbl} = 0.42 A will be obtained.

In a next step, using the obtained value of I_{hbl}, the exact value of the transformer inductance ($L_p = L_{lk} + L_m$) can be calculated.

Assuming small variations of the resonant capacitor voltage (V_{cr}), the charge (T_c) and discharge (T_d) times (5) and (6) of the magnetizing transformer current can be used to obtain the switching period (T) from (7) [21]:

$$T_c = \frac{L_p}{V_{in} - V_{cr}} I_{hb\_pp} = \frac{L_p}{V_{in} - N V_{out}} I_{hb\_pp} \quad (5)$$

$$T_d = \frac{L_p}{V_{cr}} I_{hb\_pp} = \frac{L_p}{N V_{out}} I_{hb\_pp} \quad (6)$$

$$T = I_{hb\_pp} L_p \frac{V_{in}}{(V_{in} - N V_{out}) N V_{out}} \quad (7)$$

Equation (7) shows that the switching frequency ($F_{sw} = 1/T$) increases with higher input voltage (V_{in}). Based on the frequency range of the transformer magnetic core, the desired operating frequency is set to 250 kHz at the nominal input and output voltage. This way $L_p = 117\ \mu H$ is obtained.

Knowing L_p, the exact value of the required negative current to achieve ZVS can be calculated by matching the energy in L_p and to the parasitic capacitance associated to the half-bridge node (C_{p_eq}) for the worst case (V_{in_max}), this is shown in (8).

$$\frac{1}{2} L_p I_{hbl}^2 > C_{p\_eq} \left(V_{in\_max} \right) V_{in\_max}^2 \quad (8)$$

On the other hand, the negative current needs to be compensated with positive peak current as indicated by (3), therefore devices with lowest C_{oss} (and in particular low $C_{o(tr)}$ as explained in [25]) are desired. High peak-to-peak current (I_{hb_pp}) not only affects the amount of conductive losses but as well increases the magnetic losses.

To reduce conductive losses, switches with low R_{dson} and C_{oss} are desired. On the other hand, power switches show a dependency of the output capacitance C_{oss} with R_{dson}. Therefore, a tradeoff between both parameters needs to be achieved when choosing the devices. Considering the previous statements, Fig. 2 shows that wide bandgap devices, particularly those based on GaN technology [26], [27], are the closest to an ideal switch (zero ON resistance (R_{dson}) and parasitic capacitance $C_{o(tr)}$) and therefore the most suitable for this application.

The dependency of the losses with the required negative magnetizing current to achieved ZVS is complex to calculate. As described in [21], the temporal equations of the system do not have a numeric solution, therefore simulation can provide the value of the RMS and peak-to-peak currents to calculate conduction and magnetic losses respectively.

The transformer design requires a tradeoff between copper and magnetic losses, typically, the peak to peak flux needs to be selected according to the switching frequency. As example of design, the peak to peak flux is chosen to 200 mT and the peak flux to around 175 mT, avoiding high values which increase magnetic losses and the risk of saturation.
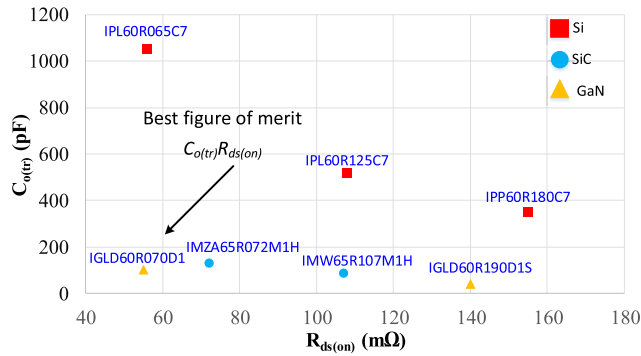
FIGURE 2. $C_{o(tr)}$ vs. $R_{ds(on)}$ parameters for different switches and technologies. GaN devices show the best figure $R_{ds(on)}C_{o(tr)}$.
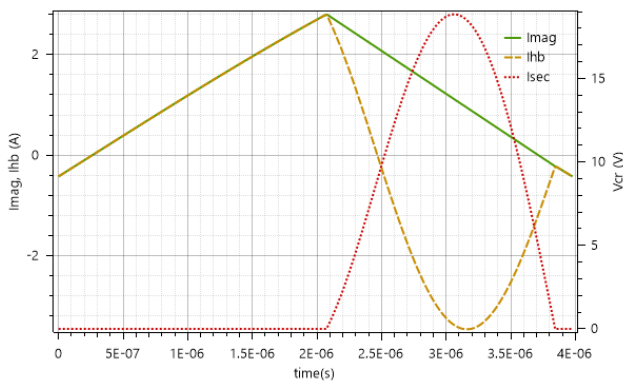
TABLE 2. Loss breakdown @380Vin.

Element	I_{rms}/Flux	$R_{ds(on)}$	P_{loss}
Input capacitor	0.926 A	250 mΩ	0.214 W
HS switch	1.137 A	190 mΩ	0.245 W
LS switch	1.578 A	190 mΩ	0.473 W
Shunt resistor	1.137 A	90 mΩ	0.116 W
Transformer primary	1.946 A	100 mΩ	0.378 W
Transformer secondary	8.85 A	5 mΩ	0.392 W
Magnetic core	-24 to 173 mT	3C95	0.775 W
SR	8.85 A	15 mΩ	1.175 W
Output capacitor	7.16 A	10 mΩ	0.512 W
Controller & driving	-	-	0.5 W
Efficiency			4.78 W => 98.04%

FIGURE 3. Simulated waveforms under the conditions: V_{in} = 380 V, V_{out} = 48 V, I_{out} = 5 A.

(a)

(b)

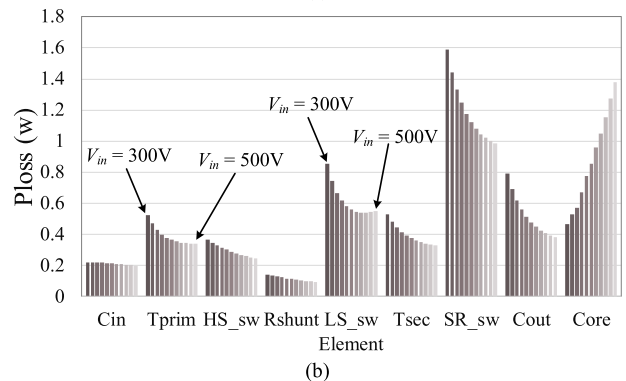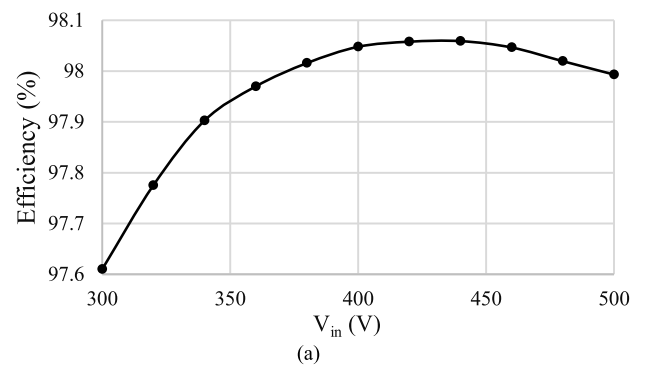**FIGURE 4.** (a) Calculated efficiency vs. input voltage, (b) components loss breakdown for different input voltages (V_{in}).

A core type EQ25 has been selected due to its small size and low profile. As calculated previously, the primary to secondary turns-ratio is 21:5 and the chosen ferrite material is 3C95 due to its low losses over temperature for the given operating (F_{sw}).

Finally, to minimize the RMS value of the currents at full load, the resonant capacitor (C_r) is adjusted to match the discharge time (ON time of the LS switch: T_{ls}) considering the transformer leakage inductance (L_{lk}), as shown in (9). The resulting waveforms would be similar to those in Fig. 3.

$$T_{ls} \approx \pi \sqrt{C_r L_{lk}} \qquad (9)$$

III. ESTIMATION OF THE CONVERTER EFFICIENCY

Assuming perfect ZVS and ZCS conditions, and therefore neglecting switching losses, the total losses of the converter consist of conductive losses in the different resistive elements, magnetic losses in the core of the transformer and control and driving losses. To calculate the first ones, the RMS currents and the resistance of each element are needed. For the second ones the volumetric losses and core size are required. The losses due to control and driving are estimated to be approximate 0.5 W.

The RMS values of the different elements can be extracted from simulations. Fig. 3 shows the simulated waveforms of the converter in steady state under the conditions: V_{in} = 380 V and V_{out} = 48 V / I_{out} = 5 A. I_{mag} represents the transformer magnetizing current and I_{hb} and I_{sec} the primary and secondary transformer currents respectively, both represented in Fig. 1.

To estimate the magnetic losses, the magnetic field (B) induced by the magnetizing current (I_{mag}) needs to be calculated as shown in (10), being A_e the
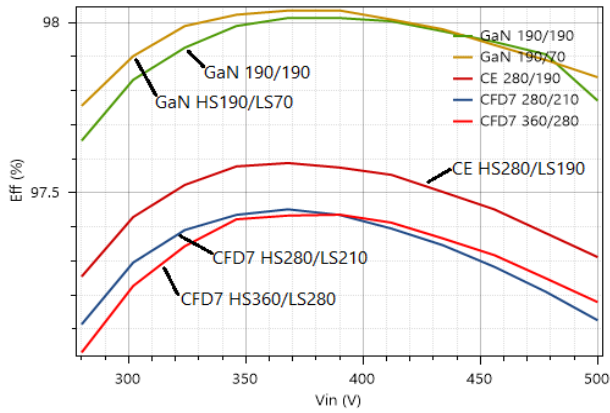
FIGURE 5. Calculated efficiency vs. input voltage for different devices and technologies (GaN and Si: CFD7 and CE) from Infineon.

TABLE 3. Main components of the converter prototype.

Element	Characteristics	Part number
Controller	AHB controller	XDPS2201 (modified)
Input capacitor	450V/47uF	450BXW47MEFR16X25
HS GaN	190mΩ/600V	IGLD60R190D1
LS GaN	190mΩ/600V	IGLD60R190D1
SR Mosfet	9.3mΩ/150V	BSC093N15NS5
Output capacitor	3x330uF/50V	A750MW337M1HAAE020

effective area of the core.

$$B(t) = \frac{I_{mag}(t)\, L_p}{A_e N} \tag{10}$$

The volumetric losses can be calculated using vendor specific tools or ferrite datasheet. When available, the Steinmetz coefficients and sinusoidal approximation can be used. The magnetic losses given in datasheet are typically based on homogenous distribution of the magnetic flux in a ring core, therefore an extra of 20% losses is added for non-homogenous distribution in specific ferrite core. Table 2 shows the loss breakdown in the different components under the simulated conditions shown in Fig. 3.

To better understand and optimize the converter, a numerical method has been developed. It iterates over the equations that define the converter [21] and extracts the currents required to calculate the resistive and magnetic losses under different conditions.

Fig. 4.a shows the efficiency over the input voltage and Fig 4.b shows the loss breakdown over input voltage ranging from 300 V to 500 V obtained with this method. The listed elements are: input capacitor (C_{in}), transformer primary winding (T_{prim}), high side switch (HS_sw), current sense resistor (R_{shunt}), low side switch (LS_sw), transformer secondary winding (T_{sec}), synchronous rectifier switch (SR_sw), output capacitor (C_{out}) and transformer core (Core).

TABLE 4. Transformer specification.

Element	Value
Core type	EQ25 (16mm height)
Core material	3C95
L_m	120 uH
L_{lk}	3 uH
N_p	21 turns (Litz 40 × 0.1 mm)
N_s	5 turns (TIW Litz 120 × 0.1 mm)
Winding interleaving	P-S-P
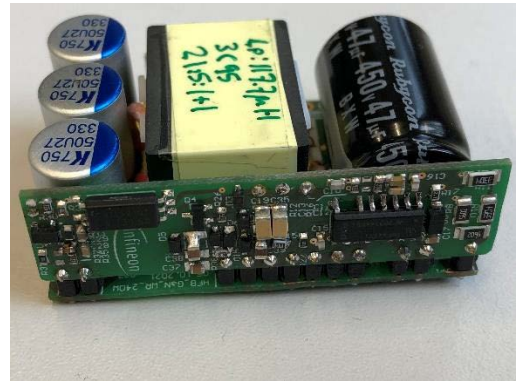
(a)
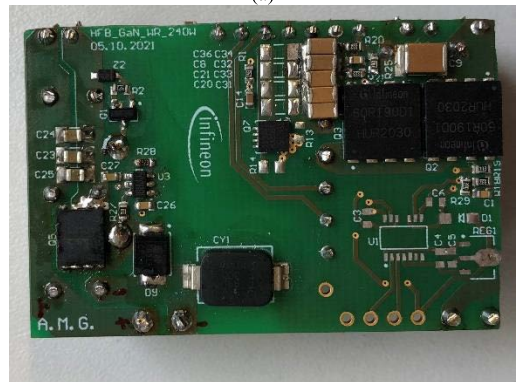
(b)

FIGURE 6. Top and back side view of the 240 W DC-DC GaN prototype. Size: 51 × 36 × 19 mm, power density: 112 W/inch^3.

It is clearly seen how the resistive losses dominate at low input voltage whereas magnetics losses in the core are dominant at higher input voltage due to the frequency increase and higher magnetizing current required to achieve ZVS.

The same method is used to evaluate different switches and input voltages to estimate the efficiency. Such method complements the general design rules explained before and helps finding the optimal design. Figure 5 shows the superior performance of the GaN devices compared to Silicon for the reasons previously explained.

IV. PROTOTYPE

Finally, a prototype has been built to support the theory. The dimensioning has been done accordingly to the presented
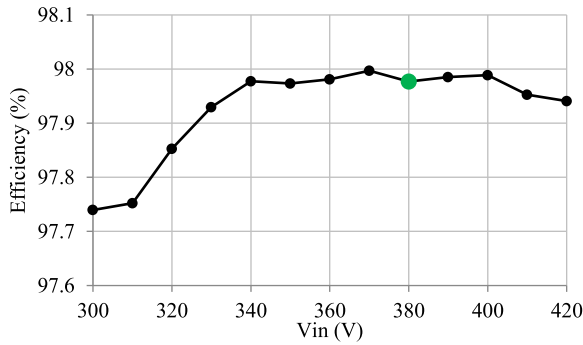
FIGURE 7. Full load (48 V / 5 A) efficiency versus input voltage, green dot mark the nominal input voltage.
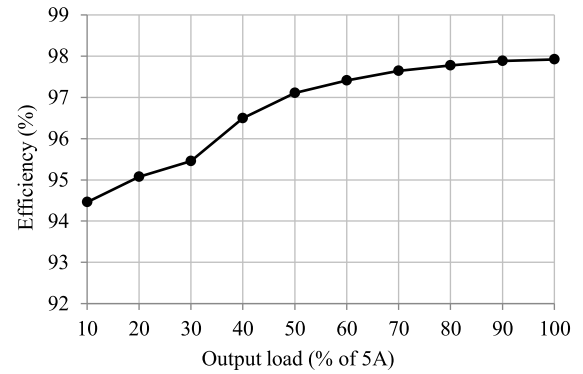

FIGURE 8. Full load oscilloscope waveforms showing V_{hb} ZVS operation.

FIGURE 9. Thermal picture of the components side at 380 V input voltage.

FIGURE 10. Efficiency vs. load @48 V output 380 V input.

FIGURE 11. Efficiency versus output voltage for I_{out} = 5 A.

guidelines and design optimization process to fulfill the requirements given in Table 1. The devices used in the final design are shown in Table 3.

Table 4 shows the transformer construction details.

Fig. 6 shows a picture of the prototype and Fig. 7 the measured efficiency at full load vs. input voltage, the measured efficiency follows the same pattern as the simulated efficiency in Fig. 4. The primary signal waveforms are shown in Fig. 8 where ZVS can be observed.

Fig. 9 shows the thermal behavior at full load under 380V input. As expected from the loss breakdown it can be

observed that the SR MOSFET is the hottest device in the design.

Finally, Fig. 10 and Fig. 11 show the efficiency versus load and output voltage respectively. Different control methods are applied depending on the output conditions (forced CCM at heavy load and DCM at light load) as explained in [21].

V. CONCLUSION

A GaN-based Asymmetrical Half-Bridge Fyback converter has been proposed as an isolated second-stage DC-DC converter for USB-PD EPR and battery chargers applications. The proposed topology combined with GaN switches technology achieves outstanding characteristics for such applications: high efficiency, high power density and wide output voltage range. A general method for dimensioning the converter has been presented and the results of a computational iterative method to optimize the final design has been shown.

The efficiency (98%) and power density (6.88 W/cm^3 or 112 W/inch^3) provided by the converter, thanks to the forward energy transfer mode, outperforms many other state-of-the-art topologies. Furthermore, the capabilities to provide wide input and output voltage range, thanks to the flyback energy transfer mode, makes the converter the optimal choice for battery charger and USB-PD EPR applications.

Wide band gap devices and in particularly GaNs, due to its low C_{oss} enabling low circulating current, are especially suitable for this topology. They can provide higher efficiency and a better performance than Si based devices.

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