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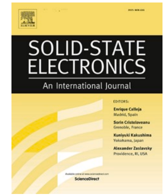

Performance of FDSOI double-gate dual-doped reconfigurable FETs

C. Navarro, L. Donetti, J.L Padilla, C. Medina, J. Ávila, J.C. Galdón, M. Recio, C. Márquez, C. Sampedro, F. Gámiz

Nanoelectronics Research Group, CITIC-UGR, University of Granada, Granada, Spain

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In this work, the electrical performance of a novel reprogrammable FDSOI device with dual-doping at source/drain and only two top gates is investigated through advanced 3D TCAD simulations. The static and dynamic operations are evaluated and compared with those of traditional Schottky barrier RFETs and standard 28 nm FDSOI MOS transistors under manufacturable geometries.

1. Introduction

Reconfigurable FETs (RFET), MOS-like devices whose polarity N or P can be in-situ decided through an adequate biasing scheme, are being investigated as a possible solution for custom reprogrammable logic designs [1]. A complete review of these devices can be found in [2]. Conventional RFETs present metallic NiSi source/drain (S/D) regions ensuring the availability of both holes and electrons when required. The use of close to mid-gap S/D metal workfunctions allows for similar electron/hole Schottky barriers (SB) to achieve symmetrical output currents. Besides the fabrication complexity of dealing with silicides and Schottky contacts, this approach generally suffers from limited driving currents as the carrier injection barriers cannot be reduced without altering the semiconductor material or the expected N/P current symmetry [3]. Recently, a three-gate RFET device based on S/D dual-doping (DD), i.e., the simultaneous presence of both N and P doped regions at source and drain, was proposed to improve many of the Schottky counterpart weaknesses [4]. The use of both N and P dopings within the same device can be found in several standard technologies like BJTs, gated P-I-N diodes (Field-Effect diodes and TFETs) [5,6,7], G4-FETs [8], or sharp switching FETs [9,10] among others. In this work, an analogous but simplified configuration with only two top gates and more pragmatic dimensions, aiming for 28 nm FDSOI technology, is evaluated and benchmarked through TCAD simulations with standard SB-RFETs and MOSFETs (Fig. 1).

2. Simulation details and RFET operation

Synopsys 3D-TCAD simulations [11] were conducted to test all fully depleted device structures (SB-RFETs, DD-RFETs, and standard N/P MOSFETs, Fig. 1). Poisson's, electron/hole continuity equations and density gradient were included by default. Room temperature (300 K) was maintained for the whole study. Fixed mobility was extracted from experimental results according to the S/D spacing [12]. Regardless of the considered device, all top gates workfunctions were set to 4.7 eV and feature P-type polysilicon doping. The substrate is N^+-type doped to form an effective ground plane as a back-gate terminal. For SB-RFETs, the WKB model and non-local path were considered together with optimistic tunneling effective masses, m_n*= 0.16 m_0 and m_n*= 0.19 m_0, lower than other SB-RFET studies [13]. The S/D metal workfunction was set to 4.65 eV to achieve N/P current symmetry. On the other side, a S/D doping of $N_{S/D} = 10^{21}$ cm^{-3} is present for DD-RFETs and MOS devices. The front-gates EOT were set to 1.5 nm, while the Si-film (Boron, $N_B = 10^{16}$ cm^{-3}) and BOX thicknesses were fixed to 7 and 25 nm, respectively. The physical width, W, was 0.2 µm while the total device length $L_{S/D}$ was around 145 nm. The width in DD-RFETs is shared between the N (W_N) and P ($W_P = W\text{-}W_N$) doped regions. RFET gates length, L_{PG} and L_{CG}, are fixed to 28 nm, while for MOS devices $L_{CG} = L_{S/D}$ with no polarity gate (PG).

RFETs operation is analogous regardless of the S/D material [3,4]. A control gate (CG) is responsible for modulating the current flow (device

E-mail address: carlosnm@ugr.es (C. Navarro).

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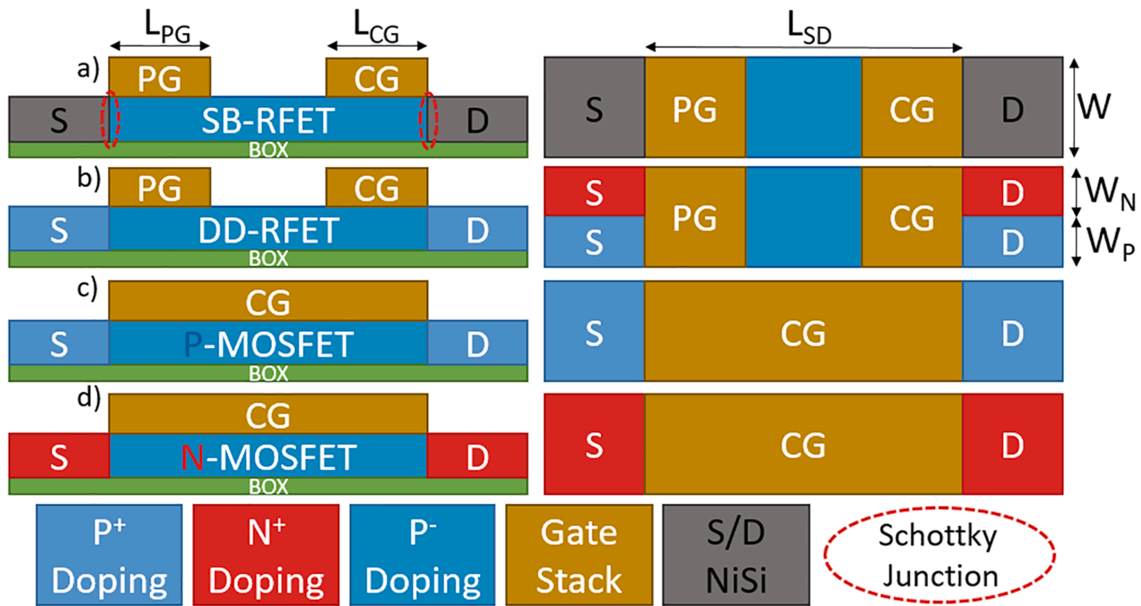

Fig. 1. Lateral (left) and top (right) views of a) SB-RFET, b) DD-RFET, c) P-MOS and d) N-MOS FDSOI devices. Note the dual N/P doped regions at S/D in b).

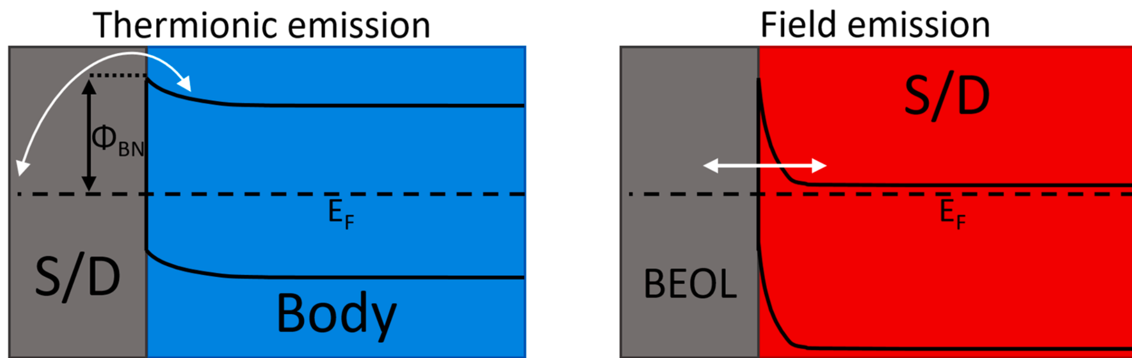

Fig. 2. Main carrier injection mechanisms for left) SB-RFET, thermionic emission from S/D to channel; and right) DD-RFET/MOSFET, field emission from BEOL to S/D. The picture represents the electron injection case.

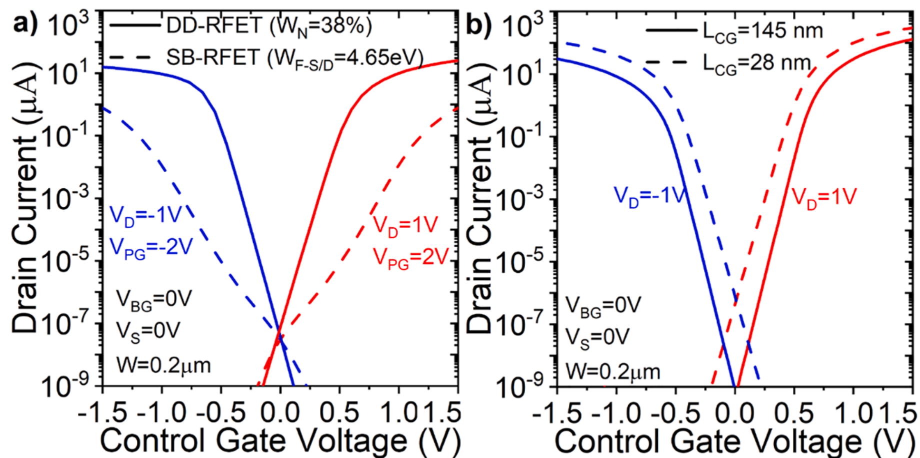

Fig. 3. I_D-V_{CG} comparison for a) RFETs and b) regular MOS transistors. 28 nm MOSFETs in b) shown for reference.

ON/OFF) while one or more PG are responsible for selecting the transport carrier (N/P flavor). Polarity gates enable the unipolar conduction during the OFF state and represent the key difference with respect to analogous devices like SB-MOSFETs. The main difference between SB- and DD-RFETs is, other than the S/D topology, the carrier injection mechanism (Fig. 2). The former mostly relies on thermionic emission, where carriers must surmount the top of the Schottky barrier, from the NiSi metallic S/D towards the channel with barriers approximately

Table 1
$V_D = \pm 1$ V, $V_{PG} = \pm 2$ V, $V_{BG} = V_S = 0$ V and W = 0.2 μm. a) W_N = 38%. b) $W_{F\text{-}S/D}$ = 4.65 eV. c) $L_{S/D}$ = 145 nm. ★: $I_{ON} = I_D$ ($V_{CG} = \pm 1$ V). ●: $I_{OFF} = I_D$ ($V_{CG} = 0$ V).

	DD-RFET[a]	SB-RFET[b]	MOSFET[c]
$I_{ON-N}(\mu A)^{\star}$	9.6	0.011	30.1
$\|I_{ON-P}(\mu A)\|^{\star}$	9.3	0.011	8.5
$I_{OFF-N}(pA)^{\bullet}$	0.076	0.030	< 0.001
$\|I_{OFF-P}(pA)\|^{\bullet}$	0.036	0.029	< 0.001
$SS_N(mV/dec)$	81	216	65
$\|SS_P(mV/dec)\|$	75	205	65

equal to half the semiconductor band-gap ($\Phi_{BN} + \Phi_{BP} = E_g$). The latter is based on field emission, where carriers tunnel through the energy barrier, from the back-end of line metal contacts (not illustrated in Fig. 1) to the heavily-doped S/D regions ensuring an unimpeded transfer of majority carriers [14], i.e. an ohmic contact.

3. Static characteristics

The drain current as a function of the control gate voltage curves (I_D-V_{CG}) are compared in Fig. 3 for all the analyzed devices. When present, the PG voltage is fixed to ± 2 V. Note the remarkable difference between reconfigurable devices with metallic or dual doping S/D terminals. A difference of three orders of magnitude, in line with previous studies [4], is found for the ON current even with favorable tunneling masses in the case of the SB-RFETs. The benefit of Schottky contacts resulting from the injection of both carriers is also the origin of the limited driving current: symmetrical N/P currents imply large Schottky barriers for both carriers. Table 1 summarizes the main static parameters highlighting the anticipated poor current performance of SB-RFETs. These results are worse than those for the three-gate RFETs due to the reduced electrostatic control over the channel [3,4]. As expected, regular MOSFETs exhibit the best characteristics with larger ON currents, reduced OFF currents, and close to ideal subthreshold regimes (≈60 mV/dec). Notice that the DD-RFET P ON current is similar with respect to P-MOSFETs due to the larger V_{PG} in RFETs. The influence of this PG bias on reconfigurable devices can be inferred from Fig. 4, where the ON and OFF currents are compared. DD-RFET ON current is systematically larger than for SB-RFETs no matter V_{PG}, though they show a larger dependence on this parameter. The steep rise in the OFF current at low $|V_{PG}|$ is related to the ambipolar transport, a known issue in analogous devices such as SB-MOSFETs. Separately, the back-gate terminal can enhance the channel conduction and allow a better control of the ambipolarity at the expense of poorer switching characteristics: larger OFF-currents and subthreshold swings (SS), Fig. 5. Fig. 6 shows the RFETs ON current as a function of the parameter that modulates the RFET N/P current symmetry: W_N and $W_{F\text{-}S/D}$ for dual doped and Schottky barrier RFETs, respectively. A $W_{F\text{-}S/D}$ of 4.65 eV (as in [3]) results in symmetric currents for SB-RFETs while the N-doping width is set to W_N = 38%, wider than in [4] due to the change in the gate polysilicon and substrate doping species. From the manufacturing point of view, SB-RFETs are much

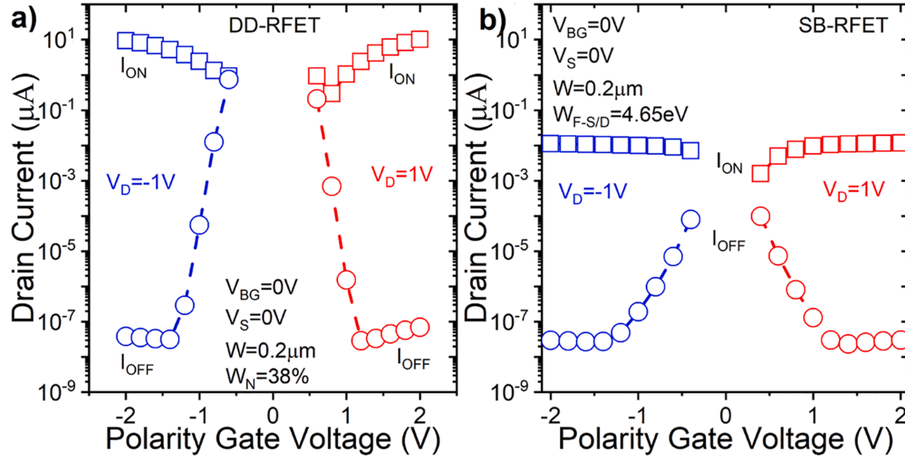

Fig. 4. ON and OFF currents for a) DD-RFETs and b) SB-RFETs as a function of the polarity gate voltage (V_{PG}). $I_{ON} = I_D$ ($V_{CG} = \pm 1$V). $I_{OFF} = I_D$ ($V_{CG} = 0$ V).

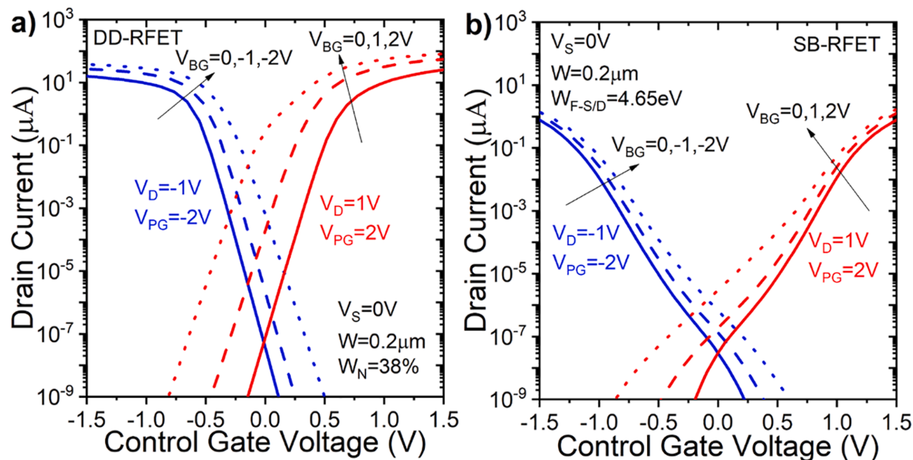

Fig. 5. I_D-V_{CG} comparison at different back-gate voltages (V_{BG}). a) DD-RFETs and b) SB-RFETs.

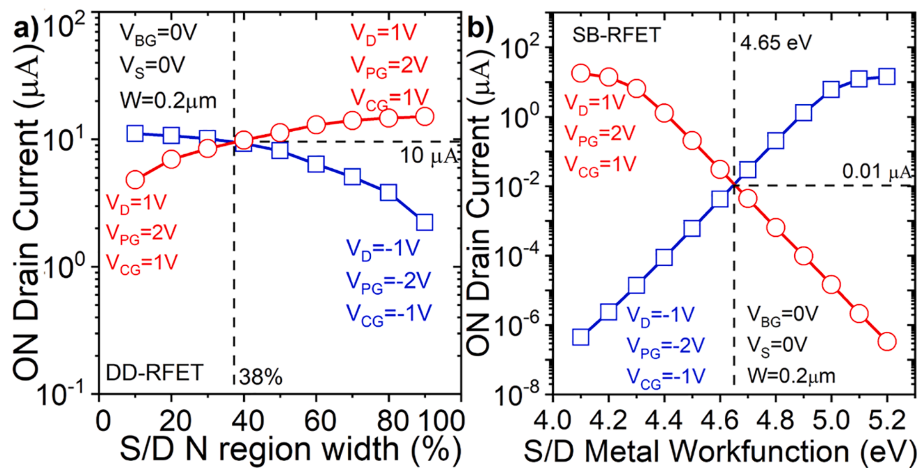

Fig. 6. Current symmetry modulation through a) the source/drain N doped region width, W_N, and b) the source/drain metal workfunction, $W_{F\text{-}SD}$.

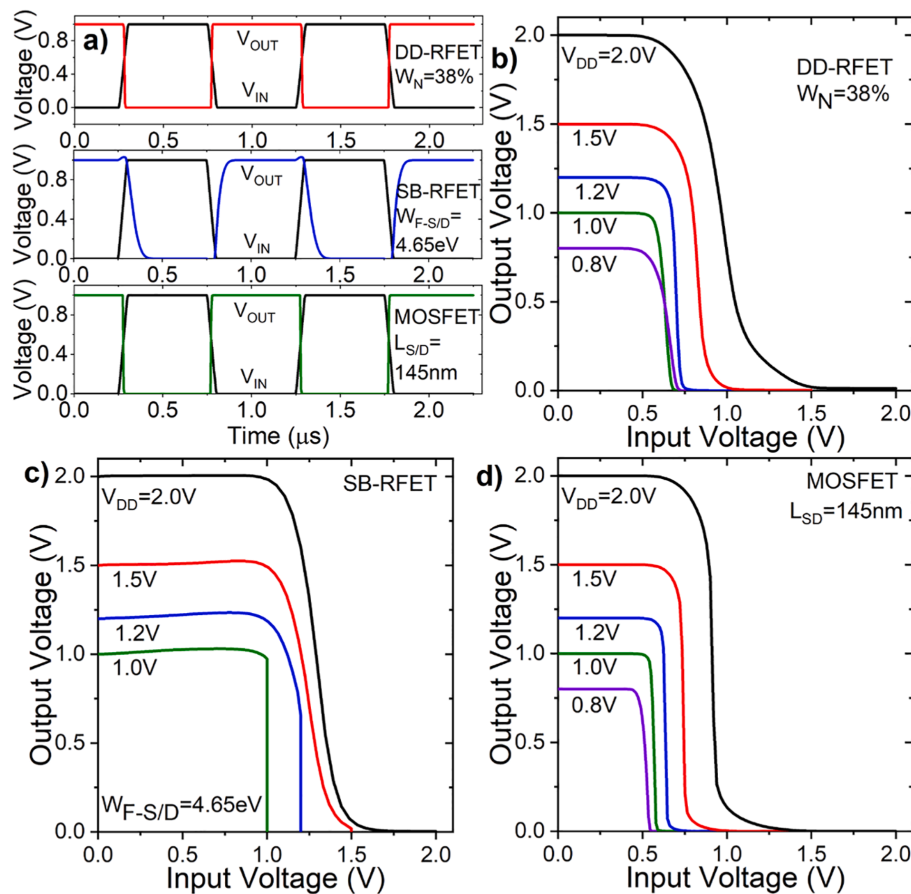

Fig. 7. a) Inverter transient response and b-d) VTC curves for b) DD-RFETs, c) SB-RFETs and d) MOSFETs. f = 1 MHz and C_{out} = 0.3fF. t_r/t_f = 0.1 µs.

more prone to suffer from serious variability issues: the ON current dependence (the slope) is more accentuated with the S/D workfunction than with the doping width. Besides, the technical complexity of introducing exotic materials, dealing with potential challenges as the Fermi-Level pinning, and including addition processing steps is not comparable to defining widths through layout mask designs in the case of DD-RFETs. On the positive side, SB-RFETs feature fewer fabrication steps with no random dopant fluctuations (no S/D implantation) and lower thermal budget (doping activation or S/D epitaxy to reduce the device series resistance).

4. Dynamic operation

The dynamic operation is evaluated via 3D mixed-mode simulations of a standard CMOS logic inverter. A capacitor at the output (C_{out}) of 0.3 fF models the following logic stage parasitic capacitances [15]. This output capacitance represents the equivalent gate capacitance of an RFET inverter connected as the following stage. This value should be increased according to the expected load and parasitics. RFET PGs are biased to V_{DD} and ground for the pull-down/up network, respectively, to form the inverter. The density gradient quantization correction is neglected to reduce convergence issues. Fig. 7 shows the transient time

switching evolution at $V_{DD} = 1$ V and the voltage transfer characteristic (VTC) for different power supplies. At only 1 MHz, the DD-RFET already exhibits faster and more symmetric switching than Schottky RFETs with the MOSFET inverters being the steepest. The degraded dynamic operation in SB-RFET is related to the much lower current rather than to the capacitances as they are very close to DD-RFETs (not shown).

5. Conclusions

This work confirms the viability and interest of pursuing dual doped reconfigurable devices in 28 nm FDSOI technology. The transition from an aggressively optimized 3-gate structure to a more practical 2-gate design does not jeopardize the operation being the performance is slightly degraded. These novel devices present improved static and dynamic operation, limited contact variability, and reduced fabrication efforts in comparison to their Schottky barrier equivalent. Although standard MOSFETs exhibit overall better performance, easier layout routing and reduced footpring, dual doped RFETs are still appealing as a possible solution for non-high-end on-the-fly reprogrammable logic.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgements

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References

[1] Heinzig A, Slesazeck S, Kreupl F, Mikolajick T, Weber WM. Reconfigurable Silicon Nanowire Transistors. Nano Lett 2012;12(1):119–24.
[2] Mikolajick T, Galderisi G, Simon M, Rai S, Kumar A, Heinzig A, et al. 20 Years of reconfigurable field-effect transistors: From concepts to future applications. Solid State Electron 2021;186:108036.
[3] Navarro C, Barraud S, Martinie S, Lacord J, Jaud M-A, Vinet M. Reconfigurable field effect transistor for advanced CMOS: Advantages and limitations. Solid State Electron 2017;128:155–62. https://doi.org/10.1016/j.sse.2016.10.027.
[4] Navarro C, Marquez C, Navarro S, Gamiz F. Dual PN Source/Drain Reconfigurable FET for Fast and Low-Voltage Reprogrammable Logic. IEEE Access 2020;8: 132376–81. https://doi.org/10.1109/ACCESS.2020.3009967.
[5] Manavizadeh N, Raissi F, Soleimani EA, Pourfath M, Selberherr S. Performance assessment of nanoscale field-effect diodes. IEEE Trans Electron Dev 2011;58(8): 2378–84. https://doi.org/10.1109/TED.2011.2152844.
[6] Navarro C, Bawedin M, Andrieu F, Cluzel J, Cristoloveanu S. Electrical characterization of FDSOI by capacitance measurements in gated p-i-n diodes. IEEE Trans Electron Dev 2016;63(3):982–9. https://doi.org/10.1109/TED.2016.2520521.
[7] Ionescu AM, Riel H. Tunnel field-effect transistors as energy- efficient electronic switches. Nature 2011;479(7373):329–37. https://doi.org/10.1038/nature10679.
[8] Akarvardar K, Cristoloveanu S, Bawedin M, Gentil P, Blalock BJ, Flandre D. Thin film fully-depleted SOI four-gate transistors. Solid- State Electron 2007;51(2): 278–84. https://doi.org/10.1016/j. sse.2007.01.013.
[9] Navarro S, Navarro C, Marquez C, El Dirani H, Galy P, et al. Experimental demonstration of operational Z^2-FET memory matrix. IEEE Electron Device Lett 2018;39(5):660–3. https://doi.org/10.1109/LED.2018. 2819801.
[10] Navarro C, Navarro S, Marquez C, Padilla JL, Galy P, Gamiz F. 3-D TCAD study of the implications of channel width and interface states on FD-SOI Z^2-FETs. IEEE Trans Electron Devices 2019;66(6):2513–9. https://doi.org/10.1109/TED.2019.2912457.
[11] Synopsys Sentaurus Device User Guide (O-2018.06), Synopsys Inc.
[12] DeSalvo B, Morin P, Pala M, Ghibaudo G, Rozeau O, Li Q, et al. A mobility enhancement strategy for sub-14 nm power-efficient FDSOI technologies. pp. 7.2.1–7.2.4. In: IEDM Tech Dig.; 2014. https://doi.org/10.1109/IEDM.2014.7047002.
[13] Trommer J, Heinzig A, Slesazeck S, Mikolajick T, Weber WM. Elementary Aspects for Circuit Implementation of Reconfigurable Nanowire Transistors. IEEE Electron Device Lett 2014;35(1):141–3. https://doi.org/10.1109/LED.2013.2290555.
[14] Sze SM. Physics of Semiconductor Devices. NJ, USA, Wiley: Hoboken; 2006.
[15] De Marchi M, Sacchetto D, Zhang J, Frache S, Gaillardon P-E, Leblebici Y, et al. Top–Down Fabrication of Gate-All-Around Vertically Stacked Silicon Nanowire FETs With Controllable Polarity. IEEE Trans Nanotechnol 2014;13(6):1029–38.