IEEE Access
Multidisciplinary ⁝ Rapid Review ⁝ Open Access Journal

Received May 31, 2020, accepted June 20, 2020, date of current version July 2, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3004440

Non-Linear Capacitance of Si SJ MOSFETs in Resonant Zero Voltage Switching Applications

MANUEL ESCUDERO[1], MATTEO-ALESSANDRO KUTSCHAK[1], NICO FONTANA[1], NOEL RODRIGUEZ[2], AND DIEGO PEDRO MORALES[2]

[1]Infineon Technologies Austria AG, 9500 Villach, Austria
[2]Department of Electronics and Computer Technology, University of Granada, 18071 Granada, Spain

Corresponding author: Manuel Escudero (manuel.escuderorodriguez@infineon.com)

ABSTRACT The parasitic capacitances of modern Si SJ MOSFETs are characterized by their non-linearity. At high voltages the total stored energy $E_{oss}(V_{DC})$ in the output capacitance $C_{oss}(v)$ differs substantially from the energy in an equivalent linear capacitor $C_{oss(tr)}$ storing the same amount of charge. That difference requires the definition of an additional equivalent linear capacitor $C_{oss(er)}$ storing the same amount of energy at a specific voltage. However, the parasitic capacitances of current SiC and GaN devices have a more linear distribution of charge along the voltage. Moreover, the equivalent $C_{oss(tr)}$ and $C_{oss(er)}$ of SiC and GaN devices are smaller than the ones of a Si device with a similar $R_{ds,on}$. In this work, the impact of the non-linear distribution of charge in the performance and the design of resonant ZVS converters is analyzed. A Si SJ device is compared to a SiC device of equivalent $C_{oss(tr)}$, and to a GaN device of equivalent $C_{oss(er)}$, in single device topologies and half-bridge based topologies, in full ZVS and in partial or full hard-switching. A prototype of 3300 W resonant LLC DCDC converter, with nominal 400 V input to 52 V output, was designed and built to demonstrate the validity of the analysis.

INDEX TERMS Hard-switching, non-linear capacitance, resonant converter, wide band gap, zero voltage switching.

NOMENCLATURE

C_{ds}	Drain to source capacitance.
C_{gd}	Gate to drain capacitance.
C_{gs}	Gate to source capacitance.
C_{iss}	Input capacitance. C_{gs} plus C_{gd}.
$C_{oss,1}$	Output capacitance of the device turning-on in a half-bridge.
$C_{oss,2}$	Output capacitance of the device turning-off in a half-bridge.
$C_{oss(er)}$	Effective output capacitance, energy related.
$C_{oss(tr)}$	Effective output capacitance, time related.
C_{oss}	Output capacitance. C_{ds} plus C_{gd}.
E_{ind}	Energy stored in the series inductor.
$E_{ind,1}$	Required stored energy in single device topologies.
$E_{ind,2}$	Required stored energy in single device topologies starting at higher voltage than V_{DC}.
$E_{ind,3}$	Required stored energy in single device topologies starting at voltage lower than V_{DC}.
$E_{ind,4}$	Required stored energy for charging $C_{oss,2}$.
$E_{ind,5}$	Total required stored energy in half-bridge topologies.
$E_{ind,linr,1}$	Required stored energy in single device topologies for linear capacitances.
$E_{ind,linr,2}$	Required stored energy in single device topologies starting at voltage higher than V_{DC} for linear capacitances.
$E_{ind,linr,3}$	Required stored energy in single device topologies starting at voltage lower than V_{DC} for linear capacitances.
E_{oss}	Stored energy in the C_{oss}.
$E_{oss,linr}$	Stored energy in a linear C_{oss}.
i_{ch}	Channel current.
i_d	Drain current.
i_{dg}	Drain to gate current.
i_{ds}	Drain to source current.
L_r	Series resonant inductor.
Q_{gd}	Stored charge in C_{gd}.
Q_{oss}	Stored charge in C_{oss}.
$V_{gs,max}$	Maximum induced gate to source voltage by the Miller feedback effect.
$V_{G,off}$	Turn-off driving voltage.

The associate editor coordinating the review of this manuscript and approving it for publication was Francesco Della Corte.

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

V_{Miller}	Miller-Plateau voltage.
$R_{ds,on}$	Drain to source on-state resistance.
R_g	Integrated gate resistance.
$R_{g,off}$	Turn off gate resistance.
R_s	Series resistance.
V_{DC}	Nominal voltage of the converter's supply.
V_{ds}	Drain to source voltage.
V_{end}	Final supply voltage.
V_{start}	Initial supply voltage.
V_{supply}	Converter's supply voltage.
V_{th}	Gate threshold voltage.
$\Delta E_{loss,tot}$	Total energy loss in the hard-switched turn-on transition of a half-bridge.
$\Delta E_{loss,t,linr}$	Total energy loss in the hard-switched turn-on transition of a half-bridge for linear capacitances.
$\Delta E_{loss,2}$	Energy lost in the hard-switched charge of $C_{oss,2}$.
$\Delta E_{loss,2,linr}$	Energy lost in the hard-switched charge of $C_{oss,2}$ for linear capacitances.
$\Delta E_{supply,2}$	Supplied energy for the hard-switched charge of $C_{oss,2}$.
$\Delta E_{supply,2,linr}$	Supplied energy during the hard-switched. charge of $C_{oss,2}$ for linear capacitances.
ΔQ	Variation of stored charge.
ΔV_{supply}	Variation in the supply voltage.

I. INTRODUCTION

The development of Switched Mode Power Supplies (SMPS) continuously moves towards improvements in efficiency, volume and cost, which can be observed in the trend of high efficiency standards, like the Climate-Savers-Computing Initiative (CSCI) [1] or the 80 PLUS qualification program [2], with increasing requirements extending also to light load operation. The efficiency, volume and cost are parameters of performance closely interdependent in the design of SMPS [3], [4]. The improvements in one of the parameters often implies a negative impact in one or, often, several of the other ones. It is only through new design paradigms or technology breakthroughs that it is possible to push further the limits in terms of efficiency, volume, cost or the overall performance of power converters.

One of the key design paradigms in modern high-efficiency SMPS is the reduction or the elimination of the switching losses in the power semiconductors devices, which has limited traditionally the maximum switching frequencies and, consequently, the maximum power density of the converter. The switching losses can be reduced limiting the overlap of current and voltage during the switching transitions by one of these means: turning the switch at Zero Voltage (ZVS), at Zero Current (ZCS) or a combination of both. The ZVS turn-on of High Voltage (HV) devices is especially beneficial because the high amount of energy stored in the parasitic capacitances would be otherwise lost [5]–[7]. The ZVS can be achieved discharging and charging the parasitic capacitances in a lossless manner prior to the switching transition.

The charge and discharge of a capacitor can be near lossless when the energy is transferred from an inductor and such transfer is not resistively limited. This can be considered true when the charge and discharge transient is underdamped: the RC time constant of the circuit is several orders of magnitude smaller than the time constant of the LC resonance [8], [9]. This property is the key attribute in the so-called resonant and quasi-resonant converters, all of which comprise at least one inductor, which charges and discharges the parasitic capacitances of the switches in a resonant manner. Apparently, in some cases a variable series resistance within the output capacitance of power semiconductor devices may limit resistively its charge and discharge causing additional losses that will not be analyzed in this work [10].

Commonly used resonant converter topologies may comprise one single switching device or several of them, stacked in pairs and conforming one or several building blocks, so-called half bridges. Examples of single switch resonant or quasi-resonant topologies are the fly-back and its variants [11], and the Critical Conduction Mode (CrCM) [12] boost converter. For high-power applications are common two switch topologies, like the Transition Conduction Mode (TCM) [13] boost converter and the half-bridge LLC [14], and four switch topologies, like the Phase Shift Full Bridge (PSFB) [15], [16], the Dual Active Bridge (DAB) [17] and the full-bridge LLC. The general analysis in this work will be applied to the two basic scenarios, a single device and a half-bridge (or stacked devices), which can be conveniently extended to any of the above-mentioned topology examples.

Another key design paradigm in modern high-efficiency SMPS is the reduction of switching losses by the improvement of the characteristics of the switching device itself. Silicon (Si) based power switching devices have continuously improved their Figure Of Merit (FOM) becoming closer and closer to the theoretical limit of the material itself [18], [19]. Frequently, the improvement of the FOM implies certain side effects on the device characteristics, e.g. the distribution of charge in the parasitic capacitance along the blocking voltage becomes highly non-linear (Fig. 1). The non-linear distribution of charge in the output capacitance of modern Super Junction (SJ) MOSFETs allows the total stored energy to be much less of what would be stored in an equivalent linear capacitor with the same amount of charge $C_{oss(tr)}$ (Fig. 2). This divergence requires the definition of an additional energy related equivalent linear capacitor $C_{oss(er)}$ (Fig. 3), which would store the same amount of energy than the non-linear output capacitance of the semiconductor switch. The equivalent $C_{oss(tr)}$ and $C_{oss(er)}$ (1-4) have been previously defined in the literature [20] and are commonly available in the datasheet of commercial devices.

$$Q_{oss}(V_{DC}) = \int_0^{V_{DC}} C_{oss}(v)dv \quad (1)$$

$$C_{oss(tr)}(V_{DC}) = \frac{Q_{oss}(V_{DC})}{V_{DC}} \quad (2)$$

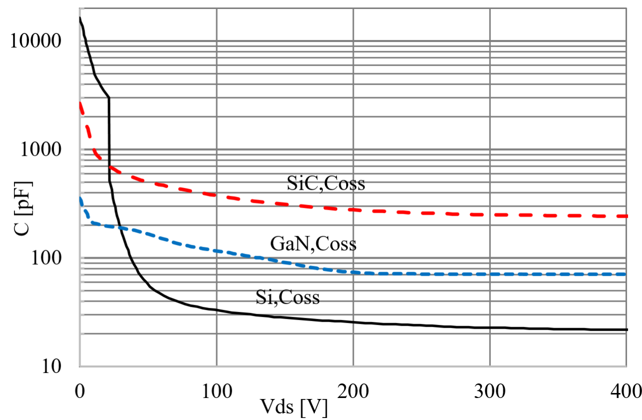

FIGURE 1. IPP60R170CFD7 (Si), IMZA65R027M1H (SiC) and IGT60R070D1 (GaN) typical output capacitances C_{OSS}. Data extracted from the datasheets of the devices.

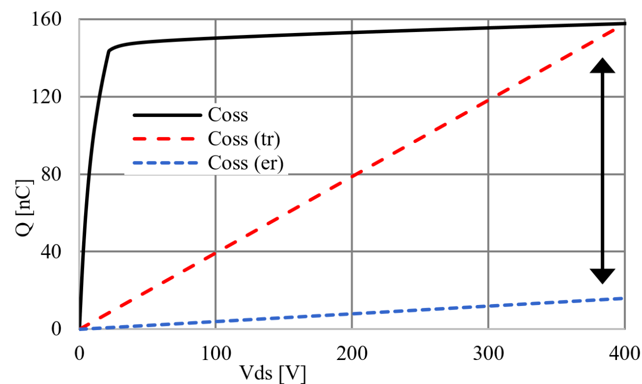

FIGURE 2. Si typical stored charge in its C_{OSS} and the stored charge in an equivalent $C_{oss(tr)}$ and an equivalent $C_{oss(er)}$.

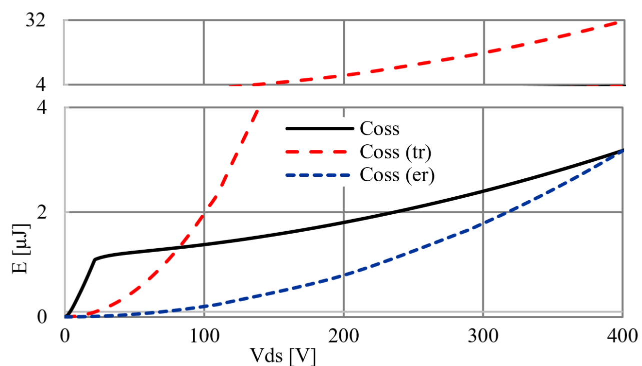

FIGURE 3. Si typical stored energy in C_{OSS} and the stored energy in an equivalent $C_{oss(tr)}$ and in an equivalent $C_{oss(er)}$.

$$E_{oss}(V_{DC}) = \int_0^{Q_{oss}(V_{DC})} v dq = \int_0^{V_{DC}} v \cdot C_{oss}(v) dv \quad (3)$$

$$C_{oss(er)}(V_{DC}) = \frac{2E_{oss}(V_{DC})}{V_{DC}^2} \quad (4)$$

Moreover, the commercial availability of switching devices made of Wide Band Gap (WBG) semiconductor materials promises to bring a considerable leap in performance in power converters [21]–[23]. Currently, the most promising technologies are Silicon Carbide (SiC) MOSFETs and Gallium Nitride (GaN) HEMTs. The devices made of WBG semiconductors can have parasitic capacitances several orders of magnitude smaller than a Si device with similar $R_{ds,on}$. Furthermore, the distribution of charge along the voltage of currently available WBG devices is more linear than the distribution of charge in Si devices (Fig 1). It can be observed in Fig. 4 and Fig. 5 that the equivalent $C_{oss(tr)}$ and $C_{oss(er)}$ for SiC and GaN technologies do not diverge as much as in the Si example.

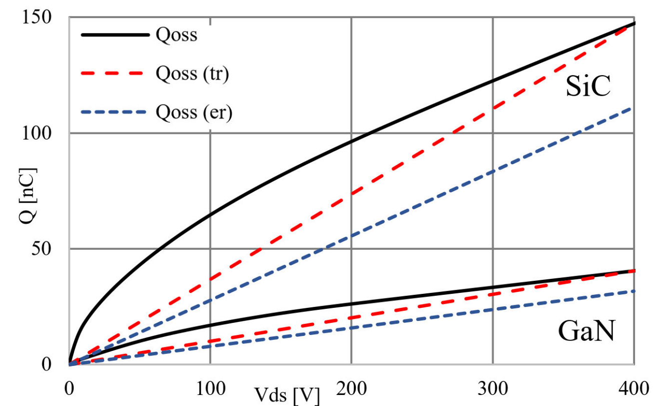

FIGURE 4. SiC and GaN typical stored charge in its C_{OSS} and the stored charge in an equivalent $C_{oss(tr)}$ and an equivalent $C_{oss(er)}$.

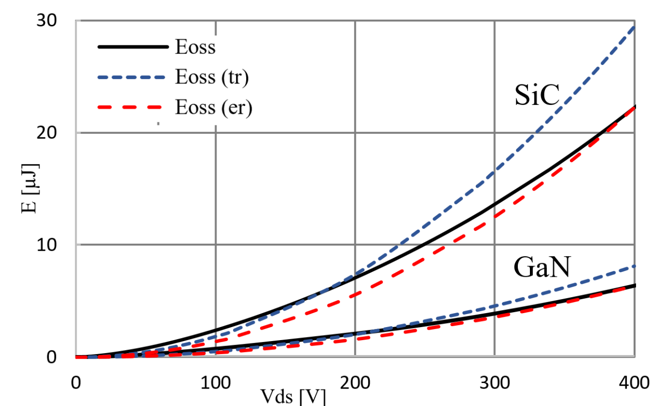

FIGURE 5. SiC and GaN typical stored energy in their C_{OSS} and the stored energy in an equivalent $C_{oss(tr)}$ and in an equivalent $C_{oss(er)}$.

In this work the impact on the performance and design of resonant converters originated by the absolute stored charge within the parasitic output capacitance and its distribution along the voltage excursion is analyzed. This works aims to bring further insights in the behavior of the power switches' non-linear capacitances in resonant converters, to extend and complete the analysis presented in [5] and [20]. Moreover, this works includes the analysis of single device and half-bridge device topologies.

For the sake of a meaningful comparison of their output capacitances, a Si SJ MOSFET (IPP60R170CFD7) [24] is

compared to a SiC MOSFET (IMZA65R027M1H) [25] with nearly equal total stored charge, and compared to a GaN HEMT (IGT60R070D1) [26] of nearly equal total stored energy. A summary of the main characteristics of the devices is listed in Table 1. For the sake of simplicity, only the parasitic capacitances of the device itself will be considered in the following analysis: the effects of the packaging, the heat-sink mounting or the PCB layout will be omitted. In the following, the compared devices will be referred simply as Si, SiC and GaN unless otherwise noted.

TABLE 1. Summary of device characteristics.

	IPP60R170CFD7	IMZA65R027M1H	IGT60R070D1
$R_{DS,on}$	144 mΩ @ 25 °C	27 mΩ @ 25 °C	55 mΩ @ 25 °C
Q_{oss}	157 nC @ 400 V	147 nC @ 400 V	40.5 nC @ 400 V
E_{oss}	3.18 µJ @ 400 V	29.46 µJ @ 400 V	8.10 µJ @ 400 V
Q_{gd}	3.18 nC @ 400 V	12.2 nC @ 400 V	2.08 nC @ 400 V
C_{gs}	1208 pF	2114 pF	380 pF
R_g	10.9 Ω	3 Ω	0.78 Ω
V_{th}	4 V	4.5 V	1.2 V

The rest of this work is organized as follows. In Section II, the required initial stored energy in the resonant inductor to achieve full ZVS in single and half-bridge based topologies is analyzed. In Section III, the impact on the losses of partial or full hard switching in single and half bridge based topologies is analyzed. In Section IV, the impact of the parasitic capacitance characteristics on the dv/dt during hard-switched turn-off and the impact on the losses of purposely decreasing the maximum dv/dt is analyzed. In Section V, the analysis is verified experimentally on a 3.3 kW half-bridge LLC DCDC converter prototype with nominal 400 V input and wide range output: 43.5 V – 59.5 V. Finally, in Section V the conclusions of this work are summarized.

II. ANALYSIS OF ZERO VOLTAGE SWITCHING ENERGIES

A. SINGLE DEVICE TOPOLOGIES

For the sake of generality in the analysis, a single device resonant converter during the switching transition is represented by the simplified equivalent circuit in Fig. 6. In this simplified circuit there is a capacitor C_1 that stands for the equivalent output capacitance C_{oss} of the power switch. The inductor L_r stands for a discrete auxiliary resonant inductance or other equivalent inductances in the circuit (e.g. the leakage of a transformer), which provides the initial energy for the ZVS transition. An equivalent series resistor R_s stands for all of the series resistances along the charging and discharging path.

In its initial state the switch is off or in its blocking state, and the output capacitor C_{oss} is charged-up to a starting voltage V_{DC} equal to the voltage in V_{supply}. Because the drain to source voltage V_{ds} equals to the supply voltage V_{DC}, the circuit is stable and would remain in this state indefinitely unless there is a certain initial energy E_{ind} in the inductor that forces the output charge Q_{oss} out of C_{oss} and into V_{supply}. Thanks to that initial energy (E_{ind}) the capacitor C_{oss} would

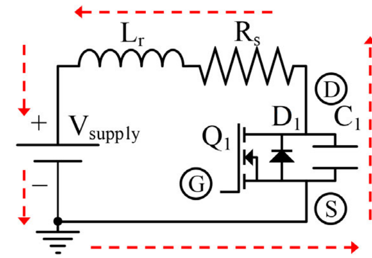

FIGURE 6. Simplified circuit for the analysis of the resonant discharge of the output capacitance of the power switch in a single device topology.

be effectively discharged and with zero stored energy (E_{oss}) at the end of the transition, enabling a ZVS turn-on. Like a transfer between two capacitors in series, the total amount of charge that is transferred corresponds to the initial amount of charge in the smallest of the capacitors, which is C_{oss} in this scenario. Because C_{oss} is a non-linear capacitor the total amount of charge in C_{oss} when it is charged up to a voltage V_{DC} is referred as $Q_{oss}(V_{DC})$.

Although less lossy than a purely resistively limited charging, the resonant charge and discharge of C_{oss} still causes conductive losses due to the required circulating currents passing through the circuit and its equivalent series resistance R_s. Notice that the related conductive losses would be proportional to the square of the current passing through the circuit, while the required ZVS current is proportional to the square root of E_{ind} and inversely proportional to the square root of the resonant inductor L_r.

Continuing with the simile of the two capacitors in series, assuming V_{supply} to be a linear capacitor, the amount of energy that is stored in it because of the charge ΔQ that has been transferred from C_{oss}, can be calculated with (5). Because we can safely assume the capacitance of V_{supply} to be much bigger than the equivalent capacitance of C_{oss}, we can neglect the variation of voltage ΔV_{supply} in equation (5) and simplify the expression into (6).

$$\Delta E_{supply} = \Delta Q \cdot \frac{V_{end} + V_{start}}{2} = \Delta Q \cdot \frac{\left(V_{DC} + \Delta V_{supply}\right) + V_{DC}}{2} \quad (5)$$

$$\Delta E_{supply} = Q_{oss}\left(V_{DC}\right) \cdot \frac{2 \cdot V_{DC}}{2} = Q_{oss}\left(V_{DC}\right) \cdot V_{DC} \quad (6)$$

The energy extracted from C_{oss} during its discharge corresponds to the initial energy that was stored in it at the supply voltage V_{DC}, which is referred as $E_{oss}(V_{DC})$. Because C_{oss} is a non-linear capacitor, $E_{oss}(V_{DC})$ has to be calculated with equation (3). The energy extracted from C_{oss} is not lost during the transition, but transferred to and later stored in V_{supply}. The rest of the energy that is stored in V_{supply} has to be provided by the resonant inductor, and corresponds to the minimum initial energy required at the start of the transition for achieving full ZVS (7-8).

$$E_{ind,1} = \Delta E_{supply} - E_{oss}\left(V_{DC}\right) \quad (7)$$

$$E_{ind,1} = Q_{oss}\left(V_{DC}\right) \cdot V_{DC} - E_{oss}\left(V_{DC}\right) \quad (8)$$

In the case of C_{oss} being a linear capacitor, the energy stored in it can be calculated with (9) and the previous formula can be simplified into (10). In this case, the required energy results to be equal to the initial energy stored in C_{oss}.

$$E_{oss,linr}(V_{DC}) = Q_{oss}(V_{DC}) \cdot \frac{V_{DC}}{2} \tag{9}$$

$$E_{ind,linr,1} = Q_{oss}(V_{DC}) \cdot \frac{V_{DC}}{2} \tag{10}$$

The clear consequence of this analysis is that in single device resonant topologies the most relevant parameter is the total stored charge in the output capacitance of the device. Moreover, the bigger the divergence between the equivalent charge related capacitance $C_{oss(tr)}$ and energy related capacitances $C_{oss(er)}$ the higher the required initial energy in the inductor (11). Si SJ MOSFETs have the biggest divergence between the values among the three compared devices. Consequently, while the Si and the SiC devices have very similar $C_{oss(tr)}$ the initial required energy is nearly twice as much for the Si device due to the much smaller $E_{oss}(V_{DC})$ of the Si device in comparison to the SiC device. In the case of GaN, because its output charge $Q_{oss}(V_{DC})$ is much smaller, the required initial energy is also much smaller.

$$E_{oss}(V_{DC}) < E_{oss,linr}(V_{DC}) \xrightarrow{\text{yields}} E_{ind,1} > E_{ind,linr,1} \tag{11}$$

The previous analysis is verified by the calculation of the required initial energies for achieving ZVS in the three example devices (Si, SiC and GaN), and the simulation of the energy distribution in time during the transition, represented in Fig. 7 and Fig. 8. The drain to source voltage along time during the transition has been represented in Fig. 9, where it can be observed that the transition time also depends mostly on the total stored charge $Q_{oss}(V_{DC})$. Table 2 summarizes the results of the simulations, which has been represented in the previous figures.

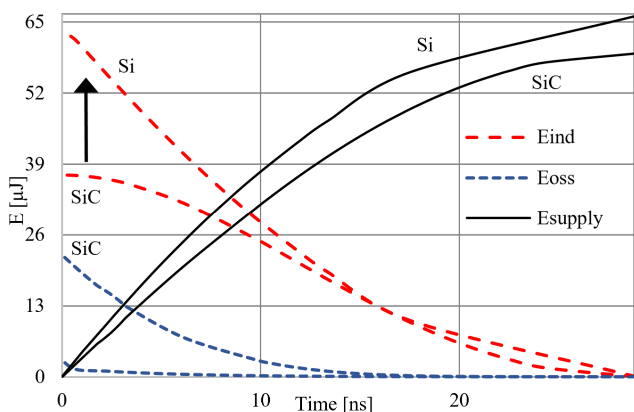

FIGURE 7. Si and SiC typical distribution of energies during the resonant discharge of the C_{oss}.

B. SINGLE DEVICE AT A HIGHER VOLTAGE

In certain topologies, the voltage stored in C_{oss} before the discharge transition could be higher than the voltage in the supply V_{DC}. Since the initial voltage in C_{oss} is higher than the voltage in V_{supply}, both capacitors will tend to balance naturally. If we assume the equivalent capacitance of V_{supply} to be much bigger than the equivalent capacitance of C_{oss}, the balance voltage will be, for all purposes, equal to V_{DC}.

When the voltages become equal, the total amount of charge that has been transferred from C_{oss} into V_{supply} can be calculated with (12) and the energy that has been consequently stored in V_{supply} can be estimated with equation (13). The energy that has been extracted from C_{oss} can be calculated with (14). Because the ΔQ was stored in C_{oss} at a higher voltage than V_{DC}, the initial energy in C_{oss} was always necessarily higher than the energy that has been transferred into V_{supply}. The rest of the energy would have been stored in

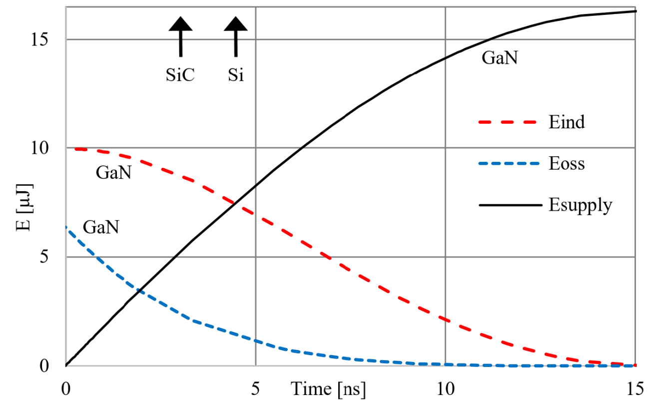

FIGURE 8. GaN typical distribution of energies during the resonant discharge of the C_{oss}.

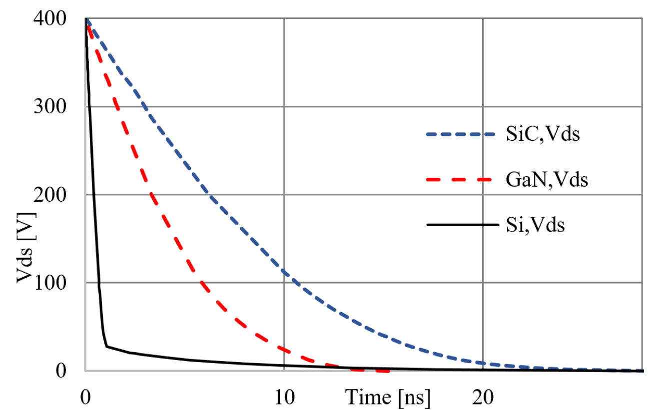

FIGURE 9. Si, SiC and GaN typical V_{ds} voltage during the resonant discharge of C_{oss}.

TABLE 2. Single device summary.

	IPP60R170CFD7	IMZA65R027M1H	IGT60R070D1
V_{DC}	400 V	400 V	400 V
$E_{ind,1}$	62.95 µJ	37.05 µJ	9.97 µJ
E_{supply}	66.13 µJ	59.29 µJ	16.32 µJ
Time	28.90 ns	28.83 ns	15.24 ns

the resonant inductor (15-16).

$$Q = Q_{oss}(V_{DC} + \Delta V) - Q_{oss}(V_{DC}) \quad (12)$$

$$\Delta E_{supply} = \Delta Q \cdot V_{DC} \quad (13)$$

$$\Delta E_{oss} = E_{oss}(V_{DC} + \Delta V) - E_{oss}(V_{DC}) \quad (14)$$

$$\Delta E_{ind} = \Delta E_{oss} - \Delta E_{supply} \quad (15)$$

$$\Delta E_{oss} > \Delta E_{supply} \xrightarrow{\text{yields}} \Delta E_{ind} > 0 \quad (16)$$

After both C_{oss} and V_{supply} have reached the same voltage, V_{DC}, the scenario becomes equal to the one analyzed in the previous section for single device topologies, where the initial energy required in the inductor is equal to $E_{ind,1}$(8). Therefore, the initial energy required at the start of the transition would be $E_{ind,1}$ minus the additional ΔE_{ind} that has already been stored in the inductor during the natural balance of the capacitor voltage (17-19).

$$E_{ind,2} = E_{ind,1} - \Delta E_{ind} \quad (17)$$

$$E_{ind,2} = Q_{oss}(V_{DC}) \cdot V_{DC} + \Delta Q \cdot V_{DC} - E_{oss}(V_{DC} + \Delta V) \quad (18)$$

$$E_{ind,2} = Q_{oss}(V_{DC} + \Delta V) \cdot V_{DC} - E_{oss}(V_{DC} + \Delta V) \quad (19)$$

Because of this, the higher the initial difference between the voltages the lower the required initial stored energy in the resonant inductor. The turning point is the one where the initial required energy in the inductor $E_{ind,2}$ equals zero, which occurs when ΔE_{ind} is greater than or equal to $E_{ind,1}$ (20).

$$E_{ind,2} = 0 \xrightarrow{\text{yields}} Q_{oss}(V_{DC} + \Delta V) \cdot V_{DC} = E_{oss}(V_{DC} + \Delta V) \quad (20)$$

For a linear capacitor, the previous expression (20) can be simplified into the well-known condition that the starting voltage should be at least twice of the supply voltage V_{DC} (21-23).

$$E_{oss,linr,2}(V_{DC} + \Delta V) = Q_{oss}(V_{DC} + \Delta V) \cdot \frac{(V_{DC} + \Delta V)}{2} \quad (21)$$

$$Q_{oss}(V_{DC} + \Delta V) \cdot V_{DC} = Q_{oss}(V_{DC} + \Delta V) \cdot \frac{(V_{DC} + \Delta V)}{2} \quad (22)$$

$$V_{DC} = \frac{(V_{DC} + \Delta V)}{2} \xrightarrow{\text{yields}} \Delta V = V_{DC} \quad (23)$$

For modern Si SJ MOSFETs the variation in stored energy at high voltages is comparatively smaller than in a charge equivalent linear capacitor $C_{oss(tr)}$. Consequently, the decrease on the required starting energy in the inductor at starting voltages higher than the supply is comparatively smaller than in the SiC or GaN example devices. Practically, without additional stored energy in the inductor the full ZVS range is very much constrained (e.g. CrCM boost converter). Another side effect of the same phenomena is that a small amount of residual energy in the parasitic inductances during the charge of the C_{oss} potentially induces a higher V_{ds} overshoot in Si SJ switches than in an equivalent linear $C_{oss(tr)}$ capacitance. This effect makes this technology less suited for applications like synchronous rectification [27]. The required initial energy in the inductor for different starting voltages and a V_{DC} equal to 200 V has been calculated for the three example devices (Si, SiC and GaN) and represented in Fig. 10.

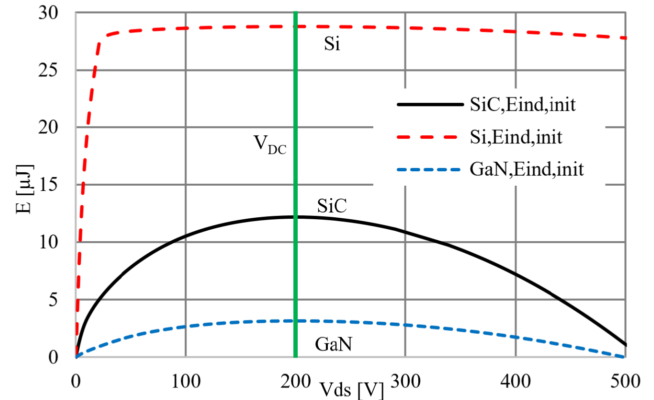

FIGURE 10. Si, SiC and GaN typical additional required energy for discharge of C_{oss} for different initial V_{ds} voltages when the supply voltage is 200 V.

The previous analysis is verified by the calculation of the required initial energies for achieving ZVS in the three example devices (Si, SiC and GaN), and the simulation of the energy distribution in time during the transition, which is represented in Fig. 11 and Fig. 12. For the simulated examples in Fig. 11 and Fig. 12 the starting voltage in C_{oss} was 400 V and the V_{supply} voltage was half of it (200 V). Table 3 makes a summary of the results in the previously stated conditions.

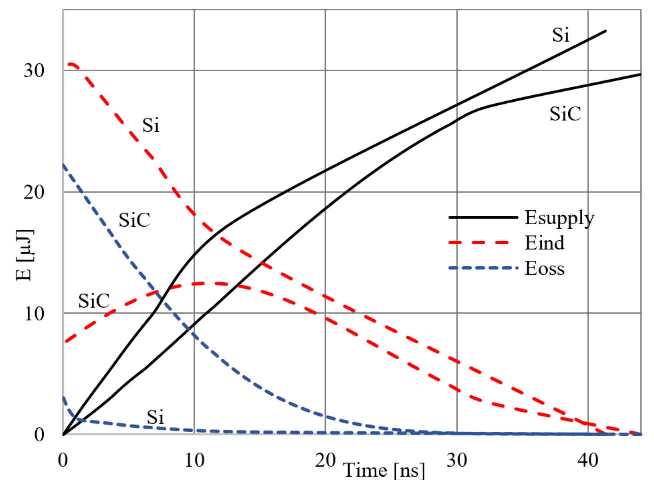

FIGURE 11. Si and SiC typical distribution of energy during the discharge of the C_{oss} with starting voltage equal to 400 V and V_{DC} voltage equal to 200 V.

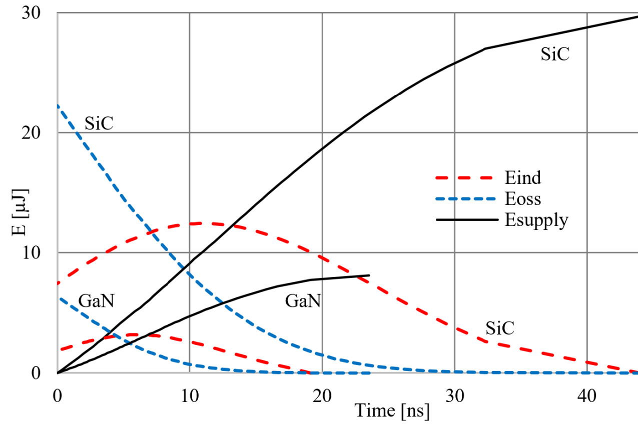

FIGURE 12. SiC and GaN typical distribution of energy during the discharge of the C_{oss} with starting voltage equal to 400 V and V_{DC} voltage equal to 200 V.

TABLE 3. Single device at a higher voltage summary.

	IPP60R170CFD7	IMZA65R027M1H	IGT60R070D1
V_{DC}	200 V	200 V	200 V
ΔV	200 V	200 V	200 V
$E_{ind,2}$	30.08 µJ	7.45 µJ	1.76 µJ
$Q_{oss}(V_{DC})$	153.01 nC	96.35 nC	26.08 nC
$E_{oss}(V_{DC})$	1.80 µJ	7.06 µJ	2.05 µJ
E_{supply}	33.25 µJ	29.69 µJ	8.12 µJ
Time	41.32 ns	43.99 ns	23.52 ns

C. SINGLE DEVICE AT A LOWER VOLTAGE

For completeness, the required energy for the discharge of C_{oss} when its initial voltage is lower than V_{DC} is analyzed in this section. The remaining charge in C_{oss} will be transferred into V_{supply}, which yields a net energy variation in V_{supply} that can be estimated by (24). The energy extracted from C_{oss} can be calculated with equation (25). The required initial energy in the inductor at the start of the transitions equals to the difference between the stored and the extracted energies, which can be calculated with equations (26-27).

$$\Delta E_{supply} = Q_{oss}\left(V_{DC} - \Delta V\right) \cdot V_{DC} \tag{24}$$

$$E_{oss}\left(V_{DC} - \Delta V\right) = \int_0^{(V_{DC}-\Delta V)} v \cdot C_{oss}(v)dv \tag{25}$$

$$E_{ind,3} = \Delta E_{supply} - E_{oss}\left(V_{DC} - \Delta V\right) \tag{26}$$

$$E_{ind,3} = Q_{oss}\left(V_{DC} - \Delta V\right) \cdot V_{DC} - E_{oss}\left(V_{DC} - \Delta V\right) \tag{27}$$

For an equivalent charge related linear capacitor $C_{oss(tr)}$ the stored energy can be alternatively calculated with (28), whereas the expression in (27) can be simplified into (29-30). In this scenario, the energy required is equal to the energy initially stored in C_{oss}.

$$E_{oss,linr}\left(V_{DC} - \Delta V\right) = Q_{oss}\left(V_{DC} - \Delta V\right) \cdot \frac{\left(V_{DC} - \Delta V\right)}{2} \tag{28}$$

$$E_{ind,linr,3} = Q_{oss}\left(V_{DC} - \Delta V\right) \cdot \left(V_{DC} - \frac{\left(V_{DC} - \Delta V\right)}{2}\right) \tag{29}$$

$$E_{ind,linr,3} = Q_{oss}\left(V_{DC} - \Delta V\right) \cdot \left(\frac{V_{DC} + \Delta V}{2}\right) \tag{30}$$

Like in the other two previous scenarios for single device topologies, the non-linear distribution of charge in the output capacitance of Si SJ devices requires comparatively more initial energy stored in the inductor than SiC or GaN for achieving full ZVS. The results of the analysis were already represented in Fig. 10 for a supply voltage V_{DC} equal to 200 V and starting V_{ds} voltages lower than 200 V. Table 4 makes a summary of the results for an alternative scenario where VDC equals 400 V and the starting V_{ds} equals half of it (200 V).

TABLE 4. Single device at a lower voltage summary.

	IPP60R170CFD7	IMZA65R027M1H	IGT60R070D1
VDC	400 V	400 V	400 V
ΔV	-200 V	-200 V	-200 V
$E_{ind,3}$	62.86 µJ	31.95 µJ	8.44 µJ
E_{supply}	64.65 µJ	39.02 µJ	10.52 µJ
Time	28.61 ns	22.61 ns	11.82 ns

D. HALF-BRIDGE TOPOLOGIES

For the sake of generality in the analysis, a half-bridge in a resonant or quasi-resonant converter during the switching transition is represented by the simplified equivalent circuit in Fig. 13. In the simplified circuit there is a capacitor C_2 that stands for the output capacitance $C_{oss,2}$ of the device which is turning-off. The capacitor C_1 stands for the output capacitance $C_{oss,1}$ of the device which is turning-on. The inductor L_r is connected to the mid-point of the half-bridge and stands for an equivalent resonant inductance that provides the required energy for the ZVS transition. The equivalent series resistor R_s stands for all of the parasitic series resistances along the charging and discharging path.

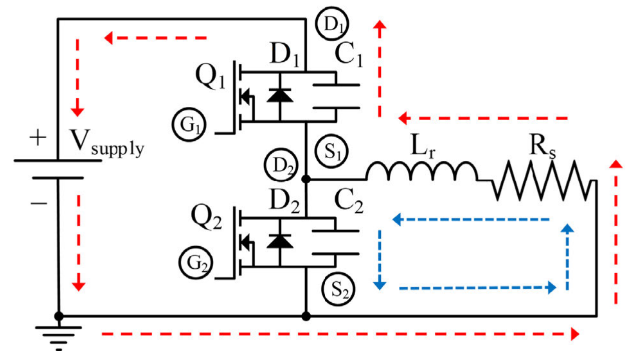

FIGURE 13. Simplified equivalent circuit for the analysis of the required initial energy to achieve ZVS in a half bridge configuration.

In this scenario, the output capacitance $C_{oss,1}$ of the device that is turning-on is discharged towards the supply V_{supply} just like in the single device topology example. However,

the output capacitance $C_{oss,2}$ of the device that is turning-off is being charged up to the supply voltage from the resonant inductor. Because the conduction path for the discharge of the $C_{oss,1}$ and the conduction path for the charge of $C_{oss,2}$ closes around different paths, the energy required for each of the transitions can be analyzed separately and later joined together to get the complete result. Notice that the analysis of the discharging transition of $C_{oss,1}$ is equivalent to the single device scenario analyzed in the previous section.

The previous analysis for single device topologies can also be applied for the charge of the capacitance $C_{oss,2}$ in Fig. 13. The supply voltage in V_{supply} is assumed equal to zero, which is effectively a short circuit. Substituting the values in equation (8) and taking into account the inverted polarity of voltages yields the well-known expression in (31). Alternatively, a more simple analysis methodology for the charge of $C_{oss,2}$ would be based on the balance of energies. All the energy stored in the inductor at the start of the transition would be moved and stored without loss into $C_{oss,2}$, which comprehensively yields as well to the expression in (31).

$$E_{ind,4} = Q_{oss}(-V_{DC}) \cdot 0 - E_{oss}(-V_{DC}) = E_{oss}(V_{DC}) \quad (31)$$

To the result previously obtained in equation (8) has to be added the result of equation (31) accounting for the additionally required charge of $C_{oss,2}$ and resulting in a single expression which can be used to calculate the minimum required inductor energy to reach ZVS in a half-bridge (32). For simplicity in the analysis, both stacked devices and their capacitances have been considered to be equal.

$$E_{ind,5} = E_{ind,1} + E_{ind,4} = Q_{oss}(V_{DC}) \cdot V_{DC} \quad (32)$$

The consequence of the analysis is that in stacked devices topologies the required initial energy to achieve ZVS is independent of the stored energy $E_{oss}(V_{DC})$ and depends exclusively on the stored charge $Q_{oss}(V_{DC})$ and the supply voltage of the system V_{DC}. Unlike in the previous single device topology scenario, the non-linear distribution of charge in Si does not have a drawback on the ZVS range compared to other devices with an equivalent $C_{oss(tr)}$.

On the other hand, the $R_{ds,on}$ of a SiC or GaN device with an equivalent $C_{oss(tr)}$ is smaller than the $R_{ds,on}$ of the Si, which potentially decreases the conduction losses and improves the overall performance of the system. Therefore, the optimum results in the replacement of a Si device with a specific $R_{ds,on}$ by a SiC or GaN device with a similar or equal $R_{ds,on}$ requires to redesign the converter taking into account the reduced ZVS energy requirements. A simple one to one $R_{ds,on}$ based replacement would not take full advantage of the potential reduction in circulating currents and the overall benefits of the improved semiconductor technology characteristics.

The previous analysis is verified by the calculation of the required initial energies for achieving ZVS with the three example devices (Si, SiC and GaN), and the simulation of the energy distribution in time during the transition, represented in Fig. 14 and Fig. 15. The drain to source voltage along time during the transition has been represented in Fig. 16, where

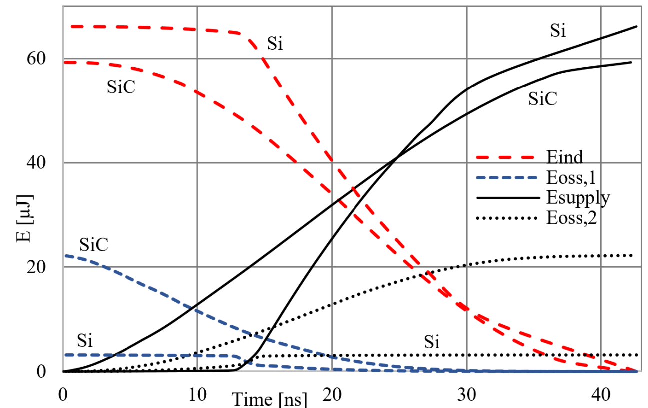

FIGURE 14. Si and SiC typical distribution of energy during the discharge of $C_{oss,1}$ and the charge of $C_{oss,2}$.

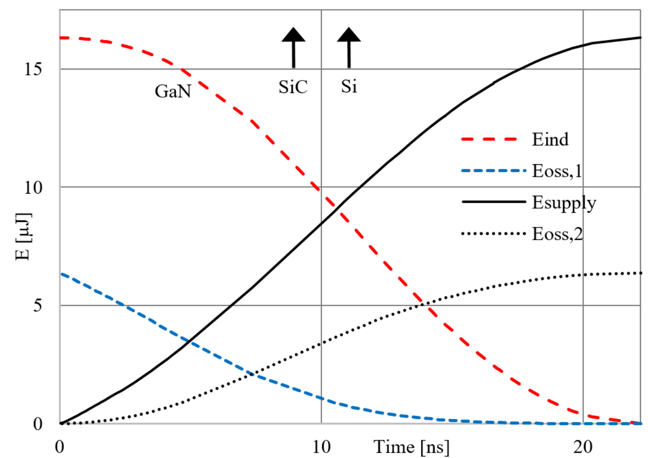

FIGURE 15. GaN typical distribution of energy during the discharge of $C_{oss,1}$ and the charge of $C_{oss,2}$.

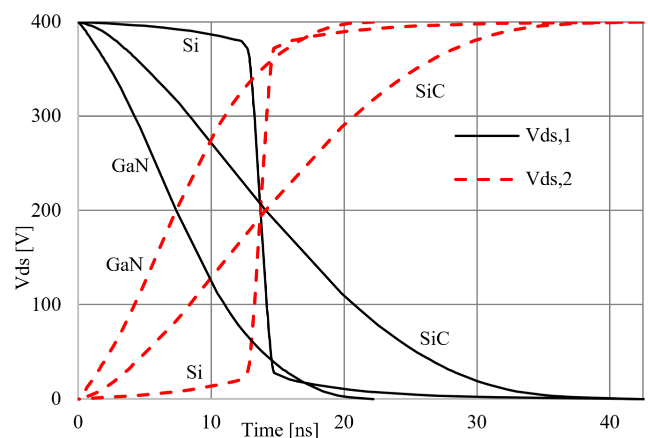

FIGURE 16. Si, SiC and GaN typical V_{ds} voltage during the resonant discharge of $C_{oss,1}$ and the resonant charge of $C_{oss,2}$.

it can be observed that the total transition time also depends mostly on the total stored charge $Q_{oss}(V_{DC})$, similar for Si and SiC but much smaller for GaN. Table 5 makes a summary of the results represented in the previously stated figures.

TABLE 5. Half-bridge summary.

	IPP60R170CFD7	IMZA65R027M1H	IGT60R070D1
V_{DC}	400 V	400 V	400 V
$E_{ind,5}$	66.13 µJ	59.29 µJ	16.32 µJ
E_{supply}	66.13 µJ	59.29 µJ	16.32 µJ
Time	42.62 ns	42.19 ns	22.20 ns

III. HARD SWITCHED TURN-ON LOSSES

A. SINGLE DEVICE TOPOLOGIES

The conclusions extracted from the analysis in the previous sections are valid whenever full ZVS is ensured in all the operating conditions of interest of the resonant converter. However, it is not always possible or necessarily better performing a converter designed to operate in full ZVS in all conditions. Depending on the balance of switching to conduction losses in a specific design, it could be more effective to allow partial ZVS (or partial hard-switching). The impact of partial ZVS, and the non-linear stored charge distribution along the voltage in C_{oss} in the event of partial ZVS will be analyzed in this section.

In single device topologies it is only necessary to consider the remaining stored energy $E_{oss}(\Delta V)$ at the voltage ΔV at which the device turns-on under partial or full hard-switching [5]. That remaining energy will be dissipated within the device itself. In this scenario, the switching losses of Si compared to the other two devices would be bigger or smaller depending on the hard-switched voltage. In Fig. 17 can be observed that the Si device is superior to an equivalent $C_{oss(tr)}$ SiC device in the range between 75 V and 400 V (V_{DC}). More noticeably, it can be observed in Fig. 17 that the Si device is superior to a similar $C_{oss(er)}$ GaN device in the voltage range between 175 V and 375 V. However, the Si device performs worse than the other two devices in partial or full hard-switching out of those ranges. Fig. 18 represents the comparative increment of losses

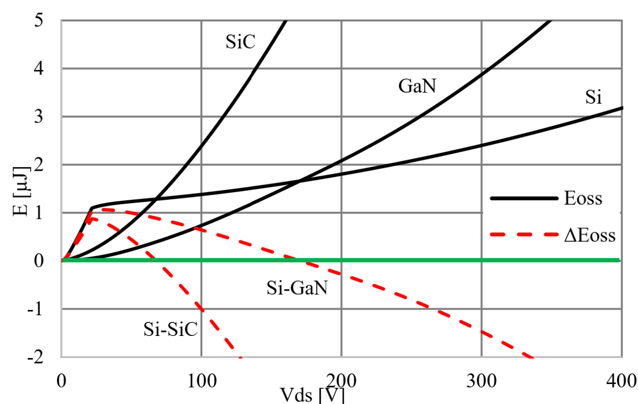

FIGURE 17. Si, SiC and GaN calculated typical hard-switching losses at different V_{ds} voltages and comparative loss between the Si and the SiC and GaN devices.

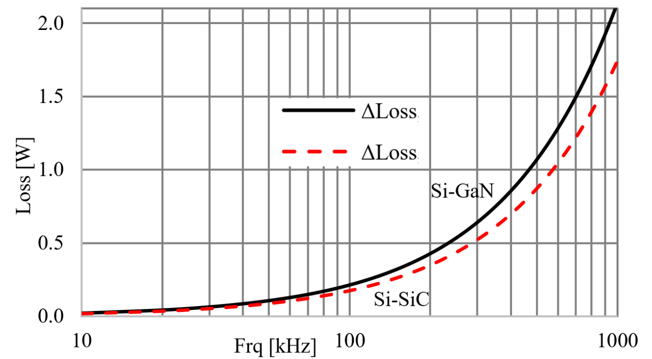

FIGURE 18. Calculated comparative increase of losses for the hard-switching of the Si, SiC and GaN devices at 22 V and different switching frequencies.

between Si and the other two devices while hard-switching them at 22 V and at different frequencies.

Consequently, the non-linear distribution of charge in Si output capacitance C_{oss} could be theoretically advantageous to other equivalent $C_{oss(tr)}$ devices and/or $C_{oss(er)}$ devices when partial ZVS occurs within a defined voltage range. However, in practice, for a decreasing initial inductor energy, Si would perform initially worse until the remaining E_{oss} of SiC and GaN goes beyond the remaining E_{oss} of Si (Fig. 19). Table 6 makes a summary of the results in a scenario with low initial E_{ind}, which is enough for GaN to achieve full ZVS but causes SiC to present more switching losses than Si.

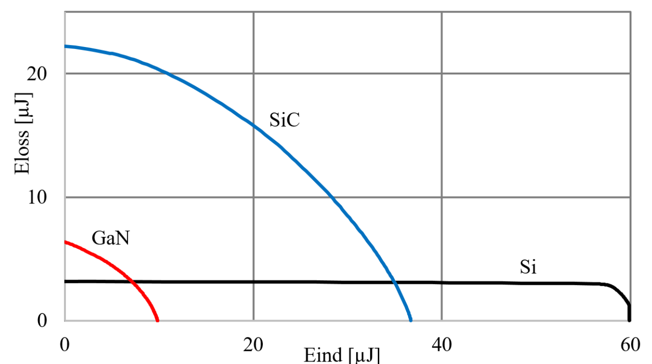

FIGURE 19. Calculated comparative increase of loss for the hard-switching of the Si, SiC and GaN devices with different starting energies in the resonant inductor.

TABLE 6. Single device hard-switched summary.

	IPP60R170CFD7	IMZA65R027M1H	IGT60R070D1
V_{DC}	400 V	400 V	400 V
E_{ind}	10 µJ	10 µJ	10 µJ
$V_{ds,1}$	398 V	379 V	0 V
$E_{oss,1}(V_{ds,1})$	3.16 µJ	20.24 µJ	0 µJ
E_{loss}	3.16 µJ	20.24 µJ	0 µJ

B. HALF-BRIDGE TOPOLOGIES

In the event of partial or full hard-switching in the stacked configuration in Fig. 13, the device which is hard-switched

turned-on (Q_1 in this analysis) dissipates within itself the remaining stored energy in its output capacitance $E_{oss}(\Delta V)$, similarly to the single device scenario. However, in a half-bridge configuration, in the event of partial or full hard-switching the capacitance which was being charged ($C_{oss,2}$), completes its charge resistively.

The energy that is extracted from the supply during the resistive charge of $C_{oss,2}$ can be calculated with (33), whereas the energy stored into $C_{oss,2}$ can be calculated with (34-35). The difference between the supplied and the stored energy (36) corresponds to the energy that has been dissipated within the series resistances in the charging path R_s, mostly in the channel of the opposing device Q_1.

$$\Delta E_{supply,2} = (Q_{oss}(V_{DC}) - Q_{oss}(V_{DC} - \Delta V)) \cdot V_{DC} \quad (33)$$

$$\Delta E_{oss,2} = E_{oss}(V_{DC}) - E_{oss}(V_{DC} - \Delta V) \quad (34)$$

$$\Delta E_{oss,2} = \int_{(V_{DC}-\Delta V)}^{V_{DC}} v \cdot C_{oss}(v) dv \quad (35)$$

$$\Delta E_{loss,2} = \Delta E_{supply,2} - \Delta E_{oss,2} \quad (36)$$

The total loss in the event of partial or full hard-switched turn-on in a half-bridge is the sum of the loss within the switching device Q_1 plus the loss caused by the completion of the charge of the opposing device Q_2 (37).

$$\Delta E_{loss,tot} = \Delta E_{loss,2} + E_{oss,1}(\Delta V) \quad (37)$$

In the case of a linear capacitor the stored energy $\Delta E_{oss,2}$ calculated in (35) can be simplified into (38-40). Whereas the energy extracted from the supply can be further simplified into (41), and the expression for the dissipated energy during the completion of the charge simplified into (42-43).

$$E_{oss,2,linr}(V_{DC}) = Q_{oss}(V_{DC}) \cdot \frac{V_{DC}}{2} = C_{oss(tr)} \cdot \frac{V_{DC}^2}{2} \quad (38)$$

$$E_{oss,2,linr}(V_{DC} - \Delta V) = C_{oss(tr)} \cdot \frac{(V_{DC} - \Delta V)^2}{2} \quad (39)$$

$$\Delta E_{oss,2,linr} = C_{oss(tr)} \cdot \left(\frac{V_{DC}^2}{2} - \frac{(V_{DC} - \Delta V)^2}{2} \right) \quad (40)$$

$$\Delta E_{supply,2,linr} = C_{oss(tr)} \cdot \left(V_{DC}^2 - (V_{DC} - \Delta V) \cdot V_{DC} \right) \quad (41)$$

$$\Delta E_{loss,2,linr} = \Delta E_{supply,2,linr} - \Delta E_{oss,2,linr} \quad (42)$$

$$\Delta E_{loss,2,linr} = C_{oss(tr)} \cdot \frac{(\Delta V)^2}{2} \quad (43)$$

The total loss in the event of partial or full hard-switched turn-on in a half-bridge with linear capacitances $C_{oss(tr)}$ results in the expression in (44). Therefore, when partial ZVS occurs within certain voltage range the non-linear distribution of charge in the Si output capacitance C_{oss} is theoretically advantageous with regard to other equivalent $C_{oss(tr)}$ devices or equivalent $C_{oss(er)}$ devices (Fig. 20 and Fig. 21). However, the required resonant energy to reach a certain switching voltage is very distinct. Consequently, for a certain available resonant energy the switching losses are directly related to the equivalent $C_{oss(tr)}$, which has been represented in Fig. 22,

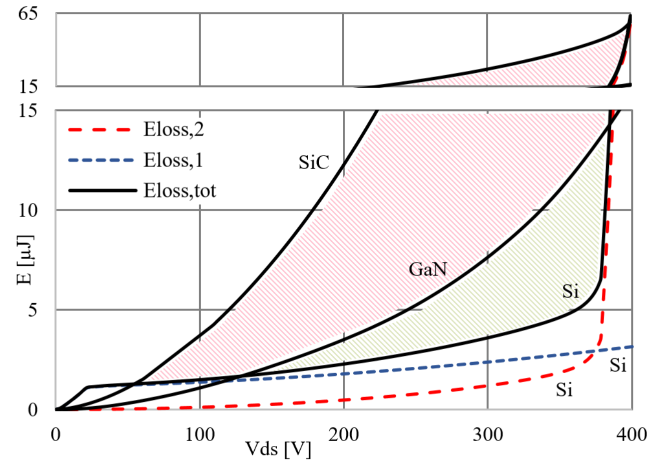

FIGURE 20. Si, SiC and GaN calculated typical half bridge hard-switching loss at different Q_1 turn-on voltages.

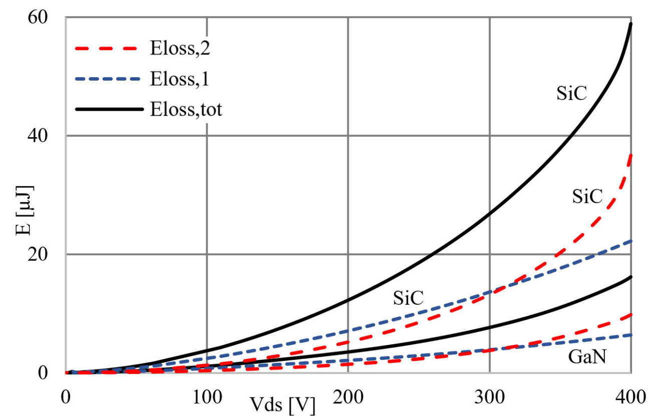

FIGURE 21. SiC and GaN calculated typical half bridge hard-switching loss at different Q_1 turn-on voltages.

TABLE 7. Half-bridge hard-switched summary.

	IPP60R170CFD7	IMZA65R027M1H	IGT60R070D1
V_{DC}	400 V	400 V	400 V
E_{ind}	10 µJ	10 µJ	10 µJ
$V_{ds,1}$	398 V	384 V	129 V
$V_{ds,2}$	2 V	16 V	271 V
$Q_{oss,2}(V_{ds,2})$	26.79 nC	22.25 nC	20.15 nC
$E_{oss,1}(V_{ds,1})$	3.16 µJ	20.73 µJ	3.28 µJ
E_{loss}	52.35 µJ	48.67 µJ	6.16 µJ

where the SiC and GaN devices outperform the Si device in all the energy range. Moreover, notice how the total switching loss of Si increases dramatically near the end of the supply range V_{DC} because most of the charge in $C_{oss,2}$ is stored under a V_{ds} of 22 V.

$$\Delta E_{loss,t,linr} = C_{oss(tr)} \cdot (\Delta V)^2 \quad (44)$$

Table 7 makes a summary of the results in Fig. 22 in a scenario with low initial E_{ind}, which is not enough for any of the devices to achieve full ZVS.

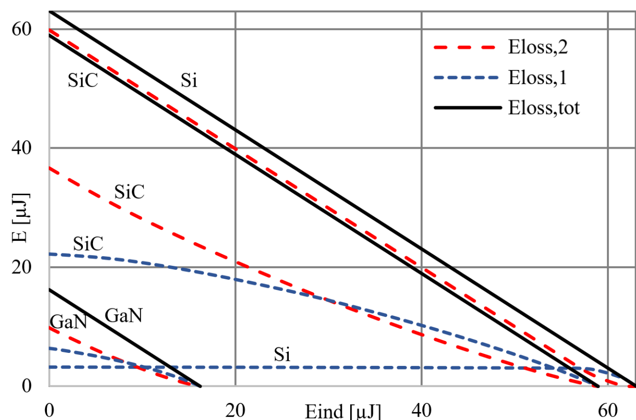

FIGURE 22. Si, SiC and GaN calculated typical half bridge hard-switching loss for different starting energies in the resonant inductor.

C. MILLER FEEDBACK EFFECT

The charge of the gate to drain capacitance C_{gd}, which is part of C_{oss}, causes the injection of current into the gate to source capacitance C_{gs} and into the gate-driving path. Depending on the rising slope of the drain voltage, the ratio of the capacitance values and the impedance of the gate-driving path, it could happen that the device turns-on unexpectedly by the so-called Miller feedback effect. The phenomena could occur during the turn-off transition, effectively delaying the turn-off and increasing the switching losses, or during the hard-switching turn-on of the opposing device, causing a short circuit of the half-bridge that may destroy the devices. This mechanism is frequently confused with hard-commutation, which could also cause the failure of the devices by other means [28], [29].

Applying a similar analysis to one in the previous sections for the charge of two capacitors in series, we can stablish criteria for the minimum prerequisites for the Miller feedback induced turn-on to occur. The worst possible scenario is where all the charge in C_{gd} ($Q_{gd}(V_{DC})$ in equation (45)) is transferred into C_{gs} fast enough that negligible voltage is discharged through the gate driving path. The induced voltage raise in C_{gs} (which is approximately equal to C_{iss}) should reach at least the threshold voltage of the device V_{th} for the feedback induced turn-on to occur (46). With the parameters in Table 1, it can be calculated that for the Si device the $V_{gs,max}$ would be 2.63 V, well under its threshold, whereas for the SiC device is 5.77 V and for the GaN device is 5.47 V, both of which are above their respective thresholds.

$$Q_{gd}(V_{DC}) = \int_0^{V_{DC}} C_{gd}(v)dv \tag{45}$$

$$V_{gs,max} \cong \frac{Q_{gd}(V_{DC})}{C_{iss}} < V_{th} \tag{46}$$

IV. HARD SWITCHED TURN-OFF LOSSES

A contribution to the switching losses that is frequently neglected in resonant ZVS topologies is the one caused by the hard-switched turn-off transition. In resonant ZVS topologies, in spite of the devices turning-on under ZVS conditions, the prior turn-off necessarily happens in hard-switching. However, it is true that hard-switching turn-off losses can be significatively lower than the hard-switched turn-on losses, and that whenever the device turns-off fast enough the losses are in fact negligible. In this section, we analyze the conditions for a fast and near lossless turn-off and the consequences of a slow or delayed turn-off.

The dv/dt during a resonant turn-off transition is given by the available resonant current and the size of the output capacitances of the semiconductor device. The output capacitance C_{oss} of the semiconductor power switch can be split conveniently into the equivalent drain to source capacitance C_{ds} and the gate to drain capacitance C_{gd}. While the drain voltage raises, both capacitances are charged simultaneously, but through different paths. Whenever the dv/dt is limited by the C_{gd} charging path, the turn-off of the device is slowed down, and the channel carries part of the resonant current, which is therefore not fully stored in C_{oss} (47-50). Moreover, the overlap of current and voltage during a slowed down turn-off causes losses.

$$\frac{dv}{dt} = \frac{i_{dg}(t)}{C_{dg}(v)} = \frac{i_{ds}(t)}{C_{ds}(v)} \tag{47}$$

$$i_d(t) = i_{ch}(t) + i_{dg}(t) + i_{ds}(t) \tag{48}$$

$$i_{ch}(t) = 0 \xrightarrow{\text{yields}} i_{ds}(t) = i_d(t) - i_{dg}(t) \tag{49}$$

$$\frac{C_{ds}(v)}{C_{dg}(v)} = \frac{i_d(t) - i_{dg}(t)}{i_{dg}(t)} = \frac{i_d(t)}{i_{dg}(t)} - 1 \tag{50}$$

The maximum gate current $i_{dg}(t)$ capability depends on the driver's turn-off path total impedance $R_{g,off}$, the off-state driving voltage $V_{G,off}$ and the voltage at the gate during the voltage transition (V_{Miller} or approximately V_{th} when the channel does not conduct) (51). We can substitute (51) in (50) and simplifiy it into (52) assuming the driver turn-off voltage to be zero, which is the most frequent case for the devices in this comparison. The expression (52) summarizes the condition for a lossless resonant turn-off. Notice that $C_{ds}(v)$ and $C_{dg}(v)$ are a function of the voltage. Moreover, the condition is a function of the drain current $i_d(t)$, which is load dependent in most of the converters. From the previous analysis it can be concluded that the fast turn-off range can be extended by several means: decreasing $R_{g,off}$, increasing V_{th} of the device, or increasing the ratio of $C_{ds}(v)$ to $C_{dg}(v)$ (e.g. placing an additional capacitor in parallel to $C_{ds}(v)$).

$$i_{dg}(t) = \frac{V_{gs}(t) - V_{G,off}}{R_{g,off}} \approx \frac{V_{th}}{R_{g,off}} \tag{51}$$

$$\frac{C_{ds}(v)}{C_{dg}(v)} \geq \frac{i_d(t) \cdot R_{g,off}}{V_{th}} - 1 \tag{52}$$

The previous analysis is verified by the simulation of the slow turn-off losses in the three example devices (Si, SiC and GaN) and represented in Fig. 23 and Fig. 24. Whereas all the devices in the simulated examples are turning-off with the same resonant current of 12 A, the driving impedance has been adjusted for all of them to cause the same amount of total

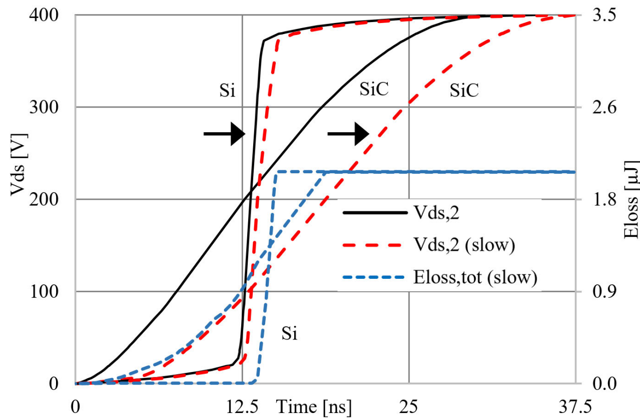

FIGURE 23. Si and SiC calculated typical hard-switched turn-off slowed down by the gate impedance. Si: $R_{g,off} = 10.9\ \Omega$ (value of the embedded R_g) and 12A turn-off current. SiC: $R_{g,off} = 19\ \Omega$ (including embedded R_g) and 12A turn-off current.

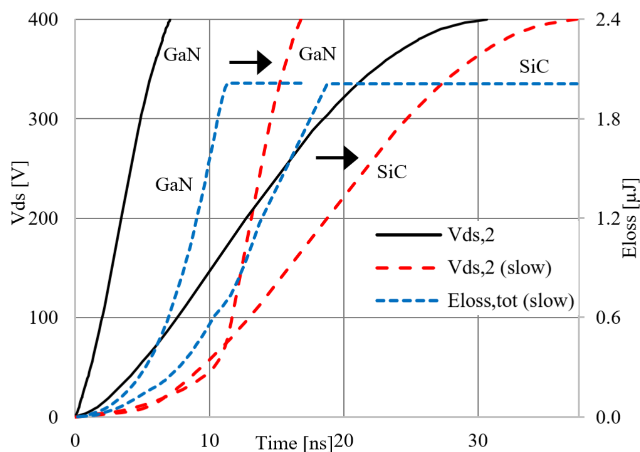

FIGURE 24. SiC and GaN calculated typical hard-switched turn-off slowed down by the gate impedance. SiC and GaN: $R_{g,off} = 19\ \Omega$ (including embedded R_g) and 12 A turn-off current.

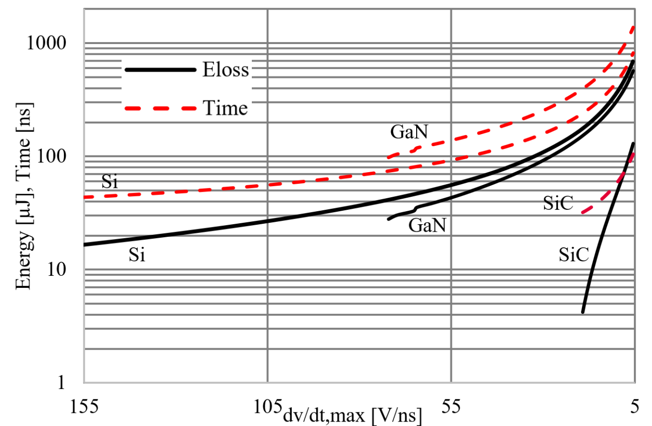

FIGURE 25. Slow turn-off with limited dv/dt. Calculated total time of the transition and switching losses for the three different capacitance profiles.

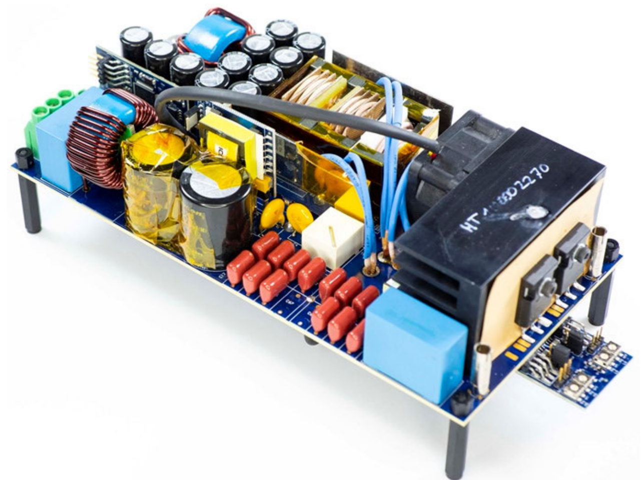

FIGURE 26. Prototype of the 3.3 kW LLC resonant converter (EVAL_3K3W_LLC_HB_CFD7) [31].

loss ($E_{loss,tot}$). Notice, however, that the driving impedance for the Si device already accounts for the integrated resistance and cannot be further decreased, whereas the driving impedance of the SiC and GaN devices has been increased with additional external resistances.

On the other hand, it is sometimes desirable to slow down the maximum dv/dt during the switching transitions in certain applications or due to EMI constraints [30]. The dv/dt can be controlled limiting the charge of C_{gd} at the expense of the additional switching losses. Fig. 25 represented the switching losses while limiting the maximum dv/dt for the three devices in the comparison (Si, SiC and GaN). It can be observed that, whereas the non-linearity of Si causes extremely high maximum dv/dt, the SiC device is very well suited for low dv/dt applications because its capacitances are quasi-linear and relatively big in comparison to GaN. Table 8 makes a summary of the results of the required conditions for achieving similar turn-off losses with the same initial current and voltage in the three analyzed devices.

V. EXPERIMENTAL

A 3300 W LLC DCDC converter [31] (Fig. 26) was designed and built with the specifications given in Table 9 to test the analysis and guidelines presented in this work. The Si device IPW60R031CFD7 in Table 10 was mounted for its test in the primary side HV half-bridge of the converter. The control was implemented with XMC^{TM} 4200 ARM® Cortex®-M4 microcontroller from Infineon Technologies AG. The equivalent simplified circuit of the prototype corresponds to the one in Figure 13. A complete schematic can be found in [31].

Because of the wide input and wide output range requirements of the prototype the circulating currents are relatively high and the converter switches in full ZVS along most of its operating range. In Fig. 27 the characteristic change of slope in the drain voltage caused by the non-linear capacitance of Si can be observed. Notice in Fig. 27 a slight evidence of Miller plateau that can be identified during the turn-on because of a slightly short dead-time. In Fig. 28 illustrates the lossless

TABLE 8. Hard-switched turn-off loss summary.

	IPP60R170CFD7	IMZA65R027M1H	IGT60R070D1
V_{DC}	400 V	400 V	400 V
$R_{g,off}$	10.90 Ω	19.06 Ω	19.30 Ω
i_d	12 A	12 A	12 A
$dv/dt_{,max}$	216.01 V/ns	17.45 V/ns	71.96 V/ns
$E_{loss,tot}$	2.01 µJ	2.01 µJ	2.01 µJ
Time	36.99 ns	37.37 ns	16.82 ns

TABLE 9. Key parameters of prototype.

Parameter	Value
Nominal input voltage	400 V
Input voltage range	350 V - 415 V
Nominal output voltage	52 V
Output voltage range	43.5 V – 59.5 V
Maximum output power	3300 W
Maximum output current	65 A
Switching frequency	45kHz-250 kHz
Resonant frequency	70 kHz
Magnetizing inductance (Lm)	100 µH
Resonant inductance (Lr)	10 µH

TABLE 10. Summary of device characteristics.

	IPW60R031CFD7	IMZA65R027M1H	IGT60R070D1
$R_{DS,on}$	26 mΩ @ 25 °C	27 mΩ @ 25 °C	55 mΩ @ 25 °C
Q_{oss}	840 nC @ 400 V	147 nC @ 400 V	40.5 nC @ 400 V
E_{oss}	16.24 µJ @ 400 V	29.46 µJ @ 400 V	8.10 µJ @ 400 V
C_{gs}	5623 pF	2114 pF	380 pF
R_g	3.8 Ω	3 Ω	0.78 Ω
V_{th}	4 V	4.5 V	1.2 V

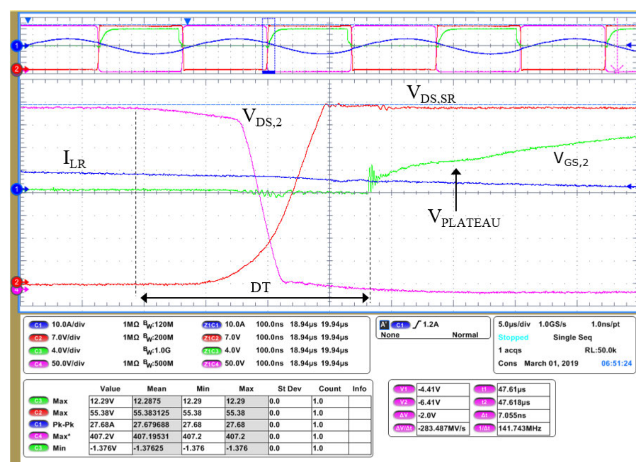

FIGURE 27. ZVS turn-on in the LLC 3.3 kW converter switching at its resonant frequency. $V_{DS,SR}$ corresponds the drain voltage of one of the secondary side's rectification devices.

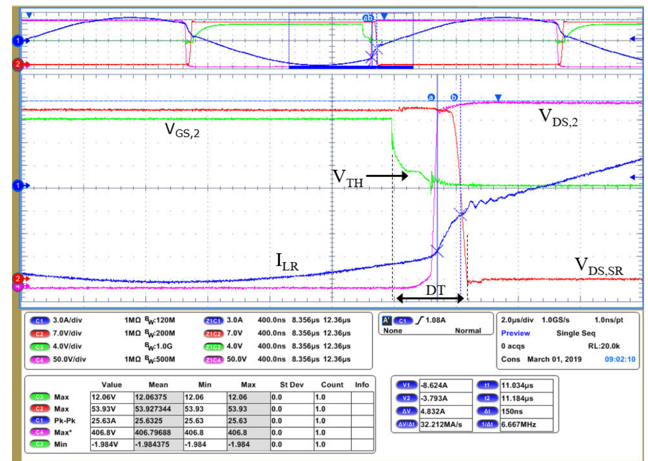

FIGURE 28. Fast and lossless hard-switched turn-off in the LLC 3.3 kW switching above its resonant frequency.

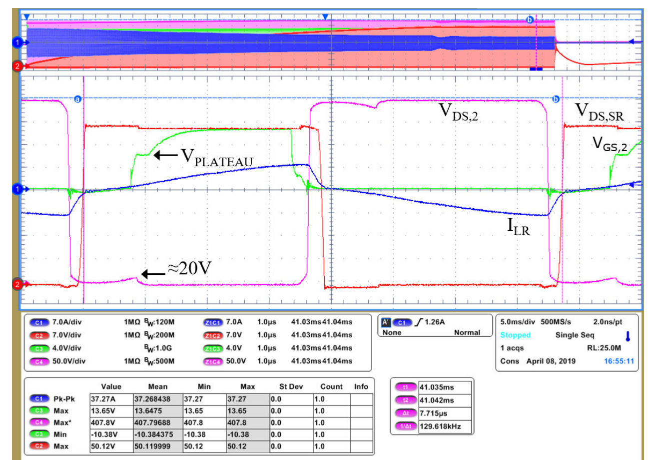

FIGURE 29. Partial ZVS turn-on in the LLC 3.3 kW converter operating at light load and switching far above its resonant frequency.

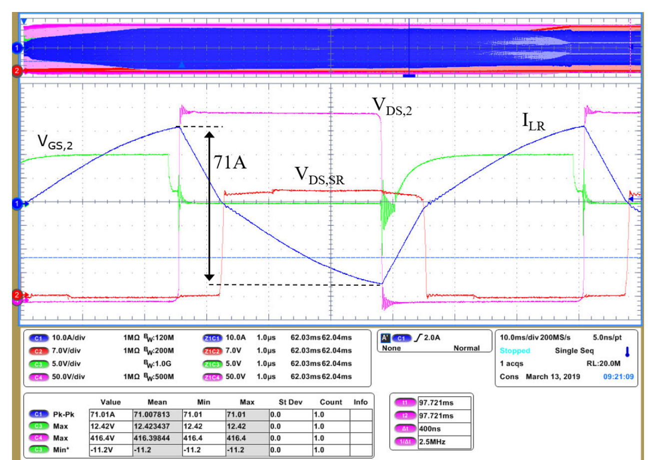

FIGURE 30. High current hard-switched turn-off transitions in the LLC 3.3 kW. The high resonant current causes high dv/dt and di/dt within the commutation loop.

turn-off transition while the converter operates slightly above resonance. Notice in Fig. 28 the Miller plateau at a voltage near the threshold during the resonant charge of C_{oss}.

In the LLC topology, at light loads and low output voltages the relation between the switching frequency and the gain of the converter becomes non-monotonic. This effect is caused

by the parasitic capacitances of the transformer and the secondary side rectifiers [14]. In these operating conditions, the switching frequency of the converter increases to maintain the regulation, while the resonant current and the available energy for the ZVS transition decreases. In Fig. 29 the partial hard-switching when the converter's frequency raises up to 130 kHz can be observed. As previously analyzed, the switching losses of the Si device would be higher than an equivalent $C_{oss(tr)}$ SiC device in this very same condition. Furthermore, a SiC or GaN device of equivalent $R_{ds,on}$ will be still capable by far of achieving full ZVS.

During the start-up, at high loads and low voltages the converter operates switching off relatively high currents. In these conditions the switching losses could increase significatively if the turn-off transition is limited by the driving path. Moreover, because of the high resonant currents, the dv/dt and di/dt within the commutation loop increase, causing the voltage ringing in Fig. 30. However, the speed of the transition can be controlled by the impedance of the driving path $R_{g,off}$ or by adding a capacitance in parallel to C_{ds}.

VI. CONCLUSION

The parasitic capacitances of modern Si SJ MOSFETs are characterized by its non-linearity. At high voltages the total stored energy $E_{oss}(V_{DC})$ in the output capacitance $C_{oss}(v)$, differs substantially from the energy in an equivalent linear capacitor $C_{oss(tr)}$ that stores the same amount of charge. That difference requires the definition of an additional equivalent linear capacitor $C_{oss(er)}$ that stores the same amount energy at a specific voltage. However, the parasitic capacitances of current SiC and GaN devices have a more linear distribution of charge along the voltage. Moreover, the equivalent $C_{oss(tr)}$ and $C_{oss(er)}$ of SiC and GaN devices is smaller than the ones of a Si device with a similar $R_{ds,on}$.

In this work the impact of the non-linear distribution of charge in the output capacitance of modern Si devices on the performance and requirements for the design of resonant ZVS converters has been analyzed. Furthermore, the non-linear capacitance of Si has been compared to the quasi-linear capacitance of a SiC device of equivalent time related output capacitance $C_{oss(tr)}$, and compared to the quasi-linear capacitance of a GaN device of similar energy related output capacitance $C_{oss(er)}$. The advantages and disadvantages of each of the alternatives have been analyzed for single device and half-bridge based topologies, as well as in full ZVS and partial or full hard-switching operating conditions.

In half-bridge topologies the required energy to achieve full ZVS depends exclusively on the total output stored charge $Q_{oss}(V_{DC})$ and the supply voltage V_{DC}, whereas in single device topologies the required energy is further increased by a relatively smaller $E_{oss}(V_{DC})$. In summary, in the full ZVS scenario, the equivalent SiC and the GaN devices are superior to the Si device in single device and half bridge topologies.

In partial hard-switching turn-on, within certain hard-switching turn-on voltage, the losses of the Si device could be lower than the switching losses of the equivalent $C_{oss(tr)}$ SiC or the equivalent $C_{oss(er)}$ GaN device. However, for a certain energy in the resonant inductor the switching voltage of the SiC or the GaN devices is much lower. Moreover, the Si advantage window dramatically diminishes when is compared to equivalent $R_{ds,on}$ SiC or GaN devices.

Overall, this work demonstrates that a meaningful one-to-one replacement of devices without a redesign of the converter would be among devices with an equivalent $C_{oss(tr)}$. Moreover, to fully unleash the potential improvement in the overall performance of the converter while replacing a Si device by an equivalent $R_{ds,on}$ SiC or GaN device requires the redesign of the resonant ZVS converter accounting for the reduced ZVS energy requirements. Finally, a highly efficient 3300 W DCDC LLC resonant converter prototype was designed and built to demonstrate the validity of the analysis.

REFERENCES

[1] *Climate Savers Computing Initiative (CSCI)*. Accessed: Feb. 1, 2020. [Online]. Available: http://www.climatesaverscomputing.org

[2] *80Plus Program*. Accessed: Feb. 1, 2020. [Online]. Available: http://www.plugloadsolutions.com

[3] J. W. Kolar, U. Drofenik, J. Biela, M. L. Heldwein, H. Ertl, T. Friedli, and S. D. Round, "PWM converter power density barriers," in *Proc. Power Convers. Conf. Nagoya*, Apr. 2007, p. 9.

[4] U. Badstuebner, J. Biela, and J. W. Kolar, "Design of an 99%-efficient, 5kW, phase-shift PWM DC-DC converter for telecom applications," in *Proc. 21th Annu. IEEE Appl. Power Electron. Conf. Exposit. (APEC)*, Feb. 2010, pp. 773–780.

[5] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of power MOSFETs revisited," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016.

[6] I. Castro, J. Roig, R. Gelagaev, B. Vlachakis, F. Bauwens, D. G. Lamar, and J. Driesen, "Analytical switching loss model for superjunction MOSFET with capacitive nonlinearities and displacement currents for DC–DC power converters," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2485–2495, Mar. 2016.

[7] J. Wang, H. S.-H. Chung, and R. T.-H. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 573–590, Jan. 2013.

[8] S. Paul, A. M. Schlaffer, and J. A. Nossek, "Optimal charging of capacitors," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 47, no. 7, pp. 1009–1016, Jul. 2000.

[9] Y. Perrin, A. Galisultanov, H. Fanet, and G. Pillonnet, "Optimal charging of nonlinear capacitors," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5023–5026, Jun. 2019.

[10] J. Roig and F. Bauwens, "Origin of anomalous C_{OSS} hysteresis in resonant converters with superjunction FETs," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 3092–3094, Sep. 2015.

[11] A. Medina-Garcia, M. Schlenk, D. Morales, and N. Rodriguez, "Resonant hybrid flyback, a new topology for high density power adaptors," *Electronics*, vol. 7, no. 12, p. 363, Dec. 2018.

[12] J. W. Kim, S. M. Choi, and K. T. Kim, "Variable on-time control of the critical conduction mode boost power factor correction converter to improve zero-crossing distortion," in *Proc. Int. Conf. Power Electron. Drives Syst.*, Nov. 2005, pp. 1542–1546.

[13] C. Marxgut, J. Biela, and J. W. Kolar, "Interleaved triangular current mode (TCM) resonant transition, single phase PFC rectifier with high efficiency and high power density," in *Proc. Int. Power Electron. Conf. ECCE ASIA*, Jun. 2010, pp. 1725–1732.

[14] Q. Cao, Z. Li, and H. Wang, "Wide voltage gain range LLC DC/DC topologies: State-of-the-art," in *Proc. Int. Power Electron. Conf. (IPEC-Niigata -ECCE Asia)*, May 2018, pp. 100–107.

[15] M. Escudero, D. Meneses, N. Rodriguez, and D. P. Morales, "Modulation scheme for the bidirectional operation of the phase-shift full-bridge power converter," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1377–1391, Feb. 2020.

[16] X. Ruan, "Soft-switching PWM full-bridge converters," in *Nanjing University of Aeronautics and Astronautics*. Beijing, China: Wiley, 2014, pp. 1–66.

[17] M. Ryu, D. Jung, J. Baek, and H. Kim, "An optimized design of bi-directional dual active bridge converter for low voltage battery charger," in *Proc. 16th Int. Power Electron. Motion Control Conf. Expo.*, Sep. 2014, pp. 177–183.

[18] B. J. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *IEEE Electron Device Lett.*, vol. 10, no. 10, pp. 455–457, Oct. 1989.

[19] J. Roig and F. Bauwens, "Overcoming switching limits in silicon power MOSFETs with silicon-based solutions," *IET Power Electron.*, vol. 11, no. 4, pp. 629–637, Apr. 2018.

[20] D. Costinett, D. Maksimovic, and R. Zane, "Circuit-oriented treatment of nonlinear capacitances in switched-mode power supplies," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 985–995, Feb. 2015.

[21] G. Liu, D. Li, Y. Jang, and J. Zhang, "Over 300 kHz GaN device based resonant bidirectional DCDC converter with integrated magnetics," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2016, pp. 595–600.

[22] Q. Haihong, X. Kefeng, N. Xin, Z. Ziyue, Z. Zhiyuan, and F. Dafeng, "Characteristics of SiC MOSFET and its application in a phase-shift full-bridge converter," in *Proc. IEEE 8th Int. Power Electron. Motion Control Conf. (IPEMC-ECCE Asia)*, May 2016, pp. 1639–1643.

[23] C. Fei, R. Gadelrab, Q. Li, and F. C. Lee, "High-frequency three-phase interleaved LLC resonant converter with GaN devices and integrated planar magnetics," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 653–663, Jun. 2019.

[24] IPP60R170CFD7. *600V CoolMOSTM CFD7 Power Transistor*. Accessed: Feb. 1, 2020. [Online]. Available: https://www.infineon.com/dgdl/Infineon-IPP60R170CFD7-DS-v02_01-EN.pdf?fileId=5546d4625e763904015ea3d82d3331b1

[25] IMZA65R027M1H. *650V CoolSICTM M1 SiC Trench Power Device*. Accessed: Feb. 1, 2020. [Online]. Available: https://www.infineon.com/dgdl/Infineon-IMZA65R027M1H-DataSheet-v02_00-EN.pdf?fileId=5546d4626f229553016f85d997f90532

[26] IGT60R070D1. *600V CoolGaNTM enhancement-mode Power Transistor*. Accessed: Feb. 1, 2020. [Online]. Available: https://www.infineon.com/dgdl/Infineon-IGT60R070D1-DataSheet-v02_12-EN.pdf?fileId=5546d46265f064ff016686028dd56526

[27] M. Escudero, M.-A. Kutschak, D. Meneses, D. P. Morales, and N. Rodriguez, "Synchronous rectifiers drain voltage overshoot reduction in PSFB converters," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7419–7433, Jul. 2020.

[28] G. Deboy, J. Hancock, M. Purschel, U. Wahl, and A. Willmeroth, "Compensation devices solve failure mode of the phase shift ZVS bridge during light-load operation," in *Proc. APEC. 17th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2002, pp. 988–993.

[29] L. Saro, K. Dierberger, and R. Redl, "High-voltage MOSFET behavior in soft-switching converters: Analysis and reliability improvements," in *Proc. INTELEC 20th Int. Telecommun. Energy Conf.*, Oct. 1998, pp. 30–40.

[30] L. Xie, X. Ruan, and Z. Ye, "Modeling of common-mode noise in phase-shift full-bridge converter," in *Proc. IECON 42nd Annu. Conf. IEEE Ind. Electron. Soc.*, Oct. 2016, pp. 1371–1375.

[31] M. Kutschak and M. Escudero. *3300 W 52 V LLC with 600 V CoolMOS CFD7 and XMC*. Accessed: Feb. 1, 2020. [Online]. Available: https://www.infineon.com/dgdl/Infineon-Evaluationboard_EVAL_3K3W_LLC_HB_CFD7-ApplicationNotes-v01_00-EN.pdf?fileId=5546d4626cb27db2016d3a60583725dc

MANUEL ESCUDERO was born in Granada, Spain, in 1983. He received the M.Sc. degree in computer engineering from the University of Almería, Almería, Spain, in 2010, and the M.Sc. degree in electronics engineering from the University of Granada, Granada, in 2016. In 2015, he joined Infineon Technologies Austria AG, where he is currently working as an Application Engineer for Power Management and Multimarket.

MATTEO-ALESSANDRO KUTSCHAK was born in Vienna, Austria, in 1977. He received the Dipl.Ing. (FH) degree in electronics engineering from Fachhochschule Technikum Wien, Vienna, in 2000. In 2000, he joined Artesyn-Technologies Vienna, where he remained as a Power Supply Design Engineer for telecom and server applications, until 2008. In 2008, he joined Infineon Technologies Austria AG, where he is currently working as a Principal Application Engineer for Power Management and Multimarket, and has collaborated in the definition of the HV semiconductor technologies for Si, SiC, and GaN. He has coauthored over 40 inventions and international patents.

NICO FONTANA was born in Gemona del Friuli, Italy, in 1990. He received the M.Sc. degree in electronics engineering from the University of Udine, Italy, in 2016. In 2016, he joined Infineon Technologies Austria AG, where he is currently working as an Application Engineer of high-voltage MOSFETs.

NOEL RODRIGUEZ received the B.Sc. and M.Eng. degrees in electronics engineering from the University of Granada, in 2004, and the double Ph.D. degree from the University of Granada and the National Polytechnic Institute of Grenoble, France, in 2008.

He is currently a Tenured Professor of electronics with the Department of Electronics and Computer Technology and the Co-Founder of the Pervasive Electronics Advanced Research Laboratory (PEARL) at the University of Granada. His current research interests include low-power energy conversion, electric mobility, and new materials and devices for electronic applications. He has coauthored 15 international patents and more than 100 scientific contributions. He received the First National Award of University Education. He also received the Extraordinary Award for his Ph.D. degree.

DIEGO PEDRO MORALES received the B.Sc., M.Eng., and Ph.D. degrees in electronics engineering from the University of Granada, in 2001 and 2011, respectively.

Since 2001, he has been an Associate Professor with the Department of Computer Architecture and Electronics, University of Almería, before joining the Department of Electronics and Computer Technology, University of Granada, in 2006, where he currently serves as a Tenured Professor. He is the Co-Founder of the Biochemistry and Electronics as Sensing Technologies (BEST) Research Group, University of Granada. His current research interests include low-power energy conversion, energy harvesting for wearable sensing systems, and new materials for electronics and sensors. He has coauthored more than 80 scientific contributions.