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Dual PN Source/Drain Reconfigurable FET for Fast and Low-Voltage Reprogrammable Logic

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ABSTRACT Schottky junction reconfigurable FETs suffer from limited output currents to drive the following stages, jeopardizing their viability for high-end applications. This drawback becomes dramatic at low voltages. In this work, an analogous novel low-bias reprogrammable device is presented. It features a dual PN doping at source and drain which improves the driving current density thanks to the presence of both electron and hole reservoirs within the same structure. 3D-TCAD results for this innovative device on advanced Silicon-on-Insulator technology are presented and compared with traditional reconfigurable FETs and CMOS structures.

INDEX TERMS Barrier, dual doping, fast logic, low-bias, polarity, reconfigurable, reprogrammable, RFET, Schottky.

I. INTRODUCTION

Reconfigurable Field-Effect Transistors (R-FET) [1] are being currently studied to implement circuits with custom on-the-fly logic functions [2], [3]. Their main benefit, the reprogrammable bipolar FET characteristic, is achieved via source/drain (S/D) metallic regions (typically Ni silicides) to induce lateral Schottky junctions (Fig. 1a). Carrier injection is then modulated through additional electrodes (polarity gates, PG) whose aim is to bend the semiconductor energy bands defining the dominant N or P polarity: positive voltages approach the conduction band to the metal workfunction favoring electron tunneling while negative voltages behave similarly for the valence band and holes. PGs also prevent the ambipolar current. The ON/OFF state is driven, as usual, by a control gate (CG). In order to feature symmetric N and P current branches, the S/D metal workfunction lies close to the mid energy band-gap to obtain analogous electron/hole Schottky barriers (SB). Deviations from mid-gap should compensate different carrier effective masses and mobilities. Nevertheless, the simplicity of this operation principle is as well the main drawback: since the SB cannot be modified to maintain the current symmetry, the carrier injection (through thermionic emission and quantum barrier tunneling) is, regardless the polarity, low and the Schottky R-FET performance is inferior to regular CMOS [4]. Changing the device geometry (nanowire, planar, FinFET...) or employing mobility enhancement strategies (strain, volume inversion...) are marginal boosts aiding to achieve the current symmetry goal but insufficient to solve the challenge: the output current is limited by the carrier injection mechanism. The unique solutions are to excessively rise the PGs bias to improve the SB tunneling impeding the low-voltage operation or employ low-bandgap materials as Ge [5] that also increase the OFF current and bring some integration and fabrication concerns. Experimental silicon results show R-FET currents consistently around or below 30 μA/μm [1], [6], [7] demonstrating this obstacle. Although R-FETs are not expected to beat regular FETs in terms of performance or integration density, as long as their output currents are not even close, they will be relegated to a second plane due to their drawbacks: complex routing, larger footprint, and additional polarity gate circuitry.

In this work, a novel structure featuring a PN dual doping (DD) profile at S/D edges of the channel, the DD R-FET, is proposed to enhance the driving current density (Fig. 1b). The DD R-FET replicates the Schottky R-FET structure but differs in the S/D side electrodes. The presence of both N- and P-type reservoirs solves the lack of carriers from Schottky R-FETs allowing larger current densities at analogous conditions. This is possible due to the much larger carrier

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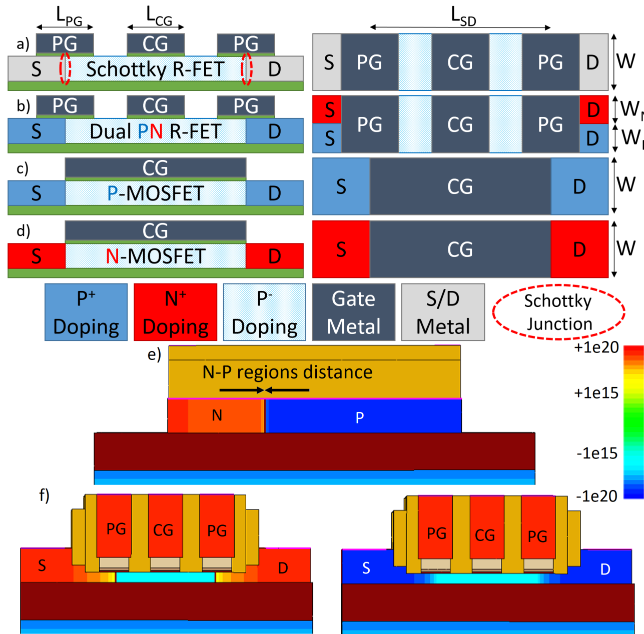

FIGURE 1. Side (left) and top (right) views of different FET structures implemented on Fully Depleted (FD) SOI: a) Schottky barrier Reconfigurable FET (R-FET) with S/D metal regions; b) the proposed dual doped PN R-FET with N+ and P+ S/D terminals; and regular c) P- and d) N-type MOSFETs. Half the PG covers the S/D terminals in R-FETs. Actual e) side and f) front and rear views (illustrating the device width and length, respectively and Gaussian doping profiles) of the dual doped R-FET. Note the nitride spacers in-between gates to account for fringing fields.

population availability in DD R-FETs. The carrier injection from BEOL access contacts is now ensured thanks to the high S/D doping that narrows the depletion region at the metal-semiconductor interface and allows easy carrier flow in both directions at any bias by tunneling [8], behaving as an ohmic contact. In this regard, the difference with Schottky R-FETs is that DD R-FETs feature a tunneling barrier-width that is always very thin and does not depend on any terminal bias.

The proposed device structure resembles a parallel N/P MOSFET combination with shared terminals (CG, PG and S/D) able to selectively be switched OFF combining the gates biasing. The use of both N- and P-type side terminals within the same device is not uncommon as found in body-contacted devices (such as H- or T-gate structures [9]), gated P-I-N diodes (Field-Effect diodes) [10]–[12], G4-FETs [14] or sharp switching FETs [13], [15], [16]. It should be highlighted that the device operation principles do not require perfect shallow N-P junctions at S/D (as will be shown later), i.e., the N and P doping profiles at source (or drain) might be spaced to comply with the manufacturing process (see Fig. 1e). This device concept can be extended to any device geometry and number of polarity/control gates, e.g. 2-gates nanowires [1] or 2-gates planar FD-SOI [4].

II. SIMULATIONS FRAMEWORK

Synopsys 3D-TCAD simulations [17] were employed to test and benchmark all four Fully-Depleted (FD) SOI (Silicon-On-Insulator) structures from Fig. 1. Poisson's, electron/hole continuity equations and density gradient [18], [19] (to deal with the vertical quantum confinement) were included by default. The mobility was fixed from experimental results [20] depending on the S/D spacing (L_{SD} in Fig. 1): $\mu_n \simeq$ 233-245 cm^2/Vs and $\mu_p \simeq$ 63-70 cm^2/Vs. The Wentzel Kramers Brillouin (WKB) model and non-local mesh were employed as an approximation for the quantum tunneling injection in case of the Schottky barrier R-FET. This model has proven to be consistent with experimental results as shown in [1]. Effective tunneling masses were fixed to $m_n^* = 0.16\ m_0$ and $m_p^* = 0.19\ m_0$ (which represent optimistic values and differ from previous works [21], [22]) and the Schottky S/D metal workfunction was assumed to initially be 4.6 eV. All top gates workfunctions (CG and PGs) are fixed to 4.7 eV. Band-to-band tunneling (BTBT) is initially neglected. Accounting for BTBT at the source and drain junctions slightly increases the ambipolar current if the closest polarity gate is strongly biased (as GIDL in traditional MOSFETs). However, No significant BTBT occurs between the N and P doped regions at S/D since the junction area is small and an electrode short-circuits both sides of the junctions. Nevertheless, it is always possible to space both doping profiles to further reduce this BTBT component.

Device architectures emulate the UTBB FD28 SOI technology [23]: $EOT \simeq$ 1.5 nm (HfO_2/SiO_2), $t_{Si} \simeq$ 7 nm, $t_{BOX} \simeq$ 25 nm, uniform p-type (Boron) wafer doping of $N_B \simeq 10^{16}$ cm^{-3} (essentially undoped devices in such small volumes) and Gaussian S/D doping profiles from STMicroelectronics FD-SOI fabrication flow with peaks of $N_{S/D} \simeq 10^{21}$ cm^{-3}. A $\simeq$15 nm silicon epitaxy is carried out at the ungated S/D regions to reduce the series resistance. The polarity- and control-gate lengths in R-FETs are fixed to 20 nm (without spacers) while the distance between them depends on the overall source-drain length, L_{SD}, which ranges from $\simeq$ 70 up to $\simeq$ 110 nm. The MOSFET CG extends throughout the whole S/D length. The total width is fixed in all devices to 0.2 μm (W or W_N+W_P). Lastly, the back-gate voltage, V_{BG}, is normally grounded unless specified otherwise.

III. TCAD RESULTS

Figure 2 depicts the DC $|I_D(V_{CG})|$ characteristics for all the test devices. Note that both Schottky and DD R-FETs exhibit bipolar behavior by simply adjusting the polarity-gate bias (Fig. 2a and b) which demonstrates the feasibility of employing the dual PN doped device for in-situ reconfigurable logic. The use of different supply voltages in RFETs to drive the SB height is usual but will not be mandatory for the DD RFET as will be shown later. The subthreshold swing (SS) is similar and always close to 80 mV/dec even with these short control-gates since the S/D influence is suppressed as well by the lateral PGs. The Schottky RFET exhibits a non-traditional dependence on the source-drain length due to the carrier availability at the source side. Observe that the dual doped PN device exhibits, as anticipated, larger output

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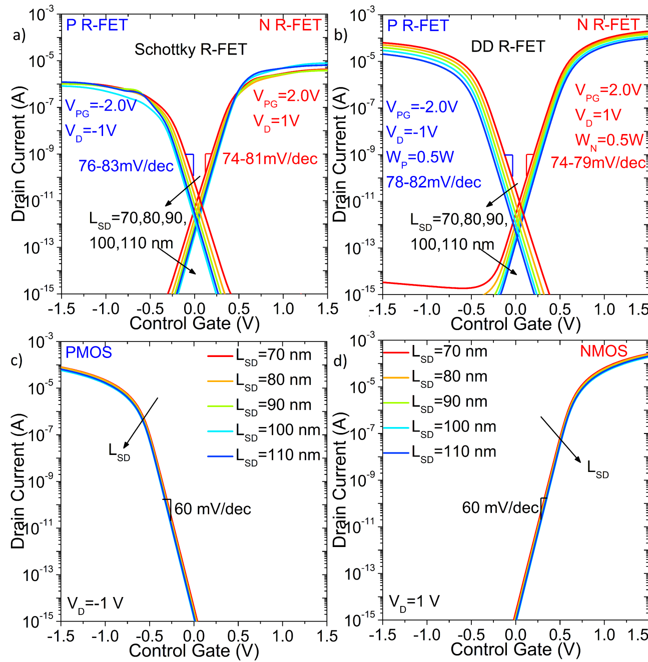

FIGURE 2. Static DC $|I_D(V_{CG})|$ curves for devices in Fig. 1: a) Schottky R-FET, b) Dual PN R-FET and FD-SOI c) P- and d) N-MOSFETs. $V_{BG} = V_S = 0$ V.

TABLE 1. Devices ON current for different biasing conditions, $V_{PG} = 1$ V (left) and 2 V (right). $V_{CG} = V_D = 1$ V and $V_S = V_{BG} = 0$ V.

Device	*Polarity*	*Ion (A)*	*Ion (A)*	*Width (nm)*
MOSFET	N	67.52 μ		200
	P	22.02 μ		200
Schottky R-FET	N	5.03 n	1.58 μ	200
	P	9.19 n	1.72 μ	200
DD R-FET	N	12.69 μ	48.93 μ	40
	P	17.84 μ	48.09 μ	160

currents than Schottky R-FETs. On the other hand, reference MOSFETs drive more current than any R-FET (even with lower gate biasing $|V_{CG}| = 1$ V in contrast to $|V_{PG}| = 2$ V), but unipolar, with reduced leakage and sharper switching ($SS \simeq 60$ mV/dec), which denotes the enhanced SCE (Short-Channel Effects) mitigation in ultra-thin FD-SOI (Fig. 2c and 2d). The simulated currents are summarized in Table 1 for easy comparison. Regular MOSFETs can be further scaled down, hence increasing their current, which cannot be easily achieved for any R-FET device (Schottky or doping-based). A more detailed comparison between Schottky R-FETs and planar FD-SOI MOSFETs can be found in [4].

The DD R-FET operation can be better understood by observing the source-to-drain carrier profiles, illustrated in Fig. 3 for the P-type polarity ($V_{PG} = -2$ V). On the one hand, the electron density is never high across the whole device, even at the N-side (Fig. 3a), due to the polarity gate-induced field preventing the simultaneous ambipolar operation. On the other hand, the hole inversion channel in-between the source and drain is not formed unless the control gate terminal is negatively biased and only at the P-side ($V_{CG} = -1.5$ V in Fig. 3d). This corresponds to the ON-mode of the device when all gates are negatively biased. The reciprocal N-type polarity analysis present analogous conclusions (not shown).

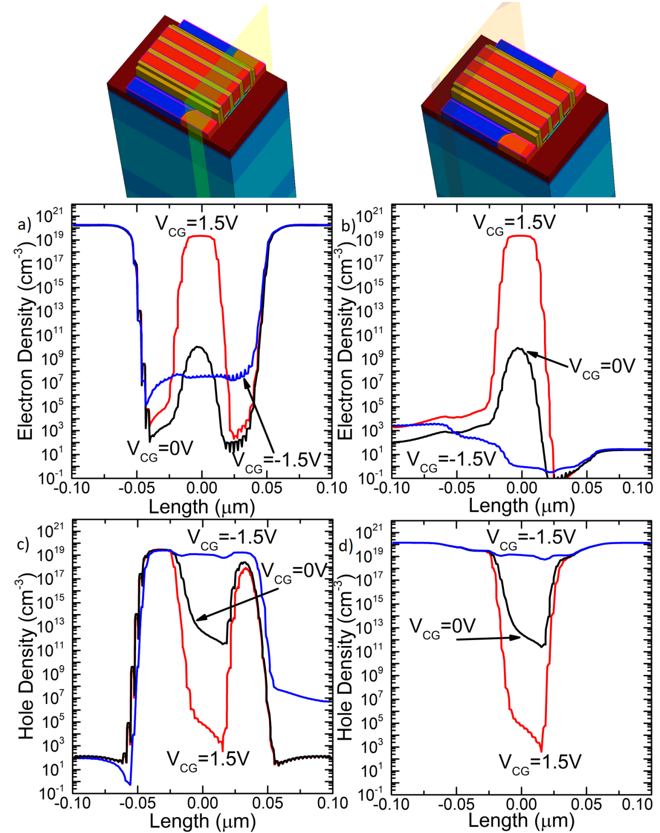

FIGURE 3. Carrier densities cuts (10 nm away from each edge of the device) along the length-axis (from source to drain) illustrating the different P-polarity ($V_{PG} = -2$ V) operation modes. a,b) electron and c,d) hole densities profiles along the a,c) N- and b,d) P-sides at S/D. $V_{BG} = V_S = 0$ V and $V_{DS} = -1$ V. $L_{SD} = 70$ nm. N-type ($V_{PG} = 2$ V) profiles are analogous but reciprocal.

Figure 4 illustrates the impact that the spacing (along the width direction as in Fig. 1e) in-between the adjacent N and P junction (either at the source, the drain or at both sides) has on the DD R-FET operation. Any non-zero distance implies a smoother doping profile transition from one species to the other. As expected, the current characteristics do not change because the operation does not rely on the junction properties. Indeed, as the two profiles are more distant from each other, the effective width increases as the net doping augments (doping profiles are less compensated) and the overall driving current is enlarged. Nevertheless, note that spacing the profiles negatively affects the final device footprint.

DD R-FETs achieve the symmetry by adjusting the N and P effective width ratio during the ion implantation (W_N and W_P in Fig. 1). Figure 5a shows that W_N modulation (hence $W_P = W - W_N$) controls the current in both branches enabling the current symmetry goal (around $W_N \simeq 0.2W$, induced by the N/P mobility ratio $\mu_n/\mu_p \simeq 233/63 \simeq 4$). In contrast, Schottky R-FET symmetry is much harder to

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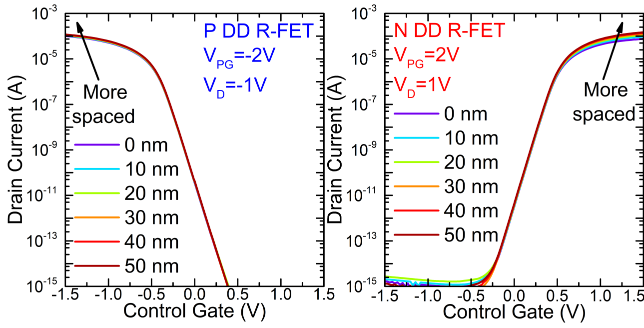

FIGURE 4. DD R-FET static DC $|I_D(V_{CG})|$ curves for different spacing between the N and P doping profiles at source and drain for a) N- and b) P-polarities. The distance is illustrated in Fig. 1e. $V_{BG} = V_S = 0$ V. $L_{SD} = 70$ nm.

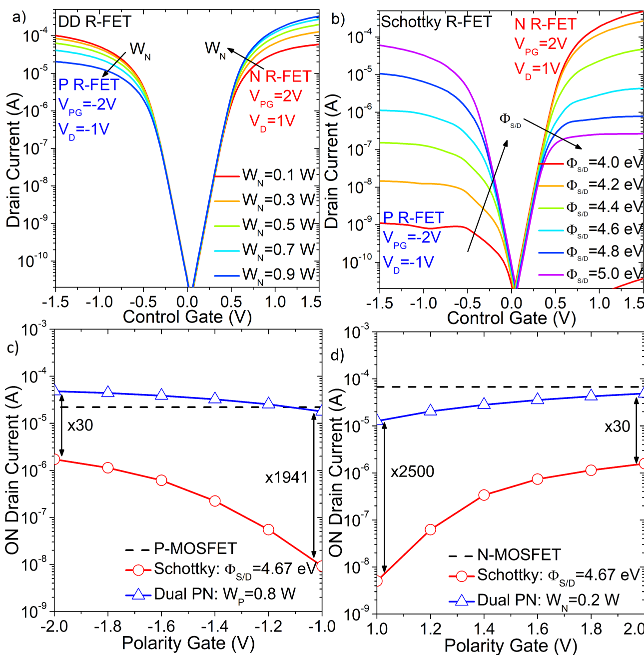

FIGURE 5. Current symmetry modulation in a) dual PN and b) Schottky R-FETs at same conditions ($|V_{PG}| = 2$ V). Polarity Gate bias impact on the ON current ($|V_{CG}| = |V_D| = 1$ V) for c) P- and d) N-type FETs once R-FETs are symmetric (Schottky: $\Phi_{S/D} = 4.67$ eV; Dual PN: $W_N = 0.2W$). $V_{BG} = V_S = 0$ V. $L_{SD} = 70$ nm.

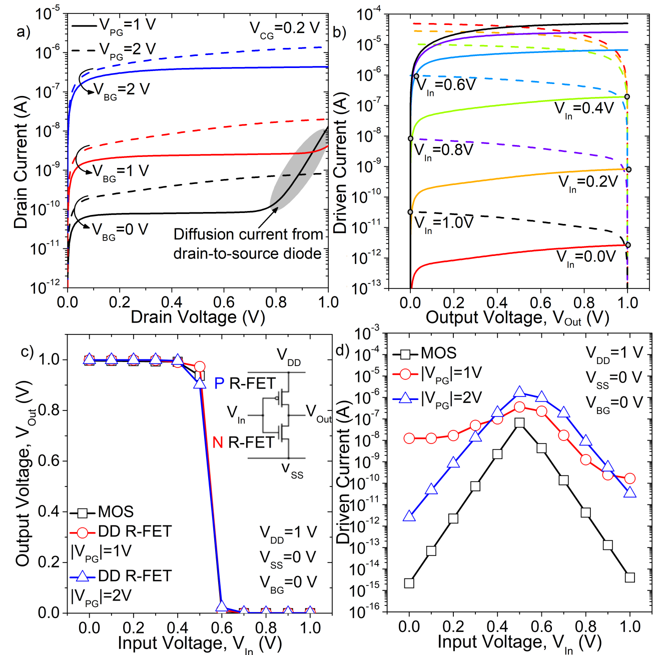

FIGURE 6. a) Dual PN R-FET DC $|I_D(V_D)|$ N-type curves showing the non-ideal diode diffusion current if the V_{PG} and/or V_{BG} are not strongly biased. b) DC $|I_D(V_D)|$ load curves for N- (solid lines) and P-type (dashed lines) dual PN R-FETs at $|V_{PG}| = 2$ V. Logic inverter response extracted from the previous load curves crossing points: c) output voltage and d) driving N/P current. $L_{SD} = 70$ nm, $V_{BG} = 0V$ and $W_N = 0.2 \cdot W$ ($W = 0.2$ μm).

achieve since it is based on the S/D metal workfunction adjustment ($\Phi_{S/D}$) which might suffer from complications with the silicidation process and fermi-level pinning [24], [25]. Figure 5b evidences the current balance when employing close to mid-gap workfunctions. Note that the current is only high, hence comparable to DD R-FETs and regular MOSFETs, for one carrier at a time: when $\Phi_{S/D}$ approaches the conduction or valence band.

Another essential parameter in R-FETs is the PG bias, responsible for suppressing the ambipolar OFF current which steadily rises when lowering $|V_{PG}|$. In Schottky R-FETs, PGs control the tunneling barrier width, hence available carriers, whereas in dual PN R-FETs, PGs induce closer heavily-doped S/D regions. The PG can be employed as well to correct current asymmetries. Figure 5c and 5d show the ON current ($|V_{CG}| = |V_D| = 1$ V) as a function of V_{PG}. Schottky R-FET strongly suffer from $|V_{PG}|$ reduction which dramatically limits the ON current. The impact on dual PN R-FETs is less severe and highlights an interesting point: the smaller effective width ($W_{N/P}$ compared to W) can be partially compensated by the closer S/D induced by the PGs and their higher bias ($|V_{PG}| > |V_{CG}|$). This explains why the dual PN R-FET can show even larger currents at lower width (Fig. 5c). Dual PN R-FETs are therefore more suitable than Schottky R-FETs for low-voltage circuits and faster reprogrammable logic presenting output currents 30 to 2500 times higher (at $|V_{PG}| = 2$ and 1 V, respectively) and appropriate for single-supply voltage operation. This advantage however might be slightly mitigated in multi gate devices [26], [27] (RFETs with additional gates in series for improved logic functions) where the extra series resistance is expected to impact more on the DD RFET than on the SB RFET.

IV. LOGIC INVERTER RESPONSE

The logic inverter gate response is extracted by analyzing the load $I_D(V_D)$ curves for N and P-type R-FETs [28]. Fig. 6a shows the undesired lateral diode forward biasing at high $|V_{DS}|$ degrading the OFF current. This effect is important if $|V_{DS}|$ is high enough (typically around $\simeq E_g/q$ due to the high S/D doping concentrations) and the diode can be forward biased. As a result, the $I_D(V_D)$ curve exhibits an

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exponential growth in the OFF state. This effect is only significant when the drift MOS-like current is very low ($|V_{CG}| \simeq 0$ V) but can be suppressed by the PG bias (or even the back-gate terminal). Furthermore, this diffusion component should not represent a problem for low-voltage operation as V_{DS} would be insufficient to abate the junction built-in barrier.

The dual PN R-FET load curves for N and P-type R-FETs are shown in Fig. 6b with $|V_{PG}| = 2$ V without observing diode diffusion currents. The crossing points, at fixed CG voltage (V_{In}), provide both the output voltage (V_{Out}, Fig. 6c) and dynamic N/P-MOSFET driving current (Fig. 6d). The FDSOI MOS inverter behavior, showing an optimized performance, has also been included for easy comparison. The resultant DD R-FET transfer characteristic demonstrates an almost perfect voltage inverter behavior following the MOS inverter. The current while switching is controlled by the PG bias. It is larger than for the NMOS and peaks at the voltage transition as expected.

CONCLUSION

A novel RFET approach, the DD R-FET, has been proposed without the need of lateral Schottky junctions thanks to a dual PN doping profile at source and drain.

3D-TCAD simulations demonstrate the benefits of implementing such dual doped structure with respect to regular Schottky reconfigurable devices. Results show current improvements above 30 times higher at identical footprint and biasing condition, maintaining similar electrostatic control (SS). Note that DD R-FETs cannot be employed for dopant-free CMOS implementations. Nevertheless, DD RFETs present many other advantages with respect to Schottky RFETs that makes these novel devices more appealing: i) easier fabrication since there is no need for lateral S/D silicidation steps to achieve the Schottky contacts; ii) Lower silicidation variability without Fermi-level pinning issues which might jeopardize the reconfigurable current symmetry; iii) full CMOS process compatibility without expected exotic metals impeding the CMOS co-integration to solve fabrication challenges and reduce costs; iv) greatly enhanced output current for fast logic or larger capacitances/fan-out stages (even when accounting for optimistic Schottky RFETs parameters); v) precise and simple n/p current modulation through mask set width definitions; vi) possibility of using mobility enhancement strategies to further boost the performance and vii) suitable for low-voltage/power applications as DD R-FETs are fully functional at reduced biasing conditions.

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