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On the Low-Frequency Noise Characterization of Z^2-FET Devices

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ABSTRACT This paper addresses the low-frequency noise characterization of Z^2-FET structures. These double-gated p-i-n diode devices have been fabricated at STMicroelectronics in an ultrathin body and box (UTBB) 28-nm FDSOI technology and designed to operate as 1T-DRAM memory cells, although other applications, as for example electro static discharge (ESD) protection, have been reported. The experimentally extracted power spectral density of current reveals that the high-diode series resistance, carrier number fluctuations due to oxide traps, and gate leakage current are the main noise contributors at high-current regimes. These mechanisms are expected to contribute to the degradation of cell variability and retention time. Higher flicker noise levels have been reported when increasing the vertical electric field. A simple model considering the contribution of the main noise sources is proposed.

INDEX TERMS 1T-DRAM, noise measurement, p-i-n diodes, semiconductor device reliability, silicon on insulator technology, Z^2-FET.

I. INTRODUCTION

One of the best positioned alternatives to overcome the scaling limitations of the One-Transistor, One-Capacitor (1T1C) Dynamic Random Access Memory (DRAM) cells is the one-transistor DRAM (1T-DRAM) structure [1]–[3]. Inside this approach, a novel solution has been the implementation of the Z^2-FET device as 1T-DRAM cell [4], [5]. The Z^2-FET structure is formed by a double-gated p-i-n diode with four terminals: anode (A), cathode (K) and front/back gates (FG/BG). The body is split into two different regions, the one covered by the top-gate and adjacent to the anode (L_n), and the ungated and unsilicide one (L_p) close to the cathode, Figure 1.a. The memory operation is based on inducing high vertical energy barriers through a complementary gate biasing scheme ($V_{FG} > 0\,V$ and $V_{BG} < 0\,V$). These energy barriers block the current flow in forward condition ($V_A > 0$) and the Z^2-FET operates as a Shockley diode [6], Figure 1.b. Only when the anode voltage (V_A) is high enough to allow the carriers to overcome the gate-induced energy barriers, $V_A > V_{ON}$ (triggering voltage), the Z^2-FET recovers the p-i-n diode behavior. As Figure 1.c shows, this bias condition (V_{ON}) significantly depends on the front-gate voltage (V_{FG}). The memory operation is achieved shifting V_{ON} as a function of the logical memory state by temporarily modifying the amount of charge stored under the front gate. If V_{ON} remains below the reading bias condition (V_{AR}) the current level will be high ('1'-state), otherwise the current will present a low level ('0'-state) when $V_{ON} > V_{AR}$. In comparison with other 1T-DRAM approaches [1]–[3], the Z^2-FET operation is not based on any degrading mechanism such as impact ionization or band-to-band tunneling, expecting higher reliability.

The Z^2-FET operation as memory cell has already been modeled and exhaustively characterized in previous works demonstrating promising results such as over $15Mb/mm^2$ integration density and potentially tens of *ms* retention times [7]–[10]. Additionally, its performance inside a memory matrix has been satisfactorily evaluated [11] as well as Electro Static Discharge protection [12]. However, it has been reported that, compared to thicker gate oxide Z^2-FETs [7], thinning the insulator yields lower performance in terms of retention time and stability of the logic states during holding [13]. Despite some works have assessed the scalability and the fabrication process dependence on the memory

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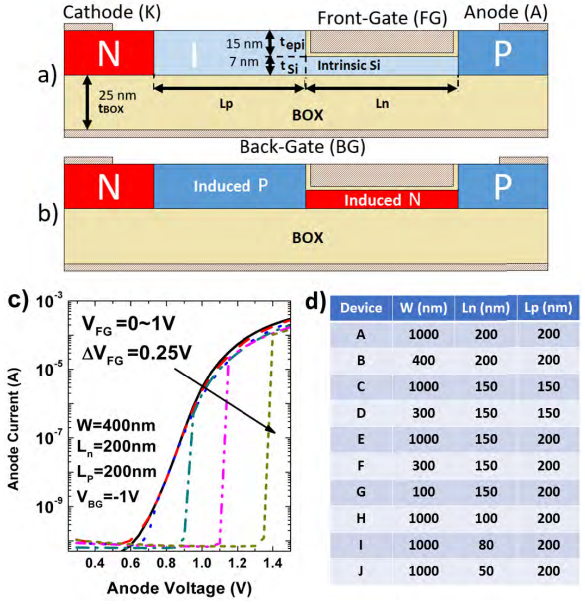

Device	W (nm)	Ln (nm)	Lp (nm)
A	1000	200	200
B	400	200	200
C	1000	150	150
D	300	150	150
E	1000	150	200
F	300	150	200
G	100	150	200
H	1000	100	200
I	1000	80	200
J	1000	50	200

FIGURE 1. 2-D Z²-FET structure in (a) equilibrium (same potential in all terminals), p-i-n diode and (b) under normal memory operation inducing a virtual n-p-n-p doping via gate-biasing ($V_{FG} > 0$ V, $V_{BG} < 0$ V and $V_A = V_K = 0$ V). (c) Experimental characterization of the anode current as a function of the anode voltage for different front-gate bias conditions, T = 300K. V_{ON} voltage associated with the steep slope increases with the gate voltage. (d) Dimensions of the different devices tested in this work.

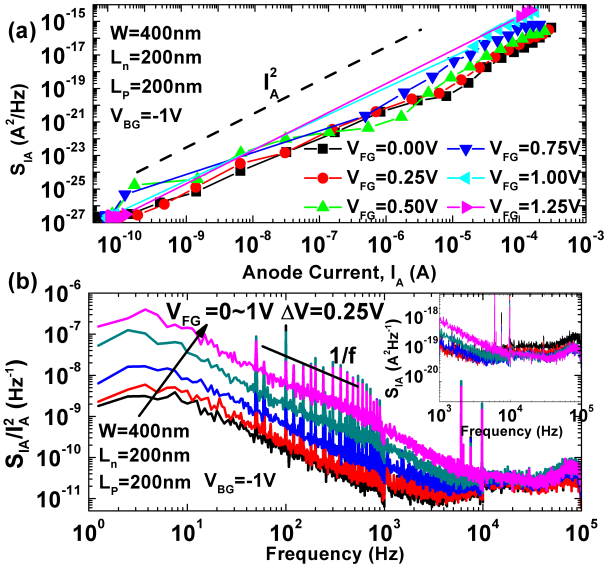

FIGURE 2. (a) Current noise spectral densities as a function of anode current for different front-gate biases at $f = 10Hz$. (b) Normalized noise spectral density in the frequency domain for the same bias conditions as in (a). The inset shows a zoom in frequency of the power density of the noise without current normalization. Higher noise plateaus are observed for higher anode current levels. T = 300K.

performance [14], the instability sources are still not entirely determined and an in-depth study of the reliability of these devices is desirable. Charge in the '1'-state can leak away from the body either by recombination or by tunneling through the gate oxide. On the other hand, carrier generated by temperature or field-assisted mechanisms will compromise the '0'-state. In many cases, these processes are assisted by defects in the body or at the interface with the gate dielectric. In this regard, in our search of the possible sources of noise and variability, we have experimentally characterized, for the first time, the low-frequency noise signature of scaled Z²-FET devices at similar biasing conditions as when they operate as memory cell.

The considered Z²-FET devices were fabricated in 28-nm STMicroelectronics ultra-thin-body and BOX fully-depleted silicon-on-insulator (UTBB FD-SOI) technology featuring a high-k/metal gate stack [15] (physical dimensions depicted in Figure 1.a). Specifically Metal Silicide/TiN/HfO_2/SiO_2 materials have been used to assemble a gate thickness around 3.1 nm. The length and width of the evaluated devices are illustrated in Figure 1.d. The low-frequency noise characterization was carried out using a low-noise-current amplifier connected to a software-based spectrum analyzer [16].

II. RESULTS AND DISCUSSION

Firstly, the noise characteristic of Z²-FET device is shown in Figure 2 at different front-gate voltages: at weak vertical electric field where the device works as a p-n diode and, once the p-i-n diode behavior is recovered after overcoming the virtual n-p-n-p induced energy barriers (strong lateral and vertical electric fields). Figure 2.a depicts the noise power spectral density as a function of the anode current. Curves almost follow a quadratic trend with the anode current, $S_{IA}(f) \propto I_A^2$, instead of the linear dependence expected in regular diodes associated with shot noise contribution ($S_{shot} = 2qI_A$) [17]. This behavior, also reported in works dealing with p-i-n and gated diodes [18], [19] and in transistors, is attributed to $1/f$ noise processes [17]. Note in Figure 2.a that, when the energy barriers are built, there are no intermediate current levels, only '0' or '1' states, i.e., the current sharply jumps between the low and high levels. In order to clarify the low-frequency noise origin, Figure 2.b depicts the normalized noise power in frequency domain. The spectral signature presents an unambiguous 1decade/1decade slope followed by a plateau, characteristics associated with the flicker (1/f) and shot noise contributions, respectively [20]–[22]. This latter contribution of the shot noise has been corroborated in the inset of Figure 2.b, where lower front gate voltages (weak energy barriers) imply higher anode currents and thus an increase in the noise level.

The presence of flicker ($1/f$) noise is attributed either to fluctuations in the number of carriers due to trapping/detrapping mechanisms [20], or due to variations in the carrier mobility [22]. Additionally, it is noticeable in both figures the existence of an increment of the noise power for high vertical electric fields, even in normalized current levels, demonstrating a gate voltage dependence of the noise signature. To shed light on the noise components, Figure 3.a depicts the normalized noise power spectral density as a function of the anode current for different gate biases. At weak front-gate bias (black and red lines), the normalized noise spectral density presents a drop with the anode current (below

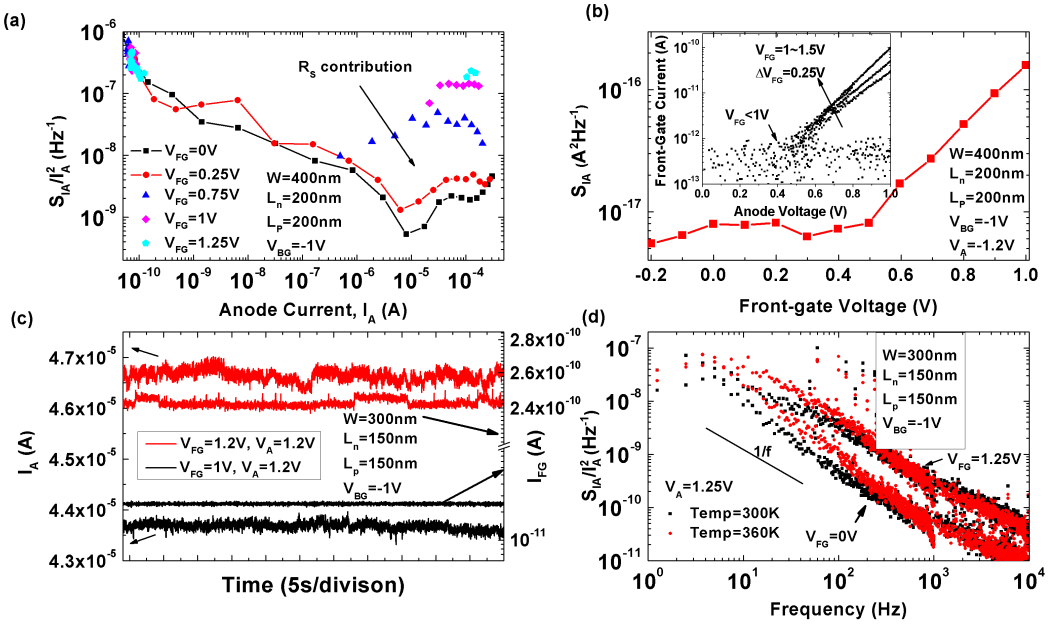

FIGURE 3. Normalized power spectral densities of noise: (a) as a function of I_A (anode voltage sweeps at constant V_{FG}) and (b) as a function of the front-gate voltage at $V_A = 1.2V$ and $f = 10Hz$. (c) Anode and gate currents evolution with the time for two different high gate biases where trapping and detrapping event are discernible in both cases. The gate current increases with the gate voltage. (d) Normalized power noise spectral density as a function of the frequency for two different gate voltages and temperatures. Temperature increases the low frequency noise according to trapping-detrapping mechanisms.

$I_a < 10\mu A$). This almost linear inverse dependence of the noise in the channel current is usually attributed to the carrier mobility fluctuations observed in bulk devices, as diodes or BJT transistors [22]. However, at high current regime ($I_a > 10\mu A$), where the series resistance (R_S) of the diode limits the effective anode voltage dropping on the Z^2-FET, hence its current, a noticeable increment of the noise is observed. The increasing noise level as a function of the current suggests that the series resistance, which contributes with a flicker ($1/f$) noise component [23]–[25], becomes more significant than the intrinsic resistance contribution (decreasing with the higher anode current) [25]. Regarding the vertical electric field dependence, note that the noise power density increases with V_{FG} at high current regimes, suggesting additional noise mechanisms. This statement can be clarified through the analysis of the noise signature with variable front-gate bias as Figure 3.b shows. For the sake of simplicity, a static high anode voltage has been selected ($V_A = 1.2V$) to maintain the device in '1'-state regardless of the applied vertical field (V_{FG}). As observed, the noise level remains constant at weak vertical electric field ($V_{FG} < 0.5V$ in this particular case) while the device is operating without high-energy barriers, indicating that there is no noise dependence with V_{FG} in this regime. However, at higher gate voltages ($V_{FG} > 0.5V$) the noise rises in agreement with the $1/f$ noise excess observed in Figure 2.b. Analysis of the time signature of the anode and gate currents for low and high gate voltages, Figure 3.c, shows both a significant gate leakage current increase (also observed in the inset of Figure 3.b) exhibiting several current levels (Random Telegraph Signals) and a higher number of fluctuations in the anode current for the highest gate voltage. This front-gate bias dependence suggests surface noise components as the trapping-detrapping events due to interface and oxide traps (usually reported with Lorentzian features and also treated as Generation-Recombination noise) and the contribution of the gate-current noise as additional noise mechanisms at high vertical electric fields [24]. Moreover, measurements at higher temperature (360K) were conducted, Figure 3.d. The noise excess observed at higher temperature (red symbols) can be explained by the temperature dependence on the trap activation (more trapping and detrapping events are expected at high temperature) and the higher gate current experimented in the device (not shown). Since the retention time of this thin-oxide device is limited by the fall of the '1'-state (loss of the stored charge) during the holding operation (high vertical electric field and low anode bias) [13], these gate tunneling and trapping/detrapping events at the interface are the main responsible of the retention disturbance. These results are in agreement with the higher gate tunneling levels measured in wider devices (not shown) and shorter retention times [13].

In order to isolate the noise contributions and to determine how the device scaling affects its reliability, Figure 4 extends these considerations to devices featuring different lengths and widths (summarized in Figure 1.d). Figure 4.a reinforces the idea that the devices are mainly affected by large series diode resistance (when the vertical electric field is low): the noise follows the characteristic monotonic slope attributed to a large R_S [23], [24], [26] and higher noise levels are observed for narrower devices [27] since $R_S \propto 1/W$. On the

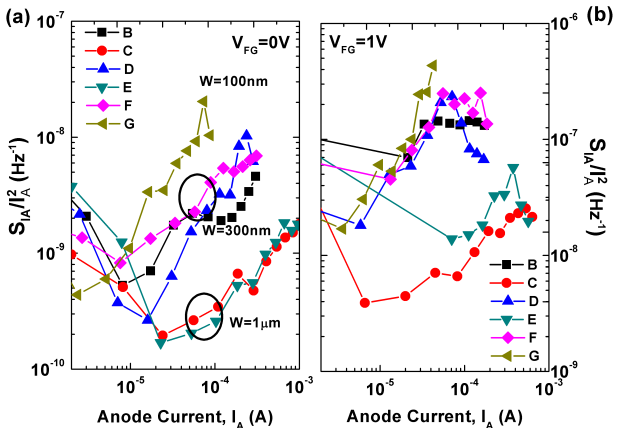

FIGURE 4. Normalized current noise spectral densities as a function of anode current for devices featuring different intrinsic region lengths at (a) $V_{FG} = 0\ V$ and (b) $V_{FG} = 1\ V$. Frequency $f = 10Hz$. T = 300K.

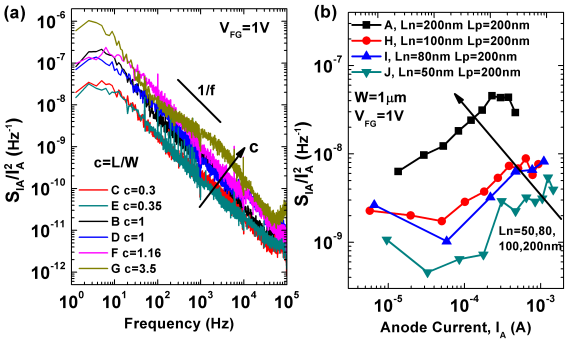

FIGURE 5. Normalized current noise spectral density as a function of: (a) the frequency for devices with different dimensions, (b) the anode current for devices with different gate lengths at frequency $f = 10\ Hz$. T = 300K.

other hand, Figure 4.b corroborates that increasing the front-gate voltage, higher noise levels are observed due to the contribution of interface and gate oxide traps and the higher gate leakage current. Note that, to make more effective this comparison only results above V_{ON} are presented since no intermediate values are measurable for the case of Figure 4.b (high vertical electric field). At this point, we cannot neglect that the higher V_{FG} increases the intrinsic resistance (R_{in}) of the device and consequently the noise level due to the formation of the barriers and the reduction of carrier density through diffusion. It is worth noting that the noise levels at $V_{FG} = 1V$ are one order of magnitude higher, which should be attributed to the simultaneous contribution of surface noise mechanisms and the increase of the intrinsic resistance. Figure 5.a shows the normalized noise spectral density under bias conditions where all the noise contributions take place. The flicker noise component increases according to the diode series and intrinsic resistances enlargement due to width reduction and length increase, respectively. Note that the dimension ratio $c = L/W$, expected to be proportional to the total diode resistance [27], is shown corroborating the resistances increase. Indeed, higher V_{ON}, I_{ON} and memory window variability, and '0'-state degradation have been demonstrated in [13] for narrower devices at high anode voltages, corresponding with this noise excess. Additionally, a noticeable hump (around $f = 10^3$Hz) conforming a $1/f^2$ trend in Device *G* suggests that this device is affected by a single trap (Random Telegraph Noise) for this specific bias condition, explained by the reduced dimensions of this device and corroborating the surface noise mechanisms.

Regarding the gate length of the devices, Figure 5.b shows the normalized spectral density of the noise for devices with the same width and different gated region lengths at high V_A. As observed, the shorter the device length, the lower the spectral noise level. This observed noise drop is due to the reduction of gate dimensions which implies a R_{in} reduction, a decrease of active interface and oxide traps and lower gate leakage currents [24]. This fact highlights the need to scale properly the device dimensions in order to mitigate the noise contributions which disturb the memory operation.

According to the previous analysis and assuming that the noise sources are not correlated, the anode current fluctuations of the Z²-FET can be modeled as the sum of the contributions of the different mechanisms mentioned:

$$\frac{S_I}{I^2} = \frac{1}{R_t^2}\left(\frac{\alpha_{in} R_{in}^2}{fN_{in}} + \frac{\alpha_S R_S^2}{fN_S} + 4KTR_t\right) + 2q/I + \frac{S_{1/f}}{I^2} \quad (1)$$

where the flicker noise corresponding to the mobility fluctuations is modeled [22], [25] as $\frac{\alpha_{in} R_{in}^2}{fN_{in} R_t^2}$, while the flicker noise contribution of the series resistance reads as [23], [25], [28] $\frac{\alpha_s R_S^2}{fN_S R_t^2}$, where R_{in} and R_S are the intrinsic body and series resistances, respectively, and R_t their joint contribution [25] ($R_S + R_{in}$). N_{in} and N_S are the effective charge number of carriers and α_{in} and α_S are the Hooge constants. The term $4KT/R_t$ models the thermal noise of the resistances, $2q/I$ the normalized contribution of the shot noise associated with carrier injection through the $p-n$ junctions [17] and $\frac{S_{1/f}}{I^2}$ the contribution of the surface noise mechanisms which follows a $1/f$ trend in frequency domain [20], [26], [29]. This latter contribution can be seen as the sum of the fluctuation in the number of carriers (trapping and detrapping) at the interface and oxide gate traps and an additional term regarding the gate leakage noise contribution [24], as the previous analyses of Figure 3.c and 3.d have suggested. Therefore, the surface noise contribution can be modeled as $S_{1/f} = S_{trap} + \alpha_D^2 S_{ig}$, where the first term is related to the carrier number fluctuations (trapping/detrapping phenomena in oxide traps) and the second one to the gate leakage current. The noise spectral density of the fluctuation in number of carriers due to multiple traps corresponds to [20], [30]:

$$\frac{S_{trap}}{N^2} = 4\sum_i \frac{\Delta N^2}{N^2} \frac{\tau_i}{1 + (2\pi f \tau_i)^2} \quad (2)$$

where the current noise spectral density follows a $1/f$ trend when several traps are energetically activated with different characteristic times τ. This noise power spectral density depends on the gate bias and the temperature as it was shown in Figure 3. In case of single actived trap, as the case of

Device G in Figure 5.a, the noise level follows a $1/f^2$ trend. On the other hand, the anode noise excess due to the gate leakage current is modeled by $\frac{\alpha_D^2 S_{ig}}{I^2}$ where α_D is gate-partitioning coefficients, and S_{ig} the gate-current noise spectral density at constant anode voltage [24].

III. CONCLUSIONS

In this work, the low-frequency noise characterization of Z^2-FET devices has been carried out for the first time. The noise power presents a $1/f$ trend which depends on the bias and temperature conditions. The analysis suggests that the increase of the diode series resistance is the main contributor to the noise at high anode current and low vertical field. This noise is increased by the down-scaling of the device width. When high vertical fields are applied, there is an additional surface noise component due to the contribution of trapping events and the gate leakage current, demonstrating an excess noise at high temperature. The trapping events are observed in the time signature of the anode and gate currents suggesting trap assisted tunneling as the gate leakage mechanism. These effects can be responsible for the lower retention time documented in thin gate oxide Z^2-FET memory cells. A simple model taking into account the different noise contributions has been proposed. Finally, we can conclude that the down-scaling of the length dimension of the devices contributes to mitigate the noise of Z^2-FET as it reduces the intrinsic resistance of the diode and the gate leakage current.

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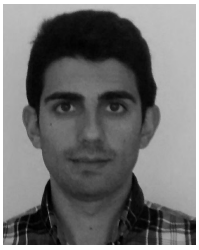

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