

# Gate capacitance performance of p-type InSb and GaSb nanowires

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**Abstract**—The electrostatic behavior of p-type nanowires made of antimonide III-V materials (InSb and GaSb) is analyzed by means of a self-consistent solution of the Poisson and Schrödinger equations, under the  $k$ - $p$  approximation. The results are compared to those achieved for Si and Ge NWs, and the contribution of each of the capacitance terms (quantum and inversion layer capacitances) is thoroughly analyzed.

**Keywords**- III-V semiconductors, p-type semiconductors, gate capacitance.

## I. OBJECTIVE AND NUMERICAL APPROACH

III-V nanowires (NWs) have attracted extensive research interests in recent years because of their unique physical properties. For the practical implementation of CMOS circuits based on NWs, p-channel FETs are needed. Several materials are currently being investigated as technologically relevant p-type semiconductors. In particular, increasingly more attention has been focused on InSb and GaSb owing to their excellent hole transport properties [1]. In this work we study the electrostatic properties of small NWs made of these materials and carry out a comparison with equivalent devices based on Si and Ge.

While the effective mass approximation (EMA) can be used to describe the Conduction Band (CB) of most semiconductors, this approach fails in the description of the Valence Band (VB) and more complicated models have to be employed to take into account the coupling of the different subbands forming the VB (Heavy Holes, Light Holes and Split-Off). Moreover, the coupling between the VB and the CB has to be considered for direct small-gap materials, such as III-V compounds. Thus, to analyze p-type NWs, we have developed a numerical tool that self-consistently solves the Poisson and the Schrödinger equations, being the VB described by means of an eight-band  $k$ - $p$  model which accounts for the coupling between the VB and the CB. For indirect group IV semiconductors, a simplified six-band  $k$ - $p$  model has been used, since the coupling of the CB and the VB is considered as negligible. To accurately reproduce the cylindrical geometry while taking into

account crystal anisotropy, the Finite Elements Method has been employed to discretize and solve the resulting equation system [2].

## II. RESULTS

In this study we have considered a cylindrical NW with 5nm diameter, oriented along the [111] direction. Four different devices have been simulated, each of them corresponding to the following materials: InSb, GaSb, Si and Ge. In all the cases, the same insulator ( $\text{Al}_2\text{O}_3$ ) with a thickness of 1.5nm has been used. This way, identical contribution of the insulator capacitance for all NWs is attained, so that we can focus on the channel material behavior. Fig. 1 shows the bandstructure at a gate overdrive voltage of -0.4V. The energy is referred to the VB edge, and the Fermi level ( $E_F$ ) is depicted by a dashed grey line. The threshold voltage ( $V_T$ ) is calculated from the maximum of the second derivative of the charge with respect to the gate voltage [3]. A quite different scenario is observed between Si and the other three channel materials. The former shows a large number of bands per unit energy with a lower curvature, which corresponds to a higher DOS and higher effective mass as compared to the latter. Fig. 2 presents the gate capacitance behavior as a function of the gate overdrive voltage. As shown, despite the noticeable differences found in the band structure of each of the studied NWs, the performance in terms of the  $C_G$  is quite similar for all of them. To analyze this effect, we have separated and depicted the three terms determining the gate capacitance: quantum capacitance ( $C_q$ ), centroid capacitance ( $C_C$ ) and insulator capacitance ( $C_{\text{ins}}$ ) [4].  $C_q$  behaves as expected from the DoS of each material, with the largest value achieved by the Si NW, and the lowest by the InSb one. As for the  $C_C$  term, it is strongly related to i) the dielectric constant of the semiconductor, and ii) the charge centroid position. As the dielectric constant of Si is lower than the one of the other materials, a lower  $C_C$  in the subthreshold regime is achieved for Si, as the charge is basically placed at the same position regardless the employed material. This can be checked by depicting the charge centroid position (Fig. 3), which has been calculated as in [4]. As the gate overdrive voltage is

increased, the centroid of III-V NWs and Ge becomes larger than the calculated for Si devices. This fact produces a compensation of the higher values of their dielectric constant, and, as a consequence, the  $C_G$  values for the four considered devices become very similar.

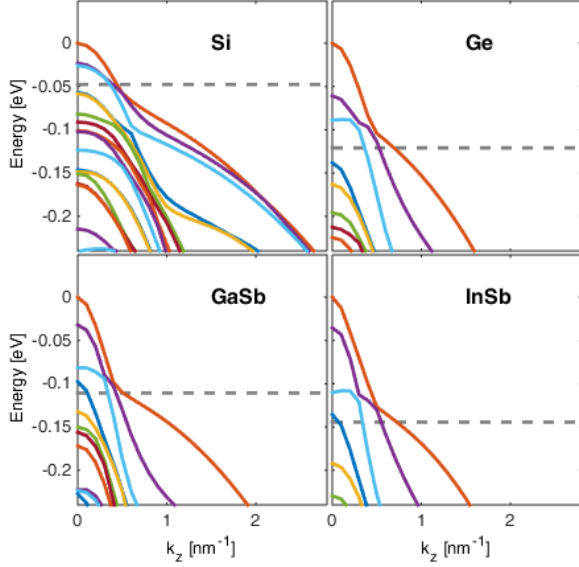


Figure 1. Band structure achieved at  $V_G - V_T = -0.4V$  for the four devices under study. The energy is referred to the maximum value of the VB, while the Fermi energy is depicted as a horizontal dashed line.

### III. CONCLUSION

A numerical simulator that self-consistently solves the Poisson equation and the eight-band  $kp$  method in the cross section of 5nm cylindrical NWs has been developed. A comprehensive study of the electrostatic performance of this device has been carried out focusing on p-type channels and four different materials: Si, Ge, InSb and GaSb. Our results indicate that, in spite of their low effective mass and small density of states, GaSb and InSb NWs hold the comparison with Si and Ge in terms of gate capacitance and inversion charge. The good electrostatic performance, combined with the expectation of excellent transport characteristics, place GaSb and InSb as attractive alternatives for p-type devices on CMOS logic based on NWs.

### ACKNOWLEDGMENT

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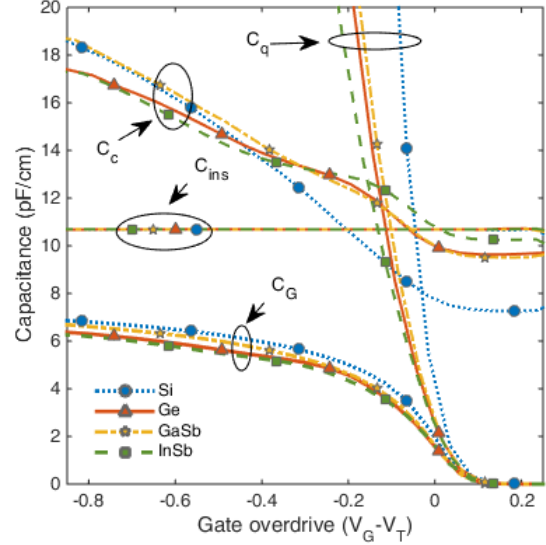


Figure 2. Gate capacitance ( $C_G$ ) as a function of the gate overdrive voltage ( $V_G - V_T$ ).  $C_G$  can be calculated as the series combination of the three other terms depicted:  $C_{ins}$ ,  $C_c$  and  $C_q$ .

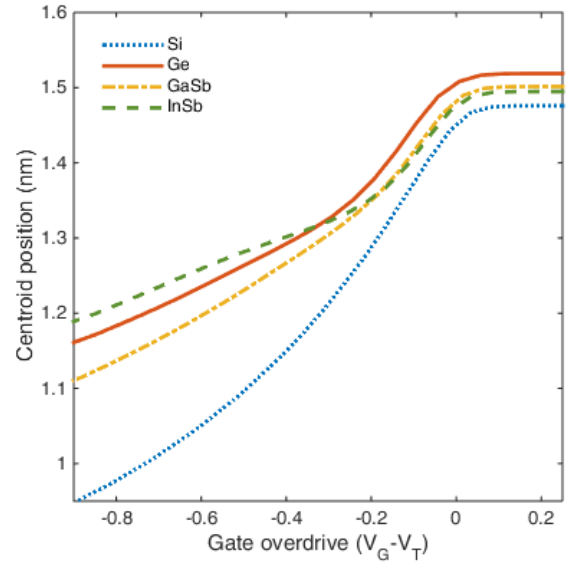


Figure 3. Charge centroid position as a function of  $V_G - V_T$  for each of the devices under study. The centroid is referred to the semiconductor/insulator interface, i.e., a larger centroid implies a higher separation of the charge from the insulator.