First Experimental Demonstration of III-V Capacitor-less DRAM Cells down to 14 nm Gate Length

Carlos Navarro†*, Siegfried Karg‡, Carlos Marquez†, Santiago Navarro†, Clarissa Convertino‡, Cezar Zota‡, Lukas Czornomaz‡ and Francisco Gamiz†

Semiconductor-based memories are essential elements of today's electronics. With the upcoming Internet of Things (IoT) era, the number of interconnected devices is growing exponentially and so does the memory market. In this work, III-V single-transistor dynamic RAM cells are experimentally demonstrated for the first time. In particular, indium gallium arsenide on insulator (InGaAs-OI) transistors, operating as MSDRAM (Meta-Stable Dip RAM) cells, are analyzed for different geometries. Experimental results show different current levels for each logic state proving the successful memory behavior down to 14 nm gate length. This work confirms the feasibility of employing III-V materials to implement aggressively scaled dynamic memory cells without an external capacitor for III-V embedded applications.

A significant research effort in the memory field to implement new solutions and to optimize the existing ones has been lately carried out and is still ongoing[1]. In this respect and beside Magnetoresistance RAM (MRAM)[2], Resistive RAM (ReRAM)[3] or Phase-change memory (PCM)[4] alternatives, different dynamic RAM (DRAM) candidates have been recently proposed based on the floating-body effect (FBE)[5]: ARAM[6], A2RAM[7–9], MSDRAM[10] or the Z^2-FET[11–15]. This innovative approach allows to get rid of the external capacitor and to reduce the manufacturing complexity while simultaneously minimizing the cell footprint. All these FBE-based contenders[6–8,10–12,16,17] have been already experimentally demonstrated in silicon but there are few reports for other materials such as III-Vs yet. III-V channel materials are uniquely

† University of Granada, 18071 Granada, Spain. *E-mail: carlosnm@ugr.es
‡ IBM Research Zürich, CH-8803 Rüschlikon Switzerland.

positioned to provide lower MSDRAM operating voltage (down to 0.5 V), due to increased electron mobility, as well as allow for band-gap engineering to optimize hole generation through band-to-band tunneling in the floating body. Previous studies are either exclusively based on TCAD results[18–21] or have been mainly focused on co-integrating silicon and III-V elements to improve the capacitor-less cells performance[22]. This paper reports the first experimental demonstration of III-V transistors operating as a capacitor-less DRAM (1T-DRAM) cell. Furthermore, memory behavior down to 14 nm gate length is evidenced, resulting in the shortest gate length 1T-DRAM demonstration to date. Due to the simplicity of operation and easier fabrication, the MSDRAM concept[10] was verified in indium gallium arsenide (InGaAs).

Single-transistor DRAM principles

The information in traditional DRAM cells (formed by one transistor and one capacitor) is read by sensing the potential variation due to the charge displacement between the capacitor plates. On the other hand, the idea behind 1T-DRAM cells, featuring no external capacitor, is to store the charge representing the information within the transistor body. As the charge modulates the inner device electrostatics, different current levels (associated with each logic state) are achieved enabling the memory operation.

An MSDRAM cell[10] is originally based on three mechanisms: i) inter-gate coupling between front and back interfaces[23]; ii) floating-body effect[5] and iii) non-equilibrium conditions[24]. Available holes in the body are accumulated at the front channel thanks to a negative V_{FG} while the back interface is driven into inversion (fixed positive V_{BG}). The back-channel inversion level is modulated by the inner hole density. For instance, few holes yield a body potential drop inducing, by inter-gate coupling, an increase in the back-gate threshold voltage and thus a lower back-channel inversion. Limited current densities ($I_0 \equiv$ '0'-state, Fig. 1a) are then sensed afterwards if pulsing the drain voltage to read (R). In contrast, larger hole densities provide greater drain currents ($I_1 \equiv$ '1'-state, Fig. 1b). Fig. 1c schematically depicts the logic state

difference when modulating the inner hole population. Charge evacuation (W_0, Fig. 1d) is induced by capacitive coupling ($V_{FG} > 0$ V and $V_D = 0$ V) while band-to-band (BtB) tunneling at the drain edge arises as the preferred mechanism ($V_{FG} < 0$ V and $V_D > 0$ V) to inject the charge inside the body (W_1, Fig. 1e,f).

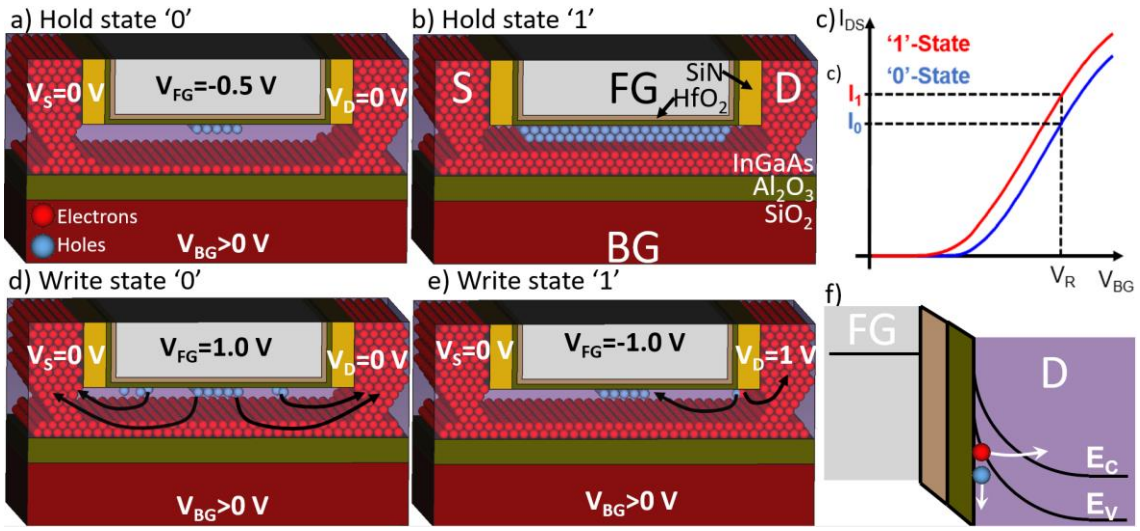

Fig. 1 | MSDRAM basics: logic states and programming operation details. a Logic '0'- and **b** '1'-state hold (H) operation of an MSDRAM cell. The driven current flows through the back channel while the top interface is used to store the information (as positive charge, holes) thanks to the front gate-induced potential well and FBE[5] in SOI technology. Free holes gather at the front channel to modulate, by inter-gate coupling, the back-channel inversion and modify the cell conductance. **c** Sensing logic state discrimination for a constant reading voltage (V_R). **d,e** Programming mechanisms to eject by capacitive coupling (W_0 in **d**) or introduce by band-to-band tunneling (W_1 in **e**) holes from/into the body. **f** Detail of the body hole injection mechanism by band-to-band tunneling (GIDL) at the drain edge: the strong biasing between front gate and drain enables the energy bands to bend allowing electron tunneling from the valence to the conduction band. Schematics **a**,**b**,**d**,**e** do not show the silicon substrate in-between the buried oxide and the back-gate terminal for simplicity.

III-V transistors as 1T-DRAM cells

General purpose n-type InGaAs-OI (InGaAs On Insulator) transistors integrated on Si substrates were fabricated by IBM Research Zürich. Samples feature a relatively thin InGaAs channel layer of ≈20 nm, thick enough to avoid the supercoupling effect[25–27] and enable the memory operation. The grown In mole fraction corresponds to $In_{0.53}Ga_{0.47}As$[28–31], which provides a balance between on and off state performance, through high electron mobility and relatively large band gap, respectively. To prevent carriers from escaping through the slightly p-type doped silicon substrate, the body lies on-top of an Al_2O_3/SiO_2 buried insulator bi-layer (BOX) thicknesses with 10/25 nm, respectively. No dedicated ground-plane (GP) is present, making difficult the efficient application of back-gate biasing schemes: the back-gate electrode (BG) is located at the bottom side of the wafer. A thin Al_2O_3/HfO_2 high-k front-gate (FG) insulator, with close to 4 nm overall thickness, is employed to ensure good front-channel electrostatic control (the equivalent front oxide thickness, EOT, is around 1 nm). Both source and drain (S/D) regions are raised 25 nm reducing the access series resistance while 9 nm thick SiN_x spacers (l_{SP}) are formed to isolate the gate stack from S/D. A transmission electron microscopy (TEM) image of a scaled III-V transistor with approximately $L_G \approx 14$ nm is illustrated in Fig. 2a. In regard to the doping concentrations, S/D raised terminals are n-type with $N_D \approx 2 \cdot 10^{19}$ cm^{-3}. These two lateral doping profiles do not significantly extend below the gate stack, limiting the carrier injection through GIDL and the memory performance. Additionally, the body is residually n-type doped with around $2 \cdot 10^{16}$ cm^{-3} which could as well negatively impact on the optimum behavior.

2D TCAD Simulations

In order to test the memory operation of this structure, standard 2D TCAD simulations were initially conducted using the Synopsys tool[32]. The employed structure, Fig. 2b, reproduced the same architecture as in experimental devices, Fig. 2a. Fig. 2c shows the anode current readout validating different current levels according to the previous biasing conditions. The electron and hole densities after programming are plotted in Fig. 2d,e demonstrating the MSDRAM operation in these devices: high hole and electron densities (top and bottom interfaces, respectively) are reached after writing '1'-state, W_1, while after W_0 both populations are reduced. Due to the high V_{BG} voltage and the residual body doping, the electron density after W_0 is not negligible and the '0'-state current is significant, as will be discussed in the next section.

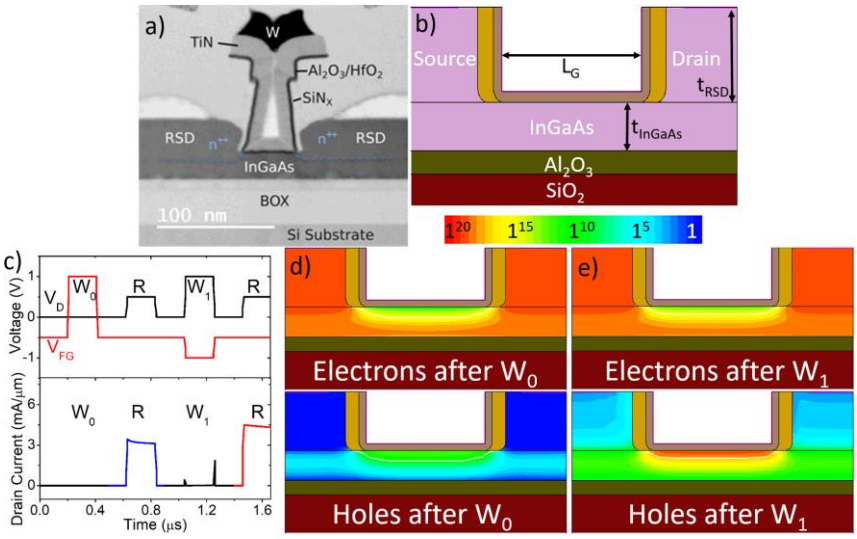

Fig. 2 | InGaAs-OI transistor structure and non-calibrated TCAD results. a TEM image for a ≈14 nm length device fabricated at IBM Research Zurich. **b** Corresponding 2D structure used in simulations with L_G=90 nm. Al_2O_3/HfO_2 front-oxide thickness, t_{FOX} ≈ 4 nm, III-V layer thickness, t_{InGaAs} ≈ 20 nm, SiO_2 buried-oxide thickness, t_{BOX} ≈ 10+25 nm, raised source/drain epitaxy thickness, t_{RSD} ≈ 30 nm, and SiN gate stack lateral spacers, L_{SP} ≈ 9 nm. N-type source/drain and body doping: $N_{S/D} = 2\cdot 10^{19}$ cm^{-3} and $N_B = 2\cdot 10^{16}$ cm^{-3}. **c** Applied voltages and drain current

readout demonstrating the memory operation (the logic current levels are overestimated due to the default InGaAs constant mobility model. Electron and hole densities, after **d** W_0 and **e** W_1 respectively, demonstrating the MSDRAM memory operation in similar structures to the experimental devices: successful hole evacuation/injection modulating the readout current (electron population). V_{BG} = 5 V, V_S =0 V, L_G = 90 nm and W = 1 μm.

Experimental results

Fig. 3 illustrates the front and back static switching characteristics as a function of the opposite gate terminal bias for distinct III-V cell aspect ratios. The strong front-gate control over the top channel is easily observed with well-defined transfer curves, especially when limiting the back interface to depletion or accumulation regimes, Fig. 3a,b,e,f. Moderate front subthreshold swings (SS_{FG}) are found with over ≈150 mV/dec (V_{BG} = 0 V for L_G=90 nm) and above 200 mV/dec (V_{BG} = 0 V for L_G=14 nm) demonstrating the impact of short-channel effects (SCE) on the electrostatic control. Given the thin EOT and body, the high SS_{FG} also reveals the presence of interface defects at the gate/channel interface[5]. As the back-gate voltage increases, the current flow gradually switches from the top to the bottom channel. The inversion channel shifts towards the back interface flattening the current as it becomes more insensitive to the front-gate electrostatic control. This relation confirms the inter-gate coupling[23] effect enabling the MSDRAM operation.

Regarding the back-interface current in Fig. 3c,d,g,h, significant differences can be discerned with respect to the top channel: the larger subthreshold swing (SS_{BG}>1,000 mV/dec at V_{FG}=0 V for L_G = 14 nm) reflects the poor back-gate electrostatic control due to the ineffective back-gate terminal: i) there is no GP to effectively terminate the electric field lines, ii) the back gate contact goes through the whole substrate and iii) the BOX dielectric is thicker than at the front interface. These limitations imply that the body electrostatic potential mainly follows the front

gate, typically negatively biased. As a result, large back-gate voltages must be employed to drive the back channel. However, the maximum back-gate voltage is restricted to avoid reliability concerns[33]. Interestingly, in the $I_D(V_{BG})$ curves, two separate current onsets can be distinguished reflecting the threshold voltage for each channel. As for the top interface, the drain current hump gradually shifts to lower back-gate voltages manifesting again the interface coupling.

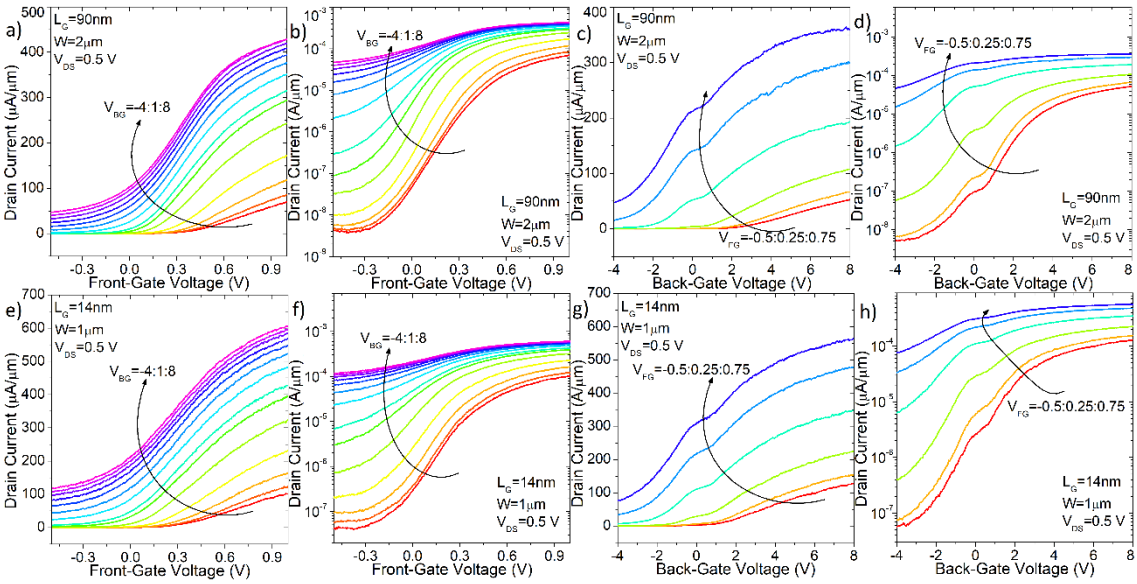

Fig. 3| Front and back-channel static DC operation for two III-V InGaAs-OI transistors. a,b,e,f Front- and **c,d,g,h** back-channel switching characteristics in linear (**a,c,e,g**) and logarithmic (**b,d,f,h**) scales for L_G=90 nm (**a,b,c,d**) and L_G=14 nm (**e,f,g,h**). Typical MOS-like switching characteristics observed. V_S = 0 V and V_D = 0.5 V.

The transient memory operation is depicted in Fig. 4 for different cell sizes. Several biasing conditions, with distinct drain and gate voltages during the programming ($W_{0/1}$), reading (R) and holding were tested to optimize the memory current ratio (I_1/I_0), not shown. The selected pattern is shown in Fig. 4a and follows a W_0-5xR-W_1-5xR sequence. The resultant readout drain

current is illustrated in Fig. 4b-d successfully proving, for all considered geometries, distinct logic states according to the programming operation: lower and higher drain currents after W_0 and W_1, respectively. Note that the '0'-state current is not negligible as highlighted before with the simulations due to the residual n-type body doping. A V_{BG}=2 V is not high enough for L_G=90 nm, Fig. 4b, and the drain current is low. On the other hand, short-channel effects in downscaled cells allow them to employ limited back-gate voltages and still obtain significant current levels, Fig. 4c,d. However, the impact of SCE is not always beneficial and degrades the current ratio (I_1/I_0) and margin (I_1-I_0) when moving from L_G=20 to 14 nm (Fig. 5c). It is worth remarking that, with L_G=14 nm, this cell represents the shortest gate length 1T-DRAM experimental demonstration so far.

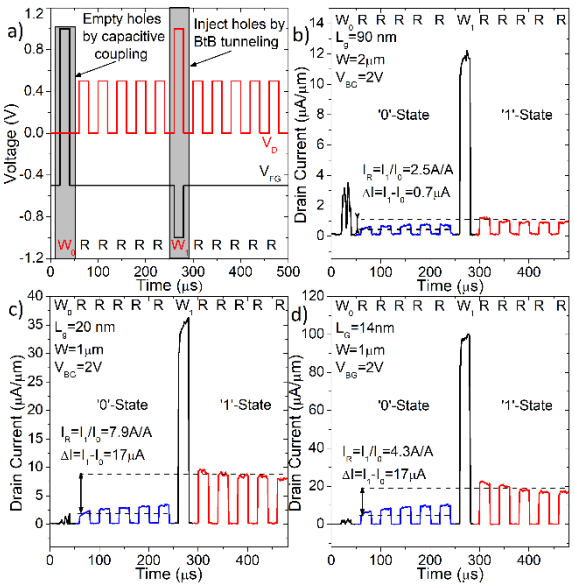

Fig. 4 | Experimental III-V InGaAs-OI capacitor-less DRAM cell demonstration for distinct geometries. a W_0-5xR-W_1-5xR sequence bias pattern to test the memory operation. **b,c,d** Drain current readout successfully probing the memory behavior for **a** L = 90 nm (W = 2 μm), **b** L = 20 nm (W = 1 μm) and **c** L = 14 nm (W = 1 μm). V_S = 0 V.

Cells can be operated at lower biasing conditions at the expense of lower performance as indicated in Fig. 5a, a 1.5 V bias range (all terminals comprised) is possible, strongly reducing the '1'-state programming current by 95% and making the cell more suitable for low-power applications. Fig. 5b,c show the memory current levels and ratio as a function of the back-gate voltage. Typical $I_D(V_G)$ switching-like curves are found when increasing the back-gate bias for both '1' and '0'-states (Fig. 5b) reflecting the inversion of the back-channel with different front-surface potentials (hole concentrations) as predicted in Fig. 1c. While the current margin rises with V_{BG}, the ratio gradually vanishes (Fig 5c): it is not possible to enhance simultaneously both metrics and a tradeoff arises. Curves in Fig. 5c follow the same dependence on the back-bias as found by TCAD simulations[34]. Fig. 5d illustrates the current levels for different mask-gate lengths. The shape of both curves matches the expected MOS current dependence on the length and further validates the MSDRAM operation in the III-V cells.

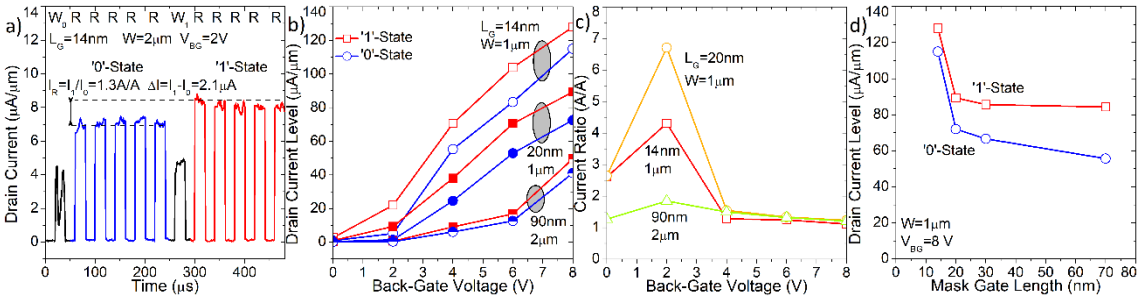

Fig. 5 | Low power demonstration, current levels and ratio as a function of back-gate voltage and length. a Transient anode current response to a low bias pattern (W_0: V_{FG}=0.75 V ; W_1: V_D=0.5 V and V_{FG}=-0.75 V with other biasing as in Fig. 5a) illustrating the low-current W_1 operation. '1' and '0'-state **b** current levels and **c** current ratio for different geometries as a function of the back-gate voltage. **d** Current levels as a function of the gate length at constant width (W=1μm). V_S = 0 V.

Note that slight ‘0’ and ‘1’ -state degradations are observed with time in Fig. 4: the ‘0’-state is perturbed by SRH (Shockley-Read-Hall) thermal generation and parasitic GIDL injection increasing the hole population towards the ‘1’-state, hence the drain current. On the other hand, the ‘1’-state current decay is related to an initial hole overpopulation where excess holes rapidly recombine or leak at the side S/D reducing the current. These mechanisms perturbing the hole population are ultimately responsible of limiting the cell retention time. Fig. 6a depicts a 50 ms constant reading operation after programming from which the retention time can be extracted. Notice how both current level overlay after a given time reflecting the stationary conditions when stored states are already lost. Fig. 6b shows a worst-case retention time of slightly over 3 ms (room temperature) for L_G=14 nm, enough for fast embedded applications. The dependence on the back-gate voltage is represented in Fig. 6.c: the retention decreases for larger V_{BG} due to reduction in the potential well where holes are stored increasing the leakage and the recombination enhancement between top hole and bottom electron channels.

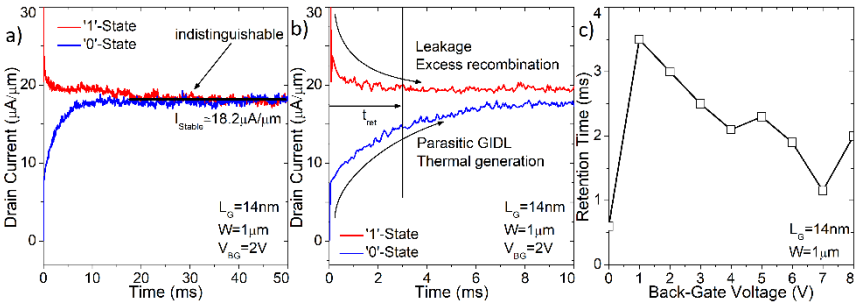

Fig. 6 | Experimental retention time on ultra-scaled InGaAs-OI cell. ‘1’ and ‘0’-state current levels evolution with time reflecting the hole body concentration perturbation with time due to different mechanisms. **a** Continuous reading proving state lost with time and current overlay between states (same applied voltages as in Fig. 5a). **b** Detail from Fig. 6a demonstrating a worst-case (continuous reading yields larger parasitic GIDL than holding due to the larger drain bias) retention time of 3 ms at V_{BG}=2 V. **c** Retention time extracted for

different back-gate biases confirming systematic retention over 1 ms at V_{BG}>0 V. The retention time is defined as the time the '0'-state takes to increase a 50% towards the stable current level (18.2 μA/μm). Same reading and programming conditions as those found in Fig. 5a.

The InGaAs MSDRAM performance and behavior can be explained by several mechanisms[34]: i) although the GIDL injection mechanism was expected to be enhanced due to the lower energy band-gap of $In_{0.53}Ga_{0.47}As$ with respect to Si[35] (≈ 0.74 eV compared to ≈ 1.12 eV at 300 K), the reduced S/D doping profile concentration[36] limits the effective injection due to the lowering in the drain-gate vertical electric field; ii) the lower energy band-gap may cause parasitic hole injection to occur, not only close to the drain, but also along the whole front interface and during other memory operations such as holding, impacting on the memory retention performance; iii) the larger InGaAs intrinsic carrier concentration[35] (≈ $6.3 \cdot 10^{11}$ cm^{-3} compared to ≈ $1.5 \cdot 10^{10}$ cm^{-3} in silicon) restricts the effective front-gate induced potential well where holes are accumulated thanks to the FBE (the lateral built-in potential between the body and the lateral source and drain regions is reduced and the current level margin and ratio drop with respect to silicon). On the other hand, as shown in this work, the InGaAs 1T-DRAM cells exhibit higher performance at low operating voltages due to the reduced band gap and high electron mobility of the InGaAs channel material.

Discussion

Single transistor DRAM cells were implemented and experimentally validated in InGaAs-OI transistors. Distinct current levels were achieved by modulating the stored hole population within the body in different geometries, demonstrating ultra-high scaling down to 14 nm mask-gate length. The promising 1T-DRAM performance is expected to be further improved, among other solutions, via optimized doping profiles and a dedicated ground plane electrode. This work opens up several other avenues of research to either optimize the demonstrated

memory performance in InGaAs-OI cells or through further band-gap engineering and exploration of heterostructures in 1T-DRAM architectures employing III-V materials.

Methods

Substrate fabrication. The InGaAs-On insulator wafer was obtained by metal organic chemical vapor deposition (MOCVD). UTBB InGaAs-OI samples fabrication begins with a (100)-oriented InP donor wafer. An $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ etch-stop heterostructure is then grown at 550ºC followed by the growth of the $In_{0.53}Ga_{0.47}As$ active layer. Subsequently, the wafers are loaded in an Atomic Layer Deposition tool (ALD) where the Al_2O_3 buried oxide (BOX) is deposited at 250ºC on top, capping the active layer. Later the target wafer is transferred to the substrate (100)-oriented p-type Si wafer by direct wafer bonding (DWB). Both wafers are brought into contact at room temperature and ambient atmosphere to initiate the bonding, achieved by a later annealing process. More details can be found in [37] for an analogous process.

III-V transistor fabrication. Following dummy gate deposition and patterning, SiNx spacers were formed by plasma-enhanced atomic layer deposition (PEALD) and dry etching. Selective MOCVD regrowth of $In_{0.53}Ga_{0.47}As$ raised source/drain (RSD) was achieved using a low temperature Sn doping process. A Si CMOS-compatible replacement gate process with high-k/metal gate completes the fabrication.

Instrumentation and electrical characterization. III-V samples were electrically characterized at room temperature (≈ 300 K) employing a Süss Microtech 300 mm semi-automatic wafer prober station along with an Agilent B1500A semiconductor device analyzer. Static analyses were carried out with standard High-Resolution Source-Measurement-Unit (HRSMU) while transient studies employed two arbitrary waveform generators (WGFMU from a B1530 expansion module). The applied memory patterns were custom-designed where the bias sequence timing was selected to guarantee low impact of parasitic RC contribution from cables and connectors: rising/falling times of 50 ns and pulse width typically of 20 μs (although faster operation is possible, see simulations results, Fig.2c). Noisy curves are the result of non-ideal contact between probes and device pads.

Simulation Framework. Non-calibrated 2D numerical simulations were performed using Synopsys tools (version N-2017.09)[32] to validate the inner cell operation. Density gradient, Fermi statistics, Auger, radiative and SRH generation/recombination models were accounted at room temperature, 300 K. The energy band-gap and dielectric permittivity match those found in [35]. The cell structure was built taking the TEM image architecture (Fig.2a) as reference with source/drain Gaussian doping profiles ($6{\cdot}10^{19}$ cm-3) and residual n-type body doping ($2{\cdot}10^{16}$ cm-3). The TiN front-gate work-function was set to 4.6 eV. Mobility follows the constant mobility model. Gate-induced

drain leakage by band-to-band tunneling was also considered in the drain region to model the hole generation at negative front-gate voltages to program the memory logic '1'-state.

Data availability. The data supporting the plots within this paper and other findings in this study are available from the corresponding author upon reasonable request.

References

1. Moore, M. International Roadmap for Devices and Systems. 23 (2016).
2. Hung, C. C. *et al.* High density and low power design of MRAM. *IEDM Tech. Dig.* 575–578 (2004). doi:10.1109/IEDM.2004.1419225
3. Zhuang, S. T. H. and W.-W. Electrically Programmable Resistance Cross Point Memory. US 6,531,371 B2 (2001).
4. Simpson, R. E. *et al.* Interfacial phase-change memory. *Nat. Nanotechnol.* **6,** 501–505 (2011).
5. Colinge, J.-P. *Silicon-on-Insulator Technology: Materials to VLSI*. (Springer US, 2004). doi:10.1007/978-1-4419-9106-5
6. Rodriguez, N., Gamiz, F. & Cristoloveanu, S. A-RAM memory cell: Concept and operation. *IEEE Electron Device Lett.* **31,** 972–974 (2010).
7. Rodriguez, N. *et al.* Experimental Demonstration of Capacitorless A2RAM Cells on Silicon-on-Insulator. *IEEE Electron Device Lett.* **33,** 1717–1719 (2012).
8. Gámiz, F., Rodriguez, N., Navarro, C., Marquez, C. & Cristoloveanu, S. Tri-Dimensional A2-RAM Cell: Entering the Third Dimension. in *Functional Nanomaterials and Devices for Electronics, Sensors and Energy Harvesting* 105–124 (2014). doi:10.1007/978-3-319-08804-4_6
9. Rodriguez, N. *et al.* Experimental developments of A2RAM memory cells on SOI and bulk substrates. *Solid. State. Electron.* **103,** 7–14 (2015).
10. Bawedin, M., Cristoloveanu, S. & Flandre, D. A capacitorless 1T-DRAM on SOI based on dynamic coupling and double-gate operation. *IEEE Electron Device Lett.* **29,** 795–798 (2008).
11. Wan, J., Le Royer, C., Zaslavsky, A. & Cristoloveanu, S. A Compact Capacitor-Less High-Speed DRAM Using Field Effect-Controlled Charge Regeneration. *IEEE Electron Device Lett.* **33,** 179–181 (2012).
12. Navarro, C. *et al.* Extended Analysis of the Z2-FET: Operation as Capacitorless eDRAM. *IEEE Trans. Electron Devices* **64,** 4486–4491 (2017).
13. Cristoloveanu, S. *et al.* A review of the Z 2 -FET 1T-DRAM memory: Operation mechanisms and key parameters. *Solid. State. Electron.* **143,** 10–19 (2017).
14. Navarro, S. *et al.* Experimental Demonstration of Operational Z2 -FET Memory Matrix. *IEEE Electron Device Lett.* **39,** 660–663 (2018).
15. Navarro, C. *et al.* Z2-FET as Capacitor-Less eDRAM Cell For High-Density Integration. *IEEE Trans. Electron Devices* **64,** 4904–4909 (2017).
16. Wann, H.-J. W. H.-J. & Hu, C. H. C. A capacitorless DRAM cell on SOI substrate. *Proc. IEEE Int. Electron Devices Meet.* 635–638 (1993). doi:10.1109/IEDM.1993.347280
17. Okhonin, S., Nagoga, M., Sallese, J. M. & Fazan, P. A SOI capacitor-less 1T-DRAM concept. in *2001 IEEE International SOI Conference. Proceedings (Cat. No.01CH37207)* 153–154 (IEEE, 2001). doi:10.1109/SOIC.2001.958032
18. Navarro, C. *et al.* Towards InGaAs MSDRAM Capacitor-Less Cells. *ECS Trans. 2018* **85,** 195–200 (2018).
19. Yoon, Y. J. *et al.* Capacitorless one-transistor dynamic random access memory based on

double-gate GaAs junctionless transistor. *Jpn. J. Appl. Phys.* **56,** (2017).
20. Yoon, Y. J., Seo, J. H. & Man Kang, I. Capacitorless one-transistor dynamic random-access memory based on asymmetric double-gate Ge/GaAs-heterojunction tunneling field-effect transistor with n-doped boosting layer and drain-underlap structure. *Jpn. J. Appl. Phys.* **57,** 04FG03 (2018).
21. Bawedin, M., Uren, M. J. & Udrea, F. DRAM concept based on the hole gas transient effect in a AlGaN/GaN HEMT. *Solid. State. Electron.* **54,** 616–620 (2010).
22. Pal, A. *et al.* GaP source-drain vertical transistor on bulk silicon for 1-transistor DRAM application. in *2013 5th IEEE International Memory Workshop* **2,** 192–195 (IEEE, 2013).
23. Hyung-Kyu Lim & Fossum, J. G. Threshold voltage of thin-film Silicon-on-insulator (SOI) MOSFET's. *IEEE Trans. Electron Devices* **30,** 1244–1251 (1983).
24. Bawedin, M., Cristoloveanu, S., Flandre, D. & Udrea, F. Dynamic body potential variation in FD SOI MOSFETs operated in deep non-equilibrium regime: Model and applications. *Solid. State. Electron.* **54,** 104–114 (2010).
25. Eminente, S., Cristoloveanu, S., Clerc, R., Ohata, A. & Ghibaudo, G. Ultra-thin fully-depleted SOI MOSFETs: Special charge properties and coupling effects. *Solid. State. Electron.* **51,** 239–244 (2007).
26. Navarro, C. *et al.* Supercoupling effect in short-channel ultrathin fully depleted silicon-on-insulator transistors. *J. Appl. Phys.* **118,** (2015).
27. Cristoloveanu, S., Athanasiou, S., Bawedin, M. & Galy, P. Evidence of Supercoupling Effect in Ultrathin Silicon Layers Using a Four - Gate MOSFET. **3106,** 10–13 (2016).
28. Czornomaz, L. *et al.* Confined Epitaxial Lateral Overgrowth (CELO): A novel concept for scalable integration of CMOS-compatible InGaAs-on-insulator MOSFETs on large-area Si substrates. *Dig. Tech. Pap. - Symp. VLSI Technol.* **2015–Augus,** T172–T173 (2015).
29. Deshpande, V. *et al.* Demonstration of 3-D SRAM Cell by 3-D Monolithic Integration of InGaAs n-FinFETs on FDSOI CMOS with Interlayer Contacts. *IEEE Trans. Electron Devices* **64,** 4503–4509 (2017).
30. Pearsall, T. P. & Hirtz, J. P. The carrier mobilities in Ga0.47In0.53As grown by organo-mettalic CVD and liquid-phase epitaxy. *J. Cryst. Growth* **54,** 127–131 (1981).
31. Zota, C. B., Wernersson, L. E. & Lind, E. High-Performance Lateral Nanowire InGaAs MOSFETs with Improved On-Current. *IEEE Electron Device Lett.* **37,** 1264–1267 (2016).
32. Synopsys Reg. *Sentaurus Device User Guide (Version N-2017.09)*. (2017).
33. Schwarzenbach, W., Malaquin, C., Allibert, F., Besnard, G. & Nguyen, B.-Y. Systematic evaluation of SOI Buried Oxide reliability for partially depleted and fully depleted applications. *2015 IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. S3S 2015* 6–8 (2015). doi:10.1109/S3S.2015.7333496
34. Navarro, C. *et al.* InGaAs Capacitor-Less DRAM Cells TCAD Demonstration. *IEEE J. Electron Devices Soc.* **6,** 884–892 (2018).
35. Levinshtein, M., Rumyantsev, S. & Shur, M. Gallium Indium Arsenide (AlxIn1-xAs). in *Handbook Series on Semiconductor Parameters Volume 2: Ternary And Quaternary III-V Compounds* (1996).
36. Lind, A. G., Aldridge, H. L., Hatem, C., Law, M. E. & Jones, K. S. Review—Dopant Selection Considerations and Equilibrium Thermal Processing Limits for n + - In0.53Ga0.47As. *ECS J. Solid State Sci. Technol.* **5,** Q125–Q131 (2016).
37. Czornomaz, L. *et al.* Scalability of ultra-thin-body and BOX InGaAs MOSFETs on silicon. *Eur. Solid-State Device Res. Conf.* 143–146 (2013). doi:10.1109/ESSDERC.2013.6818839

Acknowledgements

H2020 REMINDER European (grant agreement No 687931) and TEC2014-59730 and P12-TIC-1996 National projects are thanked for financial support.

Author contributions

C.N. carried out the experiments, wrote the initial manuscript seed and performed the TCAD simulations. C.C., C.Z. and L.C. fabricated the MSDRAM samples, S.K. provided fabrication details and actively participated in the experimental characterization. C.M. helped with the experimental setup and later data analysis. S.N. took care of the graphics design and processed the experimental and simulation data. F.G. coordinated and supervised the whole work. All authors finally discussed the results and revised and commented on the submitted manuscript.

Competing interests

The authors declare no competing interests.