Confinement Orientation Effects in S/D Tunneling

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Abstract

The most extensive research of scaled electronic devices involves the inclusion of quantum effects in the transport direction as transistor dimensions approach nanometer scales. Moreover, it is necessary to study how these mechanisms affect different transistor architectures to determine which one can be the best candidate to implement future nodes. This work implements Source-to-Drain Tunneling mechanism (S/D tunneling) in a Multi-Subband Ensemble Monte Carlo (MS-EMC) simulator showing the modification in the distribution of the electrons in the subbands, and, consequently, in the potential profile due to different confinement direction between DGSOIs and FinFETs.

I. INTRODUCTION

The study of alternative technical approaches for electronic devices is necessary to fulfill the requirements of power consumption, delay time and scalability demanded by ITRS [1]. Currently, there are two main work trends on the simulation of semiconductor processes and devices. The first one is the study of quantum effects in the nanometric dimensions of the conventional devices. The second one is mainly focused on novel engineering solutions to create improved device architectures.

The inclusion of quantum effects in the transport direction is mandatory when the dimensions of the electronic devices are reduced. In particular, Source-to-Drain tunneling (S/D tunneling) allows electrons to go through the potential barrier instead of rebound from it. When this quantum effect is taken into account, the height of the potential barrier is modified increasing the subthreshold current. Moreover, this phenomenon introduces noise because the number of affected electrons has a random nature. A ballistic non-equilibrium Green's Function (NEGF) approach has demonstrated that S/D tunneling is a scaling limit due to the reasons mentioned above [2]. In addition, it will distort the MOSFET operation at transistor channel lengths around 3nm [3]. This phenomenon is of special interest when the operation regime is near-threshold because the leakage current increases and V_{th} decreases [4].

At the same time, different technological architectures are proposed to overcome the limitations of conventional planar devices [5, 6]. For this reason, new transistor architectures based on multiple gates [7] are replacing standard technology as a way to keep short channel effects (SCEs) under control. Furthermore, the increased electrostatic confinement provided by multiple gates relaxes the manufacturing constraints in comparison to conventional planar devices. For example, a channel thickness (T_{Si}) is required to be one fourth of the channel length to guarantee acceptable short-channel effects in SOI technology. However, extremely thinner T_{Si} can represent a critical parameter in the fabrication of electronic devices as they are scaling down. This critical T_{Si} of a double gate transistor is approximately twice as wide as T_{Si} of a single-gate device with the same short-channel properties. It therefore alleviates the fabrication problem. If we consider a double gate device, these gates can be oriented horizontally, Double-Gate Silicon-On-Insulator (DGSOIs), or vertically, FinFETs. Ideally,

both channels are activated simultaneously and feature identical characteristics. The gates are parallel to the standard wafer orientation for DGSOIs whereas they are perpendicular in FinFETs as depicted in Figure 1. It should be highlighted that the FinFET is a 3D structure whereas our MS-EMC simulator makes use of a 2D description. However, it was demonstrated that FinFETs with a big enough aspect ratio show similar behavior in all transport regimes when 2DMS-EMC, which consider infinite fin height, and other 3D codes are used [8].

This work presents a meticulous comparison between DGSOIs and FinFETs by means of a Multi-Subband Ensemble Monte Carlo (MS-EMC) simulator when S/D tunneling mechanism is taken into account. It will be shown the influence of the orientation on the S/D tunneling and, consequently, on the device characteristics.

The outline of this work is as follows. Section II gives an overview of the code developed to carry out our research, where the starting point simulation frame and the S/D tunneling algorithm are accurately described. Subsequently, the results and discussions are summarized in Section III. Finally, the conclusions of this paper are summed up in Section IV.

II. SIMULATION SET-UP

Our MS-EMC simulator is based on the mode-space approach of quantum transport [9]. The device structure is divided into slices along the confinement direction where the 1D Schrödinger equation is solved, whereas the 2D Bolzmann Transport Equation (BTE) is solved in the transport plane as showed in Figure 1. Both equations are coupled to the 2D Poisson equation to keep the self-consistency of the solution. This simulator has already demonstrated its capabilities studying different advanced nanodevices [10–13]. The main advantage of this tool against NEGF approach is the reasonable computational time when scattering mechanisms and quantum effects on the ultrascaled devices are taken into account.

In addition, the fundamentals of the free-flight technique of an electron used in Monte Carlo algorithms are based on the stochastic and ergodicity processes. It calculates the positions of each electron in the transport direction after a random flight time which finishes

because of the random choice of a scattering event. After each flight, the new position and transport properties of the electrons are calculated. Depending on the carrier location and energy, our algorithm estimates the probability of undergoing a tunnel process. For this reason, another advantage of the MS-EMC simulator is the ability to switch on and off the tunneling process as it is included in a separate routine after each iteration.

The model employed here to include the S/D tunneling is an extension of the non-local band-to-band tunneling (BTBT) algorithm [14]. In that work, the same classical path and tunneling probability were considered, whereas the starting and ending point in the tunneling path belong to Valence and Conduction Band, respectively. The main advantage of this method is that, once it has been implemented in the simulator, it is possible to extend it from the study of BTBT to that of S/D tunneling because the description of both mechanisms is based on the same assumptions.

In this work, the performance of DGSOI and FinFET devices is analyzed when S/D tunneling is included in order to determine its impact. The considered confinement direction of these devices on standard wafers changes between (100) for planar DGSOIs and $(0\bar{1}1)$ for vertical FinFETs, and <011> for the transport direction as depicted in Figure 1. The differences in the confinement direction modify the electron distribution in the subbands, and, consequently, the potential profile. The carrier transport effective mass is also modified [15]. Table I summarizes the masses of each device and Table II shows their numerical values. Where $m_l = 0.916m_0$ and $m_t = 0.198m_0$ are the longitudinal and transversal effective masses in silicon, respectively, m_0 is the electron free-mass, m_x is the transport mass, m_z is the confinement mass, and Δ_2 and Δ_4 represent the degeneration factors of each valley. Moreover, the lower energy subband changes from Δ_2 in DGSOI to Δ_4 in FinFET.

These devices have been parametrized for gate lengths ranging from 5 nm to 20 nm. The rest of the technological parameters remains constant, channel thickness T_{Si}= 3 nm, gate oxide with Equivalent Oxide Thickness EOT= 1 nm and metal gate work function of 4.385 eV.

The position and energy of each electron are calculated after each free-flight as described above. In a semiclassical approximation, if the total energy of this electron is lower than the potential barrier at this position, the electron must undergo a backscattering. When

S/D tunneling is taken into account, there is a probability for the electron to go through the barrier. There are two steps to determine that probability at a specific energy.

Firstly, the tunneling probability of the electron T_{dt} is calculated using the WKB approximation [16]:

$$T_{dt}(E) = \exp\left\{-\frac{2}{\hbar}\int_a^b \sqrt{2m^*_{tr}(E_i(x) - E)}\,\mathrm{d}x\right\} \tag{1}$$

where a and b are the starting and ending points, E and m^*_{tr} are the energy and transport effective masses of the electron, respectively, and $E_i(x)$ the energy of the *i-th* subband. This approximation has already been used to study this phenomenon in other electron devices [17]. Our MSB-EMC simulator offers a detailed description of the subband structure. Consequently, T_{dt} has been calculated for each electron keeping in mind the minimum energy of its subband instead of the Conduction Band [18].

In that point, several assumptions have been considered after each integration step to enhance the calculation of T_{dt} and to reduce the computational effort. The exact starting and ending points in the tunneling path are calculated to evaluate T_{dt}. In addition, a maximum tunneling rejection length is also introduced (L_{max}). If the tunneling length of an electron from the starting point to a specific integration step is higher than L_{max}, the calculation of T_{dt} stops. L_{max} has been chosen herein at L_{max}= 10 nm because T_{dt} decreases substantially for higher lengths. It remains constant regardless of the channel length.

Secondly, a rejection technique is used to determine whether the particle will tunnel or not. A uniform distributed random number r_{dt} is generated and compared to T_{dt}. On the one hand, if $r_{dt} > T_{dt}$, the electron will turn back with $v_x = -v_x$. On the other hand, if $r_{dt} \leq T_{dt}$, the electron will go through the barrier.

Subsequently, if the electron undergoes a tunnel process, it is required to find the most probable tunneling path to completely determine its new position. The motion inside the barrier obeys Newton mechanics considering an inverted potential profile and ballistic transport [19]. This classical trajectory could be found by the following steps [4] as shown in Figure 2. Firstly, a pseudo-particle is placed at the starting point a with zero kinetic energy (Figure 2(b)). It is assumed that this particle is going to exit the barrier with the same

transport properties. Consequently, its flight direction is maintained before starting its motion. It is also marked to force a ballistic transport inside the barrier. Then, it accelerates in this system according to Newton's second law of motion (Figure 2(c)):

$$\vec{a} = \frac{q\xi}{m^*_{tr}} \tag{2}$$

where ξ is the electric field. Lastly, it reaches the ending point b (Figure 2(d)). Thereafter, the particle recovers its transport properties.

III. RESULTS AND DISCUSSION

A set of simulations at low bias condition has been performed to determine the importance of S/D tunneling on each device. The modifications in the energy profile of the lower energy subbands and the carrier transport effective mass caused by the difference in the confinement directions are shown in Figure 3 and 4, respectively. Both devices present similar energy profiles but the lower energy subband changes from Δ_2 in DGSOIs to Δ_4 in FinFETs (Figure 3). This change modifies the distribution of the population and the effective transport mass in the subbands. Moreover, Figure 3 shows the increase of the potential barrier when S/D tunneling is considered because of the existence of electrons located inside the potential barrier.

The average effective transport mass of the electrons as a function of the total energy and the total population which undergoes this tunnel process is higher in the FinFET than in the DGSOI as depicted in Figure 4. These values correspond to m_x of the fundamental valleys in Table II. It is also represented in Figure 4 the lower energy profile of the less populated valleys: Δ_2 in FinFET, and Δ_4 in DGSOI. The average effective mass in these non-fundamental subbands decreases for the FinFET whereas it increases for the DGSOI. Despite this, the average effective mass continues being higher for the less populated valley in FinFET than in DGSOI.

As a result, assuming similar energy profile (Figure 3), which means similar tunneling length at a specific starting point a, the higher is the value of m^*_{tr} in the fundamental valley in Equation (1) for the FinFET orientation, the smaller is T_{dt}. Besides, the value of m^*_{tr} in

the non-fundamental valley is higher in the DGSOI than in the FinFET, whereas the energy profile remains constant between both valleys. However, the reduction of the population in this valley decreases the number of particles involved in S/D tunneling. For these reasons, the FinFET reduces its effectiveness of the tunnel phenomenon compared to the DGSOI one.

The higher T_{dt}, the higher the probability of an electron undergoing S/D tunneling for the same energy. It therefore increases the number of particles affected by S/D tunneling for the DGSOI than for the FinFET. This effect is shown in Figure 5 where the electron distribution in arbitrary units from the fundamental subband as a function of total energy is represented.

Electrons with reduced energy must go through longer tunneling paths. When its length is similar to 10nm, which corresponds to L_G in Figure 5, the population decreases substantially. That is the reason why the maximum tunneling rejection length has been chosen at 10nm.

The same effect is also shown in the percentage of electrons near the potential barrier affected by S/D tunneling respect to the total number of electron with lower energy than the top of the barrier in the same region, which is higher for DGSOI (Figure 6 top) than for FinFET (Figure 6 bottom). In addition, there is a maximum of this percentage for the FinFET due to a reduced height of the potential barrier. When V_{GS} increases, the height of the potential barrier decreases causing the enhancement of the thermionic current. It therefore induces the reduction of the number of electrons near the potential barrier with lower energy. It is necessary to highlight that the change in the channel length modifies the tunneling length and, consequently, T_{dt}. For this reason, the number of particles that suffer S/D tunneling increases when the devices are scaling down. By way of contrast, the maximum percentage appears in DGSOI devices but it is shifted to higher gate voltages (not shown).

This quantum effect produces a noticeable modification of the $I_D - V_{GS}$ characteristics (Figure 7). Despite the increase of the potential barrier when S/D tunneling is included (Figure 3), a higher current level is observed. The number of electrons that flows from source to drain is higher because of the possibility of tunneling through the barrier. This increase is also exacerbated when the devices are scaled down. As it is shown, the influence

of the S/D tunneling is lower in the FinFET (Figure 7 bottom) compared to DGSOI (Figure 7 top).

The inclusion of tunneling introduces an important reduction in the threshold voltage (V_{th}) as it is shown in Figure 8. Due to the reduced number of particles affected by this phenomenon in the FinFET compared to the DGSOI, the shift of the V_{th} is smaller in the vertical device than in the horizontal one. This effect is amplified in both devices as the channel length is reduced.

The impact of the S/D tunneling on the electrostatics can be observed in Figure 9 where the threshold voltage variation (ΔV_{th}) between a simulation with and without taking it into account is shown. This difference is also aggravated for reduced L_G because the influence of this quantum effect in the electrostatics is lower in the FinFET.

IV. CONCLUSIONS

This work presents the implementation of S/D tunneling in a MSB-EMC simulator for the study of its impact in DGSOIs and FinFETs. Our simulations show important differences fully caused by the change in the confinement directions in both DGSOIs and FinFETs when S/D tunneling is taken into account due to the electron distribution and the variation of transport effective mass. Nevertheless, FinFET devices show less degradation in their subthreshold characteristics, and therefore are better candidates to implement future nodes, especially for ultra-low power applications.

V. ACKNOWLEDGMENT

The authors are grateful for the support given by the Spanish Ministry of Science and Innovation (TEC2014-59730-R), H2020 - REMINDER (687931), and H2020 - WAYTOGO-FAST (662175).

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Figures

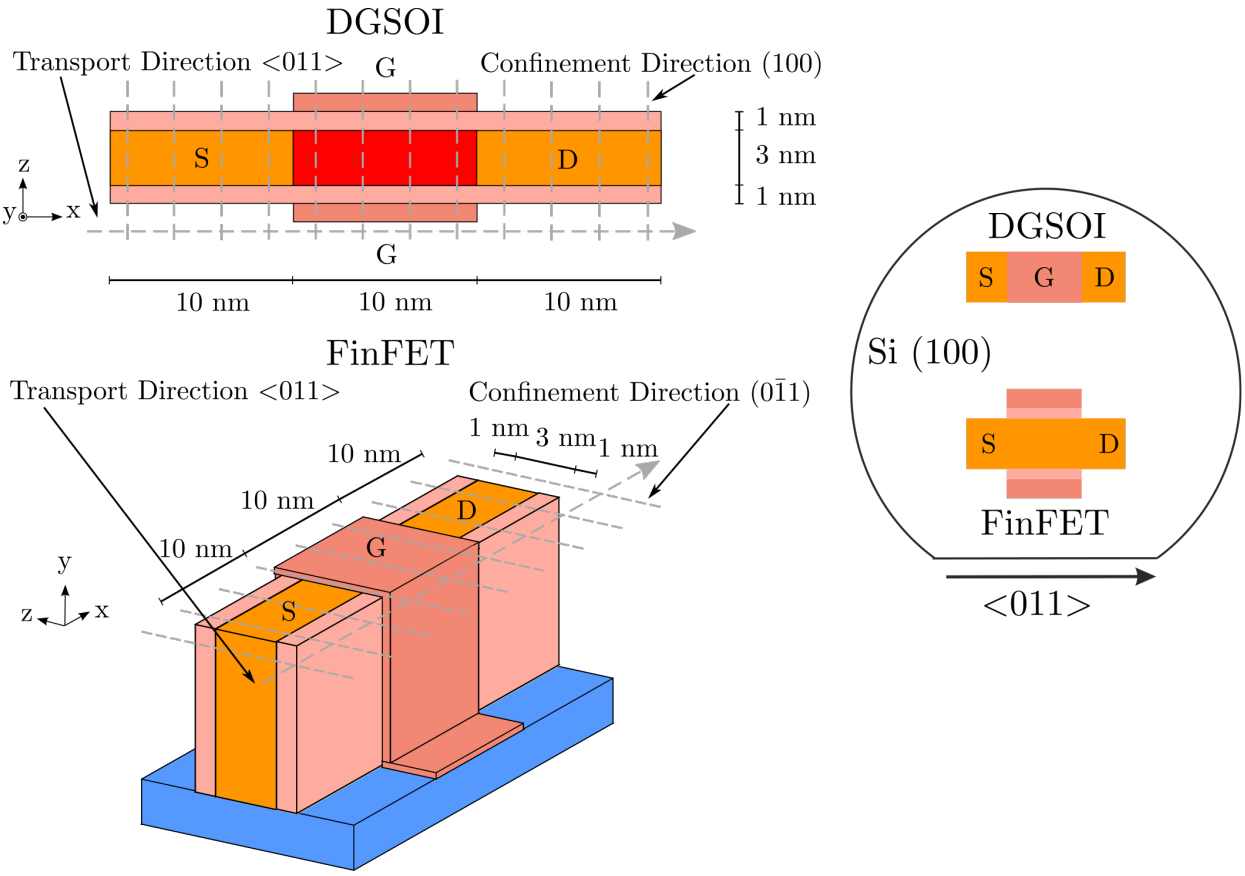


Figure 1: DGSOI and FinFET structures analyzed in this work. 1D Schrödinger equation is solved for each grid point in the transport direction and BTE is solved by the MC method in the transport plane.

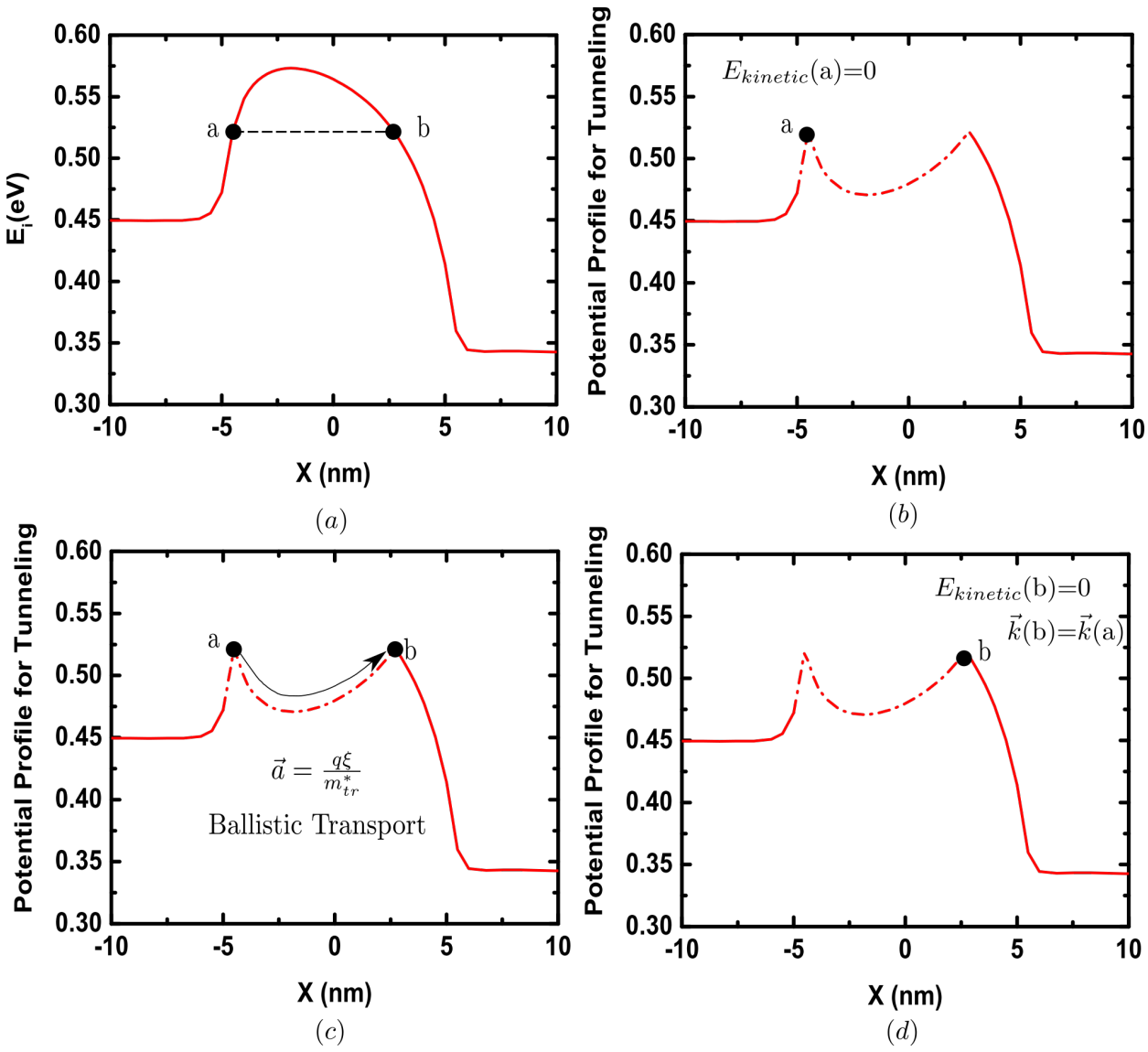


Figure 2: Representation of the tunneling model: The potential barrier (a) is inverted and the particle is placed at the starting point a (b), it follows a classical path obeying Newton's second law of motion (c) until it reaches the ending point b (d).

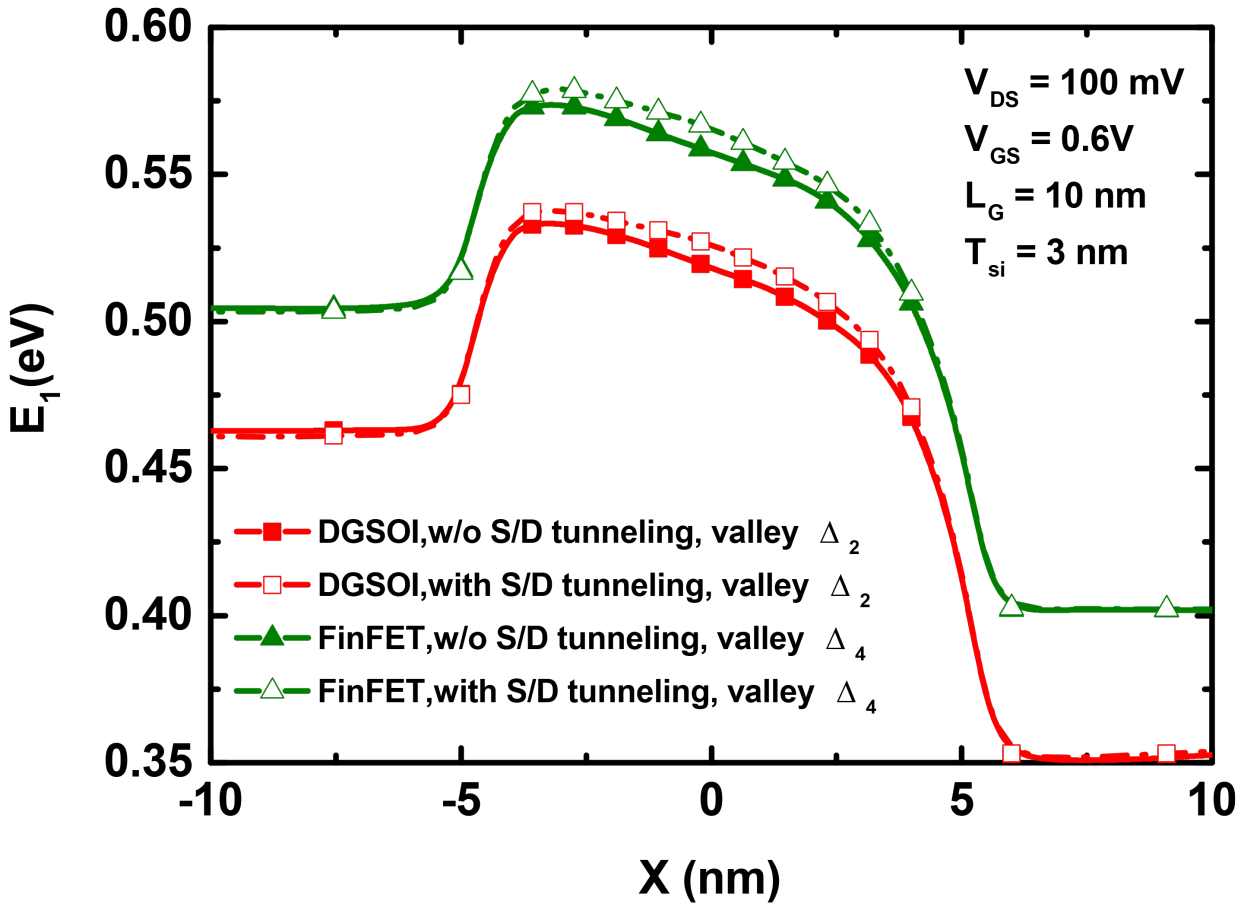
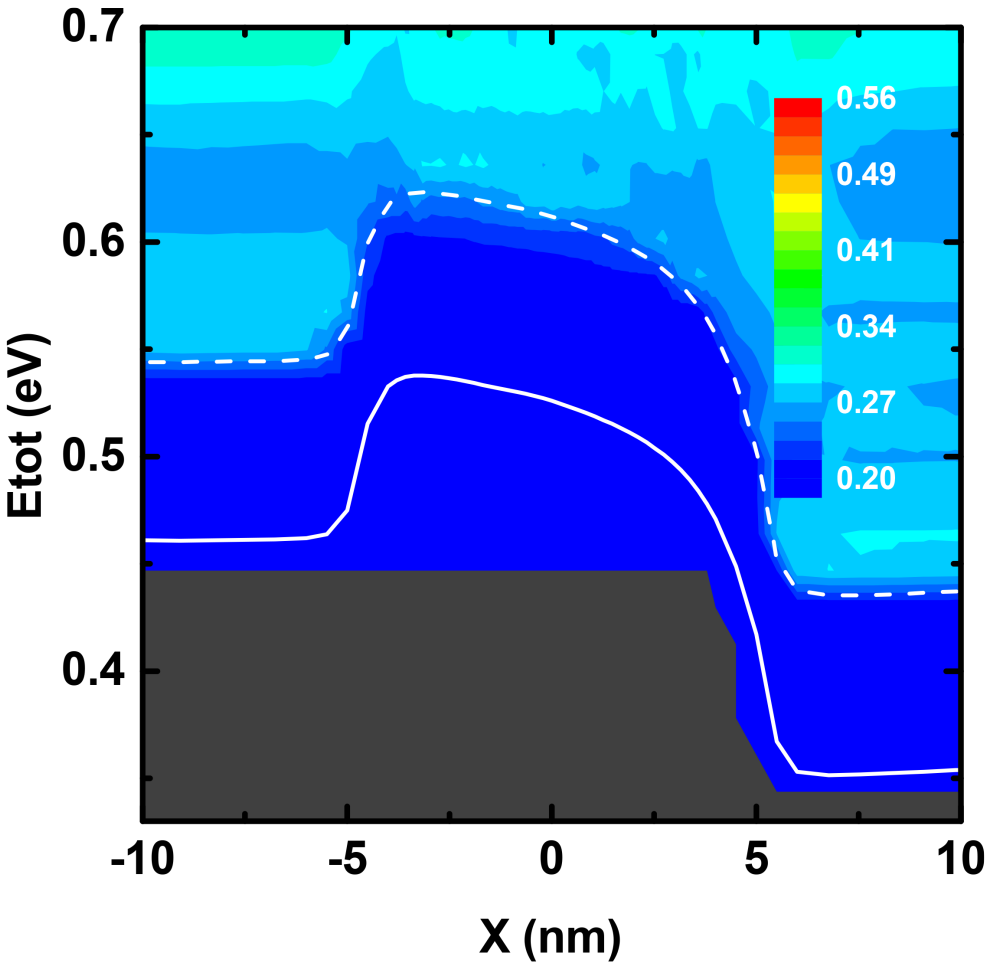
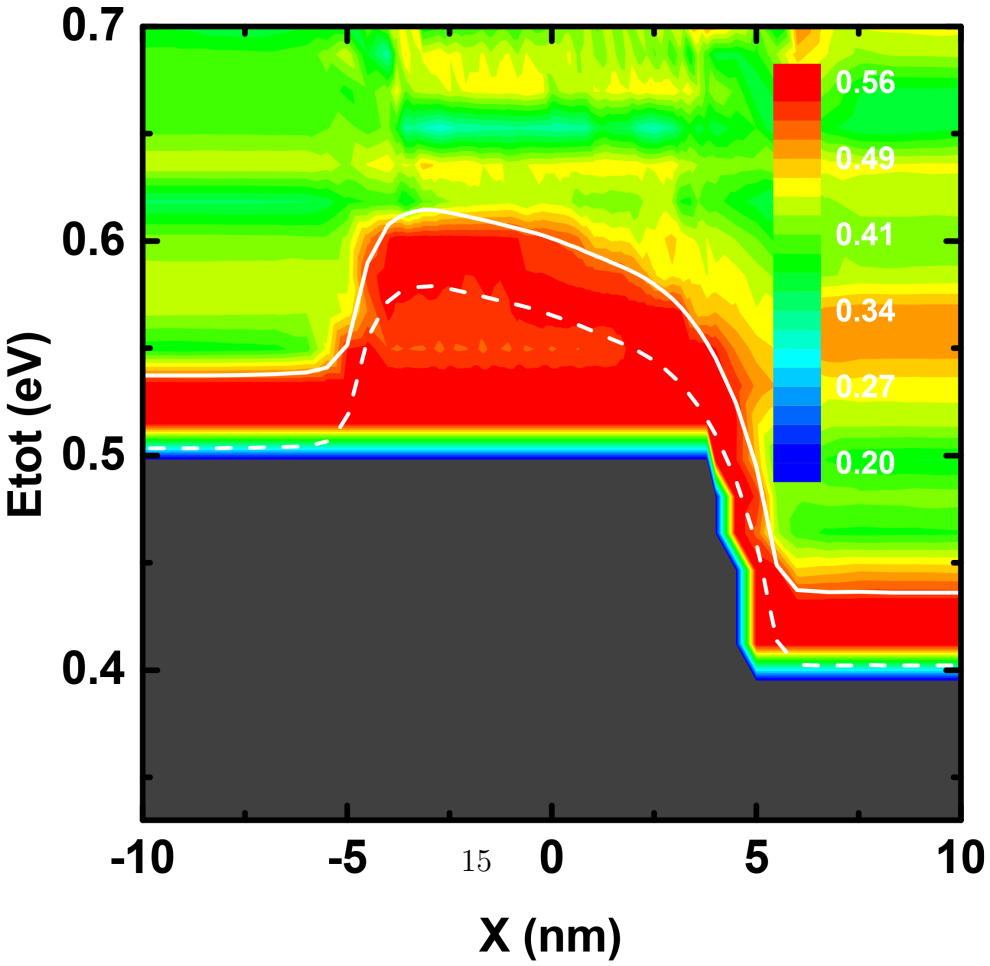


Figure 3: Energy profile of the lowest energy subband in the 10nm device for DGSOI (valley Δ_2) and FinFET (valley Δ_4) with and w/o S/D tunneling with $V_{GS} = 0.6V$ and $V_{DS} = 100mV$.


0.7
0.6
0.5
0.4
Etot (eV)
0.56
0.49
0.41
0.34
0.27
0.20
-10
-5
0
5
10
X (nm)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Etot (eV)
0.56
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-5
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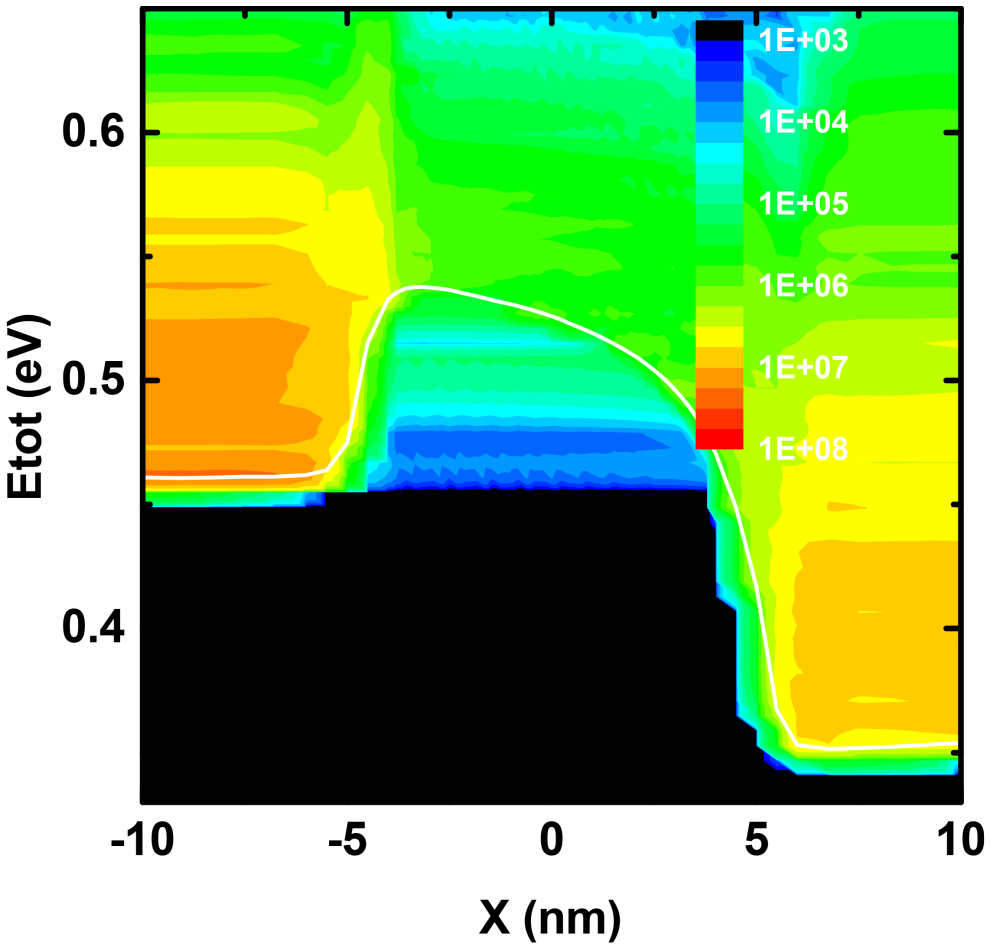
5
10
X (nm)

Figure 4: Average effective mass of the electron distribution with the lower energy subband of the valley Δ_2 (solid) and of the valley Δ_4 (dashed) as a function of the total energy and the total population in the 10nm device including S/D tunneling for DGSOI (top) and FinFET (bottom) with $V_{GS} = 0.6V$ and $V_{DS} = 100mV$.


1E+03
1E+04
1E+05
1E+06
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Etot (eV)
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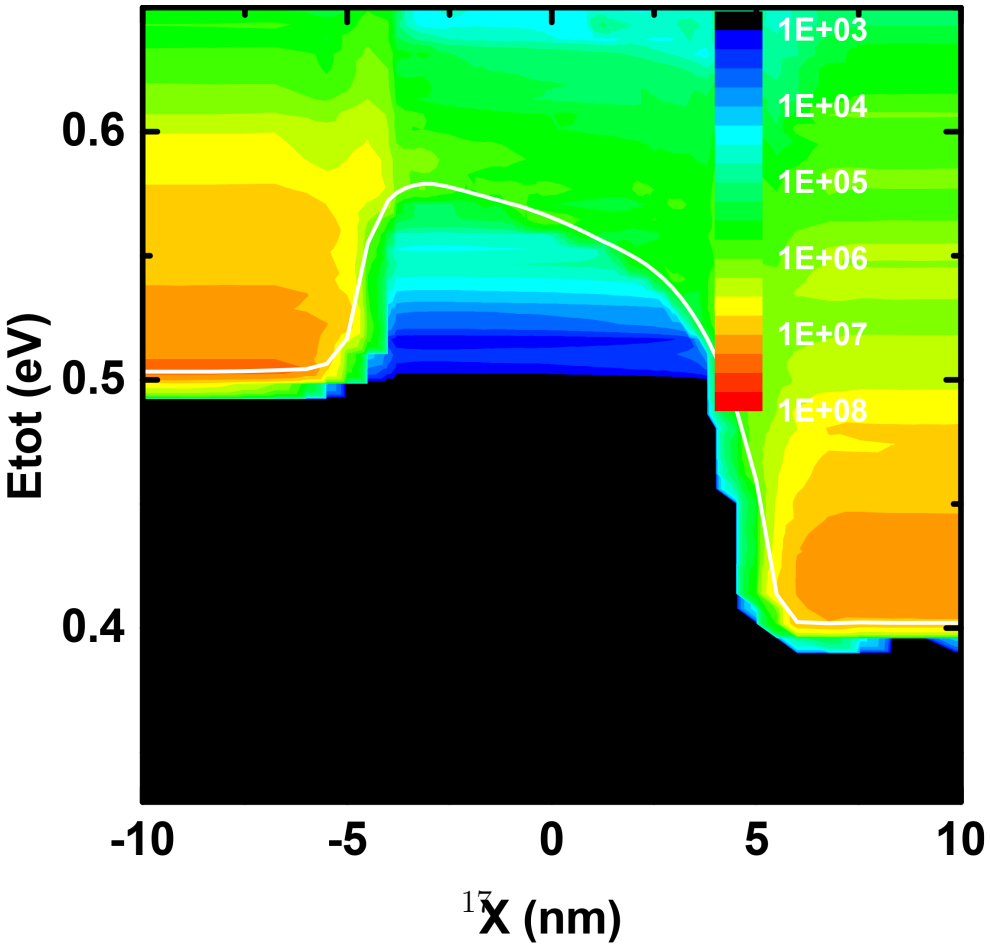
5
10
X (nm)


1E+03
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Etot (eV)
-10
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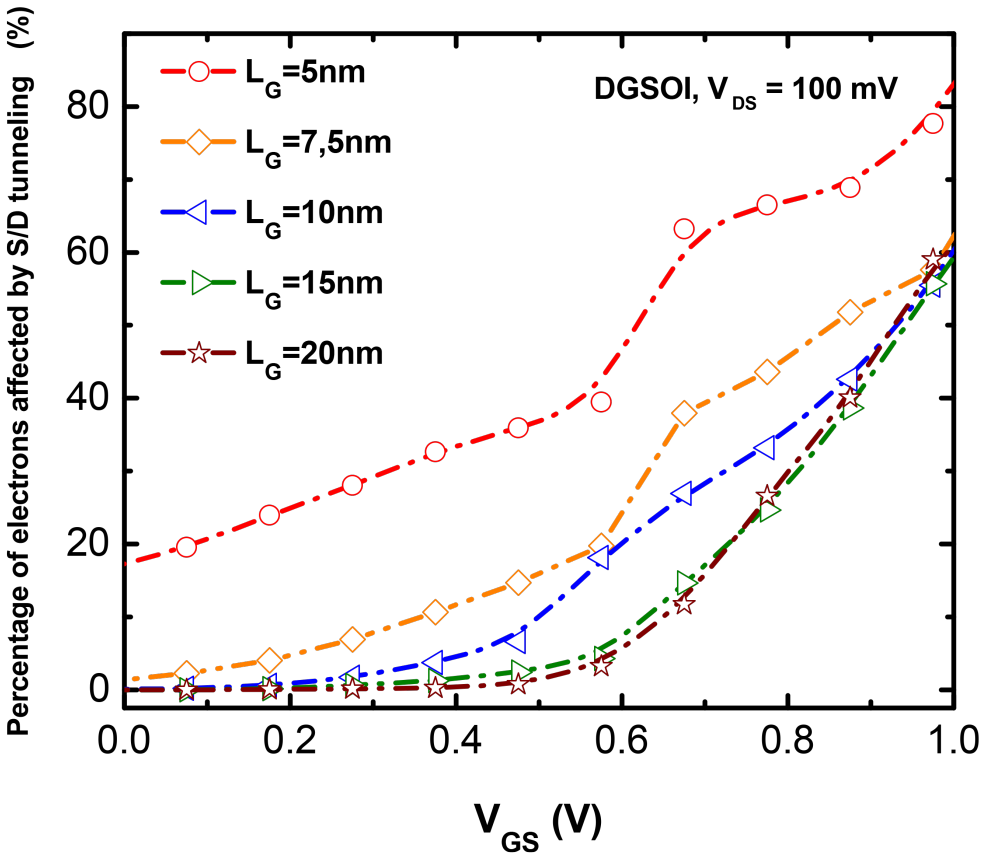
5
10
X (nm)

Figure 5: Electron distribution in arbitrary units in the lower energy subband as a function of total energy in the 10nm device including S/D tunneling for DGSOI (top) and FinFET (bottom) with $V_{GS} = 0.6V$ and $V_{DS} = 100mV$.


Percentage of electrons affected by S/D tunneling (%)
DGSOI, V_DS = 100 mV
L_G=5nm
L_G=7,5nm
L_G=10nm
L_G=15nm
L_G=20nm
0
20
40
60
80
0.0
0.2
0.4
0.6
0.8
1.0
V_GS (V)

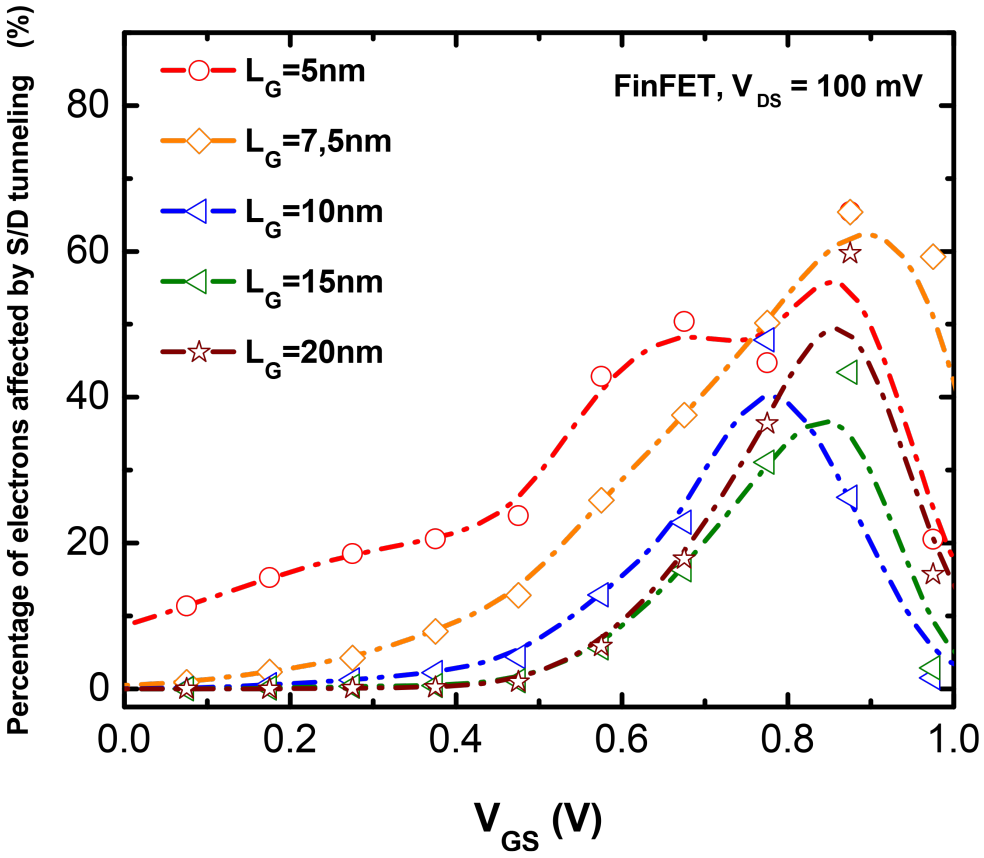

Percentage of electrons affected by S/D tunneling (%)
FinFET, V_DS = 100 mV
L_G=5nm
L_G=7,5nm
L_G=10nm
L_G=15nm
L_G=20nm
0
20
40
60
80
0.0
0.2
0.4
0.6
0.8
1.0
V_GS (V)

Figure 6: Percentage of electrons near the potential barrier affected by S/D tunneling respect to the total number of electron with lower energy than the top of the barrier in the same region as a function of L_G at low drain bias for DGSOI (top) and for FinFET (bottom).

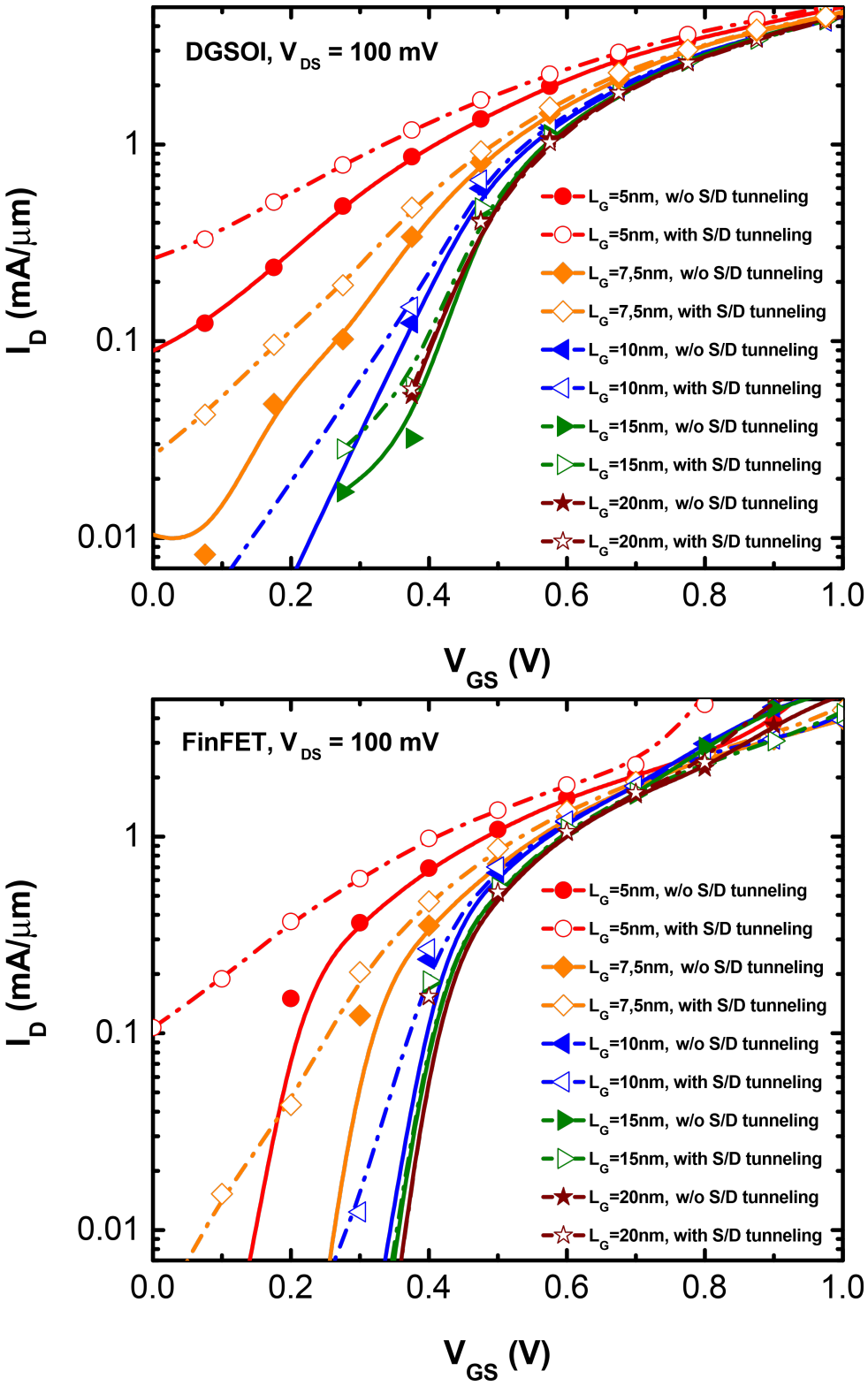


Figure 7: $I_D$vs.V_{GS} as a function of L_G at low drain bias with and w/o considering S/D tunneling for DGSOI (top) and FinFET (bottom).

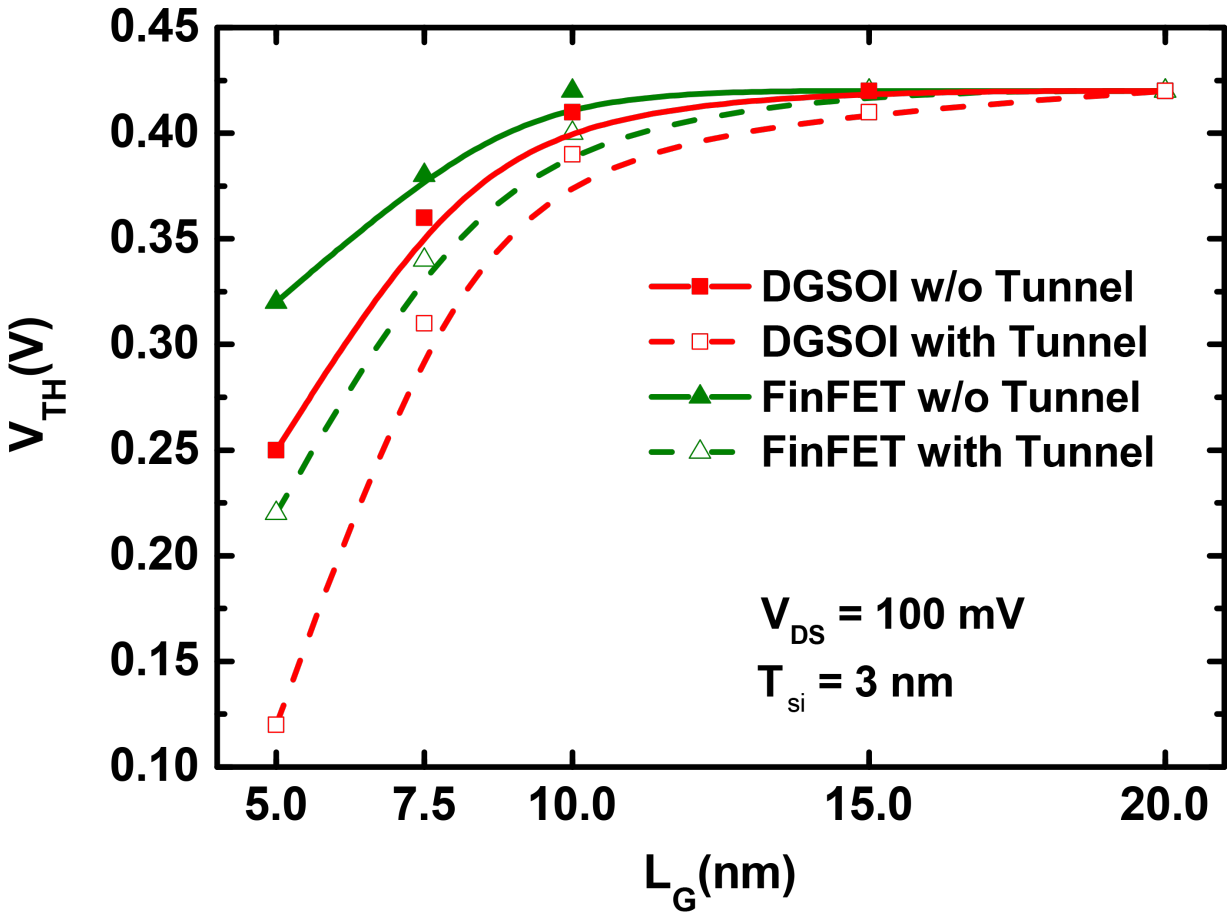


Figure 8: Threshold voltage (V_{th}) for FinFETs and DGSOIs as a function of L_G at low bias condition and $T_{si} = 3nm$ with and w/o considering S/D tunneling.

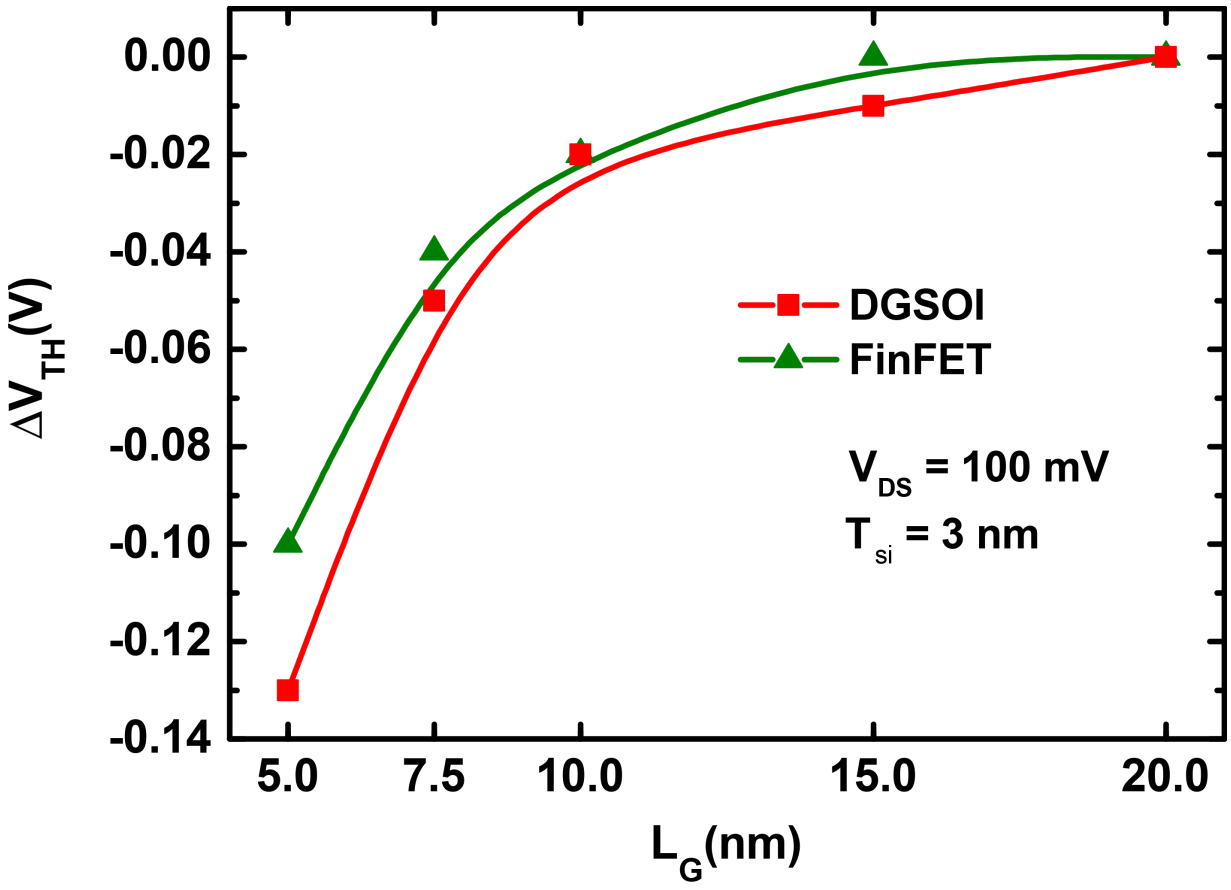


Figure 9: Difference between the threshold voltage (ΔV_{th}) of a simulation considering S/D tunneling and w/o taking it into account as a function of L_G for DGSOIs and FinFETs at low drain bias condition and $T_{si} = 3nm$.

Tables

Device	Valley	m_x	m_y	m_z
DGSOI	Δ_2	m_t	m_t	m_l
(100)<011>	Δ_4	$\frac{2m_l m_t}{m_l+m_t}$	$\frac{m_l+m_t}{2}$	m_t
FinFET	Δ_2	m_t	m_l	m_t
$(0\bar{1}1)$<011>	Δ_4	$\frac{m_l+m_t}{2}$	m_t	$\frac{2m_l m_t}{m_l+m_t}$

Table I: Effective mass in silicon for DGSOI and FinFET devices studied in this work where m_x is the transport mass and m_z is the confinement mass.

Device	Valley	m_x	m_y	m_z
DGSOI	Δ_2	0.198	0.198	0.916
(100)<011>	Δ_4	0.326	0.557	0.198
FinFET	Δ_2	0.198	0.916	0.198
$(0\bar{1}1)$<011>	Δ_4	0.557	0.198	0.326

Table II: Numerical values of effective mass in silicon for DGSOI and FinFET devices studied in this work where m_x is the transport mass and m_z is the confinement mass.