Universidad de Granada

Doctoral Thesis

Electrical Characterization of Reliability in Advanced Silicon-On-Insulator Structures for sub-22nm Technologies

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Guarantee by signing this thesis:

that the research work contained in the present report, entitled ***Electrical characterization of reliability in advanced Silicon-On-Insulator structures for sub-22nm technologies***, has been performed under the full guidance of the Ph.D Advisors and, as far as our knowledge reaches, during the work, it has been respected the right of others authors to be cited, when their publications or their results have been used.

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To my Parents, Brother and my Little

He who learns and learns and does not practice what he knows is similar to one who plows and plows, but does not sow.

Plato, Greek Philosopher

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List of Abbreviations and Symbols

Abbreviations

BESOI	Bond-and-Etch-back SOI
BI	Bias Instability
BJT	Bipolar Junction Transistor
BOX	Buried Oxide (buried isolation layer of a SOI structure)
BTBT	Band–to–band Tunneling
CMOS	Complementary MOS technology
CVD	Chemical Vapor Deposition
DIBL	Drain Induced Barrier Lowering
EOT	Equivalent Oxide Thickness
ETSOI	Extremely Thin SOI
FET	Field–Effect Transistor
FDSOI	Fully Depleted SOI
GAA	Gate-all-around
GLM	Gate Leakage Mechanism
GO	Graphene Oxide
HKMG	High-κ Metal Gate
IL	Interface Layer
ITRS	International Technology Roadmap for Semiconductors
JFET	Junction Field-Effect Transistor
MEMS	Micro–Electro–Mechanical Systems
MIS	Metal–Insulator–Semiconductor
MOSFET	Metal–Oxide–Semiconductor Field–Effect Transistor
MuGFET	Multiple Gate Field-Effect Transistor

MSM	Measure-Stress-Measure method
NMOS	N-channel MOSFET
NBTI	Negative Bias Temperature Instability
OTF	On-The-Fly method
PBTI	Positive Bias Temperature Instability
PDSOI	Partially depleted SOI
PMOS	P–channel MOSFET
RTN	Random Telegraph Noise
SCE	Short Channel Effects
SGSOI	Single Gate SOI
S/D tunneling	Direct Source to Drain tunneling
SOC	System-on-Chip
SOI	Silicon On Insulator
SS	Subthreshold Swing
TCAD	Technology Computer Aided Design
TEM	Transmission Electron Microscopy
TFET	Tunneling Field-Effect transistor
TLM	Transmission Line Method
TMD	Transition Metal Dichalcogenide
UTB	Ultrathin-Body
UTBB-FDSOI	Ultra-Thin Body and Buried oxide Fully Depleted SOI

Symbols

Symbol	Description
C_D	Depletion capacitance
C_f	Fixed oxide capacitance
C_{it}	Interface trapped capacitance
C_{ot}	Oxide trapped capacitance
C_{ox}	Oxide capacitance
C_{Si}	Silicon capacitance
D_{it}	Interface trapped density
E_g	Bandgap energy
J_n	Electron current density
J_p	Holes current density
κ	Dielectric constant
L	Gate length
L_T	Transfer length
μ_n	Electron mobility
n	Electron concentration
p	Hole concentration
ϕ_m	Metal workfunction
ϕ_n	Potential difference between E_C and E_F
ϕ_p	Potential difference between E_V and E_F
Φ_{fb}	Flatband potential
Φ_s	Surface potential
Q_f	Fixed oxide charge
Q_{it}	Interface trapped charge
Q_m	Mobile oxide charge
Q_{ot}	Oxide trapped charge
ρ_c	Contact resistivity
R_C	Contact resistance
R_m	Metal resistance
R_{sh}	Sheet resistance
R_T	Total resistance
SiO_2	Silicon dioxide
T	Temperature (Absolute)
T_{OX}	Gate dielectric thickness
T_{Si}	Silicon Thickness

u	Sound velocity in the material
V_{DD}	Supply voltage
V_{DS}	Drain–to–source voltage
V_{GS}	Gate–to–source voltage
V_{TH}	Threshold voltage

Physical constants

ϵ_0	vacuum permittivity	$8.85418782 \cdot 10^{-12}$ F/m
m_0	electron rest mass	$9.10938291 \cdot 10^{-31}$ Kg
h	Planck's constant	$6.62606957 \cdot 10^{-34}$ J·s
$\hbar$	reduced Planck's constant	$1.05457172 \cdot 10^{-34}$ J·s
k_{B}	Boltzmann's constant	$1.38064881 \cdot 10^{-23}$ J/K
q	elementary charge	$1.60217656 \cdot 10^{-19}$ C

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Prologue

Context

Since the MOSFET transistor was demonstrated in 1959 [1] and after Gordon Moore well determined in the 1960's with his 'Moore's law' [2], the semiconductor industry trend has been the miniaturization (reduction the device size) with the goal of increasing the number of devices per chip and improving the switching frequency. Consequently, the voltages are reduced in proportion to the dimension in order to keep the electric fields constant. Regrettably, huge technology difficulties have been found to follow some of the 'scaling rules' needed in the transistor miniaturization, however, the way to solve the majority of them has also been found.

One of the ways to increase the device performance is reducing the thickness of the silicon oxide insulator. Silicon dioxide (SiO_2) has been the preferred gate insulator for silicon MOSFET since its very beginning in the 1960's due to the easiness to grow controlled SiO_2 thin layers on Si films. The oxide thickness has been reduced over the years from 300nm, for 10μm technology, to 1.2nm, for 65nm technology [3]. In these latter thicknesses, the electric filed in the oxide becomes very high causing current leakage through the insulator and even destructive breakdown of the oxide [4]. Moreover, tunneling leakage current appears in SiO_2 films thinner than 1.5nm, doing the device inoperative [5]. To solve this issue while following the scale trend, materials having larger dielectric constants (high-k dielectrics) have been proposed to replace the SiO_2 [6]. These high-κ dielectric insulators allow thicker films while keeping the same gate capacitance according to Equation 1:

$$C = \frac{\kappa \epsilon_0 A}{t_{ox}} \tag{1}$$

where κ is the relative dielectric constant of the material, ϵ_0 is the permittivity of free space, A the capacitor area and t_{ox} the thickness of the insulator. However, adopting high-κ dielectrics in integrated circuits (ICs) introduces chemical reactions between them and the silicon substrate, as well as lower surface mobility than the in Si/SiO_2 structure [7]. These issues can be minimized by inserting a thin SiO_2 interfacial layer between the silicon substrate and the high-κ dielectric and using a metal gate instead of a poly-Si gate [7]. Despite the improvements introduced, new effects and instabilities such as interface trapping, oxide mobile charges or random telegraph noise (RTN), come into action due to the increase in the number of interfaces,the quality of them, and the properties of the new material introduced. These reliability issues make necessary an extensive characterization of the transistor behavior under different bias conditions.

On the other hand, the randomness in the position of dopant atoms in the device is an inherent source of fluctuations as the dimensions shrink. This effect in the depleted layer under the channel causes fluctuations (variability) in the threshold voltage of the transistors from device to device [8]. Voltages must overcome these fluctuations intrinsic to fabrication process and cannot be reduced as desired. These voltage limitations imply high electric fields in the transistor which triggers new instability effects such as hot carrier degradation, negative bias instability (NBTI) or impact ionization, among others.

The extreme scaling down in the length of transistors to nanometer ranges and the difficulties involved in the manufacturing process, have originated the arising of new structures and materials to fabricate the transistors. The increase of extrinsic parasitic resistances and capacitances caused by the scaling of the transistor is relieved by reducing the parasitic junction capacitance [9]. The Silicon-on-Insulator (SOI) technology, with the integration of an ultra-thin buried oxide (BOX), improves the threshold voltage variability [10]. Besides, this buried oxide layer eliminates the need to add dopants to the channel, thus making it fully depleted, (FDSOI). Other technologies adopted are the ultra-thin body FETs and vertical transistor structures which use a double gate structure such as the FinFET [11].

Finally, there has been a recent trend to investigate the role of new materials in electronics applications in general, leaded by two dimensional (2D) semiconductors such as graphene [12] or transition metal dichalcogenides (TMDs) [13].

These materials hold stunning electrical properties in very thin scales and are being investigated to be incorporated in future technology nodes.

To sum up, this work studies the impact of the miniaturization on the transistor through the characterization of reliability effects. The instability effect involved in new process schemes and materials associated to gate (NBTI, RTN, impact ionization, etc.) will be the main focus of this thesis. Moreover, electrical characterization and synthesis of new electronic 2D materials have been carried out.

Outline

The structure of the work is described as follows:

Chapter 1. MOSFET Scaling. This chapter focuses on the study of the transistor structures and technologies proposed to achieve the goals imposed by technology miniaturization. These technologies are the Silicon-on-Insulator, the use of high-κ insulator as gate oxide and the gate stack structure. The two dimensional (2D) materials proposed in the next technologies nodes are analyzed and the reliability effects concerning all these technology improvements are summarized.

Chapter 2. Experimental Characterization. This chapter introduces the experimental techniques and the theoretical framework which allow to carry out the electrical characterization of reliability issues in semiconductor devices. The techniques used for electrical characterization of bare SOI wafers, and the defects located in the oxide-Si interfaces of these devices are described. The substrate bias dependence of the threshold voltage, the sources of instability and the noise characterization of SOI transistors are detailed. Additionally, the characterization of wafer variability through automatic measurement setups is explained in this chapter. Finally, The characterization techniques to extract the sheet resistance and contact resistivity of 2D materials (both bare substrates and metallized substrates) are detailed.

Chapter 3. Bias Instability. This chapter is focused on the reliability issues affecting the electrical characteristics of a MOS transistor when the gate is stressed with relatively high voltage (Bias Instability). In this chapter, the instability of bare SOI wafers is characterized by using the Pseudo-MOSFET

technique. The effect of positive and negative stress pulses on the properties of both hole and electron channels is systematically investigated using several characterization methods. The origin of the instability, the dependence of the degradation with time, and the recovery after the stress are discussed.

Chapter 4. Random Telegraph Noise. In this chapter Random Telegraph Noise (RTN) has been studied in ultra-thin SOI MOSFETs. A new experimental characterization protocol which aims to identify unequivocally the single-trap RTN signals in optimum bias conditions is introduced. The methodology combines a modified Weighted Time Lag Plot algorithm assisted with $1/f$ spectral scanning by gate bias. The procedure has been applied to study the influence of the back-gate bias on the RTN characteristics of the SOI devices with coupled front and back interfaces. The effect of the temperature on the characteristic times has been studied in the range from 248 to 323 K validating the results obtained at room temperature.

Chapter 5. Impact Ionization. This chapter faces the study of impact ionization in Silicon-On-Insulator transistors from the direct characterization of the body current and electrostatic potential. Thin and ultra-thin body-contacted silicon-on-insulator transistors have been fabricated for that purpose, and biased at zero-body potential and zero-body current conditions. The influence of the channel length on the evolution of the body potential as well as the substrate bias dependence are analyzed.

Chapter 6. Conclusions. This chapter faces the main ideas extracted from the thesis, from the theoretical to the experimental achievements. The future steps are also shown in this chapter.

Appendix A. Electrical characterization of laser rGO This appendix is focused on the electrical characterization of laser-assisted reduced graphene oxide by point contact techniques. The careful investigation of in-line two and four point-contact techniques applied to macroscopic samples of reduced graphene oxide is carried out. Then, the application of the characterization technique to improve the conductivity of the samples is shown.

Chapter 1

MOSFET Scaling

The scaling of the dimensions of a MOSFET and the consequent performance improvement of the transistors have been shocking during the last four decades, since Dennar et al. described the MOSFET scaling rules in 1974 [14]. Starting at a minimum feature length of 10 mm in 1970, the gate length was gradually reduced to a feature size of decades of nanometers in the last years. Proper scaling of MOSFET, however, requires not only a size reduction of the gate length and width but also a reduction of all other dimensions including the gate/source and gate/drain alignment, the oxide thickness and the depletion layer widths. The 'scaling rules' of MOSFET device parameters are illustrated in the Table 1.1.

In 1965, Gordon Moore predicted that the trend in the semiconductor industry miniaturization following the previous cited scaling rules. In first instance, he predicted the number of transistors in an integrated circuit (IC), doubles approximately every year [2]. This prediction turned out to be exaggerated and ten years after, Gordon Moore revised his calculations, affirming that it would double every two years, as shown in Figure 1.1. Although the miniaturization limit is not yet in sight, the industry has had to overcome some challenges in its continuation [15]. Some of these challenges and the corresponding solution will be detailed in this chapter.

Two types of scaling are shown in Table 1.1: constant field scaling and constant voltage scaling. Constant field scaling yields the largest reduction in the power consumption of the transistor. However, it requires a reduction in the power supply voltage as well as a decrease in the minimum feature size. Constant

Table 1.1: Comparison of the effect of scaling on MOSFET device parameters. α is the scaling factor.

Parameter	Symbol	Constant field scaling	Constant voltage scaling
Gate length	L	$1/\alpha$	$1/\alpha$
Gate width	W	$1/\alpha$	$1/\alpha$
Electric Field	ϵ	1	α
Oxide thickness	t_{ox}	$1/\alpha$	$1/\alpha$
Concentration	N_a	α^2	α^2
Oxide capacitance	C_{ox}	α	α
Voltage	V	$1/\alpha$	1
Current	I	$1/\alpha$	α
Power	P	$1/\alpha^2$	α

voltage scaling does not have to reduce the voltage, being the preferred scaling method since it provides voltage compatibility with older circuit technologies. The disadvantage of constant voltage scaling is that the electric field increases as the minimum feature length is reduced. This leads to velocity saturation, mobility degradation, increased leakage currents, lower breakdown voltages and other reliability problems. To solve these and other reliability issues, new structures and materials have been proposed to improve the transistor behavior as it will be shown in the following sections.

Another key assumption in scaling law was the ability to scale down the gate oxide thickness. SiO_2 has been the preferred gate insulator for silicon MOSFET since its very beginning in the 1960's (easiness to grow controlled thin SiO_2 layers on Si films). The oxide thickness has been reduced, over the years from 300nm for 10μm technology to 1.2nm for 65nm technology [3,16], as is shown in Figure 1.2. This 1.2nm-thick dielectric is only a few atomic layers thick and represents the limit to which SiO_2 can be scaled because, below this thickness, tunneling leakage current makes the device inoperative [5]. The solution adopted in this context was the introduction of high-κ dielectric insulators which permit thicker films while keeping the same gate capacitance.

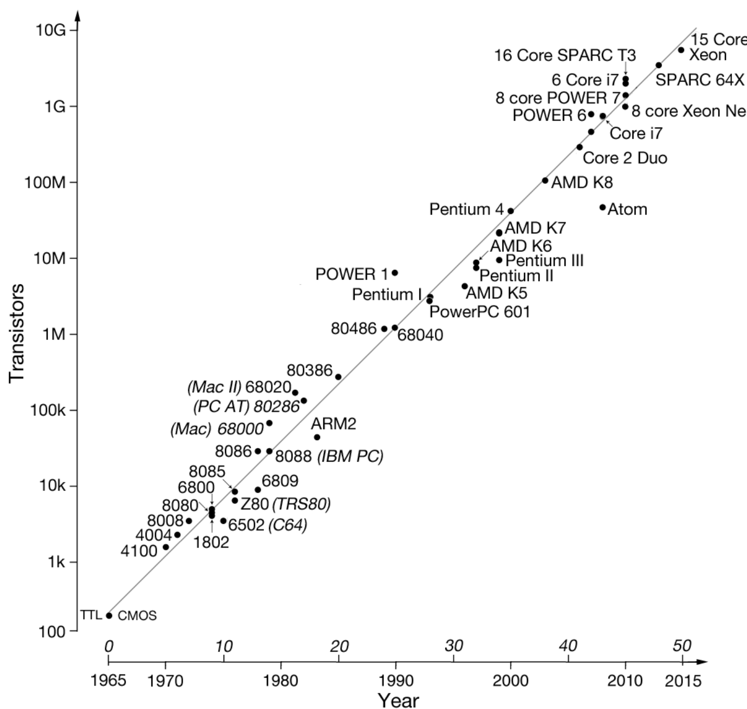

Figure 1.1: Moore's law over time (line). Correspondence with some commercial processors is shown.

1.1 Gate scaling: high-κ dielectrics

The introduction of high-κ materials as gate insulator has been a successful advance to bypass the limitation in the minimum oxide thickness imposed by leakage and tunneling current when SiO_2 is employed. Following Equation 1.1, high-κ dielectric insulators allow thicker films while keeping the same gate capacitance.

$$C = \frac{\kappa \epsilon_0 A}{t_{ox}} \tag{1.1}$$

where κ is the relative dielectric constant of the material, ϵ_0 is the permittivity of free space, A the capacitor area and t_{ox} the thickness of the insulator. In Figure 1.3, a transmission electron microscopy (TEM) image is shown for two alternative structures to obtain an equivalent gate oxide capacitance using SiO_2 and high-κ layers. Equivalent oxide thickness (EOT) determines how thick (nanometer) the

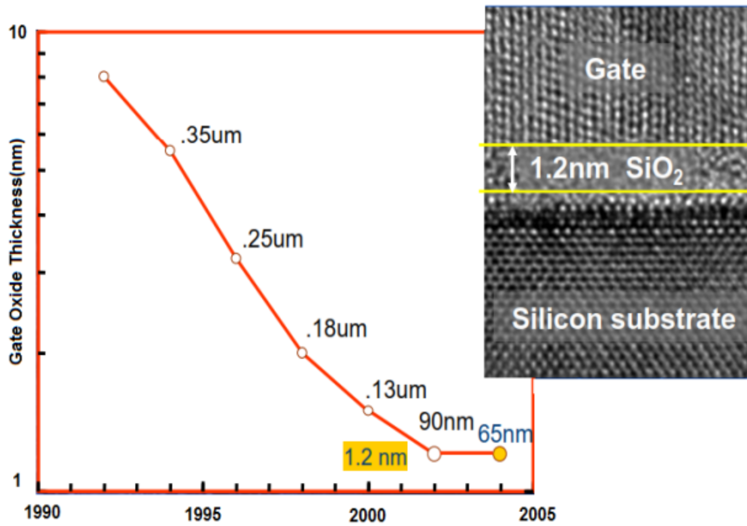

Figure 1.2: Gate oxide thickness scaling according to the node technology. Inset: TEM image of a 90nm node with a dielectric thickness of 1.2nm [17].

SiO_2 is required to induce the same effect as the high-κ material being used.

Being a good advance, the implementation of high-κ oxides entails some issues when the material is selected. Some of the requirements the high-κ insulator must satisfy are:

- The material must be compatible with Silicon and the fabrication process followed in the transistor manufacturing (also economically speaking).
- It must be able to continue scaling to lower EOTs.
- The number of defects in the interfaces surrounding the high-κ insulator must be minimized.
- Mobility decrease and reliability issues must be minimized.

According to the previous criteria, the immediate conclusion could be to increase the factor κ as much as possible to continue EOT scaling. However, very large κ values will produce unwanted strong fringing fields from the gate to the source/drain regions. These fringing fields reduce the gate control and introduce short-channel effects [19]. On the other hand, it is also necessary that the high-κ

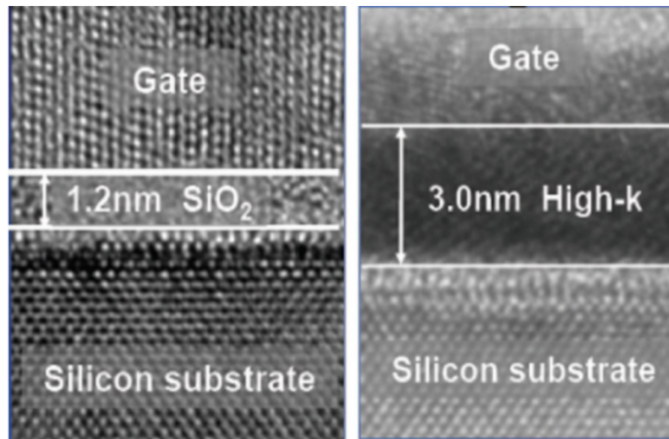

Figure 1.3: TEM image of a 1.2nm EOT transistor (left) using 1.2nm of SiO_2 layer in the gate oxide, (right) using 3nm of high-κ material as gate oxide [18].

oxide has a band gap larger than 5 eV in order to minimize the injection by the Schottky emission of carriers into the oxide bands that causes unacceptable high leakage currents. Nevertheless, the larger κ factor, the lower band-gap, i.e., a trade-off between dielectric constant and band-gap is necessary to achieve good reliability, low current leakages and device miniaturization. Some of the most common high-κ materials are summarized in Figure 1.4, where the band gap is plotted as a function of the the dielectric constant.

One of the most well positioned candidates to continue EOT scaling below $1.0nm$ is the hafnium dioxide, HfO_2. It is an oxide with lower oxygen diffusion coefficients than the SiO_2 thus overcoming the problem of the unstable interface formed with Si.

The integration of high-κ dielectrics in the fabrication process introduces chemical reactions with the Silicon substrate. In this context, to improve the stability reducing the interface reactivity, an interlayer of SiO_2 is added between the Silicon substrate and the high-κ insulator. Despite this layer degrades the properties of both the dielectric and the underneath Silicon resulting in a total gate oxide capacitance as shown the Equation 1.2 [20], this interlayer is required in order to maintain the quality and reliability of the transistor and the carrier mobility in the channel [7, 21].

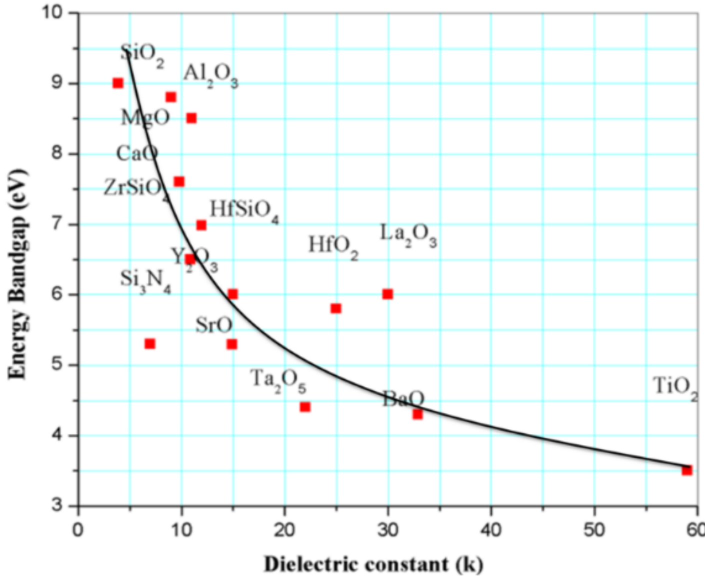

Figure 1.4: Band gap as a function of the dielectric constant (κ) for different high-κ insulator materials [18].

$$\frac{1}{C_{ox}} = \frac{1}{C_{IL}} + \frac{1}{C_{H-\kappa}} \tag{1.2}$$

1.2 Gate scaling: metal stack

The gate capacitance of a transistor is defined as the series combination of the oxide capacitance, the depletion capacitance of the gate electrode and the capacitance of the Si channel. These three capacitances add as shown in Equation 1.3:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_D} + \frac{1}{C_{Si}} \tag{1.3}$$

The channel capacitance (C_{Si}) contribution is intrinsic and cannot be easily changed once the channel is inverted. However, the depletion capacitance of the gate electrode depends on the used metal gate. Poly-Si (degenerately doped polycrystalline Silicon) has been the most used material as metal gate due to its

stability at high temperatures and the good compatibility with the SiO_2. The carrier density in Poly-Si is relatively low, which means a substantial depletion depth. However, a metal with a higher carrier density could reduce the depletion depth increasing the correspondent capacitance and making this contribution negligible [7, 22]. A schematic illustration of the transistor structure proposed with high-κ and metal gate stack is compared to the *classical* structure in Figure 1.5.

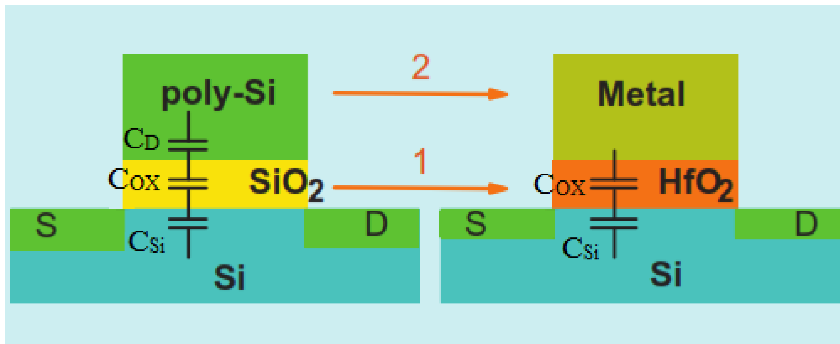

Figure 1.5: Illustration of the replacement of SiO_2 gate oxide and the poly-Si gate by high-κ gate oxide and metal gate (HKMG) [23].

The interface between the metal gate and the gate oxide is, at least, as importat to the MOFET performance as the interface between the channel and the oxide because this interface sets the threshold voltage. In addition, a gate material must be carefully chosen as the work function of the metal is a critical property to the MOSFET operation [18].

The first Hf-based high-κ metal gate (HKMG) transistor was manufactured by Intel in 2007 [24]. Since then, Hf-based HKMG technology has gained wide acceptance, so that nowadays, the family of HfO_2-based materials (HfO_2, $HfSi_xO_y$ and $HfSi_xO_yN_z$) leads the replacement of SiO_2 gate dielectrics in advanced CMOS applications. A comparative between the transistor structure used in 65nm and 45nm node is shown in Figure 1.6.

Despite all the previous advances, even with the use of high-κ oxides, it has not been possible to continue the scaling of planar bulk MOSFETs below the 20 nm node, mainly because the EOT of the gate dielectric cannot be scaled according to Dennard's scaling rules. At the 22 nm node and below, the semiconductor industry has introduced new device structures such as fully depleted device ar-

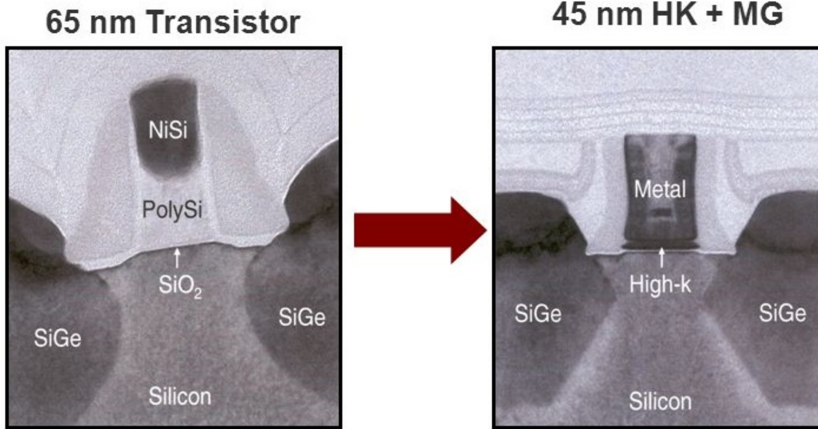

Figure 1.6: TEM image of (left) a 65nm node technology transistor, (right) a 45nm node technology transistor implementing high-κ and metal gate technologies [24].

chitectures, improving short-channel performances without scaling the dielectric EOT, or Gate-All-Around FET (GAA-FET) structures to improve electrostatic properties. Silicon nanowire channel devices, multiple-gate MOSFETs (e.g., Fin-FETs) and ultra-thin body Fully-Depleted Silicon-On-Insulator (FD-SOI) transistors are other developments proposed to allow the miniaturization even beyond the 10 nm node.

1.3 SOI technology

Silicon-on-Insulator (SOI) chips consist of millions of single-transistor islands dielectrically isolated from each other and from the underlying Silicon substrate by an insulator layer. Figure 1.7 shows a comparison of SOI and bulk transistor structures. On the one hand, the vertical isolation protects the thin active Silicon layer from most parasitic effects induced by the substrate: leakage currents, radiation-induced photocurrents, latch-up effects, etc. On the other hand, the lateral isolation makes interdevice separation in SOI free of complicated schemes of trench or well formation [25].

The scaling principles for bulk-Si MOSFETs require a reduction in junction

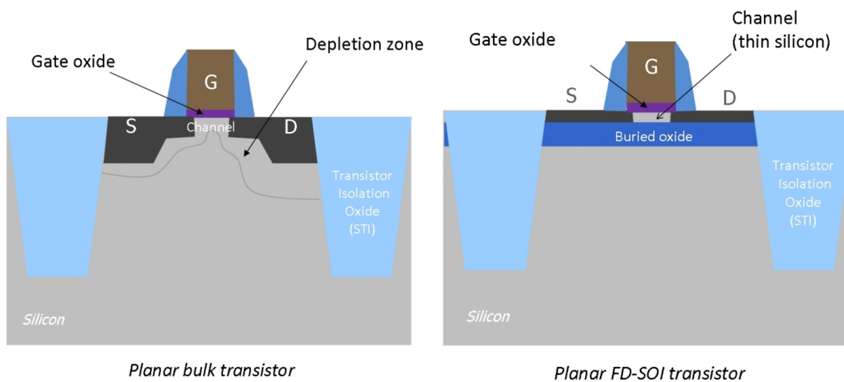

Figure 1.7: Schematic cross-section of transistor structure: (left) planar bulk transistor, (right) planar SOI transistor [26].

thickness and an increase in doping levels, which adversely affect the junction capacitance and carrier mobility. Fortunately, the scaling rules and design windows are more relaxed for SOI transistors because of additional tunable parameters: film and buried-oxide (BOX) thickness, substrate doping, and substrate biasing are available for device optimization [10].

The thinner the film, the lower the drain-to-body field penetration which causes drain-induced barrier lowering (DIBL) effect [25]. Moreover, the limited extension of drain and source regions makes SOI devices less vulnerable to short-channel effects as is shown in Figure 1.8. This advantage permits to fabricate CMOS circuits with lower power dissipation and wider operation temperature range.

1.3.1 SOI wafers fabrication

The main problem to build a SOI structure is to grow a Silicon film on an amorphous substrate (usually SiO_2). This challenge has been overcome through different approaches.

One of the first attempts was called SIMOX (**S**eparation by **IM**planted **OX**ygen). The process consisted in synthesizing a buried layer of SiO_2 beneath the surface of a Silicon wafer by implantation of oxygen ions. For each Si atom, two ions must be implanted to form the silicon dioxide layer [28]. This method implies a high implantation dose, and although some improvements have been achieved

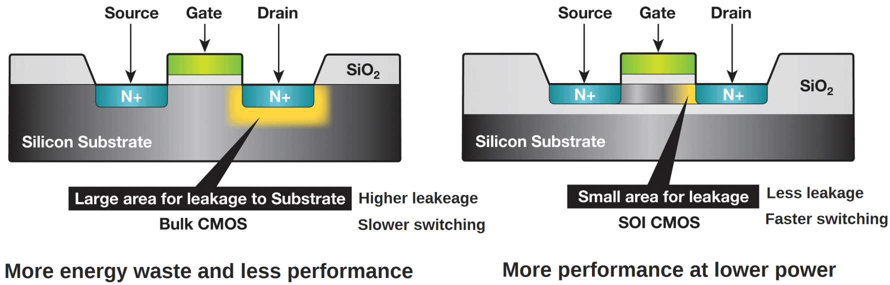

Figure 1.8: Scheme of leakage areas in: (left) bulk transistors, (right) Silicon-on-Insulator transistor [27].

in the process, the quality of the SiO_2 achieved is lower than the native thermal oxide and the number of dislocations introduced is high. Other methods were introduced to improve the SIMOX process. The first one was the Epitaxial Layer TRANsfer (ELTRAN), a technique developed by Canon in 1990 [29]. A high-quality silicon epitaxial film is grown on a porous silicon wafer. This wafer is then bonded to another handle wafer. Finally, polishing and chemical etching processes are used to obtain a SOI wafer as is shown in Figure 1.9.

The crystal quality of the SOI material obtained by wafer bonding and etch-back is, in principle, as good as that of the starting silicon wafer. The dislocation density, however is still high.

The last and most used process to manufacture a SOI wafer is a combination of these two previous methods: it is called Smart-CUT process. Smart-CUT was patented [31] and published [32] by M. Bruel et al. This process is versatile enough to fabricate SOI structures (Unibond wafers) with tuned silicon and oxide layer thicknesses. Good thickness homogeneity, low defect density, high surface quality and good electrical properties are now available in these SOI wafers.

The process steps, shown in Figure 1.10, are describe below:

1. Two conventional wafers (A and B) are considered.

2. In the donor wafer (A), a controllable thermal oxidation is carried out forming an oxide which will serve as the BOX. Its thickness can be adjusted with precision.

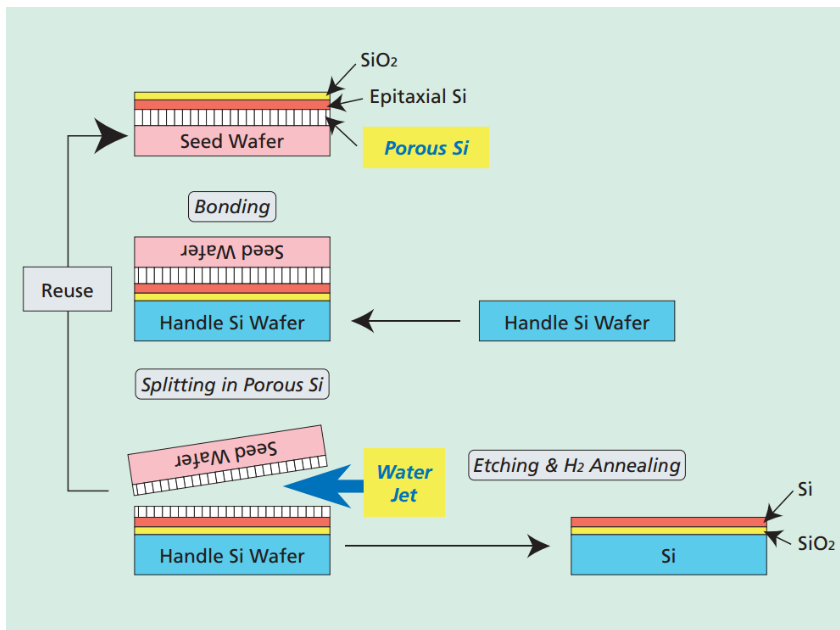

Figure 1.9: Schematic illustration of ELTRAN process flow [30].

3. A hydrogen implantation is carried out through the oxide but inside the Si. The hydrogen induces micro-cavities in the Si which allows defining a breakable plane.

4. The wafers A and B (handle wafer) are carefully cleaned in order to eliminate particles and contamination on their surfaces. Then, the two wafers are aligned and put in contact, so the bonding is made on the entire surface.

5. An annealing treatment is carried out for splitting the wafer provoking an horizontal fracture which separates the wafers naturally.

6. Finally, chemo-mechanical polishing is performed on the SOI film to reduce the surface roughness.

1.3.2 FDSOI transistors

In SOI technology, the MOSFET still remains as the most used part for conventional single gate devices. This fact, and the technological compatibility has

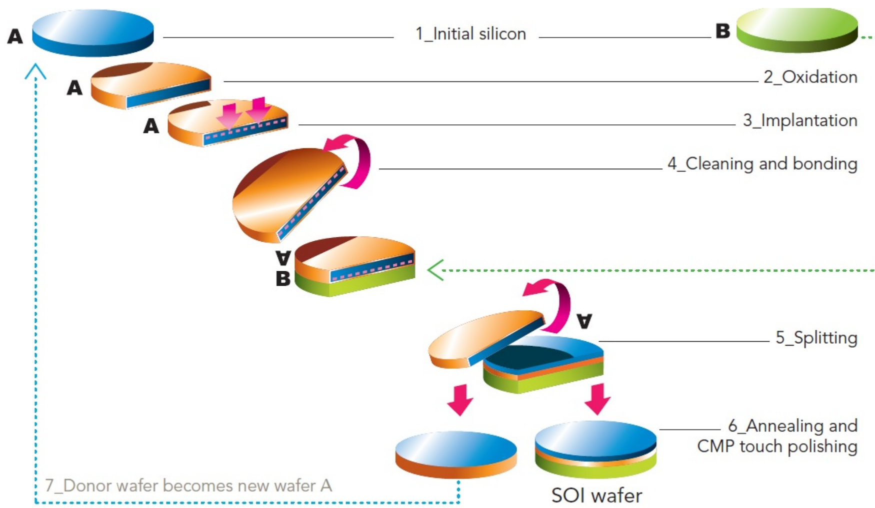

Figure 1.10: Schematic illustration of Smart-cut process flow [33].

allowed the direct transfer of the conventional CMOS technology into SOI wafer based circuits. However, the existence of a buried oxide and the development of new techniques for obtaining SOI structures have opened a new scenario for new devices impossible to implement under the conventional CMOS technology.

Fully Depleted Silicon On Insulator, or FD-SOI technology, is a planar process technology that relies on two primary innovations. First, an ultra-thin layer of insulator, called the buried oxide, is positioned on top of the base silicon. Then, a very thin silicon film implements the transistor channel. Thanks to its thinness, there is no need to dope the channel, thus making the transistor Fully Depleted. The combination of these two innovations is called 'ultra-thin body and buried oxide Fully Depleted SOI' or UTBB-FD-SOI [34, 35].

With this UTBB substrate, SOI technology enables control of the behavior of the transistors (and the threshold voltage) by biasing the substrate underneath the device (Figure 1.11). Moreover, when the bias of the substrate is positive, 'Forward Body Biasing' (FBB), the transistor can be switched faster. This provides an extremely powerful technique to optimize performance and power consumption [36–38].

Overall, FD-SOI shows outstanding power efficiency, leading to higher computing power per watt, lower thermal dissipation, and extended battery life for

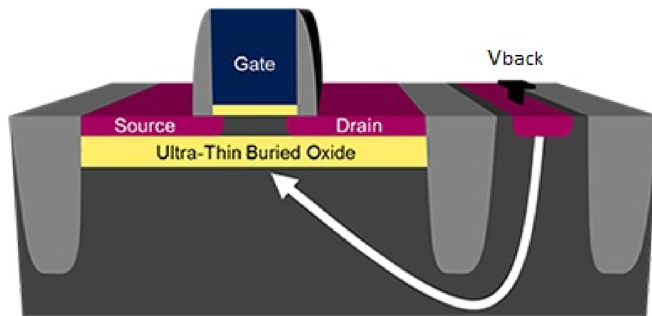

Figure 1.11: Substrate bias illustration in FDSOI transistor [35].

portable devices. FD-SOI significantly improves SRAM memory behavior, allowing it to operate at low voltage and with extremely low leakage currents, while keeping performance comparable to conventional bulk SRAM FD-SOI also brings many advantages to analog design [35].

1.4 Reliability concerns

As mentioned before, the implementation of new materials as gate dielectric, and the change in the metal of the gate and the development of new structures have permitted to increase the performance and the miniaturization of the transistor. However, these introduced improvements also imply reliability issues such as interface traps, carriers generation, current leakages, variability problems, oxide breakdown or increase in the electric field. So that, the reliability characterization of the transistor becomes mandatory in order to know the limitation in the transistors operation.

Concretely, the adaption of HKMG stacks led to a significant improvement of the gate leakage current, however, threshold voltage shift due to charge trapping and trap generation, line edge roughness (LER), work-function variation or breakdown have been remained [39]. In this context, electron mobility values for HKMG stacks typically fall below the trend for conventional SiO(N)/Poly-Si stacks. The degradation is attributed to intrinsic properties of high-κ, such as soft optical phonons, fixed charges, surface roughness, and interface dipoles as is shown in Figure 1.12 [19].

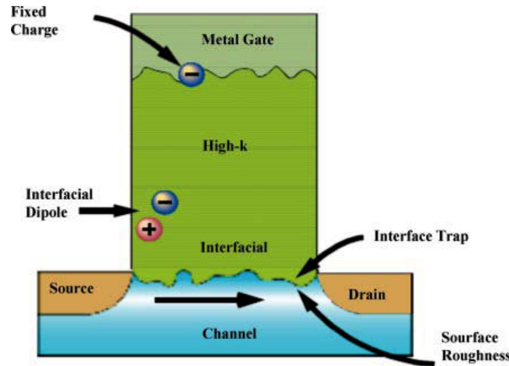

Figure 1.12: Factors contributing to carrier mobility degradation in a HKMG transistor [19].

HKMG stacks transistors include an interfacial layer (IL) between the substrate and the Hf-based dielectric, which usually consists of SiON, because it is expected to prevent, or at least minimize, an interfacial reaction between the high-κ oxide and the underlying Si. However, SiON raised severe bias instabilities being the negative bias temperature instability (NBTI) the most important [40,41]. These bias instabilities are associated to trapping and detrapping of carriers together with the movement of pre-existing oxide charges when the gate is biased or stressed with relatively high voltage. The bias temperature instability was identified as one of the most limiting reliability issues in scaled transistor. It causes an increase in the threshold voltage and following decrease in drain current and transconductance of a MOSFET. High-κ oxides such as Hf-based dielectrics present serious instabilities for negative and positive bias, after negative bias temperature and positive bias temperature stresses [42].

Additionally, the aggressive scaling of MOS transistors has decreased the current signals down to the level where they are not significantly higher than the fluctuations induced by carrier trapping phenomena, as the random telegraph noise (RTN) [43]. Random Telegraph Noise (RTN) is the fluctuation of the MOSFET current induced by stochastic single carrier trappings in gate dielectrics [44–47]. This is an important reliability issue, especially because it may induce fluctuation in V_{th} or I_d and consequently failure of basic logic circuits in highly scaled SRAM or Flash memories [48,49]. In this context, the adoption of technologies such as

high-κ metal gate stacks or ultrathin Silicon-On-Insulator (SOI) substrates has not relaxed the constrain, but even magnified it due to the increase of the number of interfaces combined with less optimized materials [50].

Not only reliability issues are involved by the traps and the gate oxide-channel interface, but also the scaling of the gate length and junctions affects the device performance. When the length of a gate in a miniaturized FET is decreased while leaving all other parameters the same, the threshold voltage is found to decrease with gate length (short channel effect). This short channel effect translates variability in channel length after fabrication into variability of threshold voltage.

As device dimensions decrease, the presence of high electric fields inside the device, are becoming a major design concern. Under the influence of the high lateral fields in short-channel MOSFETs, electrons or holes in the channel and pinch-off regions of the transistor can gain sufficient energy such that their energy distribution becomes much greater than the one expected if they were in equilibrium with the lattice. The generation of these hot carriers can be the cause of several reliability problems. These carriers can lose their energy via impact ionization, which results in substrate currents. These currents can initiate latch-up in CMOS structures [51]. Specifically impact ionization is an inherent phenomenon of very scaled MOSFET operated at a high lateral electric field regime ($V_D = V_{DD}$) [25]. The highly energetic electrons knock lattice electrons out of their bound state and promote them to a state in the conduction band, creating electron-hole pairs. In Silicon-On-Insulator (SOI) N-MOSFETs, the minority carriers, electrons, are collected by the drain, while the majority carriers, holes, cannot escape through the substrate of the device, giving rise to a gradual charge storage in the body of the transistor [52]. This phenomenon is typically manifested as an abrupt increase in the saturation current of partially depleted (PD) transistors (also known as kink effect) consequence of both the threshold voltage reduction and the source-body potential barrier lowering, however this effect is not as usual in fully depleted (FD) devices [53]. From the SOI technology prospective, impact ionization has a two-folded effect: on positive side, it leads to an increase of the device performance by the increase on the saturation current [54], especially in the field of digital circuits. In addition, impact ionization has also been used as a fast programing mechanism in SOI floating-body memory cells [55]. However, on the negative side, impact ionization worsens the noise characteristics and it may lead

to reliability issues arisen from hot carrier generation. As illustrated, the large contribution that impact ionization has on the characteristics of SOI transistors makes this phenomenon a subject that cannot be disregarded on present technologies, furthermore, when the gate length of the transistors is scaled more intensely than the supply voltage, yielding a dramatic rise in the lateral electric field.

1.5 Other structures and two dimensional materials

As the roadmaps of the biggest manufacturers show (one example shown in Figure 1.13) and as scaling of silicon based transistors has approached its physical limit, intensive efforts in finding alternative structures and channel materials have been made. For future logic devices beyond 10 nm node, the main effort is focused on Ge and III-V materials because of their superior carrier mobility. Also the structures using Nano-wire Si as the MOSFET channel, while continuing to employ the traditional high-κ oxides, are considered. Moreover, novel and two-dimensional materials like graphene or transition metal dichalcogenides are being taken into account.

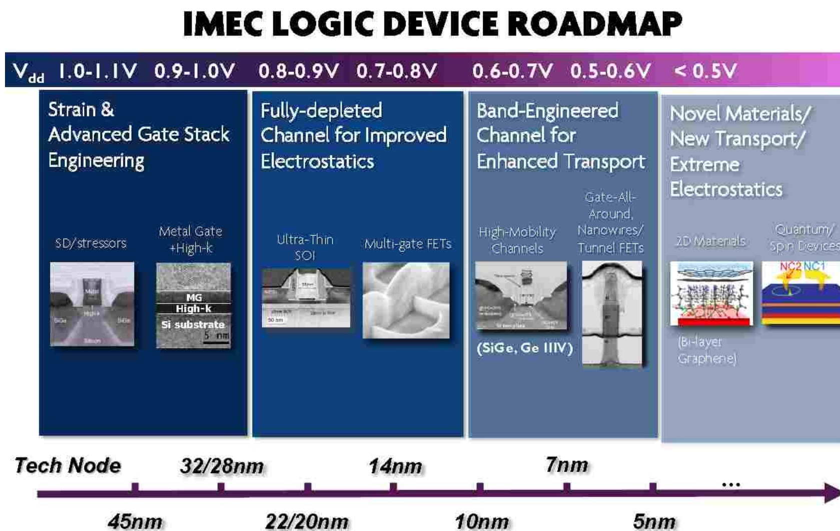

Figure 1.13: IMEC roadmap for the next technology nodes.

Graphene is an allotrope of carbon in the form of a two-dimensional, atomic-

scale, hexagonal lattice in which one atom forms each vertex. Beyond any doubt graphene has stirred the world of material research due to its unique physical properties: 200 times stronger than steel, high conductivity of heat and electricity and nearly transparent [56, 57]. In particular, in the field of electronics, graphene has found a huge niche of interest [58]. However the expectations have not been yet materialized into real-world applications due, in part, to the difficulty to produce and pattern large graphene samples. The efficient fabrication of graphene layers is a critical process to achieve the expected properties at a reasonable cost. The industrial methods for producing high quality samples, beyond the experimental approach based on the 'scotch tapping' [59], mainly involve high temperature vacuum annealing of Silicon Carbide [60] or Chemical Vapor Deposition (CVD) [61] as shows the Figure 1.14. Despite the repeatability of those methods is more than proven and the quality of the samples well demonstrated, it is also true that those methods do not fully satisfy yet the requirement for cost-effective circuit integration [12].

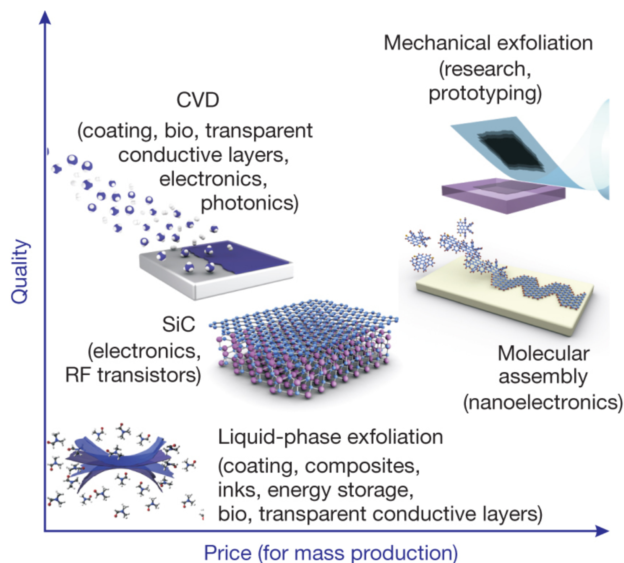

Figure 1.14: Schematic illustration of quality as a function of cost (price) for the different graphene fabrication methods [12].

Not far from the bellwether research activity related to graphene and its two-dimensional counterparts [62], the interest around a *poorer* form of graphene, the

so called reduced graphene oxide (rGO), has gained a lot of relevance due to its multiple spectrum of applications at a much lower technological effort [63–66]. Although it is far from achieving the unique properties of graphene, rGO preserves, to some extent, part of its virtues (flexibility, electrical and thermal conductivity...) [67]. But the most appealing advantage of the laser-assisted photothermal reduced graphene oxide is the possibility to create large precise conductive patterns (rGO) electrically isolated by the unexposed graphene oxide areas (GO), escaping from the need for lithographic masks. More information, details and results about the synthesize of reduced Graphene Oxide will be shown in Appendix A.

The discovery of graphene has unveiled another family of materials with layered structures, which includes boron nitride, topological insulators such as Bi_2Te_3 and Bi_2Se_3, and transition metal dichalcogenides like MoS_2, WS_2, and $NbSe_2$. Though graphene, a fascinating two-dimensional (2D) crystal, has shown a superior carrier mobility, its zero bandgap property limits its application to logic devices as graphene transistors cannot have high on/off ratios. As opposed to the semi-metal graphene, transition metal dichalcogenides (such as MoS_2), as another type of layered structure material, have shown great potential in device applications due to band gap, thermal stability, carrier mobility, and compatibility to silicon CMOS process [68]. Example of one transistor with MoS_2 as channel material proposed by Radisavljevic en al. is shown in Figure 1.15 [69]. In order to realize high performance MoS_2 or some other transition metal dichalcogenide MOSFETs, major issues must be solved: how to deposit a high-quality dielectric on 2D crystal or the fabrication of low-resistivity metal-semiconductor junction to be used as device contacts.

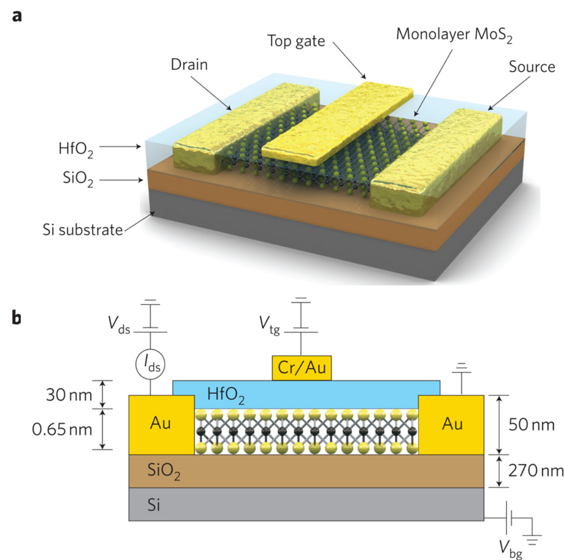

Figure 1.15: MoS_2-channel transistor proposed by Radisavljevic et al. **(a)**Three-dimensional schematic view, **(b)** Cross-sectional view with electrical connections [69].

1.6 Conclusions

Some improvements related to the miniaturization of transistors have been achieved by implementing the gate oxide with high-κ materials and substituting the poly-Si gate by a metallic material. Silicon-on-insulator technology, and concretely FD-SOI transistors with ultra-thin-body has allowed to continue with the transistor scaling beyond 22nm nodes. However, all these improvements also imply reliability issues such as interface traps, carrier generation, current leakages, variability problems, or increase in the electric field which produces degradation effects such as bias temperature instability, random telegraph noise, gate oxide breakdown or hot carrier degradation. In the next chapters, these effects will be characterized in samples from the ultimate technology nodes.

Chapter 2

Experimental Characterization

This chapter introduces the experimental techniques and the theoretical framework which allow to carry out the electrical characterization of reliability issues in semiconductor devices. In Section 2.1, the characterization techniques used to extract the sheet resistance and the contact resistivity of the bare substrates and metallized substrates are detailed. In Section 2.2, the Pseudo-MOSFET technique used for electrical characterization of bare SOI wafers, and the defects located at the oxide-Si interfaces of these devices are described. Section 2.3 shows some of the experimental processes used for the parameter extraction of SOI transistors. The substrate bias dependence of the threshold voltage, the sources of instability and the noise characterization are detailed. In addiction, the characterization of wafer variability through automatic setups is explained in this chapter.

2.1 Bare substrates

The resistivity of the materials and their interaction with the metallic contacts and pads (contact resistance) are parameters which affect the transistor behavior and define some of the electrical properties of the device. This characterization is important both in Silicon films, used for generating the channel, as in new materials like graphene or MoS_2, materials called to participate in the new technological nodes. The resistivity (ρ) (inverse of conductivity, σ) of the material, and the semiconductor-contact interaction are usually tied each other, so that both parameters can be simultaneously extracted through the same characteriza-

tion method. In this context, several experimental setups, used to determine the resistivity, sheet resistance and contact resistance of the materials are taken into account and described in the next sections.

2.1.1 Material resistivity

2.1.1.1 Point-contact methods: Two-point and Four-point

Point-contact methods constitute one of the fastest approaches for monitoring the electrical properties of the samples such as intrinsic conductivity or contact resistance. The experimental setup, shown in Figure 2.2, is based on the in-line point-contact configuration with direct contact of probes or ad-hoc deposited metal contacts (the probes are placed on top of the metal in this latter case). In this setup the total resistance, R_T, is given by [70]:

$$R_T = V/I = 2R_W + 2R_C + R_{DUT} \tag{2.1}$$

where R_W is the wire or probe resistance, R_C the contact resistance, and R_{DUT} the resistance of the device under test.

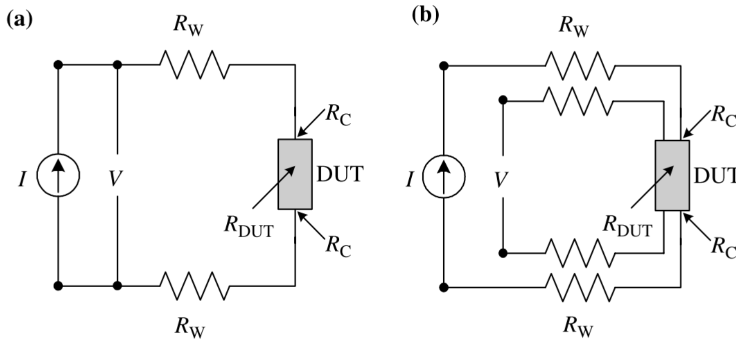

Figure 2.1: Schematic illustration of (a) two-point and (b) four-point resistance measurement configuration. Reproduced from [70].

If two probes are used for the electrical characterization, each contact serves as a current and as a voltage probe: an illustration of the setup is shown in Figure 2.1.a. Clearly it is impossible to determine R_{DUT} with this measurement configuration, the different terms in the equation are not separable and the resistance of

the device under test is masked by the contact and the probe resistance. To solve this issue, the four-probe or four-contact configuration is used. The new setup is shown in Figure 2.1.b. Although the new path (voltage measurement path) contains R_W and R_C contributions, the current flowing is very low due to high input impedance of the voltmeter. Hence, the voltage drops across R_W and R_C are negligible and the measured voltage is essentially the voltage drop across the DUT.

The experimental representation of the previous schemes is shown in Figure 2.2 and summarized in the next points:

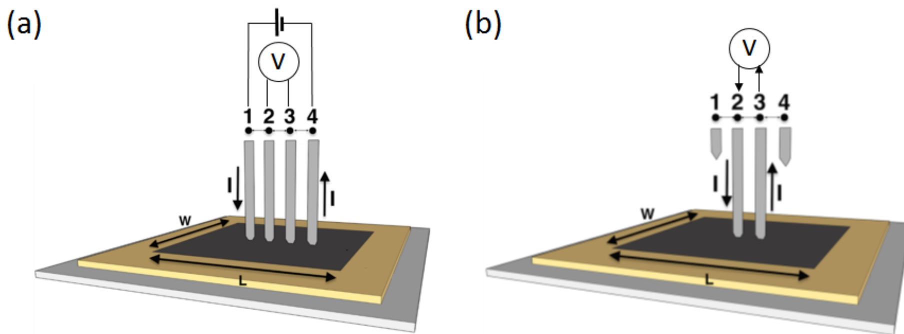

Figure 2.2: (a) Four point-contact setup: current I is forced between probes 1 and 4 by applying a constant bias V_{1-4} while the voltage drop is measured between probes 2 and 3. (b) Two point-contact setup: current I and voltage V are simultaneously applied and measured through the same probes (2 and 3).

(i) *Four point-contact setup (4PC)*: A voltage is applied between probes 1 and 4 (V_{1-4}) while the current, I, is simultaneously measured (Figure 2.2.a). The voltage difference between probes 2 and 3 (V_{2-3}) is simultaneously monitored without current flow through them (and therefore, without voltage drop due to contact resistance). The resistance $R_{4p} = V_{2-3}/I$ obtained with this configuration can be related with the sheet resistance by the relationship $R_{sh} = FR_{4p}$, where F is a form factor depending on the sample dimensions and probes position which will be described below [70]. This technique is sometimes also referred as Kelvin method [71].

(ii) *Two point-contact setup (2PC)*: A voltage is applied between probes 2 and

3 (V_{2-3}) while the current flowing through them is simultaneously measured (Figure 2.2.b). This type of measurement is easier to be carried out since there is no need to take precautions regarding probe alignment, but it is affected by the impact of the contact and probes resistances which can eventually mask the intrinsic conductivity of the sample under study [72]. Note also that even in the case that the contact resistance could be neglected, the resistance measured by the first method may not correspond to the value given by V_{2-3}/I_{2-3} due to the current spreading. Nevertheless, the two point contact method represents a good procedure to determine the contact resistance (distance-dependent two-point probe method) [73, 74].

As mentioned, a form factor is applied to determine the resistance of the material by using four-contact method. This factor takes into account the proportion of current which flows through the internal probes, the sample size, probes inter-distance, among others. In the following lines the final resistivity value is derived [70].

The electric field, E, is related to the current density, J, the resistivity ρ, and the voltage V through the next expression:

$$E = J\rho = -\frac{dV}{dr}; J = \frac{I\rho}{2\pi r^2} \tag{2.2}$$

where the relationship between the current density and the current, I, is extracted from the area estimated under the probe and represented in the Figure 2.3.a. The voltage at point P at a distance r from the probe, is:

$$\int_0^V dV = -\frac{I\rho}{2\pi}\int_0^r \frac{dr}{r^2}; V = \frac{I\rho}{2\pi r} \tag{2.3}$$

For the configuration of Figure 2.3.b, the voltage in the point P can be expressed as:

$$V = \frac{I\rho}{2\pi r_1} - \frac{I\rho}{2\pi r_2} = \frac{I\rho}{2\pi}(\frac{1}{r_1} - \frac{1}{r_2}) \tag{2.4}$$

where r_1 and r_2 are the distances from probes 1 and 2, respectively and the sign depend on the current direction. Now, following the configuration of the Figure

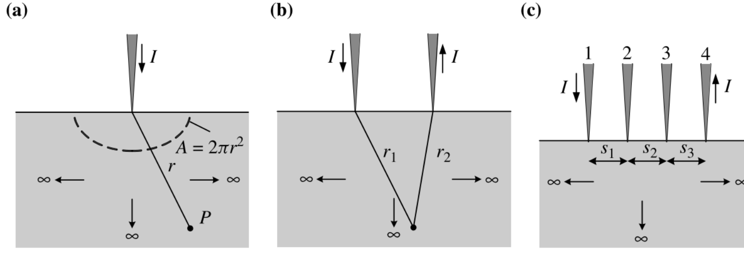

Figure 2.3: Schematic illustration showing current flow and voltage measurement in: (a) one-point probe, (b) two-point probes, and (c) collinear four-point probes configuration [70].

2.3.c, the voltages at probes 2 and 3 are:

$$V_2 = \frac{I\rho}{2\pi}(\frac{1}{s_1} - \frac{1}{s_2 + s_3}) \tag{2.5}$$

$$V_3 = \frac{I\rho}{2\pi}(\frac{1}{s_1 + s_2} - \frac{1}{s_3}) \tag{2.6}$$

where s_1, s_2 and s_3 are the probe spacing (expressed in cm). The total voltage measured between probes 2 and 3 ($V_{2-3} = V_2 - V_3$) can be expressed as:

$$V_{2-3} = \frac{I\rho}{2\pi}(\frac{1}{s_1} - \frac{1}{s_2 + s_3} - \frac{1}{s_1 + s_2} + \frac{1}{s_3}) \tag{2.7}$$

And the resistivity ρ is given by

$$\rho = \frac{2\pi}{\frac{1}{s_1} - \frac{1}{s_2+s_3} - \frac{1}{s_1+s_2} + \frac{1}{s_3}} \frac{V_{2-3}}{I} \tag{2.8}$$

If the probe spacing are equal, the previous expression is reduced to:

$$\rho = 2\pi s \frac{V_{2-3}}{I} \tag{2.9}$$

However, Expression 2.9 corresponds to semi-infinite macroscopic samples. For an arbitrarily shaped sample the resistivity is given by [70]:

$$\rho = 2\pi s F \frac{V_{2-3}}{I} \tag{2.10}$$

where F corrects for probe location near sample edges, for sample thickness, sample diameter, probe placement and temperature [70]. This factor is a product of several independent correction factors. If the sample is thinner than the probe spacing, the correction factors can be independently calculated. In this case, $F = F_1F_2F_3$ where F_1 corrects for sample thickness, F_2 for the lateral sample dimension and F_3 for the placement of the probes relative to the sample edges. If very thin samples are considered, $F_2 \approx F_3 \approx 1$ and F_1 can be approximated by the next expression [70]:

$$F_1 = \frac{t/s}{2ln(2)} \tag{2.11}$$

where t is the layer thickness. Nevertheless, if the sample is not so thin to consider this approximation, factors F_1, F_2 and F_3 depend on the dimension of the samples, and their values are tabulated in [75,76]. Using the cited approach, the resistivity expression can be extracted through:

$$\rho = \frac{\pi t}{ln(2)}\frac{V}{I} \tag{2.12}$$

where the *sheet resistance*, R_{sh}, expressed in units of ohms per square is given by:

$$R_{sh} = \frac{\pi}{ln(2)}\frac{V}{I} \tag{2.13}$$

The application of point-contact method to extract the sheet resistance of reduced graphene oxide samples are detailed in Appendix A.

2.1.2 Contact resistance

In transistors and other electronic devices, electrical contacts are an essential part of the device, and determining of the contact resistance is mandatory, since the overall performance of the device might be affected. As mentioned in the previous section, sheet resistance and resistivity are determined minimizing effects of contact resistance by using four-contact methods. As it will show, the contact resistance can be characterized by using an extension of the point-contact technique.

Considering the simple resistor geometry shown in Figure 2.4, where the two contacts are located at the ends of the bar and each one has a contact area A_c,

the measurement of the total resistance consists of several components:

$$R_T = 2R_m + 2R_C + R_{semi} \tag{2.14}$$

where R_T is the total measured resistance, R_m is the resistance due to the contact metal, R_C is associated with metal/semiconductor interface, and R_{semi} is the semiconductor (or material in general terms) resistance. In this context, the resistance of a single contact would be R_m+R_C. However, the most usual situation is that the resistivity of the metal is much lower than R_C, and therefore R_m is ignored.

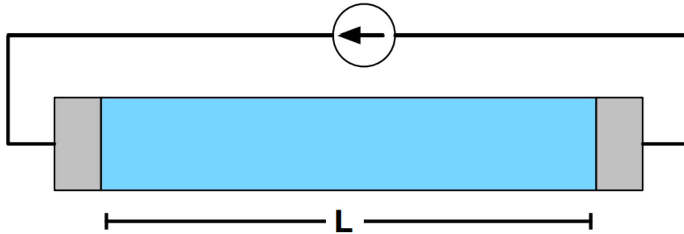

Figure 2.4: Cross-sectioned illustration of a resistor with two lateral contacts.

The semiconductor (or material) sheet resistance can be expressed as [70]:

$$R_{semi} = R_{sh}\frac{L}{W} \tag{2.15}$$

where L and W are the length and width of the material. Therefore, the total resistance is given by:

$$R_T = R_{sh}\frac{L}{W} + 2R_C \tag{2.16}$$

These results suggest a method for measuring the contact resistance. In the case of the resistor, if different lengths are available, plotting the total resistance as a function of the correspondent length of the device is possible to extract the sheet resistance and the contact resistance (Figure 2.5). Extrapolating to $L = 0$, the residual resistance corresponds to twice the contact resistance. The sheet resistance of the semiconductor can be found from the slope of the curve.

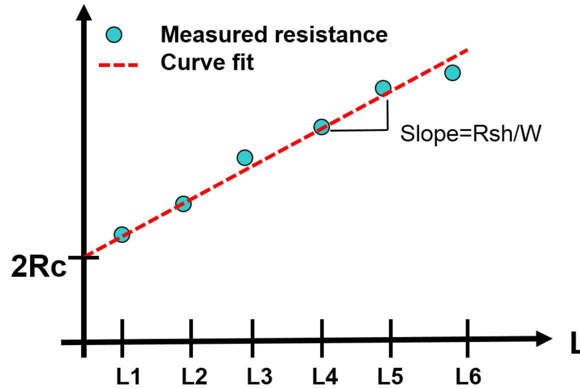

Figure 2.5: Illustration of total resistance as a function of different device lengths for the contact and sheet resistance extraction.

2.1.2.1 Contact resistivity

The contact resistance depends on the size of the contact, therefore to compare different contact deposition methods, the contact resistance is not an accurate parameter. To solve this fact, contact resistivity is extracted. Considering a small region Δx in the interface of contact-semiconductor, contact resistance is give by [70]:

$$R_C = \rho' \frac{\Delta x}{A_C} \tag{2.17}$$

where A_C is the area of the contact. The resistivity of the contact is expressed as follow.

$$\rho_c = \lim_{\Delta x \to 0} (\rho' \Delta x) = R_C A_C \tag{2.18}$$

This extracted ρ_c corresponds to the contact resistivity in the structure of Figure 2.4. However, this structure (resistor) is not the usual geometry used in transistors and other device structures. In fact, in planar technology, the contact are deposited on the surface of the material as is shown in Figure 2.6. In these structures, the current-flow through the semiconductor is uniform, but as is observed in the figure, the flow into the contact is rather different. At the edge of the contact, the current flowing in (or out) is significant. Nevertheless the current drops off until, at the far edge, there is no current. This effect is known as 'current

crowding', and can be modeled by the following expression [70]:

$$I(x) \propto \exp(\frac{-x}{L_T}) \tag{2.19}$$

where $I(x)$ is the current at the x position at the contact and L_T is the transfer length, defined as the distance from the edge of the contact over which $1/e$ of the total current is transferred from the semiconductor to the metal [77], being modelled as [70]:

$$L_T = \sqrt[2]{\frac{\rho}{R_{sh}}} \tag{2.20}$$

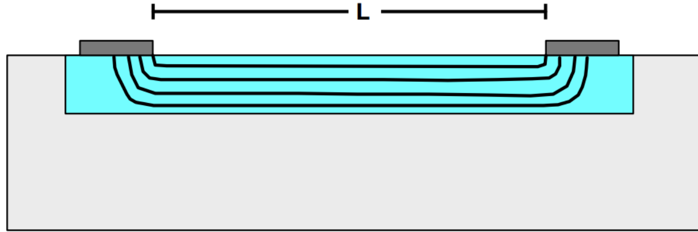

Figure 2.6: Cross-sectioned illustration of two contacts deposited on a semiconductor layer. Current flow is represented by lines.

The transfer length represents the average distance that electrons (or holes) travel in the semiconductor beneath the contact. The contact resistance can be expressed as a function of the transfer length as:

$$R_C = \frac{\rho_C}{L_T W} = \frac{R_{sh} L_T}{W} \tag{2.21}$$

Introducing Eq. 2.21 in Eq. 2.16, the total resistance is given by:

$$R_T = R_{sh}\frac{L}{W} + 2\frac{\rho_C}{L_T W} = R_{sh}\frac{L}{W} + 2\frac{R_{sh} L_T}{W} = \frac{R_{sh}}{W}(L + 2L_T) \tag{2.22}$$

The transfer length is extracted by extrapolating back to the horizontal axis the experimental results of total resistance as a function of the different lengths as is shown in Figure 2.7.

This method to obtain the contact resistance through the transfer length is

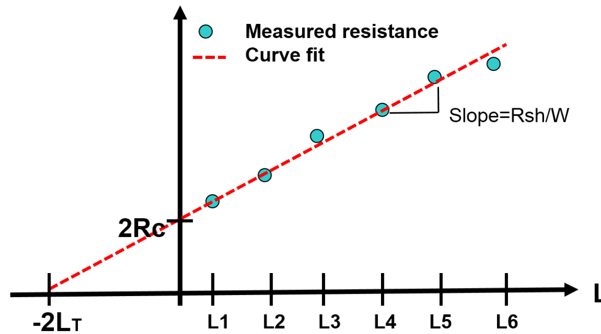

Figure 2.7: Illustration of total resistance as a function of different device length for the contact and sheet resistance extraction.

called transmission line method (TLM). One of the most usual patterns designed to carry out the resistance characterization is shown in Figure 2.8. Resistance is measured between each pair of contacts (gray rectangle) to plot the TLM graph previously mentioned.

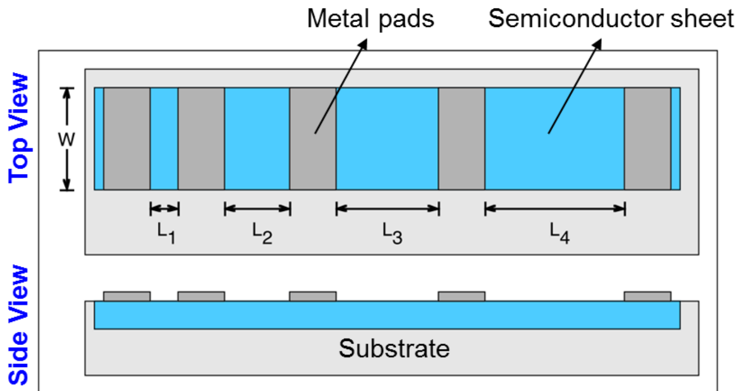

Figure 2.8: Illustration of structure designed for TLM characterization.

A problem of the previous TLM characterization is the fact that the width of the contact is not usually the same that the width of the sheet, obtaining erroneously high p_c [70]. However, the circular transmission line model (cTLM) where circular structures, consisting of a conducting circular inner region of radius L, a gap of width d, and a conducting outer region, solves this p_c overestimation

[70, 78]. The conducting regions are usually metallic and the gap typically varies from a few microns to tens of microns. The circular test structure has another advantage. It is not necessary to insolate the layer to be measured, because current can only flow from the central contact to the surrounding contact. For equal sheet resistances under the metal and in the gap, and for the geometry of the circular contact resistance structure in Figure 2.9, the total resistance between the internal and the external contacts can be approximated as [79]:

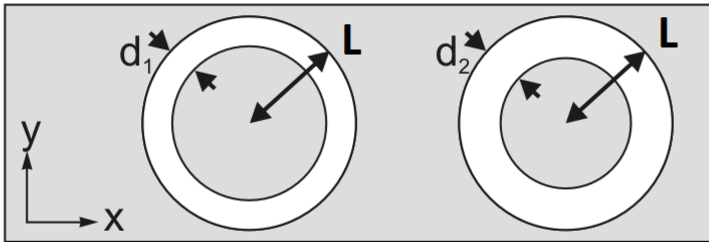

Figure 2.9: Circular contact resistance test structure. The gray regions represents metallic regions. (a) Spacing d and radius L are defined in the two structures.

$$R_T = \frac{R_{sh}}{2\pi}\left[\frac{L_T}{L}\frac{I_0(\frac{L}{L_T})}{I_1(\frac{L}{L_T})} + \frac{L_T}{L+d}\frac{K_0(\frac{L}{L_T})}{K_1(\frac{L}{L_T})} + \ln(1+\frac{d}{L})\right] \tag{2.23}$$

where I and K denote the modified Bessel functions of the first order. For $L >> 4L_T$, the Bessel function ratios I_0/I_1 and K_0/K_1 tend to unity and R_T becomes [70]:

$$R_T = \frac{R_{sh}}{2\pi}\left[\frac{L_T}{L} + \frac{L_T}{L+d} + \ln(1+\frac{d}{L})\right] \tag{2.24}$$

Additionally, if $L >> d$ as occurs in Figure 2.9, R_T is defined as:

$$R_T = \frac{R_{sh}}{2\pi L}(d+2L_T)C \tag{2.25}$$

where C is the correction factor defined as:

$$C = \frac{L}{d}\ln(1+\frac{d}{L}) \tag{2.26}$$

As mentioned in TLM method, if the total resistance is plotted as a function of gap spacing d, a linear dependence is obtained. The contact resistance (R_C) and transfer length (L_T) can be extracted from the intercept with y- and x-axis respectively. The sheet resistance of the material under the metal can be obtained from the slope of the curve.

Transmission electron microscopy (TEM) images of an experimental example carried out in this thesis on reduced graphene oxide (rGO) is shown in Figure 2.10, the physical dimension of the cTLM patterns (s and L), deposited by using a mask lithography, have been labeled.

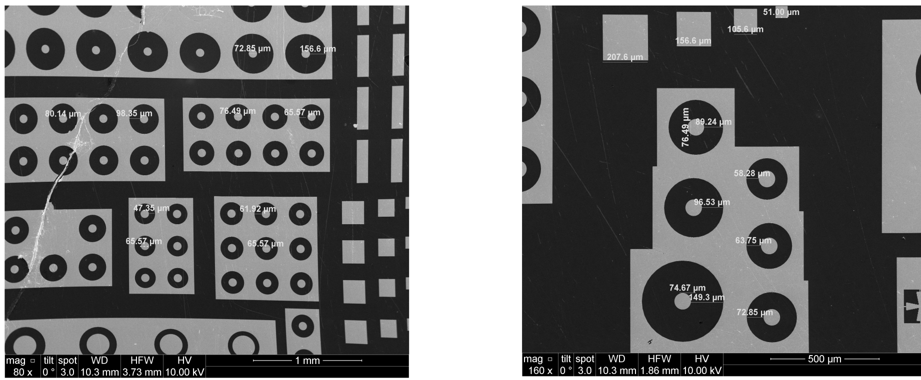

Figure 2.10: TEM image of circular contact resistance test structures on reduced graphene oxide. The gray zones represent metallic regions. Feature sizes are shown in the image.

2.2 Bare SOI wafers

The fabrication flow of an ultimate technology transistor includes several state of the art complex processes: substrate growth, dopant implantation, oxide deposition, passivation, pad metallization, etc. All these steps are very expensive in cost and time. Additionally, any manufacturing process introduces inevitable defects in the substrates. When dealing with Silicon-On-Insulator (SOI) wafers, most of the defects (broken bonds, impurities, imperfections) are set within the Si/BOX interface [25]. In this context, it is interesting to know the quality, variability and reliability of the samples (wafers) during the fabrication process. If

the wafers exhibit low mobility, large variability in the threshold voltage, current paths in the gate (or buried) oxide or other degradation effects which would imply a bad operation of the fully processed transistor; this sample or wafer could be discarded immediately, saving some expensive manufacturing steps. These bare wafers which are not fully processed can be electrically characterized before any CMOS processing, and the technique used for their electrical characterization and the parameter extraction is called pseudo-MOSFET technique.

2.2.1 Pseudo-MOS technique

The pseudo-MOS or pseudo-MOSFET is a simple test structure to characterize the Si layer and the Si-oxide interfaces of Silicon-On-Insulator wafers without having to fabricate test devices [70,80]. The original implementation is illustrated in Figure 2.11.a, where the bulk Si-substrate acts as the gate of the transistor, the buried oxide (BOX) as the gate oxide and the Si-film as the transistor body. The characterization is carried out in a manual probe station (Figure 2.11.b), where the mechanical probes work as source and drain contacts. By biasing the gate, it is possible to set the bottom interface of the silicon film in inversion, depletion, or accumulation, allowing both electron and hole conduction. Drain current-gate voltage and drain current-time measurements allow the extraction of the effective electron and hole mobilities, threshold voltage, dopant density, interface and oxide charge densities [25].

Regardless of the type of channel created, when the threshold condition is reached, the current flows governed by the same MOS transistor laws. Since the experimental curves are similar to those measured for fully processed MOSFETs, the electrical parameters, such as flat-band/threshold voltage, carrier mobility or interface traps density, can be extracted through well-established standard equations. If the drain voltage used in all the experiments (V_D) is low enough to ensure an ohmic behavior, the $I_D(V_G)$ curve can be approximated by the simplified MOSFET formula [25]:

$$I_D = f_g C_{BOX} \mu (V_G - V_{TH}) V_D \tag{2.27}$$

where C_{BOX} represents the capacitance associated to the BOX per unit area, f_g is a geometric factor which accounts for the spreading of the current lines,

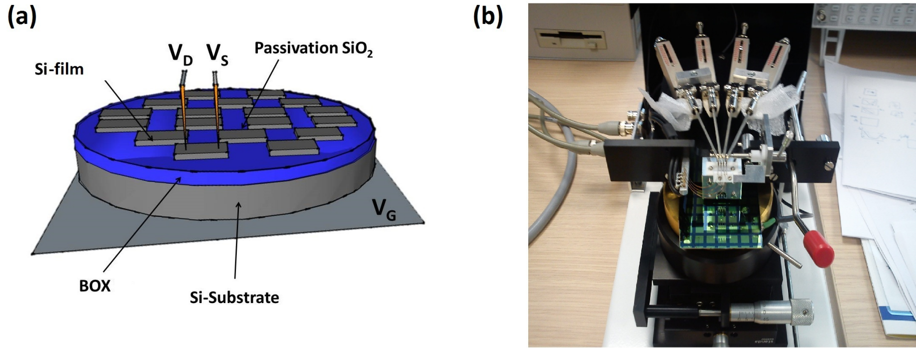

Figure 2.11: (a) Pseudo-MOSFET structure. Two probes act as drain and source contacts. The bulk Si and the buried oxide act as gate contact and gate oxide respectively. (b) Manual probe station used for the experimental characterization.

and V_{TH} is the threshold voltage for hole/electron channels defined in the next expression [81]:

$$V_{TH} = \Phi_{fb} + \left(1 + \frac{C_{it1}}{C_{BOX}}\right) 2\Phi_F + \frac{qN_A t_{Si}}{C_{BOX}} \tag{2.28}$$

where Φ_{fb} is the flatband potential, $C_{it} = qD_{it}$, the BOX-channel interface trap capacitance. The rest of parameters have the usual meaning. Similarly, the transconductance is defined as the derivative of the current law with respect to the gate bias:

$$g_m = \frac{dI_D}{dV_G} = f_g C_{BOX} \mu V_D \tag{2.29}$$

Figure 2.12 shows experimental results for drain current and transconductance as a function of the gate bias for a bare SOI wafer. The hole and electron channels are observed in the $I_D(V_G)$ plot where the mobility and threshold voltage can be extracted. In the transconductance curve ($g_m(V_G)$), accumulation, depletion and inversion regimes are well distinguished.

2.2.2 Defects of SOI substrates

As mentioned, any manufacturing process introduces defects in the fabricated substrates. These defects, or dislocations, are harmful for the performance of the

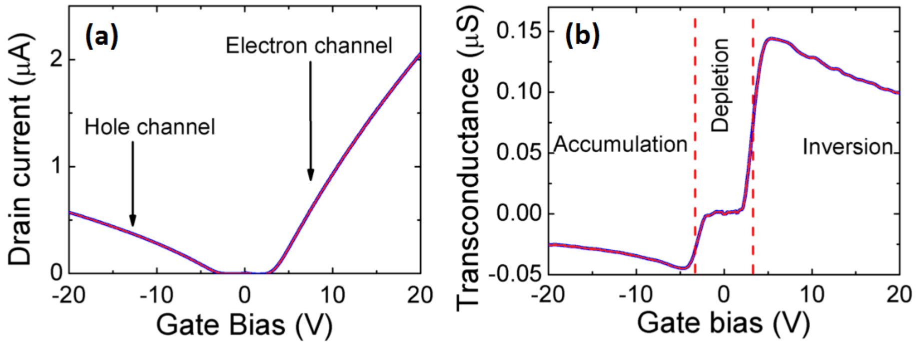

Figure 2.12: (a) Drain current as a function of gate bias. (b) Transconductance as a function of gate bias. Non-passivated bare SOI wafer, T_{Si} = 88 nm, T_{BOX} = 145 nm, V_D = 20 mV.

device, causing severe reliability issues such as reduction of the mobility, threshold voltage shifts, increase of leakage currents... The majority of these instabilities are caused by the imperfections at the Silicon-oxide interfaces (usually $SiO_2 - Si$) and inside the oxide. These imperfections are translated into oxide charges and are summarized in the following items [70]:

- *Interface Trapped Charge (Q_{it}, D_{it})*: These are positive or negative charges, caused by structural defects, oxidation-induced defects, metal impurities, or other defects caused by bond breaking processes. The charges are located at the $SiO_2 - Si$ interface. Depending on the surface potential, the charges can be charged or discharged by carriers. The majority of these charges can be neutralized by hydrogen or nitrogen forming gas annealing. Surface-states, fast states, interface states are usually referred to interface trapped charge.

- *Fixed Oxide Charge (Q_f)*: Fixed oxide charge is usually referred to positive charge near to the oxide-semiconductor interface, whose origin is related to the oxidation stage during the fabrication process. The density of fixed oxide charge can be reduced by annealing in nitrogen or argon ambient.

- *Oxide Trapped Charge (Q_{ot})*: This charge is related to holes or electrons which are trapped in the oxide by ionizing radiation, avalanche injection, Fowler-Nordheim tunneling, or other mechanisms. Therefore, the charge

can be positive or negative.

- *Mobile Oxide Charge (Q_m)*: These charges are caused primarily by ionic impurities such as Na^+, Li^+, K^+, and possibly H^+, introduced during the fabrication process.

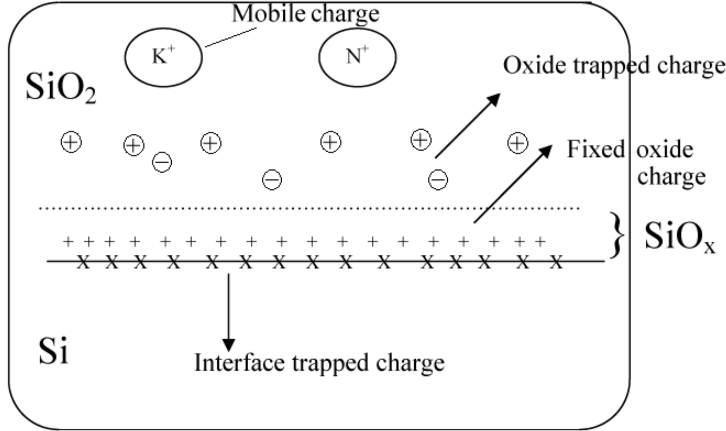

Figure 2.13: Schematic cross-sectioned illustration of the oxide charges in a $SiO_2 - Si$ interface.

The effect of these oxide charges (illustrated in Figure 2.13) in the reliability of the devices is modeled through the flatband voltage of the transistor, determined by the metal-semiconductor work function difference Φ_{MS} and the various oxide charges, through the relationship [70]:

$$V_{FB} = \Phi_{MS} - \frac{Q_f}{C_{ox}} - \frac{Q_{it}(\Phi_s)}{C_{ox}} - \frac{1}{C_{ox}}\int_0^{t_{ox}} \frac{x}{t_{ox}}\rho_m(x)dx - \frac{1}{C_{ox}}\int_0^{t_{ox}} \frac{x}{t_{ox}}\rho_{ot}(x)dx \tag{2.30}$$

where $\rho(x)$ is the oxide charge per unit volume.

The shift in the flatband voltage implies a shift in the threshold voltage (in inversion regime for thin devices: $V_{TH} = V_{FB} - 2\Phi_F - \frac{Q_B}{C_{OX}}$, where Q_B is the depletion charge density), hence the importance of oxide charges in reliability studies. Moreover, SOI technology introduces a buried oxide (BOX) in the body of the transistor, i.e., an additional $SiO_2 - Si$ interface. This interface may contribute with degradation in the performance of the device, being a possible

source of instabilities, especially when the transistor is back-biased or the silicon film is fully depleted.

The influence of oxide charge is even worse in pseudo-MOS transistors, where the channel is formed at the BOX/Si interface and the native (spontaneous) oxide on the surface of the pseudo-MOS structure may influence the device performance, especially when the film thickness is scaled down since the channel will be closer to the surface.

It has been experimentally reported [82], when the Si film was scaled down, that a coupling between the interface states from the top (free) surface and the channel appears and the usual electrical behavior of the cell or pseudo-MOS device changes. This effect, not previously accounted for in classical pseudo-MOSFET models (Eq. 2.28), manifests itself in an increase of the threshold voltage when the film thickness is reduced. Thus, the resulting expression for the threshold voltage, from the Equation 2.27, accounting the traps at the BOX-Si interface (D_{it_1}) and the thickness dependence in ultra-thin layers, is given by [82]:

$$V_T = \Phi_{fb} + \frac{2kT}{q}(1 + \frac{qD_{it_1}}{C_{BOX}}) \ln \left[\frac{1}{t_{Si}} \sqrt{\frac{2kT\epsilon_{Si}}{q^2 n_i}} \right] \tag{2.31}$$

where passivation of the surface has been considered in this model. In this case, although the passivation process does not entirely eliminate the traps, experiments suggest that trap density at the interface between the native (top) oxide and the channel is small enough ($D_{it2} \approx 2 \cdot 10^{11} (cm^2 eV)^{-1}$) and could assumed negligible [25, 82, 83]. For non-passivated surfaces with native spontaneous oxide, the trap density is very high ($D_{it2} > 10^{13} (cm^2 eV)^{-1}$) [83], and the top-surface electric field must be taken into account together with the correspondent interface trap density D_{it2} [82]:

$$V_T = \Phi_{fb} + 2\phi_F \left(1 + \frac{qD_{it1}}{C_{BOX}} + \frac{C_{Si} q D_{it2}}{C_{BOX}(C_{Si} + qD_{it2})} \right) \tag{2.32}$$

Experimental implications of this behavior in pseudo-MOS devices are shown in Figure 2.14.

In Chapter 3, a detailed study of the location of the oxide traps in bare SOI wafers and their impact on the performance of the device is carried out.

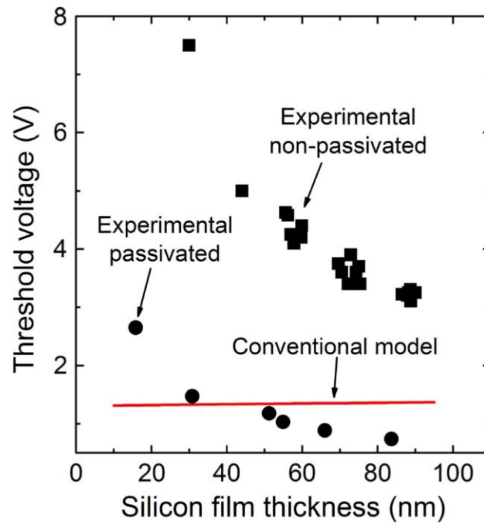

Figure 2.14: Comparison between experimental values of threshold voltage in (circles) passivated and (squares) nonpassivated samples and the conventional pseudo-MOSFET model. Reproduced from [82].

2.3 SOI transistors

Regarding reliability studies, not only the characterization of SOI substrates is interesting, but also a device-level study is mandatory. Therefore, electrical characterization of processed SOI transistors, specifically FD-SOI transistors, is carried out. As mentioned in Chapter 1, fully-depleted SOI (FD-SOI) technology offers excellent electrostatic control, which translates in a better scalability and performance, from low-power to high-speed applications. In planar SOI MOSFETs with thin buried oxide and ground-plane (GP), the GP biasing is an effective option for boosting the device performance. The GP is tuned to adjust the threshold voltage in OFF and ON states. From a reliability characterization point of view, instabilities on drain current-gate bias, drain current-drain bias and drain current-time characteristics are important. From these measurements, the majority of the transistor electrical parameters such as threshold voltage, saturation current, subthreshold current or current instability, can be extracted. In order to carry out these experiments in present CMOS technologies, especial equipment is required because of the tiny dimensions of transistor features and the fact that in most of

the cases transistors are fabricated on wafers without encapsulation.

2.3.1 Quasi-static characteristics

At least, two items of equipment are mandatory in the electrical characterization of on-wafer fully processed transistors. On the one hand, a semiconductor analyzer is required to apply and measure the corresponding current or voltage in the transistor terminals. In this PhD thesis, two commercial systems have been used: the Agilent B1500 and Keithley 4200-SCS. These analyzers allow the characterization of the current and voltage of the transistor terminals while voltage or current are established in their terminals through source-measure-units (SMUs). From these experiments, other extraction techniques based on current or voltage measurement as a function of time, capacitance-voltage, pulsed and transient measurements can be carried out. Figure 2.15 shows an illustration of one of the semiconductor analyzers where some of its features are summarized.

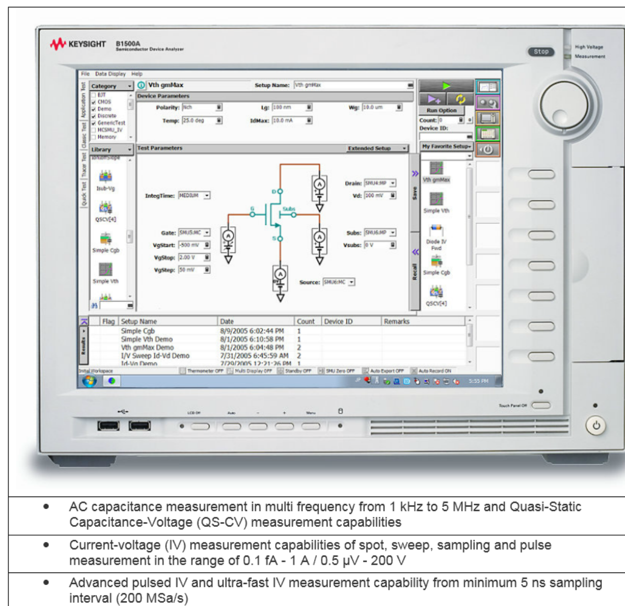

Figure 2.15: Front view of the semiconductor parametric analyzer Agilent B1500 showing a generic test in a four-terminal transistor. The main properties are summarized at the bottom.

On the other hand, a probe station is required in order to place the wafer on a platter and to select the transistor to be characterized. Once the transistor is located, metallic probes are adjusted through micro-positioners to contact with the transistor pads. In this thesis, automatic probe stations from *Süss* vendor have been used. These stations allow the automatic programmed characterization of the transistors on the wafer as well as temperature control of the chuck and back-gate biasing. In Figure 2.16, an automatic probe station and the probe contacts on one device are shown.

Figure 2.16: (Left) Wafer is loaded in the automatic probe station. (Right) Golden electroplated probes contact with the pads of a transistor in the wafer.

2.3.1.1 Threshold voltage extraction

One of the most important parameters in the electrical characterization of the transistors is the threshold voltage: gate bias point at which the channel is filled with enough carriers to let an appreciable drain current flow. A commonly used mathematical definition of threshold voltage is that voltage for which the surface potential, Φ_s, in the semiconductor below the gate oxide is given by [84]:

$$\Phi_s = 2\Phi_F = \frac{2kT}{q} \ln\left(\frac{p}{n_i}\right) \approx \frac{2kT}{q} \ln\left(\frac{N_A}{n_i}\right) \tag{2.33}$$

where n_i is the intrinsic carrier concentration, p the density of holes and N_A p-type dopant concentration. This expression is for an n-channel MOSFET and it is based on equating the surface minority carrier density to the majority carrier

density in the neutral bulk. The threshold voltage for large-size n-channel devices on uniformly doped substrates without short-channel effects, previously described, is given by [25, 70]:

$$V_{TH} = \Phi_{FB} + (1 + \frac{C_{it}}{C_{OX}} 2\Phi_F) + \frac{\sqrt{4q\epsilon_{Si} N_A \Phi_F}}{C_{OX}}) \tag{2.34}$$

In this way, drain current can be expressed as:

$$Linear Region : I_{DS} = \frac{W}{L} \mu_n C_{OX} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{2.35}$$

$$Saturation : I_{DS} = \frac{W}{2L} \mu_n C_{OX} (V_{GS} - V_{TH})^2 (1 + \lambda (V_{DS} - V_{D-Sat})) \tag{2.36}$$

For the experimental extraction of the threshold voltage, several methods are used [25, 70]. However, in order to minimize the variability among results, only two of these methods will be used in the extraction of threshold voltage along this thesis: the constant drain current method and the second derivative method or transconductance derivative method.

The second derivative method provides a reliable and high accuracy extraction from the drain current-gate voltage characterization. Its origin can be understood by analyzing the ideal case of a MOSFET modeled with a simple level 1 SPICE model, where $I_{DS} = 0$ for $V_{GS} < V_{TH}$ and I_{DS} is proportional to the gate voltage applied for values over the threshold voltage, $V_{GS} > V_{TH}$. Using the previous simplified assumption, dI_{DS}/dV_{GS} becomes a step function, which is zero for $V_{GS} < V_{TH}$ and has a positive constant value for $V_{GS} > V_{TH}$. Therefore, the second derivative, $d^2 I_{DS}/dV_{GS}^2$ will tend to infinity at the voltage where the step takes place, $V_{GS} = V_{TH}$. However, for a real device the second derivative would not become infinite, but would instead exhibit a maximum at the threshold voltage. A practical example of the extraction of the threshold voltage is illustrated in Figure 2.17 where the normalized value of drain current, transconductance and transconductance derivative are plotted as a function of the gate voltage.

On the other hand, the constant drain current extraction technique [70] evaluates the threshold voltage as the gate to source voltage value, V_{GS}, corresponding to a given constant drain current, I_{DS}. A typical value for this constant drain current is $I_{DS} = I_0 = 0.1 \mu A$ for a device with 1 μm width and 1 μm long at a

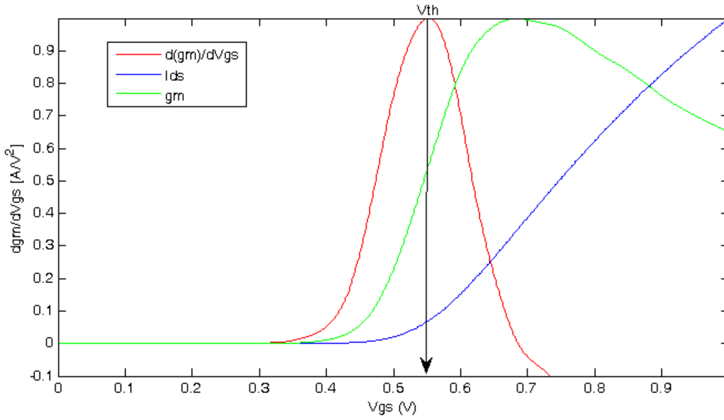

Figure 2.17: Example of threshold voltage extraction from experimental characterization of drain current-gate voltage using the transconductance derivative method.

constant drain bias of $V_{DS} = 50mV$. Since in most cases the size of the device under study will not fit these values, the reference current should be then scaled by using the expression:

$$I_{ref} = \frac{W}{L} I_0 = \frac{W}{L} 0.1 \mu A \tag{2.37}$$

This method presents two important advantages: it does not use any approximation, which makes it very favorable to study very little fluctuations on the threshold voltage more accurately and, in addition, the threshold voltage can be extracted very fast since this method does not require any special mathematical processing. Despite its simplicity, this method has the severe disadvantage of being totally dependent on the chosen value of the threshold drain current level I_0. An unappropriated selection of I_0 would result in a wrong threshold voltage determination.

2.3.1.2 Threshold voltage dependence on substrate bias

The threshold voltage of a bulk MOSFET is affected by the voltage which is applied to the back contact. The voltage difference between the source and the bulk, V_{BS} changes the width of the depletion layer and therefore the voltage across

the oxide due to the change of the charge in the depletion region. This results in a difference in threshold voltage which equals the difference in charge in the depletion region divided by the oxide capacitance, yielding:

$$\Delta V_{TH} = \frac{\sqrt{2\epsilon_s q N_A}}{C_{OX}} \left(\sqrt{(2\Phi_F + V_{SB}} - \sqrt{2\Phi_F} \right) \tag{2.38}$$

In SOI technology, electrical properties of transistors are typically influenced by the charge coupling between the front and back gates. In fact, the threshold voltage differs considerably from that of the bulk counterpart and depends on the bias and properties of the back gate. The analysis of this charge coupling between the front and back gates of the fully depleted SOI MOSFET was developed by Lim and Fossum in 1983 [85], and the analysis yields a description of threshold voltage (or front-threshold voltage, V_{Tf}), in terms, of the back-gate bias and the properties of the device, the back $Si - SiO_2$ interface, the fixed charge and fast surface-state densities.

When the back interface is depleted, i.e., the substrate voltage is higher than the one which establishes the interface in accumulation and lower than the one which makes the back interface in inversion. The threshold voltage in the transistor can be expressed as [85]:

$$V_{TH} = V_{TH}^{I} - \frac{C_{Si} C_{BOX}}{C_{of}(C_{Si} + C_{BOX} + C_{sb})} (V_{Sub} - V_{Sub}^{I}) \tag{2.39}$$

where C_{Si}, C_{BOX}, C_{of}, C_{sb} are the Silicon, BOX, front-gate oxide and fast surface-state capacitances respectively. V_{Sub} is the substrate voltage, V_{TH}^{I} is the threshold voltage of the BOX-Silicon junction approached by:

$$V_{TH}^{I} = V_{FB}^{f} + 2\Phi_B - \frac{Q_{Si}}{2C_{of}} \tag{2.40}$$

And V_{Sub}^{I} is the substrate voltage when the BOX-Silicon interface is in inversion and is given by:

$$V_{Sub}^{I} = V_{FB}^{b} + (1 + \frac{C_{sb}}{C_{BOX}}) 2\Phi_B - \frac{Q_{Si}}{2C_{BOX}} \tag{2.41}$$

where V_{FB}^{f} and V_{FB}^{b} are the flat-band voltage in front- and back-interfaces respectively and Φ_B is the surface potential in the inversion region.

When the back interface is in accumulation or inversion, the threshold voltage differs from the previously expression, however, in this thesis the substrate voltage used for the electrical characterization is inside these limits (back interface in depletion).

2.3.2 Noise characterization

In electronic devices, noise appears as fluctuations in the voltage or current signals caused either by external sources or by fundamental physical processes. Noise is a stochastic time signal and unpredictable in time domain, therefore it is necessary to use statistical descriptions and methods to analyze the behavior of those signals.

Noise signals are characterized through analysis of signals in time domain ($I_D - t$, $V_D - t$, $V_G - t$, etc.) and by the current power spectrum density in frequency domain. The experimental setup used to characterize noise spectrum consists, initially, in biasing the transistor with a fixed voltage in drain, source, substrate and gate terminals. Then, the current signal is measured periodically and transformed in voltage fluctuations with a low-noise I-V amplifier. Afterwards, these fluctuations are transformed into the spectral domain (Power Spectrum Density, PSD) through the Fast Fourier Transformation (FFT). Figure 2.18 shows a schematic of the experimental setup used for frequency noise characterization using a Synergie Concept noise analyzer.

Theoretically, three fundamental sources of noise are observed in MOSFET devices: thermal noise, flicker noise (or 1/f noise), and shot noise.

Thermal, *Johnson*, or white noise, is caused by the random thermal collision of the carriers with the crystal lattice in the semiconductor. This noise source was firstly measured by Johnson [86] and its noise power calculated by Nyquist [87]. The noise voltage mean square value is:

$$v_n^2 = \frac{4kTR\Delta f}{1 + (\omega\tau)^2} \approx 4kTR\Delta f \tag{2.42}$$

where Δf is the bandwidth of the measurement system, R is the equivalent resistance, and τ the carrier scattering time. For most practical frequencies, the second term in the denominator can be neglected and the thermal noise power is then frequency independent. Thermal noise exists in almost all electronic system.

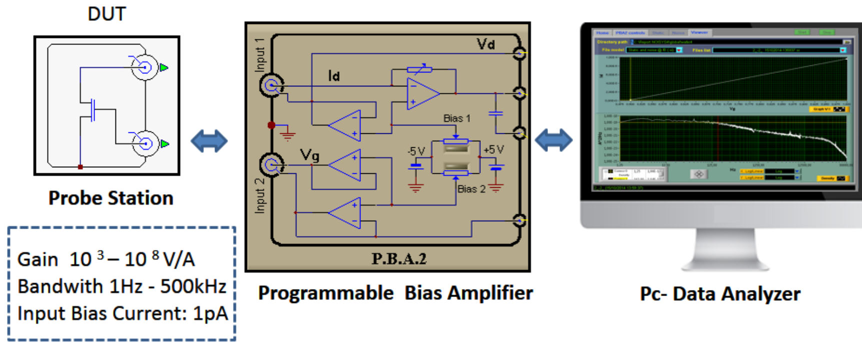

Figure 2.18: Schematic illustration of our experimental characterization setup of low-frequency noise in a transistor (device under test, DUT) by using a programmable bias amplifier and two PCs for data and result representation. The properties inside the square correspond to the Synergie Concept analyzer used in this thesis.

Sometimes the noise is expressed as the noise power spectral density:

$$S_v = 4kTR[V^2/Hz] \tag{2.43}$$

Shot noise is the second fundamental noise source and is due to the discrete nature of charge transport. It is usually observed in devices containing barriers such as *pn* junctions, Schottky diodes, etc. Schottky gave the first explanation of this type of noise in relation to vacuum tubes [88]. Its current mean square value is given by:

$$i_n^2 = 2qI_{dc}\Delta f \tag{2.44}$$

where I_{dc} is the dc current flowing through the device.

Flicker or low-frequency noise is associated with imperfections of the fabrication process and material defects and appears mostly at low frequency ranges. This kind of noise is observed under bias conditions in all semiconductor devices and the power density spectrum is characterized by a 1decade/1decade slope in the frequency domain. Although the physical origins are not totally clear, fluctuation of the number of carriers in the channel is the most probable cause [83, 89].

In Figure 2.19, an experimental low-frequency noise characterization of a SOI transistor is shown. A clear 1/f trend, i.e. 1 decade/1 decade slope, associated

with this kind of noise source is observed in the current power spectral density. This commonly trend observed in transistors was described by McWhorther [90], who attributed the source of 1/f noise to random trapping and detrapping events in charged traps near to the gate oxide. The mechanism is the carrier tunneling between the inversion channel and slow oxide traps N_{ot} located at the $Si - SiO_2$ interface.

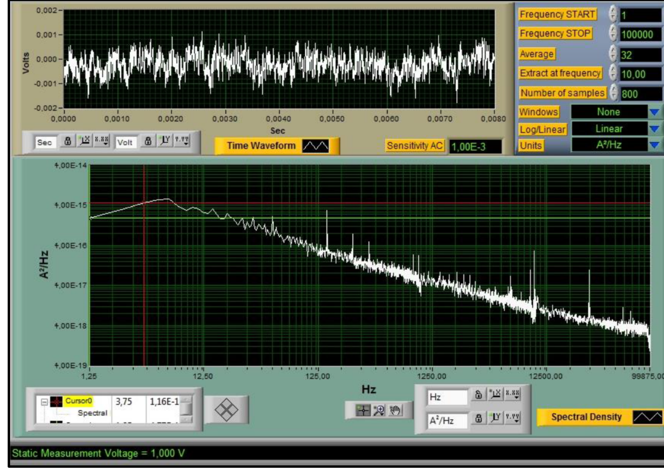

Figure 2.19: Spectral experimental characterization of current noise in a SOI transistor biased with 1V at the drain and gate terminals. At the top of the image, the voltage fluctuations at the output of the I/V amplifier in time domain are shown. At the bottom, the current power spectral density is plotted as a function of the frequency. Some experimental setup parameters appear in the top-right side.

An uniform distribution of the oxide traps N_t causes a time constant which leads to the 1/f (inverse frequency trend) spectral density characteristic. In this context, the power spectral density characteristic S_{VG} is given by the following equation [90, 91]:

$$S_{V_G} = \frac{q^2 N_{ot}}{LWC_{OX}^2 f} \tag{2.45}$$

being $N_{ot} = kTN_t\lambda_{OX}$ where N_t is the density of oxide traps per unit of volume and energy, λ is the McWhorther tunneling parameter (average tunneling length), f the frequency and the other symbols have their usual meaning described pre-

viously in this thesis. The concentration of slow traps, N_t, and interface traps, D_{it}, may be correlated by a first-order approximation $D_{it} \approx \lambda_{OX} N_t$ [25]. The equivalent drain current noise density S_{ID} can be expressed through the transconductance following the expression:

$$S_{I_D} = S_{V_G} \times g_m^2 \tag{2.46}$$

where g_m for a MOSFET in ohmic operation with constant effective mobility μ_0 can be expressed by:

$$g_m = \frac{WC_{OX}}{L} \frac{C_i}{(C_{OX} + C_d + C_{it} + C_{inv})} \mu_0 V_D \tag{2.47}$$

where C_{it} is the interface trap capacitance and C_{inv} the inversion layer capacitance.

The equivalent drain current power spectral density is obtained by combining the transconductance and current expressions of the transistors with Eq. 2.45, Eq. 2.47 and Eq. 2.46 [92, 93].

$$S_{ID} = \frac{q^2 \lambda_{OX} kTN_t}{L^3 W^{-1}} \frac{C_{inv}^2}{(C_{OX} + C_d + qD_{it} + C_{inv})^2} \mu_0^2 V_D^2 \frac{1}{f} \tag{2.48}$$

where C_{inv} can be expressed as $C_{inv} = (q/\alpha kT)Q_{inv}$, with $\alpha = 1$ in weak inversion and $\alpha = 2$ in strong inversion [25], and the drain current is equal to $(W/L)Q_{inv}\mu_0 V_D$. Thus the normalized current noise spectral density is given by:

$$\frac{S_{ID}}{I_D^2} = \frac{q^4 \lambda_{OX}}{\alpha^2 kTLW} \times \frac{N_t}{(C_{OX} + C_d + qD_{it} + C_{inv})^2} \frac{1}{f} \tag{2.49}$$

The advantage of the previous equation, also called Reimbold's equation, is to illustrate in detail the influence of the most significant device parameters, from weak inversion to strong inversion and from ohmic region to saturation region.

Moreover, other sources of noise like generation-recombination noise (G-R) must be taken into account. This noise is caused by the fluctuation of number of carriers due to random generation and recombination of electron-hole pairs [91]. In this case the noise is proportional to the square of the current:

$$S_I/I^2 = \frac{\overline{\Delta N^2}}{N^2} \times \frac{4\tau_r}{1 + 4\pi^2 \tau_r^2 f^2} \tag{2.50}$$

where τ_r is the carrier lifetime or trapping time constant. The variance $\overline{\Delta N^2}$ of the carrier number N is proportional to the concentration of generation-recombination-trapping centers and can explicitly be calculated; for example, for an accumulation or inversion thin-film layer, the G-R noise is given by [25]:

$$S_I/I^2 = \frac{q^2 f_t(1-f_t)N_s}{LWC_{OX}^2}\frac{gm^2}{I_D^2} \times \frac{4\tau_r}{1+4\pi^2\tau_r^2 f^2} \tag{2.51}$$

where N_s is the equivalent surface density of traps located at the Si film. The noise corresponds to a *Lorentzian spectrum* composed of a plateau at low frequency followed by a $1/f^2$ decrease. The measurement of the cutoff frequency (end of the plateau and beginning of the $1/f^2$ trend) provides the carrier lifetime τ_r. Similarity to G-R noise, Random Telegraph Noise (RTN) is attributed to individual carrier trapping and detrapping in oxide traps. The power spectral density of this noise, induced by single type of traps, is similar to that of the R-G noise: a plateau at low frequency followed by a $1/f^2$ decrease. An experimental result of the characterization is shown in Figure 2.20. However, when many traps with different time constants coexist, the superposition of their RTN signals results in a $1/f$ trend noise. An extensive study of this source of instability and its characterization is carried out it Chapter 4.

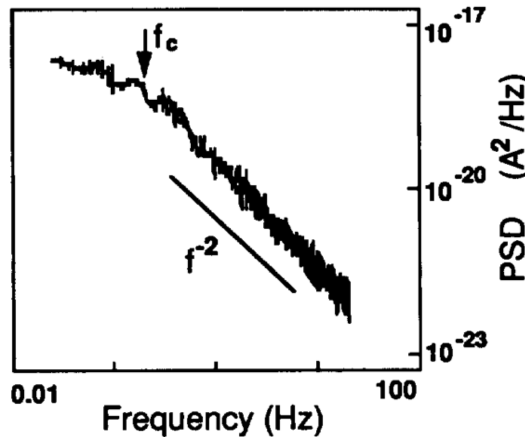

Figure 2.20: Experimental characterization of low-frequency noise in a device affected by Random Telegraph Noise. Reproduced from [94].

2.3.3 Over-the-wafer variability characterization

An important aspect regarding reliability issues is the variability of the device parameters all around the wafer, i.e. the shift of the electrical properties depending on the location of the device inside the wafer. Threshold voltage variability is one of the most important parameters after the fabrication process because influences the transistor (ON and OFF) state. As mentioned before, the possibility of automatic characterization allows the extraction of the electrical parameters, like the threshold voltage, for specific transistors for all the dies of the wafer.

Before the automatic electrical characterization, other aspects like wafer alignment, wafer profile, or thickness differences among dies, must be taken into account. The purpose of a wafer alignment is to position the wafer and to delimit each die in the wafer. Regarding the profiling, it establishes the surface planarity and thickness of the wafer on the platter. Wafer alignment and profiling are initially measured and stored. During the measurement, these data are used to move to the corresponding next transistor in a die-to-die stepping process. Usually, all these steps are carried out thanks to automatic probe station tools. In Figure 2.21 some parts of the process are shown.

Figure 2.21: (Left) Image of the alignment process in a wafer assisted by special marks (crosses and squares) patterned for this purpose. (Right) Scheme of the wafer where thickness relative differences among dies are labeled after the profiling process.

Automatic characterization opens up a world of possibilities for the statistical extraction of the electrical parameters of the devices on-wafer. It allows fast

characterization of big quantity of transistors. Some results are shown below to demonstrate the possibilities of automatic characterization (more extended results will be shown in the next chapters). For example, automatic threshold voltage extraction results are shown in Figure 2.22. This automatic characterization allows to study effects like the symmetry between source and drain bias configurations.

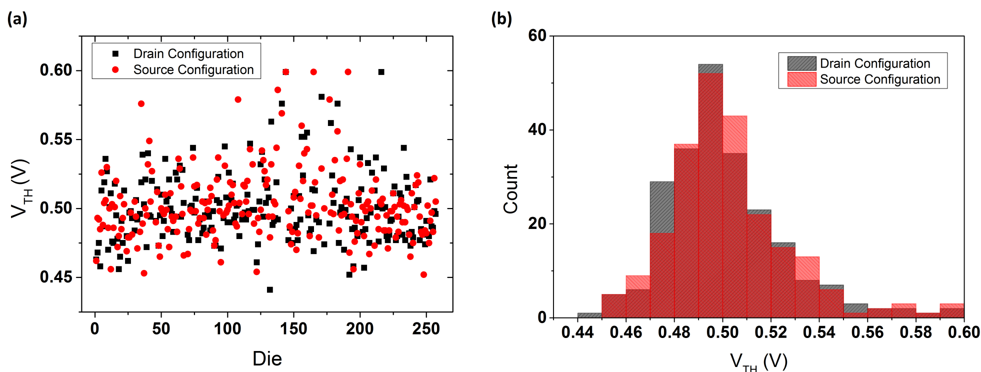

Figure 2.22: (a) V_{TH} extraction for 255 dies on the wafer when V_{DS} is biased through the drain (Drain configuration) and through the source (Source configuration). (b) Histogram of the threshold voltage as a function of the bias configuration (drain or source).

Another automatic characterization, usually carried out, is the extraction of current power spectral density for a specific transistor in all the dies of the wafer as is shown in Figure 2.23.

As expected, and the previous results well demonstrate, threshold voltage and power spectral density varies as a function of the device location over the wafer. In this context, and for on-wafer fabricated transistors, the knowledge of variability over the wafer is mandatory in order to establish the limitation in the operation of the devices (in the worst and the best cases).

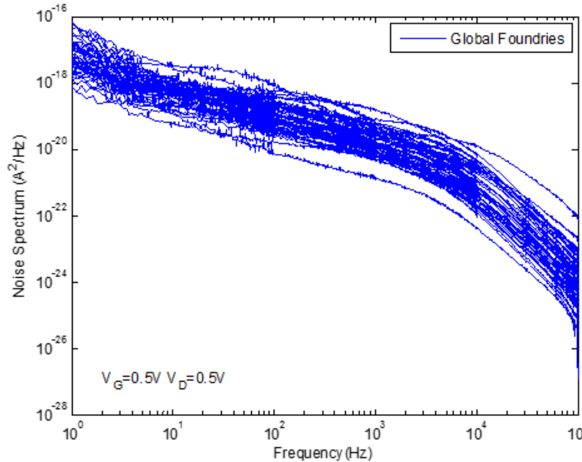

Figure 2.23: Current power spectral density of a specific transistor in several dies along the wafer. V_D=0.5V V_G=0.5V

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2.4 Conclusion

In this Chapter, the theoretical framework of the electrical parametric characterization and its experimental techniques, in bare substrates, SOI wafers and SOI transistors have been described. The methods for the characterization of resistivity and contact resistivity of devices have been detailed. In SOI wafers, the Pseudo-MOS experimental technique has been introduced, and the quasi-static characterization and oxide traps impact on the device behavior have been analyzed. The quasi-static characteristics, the threshold voltage extraction, and the substrate bias dependence in SOI processed transistors have been detailed from both theoretical and experimental points of view. The sources of noise in transistor together with the low-frequency noise characterization have been shown. Finally, brief description of automatic experimental measurements and their implications on variability and reliability issues have been explained.

Chapter 3

Bias Instability in Bare SOI Wafers

Bias Instability is a reliability issue affecting the electrical characteristics of a MOS transistor when the gate is stressed with relatively high voltage. In this chapter, the characterization of bias instability is carried out in bare SOI wafers using the Pseudo-MOSFET technique. The effect of positive and negative stress pulses on the properties of both hole and electron channels are systematically investigated using two different methods. The origin of the instability, the dependence of the degradation with time, and the recovery after the stress are discussed.

3.1 Introduction

The reliability of CMOS circuits can be severely limited by bias instability effects, which reflects the oxide and interface degradation during operation at high (positive or negative) gate voltage [41]. Bias instability can be a source of device malfunctioning after some period of correct operation. Although the exact root causes of the degradation are not yet well understood [95], as a result of aggressive scaling of MOS transistors, bias instabilities have reached more importance. In SOI devices, not only the front-gate oxide but also the Buried OXide (BOX), can be affected by BI. Such BOX degradation may happen when the substrate or back-plane are biased for threshold voltage (V_{TH}) tuning, multiple channel operation or electric field suppression [96–99].

3.1.1 MOSFETs bias temperature instabilities

By definition, bias temperature instabilities (BTI) are observed when the transistor is stressed at relatively high temperature (typically 80-100 °C) under a high constant gate voltage. These instabilities imply a reduction in the saturated drain current, a shift in the threshold voltage and an increase in the S/D series resistance [40]. An illustrative case of electrical parameters degradation after stress is shown in Figure 3.1. The instabilities are observed in most of the configurations, for either p-MOSFETs or n-MOSFETs, and whatever a negative bias and positive bias is applied. However, the most critical case occurs under a negative bias in p-MOSFET [40].

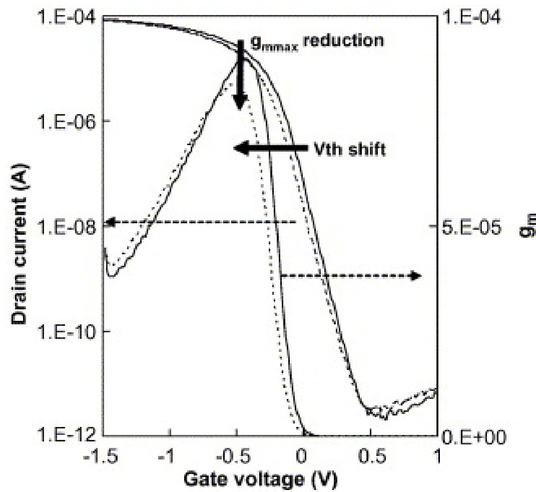

Figure 3.1: Drain current and transconductance curves as a function of the gate voltage for a 2nm-thick oxide p-MOSFET transistor before (line) and after 10,000 seconds of stress at 398 K (dashed line). Figure reproduced from [40].

Despite the microscopic details of the degradation are not fully understood, there is a general agreement stablishing that the generation of traps at the Si-oxide interface is the main cause of the degradation. Inside this agreement, a widely extended theory considers that due to the lattice mismatch between the silicon channel and the SiO_2 oxide, some Si atoms at the interface are left unbound. These trivalent Si atoms have an unpaired valence electron in a dangling orbital (dangling bond) which can be occupied by electrons. During the fabrication process, these dangling bonds are generally annealed by hydrogen atoms, creating

SiH bonds at the interface. However, it is demonstrated that under stress bias and high temperature conditions during a substantial time, these bonds might be broken leading a diffusion of the hydrogen atoms (H_2) and an increase in the number of traps as is shown in Figure 3.2 [40, 97, 98].

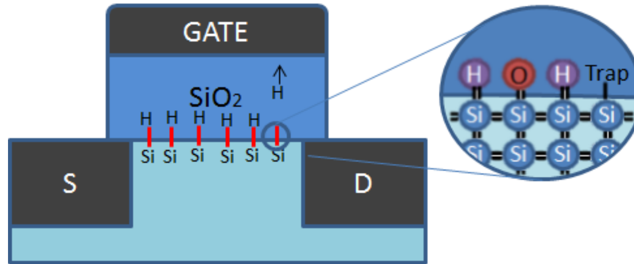

Figure 3.2: Schematic illustration of the interface between the silicon channel and the gate SiO_2 oxide. Despite the fact that traps are annealed by hydrogen atoms, during a stress period some hydrogen atoms might diffuse generating these traps again.

Additionally, it has been observed that a thermal annealing process in an hydrogen atmosphere also leads to generation of a mobile charge in oxide [100]. These mobile charge is identified as protons (H^+ ions), which can move from one Si-oxide interface to the other as a function of the sign of the applied voltage [101]. An example is shown in Figure 3.3, where the positive bias applied on the gate repels the positively charged ions and drives them to the oxide-silicon interface. The positive ions attract electrons in the silicon to the interface, reducing the threshold voltage of the transistor.

Apart from the interface charge generated after the hydrogen diffusion (Q_{it}) and the mobile charge in oxide (Q_m) previously mentioned, other types of charge should be taken into consideration: fixed oxide charge and oxide trapped charge. Fixed oxide charge, Q_f, is associated with the incompletely oxidized Si atoms at the interface. Oxide trapped charge, Q_{ot} is referred to the charge between Si-O-Si bonds in the oxide, usually caused by ion implantation. In any case, mobile charge, interface trapped charge, or even fixed charge introduced during fabrication process, imply a variation in the flat-band voltage as it was detailed in Chapter 2, Section 2.2.2). Subsequently, the variation of the flat-band voltage, caused by the change in the oxide charge, is translated into shift in the threshold voltage of the device.

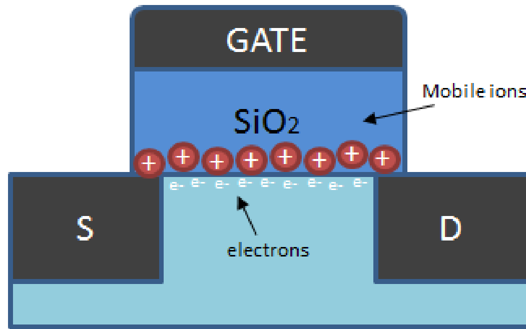

Figure 3.3: Schematic cross-section of an N-channel transistor with mobile oxide charge at the Oxide-Si interface. A movement of the positive ions and channel charge when a positive voltage is applied in the gate terminal is a source of instability.

To sum up, the following statements summarize the main characteristics of temperature bias instability (especially NBTI) in MOSFET transistor:

- The generation of interface traps, and subsequently the threshold voltage shift, follows a t^n power-law time dependence, where n is usually in the range from 0.17 to 0.3 [95].

- Despite bias temperature instability is a temperature-activated process involving generation of interface traps, bias instability may also be observed at room temperature [100, 101].

- A recovery of the degradation is observed after the stress conditions relax.

- The degradation is amplified under the presence of water, boron or nitrogen species near the Si-oxide interface.

The power-law degradation trend is extracted from the reaction-diffusion model (RD) and usually associated to the generation of traps at the silicon-oxide interface. RD model predicts the diffusion of molecular hydrogen and therefore the increase in the number of interface traps [102]. According to this model, the different experimentally extracted factors n depend on the stress time and on the nature of the diffused species, as is shown in Figure 3.4 [103]. However, other factors like the nature of oxide material or preexisting oxide and bulk traps, among others, can also alter the tendency [104]. In fact, a revised versions of the model

taking into account interface traps, hole trapping or temperature have been proposed [41, 104, 105].

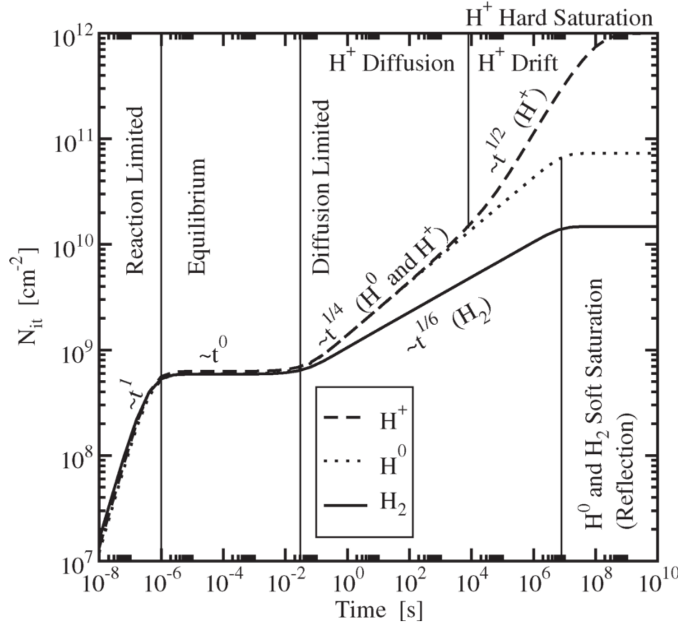

Figure 3.4: Schematic ilustration of RD model divided in five regions with different time behaviors and diffusion species. Reproduced from [103].

3.1.2 Recovery effect

After the degradation, it has been demonstrated that applying a voltage of inverse sign, opposite to that applied during the stress period, neutralizes, at least partially, the voltage shift induced. Some studies suggest the repassivization of the Si dangling bonds as possible cause of the neutralization [40, 41, 95]. This result implies that special attention should be taken during the characterization experiments, because delay between stress and measuring periods might cause neutralization of the degradation and erroneous results. For this reason, two different characterization methods will be used in this work: stress-measure-stress (SMS) and on-the-fly (OTF) techniques.

3.1.3 Motivation and wafer approach

In order to shed some light into the bias instability origins, initially, the bias instability effects appearing in bare SOI wafers, before any CMOS treatment, have been explored. Despite BI effects have been widely studied in fully processed MOSFETs, it is not common to explore this issue on bare substrates. The advantage of doing that is to monitor the BOX reliability in view of the fast optimization of the technology without need of long and costly CMOS processing of test devices. For the experiments, the transistor structure is emulated by placing two pressure-adjustable needles on the Si film acting as source and drain, whereas the substrate and BOX form the gate, Figure 5.5 (pseudo-MOSFET configuration, Chapter 2).

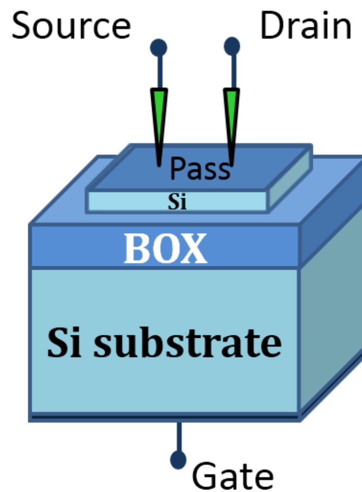

Figure 3.5: Pseudo-MOSFET configuration used for parameter extraction of SOI wafers: Two needles on the surface form source and drain terminals. The substrate and BOX act as the gate.

As mentioned in Section 2.2.1 of Chapter 2, capacitance-voltage characterization is an extended technique to extract the electrical parameter in pseudo-MOS structures. In this context, recent gate-to-channel capacitance measurements, based on this technique [106], have revealed a surprising threshold voltage shift (ΔV_{TH}) which occurs when the substrate bias is scanned slowly from negative to positive voltage (Figure 3.6).

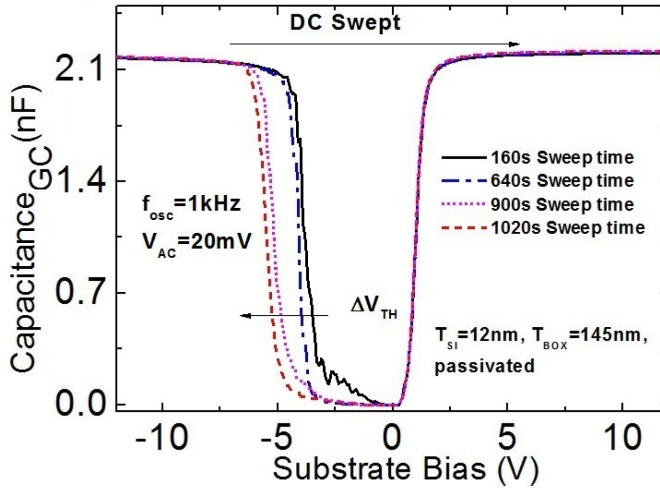

Figure 3.6: Threshold voltage shift appears in slow $C(V)$ measurements, especially in hole channels. f_{osc} is the oscillation frequency, V_{ac} the applied ac voltage and the sweep time corresponds to the duration of the measurement. More time yields more degradation in the threshold voltage.

By contrast, typical fast current-voltage characteristics obtained by the Pseudo-MOSFET have never shown any measurement-induced V_{TH} shift [80]. This shift suggests that the BOX may suffer from BI effects, resulting from the much slower voltage scan rate during capacitance experiments. We investigate the BOX instability by carrying out systematic measurements under stress conditions on bare SOI wafers with different physical characteristics.

In this chapter, Section 3.2 describes the methodology and the experimental setup: Measure-Stress-Measure (MSM) and On-The-Fly (OTF) methods are used for the electrical characterization of bias instability in bare SOI wafer. In Section 3.3, the effect of positive and negative stress pulses on the properties of both hole and electron channels are systematically investigated. The threshold voltage shift is demonstrated and modeled. The recover effect is pointed out by using the OTF characterization method in Subsection 3.3.2. Finally, the effect of the wafer surface preparation and the origin of the instability is discussed in Subsections 3.3.3 and 3.3.4.

3.2 Experimental methodology

Unibond™ un-doped wafers ($N_A \approx 10^{15} cm^{-3}$) with different film thicknesses (ranging from 12nm to 88nm) and 145nm-thick BOX are studied. MESA isolated silicon 1cm×1cm islands were etched and the surface was either passivated with 6-nm-thick SiO_2 or left unpassivated [83]. Tungsten-Carbide pressure-adjustable probes were used as source and drain electrodes for the Pseudo-MOSFET measurement configuration, Figure 3.7.

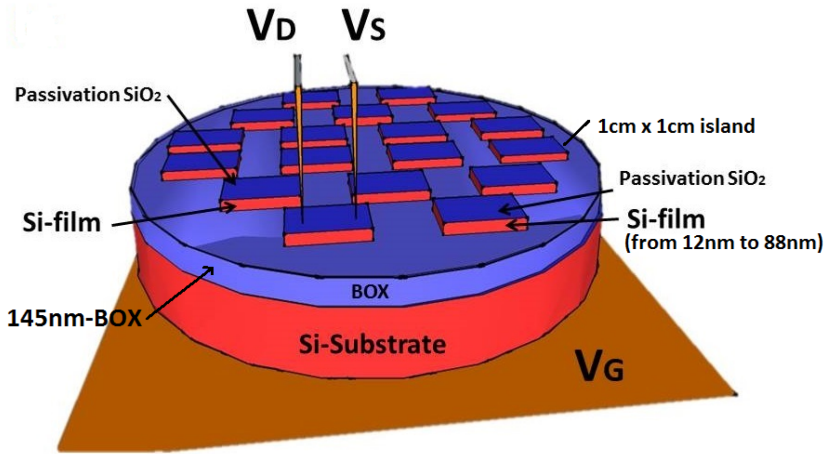

Figure 3.7: Schematic illustration of Unibond™ wafers used for the electrical characterization.

The degradation effects produced by the BI are characterized by the Measure-Stress-Measure method [41] (MSM) and the On-The-Fly method [40] (OTF):

In the MSM method (Figure 3.8), once the *fresh state* is characterized, a constant high voltage is applied to the wafer substrate (gate) while the drain and source contacts are grounded for stressing the device. After the stress period, V_G is ramped, while a low voltage is applied to the drain, to measure the $I_D(V_G)$ curve. The amount of degradation produced during the stress time is determined by, for example, calculating the threshold voltage shift with regard to the threshold voltage of the fresh device. A new stress period is then applied, followed by a new monitorization period (not shown in Figure 3.8). The method allows the characterization of negative and positive stress periods in n- and p-channel substrates

(only negative stress is shown in Figure 3.8). In all experiments, the electric field in the BOX was limited to ~4MV/cm to avoid hot carrier degradation [107, 108].

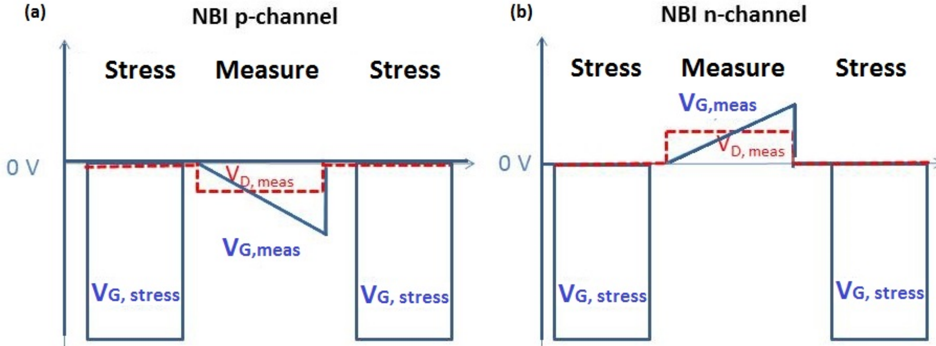

Figure 3.8: Illustration of MSM method for characterizing negative BI stress (NBI) in: (a) p-channels substrate and (b) n-channel substrate. Drain and source are grounded. During the measurement phase, the gate voltage is swept at a constant drain bias.

In the OTF method [40], the stress voltage is applied to the wafer substrate, the drain is biased at a constant voltage and the source is grounded. Intermittent, small variations in the stress voltage V_G are applied in order to obtain information about the transconductance (at the given stress V_G) through the variations of the drain current (Figure 3.9).

In On-The-Fly method, the V_{TH} shift can be obtained from the variation of drain current and transconductance. The transconductance of the Pseudo-MOSFET is given by [109]:

$$g_m = \frac{dI_D}{dV_G} = \frac{f_g C_{ox} \mu_0 V_D}{(1 + \theta(V_G - V_T))^2} \tag{3.1}$$

where f_g is the geometric coefficient [80], C_{ox} is the buried oxide capacitance, μ_0 is the low-field carrier mobility and θ is the mobility attenuation factor [109]. From a practical point of view, a trade-off must be achieved between the gate voltage step and the noise of the measurement for the numerical evaluation of Eq. 3.1. For the range of voltage applied to the 145nm-BOX wafers used in this work, a voltage $V_{Gsense} = \pm 0.1V$ provides the best compromise. The ratio between the drain current and the transconductance suppresses the influence of

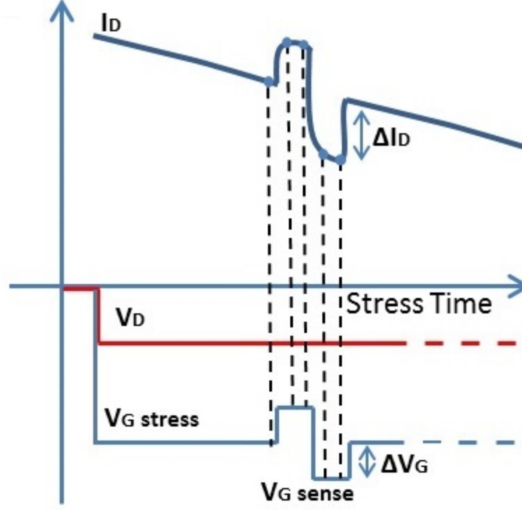

Figure 3.9: Illustration of OTF method for NBI in p-channel. During the negative gate bias stress, the drain bias is kept constant. Variations in the gate bias (V_{Gsense}) allow obtaining the transconductance and V_{TH} shift from the measured current.

the stress-induced mobility degradation.

$$\frac{I_D}{g_m} = (V_G - V_{TH})(1 + \theta(V_G - V_{TH})) \tag{3.2}$$

Assuming that θ is weakly dependent on the stress [40], the impact of the bias instability in Equation 3.2 falls only on the threshold voltage. The change in the current/transconductance ratio between the stressed and fresh state is given by:

$$\Delta(\frac{I_D}{g_m}) = \frac{I_{D1}}{g_{m1}} - \frac{I_{D0}}{g_{m0}} = \Delta V_{TH}(2\theta V_{TH_0} - 2\theta V_G - 1) + \theta \Delta V_{TH}^2 \tag{3.3}$$

where ΔV_{TH} is the shift in the threshold voltage from the initial state ($\Delta V_{TH} = V_{TH_1} - V_{TH_0}$). From Equation 3.3, the threshold voltage shift is found as:

$$\Delta V_{TH} = \frac{(1 + 2\theta V_G - 2\theta V_{TH_0})}{2\theta} - \frac{\sqrt{(2\theta V_{TH_0} - 2\theta V_G - 1)^2 + 4\theta \Delta \frac{I_D}{g_m}}}{2\theta} \tag{3.4}$$

Despite in other works the threshold voltage shift was calculated iteratively

[40], in this case, V_{TH} is extracted directly from Equation 3.4. Therefore, this method allows the extraction of the threshold voltage shift while the stress is being applied.

3.3 Results and discussion

A distinct advantage of using the Pseudo-MOSFET in BI tests is that both electron and hole channels can be probed in the same transistor-like structure just applying positive or negative bias to the substrate. A negative V_G stress injects positive charge (NBI) and a positive stress injects negative charge (PBI) into the oxide. The impact of these two types of charges on both channel polarities is probed in the very same sample.

3.3.1 BI measurements

The results for the case of Negative Bias Instability (NBI) stress are shown in Figure 3.10. The $I_D(V_G)$ characteristics for hole (Figure 3.10.a) and electron (Figure 3.10.b) channels are greatly modified using the MSM method. The curves are shifted in opposite directions for electron and hole channels, showing a significant increase of V_{TH} at room temperature.

In Figure 3.11, the case of Positive Bias Instability (PBI) stress for hole (Figure 3.11.a) and electron (Figure 3.11.b) channels is shown.

The absolute value of the V_{TH} shift, determined by the constant current method, is shown in Figure 3.12. The largest shift is observed in the NBI case for the hole channel where ΔV_{TH} can exceed 1V for 4000s stress. This result, namely the negative stress on p-channel presenting the worst instability effect, agrees with the previously mentioned BTI data reported in regular MOSFETs, [40, 41, 106].

From Figure 3.12, it is observable that the V_{TH} shift follows a well-defined power-law dependence, where the n factor depends on the channel type and the sign of the bias stress. This behavior has been attributed in the previous section to different degradations mechanisms. On one hand, the creation of interface traps and the diffusion of hydrogenated species after Si-H bonds were broken, leads to a t^n power-law (Hydrogen Reaction-Diffusion model). On the other hand, the carrier trapping and detrapping in oxide traps and mobile oxide charge also results in a power law with higher n value [110, 111]. Finally there are studies

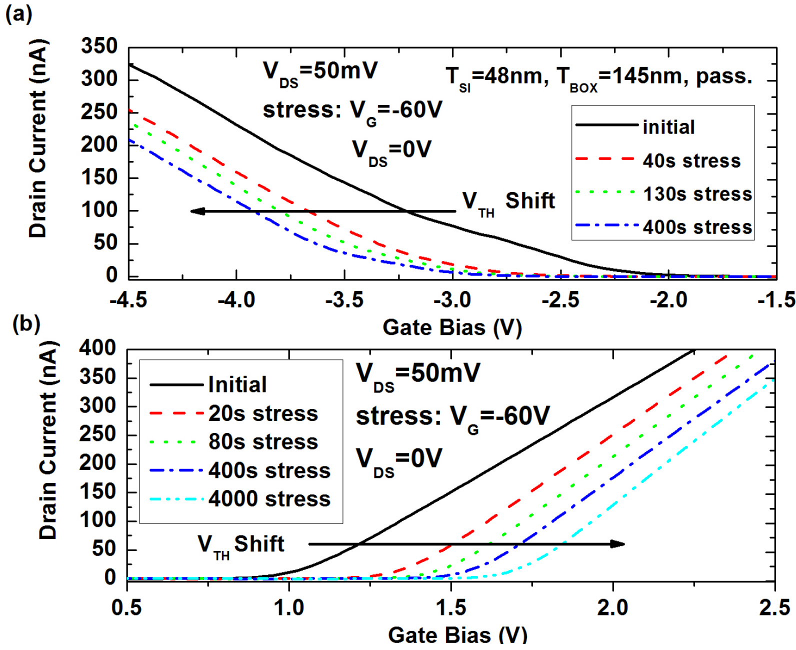

Figure 3.10: $I_D(V_G)$ characteristics showing, (a) significant negative V_{TH} shift in hole channel, and (b) positive V_{TH} shift in electron channel, after different stress times in NBI measurement conditions. Gate voltage during stress $V_{G,stress}$ = -60V, T_{Si}=48nm, T_{BOX}=145nm, passivated surface, 300 K.

attributing the BI to the sum of the two contributions [40,41,104,105]. In the case of our bare SOI wafers, the BI occurs at room temperature and relatively quickly compared to the thermally-activated BI (BTI) usually observed in processed MOS transistors. This result suggests the trapping and detrapping of carriers together with the movement of pre-existing mobile oxide charges as the main mechanisms causing the instability under the bias and temperature conditions considered in this chapter.

The application of stress voltages of increasing magnitude, *i.e.* higher vertical electric field, leads to larger BI degradation. Results for stress voltages of -12, -15 and -20 V ($E_{OX} \approx$ -0.83, -1.03 and -1.38 MV/cm) are shown in Figure 3.13. This electric field-dependent degradation has also been documented on fully processed MOSFETs [40, 41, 104].

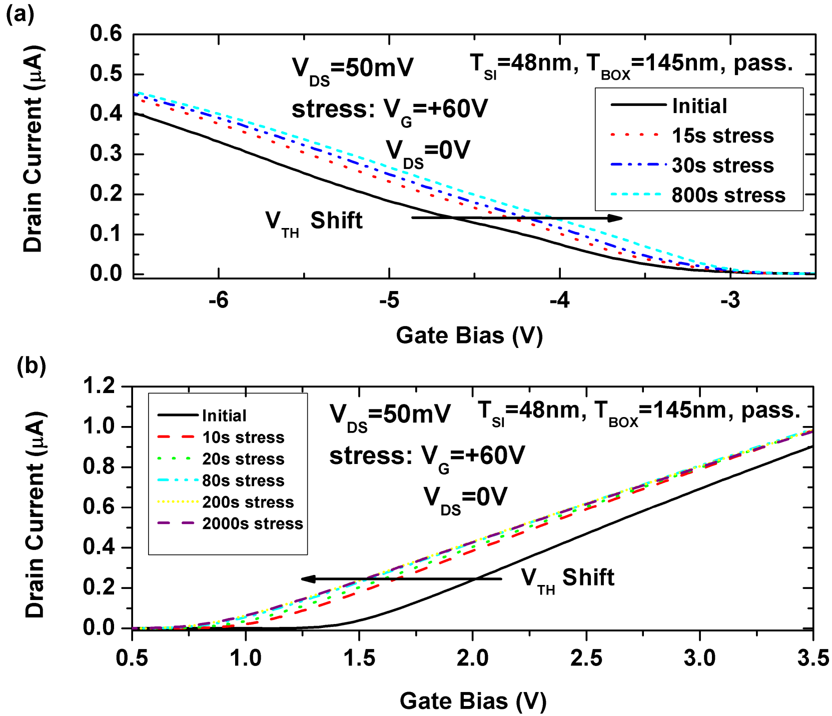

Figure 3.11: $I_D(V_G)$ characteristics showing, (a) significant positive V_{TH} shift in hole channel, and (b) negative V_{TH} shift in electron channel, after different stress times in PBI measurement conditions. Gate voltage during stress, $V_{G,stress}$, is 60V. T_{Si}=48nm, T_{BOX}=145nm, passivated surface, 300 K.

3.3.2 Recovery effects

It is known that NBI recovers after the stress is stopped, the amount of recovery depending on the sample under study [40, 41, 104, 105, 111]. Hence the MSM method can mask the actual degradation due to recovery during the measuring periods when the device is no longer under stress. The OTF method eliminates the neutralization effect and yields the actual V_{TH} degradation during the stress. In this case, the On-The-Fly characterization has been carried out by implementing the protocol described in the Section 3.2. Initially, the fresh characteristic of the device is measured obtaining some of the parameters as V_{TH_0} or Θ. After that, the device is subjected to the V_G stress. During the stress, each ten seconds period, a ΔV_G of $\pm 0.1V$ is induced and the current is simultaneously measured, as Figure 3.9 shows. By using Equation 3.4, threshold voltage shift is obtained. Figure 3.14

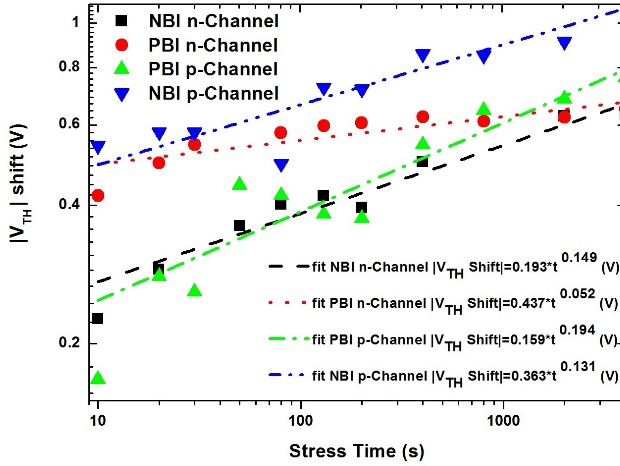

Figure 3.12: V_{TH} shift as a function of time after Negative or Positive BI in hole and electron channels. The stress bias applied to the gate is -60V for NBI and +60V for PBI. Logarithmic scale. The power law fitting is showed. The $I_D(V_G)$ characteristics, used for extracting the threshold voltage in the MSM method are obtained by sweeping the gate (substrate) from 0V to -20V for hole channels and from 0V to 20V for electron channels. $|V_{DS}|$=50mV, T_{Si}=48nm, T_{BOX}=145nm, passivated, 300 K.

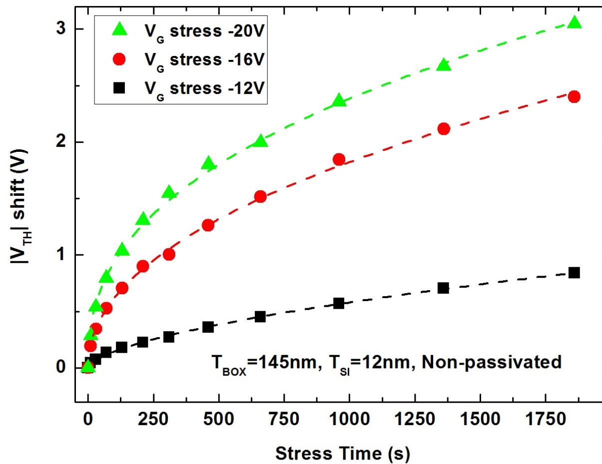

Figure 3.13: V_{TH} shift as a function of the stress time for three different stress voltages (symbols) and the corresponding fitting curves (dashed lines). Results obtained using the MSM method at room temperature. $|V_{DS}|$=50mV, T_{Si}=12nm, T_{BOX}=145nm, non-passivated surface.

shows the V_{TH} shift by using OTF method for the same device of Figure 3.13.

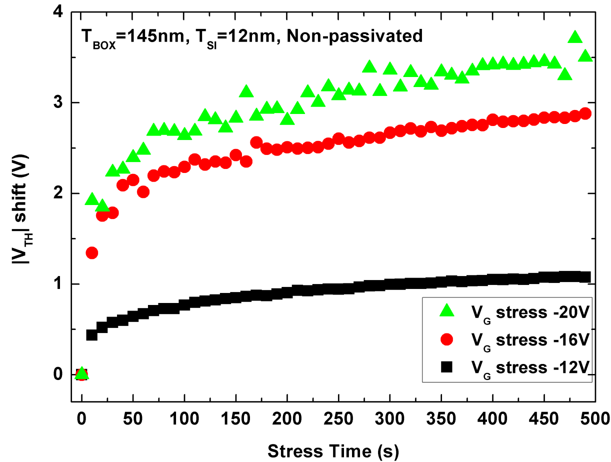

Figure 3.14: V_{TH} shift as a function of the stress time for three different stress voltages by using the OTF method at room temperature. $|V_{DS}|$=50mV, T_{Si}=12nm, T_{BOX}=145nm, non-passivated surface.

Figure 3.15 compares the V_{TH} shift using both methods, MSM and OTF. For the same stress voltage and time, the difference is significant. The OTF method produces a higher V_{TH} shift revealing the very fast recovery effect in the absence of stress.

Although the OTF method provides more accurate ΔV_{TH} results, due to the suppression of recovery periods, it does not allow characterizing accurately enough other parameters, such as mobility or transconductance degradation (OTF yields approximate values of transconductance at a given V_G and time of stress, but not the complete $g_m - V_G$ curves). Instead, the parameters can be monitored, with the MSM method. In Figure 3.16, an example of transconductance degradation is shown. Figure 3.17 shows the $\beta = f_g \Delta C_{ox} \Delta \mu_0$ parameter degradation with respect to the fresh state after stress periods with two different voltages.

Applying a positive gate bias after a negative bias stress neutralizes the degradation: the electrical parameters tend to recover the pre-stressed values, as shown in Figure 3.18. Earlier results have documented that the recovery of the initial parameters is a consequence of carrier trapping/detrapping in the oxide traps

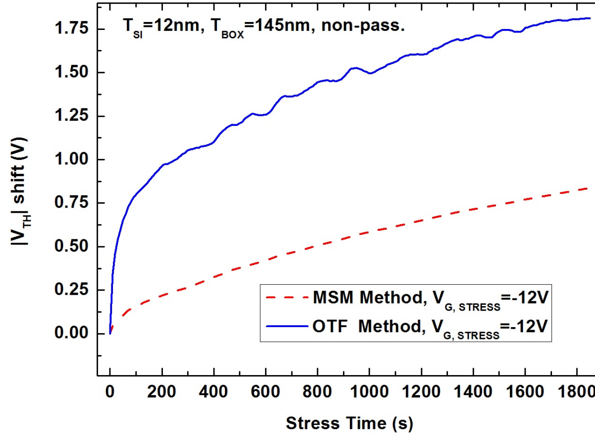

Figure 3.15: V_{TH} shift using On-The-Fly method (OTF) and Measure-Stress-Measure method (MSM). Non-passivated wafers, $|V_{DS}|$=50mV, T_{Si}=12nm, T_{BOX}=145nm, 300K.

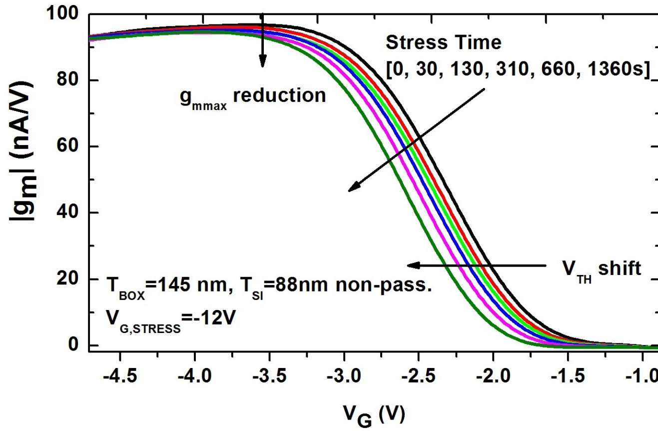

Figure 3.16: Transconductance measured on p-channel after NBI stress. T=300K.

whereas the contribution of newly generated interface traps subsists after the stress is removed [40, 41, 112–114]. According to these experiments, full recovery of V_{TH} is achieved after several hundred seconds of recovery pulse.

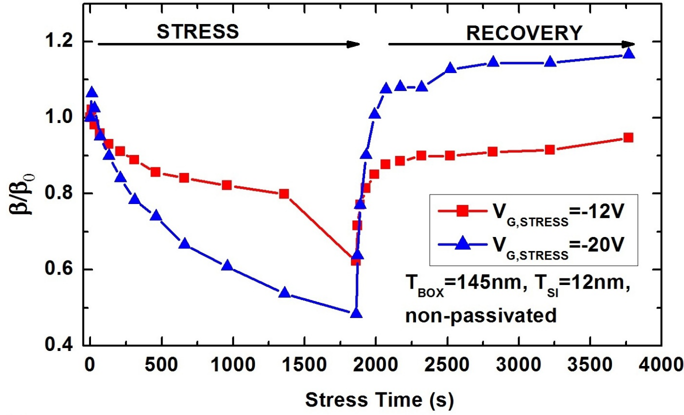

Figure 3.17: (a) β/β_0 ratio after stress as a function of time and recovery periods for two different stress biases. T=300K.

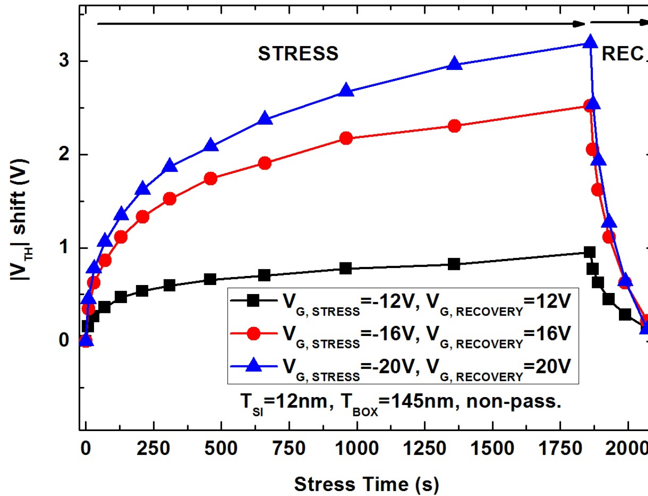

Figure 3.18: V_{TH} shift during the stress and the recovery period (REC period after 1860s of stress) for three different stress voltages using MSM method. During the recovery period the magnitude of gate voltage is the same than during the stress period but with opposite polarity. Measurements are performed at room temperature.

3.3.3 Impact of wafer surface preparation

In order to clarify the origins of the instability, wafers with variable Si-film thickness and with different top-surface oxide (passivated and non-passivated) were

characterized. These measurements reveal that the NBI increases as the Si-film thickness decreases (Figure 3.19.a). In addition, the magnitude of the V_{TH} shift is larger for the case of non-passivated than for passivated wafers (Figure 3.19.b). These results point out that the surface oxide is involved in the instability effect because the coupling between the top Si/SiO_2 interface and the channel increases in thinner and non-passivated films [82].

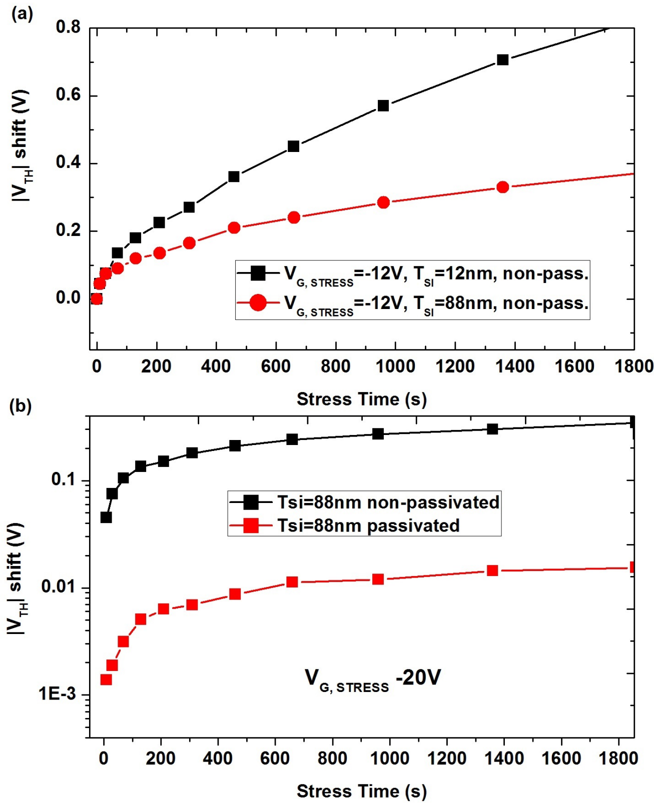

Figure 3.19: V_{TH} shift during NBI stress for hole channels, (a) for $V_{G,,stress}$= -12 V in two non-passivated wafers with different Si layer thickness and (b) for $V_{G,stress}$=-20 V in passivated and non-passivated wafers with same Si film thickness. $|V_{DS}|$=50mV, T_{BOX}=145nm, at room temperature.

One further evidence to dismiss the BOX as the main contributor to the bias instability effect is obtained by stressing the back channel of fully processed MOSFETs. 10μm×10μm transistors fabricated with the same SOI wafers were

measured [115]. Instead of using the top high-k metal gate to operate the device, the substrate and BOX serves as the gate (as in the Pseudo-MOSFET structure). Figure 3.20 shows the V_{TH} shift due to bias instability for bare SOI wafers with different thicknesses and surface qualities (passivated and non-passivated) as well as the results obtained for the fully processed MOSFETs. Only the case of NBI on p-channels is illustrated. The largest shift is obtained for the non-passivated wafer with the thinner SOI film followed by the same wafer with passivated surface. As the film gets thicker, the instability effect vanishes, being almost non-detectable for wafers with T_{Si}=88nm and passivated surface. In the case of the fully processed MOSFET (open symbols in Figure 3.20), there is no BI effect at room temperature.

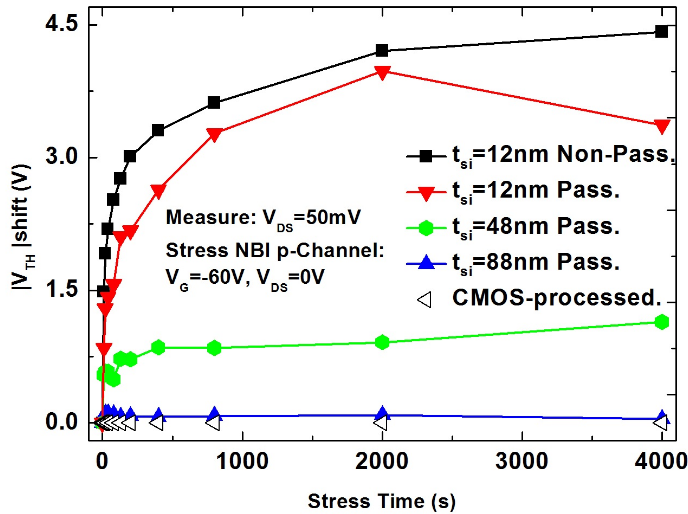

Figure 3.20: V_{TH} shift after NBI in hole channels. Comparison between bare SOI wafers with different Si layer thickness and a fully processed MOSFET wafer, $|V_{DS}|$=50mV, T_{BOX}=145nm, 300K.

3.3.4 Discussion

The results shown in Figure 3.20 discard reliability issues (at room temperature) of the BOX, exempting it as source of the instability. The largest shift obtained for the non-passivated wafer with the thinner SOI film points to the top interface as the region affected by the degradation. The trapping and de-trapping of carriers

in the top interface defects, together with the displacement of pre-existing charges in the low-quality native oxide are presumably the main mechanisms causing the bias instability at room temperature on bare SOI wafers. As a confirmation, in fully processed MOSFETs, where the top interface quality is properly controlled by the gate oxide, no BI effect was observed by stressing the back channel.

3.4 Conclusions

In this chapter, it has been demonstrated that Bias Instability tests can be conducted on bare SOI wafers by introducing a point-contact method. This technique has allowed to study both negative and positive bias stress in electron and hole channels. Negative bias instability is the predominant effect which can be neutralized after short recovery periods. The comparison of SOI wafers with different film thickness and surface quality, together with fully processed MOSFETs, points out that the instability is originated at the top surface of the wafer and not in the BOX. The fast V_{TH} shift at room temperature with very quick and full recovery, suggests that the traps at the Si-native oxide interface act as the main contributor to the instability effect.

From these results, it is possible to conclude that the V_{TH} shift observed when performing slow capacitance measurements using the Pseudo-MOSFET technique is originated by the quality of the top interface, being especially critical for the case of thin silicon films with non-passivated surface. In addiction, it is demonstrated in first instance, that the contribution of the BOX to bias instability at room temperature in state-of-the-art SOI transistors is negligible.

Chapter 4

Random Telegraph Noise in Fully-Depleted SOI MOSFETs

Random Telegraph Noise (RTN) has been studied in Ultra-Thin Fully-Depleted Silicon-On-Insulator transistors. A new protocol is introduced by combining the modified Time Lag Plot algorithm with the noise spectral density scanning characterization. The protocol allows to identify, unequivocally, the single-trap RTN signals in optimum bias conditions facilitating massive on-wafer characterization. The strength of the method is demonstrated by its application for monitoring the distribution of traps over the transistors of state-of-the-art processed SOI wafer. Additionally, the physical characteristics of the trap have been extracted based on Shockley-Read-Hall models, revealing the possible trends of capture and emission time of the trap according to its physical and energetic positions. The effect of the temperature on the characteristic times has been studied in the range from 248 to 323 K validating the results obtained at room temperature. Finally, the impact of substrate bias on the RTN fluctuation has been modeled through the Lim-Fossum interface coupling relationships, allowing to predict accurately the experimental results.

4.1 Introduction

RTN can be explained by the stochastic trapping/detrapping behavior of the channel carriers into the switching oxide traps (or border traps) in the gate di-

electrics. A trap in the oxide can occasionally capture a charge carrier from the channel, and the captured carrier can be emitted back to the channel after a period of time (Figure 4.1.a). The duration time of the captured and emitted states are denoted as τ_e (time between two consecutive emissions) and τ_c (time between to consecutive captures), respectively (Figure 4.1.b). In the time domain, V_{TH} shows a binary fluctuation caused by a single trap (Figure 4.1.c). In the frequency domain, as it is detailed in Section 2.3.2 of Chapter 2, the power spectral density (PSD) of the RTN-induced V_{TH} fluctuation shows a Lorentzian shaped spectrum with a plateau in low frequency and a slope of $(1/f^2)$ from the cutoff frequency (Figure 4.1.d).

Along the different technology generations, Random Telegraph Noise (RTN) has been a growing constrain paired with the reduction of the physical dimensions of the devices. The aggressive scaling of MOS transistors has decreased the current signals down to the level where they are not significantly higher than the fluctuations induced by carrier trapping phenomena [43]. This issue is particularly relevant in areas like the storage of information: it negatively impacts the noise margin in SRAM blocks [116, 117] as is shown in Figure 4.2.a, but also affects emerging devices like ReRAMs [118, 119] or Phase-Change Memories [120] where it becomes a crucial reliability problem. Moreover, in market extended applications like CMOS image sensors, the size reduction of the amplifier makes it more susceptible to RTN and can generate erroneous white spots in what should be dark areas, Figure 4.3.

Paired with the decrease of the signal levels, the adoption of new technologies such as high-k metal gate-stacks, ultrathin Silicon-On-Insulator (SOI) substrates or multiple-gate devices has not relaxed the RTN constrain, but even magnified it due to the increase of the number of interfaces combined with less optimized materials [50, 117]. In Figure 4.2.b, a clear increase of the threshold voltage shift when the technology area is decreased is shown. As Chapter 1 describes, the introduction of SOI technology has opened the path for the control of the threshold voltage of the transistors by using implanted ground plane or even its dynamic adjust through the substrate or back(-gate) bias [121, 122]. The impact of the back-bias on the electrical characteristics of the transistors has been extensively studied in the bibliography (threshold voltage: [85,123]; mobility: [124–126]), however there are few works addressing the effect of the back-bias on the noise char-

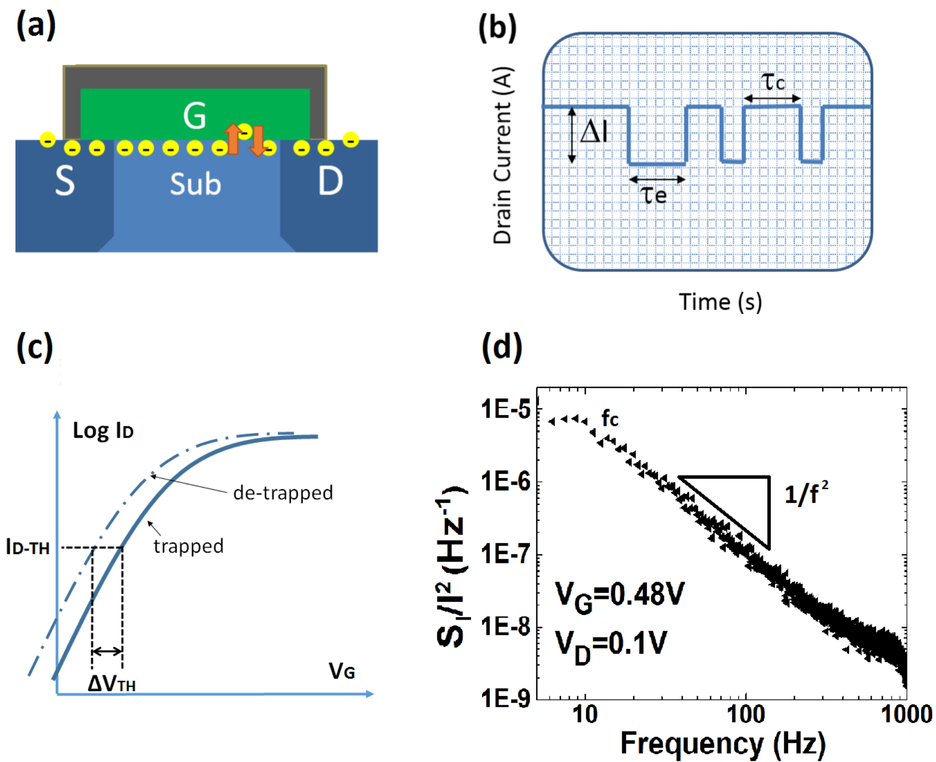

Figure 4.1: (a) Schematic illustration of a channel carrier trapped/detrapped by a trap in the gate oxide. (b) Trapping/detrapping events result in a two-level current characteristic where the capture and emission time are determined from the average high and low current levels respectively. (c) Threshold voltage shift observed between trapped (solid line) and detrapped (dashed line) carrier levels. (d) The power spectrum density (PSD) of the RTN fluctuation shows a Lorentzian shaped spectrum with a slope of $(1/f^2)$.

acteristics [127] and, in particular, there is a significant lack of results on the RTN characteristics in Fully-Depleted Silicon-On-Insulator transistors [128–130]. These new effects also require of powerful characterization tools to cope with the massive monitoring of the transistors over the wafer, aiming to extract useful statistical information to nourish the optimization of the fabrication process flows. The systematic characterization protocol that is proposed in this thesis allows the detection of transistors with a single active trap, identifying the best operation region to characterize the RTN signature. This method is based on

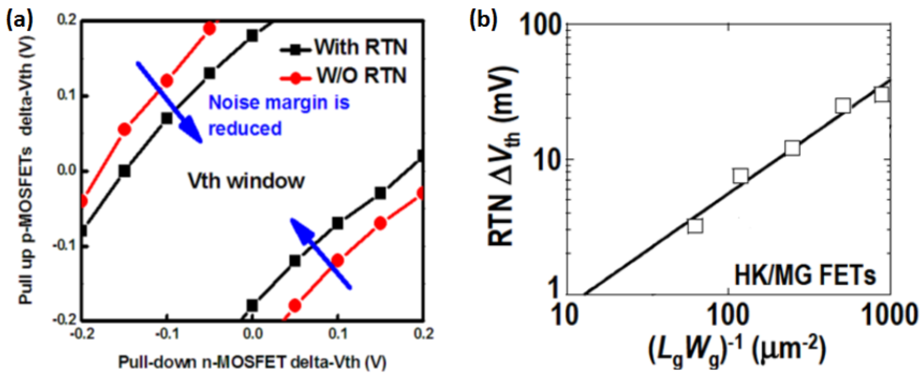

Figure 4.2: (a) Comparison of the noise margin in a SRAM memory when is (and not) affected by RTN. (b) Threshold voltage shift as a function of the inverse of the transistor area for HKMG MOSFETs. Reproduced from [117].

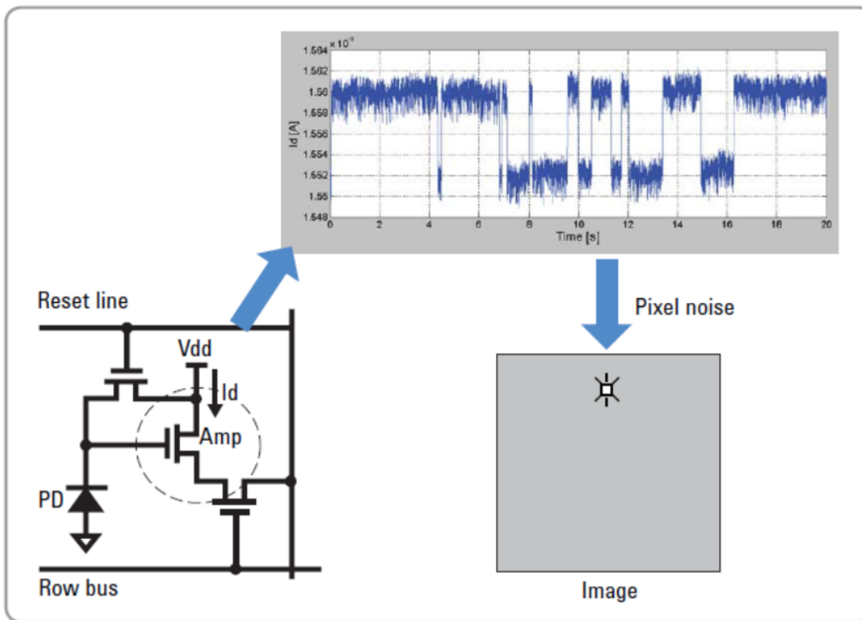

Figure 4.3: Schematic illustration of a CMOS image sensor. The scaling of the amplifier (bottom left) makes it more susceptible to RTN (top), generating erroneous white spots (bottom right). Reproduced from Agilent Report 2015.

the Spectral Scanning by Gate Bias (SSGB) combined with a modified Weighted Time-Lag-Plot (w-TLP) approach. The application of this new protocol allows an experimental study of RTN in single-trap transistors under an extended temperature range and back-bias operation.

In this chapter, Section 4.2 describes the methodology and the experimental setup: Subsection 4.2.1 introduces the Spectrum Scanning by Gate bias to easily trace the RTN in the time-domain, whereas in Subsection 4.2.2, the Weighted Time-Lag-Plot is applied to analyze the number of traps of the devices over the wafer. The RTN characterization technique, which implements both methods, is used to identify the transistors affected by a single-trap. Once single-trap devices are identified, a second selection process was carried out based on the physical location of the trap (Section 4.3). Only transistors with traps located near the source edge are retained. Inside this Section, the values of the characteristic capture and emission times are correlated with the physical position and activation energy of the trap. Section 4.4 is focused on the analysis of the dependence of the characteristic times with temperature. The back-bias influence on the capture and emission times is investigated and modelled in Section 4.5.

4.2 Methodology and experimental setup

FD-SOI MOS-transistors fabricated in a $22nm$ process at CEA-LETI [131, 132] have been used to obtain the experimental results. These Unibond^{TM} devices feature a hafnium based gate-stack ($1nm$ cap layer) with an equivalent oxide thickness $EOT = 1.3nm$, $7nm$-thick Si-film and a $145nm$-thick buried oxide (BOX). The gate length and width are of $100nm$ and $80nm$ respectively. The body of the transistors is non-intentionally doped. A TEM image of the devices is shown in Figure 4.4.

The experimental method is summarized in the schematic of Figure 4.5. At first, we characterize the low-frequency noise (LFN) of the device for different gate biases introducing the Spectral Scanning by Gate Bias approach. The output of this first stage, provides the optimum bias condition where the device is affected by RTN. Once the RTN signal is identified, the transient monitoring of the drain current, together with the application of the Weighted Time Lag Plot method, determine the number of active traps in the device. This selection of the suitable

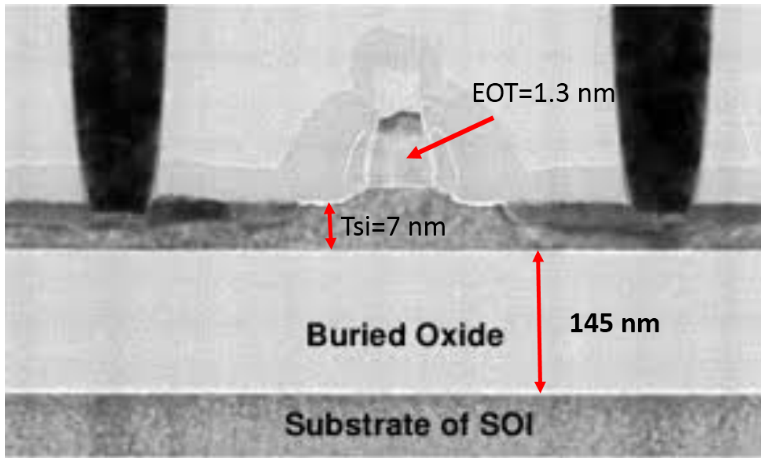

Figure 4.4: Cross-sectional TEM image of a FD-SOI transistor used for the electrical characterization of RTN.

bias condition and the single-trap device identification, permits to obtain the optimum RTN characterization of single-trap devices in an unambiguous protocol for the implementation in automatic testers.

All the experiments presented in this work are based on a direct on-wafer characterization carried out with an ad-hoc setup consisting of:

- An Agilent B1517A high resolution Source-Measurement-Unit (SMU) monitoring repeatedly the drain current during periods of $400s$ at a $2ms$ sampling-rate (the schematic is shown in Figure 4.6.a). The acquisition periods were repeated until a minimum number of 100 transitions in the current signal were captured to guarantee the significance of the statistics.

- A Süss PA-300PS semiautomatic probe station GPIB-controlled by the Agilent SMU. This tool allows the fast location and scanning of all the devices over the wafer to extract information about the distribution of traps and the variability.

- A low-noise current amplifier connected to a software-based spectrum analyzer through a high resolution A/D converter (Figure 4.6.b). The system is used for the noise spectral density monitoring.

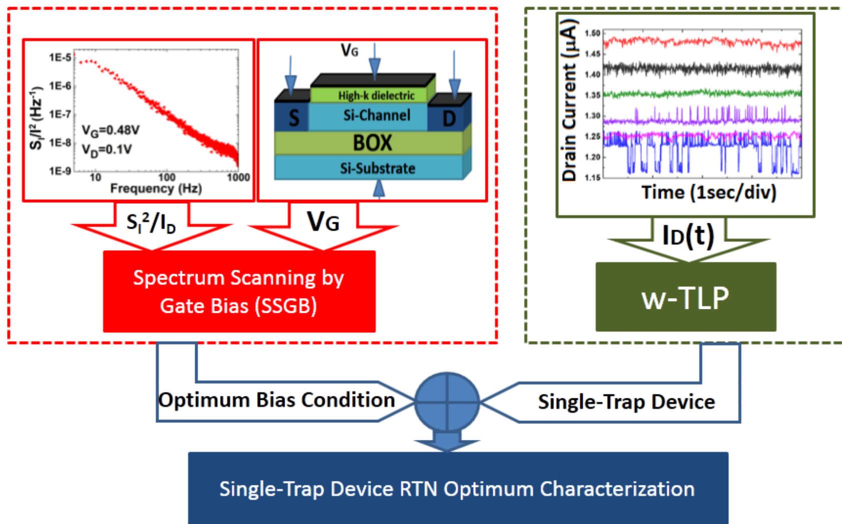

Figure 4.5: Scheme of the experimental method proposed for the single-trap random telegraph noise characterization in transistors. The method permits the optimum RTN characterization of single-trap devices combining the Spectral Scanning by Gate Bias technique and the Time Lag Plot method.

4.2.1 Determination of the optimum bias condition for the RTN apperance

The time-domain characterization of the electrical noise requires large time windows due to the extensive quantity of events needed to obtain meaningful statistics [133]. In addition, due to the dependence of the capture time (τ_c: average time at the high current level) and emission time (τ_e: average time at the low current level) of a trap with the carrier concentration of the channel [134], random telegraph noise is not easily observable in all the bias range of the transistor (see Figure 4.7). Therefore, RTN must be characterized at a bias point where the characteristic times, τ_e and τ_c, of the trap differ at most in three orders of magnitude. In this way, the transition events between states can be observed in a reasonable time-frame.

This task can be facilitated by the first method that we are introducing in this chapter: Spectral Scanning by Gate Bias (SSGB). Initially the spectral noise density of the drain current (S_I) is obtained for a given bias (preferentially close to the threshold voltage), Figure 4.8.a. The corner frequency of the noise spectrum is

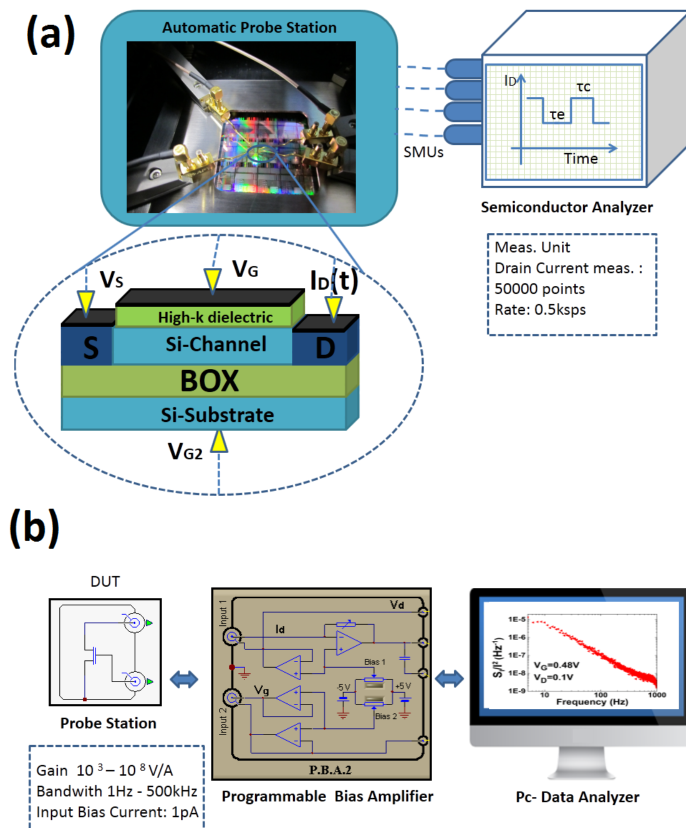

Figure 4.6: (a) Schematic of the experimental setup developed for the RTN measurements. Each terminal of the transistor is monitored by an Agilent B1517A SMU at a rate of 500 samples per second. Automatic measurements around the wafer are implemented through a Süss semiautomatic probe station. (b) Schematic of the measurement setup used to extract the spectral noise power of the drain current based on a programmable low-noise amplifier.

determined by the sum of the inverse of the characteristic times ($f_c = 1/\tau_e + 1/\tau_c$) [94] (Section 2.3.2, Chapter 2). Once the corner frequency is located ($f_c = 3.75Hz$ for the case of Figure 4.8.a), the spectral density of the current noise, S_I, is measured while V_G is swept leading to the $S_I - V_G$ curve shown in Figure 4.8.b (SSGB). The bell shaped characteristic of Figure 4.8.b identifies the bias range where the RTN will be easily observable (V_G ∈[0.4V, 0.55V] for this particular case). This result is consistent with the drain current signals shown in Figure 4.7,

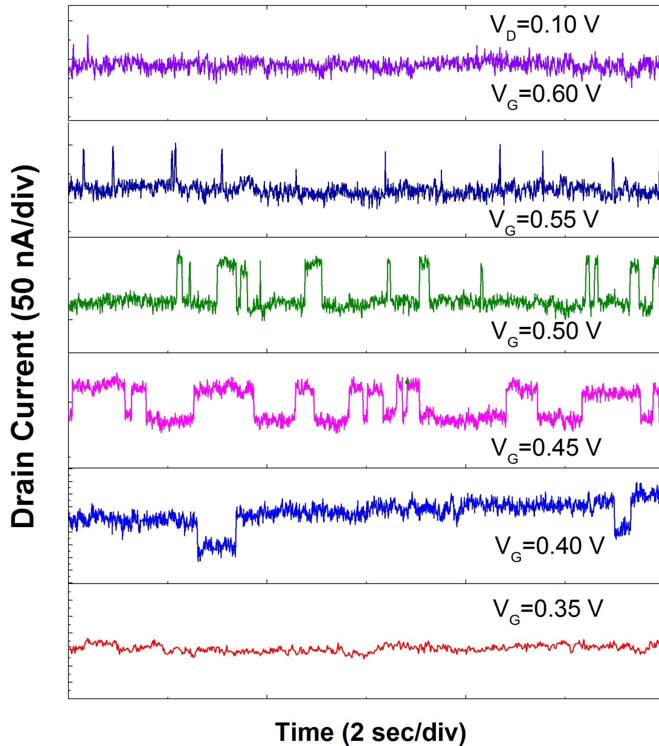

Figure 4.7: Drain current traces as a function of the time from a transistor affected by random telegraph noise for different gate voltages. (b) Normalized current noise power (S_I/I^2) dependence with frequency for different gate voltages (V_G). (c) Normalized current noise spectral density dependence with gate voltage (SSGB) for the transistor of figure (b).

where the fluctuations are visible in the same voltage range given by the SSGB plot of Figure 4.8.b.

4.2.2 Identifying the number of traps involved in the RTN signals

Once the bias range for the experiments is unequivocally determined, identifying the RTN signals corresponding to a single-trap is one of the most challenging tasks during its electrical characterization. Examples of the intricate drain current signature of multiple-trap RTN are shown in Figure 4.9. The current transients are obtained for different transistors for the same value of the gate bias.

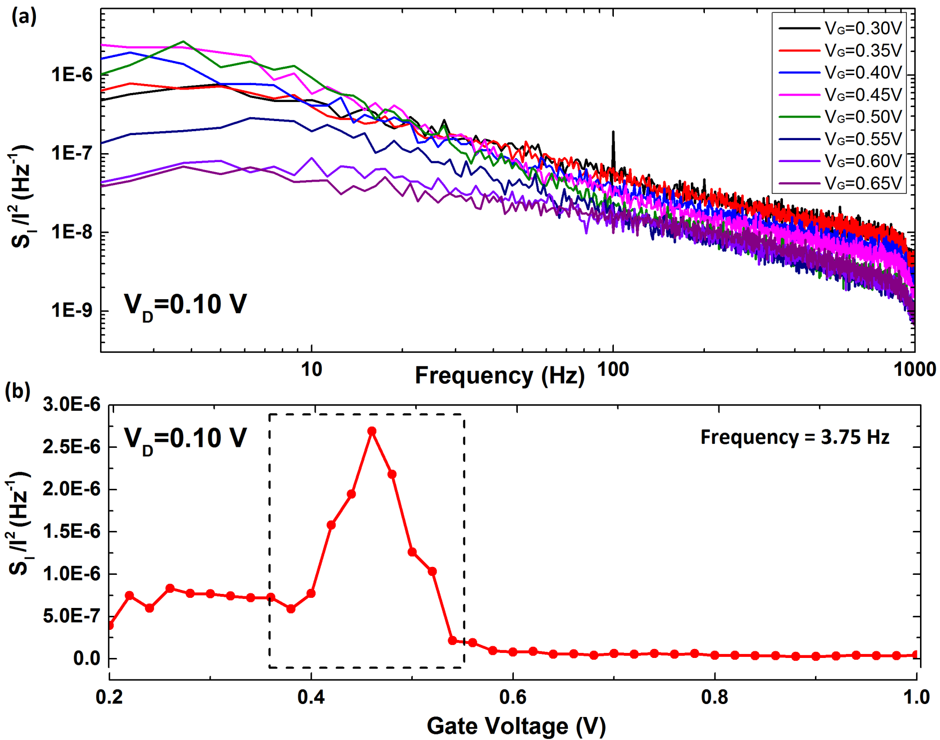

Figure 4.8: (a) Normalized current noise power (S_I/I^2) dependence with frequency for different gate voltages (V_G). (b) Normalized current noise spectral density dependence with gate voltage for the transistor of figure (a).

Despite it is difficult to discern the contribution of a single-trap from the time domain representation of Figure 4.9, this can be carried out unambiguously by a modified version of the Time Lag Plot method (TLP), partially based on the approach described in [135] and [136]. Each point of the TLP space (events) is given by the sample of the current at a specific moment, and the immediately next sample $((I_D(i), I_D(i+1)))$. Then, the TLP space event is weighted by the *appearance* function, $\mathcal{A}(I_D(i), I_D(i+1))$, which accounts for the number of events inside a certain circle of the TLP space and defined by:

$$\mathcal{A}(I_D(i), I_D(i+1)) = \sum_{j=1}^{N-1} \xi(I_D(j), I_D(j+1)) \tag{4.1}$$

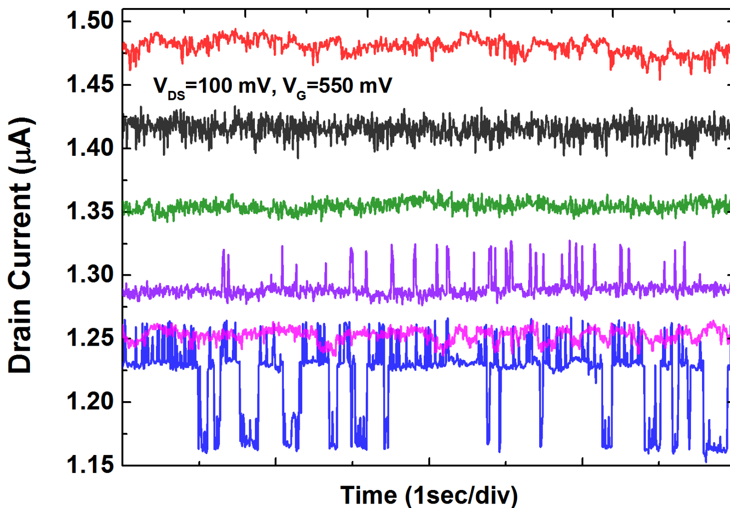

Figure 4.9: Drain current traces of different devices presenting multi-trap RTN.

where ξ is a function that eliminates the samples outside the appearance radius,

$$\xi(I_D(j), I_D(j+1)) =$$

$$= \begin{cases} 1 \text{ if } d\{[I_D(j), I_D(j+1)], [I_D(i), I_D(i+1)]\} \leq r \\ 0 \text{ if } d\{[I_D(j), I_D(j+1)], [I_D(i), I_D(i+1)]\} > r \end{cases} \tag{4.2}$$

N is the total number of samples inside the time frame analyzed; $d\{.,.\}$, is the Euclidean distance function; and r is the appearance radius, $r = 10^{-6}\sigma$ (A) (with σ the standard deviation of the samples within the time frame).

This sample-weighted approach of the conventional TLP method allows to identify the RTN levels clearly as populated regions in the diagonal of the TLP space, while populated regions outside the diagonal are related to the transitions between states. We show results of the application of the method in Figure 4.10. When the device is not affected by traps (Figure 4.10.a), a single cloud appears in the TLP space; the appearance of a constellation with two lobes indicates the presence of a single-trap (Figure 4.10.b); a three-lobes constellation, reveals the existence of three predominant current levels (two traps, Figure 4.10.c); and when multiple current levels appear, a spread lobe indicates a multi-trap situation (Figure 4.10.d).

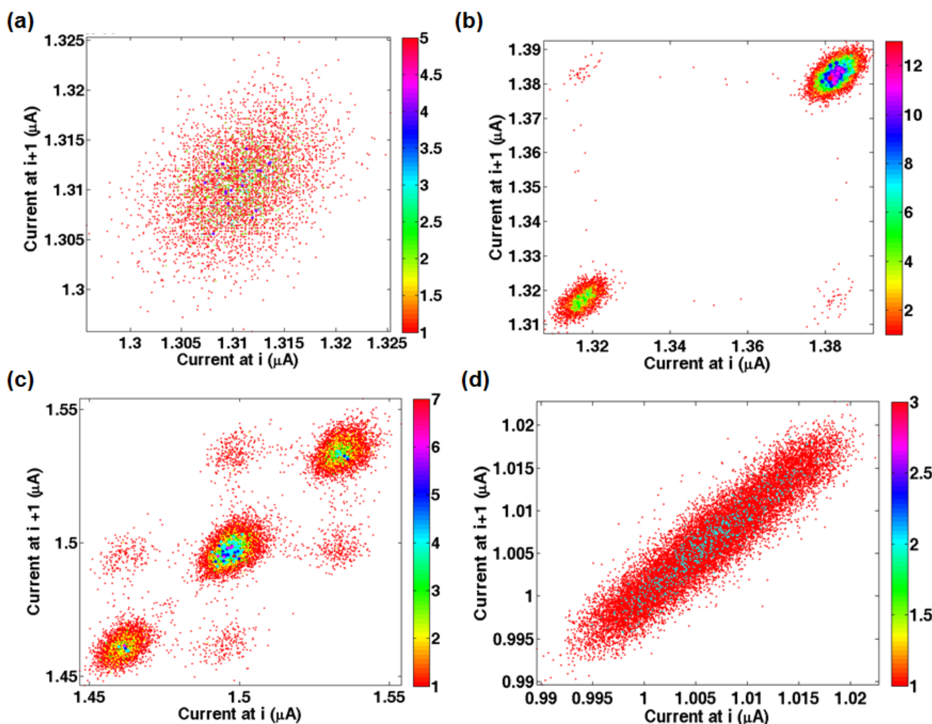

Figure 4.10: Traps constellations in the Weighted TLP space of drain current signals: (a) cloud: transistor lacking of RTN signature (only thermal noise is reflected). (b) Transistor with two lobes (states) in the TLP constellation result from the single active trap. (c) Transistor with a three-lobes constellation identifying the characteristic signature of two traps. (d) Spread cloud corresponding to a transistor with multi-trap events.

The strength of the method is fully exploited when it is combined with an automatic probe station. The distribution of traps over the transistors of the wafer can be determined by the automatic monitoring of the drain current of specific transistors and the simultaneous application of the w-TLP method described previously. Figure 4.11 shows the map of traps for a 100nm-length and 80nm-width transistor fabricated in each die of the wafer (336 transistors in total) when the bias point is close to the threshold voltage ($V_D = 0.1V$, $V_G = 0.5V$). The map represents the number of traps detected in each transistor: failed transistors, for which the automatic contact was missed or simply because they were faulty (black); transistors with only one drain current level, i.e. transistor without trap

(green); transistors with two current levels, i.e. single-trap devices (blue); transistors with three current levels, i.e. two-traps devices (red); and transistors with more than two active traps (pink). Examples of the current level for each type of transistor are shown in the annexed time domain representations of Figure 4.11.

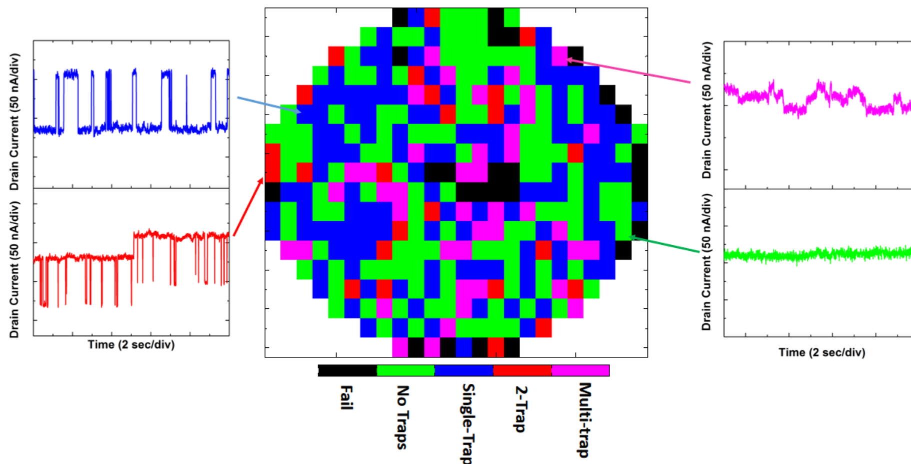

Figure 4.11: Distribution of the number of current levels detected in the transistors over the wafer at $V_D = 0.1V$ and $V_G = 0.5V$. (Left) Examples of transistors with two and three current levels (top and down respectively). (Right) Examples of multi-current level (> 3) and RTN-free transistors (top and down respectively).

Figure 4.12 presents the histogram summarizing the trap count over the wafer. From this result, and for the specific transistor studied (one $L = 80nm$, $W = 100nm$ transistor per die), we can conclude that one out of three of the transistors are affected by one trap, and virtually the same number of transistors are not affected by traps leading to RTN. The case of devices with three current levels, i.e. two traps, represents the 7.5% of the devices characterized on the wafer. Finally, the case of multi-trap devices (transistors with more of three current levels), involves 12.5% of the devices.

The previous result demonstrates the large presence of single-trap devices within this wafer run. This information constitutes an useful feedback for process engineers in the path of the optimization of the technology.

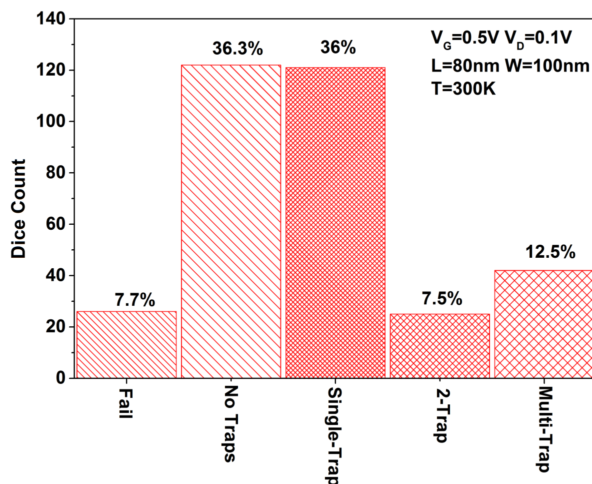

Figure 4.12: Histogram of the number of dice presenting a determined number of traps in the device under study detected from the RTN characterization ($L = 100nm$, $W = 80nm$, one transistor per die). Same bias than in Figure 4.11.

4.3 Determination of the trap location

Once single-trap devices are identified through the proposed protocol, the second selection applied to the transistors tries to avoid the dependence of the capture and emission time with the drain bias. This is an additional precaution to isolate the actual influence of the substrate bias on the characteristic times. The V_D independence can be evaluated by extracting τ_c and τ_e as a function of V_D (for a given V_G) and performing different bias configurations of the terminals. Some of the devices present a strong asymmetry in the values τ_c and τ_e when the roles of source and drain are exchanged as shown for the case presented in Figure 4.13.a. This asymmetry is consequence of the non-centered position of the trap along the length of the channel [137]. The trap is located close to the source in the case of Figure 4.13.a, while in the case of Figure 4.13.b, the symmetry shown reveals that the trap is near the center of the channel. The case of the trap close to the source, makes its characteristic times independent of the drain bias (if we wish to study the dependence of other effects, such as back-gate bias effect, any V_D influence on the RTN results should be avoided).

The impact of the drain bias on the amplitude of the RTN signals is underlined

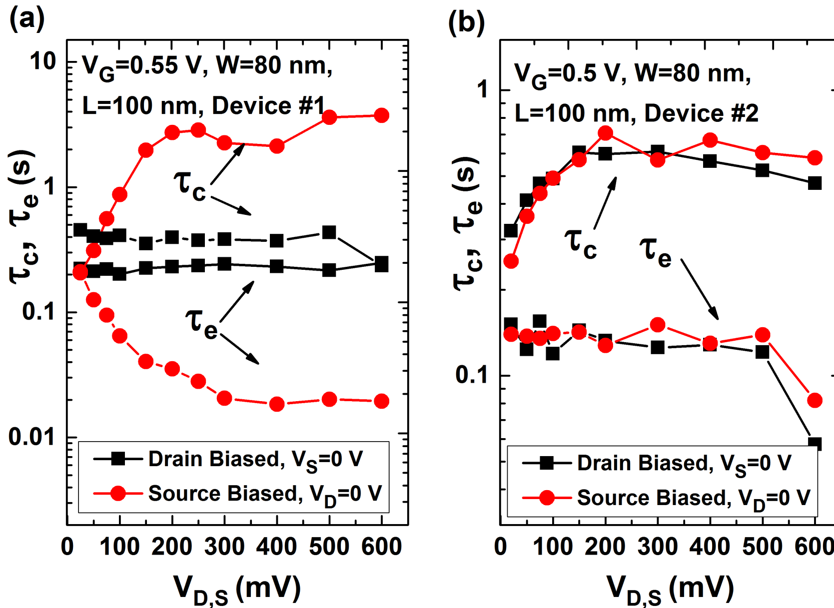

Figure 4.13: Capture and emission time dependence with the drain/source bias applied **(a)** to a device where an asymmetry appears between drain and source configuration and **(b)** to a device where drain and source configuration present similar results.

in the results shown in Figure 4.14. In this Figure, the amplitude of the RTN signal (normalized) is represented against the drain and gate bias. The origin of the RTN signal can be assimilated into a fluctuation of the threshold voltage: $V_{T-RTN} = V_{T0} + \Delta V_{T0}$, where V_{T0} is the RTN-free threshold voltage of the transistor. As the drain bias increases, the amplitude of the noise increases according to $\Delta I_D \propto (\Delta V_{T0})\, V_D$ (as long as V_D keeps low enough to guarantee linear regime [138]). This is not the case of the influence of the gate bias, since the amplitude ΔI_D remains constant with V_{GS} (the normalized amplitude decrease as shown in Figure 4.14). This fact, sometimes underrated, is of particular importance when the excursion of the drain bias ranges from extreme 0 to V_{DD} values like in digital applications [139]. In a first order approximation, the amplitude of the noise is directly proportional to the gate transconductance and to the relative position of the trap in the oxide $(1 - x_T/t_{ox})$ [140]. This model is corroborated later in this Section with the accurate extraction of the trap position from Equation 4.5.

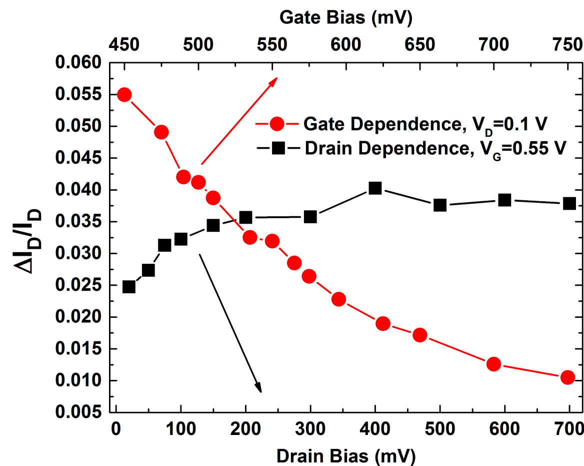

Figure 4.14: Normalized amplitude of the RTN signals as a function of the gate bias and the drain bias. Same device than in Figure 4.13.b (trap located in the middle of the channel). $L = 100nm$, $W = 80nm$.

The characteristic times of the trap are governed by Shockley-Read-Hall statistics, $\tau_c = 1/(nv\sigma)$ and $\tau_e = exp[(E_F - E_T)/k_B T]/gnv\sigma$, where E_T represents the energy level of the trap (see Figure 4.15); E_{Cox}, the insulator conduction band energy; k_B, is the Boltzmann constant; v, is the carrier average velocity; σ, is the capture cross-section; and g, is the degeneracy factor [94, 141]. According to this model, the ratio between time constants is related with the energy level of the trap:

$$\frac{\tau_c}{\tau_e} = g * exp(\frac{E_T - E_F}{k_B T}) \tag{4.3}$$

From the analysis of the schematic shown in Figure 4.15, the difference between the energy level of the trap, E_T and the Fermi energy level E_F is given by:

$$E_T - E_F = -[(E_{Cox} - E_T) - (q\phi_S - \chi_{ox} - q\psi_S) + \frac{x_T}{t_{EOT}}(|V_{FB}| + V_G - q\psi_S)] \tag{4.4}$$

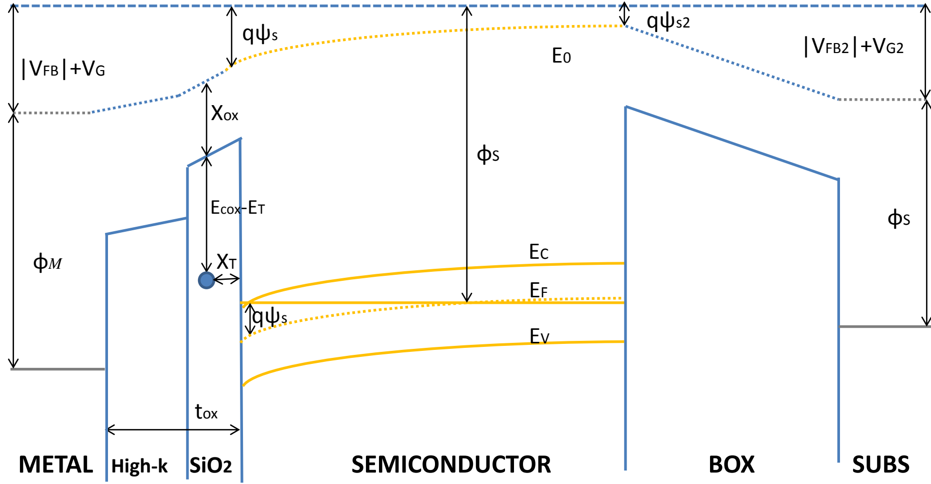

Figure 4.15: Energy-bands diagram for a back-biased (V_{BG}) SOI-MOSFET with a single trap inside the gate insulator.

where ϕ_s is the work function of the semiconductor; χ_{ox}, the electronic affinity of the oxide; ψ_s, the surface potential of the semiconductor (front-gate interface); V_{FB}, the flat-band voltage; and x_T, the physical position of the trap measured from the channel/silicon-film interface. Combining the previous relationships, the ratio between capture time and emission time yields Eq. 4.5 which relates the ratio between τ_c and τ_e with the energetic position of the trap.

$$ln\frac{\tau_c}{\tau_e} = -\frac{1}{k_B T}[(E_{Cox} - E_T) - (q\phi_S - \chi_{ox} - q\psi_S) + \frac{x_T}{t_{EOT}}(|V_{FB}| + V_G - q\psi_S)] \tag{4.5}$$

From Equation 4.5 the position of the trap is worked out by differentiating it with respect to the front gate bias V_G:

$$x_T = \frac{t_{EOT}(\frac{k_B T}{q}\frac{d\ln\frac{\tau_c}{\tau_e}}{dV_G} + \frac{d\psi_s}{dV_G})}{\frac{d\psi_s}{dV_G} - 1} \tag{4.6}$$

Once the physical position of the trap is known from Eq. 4.6, its energetic position is evaluated from Eq. 4.4. Note that Eq. 4.6 is valid as long as the trap is located inside the SiO_2 cap layer. However, this is the most common case: it is not easy to observe RTN signals caused by traps in the high-k dielectric, because there are few traps close to the silicon Fermi level due to the high conduction band offset between the hafnium based oxide and the SiO_2. Even in the case of traps located close to the conduction band edge of the hafnium based oxide, the electrons would be prone to escape due to fast thermionic emission to the metal contact of the gate [142].

Figure 4.16.a shows typical τ_c and τ_e trends obtained for two $L = 100nm$ SOI transistors. In both devices, the capture time presents strong dependence with the gate bias, the larger the carrier concentration of the inversion channel, the larger the probability for a carrier to be captured. In contrast, the emission time is basically independent of the gate bias. This absence of electric field dependence points at the thermionic emission as the primary mechanism for the electrons to escape from the trap. Both τ_c and, especially τ_e values, are larger in Device #2 than in Device #1. This fact reflects the higher difficulty for the electrons to tunnel into the trap (related to the physical position and the activation energy for the capture) and to escape from it (related to the activation energy for the emission). Quantitative confirmation is provided in Figure 4.16.b where $ln(\tau_c/\tau_e)$ is plotted as a function of V_{GS}. From Eq. 4.6, the position of the trap in Device #1 is $x_T = 0.75nm$ whereas $x_T = 0.98nm$ for the Device #2. The energy level of the trap (E_T) with respect to the conduction band of the insulator is $E_{Cox} - E_T = 3.07eV$ for Device #1 (lower in energy) and $E_{Cox} - E_T = 2.98eV$ for Device #2.

4.4 Temperature dependence

On a second stage, we studied the trapping and detrapping mechanisms as a function of temperature (same devices as in Section 4.3). Figure 4.17 shows the time-domain current characteristics of two transistors affected by single-trap

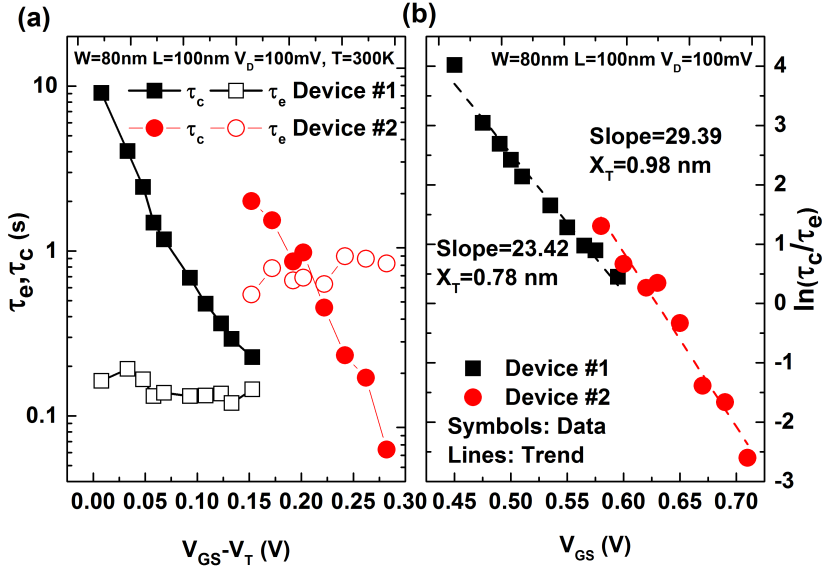

Figure 4.16: **(a)** τ_c and τ_e dependencies with the gate bias corresponding to two SOI transistor with $L = 100nm$, $W = 80nm$ and featuring a single active trap. **(b)** $ln\frac{\tau_c}{\tau_e}$ plot to extract the physical and energetic position of the trap.

RTN. The nature of the trap is responsible for different behaviors in each case (note that the difference in the absolute value of the drain current is conditioned by the threshold voltage variability). In Figure 4.17.a, as temperature increases, the carriers are able to surpass more easily the barrier of capture. In addition, the threshold voltage decreases jointly with the increase of temperature [143], and therefore, the carrier concentration for a given gate bias increases. As a result, the capture time always decreases (the trap becomes more easily filled). However, the decrease in the capture time is compensated in a different way in both devices. In Device #1, as temperature increases, the detrapping events become more intense. At low temperature $\tau_c < \tau_e$, but as T increases the relationship is reversed becoming $\tau_c > \tau_e$. The immediate consequence is that the trap tends to be empty most of the time. In contrast, for Device #2, $\tau_c > \tau_e$ at low temperature. The increase in T only tends to accentuate the difference between τ_c and τ_e. Figure 4.18.a shows the τ_c and τ_e dependence with temperature. For Device #1, the decrease in τ_e is more pronounced than in τ_c. This fact causes the fast emission of

the trap which tends to keep the current level on its high state in Figure 4.17 (τ_e may become so short that the 2ms sampling rate of the SMUs may be too large to capture the events). For Device #2, both time constants decrease simultaneously maintaining the $\tau_c > \tau_e$ asymmetry in all the temperature range.

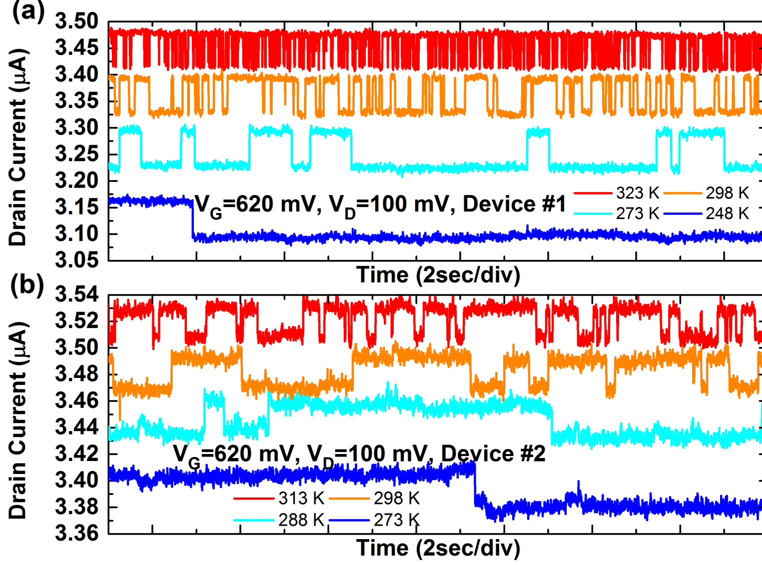

Figure 4.17: Drain current signals at a constant bias in two transistors affected by RTN. For case **(a)**, only at high temperature, $\tau_e < \tau_c$ whereas in case **(b)** $\tau_e < \tau_c$ in all the measured temperature range. $V_{t,1} = 0.442V, V_{t,2} = 0.428V$.

The explanation for the distinct behaviors is clarified through the extraction of the thermal activation energies involved in each process (capture and emission) for the two devices. The activation energies can be extracted from the temperature dependence of the capture and emission times [94]:

$$\tau_c = \frac{exp(\Delta E_c/kT)}{I_D T \sigma_0 \zeta} \tag{4.7}$$

$$\tau_e = \frac{exp(\Delta E_e/kT)}{T^2 \sigma_0 \eta} \tag{4.8}$$

where η and ζ are constants for a given device [94], ΔE_c and ΔE_e are the activation energies: thermal energy needed for capturing and emitting an electron

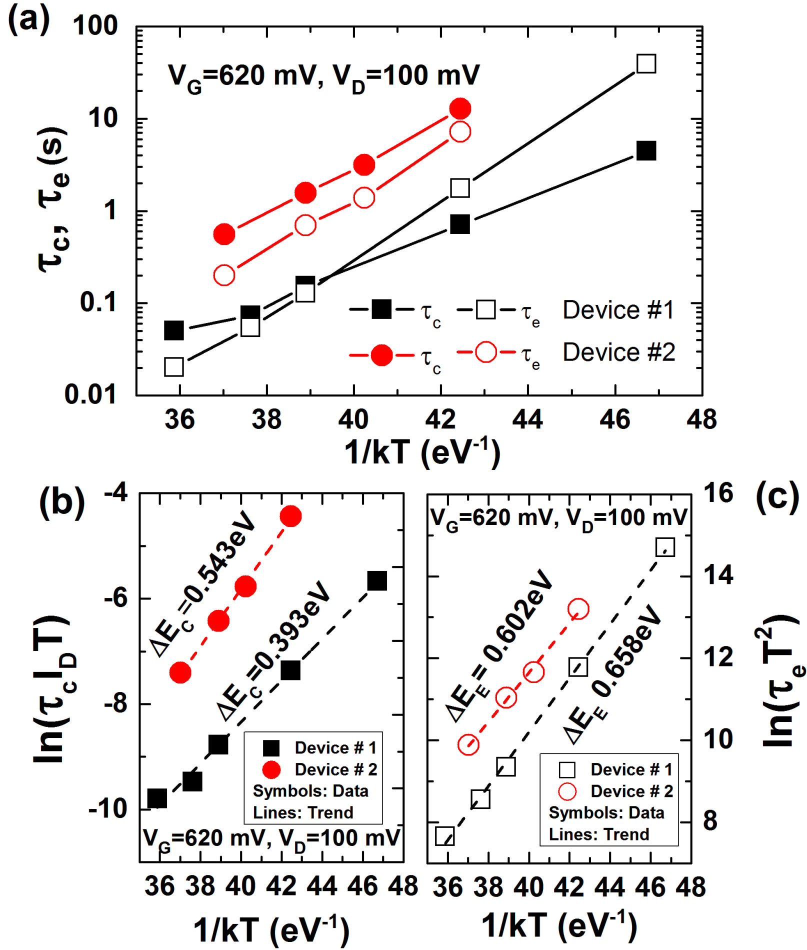

Figure 4.18: (a) τ_c and τ_e dependencies with temperature ($1/kT$) for $L = 100nm$, $W = 80nm$ SOI transistors with a single active trap. **(b)** $Ln(\tau_c I_D T)$ vs. $1/kT$ for the extraction of the capture activation energy. **(c)** $Ln(\tau_e T^2)$ vs. $1/kT$ for the extraction of the emission activation energy.

respectively. σ_0 is the intrinsic trap capture cross section. The activation energies can be derived from plots of $ln(\tau_c I_D T)$ and $ln(\tau_e T^2)$ versus $1/kT$ (Figures 4.18.b & c).

Figure 4.18.b shows the capture activation energy for each one of the two devices (ΔE_c). The case of the lower activation energy of the Device #1 ($\Delta E_c = 0.393eV$ vs. $\Delta E_c = 0.543eV$ for Device # 2) explains the shorter capture times

show in the previous Figures (4.16.a and 4.18.a). The emission activation energy extracted in Figure 4.18.c permits to determine the trap energetic position with respect to the conduction band edge of the semiconductor through $\Delta E_e - \Delta E_c = E_C - E_T$, [94]: $0.257eV$ for Device #1 and $0.06eV$ for Device #2, i.e. both traps are located above the conduction band edge at $V_G = 620mV$. In spite of the low emission activation energy for the trap in Device # 2 would favor the fast emission of the carrier (shorter τ_e), this effect is inhibited by the deeper physical location of the trap in the SiO_2 ($x_T = 0.98nm$).

To sum up the previous discussion, the competition of capture and emission times is dependent of the position and activation energies of the trap [94], therefore it must be studied in each particular case together with the trap attributes presented in Figure 4.16.b.

4.5 Substrate bias dependence

Substrate bias is an unquestionable advantage of SOI technology with respect to its bulk counterpart. This additional degree of freedom in the bias entails the possibility to tune the threshold voltage [123], suppress the vertical field (mobility enhancement [126]) or create interesting memory effects [144]...

Figure 4.19.a presents an example of experimental values of τ_c and τ_e obtained as a function of gate bias, for different substrate bias. The increase of V_{G2} (for a given V_{G1}) yields a decrease in τ_c, but an increase in τ_e. It is worth mentioning that the behavior observed in Figure 4.19.a cannot be explained only by the shift of the threshold voltage induced by the back-bias according to the Lim-Fossum model [85] (Section 2.3.1.2, Chapter 2):

$$V_t = V_t^I - \frac{C_{Si}C_{BOX}}{C_{ox}(C_{Si} + C_{BOX})}(V_{G2} - V_{G2}^I) \tag{4.9}$$

where C_{Si}, C_{BOX}, C_{ox} are the silicon, BOX and front-gate oxide capacitances respectively. V_{G2} is the substrate voltage and V_t^I is the threshold voltage of the front-channel when the back interface is inverted and V_{G2}^I is the substrate voltage to achieve inversion at the back interface [85].

The V_t shift predicted by Eq. 4.9 is not enough to correlate the curves in Figure 4.19.a: this (direct) correction would correspond only with a lateral shift

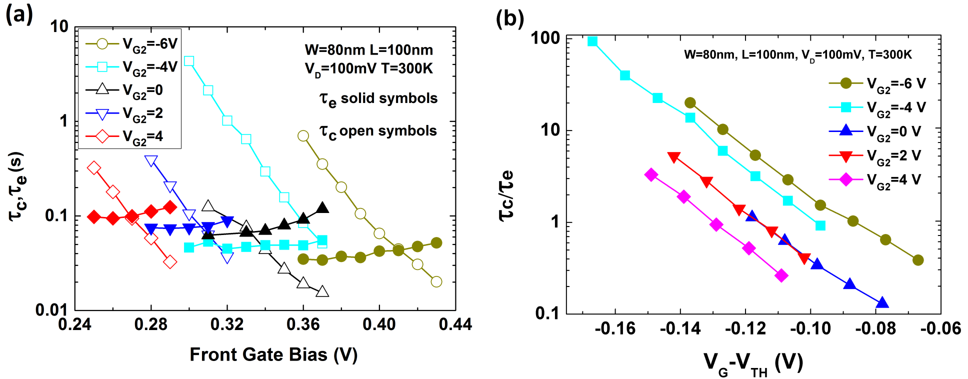

Figure 4.19: (a) Capture, τ_c, and emission, τ_e, evolution as a function of the gate bias for different substrate biases (V_{G2}). (b) τ_c/τ_e ratios as a function of the gate overdrive bias for different negative and positive substrate biases.

of the curves (displacement in the V_G axis) but, for example, it cannot explain the decrease observed in τ_e. This fact is even clearer if the τ_c/τ_e ratios, used to extract the physical parameters of the traps, are plotted as a function of the gate overdrive, Figure 4.19.b. As observed, although the curves are presented as a function of the overdrive voltage, the τ_c/τ_e ratio depends on the particular value of V_{SUB} (even though the inversion charge is the same in all cases). However, Equation 4.9 can be included in Equation 4.5 to capture the influence of the substrate bias in the whole physics of the process.

The accuracy of this model has been checked by reproducing the experimental value of $ln\frac{\tau_c}{\tau_e}$ for two different transistors (Figure 4.20) under different substrate bias conditions. As observed, the models provide very reasonable prediction of the electrical characteristics as long as Eq. 4.9 remains valid, i.e. depletion regime of the back interface.

Moreover, Figure 4.21 shows the values of τ_c and τ_e as a function of the overdrive voltage for the previous devices. From the analysis of this plot we can appreciate that for a given overdrive voltage, the capture time (τ_c) decreases whereas the emission time (τ_e) increases as V_{SUB} increases, that is to say, the carrier keeps trapped for more time. This effect is contrary from what we may expect considering classical RTN models relying on the inversion charge and the

decrease of the electric field in the Si-film while increasing the substrate bias [85]. In contrast, these results are compatible with the fact that the carrier is emitted to the metal gate contact since, for this mechanism, the lower the gate-oxide electric field intensity, the larger the probability of the trap to be filled [145].

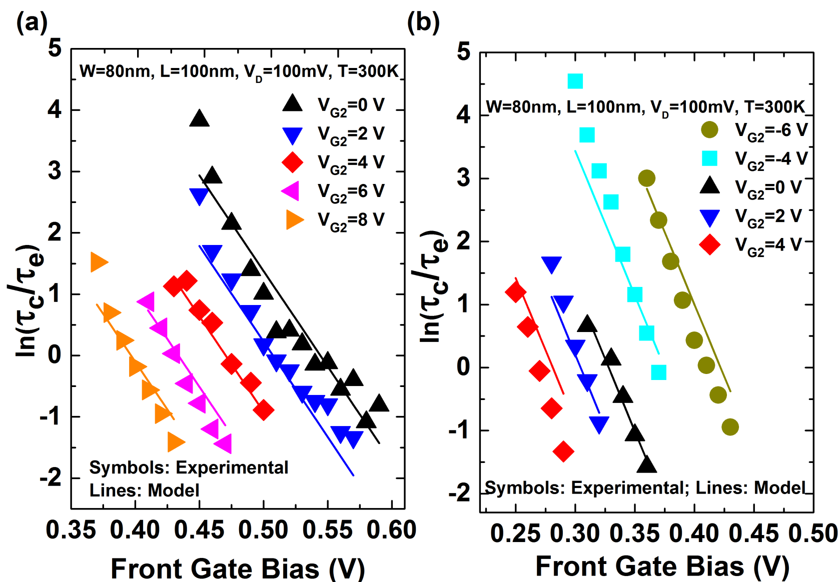

Figure 4.20: Comparison of the experimental values of $ln(\tau_c/\tau_e)$ (symbols) and the proposed model (lines) for two devices (a and b).

4.6 Conclusion

This chapter has introduced an exhaustive method to identify, experimentally, single-trap Random Telegraph Noise by combining the noise Spectral Scanning by Gate Bias technique (SSGB) with a modified Weighted Time Lag Plot method (w-TLP). The characterization protocol has been implemented in an automatic probe-station and applied for the massive test of the devices all over a wafer providing information about the distribution of traps. Shockley-Read-Hall models have been applied to determine the position of the trap inside the gate oxide in terms of the physical location and the energetic position. The combination of both attributes can produce different behavior when the carrier concentration or

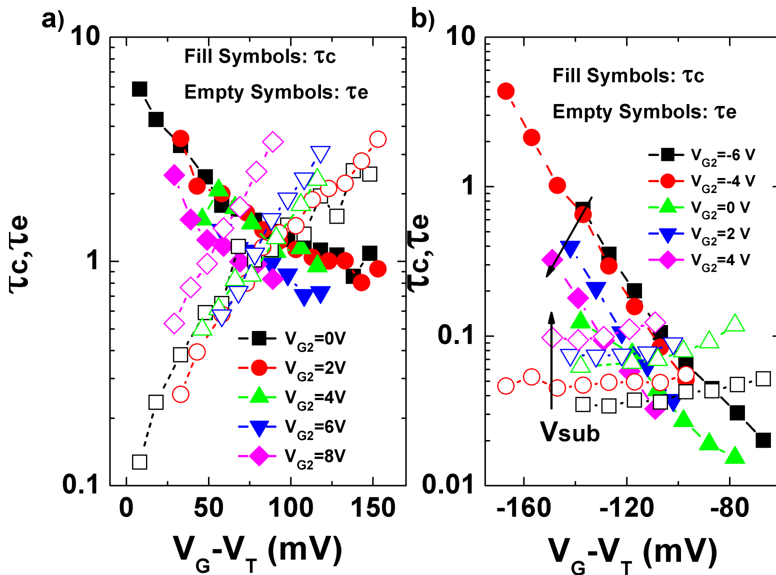

Figure 4.21: τ_c and τ_e ratios as a function of the gate overdrive voltage for different substrates biases in the same devices than in Fig. 4.20.

the temperature in the channel increases leading to extreme situations: the trap tends to be always empty or always filled. Finally, the impact of the substrate (or back-) bias is studied on the RTN characteristics. The models have been updated predicting the characteristic times under positive or negative substrate bias provided that the back interface is in depletion. Additionally, the results show a non-intuitive trend leading to an increase of the emission time (decrease of capture time) when the electric field in the film is relaxed by increasing the substrate bias, for a given inversion charge. Nevertheless, this behavior could be explained by the carrier emission to the gate metal contact.

Chapter 5

Impact Ionization in Fully-Depleted SOI Transistors

This chapter faces the study of impact ionization in Silicon-On-Insulator transistors from the direct characterization of the body current and electrostatic potential. Thin and ultra-thin body-contacted Silicon-On-Insulator transistors have been used for the experimental characterization. The large influence of the channel length on the evolution of the body potential as well as the severe loss of electrostatic control of the body by the gate due to the hole injection have been pointed out. Finally, the dependence of the impact ionization and the subsequent current generation with the substrate bias have also been studied.

5.1 Introduction

The shrinking of MOS transistor dimensions is typically performed by a scaling factor of 0.7 in feature size per each technology generation. The power-supply voltage is reduced moderately in comparison to the channel length, therefore the lateral electric field increases in each node. Impact ionization is an inherent phenomenon of scaled MOSFET operated at a high lateral electric field regime ($V_D = V_{DD}$) [25]. The highly energetic electrons, which move from the source to the drain, knock electrons out of their bound state in the crystal atoms and promote them to a state in the conduction band, creating electron-hole pairs [52]. In bulk devices, electrons are collected by the drain while holes escape through

the substrate of the device (Figure 5.1.a).

In normal device operation, carriers are injected from the channel into the drain region and accelerated under high fields. The probability of a carrier to form an electron-hole pair is given by the ionization coefficient α_i [146]. Thus the excess number of carriers in a region dx is given by $\delta_n = n\alpha_i dx$, where n is the number of carriers injected into drain depletion region from the channel. The total excess number of carriers across the drain depletion region can be obtained through $\Delta_n = \int(n + \delta_n)\alpha_i dx$. The functional dependence of α_i is given by $\alpha_i = \alpha \exp(-B_i/E)$, where α and B_i are constants and E is the magnitude of the electric field [147]. The maximum electric field can be obtained as $E_m = (V_{DS} - V_{D-sat})/l_p$ where V_{D-sat} is the drain voltage at which carrier velocity saturates and l_p is the effective length of the velocity-saturation region [146,147]. The interpretation of the previous formula is that $V_{DS} - V_{D-sat}$ is the voltage drop in the velocity-saturation (or pinch-off) region where l_d depends on the junction depth, the oxide thickness and the substrate doping concentration. By transforming to current equations one obtains [146,147]:

$$I_{ii} = I_D A_i \left(V_D - V_{D-sat}\right) \exp\left(-\frac{l_p B_i}{V_D - V_{D-sat}}\right) \tag{5.1}$$

The expression 5.1 is the mathematical description of the substrate current generated.

In Silicon-On-Insulator (SOI) N-MOSFETs, the minority carriers, electrons, are collected by the drain, while the majority carriers, holes, cannot escape through the substrate of the device (Figure 5.1.b), giving rise to a gradual charge storage in the body of the transistor [52]. This increase of the charge is translated into an increase at the body potential, reducing the threshold voltage and the source potential barrier (source-body potential barrier lowering) [53]. This effect yields an increase of the drain current, or *kink effect*, in the characteristic of the transistor (Figure 5.2). This phenomenon is typically manifested in partially depleted (PD) transistors consequence of both the threshold voltage reduction and the source-body potential barrier lowering, however this effect is not usually observable in fully depleted (FD) devices because the electric field near the drain is lower in fully depleted transistor than in partially depleted transistors [52,53].

P-channel devices are free of kink effect because the coefficient of electron-hole

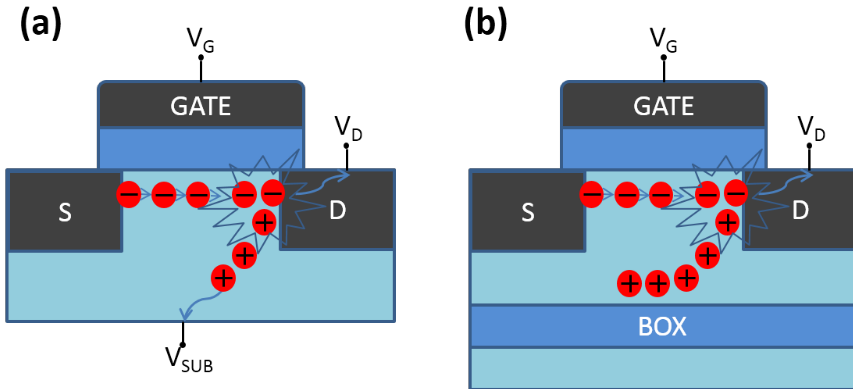

Figure 5.1: Schematic illustration of the impact ionization in a N-MOSFET. (a) In bulk transistors, electrons are collected by the drain while holes escape through the substrate. (b) In Silicon-On-Insulator transistors, the minority carriers, electrons, are collected by the drain, while the majority carriers, holes, cannot escape through the substrate of the device.

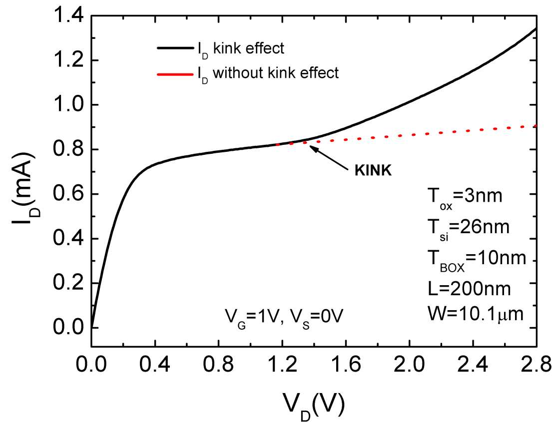

Figure 5.2: Experimental drain current as a function of drain bias in a SOI transistor where kink effect is observable (black line), and the current without kink effect (red line) is approached.

pair generation by energetic holes is much lower than that by energetic electrons.

From the SOI technology prospective, impact ionization has a two-folded effect: on positive side, it leads to an increase of the device performance by the increase on the saturation current [54], especially in the field of digital circuits. In addition, impact ionization has also been used as a fast programing mecha-

nism in SOI floating-body memory cells [55, 148] (Figure 5.3). However, on the negative side, impact ionization worsens the noise characteristics and it may lead to reliability issues arisen from hot carrier generation. In general, hot carriers, particles accelerated by the high electric field, can be injected into normally forbidden regions of the device, as the gate dielectric, where they can get trapped or generate interface states. These defects then lead to threshold voltage shifts and transconductance degradation of MOS devices, Figure 5.4. To avoid, or at least minimize hot carrier degradation, several device design modifications, such as larger designs, can be made [51]. As illustrated, the large effect that impact ionization has on the characteristics of SOI transistors makes this phenomenon a subject that cannot be disregarded on present technologies, furthermore, when the gate length of the transistors is scaled more intensively than the supply voltage, yielding a dramatic rise in the lateral electric field [149].

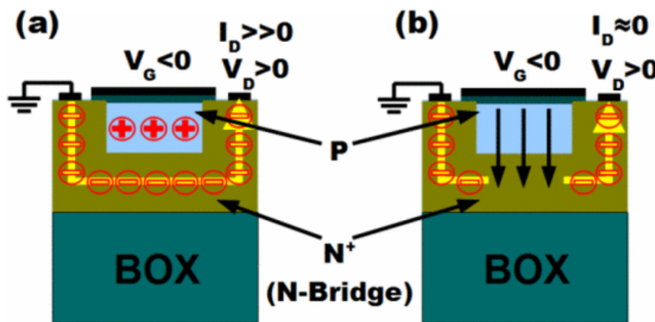

Figure 5.3: A2RAM memory cell schematic. (a) The top semi-body stores the holes generated by impact ionization or band-to-band tunneling whereas the N-bridge is used for current sensing ('1' state). (b) The holes are evacuated ('0' state). Reproduced from [148].

Despite the impact ionization might have an important role both in the increase of the device performance and in the rise of reliability issues in SOI technology, the experimental characterization is not straightforward as it could be in a bulk transistor. The BOX does not permit to characterize the body current directly, being impossible to establish a contact with the silicon layer. A possible solution is the implementation of transistors with a body-contact: H-gate body-contacted transistors with five terminals will be described below.

In the following pages, body potential and body current of thin body and ultra-thin body N-MOS SOI transistors have been studied through direct body-contact

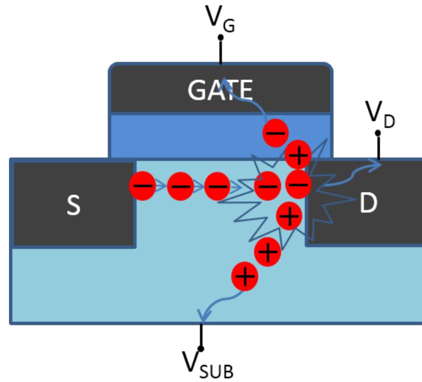

Figure 5.4: Schematic illustration of carriers being injected into the gate dielectric. These *hot carriers* (injected into the gate) might induce device degradation and reduce the transistor lifetime [51]. This degradation effect is considered as a major reliability problem in last technologies.

monitoring. In Section 5.2, the experimental methodology for the electrical characterization and the device features are explained. Section 5.3 shows and analyzes the results obtained from the experimental characterization: In Subsection 5.3.3 and 5.3.4, special attention has been paid to analyze the role of the channel scaling and the inversion charge level, extracting the impact ionization coefficients. Finally, the substrate bias dependence of impact ionization is analyzed in Subsection 5.3.5.

5.2 Methodology and experimental setup

The experiments of this chapter have been performed on H-gate body-contacted SOI MOSFETs (five-terminal devices) fabricated at CEA-LETI in a 22nm process [150]. Two sets of devices featuring a silicon body thickness of $t_{Si} = 26nm$ (thin body, TB) and $t_{Si} = 7nm$ (ultra-thin body, UTB) have been considered, with an equivalent oxide thickness (EOT) of $3.0nm$ and $1.2nm$ respectively. All the devices studied are $10\mu m$-wide with channel lengths ranging from $40nm$ to $10\mu m$. The body connection is implemented by lateral highly p-type Si doping. The layout of the devices and a schematic illustration are shown in Figure 5.5.

The measurements were performed in a Süss PA-300PS probe station driven by a Keithley 4200-SCS with 5 independent source measurement units (SMUs)

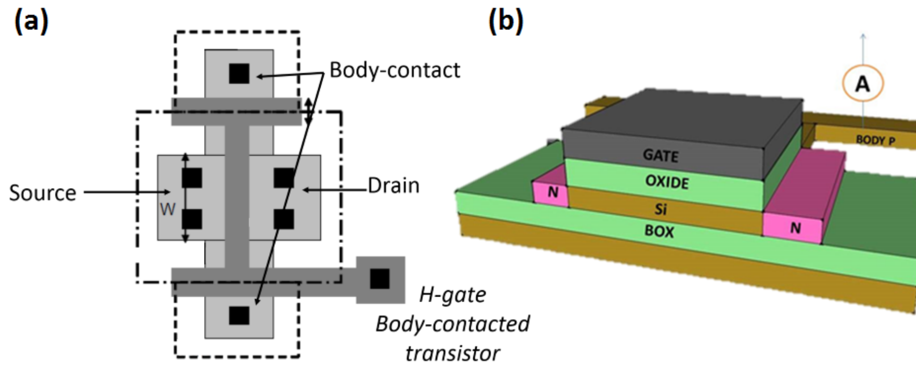

Figure 5.5: (a) Layout of the H-gate body-contacted SOI-MOSFETs used for the study. (b) Schematic 3D illustration of the body-contacted SOI device.

connected to each terminal of the device. The noise characterization is carried out by using the Synergie noise analyzer (Chapter 2). The drain current power spectral density is measured while the gate and drain terminals are biased at a fixed point.

The access to the transistor body for experimental characterization of impact ionization current entails an important drawback: when the SMU of the semiconductor analyzer is operated as drain for the holes, it is mandatory to fix a voltage at the contact to measure simultaneously the current. This experimental configuration disrupts the normal electrostatic conditions of the transistor forcing a specific potential distribution in the body of the device. To circumvent this issue, the measurements have been performed in two stages:

(i) *Zero-current measurements:* The body-contact is set to an open circuit condition, $I_B = 0$, while the potential at the contact is simultaneously measured. These measurements allow to determine the evolution of the potential of the body thus disclosing the conditions where the accumulation of positive charge raises the body potential up to the point where the body-to-source junction is forward-biased.

(ii) *Zero-potential measurements:* The body-contact bias is set to $0V$ draining the holes generated by impact ionization through the body-contact.

Figure 5.6 shows the experimental scheme of the both characterization meth-

ods.

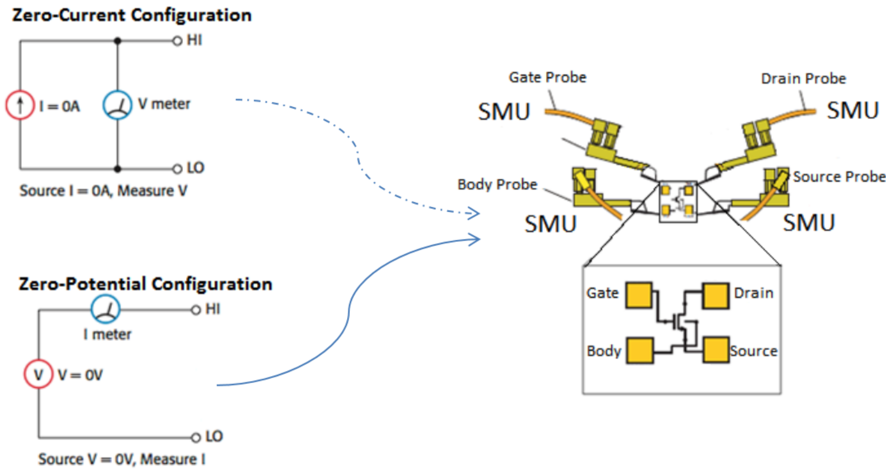

Figure 5.6: Schematic illustration of the experimental configuration used for the characterization of body-contacted devices. *Zero-current* configuration allows to measure the body potential and *Zero-potential* configuration sets the body-contact potential at $0V$ and allows to measure the hole current generated by impact ionization. The five-terminal H-gate body-contacted SOI-MOSFETs are biased and measured by using source-measure-units (Substrate contact through the platter of the equipment is not shown).

5.3 Results and discussion

Before a deeper analysis, and to corroborate that body-contacted devices do not introduce more characterization artifacts than their non body-contacted counterparts, an initial assessment of the body-contacted devices was carried out by comparing the quasi-static $I_D - V_G$ characteristics with identical devices lacking of the body-contact. The experimental result of the comparison is shown in Figure 5.7: the characteristic (even at this high V_D value) is identical in both devices showing no degradation of the driven current or threshold voltage shift.

The same strategy is carried out in the low-frequency noise characterization: Figure 5.8 shows a comparison of the low-frequency characteristics between body-contacted devices and identical devices lacking of the body-contact. Power spectral density is similar in both devices showing no degradation caused by reliability issues in the additional interfaces.

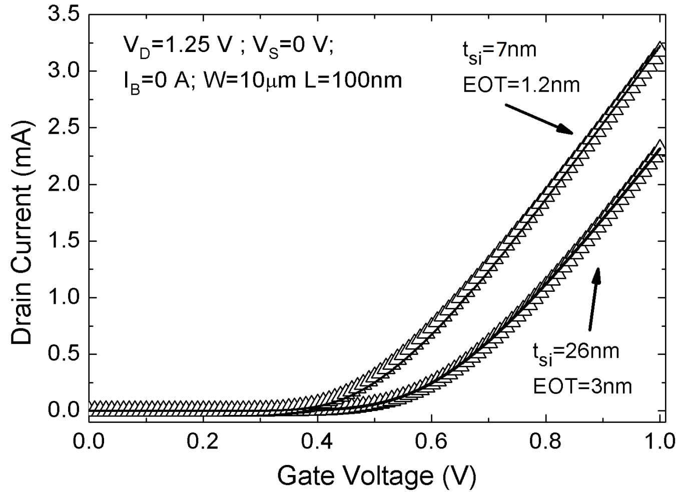

Figure 5.7: $I_D - V_G$ characteristic of a standard $100nm$-length $10\mu m$-width SOI transistor (line) and the H-gate body-contacted counterpart (symbols). Results for thin and ultra-thin body transistors are shown.

Once the similar behavior between both structures is ensured when the body-contact is not biased, the body-contact characterization can be carried out.

5.3.1 Zero-current measurements: body potential characterization

As mentioned before, for body potential characterization, the body-contact is set to an open circuit condition, $I_B = 0$, while the potential at the contact is simultaneously measured. Since no current flows through the body-contact, the potential measured at the contact corresponds, basically, to the electrostatic potential the body. Figure 5.9 shows the results for the two types of devices studied (Figure 5.9.a, UTB device; Figure 5.9.b, TB device). The drain current curves correspond to the typical characteristic extracted in SOI transistors: (a) In UTB devices (Figure 5.9.a) the increase in the drain current is marginal (however the body potential increases abruptly above $V_D = 1.2V$); (b) in the TB devices (Figure 5.9.b), the kink effect is clearly manifested when the body potential increases over 1V.

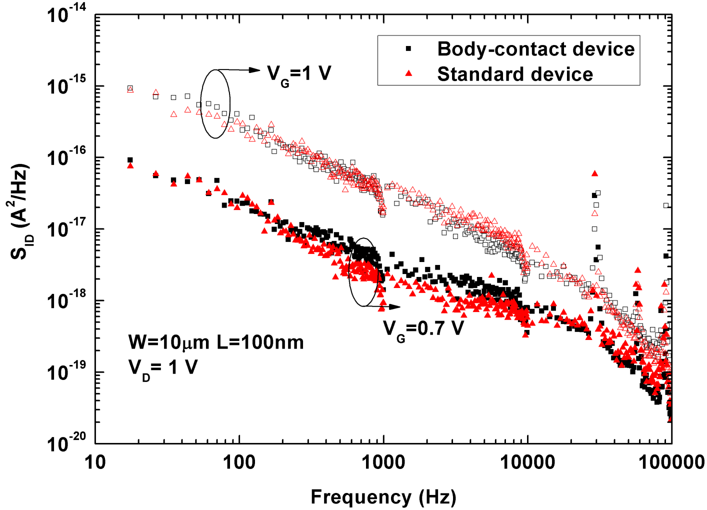

Figure 5.8: Drain current power spectral density as a function of the frequency for a body-contacted FD-SOI transistor (black symbols), and an equivalent device without body-contact (red symbols). Two bias points ($V_G = 1V$ and $V_G = 0.7V$) are shown.

5.3.2 Zero-potential measurements: body current characterization

The second experimental setup consists in monitoring the body current by draining the holes generated by impact ionization, through the body-contact. The body-contact bias is set to 0V, therefore the electrostatic conditions are altered with respect to the *zero-current* experiments. However, since the body-contact presents a non-negligible resistance, the body potential is not fully tied to the contact bias resulting always that $V_B > 0V$.

As observed in Figure 5.10, as soon as kink effect appears (particularly noticeable in TB devices), the current at the body-contact, produced by the holes generated by impact ionization, starts to increase significantly. Notice that this situation occurs when the body potential is $\sim 0.9V$ in the *zero-current* measurements of Figure 5.9.

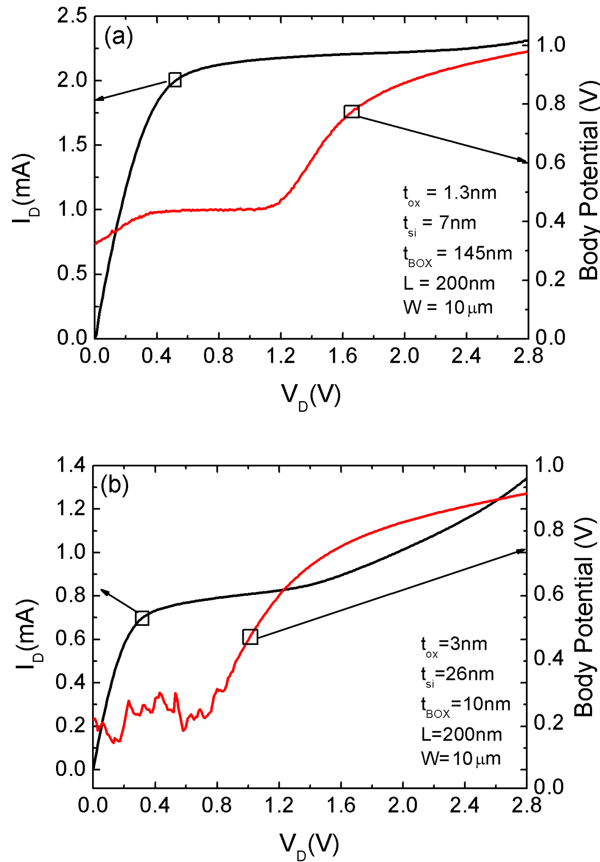

Figure 5.9: Drain current and body potential in a SOI-MOSFET with $L = 200nm$ and $W = 10.1\mu m$ when the body-contact is kept under *zero-current* condition ($I_B = 0$). Gate voltage is set to $V_G = 1V$. (a) Ultra-thin body device $t_{Si} = 7nm$, (b) thin body device $t_{Si} = 26nm$.

5.3.3 Gate length dependence

In order to study the contribution of the gate length scaling on the impact ionization, the first set of experiments has consisted of the measurement of the drain current as a function of the gate bias for UTB transistors with different channel lengths. The source-measurement-unit connected to the body-contact is set to an open circuit condition, following the *zero-current* measurement. Figure 5.11.a shows the impact of the length on the drain current of the transistor. It is observ-

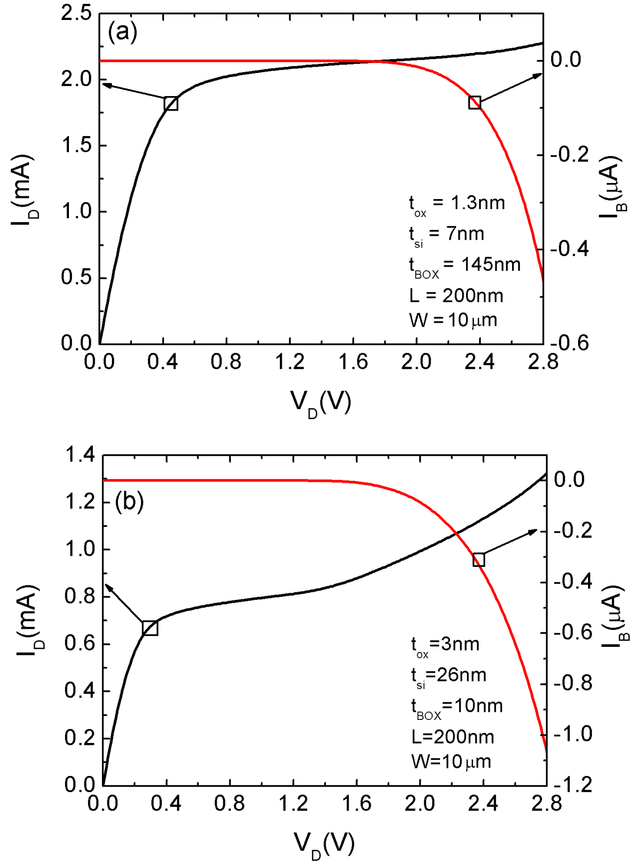

Figure 5.10: Drain and body currents on a SOI-MOSFET with $L = 200nm$ and $W = 10.1\mu m$ when the body-contact is kept under *zero-potential* condition ($V_B = 0$). Gate voltage is set to $V_G = 1V$. (a) Ultra-thin body device $t_{Si} = 7nm$, (b) thin body device $t_{Si} = 26nm$.

able that the shorter length of the device, the larger impact ionization contribution to the drain current. This behavior is easily explainable by the increase of the electric field with the decrease of the length of the device, i.e., the more energetic carriers, the more electron-hole pairs generated. The same behavior is observed in Figure 5.11.b, where the body-contact current is characterized as a function of the drain voltage using the *zero-potential* measurement. Shorter devices present higher body-contact current at the same drain voltage, i.e., more holes injected

in the body due to higher impact ionization current.

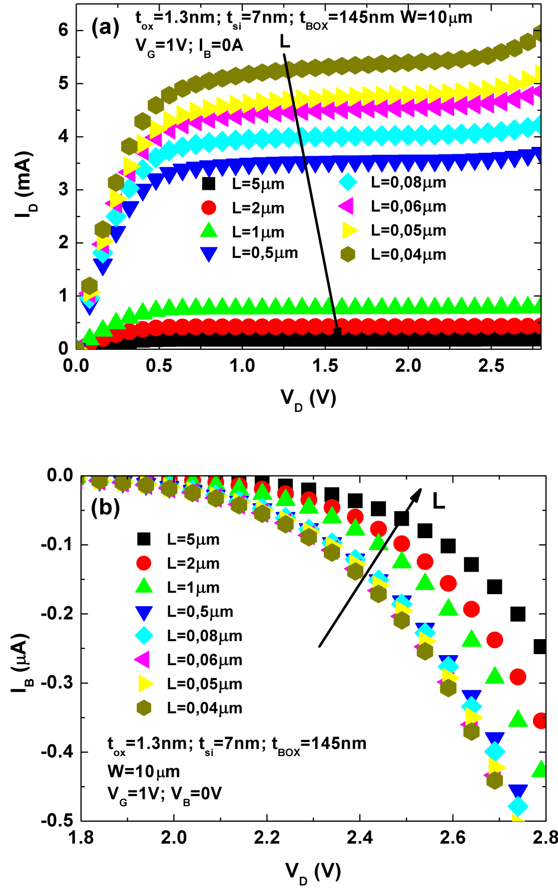

Figure 5.11: (a) Drain current as a function of the drain voltage for different gate lengths. A clear increase in the impact ionization (kink effect) is observable in the shorter devices. (b) Body-contact current as a function of the drain voltage. The shorter device, the higher hole injection in the body of the transistor.

5.3.4 Inversion charge dependence

Apart from the observed impact ionization dependence on lateral electric field, the vertical field dependence must be explored. In this point, the gate bias contribution in the body-contact potential is characterized. As result, Figure 5.12 shows the body-contact voltage as a function of the electric field at the gate for the two different body thicknesses and the most representative lengths. In Figure

5.12.a, for the longer thin body devices, the voltage of the body-contact increases up to a maximum due to the injection of holes by impact ionization, then it decreases consequence of the onset of the electron channel (the voltage never gets a negative value since the body-contact is not measuring directly at the channel interface). The situation for the shorter transistors is rather different. The electrostatic potential remains high and saturated even above the threshold voltage ($V_{th} \approx 0.42V$). This is a direct consequence of the large number of holes being injected in the body due to impact ionization. This large hole concentration produces the increase of V_B (i.e. ψ_B decrease). Note that this voltage cannot increase indefinitely since, at some, point the body/source PN junction will be triggered on. In both (thin and ultra-thin) devices the behavior is similar, although in the case of the thinner device (Figure 5.12.b) the body-contact voltage is lower as expected in fully depleted devices [151].

Figure 5.13 shows the measured body-contact voltage as a function of the gate bias for different values of the drain bias in the thin body transistor. For the longer device, (Figure 5.13.a) the body potential is controlled by the gate bias. Although for higher V_D values, the gate starts to lose the control of the body potential which becomes only dependent of the drain voltage, the prevalence of the control of the drain over the body potential (surpassing the control of the gate) occurs even at a much lower V_D for the case of the shorter devices ($L = 40nm$, Figure 5.13.b), where the gate loses the electrostatic control for $V_D > 0.55V$. The shorter the channel length, the higher the total impact ionization current, leading to an increase in the body-contact voltage due to the exacerbated injection of holes into the body.

For the sake of completeness, the role of the impact ionization at different inversion levels in the channel of the transistor is analyzed. The body-contact current has been monitored by setting the body-contact bias to 0V (*zero-potential* measurement). It was verified that the drain current is the sum of the source, body and gate currents ($I_D = -(I_S + I_B + I_G)$). The measured gate current was low in these devices (pA range), initially positive (electrons flowing out of the gate from the channel), and, as the drain bias increases becoming negative (electrons tunneling at the gate-drain overlap region). These current components do not affect the body current which is modeled by $I_B = (M-1)I_S$, where $(M-1)$ (impact ionization ratio) is obtained by the Equation 5.1 by using the source

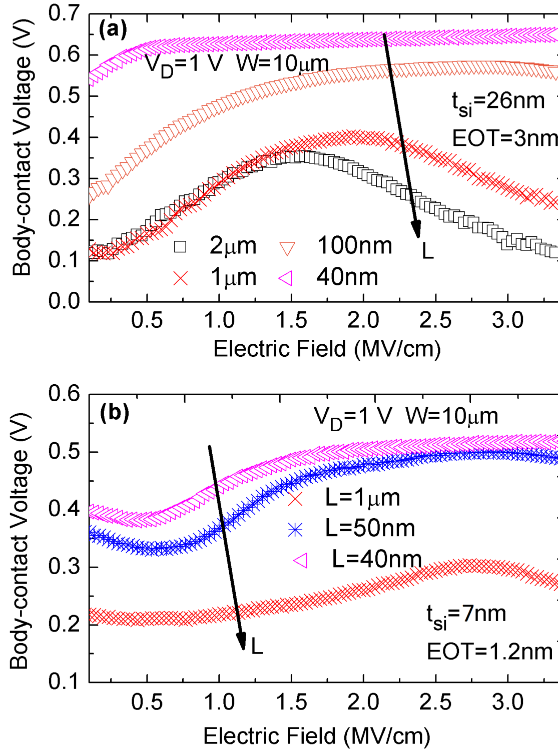

Figure 5.12: Dependence of the measured body-voltage on the gate voltage for devices with: (a) $EOT = 3nm$, $t_{Si} = 26nm$ and length of $2\mu m$, $1\mu m$, $0.1\mu m$ and $0.05\mu m$. (b) $EOT = 1.2nm$, $t_{Si} = 7nm$ and length of $1\mu m$, $0.05\mu m$ and $0.04\mu m$. $V_D = 1V, V_S = 0V, I_B = 0A$.

current which is exempt from the impact ionization contribution.

Figure 5.14 shows the measured body-contact current (Figure 5.14.a) and impact ionization ratio (I_B/I_S) obtained form Equation 5.1 (Figure 5.14.b). Note here the difference between the impact ionization ratio and the total impact ionization current. Whereas the latter is higher as higher current flows through the device ($-I_B$, Figure 5.14.a), the ratio is larger at lower inversion charge 5.14.b. This situation is predicted in Equation 5.1, since the lower V_G, the lower V_{D-sat}, and therefore less negative the argument of the exponential. This fact must be considered carefully in analog designs since the noise spectral density of the drain current can be more impacted at $V_G \simeq V_T$ (where $(M-1)$ is higher) than at

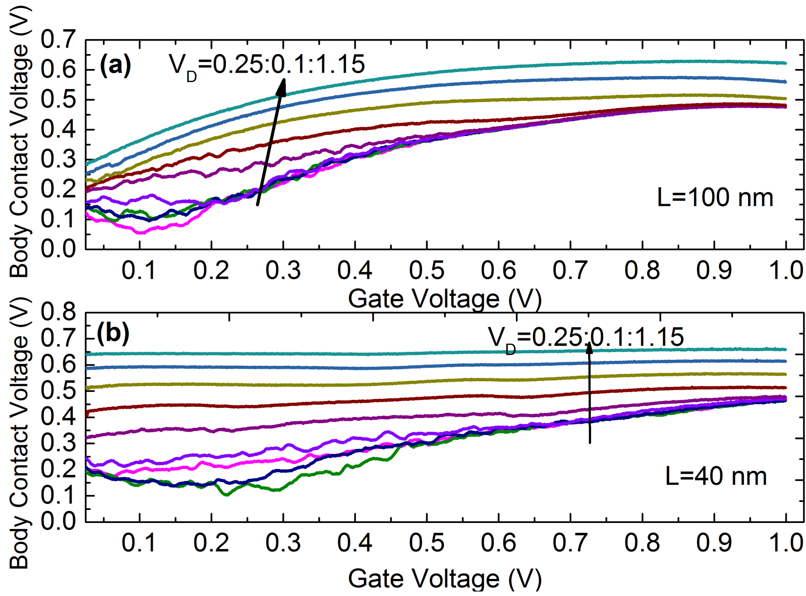

Figure 5.13: Body-voltage as a function of the gate voltage for different drain biases: (a) 100nm gate-length device, (b) 40nm gate-length device. $V_S = 0V, I_B = 0A$. $EOT = 3nm$, $t_{Si} = 26nm$.

higher V_G.

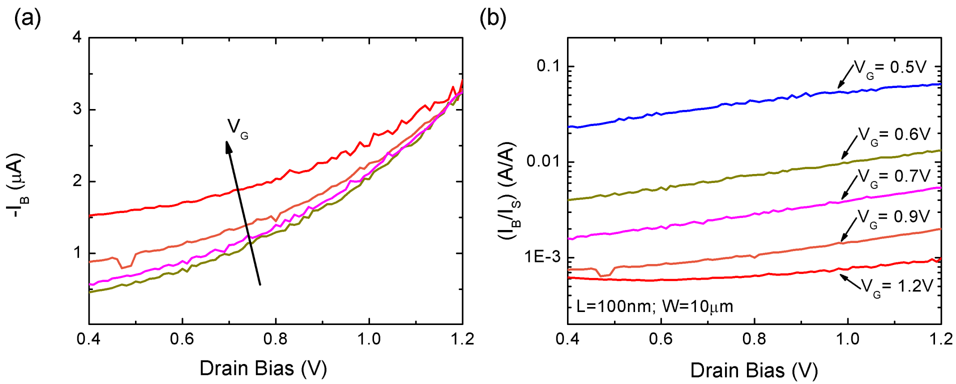

Figure 5.14: (a) Experimental body-contact current, and (b) impact ionization ratio $(M-1)$ as a function of the drain bias, obtained from direct body current monitoring at different inversion levels (V_G). $EOT = 3nm$, $L = 100nm$, $W = 10\mu m$, $t_{BOX} = 10nm$.

From the previous relationships, the ionization coefficients, A_i and B_i, can be

extracted once l_p is known. l_p was previously defined as the effective length of the velocity-saturation (pinch-off) region. One of the approaches for extracting this pinch-off length is through the simulation of the carrier density along the channel and the direct measurement of this pinch-off length. For this purpose, ATLAS-SILVACO simulations of the device have been carried out [152]. Figure 5.15 shows the result of one simulation for the thin body device, where the pinch-off length, l_p, is extracted through the decrease of concentration in the channel at the body-drain junction. Following this method, the estimated l_p values extracted are $24nm$ and $8.4nm$ for TB and UTB device respectively. These results are validated by using the expression $E = (V_{DS} - V_{D-sat})/l_p$, where V_{D-sat} is extracted from the V_D and V_G values, and the maximum of the electric field (E) can be extracted through the simulation. Other additional corroboration is carried out by using the empirical expression of l_p [147]:

$$l_p = 0.22(t_{OX})^{\frac{1}{3}}(X_j)^{\frac{1}{2}} \tag{5.2}$$

where X_j is the junction depth (in thin film SOI devices equal to t_{Si}) [153].

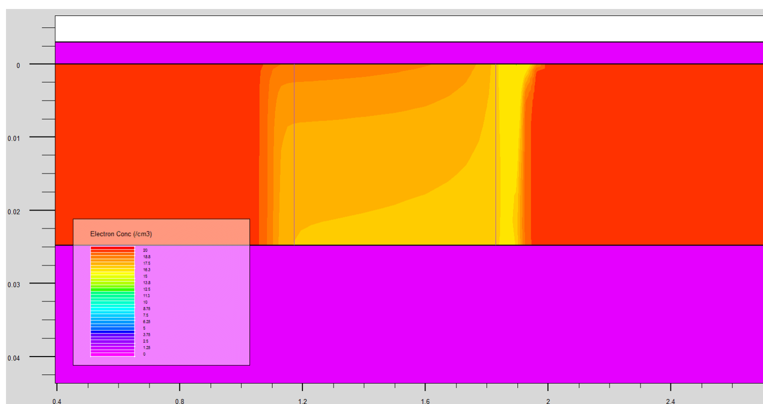

Figure 5.15: Cross-sectioned TB SOI transistor where the electron concentration is obtained from numerical simulations. $EOT = 3nm$, $T_{si} = 26nm$, $L = 100nm$, $W = 10\mu m$, $t_{BOX} = 10nm$, $V_D = 1.2V$, $V_G = 0.7V$.

Finally, the ionization coefficients A_i and B_i have been derived from the experimental results of Figure 5.14, using Equation 5.1 and extracting the value of the effective saturation length l_p from calibrated numerical simulations as shown in Figure 5.15. The updated results given in Table I are significantly

Table 5.1: Ionization coefficients

	A_i (V^{-1})	B_i $(MVcm^{-1})$
$t_{Si} = 26nm$ $EOT = 3nm$	0.010 ± 0.003	0.040 ± 0.015
$t_{Si} = 6nm$ $EOT = 1.2nm$	0.08 ± 0.03	0.8 ± 0.2

lower than those obtained from thick SOI samples or bulk devices ($A_i \approx 2.45$ and $B_i \approx 1.95MV/cm$ [146]).

5.3.5 Substrate bias effect

The impact of the substrate bias on the output characteristics is analyzed for both transistor structures. The substrate of the wafer is biased to a given value while the body-contact is set to open circuit condition. The drain current is measured in these conditions for different values of the drain voltage. According to the results shown in Figure 5.16 (a & b) the negative substrate bias, in addition to increase the threshold voltage of the device as Lim-Fossum model predicts (Section 2.3.1.2, Chapter 2), favors the impact ionization ratio (reduction of the inversion charge). This is clearly observed in Figure 5.16.c & 5.16.d if the impact ionization ratio (in percentage) is shown . For the UTB devices the ratio is about 2.5% at $V_{sub} = 0V$ and increases to 52% at $V_{sub} = -28V$. Even larger increase is obtained for the thin body device (39% at $V_{sub} = 0V$ and 557% at $V_{sub} = -2V$).

5.4 Conclusions

The study of the body potential in fully depleted SOI transistors through a body-contact has revealed significant differences as a function of the body thickness, being the impact ionization current in thin devices higher than in ultra-thin cases. Also the length of the device is an important factor. When it is scaled below 100nm, the experiments highlighted how the body of the transistor becomes flooded with holes when impact ionization takes place, and how the accumulated

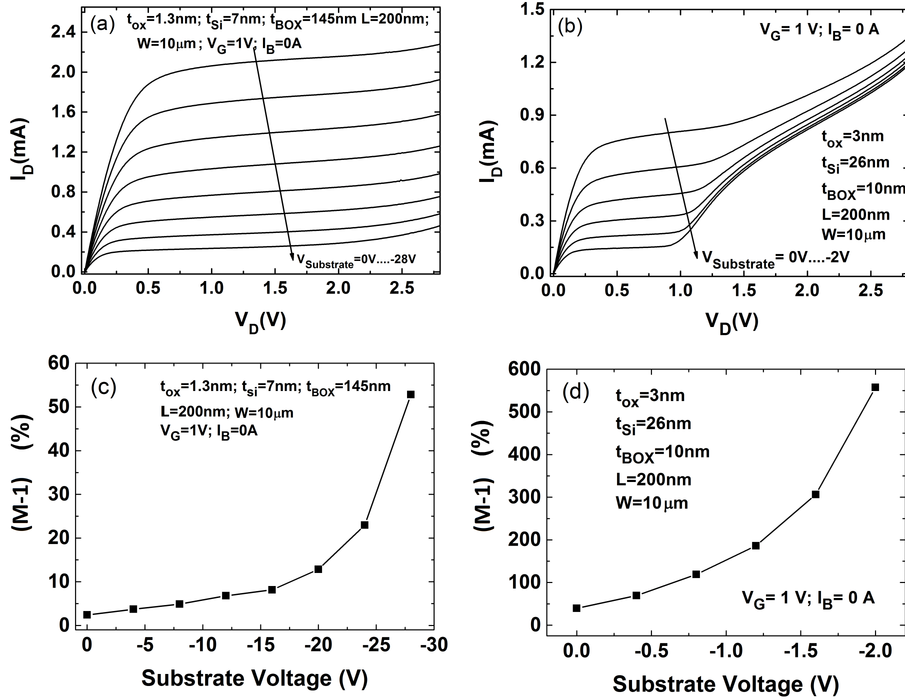

Figure 5.16: Output drain current characteristics and impact ionization ratio on a SOI-MOSFET with $L = 200nm$ and $W = 10.1\mu m$ for different substrate biases when the body-contact is kept under *zero-current* condition ($I_B = 0$): (a & c) ultra-thin body device $t_{Si} = 7nm$, (b & d) thin body device $t_{Si} = 26nm$. (c) and (d) have been extracted at $V_D = 2.8V$.

charge can take the electrostatic control of the body of the device at relatively low drain voltages. The impact ionization ratio has been found to be larger at low inversion charge, being the ionization coefficients of our state-of-the-art SOI MOSFETs significantly lower than those of legacy technologies. Finally, a substrate bias dependence analysis has revealed that the negative substrate bias, in addiction to increase the threshold voltage of the device, favors the impact ionization current ratio due to the reduction of the inversion layer charge.

Chapter 6

Conclusions

This final Chapter stands for giving the main ideas extracted from this work, from the theoretical to the experimental achievements. As a result, important advances in reliability issues in advanced fully processed silicon-on-insulator devices have been investigated.

6.1 Theoretical Framework

Chapter 1 shows a theoretical framework of the miniaturization of the MOSFET transistor in the last decades and the inconveniences that these advances in the reduction of the physical dimensions have supposed in the reliability of the device. Some improvements related to the miniaturization of transistors have been achieved by implementing the gate oxide with high-κ materials and substituting the poly-Si gate by metallic materials. Additionally, silicon-on-insulator technology and FD-SOI transistors with ultra-thin body have allowed to continue with the transistor scaling beyond 22nm nodes. However, all these improvements also imply reliability issues:

High-κ metal gate stacks transistors include an interfacial layer (IL) between substrate and Hf-based high-κ dielectric, which usually raises severe bias instabilities. The most important named negative bias temperature instability (NBTI). It causes an increase in the threshold voltage and subsequent decrease in drain current and transconductance of a MOSFET. Additionally, the aggressive scaling of MOS transistors has decreased the current signals down to the level where

they are not significantly higher than the fluctuations induced by carrier trapping phenomena as the random telegraph noise (RTN) [43]. This issue may induce fluctuations in V_{th} or I_d and, consequently, failure of basic logic circuits. The presence of high electric fields inside the device makes electrons or holes in the channel gain sufficient energy so that their energy distribution becomes much greater than the expected one if they were in equilibrium with the lattice. The generation of these hot carriers can be the cause of several reliability problems. They can lose their energy via impact ionization, which results in substrate currents. This phenomenon is typically manifested as an abrupt increase in the saturation current consequence of both the threshold voltage reduction and the source-body potential barrier lowering.

In this context, Chapter 2 has introduced the theoretical framework and the experimental methods to carry out the electrical characterization of these reliability effects in ultimate devices. Resistivity characterization of the materials, quasi-static measurement of silicon-on-insulator devices and noise characterization have been detailed in this Chapter.

6.2 Main achievements

The main results involving the reliability characterization of ultimate silicon-on-insulator devices are summarized within the respective sections:

- Chapter 3, Bias Instability Characterization. Bias Instability tests have been conducted on bare SOI wafers by introducing a point-contact method. This technique has allowed to study both negative and positive bias stress in electron and hole channels determining that negative bias instability is the predominant effect which can be neutralized after short recovery periods. The comparison of SOI wafers with different film thicknesses and surface quality, together with fully processed MOSFETs, points out that the instability is originated at the top surface of the wafer and not in the BOX. The fast threshold voltage shift at room temperature with very quick and full recovery, has suggested that the traps at the Si-native oxide interface act as the main contributor to the instability effect. Additionally, it has been possible conclude that the threshold voltage shift observed when performing slow capacitance measurements using the Pseudo-MOSFET technique

is originated by the quality of the top interface, being especially critical for the case of thin silicon films with non-passivated surface. In addiction, it has been demonstrated in first instance, that the contribution of the BOX to bias instability at room temperature in ultimate SOI transistor is negligible.

- Chapter 4, Random Telegraph Noise. An exhaustive method to experimentally identify single-trap devices has been introduced. The characterization protocol has been implemented in an automatic probe-station and applied for the massive test of the devices all over a wafer providing information about the distribution of traps and concluding that the number of traps in devices does not follow any spatial correlation. Additionally, the increase of the temperature in the channel leads to extreme situations: the trap tends to be always empty or always filled. Finally, a model of the impact of the substrate (or back) bias on the RTN characteristics have been introduced predicting the characteristic times under positive or negative substrate bias. These results reveal a non-intuitive trend which leads to an increase of the emission time (decrease of capture time) when the electric field in the film is relaxed by increasing the substrate bias, for a given inversion charge. This behavior could be explained by the carrier emission to the gate metal contact.

- Chapter 5, Impact Ionization. The study of the body potential in fully depleted SOI transistors through a body-contact has revealed significant differences depending on the body thickness. As the length of the transistor decreases, the accumulated hole injected charge can take the electrostatic control of the body of the device at relatively low drain voltages. The impact ionization ratio have been found to be larger at low inversion charge, being the ionization coefficients significant lower than those of legacy technologies. Finally, a substrate bias dependence analysis has revealed the negative substrate bias, despite increasing the threshold voltage of the device, favors the impact ionization ratio.

6.3 Future research topic

The future steps in MOSFET miniaturization are not totally clear. A wide range of possibilities is being investigated and analyzed by the biggest semiconductor manufacturers and researchers. Some of them bet that gate-all-around FETs together with SOI technology for the future market needs. Others think that high-mobility channels from SiGe, Ge or III-V materials will be mandatory for device scaling. Moreover, other structures such as nanowire channels or tunnel FETs are being taken into account. By last, the appearance of novel 2-D materials, like graphene or MoS_2 and their counterparts has attracted the attention of the semiconductor industry. In this context, the reliability studies carried out in this thesis have permitted to localize some of most important instability effects which disturb the correct operation of SOI MOSFETs. The methods developed in this thesis for the characterization of instabilities can be easily extrapolated to other novel technologies such as gate-all-around, Fin-FETs, Trigate FETs and the rest of multi-gate structures. They permit, for example, to characterize Random Telegraph Noise in novel silicon nanowires, where the channel length is strongly reduced and a single-trap may change the current into levels which make inoperative the device. The results of impact ionization in body-contacted devices allow to follow studying these structures to reduce the hot carrier degradation. Additionally in impact ionization study, the noise correlation with the length of the device and the impact ionization current is being carried out through experimental low-frequency noise characterization. To sum up, the reliability characterization and methods developed in this thesis are not only interesting in silicon-on-insulator technology, but also are applicable in the characterization of the future technology advances and nodes.

On the other hand, graphene and other 2D material can solve some of the future scaling problems by being integrated in the transistor structure. Despite graphene has stirred the world of material research due to its unique physical properties, the expectations have not been yet materialized into real-world applications due, in part, to the difficulty to produce and pattern large graphene samples. A graphene counterpart, reduced graphene oxide (rGO), has gained a lot of relevance due to its multiple spectrum of applications at a much lower technological effort. Although it is far from achieving the unique properties of graphene,

rGO preserves, to some extent, part of its virtues (flexibility, electrical and thermal conductivity...). This is the reason why we have started to synthesize and electrically characterize two dimensional materials like graphene, graphene oxide or MoS_2. Some of these steps are already advanced: reduced graphene oxide macroscopic samples have been achieved. The point-contact electrical characterization, described in this thesis, has allowed the optimization, in terms of the electrical conductivity, of the synthesized samples, even presenting promising values of the electrical conductivity competing with that of large commercial CVD samples. All these advances and results are shown in Appendix A. Additionally, studies in the interaction metal-reduced graphene oxide are being carried out through the deposition and electrical characterization of different metals on the macroscopic samples by using the transmission line method (TLM). Once the samples are totally optimized and metallized, the future steps are the reliability characterization of transistor structures incorporating these novel materials.

Appendix A

Electrical Characterization of Laser Reduced Graphene Oxide

This appendix is focused on the electrical characterization of laser-assisted reduced graphene oxide by point contact techniques. The aim is twofold: firstly, the careful investigation of in-line two and four point-contact techniques applied to macroscopic samples of reduced graphene oxide. The combination of both methods has shed light on the role of the point-contact when extracting the intrinsic resistivity of the material. Secondly, once the measurement protocol is well understood, it is applied to improve the conductivity of the samples by adjustment of the initial colloid concentration and the photothermal power intensity used for the reduction. The final optimized samples present a promising conductivity, comparable to that of large graphene sheets obtained by chemical vapor deposition methods.

A.1 Introduction

Beyond any doubt graphene has stirred the world of material research due to its unique physical properties [56,57]. In particular, in the field of electronics, always constrained by the scaling race and new integration paradigms of the semiconductor devices, graphene has found a huge niche of interest [58]. However, the expectations have not been yet materialized into real-world applications due, in part, to the difficulty to produce and pattern large graphene samples. The efficient fab-

rication of graphene layers is a critical process to achieve the expected properties at a reasonable cost. The industrial methods for producing high quality samples, beyond the experimental approach based on the 'scotch tapping' [59], mainly involve high temperature vacuum annealing of Silicon Carbide [60] or Chemical Vapor Deposition (CVD) [61]. Despite the repeatability of those methods is more than proven and the quality of the samples well demonstrated, it is also true that those methods do not fully satisfy yet the requirement for cost-effective circuit integration.

Not far from the bellwether research activity related to graphene and its two-dimensional counterparts [62], the interest around a *poorer* form of graphene, the so called reduced graphene oxide (rGO), has gained a lot of relevance due to its multiple spectrum of applications at a much lower technological effort [63–66]. Although it is far from achieving the unique properties of graphene, rGO preserves, to some extent, part of its merits (flexibility, electrical and thermal conductivity...) [67]. But the most appealing advantage of the laser-assisted photothermal reduced graphene oxide is the possibility to create large precise conductive patterns (rGO) electrically isolated by the unexposed graphene oxide areas (GO), escaping from the need for lithographic masks.

The next sections provide insights on the considerations that must be addressed to carry out simple point-contact measurements on the bare rGO films. Once the basics are established, the methodology is applied for the optimization, in terms of the electrical conductivity, of the synthesized samples. The chapter is divided in two blocks: Section A.2 summarizes the conditions under which the rGO samples have been obtained and describes the experimental methodology followed for their point-contact electrical characterization. The spectroscopic and electrical results as well as the path for the optimization of the samples are documented in Section A.3, including benchmarking with commercial graphene obtained by chemical vapor deposition. Finally, the main conclusion are drawn in Section 4.

A.2 Sample Preparation and Experimental Setup

Graphene oxide has been obtained following a modified version of the Hummers and Offerman method [154] based on the oxidation and exfoliation of natural

graphite powder through sonication in a water dispersion. This procedure yields a homogeneous dispersion, indefinitely stable, containing primarily monolayer sheets (graphene oxide). The hydrophilic nature of graphene oxide implies that water molecules can easily intersperse in the graphite oxide, causing the layer splitting [155].

Graphene oxide behaves as an electrical insulator due to the alteration suffered by the carbon atoms during the oxidation process (GO has sp^2 and sp^3 hybridized carbon atoms). The electrical conductivity can be recovered easily removing the functional groups and thus, partially restoring the original sp^2 electronic structure. Thermal annealing and hydrazine vapor reduction of GO are the two most commonly used methods to directly get conductive rGO films [156]. However, the search for safe and ecological procedures to reduce GO, points the photothermal reduction assisted by a laser as one of the most efficient processes [56,157] (Figure A.1.a).

For our experiments we synthesized 1L of 4mg/mL GO colloid. Different quantities of the dispersion were deposited on 3M® $100\mu m$-thin polyethylene terephtalate (PET) films and SiO_2/Si substrates ($90nm$ SiO_2 on highly P-type doped Si). After GO deposition, the films were left inside a class 10 cabinet on a 3D-shaker at room temperature until water was completely evaporated.

The laser-assisted photothermal reduction process was carried out by an ad-hoc laser setup mounted on a motorized in-plane platform, allowing a spacial resolution about $20\mu m$ and an effective excursion surface up to $100cm^2$ (Figure A.1.b). Two laser heads were available: the first laser features a fixed power of $4.7mW$ at a wavelength $788nm$, whereas the second system features the same mechanical characteristics with a adjustable laser power from approximately $15mW$ up to $250mW$ at a wavelength of $550nm$. The reason for using different laser sources and power intensities was to study the correlation between laser power and excursion speed during the reduction process, as well as to verify the effectiveness of the reduction at different wavelengths.

The samples fabricated for the experiments consisted of $1cm \times 1cm$ rGO squares (laterally isolated by GO) deposited whether on top of the PET film or on SiO_2/Si substrates. The process started pouring the GO colloid on a PET film (equivalent GO colloid surface concentration $100\mu L/cm^2$). Then, $1cm \times 1cm$ squares were developed by reducing the GO surface at different laser power. An

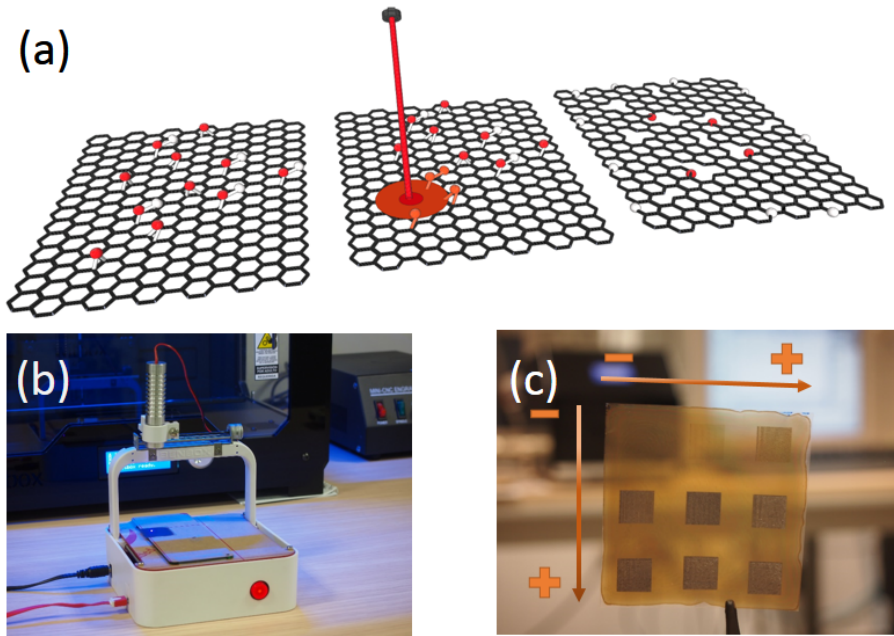

Figure A.1: (a) Illustration of GO reduction with laser diode irradiation according to the Lerf-Klinowski model [158]. Before graphene oxide thermal reduction, there is a large amount of functional hydroxyl (C-OH) and epoxyl (C-O-C) groups (left). The functional groups are broken during the reduction process (center) for obtaining the partial restoration of the graphene layers although some defects remain in the structure (right). **(b)** Image of the experimental setup based on a numerical control unit with interchangeable laser head. **(c)** An example of $1cm \times 1cm$ rGO samples on a PET substrate reduced at increasing laser power intensities, from 65mW to 105mW with an increment of 5mW in the direction of the arrows.

example of sample on PET substrate is shown in Figure A.1.c. As the GO gets more efficiently reduced, the film turns from a brownish transparent color to a dark-brown color symptomatic of the recovery of the graphitic structures.

The next objective of this work is focused on the standardization of fast and reliable electrical characterization procedures for large macroscopic samples. We centered our attention on point-contact methods to characterize the intrinsic conductivity of the material since this procedure constitutes one of the fastest approaches for monitoring the electrical properties of the samples. The experimental

setup is based on the in-line point-contact configuration [70] with direct contact of pressure-adjustable tungsten-carbide (WC) probes or ad-hoc deposited Ag contacts (the probes are placed on top of the Ag in this latter case). Two alternative measurement configurations were considered (Figure A.2):

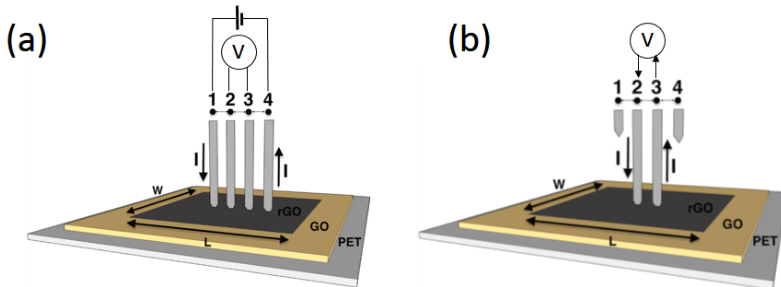

Figure A.2: **(a)** Four point-contact setup, current I is forced between probes 1 and 4 by applying a constant bias V_{1-4} while the voltage drop is measured between probes 2 and 3. **(b)** Two point-contact setup, current I and voltage V are simultaneously applied and measured through the same probes (2 and 3).

i *Four point-contact setup (4PC)*: A voltage is applied between probes 1 and 4 (V_{1-4}) while the current, I, is simultaneously measured (see Figure A.2.a). The voltage difference between probes 2 and 3 (V_{2-3}) is simultaneously monitored without current flow through them (and therefore, without voltage drop due to contact resistance). The resistance $R_{4p} = V_{2-3}/I$ obtained with this configuration can be related with the sheet resistance (R_{sh}) by the relationship $R_{sh} = FR_{4p}$, where F is a form factor depending on the sample dimensions and probes position [70]. This technique is sometimes also referred as Kelvin method [71].

i *Two point-contact setup (2PC)*: A voltage is applied between probes 2 and 3 (V_{2-3}) while the current flow through them is simultaneously measured (Figure A.2.b). This type of measurement is easier to be carried out since there is no need to take precautions regarding probe alignment, but it is affected by the impact of the contact resistance which can eventually mask the intrinsic conductivity of the sample under study [72]. Note also that even in the case that the contact resistance could be neglected, the resistance measured by the

first method may not correspond to the value given by V_{2-3}/I_{2-3} due to the current spreading. Nevertheless, the two point contact method represents a good procedure to determine the contact resistance (distance-dependent two-point probe method) [73, 74].

A.3 Results and Discussion

A.3.1 Spectroscopic characterization of laser-reduced graphene oxide

The effectiveness of the reduction process was confirmed by Raman spectroscopy (JASCO NRS-5100). This powerful and non-invasive technique can provide a large amount of information of the crystal structure related to disorder, defects, and thickness [159, 160]. The reduction process of GO can manifest itself in Raman spectra by the changes in the relative intensity of two main peaks: D and G [161]. An example is shown in Figure A.3. In the GO Raman spectrum (Figure A.3.a), the D and G peaks are located at $1352cm^{-1}$ and $1600cm^{-1}$ respectively, the 2D peak is almost non-existent. After the reduction process, Figure A.3.b and c, the D peak (related to defects and crystal distortion) is attenuated (the I_G/I_D ratio increases from $\simeq 1$ to > 1.6), and the 2D peak emerges with large intensity consequence of the partial restoration of the crystallographic structure and the reduction of the number of defects. The I_D/I_G values achieved after the reduction together with the sharpness of the peaks suggest that a thermal annealing process takes place on the rGO surface, partially healing the graphene layers [162]. The low I_{2D}/I_G ratio, and the relatively wide Full Width at Half Maximum (FWHM) (taking values from 80 to $100cm^{-1}$) reveal the multilayer nature of the samples [160]. The better ratios in Figure A.3.c, achieved despite using lower photothermal reduction power, are due to a slower excursion speed.

The elemental composition analysis was carried out by fundamental X-ray photoelectron spectroscopy (XPS, Kratos Axis Ultra-DLD) providing information about the relative levels of oxidation, C/O ratios, and the chemical environment of atoms. All spectra were calibrated with the position of the C-C peak at $284.6 \pm 0.4eV$. Figure A.4.a shows XPS spectra obtained from GO and rGO samples on SiO_2 and on PET substrates. The analysis of the area of Cs1 and

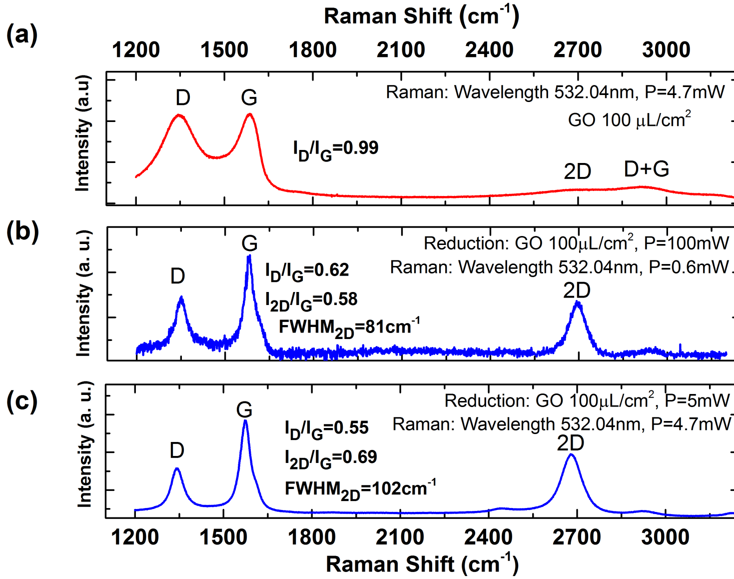

Figure A.3: Raman spectra of different samples on PET substrates: **(a)** GO before reduction, **(b)** Reduced-GO at a laser power of 100mW ($\lambda = 550nm$) at an excursion rate of $1min/cm^2$, **(c)** Reduced-GO at a laser power of 4.7mW ($\lambda = 788nm$) at an excursion rate of $24min/cm^2$

Os1 spectrum peaks provides atomic carbon to oxygen ratios (C/O) of 2.27 for the GO, 3.61 for rGO on SiO_2 and 6.36 for rGO on PET. The larger C/O ratio on the PET substrates is attributed to the different thermal conductivity of the substrates ($\sim 0.2W/mK$ for PET, $\sim 1.5W/mK$ for SiO_2). The poor heat dissipation of PET yields a more localized heat spot, favoring the reduction process, whereas the better heat dissipation of SiO_2 substrate lessens the effectiveness in the reduction process. Figure A.4.b shows the C1s spectra from the same samples of Figure A.4.a. Each spectrum is deconvoluted (CasaXPS software) into four peaks corresponding to the following functional groups: carbon sp^2 and sp^3 (C), epoxy and hydroxyls (C-O), carbonyl (C=O) and carboxylates (O-C=O) [163]. The laser reduction process decreases the oxygen-containing functional groups and recovers the carbon configurations (sp^2), confirming the results from Raman spectroscopy.

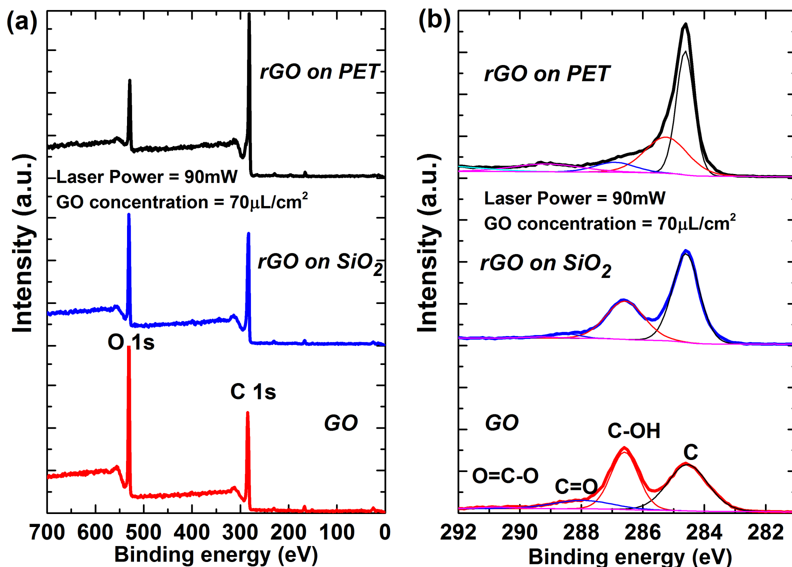

Figure A.4: XPS spectra for graphene oxide and reduced graphene oxide on PET and SiO_2 substrates: **(a)** comparison of wide spectra, **(b)** comparison of C1s peaks. The initial GO concentration before water evaporation was $70\mu L/cm^2$; the laser power, $90mW$ ($1cm^2/min$).

A.3.2 Electrical characteristics of laser-reduced graphene oxide

Prior to the measurement phase, the impact of the probe pressure on the GO surface was investigated. This initial precaution is mandatory for the 2PC setup since, as stated before (Chapter 2), the value of conductance extracted may be largely affected by the contact resistance. Figure A.5 shows the normalized conductance, when performing 2PC measurements sequentially on the same area, as a function of the WC probes load (tip radius $25\mu m$). Two samples were prepared: the first one on a PET substrate and the second on SiO_2, both starting with the same initial concentration of colloid and reduced under the same conditions. For the case of the rGO on PET the conductivity increases monotonically until saturation is achieved for a load larger than $60g$. This relationship between contact improvement and probe pressure can be related to large number of interface states created by the damage of the probe contact (amplified when increasing the probe pressure): the imperfections and induced dislocations shunt the space-charge layer; the electric field is concentrated at the edges of the probes

and the current flow is owing to field emission mechanism [164]. Additionally, due to the large number of crystal-lattice defects near the contact, the lifetime of charge carriers is extremely short in this region, so that the ohmic contact is formed due to recombination of charge carriers [164]. The situation with the rGO on SiO_2 is rather different: the relative conductance increases abruptly achieving a maximum at a load of only $20g$ and then starts to decrease for increasing loads. The different behavior is related to the nature of the *hard* SiO_2 substrate itself and consequence of the measurement procedure. The curves in Figure A.5 are obtained by successively placing the needles on the same contact points, so cumulative damage is induced easily on the harder substrate. The *soft* PET substrate can absorb more easily the needle pressure, lessening the surface damage by the substrate damping. Note that there is a large difference between the Young modulus of both substrates: $\sim 70GPa$ for SiO_2 and $\sim 2.5GPa$ for PET. This degradation phenomenon is not observed when positioning the probes on virgin surface areas; in that case, the conductivity of rGO on SiO_2 saturates for a probe load over $20g - 30g$. An example of crater created by the needle using SiO_2 substrate is shown Figure A.5 inset. All the point-contact experiments carried out on this work where performed contacting a virgin surface at a load of $70g$ for the 2PC setup, or $30g$ for 4PC or deposited Ag setups.

Typical resistance characteristics of the reduced graphene oxide are shown in Figure A.6. As observed, there is a large discrepancy between 2PC and 4PC characterization methods. We first focus on the results for 2PC. The direct contact of the WC probes on the surface yields a large value of the resistance well above the $k\Omega$ range. The value is reduced down to 190Ω when the two point-contact measurement is carried out through deposited Ag contacts. In addition, the direct contact measurement exhibits a remarkable voltage dependence revealing the nature of the field emission mechanism [165]. The difference between the values of resistance extracted using direct WC contacts and deposited Ag contacts in Figure A.6 lies in the contact resistance, dramatically high for the first case. An example of contact resistance extraction is provided in Figure A.6.b. This Figure is obtained by extracting the total resistance for several probe distances and then extrapolating it to zero probe interdistance. The residual resistance at $d = 0$ corresponds to the average resistance of probes 1 and 2, $R_{c1} + R_{c2} \approx 2R_c = 93\Omega$ [166]. The resulting contact resistance, for one single probe contacting the sample

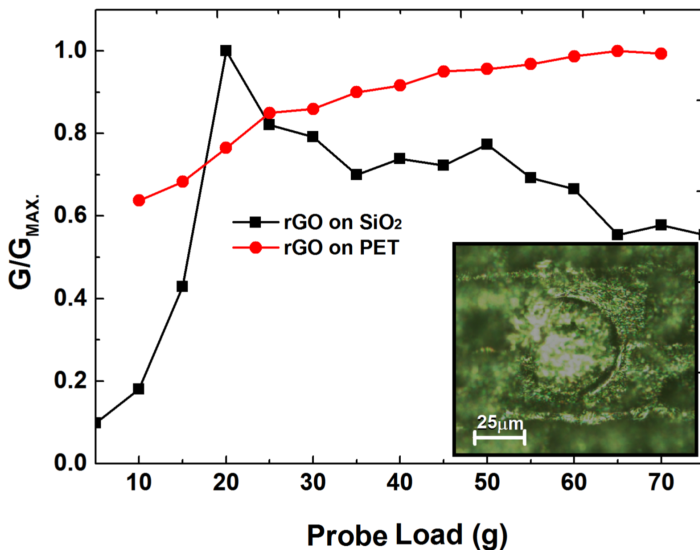

Figure A.5: Relative conductance extracted by successive 2PC measurements and direct WC contact as a function of the probe load for rGO reduced on PET and SiO_2 substrates. Inset: Microscope image of the probe crater generated by the probe.

with a deposited Ag contact, is $R_C = 46.5\Omega$. This value is much lower than that of the WC direct contact case (well above the $k\Omega$ range, which would advice against its use), but still not low enough to disclose the intrinsic properties of the rGO as the 4PC measurements will reveal. Note that this contact resistance extraction procedure is valid as long as the form factor of the current flow remains invariant with the probes distance (large rGO sample compared with the needle separation guaranteeing a linear relationship between the total two point-contact resistance, R_{2PC}, and the needles separation, d) [70].

4PC measurements, shown by open squares and open triangular symbols in Figure A.6, yield a lower value of total resistance ($\approx 80\Omega$). As exposed before, this value is not directly comparable with the 2PC value since the current flow covered by the voltage measurement differs in both cases [71]. However, the fundamental message, in terms of the standardization of the characterization protocols, is to notice how the value of resistance extracted by the 4PC method remains the

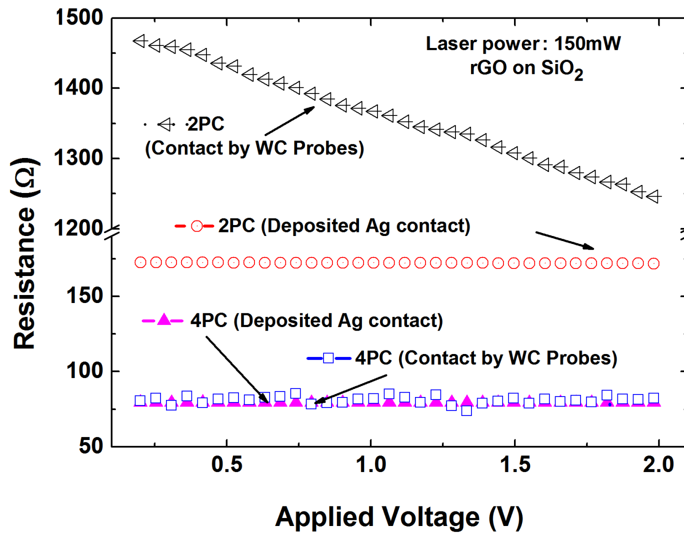

Figure A.6: Comparison of resistance extracted from 4 and 2 point-contact measurements combining direct contact of the rGO surface with the WC probes and deposited Ag contacts.

same regardless the contact approach, suppressing effectively the undesirable role of the contact resistance which is masking the intrinsic properties of the material. Notice how both 4PC curves (direct WC contact and Ag contact) yield the same resistance results in Figure A.7.b.

The corresponding extracted values of sheet resistance are shown in Figure A.7.b. Those values are obtained by multiplying the resistance by the current form factor, accounting for the sample size, and position of the probes. A detailed description of this factor can be found in [70, 167]. The value of the sheet resistance for the sample considered in Figure A.7.b, is $360\Omega/sq$. Despite both WC point-contact and Ag deposited contact generate the same value of sheet resistance, at the magnified resistance scale of Figure A.7.b, the direct point-contact leads a much more noisy measurement consequence of the large number of defects generated by the needles over the rGO contact surface. Finally, we have extracted the sheet resistance making use of its implicit definition (the resistance of a square). Ag contacts were deposited along the opposite side edges

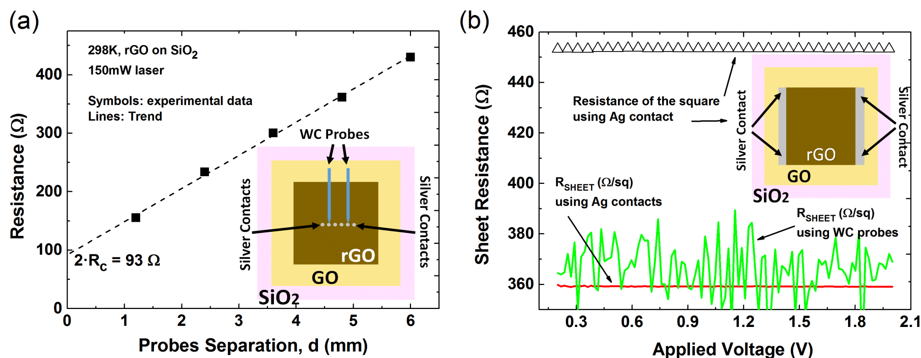

Figure A.7: (a) Example of contact resistance extraction for Ag deposited contacts by extrapolation of the 2 point-contact resistance at $d = 0$. The residual contact resistance is relatively low compared to that of direct WC contacts, explaining the differences observed in Fig. A.6. **(b)** Sheet resistance as a function of applied voltage for $1cm \times 1cm$ reduced graphene oxide sample on SiO_2 substrate with Ag deposited contacts covering opposite edges of the sample (open symbols), and 4PC measurements with direct contact of the WC probes on the rGO surface and through silver contacts (lines).

of a $1cm \times 1cm$ rGO sample. This *non-Kelvin* measurement yields a value of sheet resistance of 453 Ω/sq, about 25% larger than the one obtained by the 4PC measurement. Note that this difference corresponds, basically, with the contact resistance previously extracted for Ag contacts (Figure A.7.a).

A.3.3 Initial surface GO concentration and laser power dependencies

During the reduction process, both the laser power and the amount of deposited GO influence on the electrical properties of the resulting rGO film. The impact of the initial surface concentration of GO dispersion over the PET surface on the sheet resistance is shown in Figure A.8.a. As observed, the values of sheet resistance are scattered depending on the concentration; however, we can notice that, overall, the higher the concentration, the higher the sheet resistance after the reduction. This statement must be qualified for the extreme cases. For concentrations above $150\mu L/cm^2$ the sheet resistance saturates at values in the range from $600\Omega/sq$ to $800\Omega/sq$ approximately ($90mW$ laser power case). On the op-

posite side, we did not see improvement when reducing the concentration below $80\mu L/cm^2$. Actually, there is a point (at around $20\mu L/cm^2$, not shown in Fig. A.8.a) where the homogeneity of the samples becomes compromised and the characterization becomes ambiguous since the sheet resistance jumps to large values (over $k\Omega$). We consider that the origin of the observed behavior (at low concentration) lies in the difficulty to aggregate different flakes and therefore to restore (partially) the continuity of the polycrystalline structure of the sample by the photothermal treatment. On the other side, for the higher concentrations, only the initial layers are effectively reduced by the photothermal treatment (confirmed by mechanical exfoliation), and therefore, the improvement of the conductivity saturates.

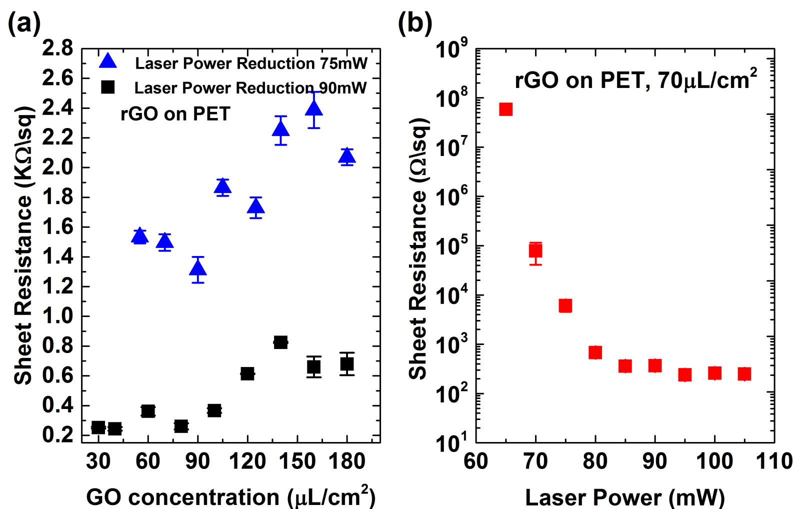

Figure A.8: (a) Sheet resistance extracted using 4PC method for $1cm \times 1cm$ samples with different initial graphene concentration (before water evaporation) for two different laser powers. **(b)** Sheet resistance of the rGO obtained with a initial surface concentration of colloid of $70\mu L/cm^2$ as a function of the laser power ($\lambda = 550nm$). Laser power above 120mW can compromise the integrity of the PET substrate at a laser excursion speed of $1cm^2/min$.

The laser power was controlled externally by a programmable power supply adjusting the laser power intensity from 30 to $250mW$ ($\lambda = 550nm$). Figure A.8.b presents results of the sheet resistance as a function of the laser power intensity. The increase in the photothermal intensity during the reduction pro-

cess boosts the conductivity, lowering the sheet resistance down to the promising value of $226\Omega/sq$. The non-linear relationship between both magnitudes (sheet resistance and laser power) eventually end-ups with the saturation of the conductivity increase. Above $95mW$, at an excursion rate of $1cm^2/min$, the increase of conductivity (decrease of resistivity) is marginal. Further power increase must be carried out with caution since it may fall outside the safe operating area of the PET substrate in terms of local heating.

A.3.4 Temperature dependence

Electrical resistivity measurements were performed for rGO samples on SiO_2 substrates from 300K to 400K under high vacuum conditions ($10^{-5}mBar$, Janis ST-500 cryostat). In this range of temperature, the samples are characterized by a non-metallic linear behavior [168]. Both 2PC (deposited Ag contacts at the opposite edge of the sample) and 4PC (Ag deposited contacts) configurations were analyzed. Experimental data in Figure A.9.a show that the trend is the same regardless the measurement configuration, being the contact resistance the only responsible for the shift of the curves. The fact that the slope of the $\rho_s(T)$ curve in the 2PC configuration is the same as in the 4PC setup, further confirms the hypothesis of the field emission as primary injection mechanism.

The experimental values of the resistance were extracted both during the heating and cooling of the samples verifying the lack of any hysteresis effect. This linear $R-T$ dependence has been studied by Sahoo et al. as a possible thermistor application of rGO [169].

A.3.5 Sample comparison

We have finished this study by comparing the sheet resistance of our rGO samples (under best reduction conditions in terms of initial colloid concentration and laser power) with that of macroscopic graphene samples produced by chemical vapor deposition methods [61] acquired from different vendors on SiO_2 and PET substrates. The results have been summarized in Figure A.10. The sheet resistance has been extracted with the 4PC configuration described in Section A.2. The values of sheet resistance extracted are well aligned with those provided by the vendors for commercial CVD graphene transferred to isolating substrates (typi-

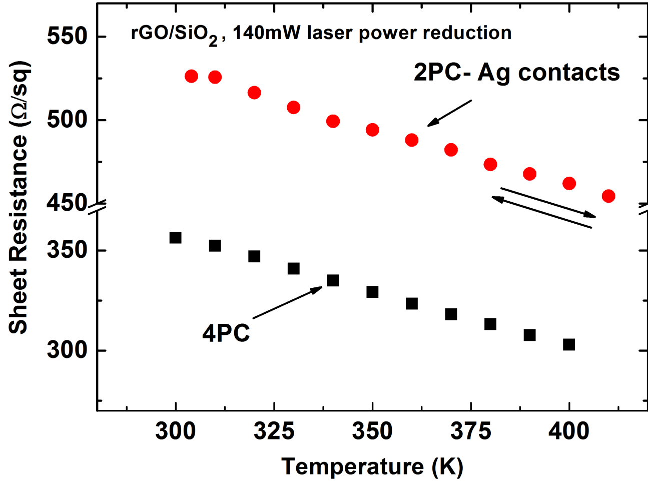

Figure A.9: Sheet resistance (ρ_s) as a function of temperature in two point-contact (2PC) and four point-contact (4PC) configurations. For the first case, the contact is carried out through deposited Ag electrodes covering two opposite edges of the sample, whereas for the 4PC case the contact is done with the WC probes on Ag deposited electrodes.

cally ranging from $500\Omega/sq$ to $1000\Omega/sq$). The more stunning message here is the good value of the sheet resistance obtained from the rGO samples, surpassing those of the CVD samples. This result reflects the goodnesses of the laser reduced GO (in terms of conductivity) once the procedure is optimized, and paves the way for its further exploration in different fields of electronics where large, flexible, inexpensive and easy patterned conductive films are needed.

A.4 Conclusion

Point-contact electrical characterization techniques have been demonstrated as a fast and reliable approach to extract the electrical properties of large macroscopic samples of laser reduced graphene oxide. The advantages and drawbacks of four point-contact and two point-contact configurations have been highlighted revealing the severe impact of the contact on the electrical characteristics. These methods have provided also a valuable feedback for the optimization of the pho-

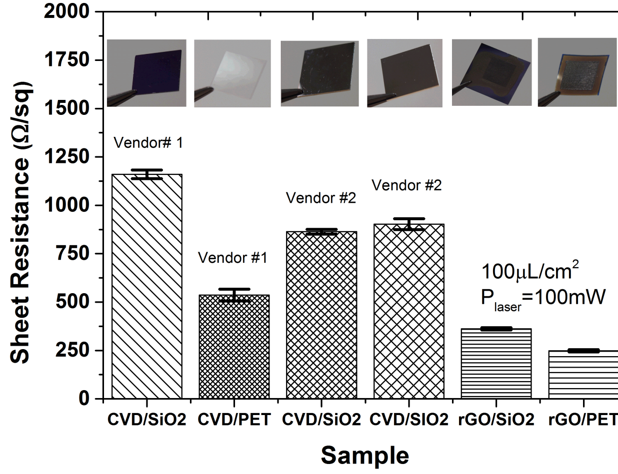

Figure A.10: Comparison of the sheet resistance, ρ_s, extracted by 4PC method from CVD graphene on PET and SiO_2 substrates acquired from commercial channels and optimized rGO samples. Characterization of two CVD samples on SiO_2 from the same vendor (Vendor 2) reflects the variability of the commercial samples

totermically assisted reduction process, allowing the selection of the best trade-off between initial colloid concentration and laser power during the reduction process. The experiments have shown that the lowest the GO concentration the better the electrical conductivity as far as the homogeneity of the layer is not compromised. On the other side, increasing the laser power intensity initially benefits the conductivity of the reduced samples before achieving a saturation regime. Against all odds the optimized rGO samples present promising values of the electrical conductivity competing with that of large commercial CVD samples.

Appendix B

List of publications

B.1 Journal papers

- C. Marquez, N. Rodriguez, F. Gamiz, A. Ohata, "Insights on the body charging by impact ionization in fully depleted SOI transistors," Submitted to Electron Device Letter, 2017.
- C. Marquez, N. Rodriguez, F. Gamiz, R. Ruiz, and A. Ohata, "Electrical characterization of Random Telegraph Noise in Fully-Depleted Silicon-On-Insulator MOSFETs under extended temperature range and back-bias operation," Solid. State. Electron., vol. 117, pp. 60–65, 2016.
- C. Marquez, N. Rodriguez, F. Gamiz, and A. Ohata, "Systematic method for electrical characterization of random telegraph noise in MOSFETs," Solid. State. Electron., Oct. 2016.
- C. Marquez, N. Rodriguez, R. Ruiz, and F. Gamiz, "Electrical characterization and conductivity optimization of laser reduced graphene oxide on insulator using point-contact methods," RSC Adv., vol. 6, no. 52, pp. 46231–46237, 2016.
- C. Fernandez, N. Rodriguez, C. Marquez, A. Ohata, and F. Allibert, "On the effective mobility extraction by point-contact techniques on silicon-on-insulator substrates," J. Appl. Phys., vol. 117, no. 3, p. 35707, Jan. 2015.
- N. Rodriguez, F. Gamiz, C. Navarro, C. Marquez, F. Andrieu, O. Faynot, and S. Cristoloveanu, "Experimental developments of A2RAM memory cells

on SOI and bulk substrates," Solid. State. Electron., vol. 103, pp. 7–14, Jan. 2015.

- C. Marquez, N. Rodriguez, J.M. Montes, R. Ruiz, F. Gamiz, C. Sampedro, A. Ohata, "Direct Characterization of Impact Ionization Current in Silicon-on-Insulator Body-Contacted MOSFETs," ECS Trans., vol. 66, no. 5, pp. 93–99, May 2015.

- C. Marquez, N. Rodriguez, C. Fernandez, A. Ohata, F. Gamiz, F. Allibert, and S. Cristoloveanu, "In Situ Characterization of Bias Instability in Bare SOI Wafers by Pseudo-MOSFET Technique," IEEE Trans. Device Mater. Reliab., vol. 14, no. 3, pp. 878–883, Sep. 2014.

B.2 Conference contributions

- C. Marquez, N. Rodriguez, F. Gamiz, and A. Ohata, "Electrical characterization of Random Telegraph Noise in back-biased Ultrathin Silicon-On-Insulator MOSFETs," 2016 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS). pp. 40–43, 2016.

- C. Marquez, N. Rodriguez, R. Ruiz, and F. Gamiz, "Correlation between critical parameters of laser reduced graphene oxide and its electrical properties," Poster contribution, Graphene Flagship-Graphene Study, pp. 16, Les Houches, France, 2016.

- C. Marquez, N. Rodriguez, R. Ruiz, and F. Gamiz, "Electrical Properties of Laser Reduced Graphene Oxide," Graphene Canada 2015, Montreal, Canada, 2015.

- C. Fernandez, N. Rodriguez, C. Marquez, and F. Gamiz, "Determination of ad hoc deposited charge on bare SOI wafers," in EUROSOI-ULIS 2015: 2015 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon, 2015, no. 2, pp. 289–292.

- V. Velayudhan, J. Martin-Martinez, M. Porti, R. Rodriguez, M. Nafria, X. Aymerich, C. Marquez, and F. Gamiz, "Threshold voltage and on-current

Variability related to interface traps spatial distribution," in European Solid-State Device Research Conference, 2015, vol. 2015–Novem, pp. 230–233.

- F. Gamiz, N. Rodriguez, C. Marquez, C. Navarro, and S. Cristoloveanu, "A2RAM: Low-power 1T-DRAM memory cells compatible with planar and 3D SOI substrates," in 2014 SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2014, pp. 1–2.
- L. Segura, N. Rodriguez, C. Fernandez, A. Ohata, C. Marquez, and F. Gamiz, "Direct Electrical Characterization of Graphene-On-Insulator by Multiple-Point Contact Configuration," in graphene 2014, 2014, no. 1, pp. 2–3.
- N. Rodriguez, F. Gamiz, C. Marquez, C. Navarro, F. Andrieu, O. Faynot, and S. Cristoloveanu, "Fabrication and validation of A2RAM memory cells on SOI and bulk substrates," in 2013 5th IEEE International Memory Workshop, 2013, pp. 135–138.
- C. Marquez, N. Rodriguez, C. Fernandez, A. Ohata, F. Gamiz, F. Allibert, and S. Cristoloveanu, "Direct point-contact characterization of Bias instability on bare SOI wafers," 2013 IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf., pp. 1–2, Oct. 2013.

B.3 Book chapters

- N. Rodriguez, R. J. Ruiz, C. Marquez, and F. Gamiz, "Scribing Graphene Circuits," in Future Trends in Microelectronics, S. Luryi, J. Xu, and A. Zaslavsky, Eds. Hoboken, NJ, USA: John Wiley and Sons, Inc., 2016, pp. 207–216.
- F. Gámiz, N. Rodriguez, C. Navarro, C. Marquez, and S. Cristoloveanu, "Tri-Dimensional A2-RAM Cell: Entering the Third Dimension," in Functional Nanomaterials and Devices for Electronics, Sensors and Energy Harvesting, A. Nazarov, F. Balestra, V. Kilchytska, and D. Flandre, Eds. Cham: Springer International Publishing, 2014, pp. 105–124.

Appendix C

Short summaries

C.1 English

The aim of the work herein presented in this PhD thesis is to study, through the electrical characterization, the reliability issues derived from the scaling down of the state-of-the-art Silicon-On-Insulator transistors. The miniaturization of the dimensions of the transistor has been the trend which semiconductor industry has followed in order to increase the number of devices per chip and, subsequently, the performance of the circuit. However, the reduction of the gate oxide thickness and the gate length, mandatory to follow the scaling rules, have implied the introduction of new dielectric materials and device structures. These advances have also introduced new instability sources which may affect the performance and the reliability of the devices.

The first reliability issue studied in this PhD thesis is the bias instability, which affects the electrical characteristics of a MOS transistor when the gate is stressed with relatively high voltage. In this context, the instabilities of bare SOI wafers are characterized by using a point-contact method know as Pseudo-MOS technique. This characterization technique permits to study both negative and positive bias stress in electron and hole channels. The comparison of SOI wafers with different film thicknesses and surface quality, together with fully processed MOSFETs, have pointed out the origin of the instability to be the interface between the native (spontaneous) oxide and the channel. The results allow the semiconductor manufacturer to pay more attention to the areas most vulnerable to sources of instability.

Another instability source, directly derived from the introduction of new dielectric materials as gate oxide and the reduction of the signal levels, is known as Random Telegraph Noise. This effect is explained by the stochastic trapping/detrapping behavior of the carriers of the channel into the switching oxide traps in dielectrics. In this work, a new protocol to study the Random Telegraph Noise in state-of-the-art Silicon-On-Insulator transistor is introduced. The protocol combines both a current-time scanning characterization and a low-frequency noise spectral density characterization, to identify the single-trap Random Telegraph Noise devices in optimum bias conditions. This experimental method has allowed to monitory the distribution of traps over the transistors on wafer, to determine the physical characteristics of the trap, to study the effect of the temperature on the characteristic times and, to characterize the impact of the substrate bias on the Random Telegraph Noise fluctuation.

The reduction of the gate length of the transistor has allowed to introduce more devices in the same area, however, if the supply-voltages are not reduced, to hold the voltage compatibility with older circuit technologies, the electric fields in the transistor increase. The increment in the lateral electric field implies the appearance of some reliability issues, usually known as short channel effects. Impact ionization is one of these effects, where the highly energetic electrons, which move from the source to the drain, knock electrons out of their bound state and promote them to a state in the conduction band, creating electron-hole pairs. In this PhD thesis impact ionization has been characterized in state-of-the-art Silicon-On-Insulator transistors. The study has been carried out in specifically fabricated five-terminal transistors with body-contact. This structure overcomes the fact that Silicon-On-Insulator structures do not permit a direct contact with the channel of the transistor due to the buried oxide. In this context, thin and ultra-thin body-contacted transistors have been characterized revealing the large influence of the channel length of the device on the body potential. A severe loss of electrostatic control of the body by the gate due to hole injection has been pointed out. Additionally, the dependence of the impact ionization with the substrate bias has been studied.

Finally, electrical characterization of laser-assisted reduced graphene oxide is carried out by using point-contact techniques. The experiments shed light on the role of the point-contact when extracting the intrinsic resistivity of the material.

The study reveals that the final optimized reduced graphene oxide samples present a promising conductivity, comparable to that of large graphene sheets obtained by chemical vapor deposition methods.

C.2 Español

El objetivo principal del trabajo que se presenta en esta tesis es estudiar, mediante la caracterización eléctrica, los efectos de inestabilidad derivados del escalado en los dispositivos de silicio sobre aislante de última tecnología. La miniaturización de las dimensiones de los transistores ha sido la tendencia que la industria semiconductora ha seguido para aumentar el número de dispositivos por chip, y por tanto, el rendimiento de los circuitos electrónicos. Sin embargo, la reducción del espesor del óxido de puerta y de la longitud de puerta, necesarios para continuar con las reglas de escalado, han implicado la introducción de nuevos materiales dieléctricos y el diseño de nuevas estructuras de dispositivo. Sin embargo, hay que tener en cuenta que estos avances también introducen fuentes de inestabilidad que pueden afectar el comportamiento y la fiabilidad de los dispositivos.

La primera fuente de inestabilidad estudiada en esta tesis doctoral es el efecto de inestabilidad por polarización. Este modifica la característica eléctrica del transistor MOS cuando el termial de puerta es estresado con un voltaje relativamente alto. En este punto, las inestabilidades de polarización se han caracterizado en obleas no procesadas de silicio sobre aislante usando el método de puntas de contacto, conocido como técnica Pseudo-MOS. Esta técnica de caracterización permite estudiar tanto estrés de polarización positivo como negativo, en dispositivos de canal de electrones y de huecos. La comparación de los resultados en obleas de silicio sobre aislante con diferentes espesores y calidades en la superfice, con dispositivos MOSFETs procesados, ha permitido determinar el origen de la inestabilidad. Estos resultados permiten a la industria del semiconductor poner la atención en las áreas críticas del dispositivo afectadas por efectos de inestabilidad.

Otra fuente de inestabilidad, consecuencia de la introducción de nuevos materiales dieléctricos como óxido de puerta y de la reducción de los niveles de señal, es conocida como ruido del telegrafista. Este efecto es producido por el atrapamiento/desatrapamiento de portadores del canal en las trampas del óxido. En este trabajo se introduce un nuevo protocolo para estudiar el ruido del telegrafista en dispositivos de silicio sobre aislante de última tecnología. El protocolo combina tanto la caracterización de la corriente en función del tiempo como el escaneo de la potencia del ruido a baja frecuencia, para identificar dispositivos afectados por una trampa y su polarización óptima. Este método experimental ha permitido

monitorizar la distribución de trampas en los dispositivos a lo largo de la oblea, determinar las características físicas de las trampas, estudiar los efectos de la temperatura en los tiempos de las mismas y caracterizar el impacto de la polarización de substrato.

La reducción de la longitud de puerta del transistor ha permitido introducir más dispositivos en el mismo área, sin embargo, si los voltajes de alimentación no se reducen de la misma forma, manteniendo la compatibilidad con tecnologías anteriores, el campo eléctrico lateral en el dispositivo aumenta. Este incremento implica la aparición de efectos de inestabilidad, comúnmente conocidos como efectos de canal corto. La ionización por impacto es uno de estos efectos, donde los electrones con alta energía, que van desde la fuente al drenador, golpean otros electrones desplazándolos hasta la banda de conducción, generando pares de electrón-hueco. El estudio de ionización por impacto se ha llevado a cabo en dispositivos de cinco terminales especialmente fabricados con un contacto de cuerpo, para poder acceder hasta el cuerpo del transistor, al no ser posible acceder al mismo en las estructura de silicio sobre aislante comunes debido al oxido enterrado. De esta forma, se han caracterizado dispositivos delgados y ultra-delgados revelando una gran influencia de la longitud del dispositivo en la evolución del potencial del cuerpo del transistor. Remarcable es también la pérdida de control electroestático del cuerpo del dispositivo en decremento del terminal de puerta, debido a la inyección de huecos. Por último, la dependencia de la ionización por impacto con la polarización de substrato se ha analizado.

Para finalizar, se ha llevado a cabo la caracterización eléctrica de óxido de grafeno reducido mediante laser a través de la técnica de puntas de contacto. Los experimentos arrojan luz sobre la dependencia de las puntas de contacto en la resistividad intrínseca del material. De hecho, se demuestra como una muestra optimizada de óxido de grafeno reducido es comparable, eléctricamente, con una muestra macroscópica obtenida mediante métodos de deposición química en fase de vapor.

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