UNIVERSIDAD DE GRANADA

CENTRO DE INVESTIGACIÓN EN TECNOLOGÍAS DE LA INFORMACIÓN Y LAS COMUNICACIONES

PROGRAMA DE DOCTORADO EN FÍSICA Y CIENCIAS DEL ESPACIO
DOCTORAL THESIS

Application of the Pseudo-MOSFET Technique on Silicon-On-Insulator Wafers

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A thesis submitted in fulfilment of the requirements
for the Doctor degree

at the

Nanoelectronics Research Group
Departamento de Electrónica y Tecnología de Computadores

21st May, 2016

Editor: Universidad de Granada. Tesis Doctorales
Autora: Cristina Fernández Sánchez
ISBN: 978-84-9163-010-4
URI: http://hdl.handle.net/10481/44457

Abstract

Keywords

Pseudo-MOSFET, SOI, Split-C(V), effective capacitance area, effective field, carrier mobility, FD-SOI MOSFETs, Graphene-On-Insulator, sensor platform.

Abstract

This work has been focused on a deep and systematic study of the point-contact Pseudo-MOSFET characterization technique.

Firstly, theoretical models for the Pseudo-MOSFET have been described and developed for ultrathin Si wafers, and for those with also ultrathin BOX. They have been validated with several simulations. Then, some Pseudo-MOSFET samples with different thickness and surface (passivated/non-passivated) have been analyzed and characterized.

Later, the combination of the Split-C(V) technique with the Pseudo-MOSFET configuration has allowed to obtain the carrier mobility in bare SOI wafers as a function of the inversion charge. Nevertheless, since the evaluation of this parameter depends strongly on the value of the effective area considered for calculations, this area has been examined as a function of the characteristics of the set up configuration.

Taking into account the variability of the area with experimental configuration parameters, a mathematical model has been proposed to calculate the effective surface in any characterization scenario. The model has been verified with the experimental results.

On the other hand, the carrier mobility have been also studied in Pseudo-MOSFET samples. In order to achieve the optimum enhancement for the mobility, the specific values for the back-gate bias have been calculated using Poisson-Schrödinger numerical simulations combined with Split-C(V) experimental results.

To conclude, new applications associated to point-contact techniques have been analyzed such us the use of the Pseudo-MOSFET as a sensor platform. In addition, several studies have been carried out on Poly-silicon or Graphene-On-Insulator samples demonstrating the flexibility of the point-contact methods to evolve with emerging substrates.

Resumen

Palabras clave

Pseudo-MOSFET, SOI, Split-C(V), área efectiva, campo eléctrico efectivo, movilidad, FD-SOI MOSFETs, Graphene-On-Insulator, plataforma sensora.

Resumen

El trabajo presentado ha consistido en un amplio y sistemático estudio sobre la técnica de caracterización eléctrica denominada Pseudo-MOSFET.

Inicialmente, se describieron y desarrollaron modelos teóricos para obleas Pseudo-MOS con láminas de Si ultradelgadas, así como para aquellas con BOX ultradelgados. Estos modelos se validaron con varias simulaciones. Más adelante, numerosas muestras de Pseudo-MOSFETs con diferentes espesores y superficies (pasivada/no pasivada) fueron analizadas y caracterizadas experimentalmente.

Posteriormente, la combinación de la conocida técnica Split-C(V) con la configuración Pseudo-MOSFET permitió obtener la movilidad de los portadores en una oblea SOI a través del valor de la carga de inversión. No obstante, ya que la evaluación de este parámetro depende en gran medida del área efectiva, dicha área fue examinada y calculada según las características de la configuración experimental.

Teniendo en cuenta la variabilidad del área con los parámetros asociados a la configuración experimental, se ha propuesto un modelo matemático que permite calcular la superficie efectiva usando cualquier configuración en el Pseudo-MOSFET. Dicho modelo ha sido validado con resultados de laboratorio.

Por otro lado, la movilidad de los portadores en obleas SOI ha sido también estudiada. Así pues, con el fin de conseguir el valor óptimo de la movilidad, se calcularon las tensiones de puerta con las que polarizar el Pseudo-MOSFET usando simulaciones numéricas y combinándolas con resultados experimentales de Split-C(V).

Para terminar, se analizaron nuevas aplicaciones asociadas a las técnicas de puntas de contacto, tales como el uso del Pseudo-MOSFET como plataforma sensora. Además, otros estudios sobre obleas de Poly-Si o Grafeno-sobre-Aislante se llevaron a cabo demostrando así la flexibilidad de estos métodos para evolucionar con los nuevos sustratos emergentes.

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Declaration of Authorship

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CERTIFY:

that the research work contained in the present report, entitled **Application of the Pseudo-MOSFET Technique on Silicon-On-Insulator Wafers**, has been performed under the full guidance of the Ph.D. supervisors and, as far as our knowledge reaches, during the work, it has been respected the rights of others authors to be cited, when their publications or their results have been used.

Granada, 21st May, 2016.

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“ *There is a will, there is a way.*”
Anonymous

Contents

Declaration of Authorship **vii**

Contents **xi**

List of Figures **xv**

List of Tables **xxiii**

Abbreviations **xxv**

1 Introduction to SOI Materials and Devices **1**
- 1.1 Motivations . . . 1
- 1.2 SOI wafers fabrication . . . 3
  - 1.2.1 Separation by IMplatation OXygen, SIMOX . . . 4
  - 1.2.2 Bond-And-Etch-Back, BESOI . . . 5
  - 1.2.3 Epitaxial Layer TRANsfer, ELTRAN . . . 6
  - 1.2.4 Smart-Cut^{TM} . . . 7
- 1.3 Advantages of SOI technology . . . 8
- 1.4 SOI devices classification . . . 9
- 1.5 SOI wafers characterization . . . 10
  - 1.5.1 Four-point probe . . . 10
  - 1.5.2 Two-point probe . . . 11
  - 1.5.3 Second Harmonic Generation, SHG . . . 12
- 1.6 Defects of SOI materials . . . 13
- 1.7 Conclusions . . . 14

2 Electrical Characterization of Bare SOI Wafers **15**
- 2.1 The Pseudo(Ψ)-MOSFET technique . . . 15
  - 2.1.1 Principle and operation . . . 15
  - 2.1.2 Methodology . . . 16
  - 2.1.3 Static characteristics . . . 16
  - 2.1.4 Y-function . . . 18
- 2.2 Theoretical models for ultrathin passivated Ψ-MOSFETs . . . 19
  - 2.2.1 Two-interfaces model . . . 19
    - 2.2.1.1 Model for passivated Ψ-MOSFET . . . 22
    - 2.2.1.2 Model for non-passivated Ψ-MOSFET . . . 23
  - 2.2.2 Three-interfaces model . . . 23

2.2.2.1 Analytical model . . . 24
2.2.2.2 Capacitive model . . . 25
2.3 Impact of the setup parameters on experimental current characteristics . . . 27
2.3.1 Implications by changing the probe pressure . . . 27
2.3.2 Implications of changing the probes interdistance . . . 28
2.3.3 Measurements on different cells . . . 29
2.3.4 Implications of repeating the measurement . . . 32
2.4 Conclusions . . . 34

3 Novel Insights In Pseudo-MOSFET Technique 35
3.1 Capacitance measurements . . . 35
3.1.1 C-V characteristics . . . 36
3.2 Impact of experimental conditions on capacitance curves . . . 38
3.2.1 Variation of the AC input signal level . . . 39
3.2.2 Variation of the probes pressure . . . 39
3.2.3 Variation of the number of probes and the probe spacing . . . 42
3.2.4 Variation of the BOX layer thicknesses. Substrate effect . . . 42
3.3 The Split-C(V) technique . . . 44
3.4 The effective area in point-contact capacitance measurements . . . 44
3.4.1 Impact of the frequency on S_{eff} . . . 45
3.4.2 Relation between C_{BOX} and S_{eff} . . . 46
3.4.3 Carrier density determination . . . 47
3.4.4 Model development . . . 48
3.4.5 Simulation results . . . 51
3.4.6 Experimental results . . . 52
3.4.6.1 Two-needle configuration . . . 52
3.4.6.2 Three-needle configuration . . . 53
3.4.7 Extraction of μ_{eff} . . . 54
3.5 Conclusions . . . 55

4 Effective Mobility Extraction in Bare SOI Substrates 57
4.1 Introduction . . . 57
4.2 The role of the top-interface on the effective electric field . . . 58
4.2.1 Discussion of the electrostatic potential . . . 59
4.2.2 Effective electric field model . . . 61
4.3 Results on mobility . . . 63
4.4 Conclusions . . . 67

5 Applications of Point-Contact Techniques 69
5.1 Poly-silicon samples . . . 69
5.1.1 Electrical characterization . . . 69
5.1.1.1 Dependence on the probe pressure . . . 70
5.1.1.2 Dependence on the drain voltage . . . 70
5.1.1.3 Dependence on delay time . . . 71
5.1.1.4 Mobility results . . . 72
5.2 Graphene-On-Insulator samples . . . 73
5.2.1 Methodology . . . 73

5.2.2 I-V characteristics . . . 75
5.2.2.1 Initial calibration . . . 75
5.2.2.2 Impact of the substrate bias . . . 75
5.2.2.3 Resistance measurements . . . 76
5.2.2.4 Obtaining of the carrier mobility . . . 78
5.2.3 C-V characteristics . . . 80
5.3 Determination of ad hoc deposited charge on bare SOI wafers . . . 80
5.3.1 Development of the model . . . 81
5.3.2 Experimental results . . . 83
5.4 Conclusions . . . 85

6 Conclusions and Future Steps 87
6.1 Main achievements . . . 87
6.2 Future research topics . . . 88

A Expansion of the Effective Mobility Study to FD-MOSFETs 89
A.1 Introduction . . . 89
A.2 Fully-Depleted SOI transistors . . . 89
A.3 Return point of effective field . . . 89
A.4 Map of bias regions . . . 92
A.4.1 Ultrathin FD-SOI transistors . . . 92
A.4.2 Thick-BOX FD-SOI transistors . . . 94
A.5 Conclusions . . . 95

B Nanoelectronics Laboratory 97
B.1 Introduction . . . 97
B.1.1 Semiconductor device parameter analyzer . . . 97
B.1.2 Parameter analyzer . . . 98
B.1.3 Triaxial cables . . . 99
B.1.4 Impedance analyzer . . . 100
B.1.5 JANDEL universal probe station . . . 101
B.1.6 Janis probe station . . . 101
B.1.7 BNC-Triaxial adapters . . . 102
B.1.7.1 Pseudo-MOSFET samples . . . 103
B.1.8 Semi-automatic probe system . . . 103
B.1.9 Microscope . . . 104

C Fabrication Process of Pseudo-MOSFET Samples 107
C.1 Description of the procedure . . . 107
C.1.1 Step 1. Cut the wafer into samples . . . 108
C.1.2 Step 2. Photolithography . . . 109
C.1.3 Step 3. Reactive-Ion Etching (RIE) of Silicon Dioxide . . . 111
C.1.4 Step 4. Removal of the residual resin . . . 111
C.2 Characterization of the samples achieved . . . 111
C.2.1 I-V characteristics as a function of the probe diameter . . . 112
C.2.2 Successive measurements on the same cell . . . 114

C.2.3 I-V measurements with different probe inter-distances 114
C.2.4 C-V Measurements with different probe inter-distances 114
C.2.5 Obtaining of the carrier mobility 116

D List of publications **117**

Bibliography **119**

List of Figures

1.1 Cross section of the superficial layer in a bulk wafer. 2
1.2 Effect of the ionizing radiation in bulk and SOI wafers. 2
1.3 Types of SOI structures: (a) when the Si layer is created directly on a substrate, and (b) when a insulator is formed inside a Si substrate. 3
1.4 The principle of SIMOX: a heavy-dose oxygen implantation into silicon followed by a very high temperature annealing step produces a buried layer of Silicon dioxide, below a thin crystalline Si film [HRK$^+$87]. 4
1.5 Schematic representation of BESOI process for SOI wafer manufacturing [GR93]. 5
1.6 Schematic representation of ELTRAN process for SOI wafer manufacturing [YSS94]. 7
1.7 Schematic illustration of the fabrication steps for a standard Unibond SOI wafer with Smart-Cut^{TM} technique [CC03]. 8
1.8 Schematic of a partially (a) and a fully (b) depleted SOI MOSFET. 9
1.9 Schematic of the 4-point probe setup. 10
1.10 Ψ-MOSFET configuration with (a) metallic pressure probes, or (b) mercury probes. 11
1.11 Energy levels diagram involved in SHG process [APL$^+$07]. 12
1.12 Schematic of the Second Harmonic Generation technique. 12
1.13 When the Silicon is bounded to an oxide, a region of defects is automatically originated at the interface. 14

2.1 A P-type $\Psi-$transistor operating in strong (a) accumulation (hole channel) and (b) inversion regime (electron channel). 16
2.2 The Jandel Universal probe station used to perform point-contact measurements is connected to the Agilent B1500A semiconductor analyzer through triaxial cables. 17
2.3 The Pseudo-MOSFET technique is applied to SOI wafers divided in 5 mm × 5 mm island and separated each other by 2 mm wide trenches of SiO_2. 17
2.4 Examples of $I_D(V_G)$ and $g_m(V_G)$ experimental characteristics which demonstrate the ambipolar behavior of a Pseudo-transistor. Non-passivated wafer, $t_{Si} = 88$ nm, $t_{BOX} = 145$ nm, $V_D = 20$ mV. 18
2.5 Comparison between experimental values of threshold voltage in (circles) passivated and (squares) non-passivated samples [HAHC07] and the conventional Pseudo-MOSFET model [CML00]. 20
2.6 Ψ-MOSFET energy-band diagram for positive values of V_G. The substrate-BOX interface is ignored in this first approach. 20
2.7 In-depth potential profiles from BOX interface to free surface for a 16nm-thick Ψ-MOSFET. (a) Passivated surface with quasi-flat profiles. (b) Non-passivated surface with linear potential variation. Profiles at threshold are presented with dashed line. $N_A = 10^{15} cm^{-3}$, $t_{BOX} = 145$ nm. 21

2.8 Electric field profiles from BOX interface to free surface for a 16nm-thick Ψ-MOSFET with (a) passivated surface and (b) non-passivated surface. Profiles at threshold are presented with dashed line. $N_A = 10^{15} cm^{-3}$, $t_{BOX} = 145$ nm. . . . 21

2.9 In-depth potential profiles from free surface to BOX interface in a Ψ-MOSFET for a certain gate bias upper to threshold voltage. Different trap charges at the top surface have been considered. $N_A = 10^{15} cm^{-3}$, $t_{Si} = 20$ nm, $t_{BOX} = 145$ nm. 22

2.10 Threshold voltage versus film thickness. Comparison between models and experimental data: (squares) non-passivated surface with $D_{it2} = 2 \times 10^{13} cm^{-2} eV^{-1}$ and (circles) passivated surface with $D_{it2} = 2 \times 10^{11} cm^{-2} eV^{-1}$. $D_{it1} = 2 \times 10^{11} cm^{-2} eV^{-1}$, $t_{Si} = 20$ nm, $t_{BOX} = 145$ nm. 23

2.11 Relative error calculated from threshold voltages obtained through simulations when third interface BOX-substrate is accounted for and when is not (adapted from [RCM+11]). 24

2.12 Ψ-MOSFET energy-band diagram for positive values of V_G taking into account the effect of BOX-substrate interface (D_{it3}). 24

2.13 Equivalent three-interface capacitance model of a Ψ-MOSFET: (a) general and (b) simplified circuit (after associating some capacitances). 25

2.14 Threshold voltage versus Si film thickness. Comparison of the two models described for ultrathin BOX and the existing two-interface model explained in Section 2.2.1 with experimental data from non-passivated wafers. $D_{it1} = 2 \times 10^{11} cm^{-2} eV^{-1}$, $D_{it2} = 2 \times 10^{13} cm^{-2} eV^{-1}$, $D_{it3} = 10^{11} cm^{-2} eV^{-1}$. 26

2.15 Variation of (a) the threshold voltage and (b) the peak value for the transconductance as a function of the probe pressure when an electron channel is induced in two of non-passivated samples. $V_D = 20$ mV 27

2.16 Current characteristics obtained as a function of the gate bias. At 80g the needles penetrate totally into the substrate. $t_{Si} = 88$ nm, $t_{BOX} = 25$ nm, $V_D = 20$ mV. . 28

2.17 (Left) Distance between probes selection. (Right) Current characteristics obtained as a function of the gate bias for different probe interdistances. Non-passivated wafer, $t_{Si} = 88$ nm, $t_{BOX} = 145$ nm, $V_D = 20$ mV, P = 80 g. 29

2.18 Current characteristics obtained as a function of the gate bias for the samples: (a) 1-A ($t_{Si} = 17.3$ nm, $t_{BOX} = 146.9$ nm); (b) MU003 ($t_{Si} = 12$ nm, $t_{BOX} = 145$ nm, Non-passivated surface), and (c) MU005 ($t_{Si} = 12$ nm, $t_{BOX} = 145$ nm, Passivated surface). $V_D = 20$ mV, P = 80 g. 30

2.19 Histograms associated to the threshold voltages extracted from I-V characteristics for (a)-(c)-(e) holes and (b)-(d)-(f) electron channels. Samples: (a)-(b) 1-A ($t_{Si} = 17.3$ nm, $t_{BOX} = 146.9$ nm); (c)-(d) MU003 ($t_{Si} = 12$ nm, $t_{BOX} = 145$ nm, Non-passivated surface), and (e)-(f) MU005 ($t_{Si} = 12$ nm, $t_{BOX} = 145$ nm, Passivated surface). $V_D = 20$ mV, P = 80 g. 31

2.20 Histograms associated to the carrier mobility extracted from I-V characteristics for (a)-(c) holes and (b)-(d) electron channels. Samples: (a)-(b) MU003 ($t_{Si} = 12$ nm, $t_{BOX} = 145$ nm, Non-passivated surface), and (c)-(d) MU005 ($t_{Si} = 12$ nm, $t_{BOX} = 145$ nm, Passivated surface). $V_D = 20$ mV, P = 80 g. 32

2.21 Fifty consecutive current characteristics extracted as a function of the gate bias for two different wafers at the same location. (a) Non-passivated and (b) passivated wafers. $t_{Si} = 88$ nm, $t_{BOX} = 145$ nm, $V_D = 20$ mV. 33

2.22 Cumulative representations of V_{TH-H} and V_{TH-E} for two samples. (a) Non-passivated and (b) passivated wafer. $t_{Si} = 88$ nm, $t_{BOX} = 145$ nm, $V_D = 20$ mV, P = 80 g. 33

3.1 The SOI sample can be treated as a capacitor formed by the BOX and the Silicon layers. The direction of the electric field depends on the polarity of the DC bias applied through the impedance analyzer. 36
3.2 Schematic of the configurations used for the extraction of the (a) gate-to-channel and (b) gate-to-substrate capacitance in bulk MOSFETs. The connection of the low and high potentials are pointed out in each case. (c) Comparison with the SOI wafer case. 36
3.3 C-V relation for an n-channel MOS capacitor as a function of the bias applied to the gate. 37
3.4 Experimental setup of how capacitance measurements were adapted to the Pseudo-MOSFET configuration. 38
3.5 Gate-to-channel capacitance curves obtained using a two-needle configuration when the AC level is modified from 20 mV to 50 mV (step 10 mV). Non-passivated wafer, t_{Si} = 88 nm, t_{BOX} = 145 nm. 39
3.6 (a) Maximum capacitance values at 100Hz and (b) threshold voltages for hole and electron channels obtained as a function of the probe pressure in a two-needle configuration. Non-passivated wafer, t_{Si} = 88 nm, t_{BOX} = 145 nm, Freq. 100 Hz. 40
3.7 (a) Equivalent impedance circuit associated to a Pseudo-MOS structure. (b) Simplified impedance model used in this work. 41
3.8 Capacitance curves measured using one needle on the surface as a function of the excitation signal frequency from 40 Hz to 60 MHz. 41
3.9 Experimental capacitance characteristics with: case (i), one needle on the surface; case (ii), two needles on the surface separated d = 1.59 mm; and case (iii), d = 3.18 mm; case (iv), three needles separated d = 1.59 mm. Non-passivated wafer, t_{Si} = 88 nm, t_{BOX} = 145 nm, oscillation level 20 mV. 42
3.10 (a) When the frequency is high enough, a depletion region in the substrate of a SOI wafer appears. (b) Electrical equivalent circuit. 43
3.11 Comparison between C-V curves at 600Hz for two Pseudo-MOSFET samples: (line) t_{Si} = 83 nm, t_{BOX} = 35 nm; (line + symbols) t_{Si} = 88 nm, t_{BOX} = 145 nm. 43
3.12 (a) Gate-to-channel capacitance curves as a function of the substrate bias obtained for different frequencies using one needle on the surface. (b) Maximum value of the curves obtained as a function of the frequency. Non-passivated wafer, t_{Si} = 88 nm, t_{BOX} = 145 nm, oscillation level 20 mV. 45
3.13 (a) Variation of the capacitance characteristics when the wafer is illuminated and when it is not. (b) Gate-to-channel capacitance curves as a function of the substrate bias obtained by the impedance analyzer at 300 Hz (dashed lines) and by QSC measurements (continuous line). Non-passivated wafer, t_{Si} = 88 nm, t_{BOX} = 145 nm, oscilation level 20 mV. 46
3.14 (a) Frequency dependence of Q_{inv} with the substrate bias. The difference of Q between 300 Hz and 1 kHz is within 2.1%. (b) Experimental data of Q_{inv} and the linear fitting extrapolated from the region between V_{SUB} = 15 V and V_{SUB} = 20 V. Non-passivated wafer, t_{Si} = 88 nm, t_{BOX} = 145 nm, oscillation level 20 mV. . 47
3.15 (a) Electron concentration simulated by ATLAS taking into account real dimensions of the cell and interface states at borders. t_{Si} = 88 nm, t_{BOX} = 145 nm, V_{SUB} = 10 V. (b) Ratio between the concentration along the film and the concentration in the needle (at 84 nm depth from the Si surface) for substrate biases from 3 V to 10 V. The doping concentrations for the silicon film and the needle region are per surface unit. 48

3.16 Schematic representation of the area covered by the carriers in (a) single-needle and (b) two-needle configurations. 49
3.17 Effective radius extracted from capacitance curves used for Figure 3.12.(a). Non-passivated wafer, t_{Si} = 88 nm, t_{BOX} = 145 nm, oscillation level 20 mV. 49
3.18 Schematics illustrating the definition of the effective surface, S_{eff} for two needles placed on the surface. (a) When an overlap occurs, the region A must be subtracted twice. (b) The physical boundaries of the etched silicon island limit the effective surface for large needle separation. 50
3.19 Schematic illustrating how the model can be extended to a multiple-needle configuration. To do this, it was necessary to take the number of the probes used in the measurements into account and also the number of the overlapped regions. . 51
3.20 (a) Effective surface obtained using the model proposed in Eqs. [3.10]-[3.13]. S_{eff} increases and decreases depending on the influence of the overlap and border regions (d_{cell} = 5 mm). (b) Effective surface simulated with the model proposed considering several frequencies. If the frequency is high enough, the maximum value of S_{eff} will be the sum of the areas generated by each probe (a constant value in a certain range of distances). 52
3.21 Comparison between the effective surface obtained in two-needle configuration extracted with Eq. [3.6] from experiments (filled dots) and the model proposed in Eq. [3.10] (open symbols). Distance between probes: (a) d = 1.59 mm, (b) d = 3.18 mm. Non-passivated wafer, t_{Si} = 88 nm, t_{BOX} = 145 nm. 53
3.22 (a) Effective surface in three-needle configuration. (b) Extracted effective surface by using Eq. [3.6] with three needles placed on the wafer surface and the model proposed in Eq. [3.14]. Non-passivated wafer, t_{Si} = 88 nm, t_{BOX} = 145 nm. . . . 53
3.23 Comparison between mobility results obtained using in Eq. [3.15] the S_{eff} value measured by two-needle configuration (black line), and the theoretical S_{eff} value calculated using Eq. [3.10] where the effective radius was measured in one-needle configuration (open symbols). Non-passivated wafer, t_{Si} = 88 nm, t_{BOX} = 145 nm. 54
3.24 Comparison between mobility results obtained by Split-C(V) technique (S_{eff} calculated using Eq. [3.10], solid line), and by considering the Pseudo-MOSFET area ($S_{eff} = 0.75 \times d^2$, dashed line). (a) d = 1.59mm; (b) d = 3.18mm. Non-passivated wafer, t_{Si} = 88 nm, t_{BOX} = 145 nm, freq = 300 Hz. 55

4.1 Point-contact characterization methods on bare SOI wafers: (a) four point-contact configuration, (b) two point-contact configuration (Pseudo-MOSFET technique), and (c) configuration for Split-C(V) measurements when two needles are employed. C and P represents the current and voltage connections respectively. . . 58
4.2 Comparison of the accumulation/inversion charge per area unit obtained from experimental results by the Split-C(V) technique (solid lines) and from simulations after calibration (open symbols), as a function of the substrate bias for the passivated wafers considered. (a) Four-needle configuration, t_{Si} = 88 nm. The distances $d_{31} \approx 0.12$ mm and $d_{32} \approx 2.5$ mm represent the separation between the contacts and the Si-island edges. (b) Pseudo-MOSFET configuration, t_{Si} = 12 nm. Distance between contacts $d = 1.59$ mm. t_{BOX} = 145 nm. 60
4.3 Electrostatic potential obtained from numerical simulations at BOX/Si-film (ψ_1) and Si-film/native oxide (ψ_2) interfaces as a function of the substrate bias. Passivated wafers (a) & (c), non-passivated wafers (b) & (d). t_{Si} = 88 nm (a) & (b), t_{Si} = 12 nm (c) & (d). t_{BOX} = 145 nm. 60

4.4 Vertical cross-section of the Silicon-On-Insulator structure (BOX/Si/Surface-Oxide). A Gauss surface (dashed lines) enclosing the Si/surface-oxide interface and the Silicon film is considered to determine the local electric field at a position z. . . . 61
4.5 (a) Comparisons between E_{S2} as a function of the substrate voltage for passivated and non-passivated SOI wafers from simulation data (solid line), and using the semi-empirical model of Eq. [4.7] (open symbols). (b) & (c) Comparisons between the effective electric field obtained by Eq. (4.6) using the simulation results (solid line), and by Eq. (4.7), employing the experimental data above the threshold condition (open symbols). $t_{Si} = 12$ nm. $t_{BOX} = 145$ nm. 63
4.6 Distances from the needles to the edges of the cell when a 4-point configuration is performed. 64
4.7 Experimental mobility curves for (a)-(c) holes and (b)-(d) electrons versus the effective electric field for passivated (solid symbols) and non-passivated (open symbols) SOI samples employing four (4p, square symbols) and two (2p, circular symbols) point-contact configurations. Substrate bias was modified from -60V to +60V. (a)-(b) $t_{Si} = 88$ nm, $t_{BOX} = 145$ nm. (c)-(d) $t_{Si} = 12$ nm, $t_{BOX} = 145$ nm. UMC curves are included for comparison [TTIT94]. 65
4.8 Experimental mobility curves for (a) holes and (b) electrons versus the effective electric field (logarithmic scale) for three different non-passivated SOI samples. The extraction is based on a two point-contact (Pseudo-MOSFET) setup with the adequate geometric factors *fg* from Table 4.2. Substrate bias was modified from from 0 to -60 V and from 0 to $+60$ V for the hole and electron channels characterization respectively. $t_{BOX} = 145$ nm. UMC curves are included for comparison [TTIT94]. 67

5.1 Schematic illustration of (a) crystalline and (b) poly-crystalline atomic structures. In (a) the atoms form regular repeating arrangements. (b) is composed by numerous crystalline structures with different orientations. 70
5.2 (a) Current curves as a function of the gate bias when the needle pressure varies from 50 g to 100 g. (b) Threshold voltage values obtained for the different probe pressures. $V_D = 100$ mV, $V_S = 0$ V. 71
5.3 (a) Current curves as a function of the gate bias when the needle pressure varies from 50 g to 100 g for different V_D values. (b) Threshold voltage values obtained for the different probe pressures. $V_S = 0$ V, P = 90 g. 71
5.4 Current curves as a function of the gate bias when the delay time is modified at two values: 100 ms, and 2 s. $V_D = 100$ mV, $V_S = 0$ V, P = 90 g. 72
5.5 Image of the graphene in one of the samples used. 73
5.6 (a)-(d) Microscope images of the graphene in one of the samples used taken lens 100X objective. 74
5.7 Schematic of the (a) two point-contact and (b) four point-contact techniques used to extract I-V characteristics for electrical characterization of graphene layers. (c) Setup employed for capacitance measurements. 74
5.8 (a) Image of one of the graphene samples positioned on the metallic chuck of the Janis station. (b) The microscope facilitates the location of the needles on the sample. 75

5.9 (a) Current obtained when a two-needle configuration is employed in a square shaped graphene layer on insulator layer satisfying $d << L$. (b) Current as a function of the needle pressure for $V_{12} = 1$ V. The current remains saturated above 50 g. Higher pressures only contribute to damage the underneath SiO_2 layer until physical breakdown. $V_{SUB} = 0$ V, d = 1.59 mm. 76

5.10 Drain current at a given bias point as a function of the substrate bias from -5 V to 5 V. $t_{BOX} = 90$ nm, $N_{D-substrate} = 10^{18} cm^{-3}$. 76

5.11 Schematic of (a) two-terminal and (b) four-terminal resistance measurements. . . 77

5.12 (a) Total resistance between probes for two-point contact configuration as a function of the probe separation. Linear regression for $d = 0$ allows the extraction of the contact resistance. (b) Form factor of the current flow for two-point contact configuration extracted combining four-probe and two-probe measurements. $V_{SUB} = 0$ V, $t_{BOX} = 90$ nm, $N_{D-substrate} = 10^{18} cm^{-3}$. 78

5.13 Conductivity as a function of the substrate voltage obtained from four-probe contact measurements for two different probe separation: $d = 220\mu$ m and $d = 440\mu$ m. $t_{BOX} = 90$ nm, $N_{D-substrate} = 10^{18} cm^{-3}$. 79

5.14 Carrier mobility extracted by the proposed four-point contact configuration for clean and contaminated samples of graphene and the actual microscope images of them. $t_{BOX} = 90$ nm, $N_{D-substrate} = 10^{18} cm^{-3}$. 79

5.15 (a) Capacitance curves as a function of the excitation signal frequency. (a) Using one and two needles and considering several distances between them. (b) Exchanging the high and low potentials in the experimental setup. $t_{BOX} = 90$ nm, $N_{D-substrate} = 10^{18} cm^{-3}$. 80

5.16 Simplified cross-section of a SOI wafer for Pseudo-MOSFET characterization technique: V_S is the source voltage and V_D is the drain voltage, both applied by pressure adjustable probes; V_G is the gate (substrate) voltage. D_{it1} and D_{it2} represent the density of interface states at BOX/Si film and Si film/top surface interfaces respectively. Two Gaussian surfaces in both edges of the Si film (dashed line, (a) and (b)) are represented 81

5.17 When a positive charged layer is added on the wafer surface, a shift of the current curves is produced (pointed by the arrows). The gate bias, V_G, was modified from -25V to 25V and the sweep total time was approximately 60s. INSET: Schematic of the sample containing the MESA isolated SOI cells. $t_{Si} = 12$ nm, $t_{BOX} = 145$ nm. 83

5.18 Threshold voltages for hole (left) and electron (right) channels extracted from the $I_D(V_G)$ curves before (squares) and after (circles) the APTES layer is created on the native oxide of the cells. 15 cells were probed. $t_{Si} = 12$ nm, $t_{BOX} = 145$ nm. 84

A.1 UMC curves from [TTIT94]. (a) Electron mobility in the inversion layer at 300 K and 77 K versus effective field E_{eff}, as a function of substrate acceptor concentration N_A. (b) Hole mobility in the inversion layer at 300 K and 77 K versus effective field E_{eff}, as a parameter of substrate donor concentration N_D. . 90

A.2 Comparison of the inversion charge concentration as a function of the front-gate bias between the experimental results (open-symbols), calculated by the Split-C(V) technique, and simulation results (solid-lines) obtained after the calibration of the solver. Back-gate bias: $V_{\mathrm{G2}} = 0$ V and $V_{\mathrm{G2}} = 2$ V. $t_{\mathrm{Si}} = 8$ nm, $t_{\mathrm{BOX}} = 10$ nm, $L = W = 10$ μm, EOT = 1.3 nm. 91

A.3 Effective field evaluated with Eq. (A.1) versus front-gate bias for different values of V_{G2} (0 V, 0.3 V, 0.6 V, 0.9 V, 1.2 V, 1.5 V, 2 V). For $V_{\mathrm{G2}} > 0$ V, two different front-gate biases lead to the same E_{eff} value. $t_{\mathrm{Si}} = 8$ nm, $t_{\mathrm{BOX}} = 10$ nm, $L = W = 10$ μm, EOT = 1.3 nm. 92

A.4 (a) Electrostatic potential cross section for two values of front-gate bias ($V_{\mathrm{G1}} = 0$ V and $V_{\mathrm{G1}} = V_{\mathrm{ret}} = 0.34$ V) when $V_{\mathrm{G2}} = 1.5$ V. (b) Effective field evaluated at the return point as a function of back-gate bias. $t_{\mathrm{Si}} = 8$ nm, $t_{\mathrm{BOX}} = 10$ nm, $L = W = 10$ μm, EOT = 1.3 nm. 92

A.5 (a) Bias map of experimental threshold voltage and simulated return point voltage as a function of the back-gate bias. Different regions can be distinguished: *(i)* $V_{\mathrm{G2}} = 0.9$ V: the transistor reaches the return point before the onset of the channel; *(ii)* $V_{\mathrm{G2}} = 1.2$ V: the threshold voltage and return point are reached simultaneously; *(iii)* $V_{\mathrm{G2}} = 1.5$ V: the front channel is in strong inversion before the field is minimum. (b) Experimental multibranch curves of mobility versus effective electric field for the three back-gate biases shown in (a). By comparison, the curve measured for $V_{\mathrm{G2}} = 0$ V shows lower mobility. $t_{\mathrm{Si}} = 8$ nm, $t_{\mathrm{BOX}} = 10$ nm, $L = W = 10$ μm, EOT = 1.3 nm. 93

A.6 (a) Experimental threshold voltage and simulated return point voltage versus back-gate bias. Three bias paths are illustrated: *(i)* $V_{\mathrm{G2}} = 1$ V, *(ii)* $V_{\mathrm{G2}} = 2$ V, and *(iii)* $V_{\mathrm{G2}} = 8$ V. (b) Corresponding mobility curves. $t_{\mathrm{Si}} = 6$ nm, $t_{\mathrm{BOX}} = 145$ nm, $L = W = 10$ μm, EOT = 1.3 nm. 94

B.1 Photography of the front of the CITIC-UGR building. 97
B.2 Front and back view of the Agilent B1500A Semiconductor Analyzer. 98
B.3 EASYExpert software. 98
B.4 Front and back view of the Keithley 4200-SCS Parameter Analyzer. 99
B.5 Keithley interactive test environment. 99
B.6 SMU plug-in module from B1500A equipment. 99
B.7 Conductors inside a triaxial cable. 100
B.8 Front and back view of the Impedance Analyzer 4294A. 100
B.9 Agilent extension cable 16048G. 100
B.10 Jandel point-contact system where Pseudo-MOSFET technique is carried out. . . 101
B.11 Janis micro-manipulated probe station. 102
B.12 BNC-triaxial adapter. 102
B.13 One of the Pseudo-MOSFET samples available in the nanoelectronics laboratory. 103
B.14 Semi-automatic probe system by Suss Microtec. This equipment provides a perfect environment for an accurate wafer current and capacitance low-noise measurements. 105
B.15 Nikon Microscope ECLIPSE LV150N. 105

C.1 Schematic of the different processes carried out at the IMEP-LAHC centre to made the cells which form the Pseudo-MOSFET samples: (a) cut the bare SOI wafer in smaller samples; (b) perform a photolithography on each sample; (c) make a RIE etching, and (d) final chemical clean of the sample. 107

C.2 Dicing saw (Disco DAD 321 machine) used to cut the substrate in smaller samples. 108

C.3 The whole SOI wafer was cut into small samples in several steps. (a)-(c) shows the sequence followed. 109

C.4 The sample was placed in a vacuum spindle to carry out the application of the resist. 109

C.5 The sample was placed in a vacuum spindle to carry out the application of the resist. . . . 110
C.6 Each sample was introduced into an optical lithographic system. . . . 110
C.7 If a positive photoresist is used, the exposed resist is dissolved in the developer. . 111
C.8 The inductively coupled plasma etcher employed during the fabrication process. . 112
C.9 Pseudo-MOSFET samples fabricated at IMEP-LAHC during the one-month stay. 113
C.10 Current characteristics extracted as a function of the probe pressure for needles with (a) 25 μm, (b) 40 μm and (c) 100 μm of diameter. . . . 113
C.11 Threshold voltages extracted from twenty current characteristics performed on the same cell for needles with (a) 25 μm and (b) 40 μm of diameter. . . . 114
C.12 Five I-V characteristics were obtained for three different separation between the needles. $d_1 = 1.59$ mm (black lines), $d_2 = 3.18$ mm (red lines), and $d_3 = 4.77$ mm (blue lines). . . . 115
C.13 C-V characteristics were obtained for three different separation between the needles. $d_1 = 1.59$ mm (black lines), $d_2 = 3.18$ mm (red lines), and $d_3 = 4.77$ mm (blue lines). . . . 115
C.14 Carrier mobility curves as a function of the gate bias for a two-needle (black line) and four-needle (blue line) configurations. . . . 116

List of Tables

2.1 Specifications of the wafers used in the statistical study. 29
2.2 Statistical data extracted from the experimental measurements. 30
2.3 Statistical data extracted from the experimental measurements. 31

4.1 Calibrated parameters for the numerical simulations (N_A: Si-film doping, P_{ch}: hole channel, N_{ch}: electron channel) 59
4.2 Geometrical factors obtained by comparing $I - V$ characteristics from two- and four-needle configurations. 66

5.1 Specifications of the Poly-Si wafers from the batch 6383-GRA fabricated by CNM company. 70
5.2 Mobility values calculated for Poly-Si wafers. 72
5.3 Set of data employed to extract Q_{SUP} through the model given by Eq. (5.13). The different intermediate parameters extracted for hole and electron channel are presented. 84

B.1 Specifications of the Silicon wafers from the batch RUN 6493-GRA fabricated by CNM. 103
B.2 Specifications of the Silicon wafers available in the laboratory fabricated by SOITEC company. 104
B.3 Specifications of the Poly-Si wafers from the batch 6383-GRA fabricated by CNM. 104

C.1 Specifications of the setup parameters. 112

Abbreviations

1-D, 2-D	**U**ni, **B**i-**D**imensional
AC	**A**lternating **C**urrent
BESOI	**B**ond-and-**E**tch-back **SOI**
BOX	**B**uried **OX**ide
CMOS	**C**omplementary **MOS**
DC	**D**irect **C**urrent
DIBL	**D**rain **I**nduced **B**arrier **L**owering
ELTRAN	**E**pitaxial **L**ayer **TRAN**sfer
EOT	**E**ffective **O**xide **T**hickness
FD-SOI	**F**ully **D**epleted **SOI** transistor
MOSFET	**M**etal-**O**xide-**S**emiconducor **F**ield-**E**ffect **T**ransistor
PD-SOI	**P**artially **D**epleted **SOI** transistor
SHG	**S**econd **H**armonic **G**eneration
SIMOX	**S**eparation by **I**mplantation of **OX**igen
SOI	**S**ilicon-**O**n-**I**nsulator
SOS	**S**ilicon-**O**n-**S**apphire
SOZ	**S**ilicon-**O**n-**Z**irconium

Chapter 1

Introduction to SOI Materials and Devices

This chapter introduces the substrate technology on which this work has been based: Silicon on Insulator (SOI). Initially, the main manufacturing techniques used in the SOI wafers industry will be described as well as the advantages of this kind of substrates. Then, a classification of SOI devices is presented differentiating between partially depleted (PD) and fully depleted (FD) transistors. Finally, several characterization methods will be explained, as well as the passivation process used to improve the quality of the top surface in bare substrates.

1.1 Motivations

In the conventional (bulk) MOS transistors, the *active region*, where the different devices are fabricated, only covers a thin superficial layer of the Silicon (typical wafer thickness is 775 μm thick for wafers 300 mm diameter [RCN03]). The rest of the wafer constitutes the substrate and gives support to the structure (Figure 1.1). Unfortunately, this last part is also the responsible for several undesired parasitic effects, such as parasitic capacitances (which decrease the operation speed of the devices) or leakage currents (which decrease the isolation between the different devices introducing unwanted electrical connections) [JB91, MK86].

A new technology developed in the latest decades emerged as an alternative to the traditional and well established bulk approach. It was called Silicon-On-Insulator (SOI) technology [Maz06, CL95] and the novelty was found in the structure of the substrates: a dielectric layer, named buried oxide or BOX, is created inside the substrate.

There exist three main reasons which motivated the development and use of SOI technology. The first one is the increase of ionic radiation hardness. In the 1970's and 1980's and, due to the Cold War, there existed a great interest for fabricating circuits which resist the ionizing radiation effects so they could operate in a hypothetic nuclear war scenario. It was demonstrated that SOI wafers were able to minimize these ionizing impact [CIL+93]: the majority of the charges generated in the substrate are blocked by the BOX reducing the current surge in the active film

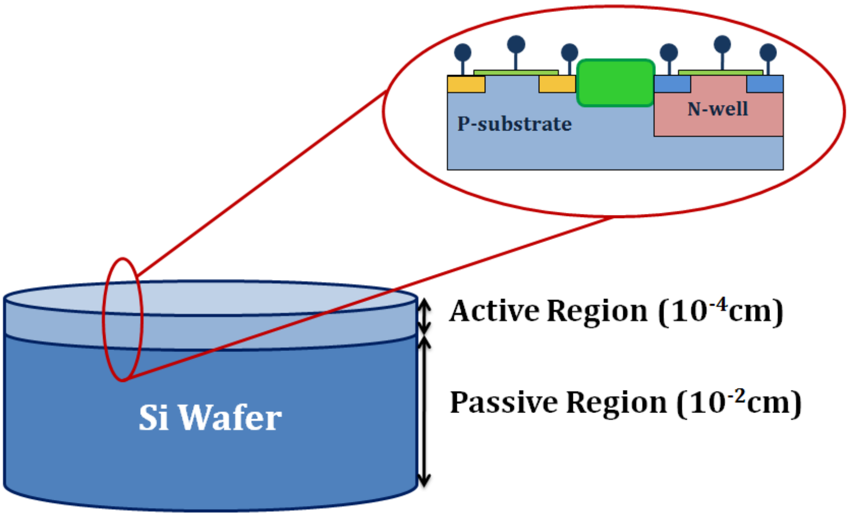
P-substrate
N-well
Si Wafer
Active Region (10-4cm)
Passive Region (10-2cm)

Figure 1.1. Cross section of the superficial layer in a bulk wafer.

(Figure 1.2). In addition, SOI has also superior immunity to the induced degradation by hot carriers than bulk Silicon substrates [SFCA92].

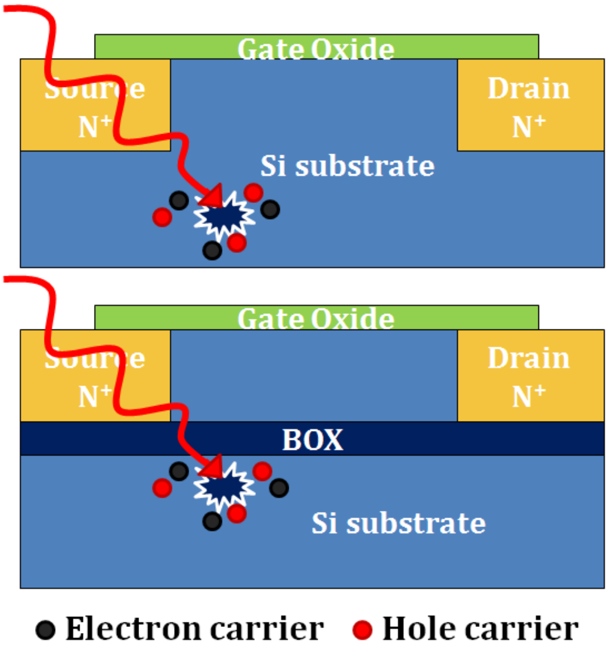
Gate Oxide
Source N+
Drain N+
Si substrate
Gate Oxide
Source N+
Drain N+
BOX
Si substrate
● Electron carrier
● Hole carrier

Figure 1.2. Effect of the ionizing radiation in bulk and SOI wafers.

Secondly, the performance enhancement led some companies to employ this technology. In digital applications, for instance, SOI circuits run faster than those made on bulk substrates when the same voltage is applied. Thus, it is possible to reduce power consumption by lowering their operating bias, without affecting their performance.

Finally, as the *end of the Roadmap* is approaching, SOI is required in order to extend the life of the traditional Silicon technology [CC03]. Transistors with gate lengths lower of 25nm do not perform well in Silicon bulk substrates, basically, due to short channel effects (SCE): the electric field in the channel induced by the gate is similar to the fields created by the source and drain regions [CL95]. These undesired effects are mitigated by using SOI structures.

All of these reasons have caused that the commercial applications of SOI devices hd grown considerably in the latest decades. Some examples at present are consumer electronics and gaming, mobile devices or dataprocessing [SOI15].

1.2 SOI wafers fabrication

SOI technology can be classified in two main alternatives (regarding the wafer architecture):

- The Silicon layer can be created directly on the top of a dielectric substrate as occurs in Silicon-on-Zirconium (SOZ) and Silicon-On-Sapphire (SOS) [Cri87] structures (Figure 1.3.(a)). This is possible if the lattice constants have approximately the same value in both materials.
- In the other alternative, the SOI substrate can be formed by a *buried oxide* (BOX) placed between the film and the substrate (Figure 1.3.(b)). This option is the most commonly used in the industry. The usual processes employed to obtain these substrates will be described from Section 1.2.1 to Section 1.2.2.

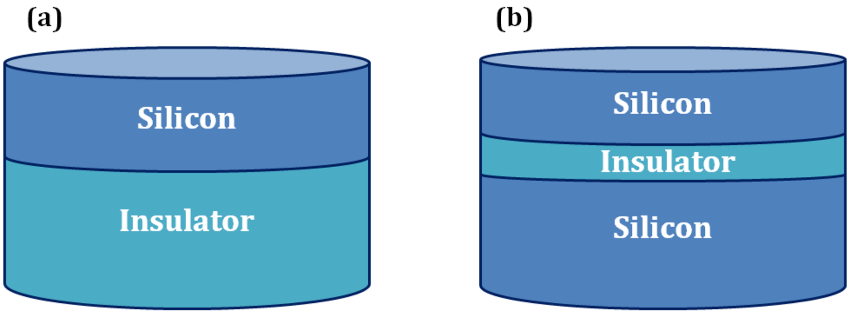

Figure 1.3. Types of SOI structures: (a) when the Si layer is created directly on a substrate, and (b) when a insulator is formed inside a Si substrate.

When dealing with SOI wafers some aspects to achieve during the fabrication are:

- Very low defect densities in both layers (buried oxide and Si film).
- Uniform thickness on the whole wafer surface.
- High quality at the Si/BOX interface.
- Good electric features of the insulator.

Nevertheless, the main problem resides in the fact that a crystalline Silicon layer (needed for the fabrication of electronic devices) must be deposited on an insulator (usually SiO_2). Nowadays, there is no deposition method to obtain *directly* a crystalline Silicon on an amorphous substrate. The main techniques employed in the SOI industry (at least at some point during the history of SOI development) can be divided into two main types: those in which the buried oxide is created by implantation through the Silicon (Separation by IMplantation of OXygen (SIMOX)), and those which use *wafer bonding* (Bond-and-Etch-back SOI (BESOI), Epitaxial Layer TRANsfer (ELTRAN) and Smart-Cut^{TM}).

1.2.1 Separation by IMplatation OXygen, SIMOX

It has been the most used fabrication method during the beginning of the development of SOI from standard bulk substrates. M. Watanabe y A. Tooi [WT66] were the first ones to discuss about the creation of Silicon dioxide (SiO_2) through oxygen ion implantation in 1966. However, it was not until 1970's when the technique was completely developed by K. Izumi, M. Doken y H. Ariyoshi [IDA78].

The principles of SIMOX are quite simple and the main steps are shown in Figure 1.4 [HRK+87]:

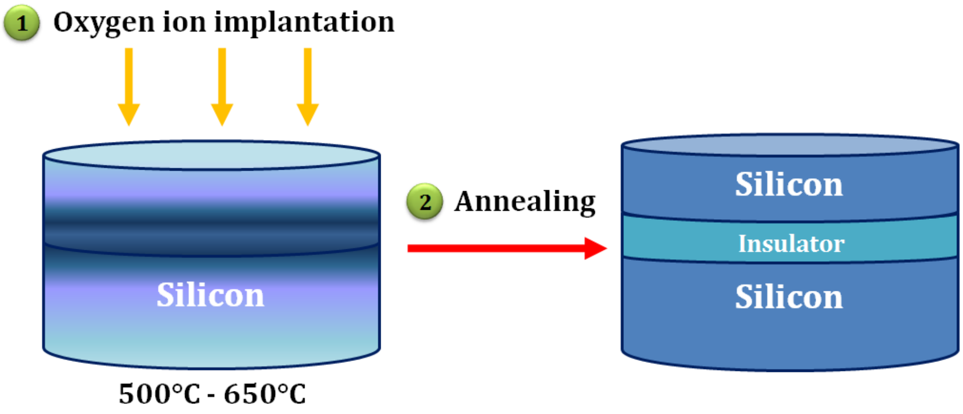

Figure 1.4. The principle of SIMOX: a heavy-dose oxygen implantation into silicon followed by a very high temperature annealing step produces a buried layer of Silicon dioxide, below a thin crystalline Si film [HRK+87].

1. The wafer is altered by a deep oxygen ion implantation at high doses (in the order of $2 \times 10^{18} ions/cm^2$) at high energies (200 keV) and at temperature close to 600-700°C [CC03]. After the implantation, both silicon and oxide are seriously damaged.
2. Then, the sample is heated up about 1150-1200°C and, later, to 1250-1405°C. The aim of this annealings is to induce the reaction between oxygen ions and Silicon in order to form SiO_2, to eliminate the high density of precipitates and residual defects and, finally, to obtain atomically sharp and planar interfaces between the near-surface regions of Si and the buried oxide. A single-crystal but highly defective Silicon overlayer (Si film) above the oxide is obtained.

In order to improve the structure and properties of interfaces, the energy and the dose of the implantation can be properly varied: the Silicon thickness can be controlled by the energy, whereas the oxygen ion doses manage the BOX thickness. The advantage of this method is that the implanted doses can be extremely precise, what guarantee a very uniform Si film and BOX thicknesses. Moreover, in order to reduce the defect density, consecutive implantations at lower doses can be done [HRK+87].

On the other hand, the temperature at which the implantation is carried out is also an important parameter due to its influence on the quality of the final material. The implantation causes defects into the layer placed on the buried oxide. If the temperature of the Silicon wafer during the implantation is too low, the Silicon overlayer may get completely amorphized forming a polycrystalline structure.

In short, SIMOX wafers can be obtained with relatively good quality, very uniform thicknesses and sudden interfaces Si/SiO_2. However, the quality of the BOX achieved is considerably lower than the native thermal oxide quality.

1.2.2 Bond-And-Etch-Back, BESOI

BESOI method is based on *Wafer Bonding* technique. The term *Wafer Bonding* is referred to the phenomenon in which two clean and polished wafers (of almost any material) are attracted by *Van der Waals* forces[1] when they are heated. In this case, two wafers are bonded to a Silicon dioxide layer, SiO_2 [GR93], as follows (Figure 1.5):

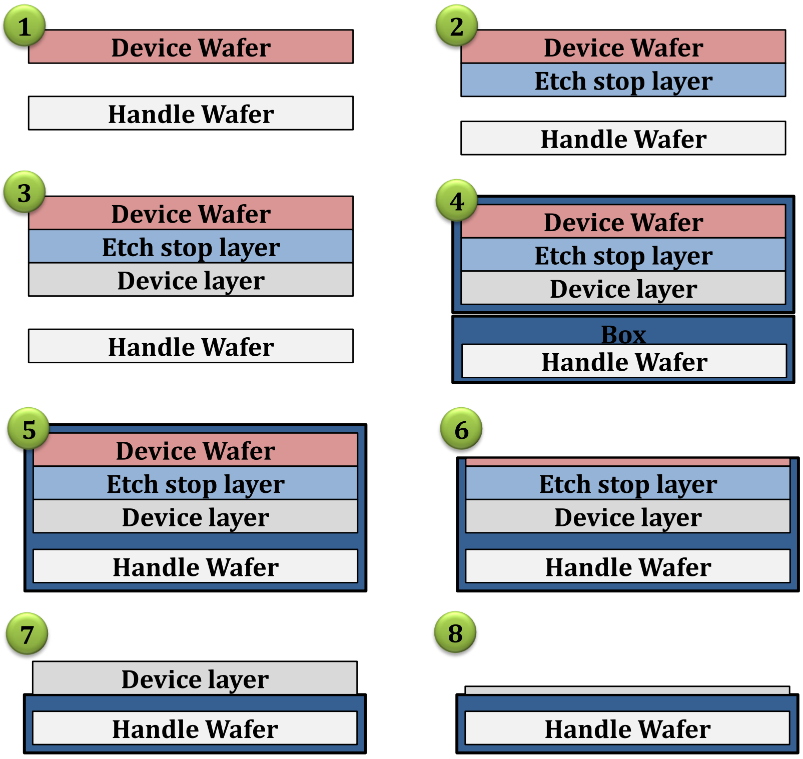
1
Device Wafer
Handle Wafer
2
Device Wafer
Etch stop layer
Handle Wafer
3
Device Wafer
Etch stop layer
Device layer
Handle Wafer
4
Device Wafer
Etch stop layer
Device layer
Box
Handle Wafer
5
Device Wafer
Etch stop layer
Device layer
Handle Wafer
6
Etch stop layer
Device layer
Handle Wafer
7
Device layer
Handle Wafer
8
Handle Wafer

Figure 1.5. Schematic representation of BESOI process for SOI wafer manufacturing [GR93].

1. Two conventional wafers are considered.

---

[1] This kind of forces are the responsible for keeping together the molecules in solids, although their strength is much lower than in the main bonds: ionic, metallic and covalent [Isr11].

2. In one of them a different layer is introduced, for example, by a selective doping (junction P^+/P^- or P/N) or a different substrate ($SiGe$) [MG92]. This layer will be used to set where the etching must stop (called *etch stop layer*).
3. The monocrystalline Si layer with the same purity than the substrate is bonded on the oxide by a SFB (Silicon Fusion Bonding) [NKL+96].
4. Both wafers are oxidized and bounded.
5. In order to eliminate the substrate, a mechanical etching is carried out on the first wafer.
6. A second etching serves to reach the *etch stop layer*.
7. Finally, the surface of the resultant wafer is smoothed by chemical mechanical polishing (CMP) treatment.

This technique presents the advantage that Si film/BOX and BOX/substrate interfaces present both good quality because they have been obtained by thermal oxidations. However, this method is relatively expensive due to the use of two initial Si wafers for the manufacturing of only one SOI wafer.

1.2.3 Epitaxial Layer TRANsfer, ELTRAN

ELTRAN technique was developed by Canon in 1990 [YSS94]. In this method the formation of a Silicon porous layer and *Wafer Bonding* technique are combined to produce a material with good uniformity in the film thickness.

It is possible to create porous Silicon when a current flows through a Silicon sample immersed in an electrolytic cell with hydrofluoric acid (HF). The resulting material keeps the crystalline structure in the regions where the chemical reaction has occurred. ELTRAN technique takes advantage of the mechanical weakness of porous Si and, at the same time, it still preserves the single crystalline quality of the original wafer. The complete process to obtain a SOI wafer by ELTRAN method follows the next steps (Figure 1.6):

1. Initially, one wafer is subjected to an anodic etching. Through suitable changes in the current flow during this stage, a layer with very fine pores is formed at the surface whereas a second layer with coarse pores remains deeper into the substrate.
2. The sample is introduced in a furnace at 1100°C with hydrogen gas (H_2) which reduces the surface roughness. After that, a crystalline Si epitaxial layer is grown.
3. The wafer obtained is cleaned and bounded to another one (*Handle Wafer*) which has a SiO_2 layer.
4. Since there is a considerable surface stress at the interface, a water stream at high pressure (20-60 MPa) makes fractures along the planar porous layers. At the end, a SOI substrate is achieved whereas the rest of the wafer can be reclaimed, polished if necessary, and then reutilized.
5. After wafer splitting, the residual porous Silicon is etched away, and the newly exposed SOI wafer surface is smoothed by a second application of hydrogen annealing.

The crystal quality of the SOI material obtained by *Wafer Bonding* and etch-back is, in principle, as good as that of the starting Silicon wafer.

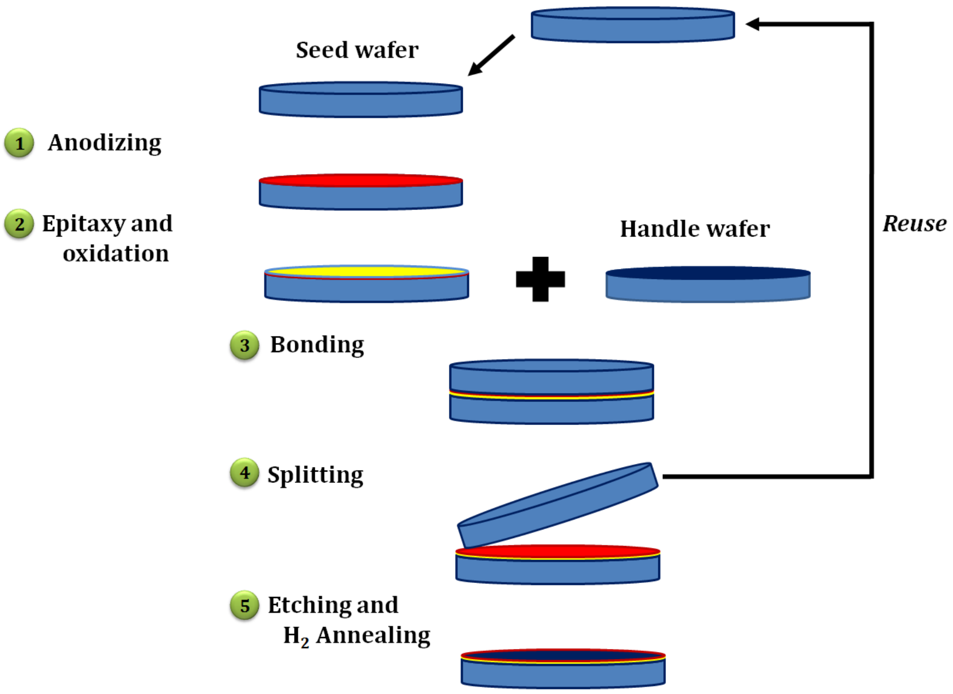

Figure 1.6. Schematic representation of ELTRAN process for SOI wafer manufacturing [YSS94].

1.2.4 Smart-Cut^{TM}

In the 1990's, a revolutionary process of wafer separation was invented by M. Bruel from CEA-Leti (Grenoble, France) [Bru95]. It combined ion implantation technology and the *Wafer Bonding* to transfer a thin surface layer from an initial wafer onto either another wafer or an insulating substrate. This method is the most used at present because it produces more effective commercial SOI wafers (which are also named Unibond) [CC03].

The basic steps of this technique are illustrated in Figure 1.7:

1. Two conventional wafers (A and B) are considered. The *donor wafer* (A for example) undergoes a controllable thermal oxidation to form an oxide which will serve as the BOX. Its thickness can be adjusted with precision.

2. A hydrogen implantation with doses between $3 \times 10^{16} - 1 \times 10^{17} ions/cm^2$ is carried out through the oxide but inside the Si. The hydrogen induces micro-cavities in the Si which allows defining a breakable plane.

3. The wafers A and B (*Handle wafer*) are carefully cleaned in order to eliminate particles and contaminations on their surface. Then, the two wafers are aligned and put in contact, so the bonding is made on the entire surface.

4. Later, an annealing treatment is carried out for dividing the wafer. There are two sequences in this stage:

    (a) At the first annealing (400-600°C) an increase of the micro-cavities size is produced and the pressure inside them is also increased. It provokes an horizontal fracture which separates the wafers naturally.

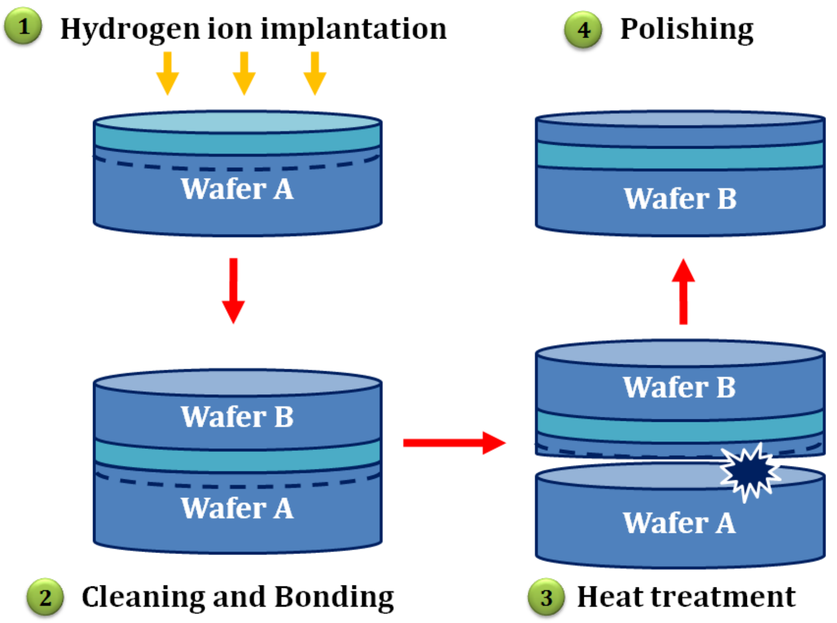

Figure 1.7. Schematic illustration of the fabrication steps for a standard Unibond SOI wafer with Smart-Cut^{TM} technique [CC03].

   (b) A second heat treatment (1100°C) serves to strengthen the bond between the *handle wafer* and the Si film. It is worth saying that, as the surface roughness is in the order of some nanometers, the A wafer can be reutilized (the process is called *refresh*).

5. Finally, chemo-mechanical polishing is performed on the SOI film to reduce the surface roughness.

This technique also enables to fabricate circuits for certain applications where the properties of the mechanical support are important, as in the case of integrated circuits on flexible substrate, glass or plastic, allowing a best integration of embedded systems [CC03].

1.3 Advantages of SOI technology

Although most of the technological processes of SOI wafers are compatible with the standards of the semiconductor industry, the final cost of the product is slightly higher. It is essentially due to the extra fabrication steps needed. Nevertheless, the advantages provided by SOI technology compared to bulk are numerous and they justify widely the cost increment for certain applications. Among the main improvements are [CC03]:

- Reduction of the electric interaction between devices and substrate (isolation), which implies:
  - Reduction of the device area and increase of the integration capability in chips.
  - Important reduction of parasitic capacitance.
  - Suppression of latch-up.

  - Lower subthreshold swing.
  - Reduction of leakage currents.
  - Lower power consumption of SOI chips by lowering their operating voltage, while still keeping the clock rate.
  - Diminution of short channel effects (SCE) by using thin SOI structures.
  - Improvement of the transconductance.
  - Higher ionic radiation immunity.
  - Higher temperature operation ranges.

- Integration of different structures in the same chip such as high speed devices, power devices, MEMS and optoelectronics [BR07].
- Possibility of making planar devices as well as three-dimensional ones [BR07].

1.4 SOI devices classification

When dealing with processed SOI transistors, the terms **PD** (*Partially Depleted*) and **FD** (*Fully Depleted*) are often used. They both are referred to the depletion thickness of the Silicon body of the transistor, located between the front-gate oxide and the BOX.

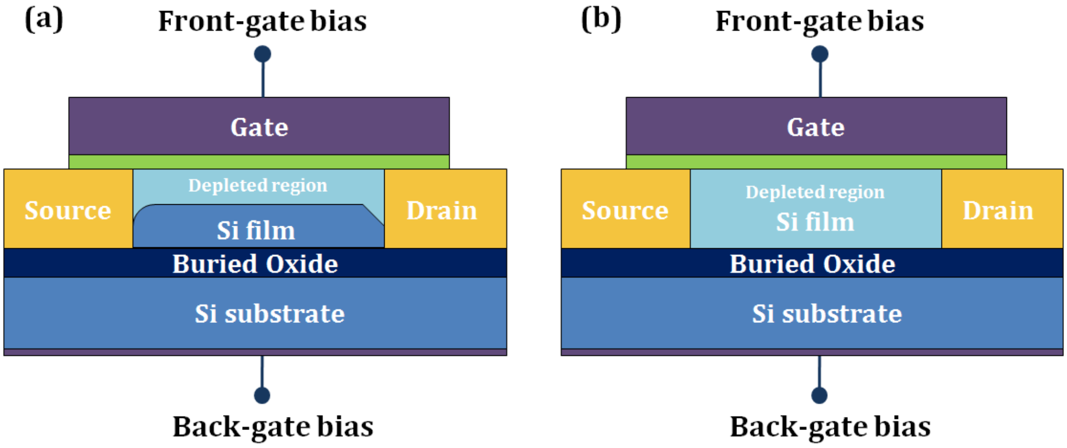
(a)
Front-gate bias
Gate
Source
Depleted region
Si film
Drain
Buried Oxide
Si substrate
Back-gate bias
(b)
Front-gate bias
Gate
Source
Depleted region
Si film
Drain
Buried Oxide
Si substrate
Back-gate bias

Figure 1.8. Schematic of a partially (a) and a fully (b) depleted SOI MOSFET.

- In **partially depleted (PD)** SOI MOSFETs (Figure 1.8.(a)), the depletion region induced by the gate does not extend from one interface to the other. In other words, the Si film is not completely depleted of mobile charges and a *neutral* zone subsists between the two insulators.
- **Fully depleted (FD)** mode (Figure 1.8.(b)) happens when the depletion region covers the whole transistor body. The depletion charge is constant and cannot extend further when the gate bias increases. The potential of both interfaces interacts by coupling, what means that the electrical characteristics of one channel vary with the opposite gate (substrate) bias.

Typically, commercial non-intentionally doped Silicon films larger than 70nm correspond to PD and below 30nm to FD [CA10].

1.5 SOI wafers characterization

In SOI technology, the quality of the Silicon film, the buried oxide and the interfaces between them should be known before the fabrication of devices in order to avoid unnecessary costs associated with unsuitable wafers. Accordingly, semiconductor characterization techniques aim to extract the wafer electrical parameters [CW92]. In the following sections, some characterization methods for as fabricated SOI wafers are described.

1.5.1 Four-point probe

This technique was originally proposed by Wenner [Wen15] in 1915 to measure the Earth resistivity. Later, in 1954, Valdes adopted it to measure semiconductor resistivity [Val54]. At present, the method is commonly used to obtain the *sheet resistivity* (ρ_{sh}) of thin conducting layers and wafers.

The starting point is an SOI wafer with four needles placed in-line on its surface and equally spaced (Figure 1.9). Then, a current flows between the outer probes is fixed (I_{14}) at the same time that the voltage drop between the inner needles is measured (V_{23}). As the voltmeters present high input impedance, the input current is almost negligible and, therefore, the resistances of probes 2 and 3 hardly have an impact on the measurements. The sheet resistivity when the probes are located far away from the sample borders is then obtained as [Sch06]:

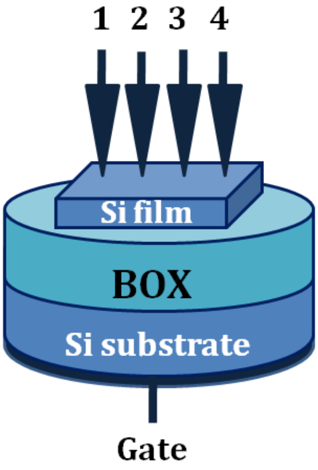

Figure 1.9. Schematic of the 4-point probe setup.

$$\rho_{sh} = \frac{\pi}{ln(2)} \frac{V_{23}}{I_{14}} \tag{1.1}$$

An important utility of this technique will be explained in Section 4.3 and it will be related to the extraction of the effective electric field originated inside a SOI wafer. In addition, in Section 5.2.2.3 will serve to calculate the form factor associated to a graphene sheet.

1.5.2 Two-point probe

The two-point probe, also referred as Pseudo-MOSFET technique (Ψ-MOSFET), is a simple and successful method used for the monitoring of the SOI wafers quality [CW92]. It is based on the MOS-like configuration implicit in any SOI substrate: the Si film can serve as the transistor body; the BOX plays the role of the gate insulator and, finally, the substrate acts as the gate terminal. So, when the gate is positively or negatively biased, an electron or hole channel is induced in the Si film/BOX interface and static curves can be extracted. Since these characteristics are similar to those of fully processed MOSFETs standard methods can be applied to extract electrical parameters[2] such as threshold voltage, mobility of electron and holes, interface traps, etc. [CML00].

The main advantage of the Ψ-MOSFET technique, as well as four-point method explained before, is that it does not require the creation of contacts. There exist two main versions of the method which differ in the way that source and drain are simulated (Figure 1.10).

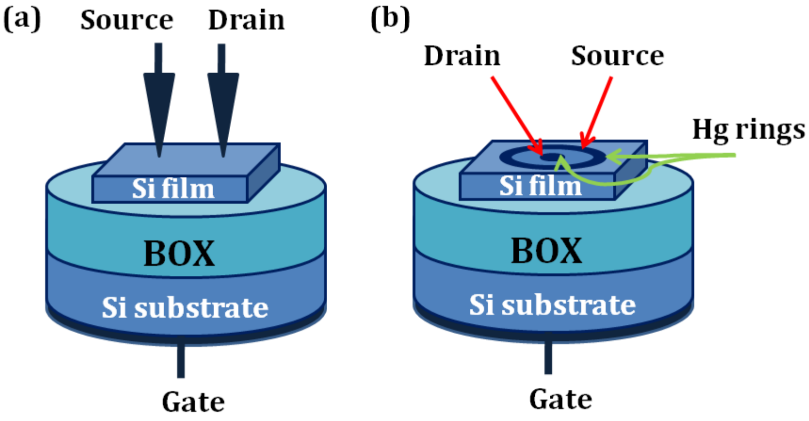

Figure 1.10. Ψ-MOSFET configuration with (a) metallic pressure probes, or (b) mercury probes.

1. The first version (Figure 1.10.(a)) was developed by S. Cristoloveau [CW92] in 1992 at IMEP and it uses two metallic needles (with adjustable pressure) on the surface of the Si film which create the source and drain contacts.
2. The second one (Figure 1.10.(b)), known as $H_g - FET$, was developed by H. J. Hovel at IBM [Hov97] in 1997. It uses mercury concentric rings to generate the contacts of source and drain. As the source is grounded, the device is perfectly isolated from the rest of the wafer. Additionally, the pressure probe dependence does not exist and the current flows following the circular geometry [MCH99].

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[2] A further explanation about equations employ in Pseudo-MOSFET method will be exposed in Section 2.1.4.

1.5.3 Second Harmonic Generation, SHG

One of the drawbacks of the Pseudo-MOSFET technique is that it is a contact based method. This produces some damage in the Si film by placing the probes directly on the wafer limiting the characterization of the Si film/BOX interface [ISD+09].

A nondestructive and noninvasive technique known as *Second Harmonic Generation* (SHG) does not employ physical contacts on the sample. The method consists of detecting the electric field in the Si film/BOX interface through optical signals.

The process has its principles in the interactions of photons (Figure 1.11): two electrons with the same frequency ω and energy $h\omega$ are absorbed at the same time that a photon with the frequency 2ω and energy $2h\omega$ is generated by a simple quantum mechanical process.

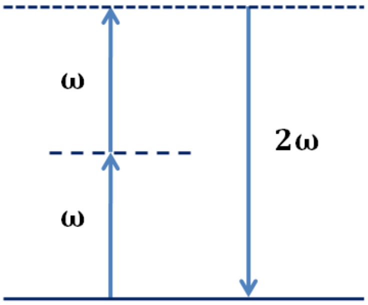

Figure 1.11. Energy levels diagram involved in SHG process [APL+07].

Figure 1.12 shows the schematic of this method. A laser irradiates beams of photons to the wafer which are reflected at the different interfaces of the structure and separated by a prism. Then, a photomultiplier (PMT) and a photon counter detect these reflections [JSF+04].

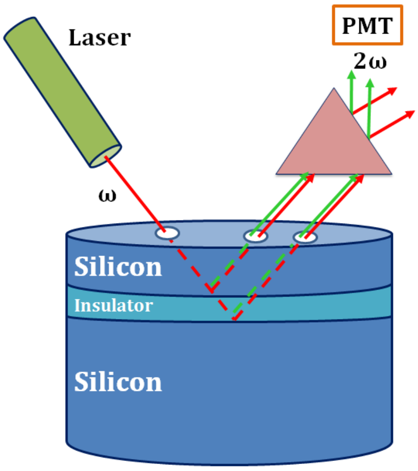

Figure 1.12. Schematic of the Second Harmonic Generation technique.

The laser generates electron-hole pairs within "Silicon regions". Some of these electrons acquire the enough energy to overcome the interface barrier and they are introduced in the oxide where they are trapped by defects. As consequence, a time-dependent electric field is created in the interfaces defined by:

$$I^{2\omega}(t) = |X^{(2)} + X^{(3)}E(t)|^2(I^{\omega})^2 \tag{1.2}$$

where $I^{2\omega}$ and I^{ω} are respectively the intensities of the generated second harmonic beam and of the incident one (fundamental and second harmonic); $X^{(3)}$ term is the third order Silicon susceptibility, and $X^{(2)}$ is the SHG effective susceptibility which depends on interface quality. $E(t)$ indicates a quasi-static electric field related to the effective surface charge density in the oxide σ (obtained by the integral of the volume charge density, ρ, through the oxide):

$$E(t) = \frac{e\sigma(t)}{\epsilon_{si}} \tag{1.3}$$

$$\sigma(t) = \int_0^{T_{ox}} \rho(z,t)dz \tag{1.4}$$

For structures with several interfaces (labeled i), the total SHG intensity is calculated as the contribution of all of them:

$$I^{2\omega}(t) = \sum_i |X_i^{(2)} + X_i^{(3)}E_i(t)|^2(I^{\omega})^2 \tag{1.5}$$

Nevertheless, the electric field is generated independently for each one, although a constant external field was applied. In this case, the equation is modified as:

$$I^{2\omega}(t) = \sum_i |X_i^{(2)} + X_i^{(3)}(E_{Ext} \pm E_i(t))|^2(I^{\omega})^2 \tag{1.6}$$

Depending on the polarity of the field, the contribution will be added or substrated from the existing field.

Many works have demonstrated that SHG is a successful technique used for real-time SOI wafers characterization, [IPN+15, DPS+15]. In addition, SHG allows to characterize the radiation response of multi-interface SOI wafers providing information about charge carrier dynamics in SOI structures [JSF+04].

1.6 Defects of SOI materials

Any manufacturing process introduces inevitable defects in the fabricated substrates. The dislocations can be harmful for the good operation of the devices leading to a decrease of the mobility, variations of the threshold voltage, increase of the leakage currents, etc [HAHC07].

When dealing with SOI wafers most of the defects (broken bonds, impurities, imperfections) are set within the Si/BOX interface. Due to the crystalline nature of the Silicon and the amorphous structure of the oxide, when these two materials are bonded an intermediate substoichiometric region appears (called SiO_x in Figure 1.13) [Pan78]. This zone contains multiple *traps* which interact with the free carriers of the semiconductor degrading the quality of the interface and, consequently, of the Silicon film and the channel.

Nevertheless, the *buried oxide* in a bare SOI wafer presents good features due to its thermal grown unlike the *upper native oxide* which is rich in defects because it is created without control (spontaneously grown). Because of that, the influence of the BOX/Si film interface on the channel results negligible. This fact becomes important when the film thickness is scaled down since the channel will be closer to the surface and, hence, it will be more sensitive to the traps density from the native oxide/Si film interface. Wafers with this kind of top layer are denominated *non-passivated*.

Nevertheless, there exists a treatment called *passivation* in which a very thin layer of a good quality oxide is grown under control on the top of the structure. In this process, wafers underwent a clean dry oxidation process at very high temperatures, i.e. at 900 °C, to passivate a Silicon wafer surface with a sub-10nm surface oxide [HAHC07]. Through this process, the trap density in the surface oxide is considerably reduced.

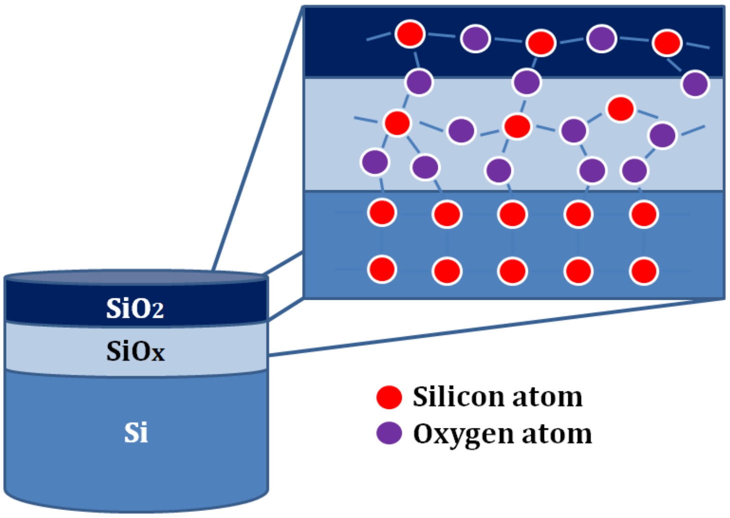

Figure 1.13. When the Silicon is bounded to an oxide, a region of defects is automatically originated at the interface.

Section 4.3 will describe the main difference of having a passivated or non-passivated surface in terms of effective electric field originated inside the wafer Silicon film, as well as the direct consequences on the values of the carrier mobility.

1.7 Conclusions

In this chapter, the main characteristics of the SOI technology have been presented, such as its advantages with respect to bulk substrates, or the main fabrication techniques employed at present. Accordingly, it has said that the Smart-Cut^{TM} technology is dominant in the manufacturing industry of SOI wafers.

Furthermore, some characterization methods employed at wafer level, have been introduced and briefly described. In the following Chapters, the point-contact techniques will acquire protagonism over the rest, and the main results obtained with this method during the development of this work will be widely described and analyzed.

Chapter 2

Electrical Characterization of Bare SOI Wafers

After the introduction to SOI technology, the syllabus of this work continues now focusing on the electrical characterization of bare SOI substrates. In particular, the following sections will be dedicated to the so called Pseudo(Ψ)-MOSFET point-contact method previously presented in Chapter 1, describing the different experimental electrical parameters that this technique allows to extract, as well as its benefits and usual applications.

2.1 The Pseudo(Ψ)-MOSFET technique

The Ψ-MOSFET method has been used for the *in-situ* characterization of Silicon-On-Insulator (SOI) structures since the beginning of the 1990s [CW92]. Both, the simplicity of its setup and the possibility of studying bare samples without any CMOS processing, turn this technique into a very useful and nondestructive tool for carrying out a preliminary wafer testing. By this way, it will be possible to have a previous knowledge about the samples quality.

2.1.1 Principle and operation

The main benefit of Pseudo-MOSFET method is found in its experimental configuration since it takes advantage of the upside-down transistor-like configuration intrinsic to any SOI structure: the substrate is used as the gate terminal; the Buried Oxide (BOX) serves as the gate insulator, and the Silicon film represents the transistor body. To complete the scheme, two metallic needles are placed on the surface acting as the source and drain contacts.

The non-implanted nature of the contacts allows the wafer to be both positively and negatively biased (Figure 2.1): when the substrate (gate terminal, V_G) takes negative values ($V_G < 0$) a hole channel is induced at the Si film/BOX interface (resulting in a *P-type transistor device*); on the contrary, if the substrate is biased positively ($V_G > 0$) the conduction in the channel is due to electrons (resulting in an *N-type transistor device*).

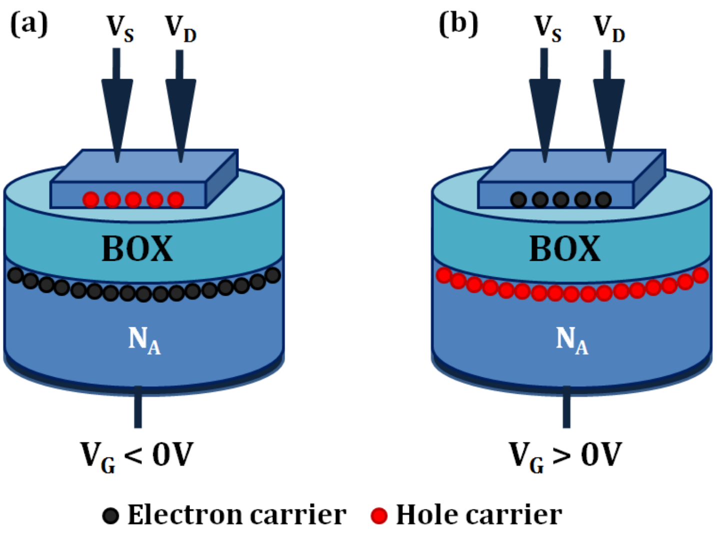

Figure 2.1. A P-type Ψ−transistor operating in strong (a) accumulation (hole channel) and (b) inversion regime (electron channel).

2.1.2 Methodology

To carry out the implementation of the Pseudo-MOSFET technique, it was necessary to use the equipments available at the Nanoelectronics Laboratory at the CITIC-UGR centre[1]. Specifically, to perform I/V curves, a Jandel Universal probe station was employed together with the Agilent B1500A semiconductor analyzer, connected to each other by triaxial cables (Figure 2.2). Thanks to several SMUs (source-monitor units) included in the analyzer, the gate, drain and source voltages (V_G, V_D, V_S) are controlled synchronously and, at the same time, their respective currents (I_G, I_D, I_S) are measured.

Regarding the samples employed in this work, Figure 2.3 shows an image of one of them. The substrates contain MESA-isolated square islands of 5 mm x 5 mm dimension with a Si film non-intentionally doped ($N_A \approx 10^{14} cm^{-3}$). This kind of samples are placed on the metallic chuck of the station since it can be biased completing the experimental configuration.

2.1.3 Static characteristics

The ambipolar operation of the Pseudo-MOS transistor allows to extract simultaneously electrical characteristics for hole and electron channels. Figure 2.4 shows examples of an standard two-needles $I_D(V_G)$ measurement and its corresponding transconductance (dI_D/dV_G). The three main operation regimes are also pointed out.

Independently of the type of channel created, when the threshold condition is reached, the current follows a behavior similar to that induced in a MOS transistor. This current (and its corresponding transconductance) is approximately three times larger for the electron channel case in comparison with the hole one, verifying the ratio between the electron and hole mobilities [TTIT94].

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[1] A complete description of all the facilities and equipments used in this thesis is included in Appendix B.

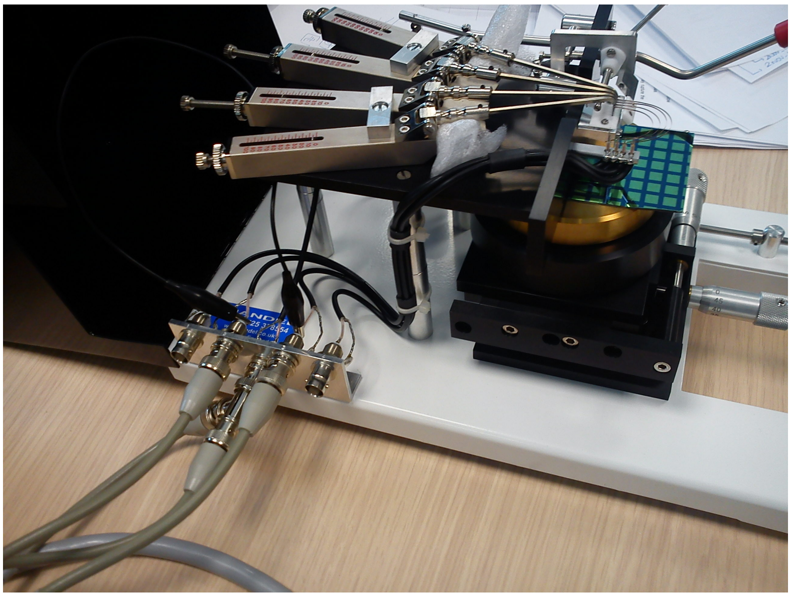

Figure 2.2. The Jandel Universal probe station used to perform point-contact measurements is connected to the Agilent B1500A semiconductor analyzer through triaxial cables.

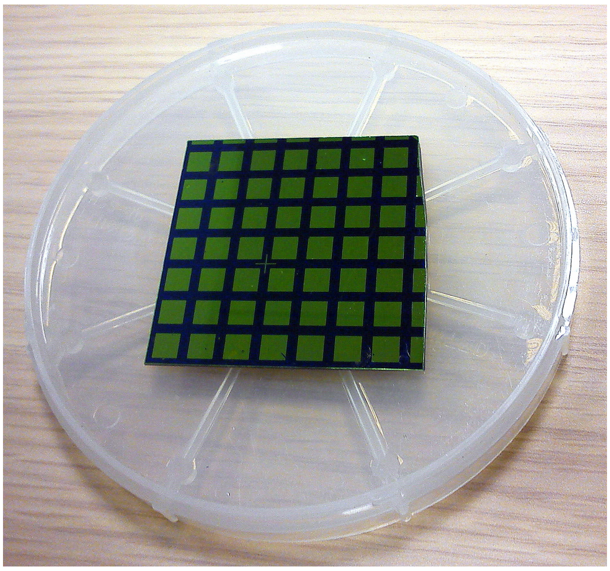

Figure 2.3. The Pseudo-MOSFET technique is applied to SOI wafers divided in 5 mm × 5 mm island and separated each other by 2 mm wide trenches of SiO_2.

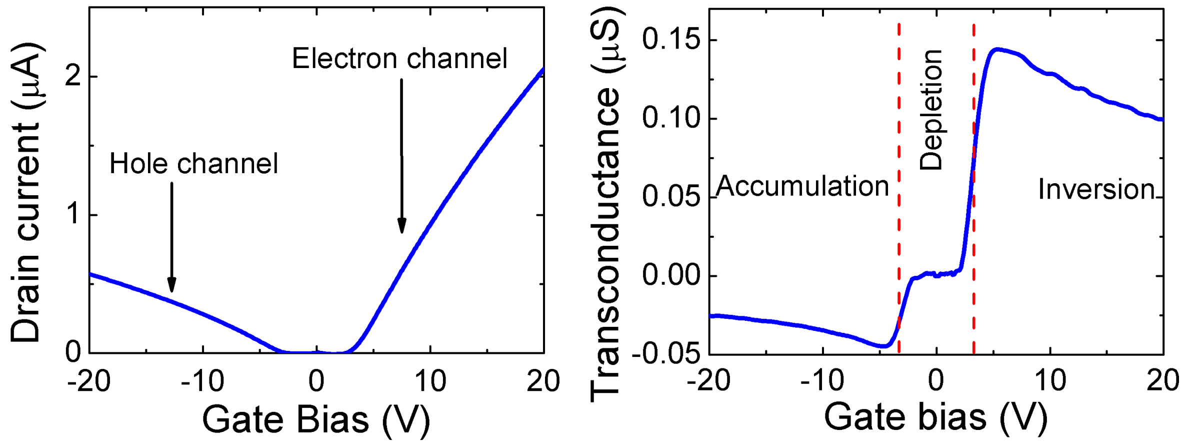

Figure 2.4. Examples of $I_D(V_G)$ and $g_m(V_G)$ experimental characteristics which demonstrate the ambipolar behavior of a Pseudo-transistor. Non-passivated wafer, $t_{Si} = 88$ nm, $t_{BOX} = 145$ nm, $V_D = 20$ mV.

Then, since the experimental curves are similar to those measured for fully processed MOSFETs, the electrical parameters, such as flat-band/threshold voltage, carrier mobility or interface traps density, can be extracted through well-established standard equations [CML00]. This way, if the drain voltage used in all the experiments (V_D) is low enough to ensure an ohmic behavior, the $I_D(V_G)$ current curve can be approximated by the simplified MOSFET formula:

$$I_D = f_{g2p} C_{BOX} \mu (V_G - V_{TH-H/TH-E}) V_D \tag{2.1}$$

where $C_{BOX} = \epsilon_{BOX}/t_{BOX}$ represents the capacitance associated to the BOX per area unit, and $V_{TH-H/TH-E}$ is the threshold voltage for hole/electron channels, respectively. The mobility attenuation factors have been neglected in the equation [SB06]. Similarly, the transconductance is defined as the derivative of the current equation with respect to the gate bias:

$$g_m = \frac{dI_D}{dV_G} = f_{g2p} C_{BOX} \mu V_D \tag{2.2}$$

Finally, an especial mention must be done for the *geometric coefficient*, f_{g2p}, which accounts for the device size ratio (similar to the W/L relationship in MOSFETs). Because of the inevitably non-parallel current lines between the two point contacts source and drain, this factor cannot be determined exactly and usually takes the value of $f_{g2p} \approx 0.75$[2] [CW92] [KBS+05].

2.1.4 Y-function

One usual way used in semiconductor research to calculate the threshold voltage from experimental results (V_{TH-H} and V_{TH-E} for hole and electron channel, respectively) is through the peak of the second derivative of the $I_D(V_G)$ characteristics ($d^2I_D/dV_G{}^2$) or from the inflexion point of the transconductance curve $g_m(V_G)$ [RCG09].

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[2] Detailed investigation of this factor will be presented in Section 4.3

This method is simple, however, it usually entails the generation of a noisy curve, in particular if the experimental curve is extracted taking few points in the sweep. Another feasible and successful option consists of applying the so called *Y-function* [Ghi88] [RCG07] calculated by dividing the current curve between the square root of the transconductance:

$$Y = \frac{I_D}{\sqrt{g_m}} = \sqrt{f_{g2p} C_{BOX} \mu V_D}(V_G - V_{TH-H/TH-E}) \tag{2.3}$$

Y-function provides a linear behavior for high values of V_G and the intercept with the horizontal axis yields the value of the threshold voltage (V_{TH-H}/V_{TH-E}). It was the main method employed in this work to obtain the threshold voltage from measurements, for instance, to analyze the effects of the probe pressure in Section 2.3.1.

Finally, the carrier mobility for electrons and holes will be also extracted from Eq. (2.3) as:

$$\mu = \frac{\left(\frac{Y}{V_G - V_{TH-H/TH-E}}\right)^2}{f_{g2p} C_{BOX} V_D} \tag{2.4}$$

2.2 Theoretical models for ultrathin passivated Ψ-MOSFETs

When dealing with experimental values, it is important to ensure the validity of the results obtained, such as the threshold voltages or mobility values, by comparing them with theoretical models. In the case of Pseudo-MOS transistors, the first equations developed for thick SOI films [CW92] started to mismatch from the actual behavior when they were applied to thinner samples (in the order of sub-100-nm-thick SOI films). One example is shown in Figure 2.5 where, unlike the *classical* model which assumes a decrease for the threshold voltage with the Silicon thickness, the experimental values demonstrate an opposite behavior for both passivated and non-passivated SOI wafers [HAHC07]).

Thus, models need to be updated accounting for the coupling between layers as well as the thickness dependence.

2.2.1 Two-interfaces model

The first adaptation of the classical models were developed for ultra-thin Silicon films maintaining a thick BOX [RCG09]. It was observed that, when the Si film was scaled down, a coupling between the interface states from the top (free) surface and the channel appeared and the usual electrical behavior of the cell changed.

Figure 2.6 shows the energy-band diagram of the Pseudo-MOSFET structure where numbers 1 and 2 are related to the Si film-BOX and free interfaces respectively. The presence of traps at both extremes of Si film is also included (D_{it1} and D_{it2})

The impact of the traps on the device characteristics will be noticeable depending on the basis of the quality of the top surface, i.e. if the top oxide has been passivated or not. Figure 2.7 shows the electrostatic potential profiles obtained by simulations for an ultrathin Pseudo-MOSFET. Depending on the density of states at the top interface (D_{it2}) a significant difference is observed.

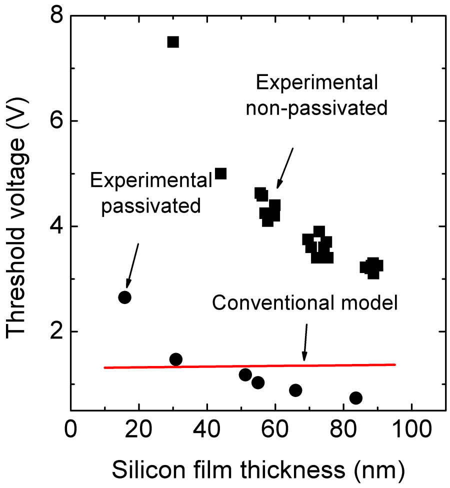

Figure 2.5. Comparison between experimental values of threshold voltage in (circles) passivated and (squares) non-passivated samples [HAHC07] and the conventional Pseudo-MOSFET model [CML00].

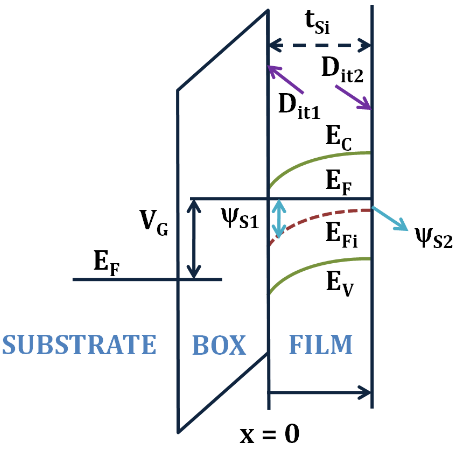

Figure 2.6. Ψ-MOSFET energy-band diagram for positive values of V_G. The substrate-BOX interface is ignored in this first approach.

- For a **passivated surface** (Figure 2.7.(a)), the potential is almost flat and gives rise to volume inversion, which means that the minority carriers are distributed throughout the whole film.
- By contrast, the potential at the **non-passivated surface** (Figure 2.7.(b)) is quasi-linear, being defined by the competition between the gate-induced field and the surface trap-induced field.

On the other hand, the electric field profiles corresponding to Figure 2.7 are reproduced in Figure 2.8.

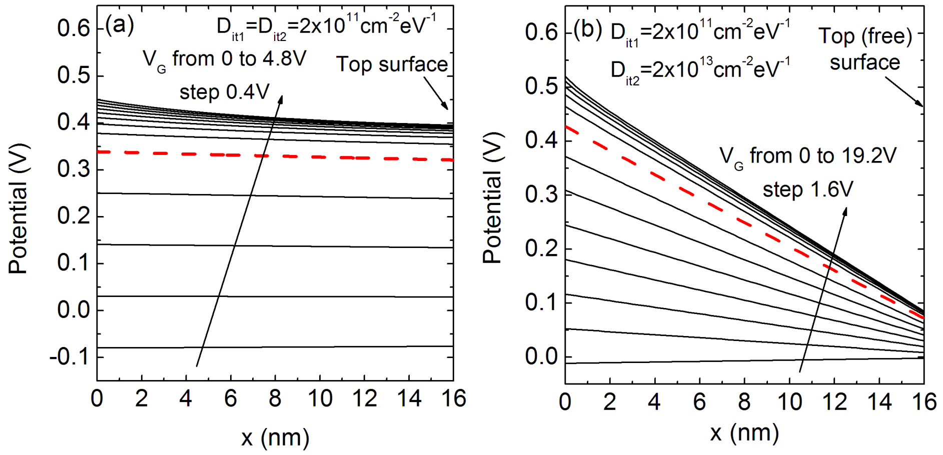

Figure 2.7. In-depth potential profiles from BOX interface to free surface for a 16nm-thick Ψ-MOSFET. (a) Passivated surface with quasi-flat profiles. (b) Non-passivated surface with linear potential variation. Profiles at threshold are presented with dashed line. $N_A = 10^{15}cm^{-3}$, $t_{BOX} = 145$ nm.

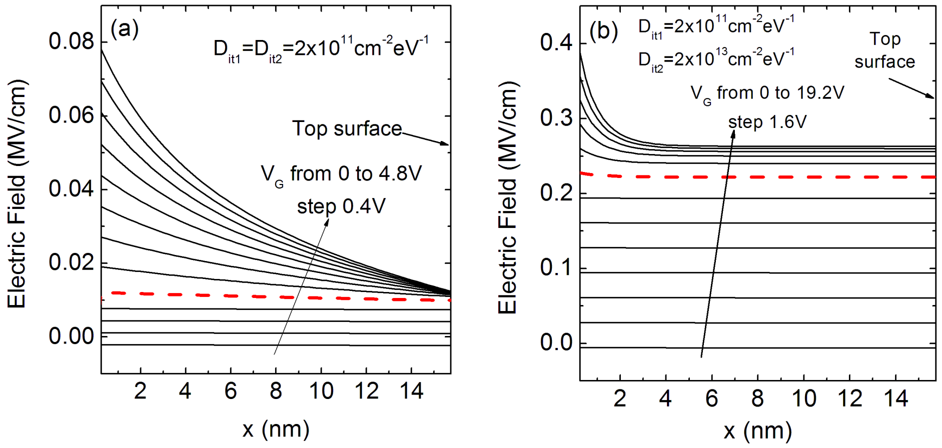

Figure 2.8. Electric field profiles from BOX interface to free surface for a 16nm-thick Ψ-MOSFET with (a) passivated surface and (b) non-passivated surface. Profiles at threshold are presented with dashed line. $N_A = 10^{15}cm^{-3}$, $t_{BOX} = 145$ nm.

- For a **passivated surface** (Figure 2.8.(a)) the field is weakly dependent on the gate bias and remains very low (even in strong inversion) at both interfaces.
- By contrast, for a **non-passivated surface** (Figure 2.8.(b)) the field rises steadily as the gate voltage increases from weak to strong inversion. Both interfaces experience very high fields. In particular, for strong inversion, the field at the Si film/BOX interface can exceed 0.5 MV/cm in 20nm-thick film. This magnitude was analyzed further in Section 4.3 in terms of mobility degradation for thin non-passivated wafers [FrM+15].

To conclude, Figure 2.9 shows a simulation done with ATLAS software from Silvaco company [Fer11] where the potential along the Si film for a Pseudo-MOSFET was reproduced. The presence of traps at the top surface was also considered through their associated charge for several possibilities: $Q_{it2} = 0$ C for an ideal case; $Q_{it2} = -10^{11}$ C corresponds with passivated surface case; $Q_{it2} = -10^{12}$ C and $Q_{it2} = -10^{13}$ C correspond with non-passivated surface samples. As observed, when Q_{it2} increases, so does the slope of the potential, what translated into a clear dependence of the potential in the channel with the potential associated to the top surface. As consequence, the electric field induced in the film becomes higher (verifying the results shown before in Figures 2.7 and 2.8).

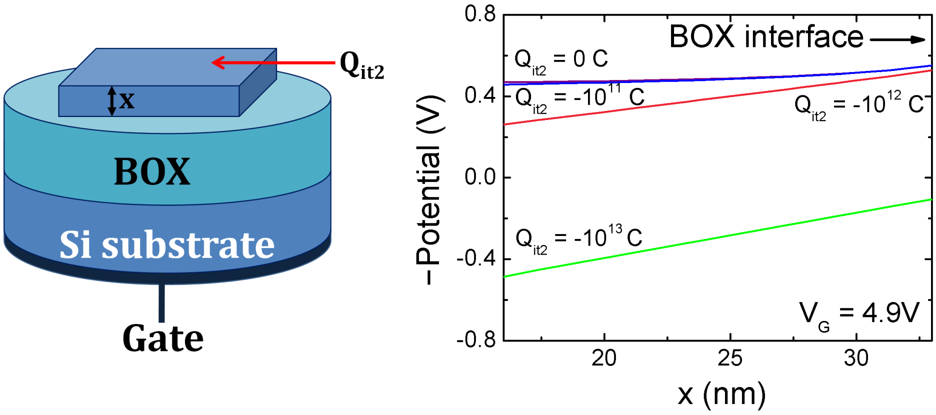

Figure 2.9. In-depth potential profiles from free surface to BOX interface in a Ψ-MOSFET for a certain gate bias upper to threshold voltage. Different trap charges at the top surface have been considered. $N_A = 10^{15} cm^{-3}$, $t_{Si} = 20$ nm, $t_{BOX} = 145$ nm.

Rodriguez *et al.* [RCG09] proposed several mathematical expressions for the threshold voltage extracted from passivated and non-passivated Pseudo-MOSFETs, which are explained in the following sections.

2.2.1.1 Model for passivated Ψ-MOSFET

If the top surface is **passivated** (by cleaning and thermal oxide growth) the traps density is significatively reduced down to the point where it can be considered negligible [HAHC07] ($D_{it2} = 2 \times 10^{11} cm^{-2} eV^{-1}$). Based on the 1-D numerical solution of Poisson equation for a low doped Si film region (N_A is insignificant in comparison with the inversion charge of mobile carriers), the final expression for the threshold voltage results [RCG09]:

$$V_T = \phi_{fb} + \frac{2kT}{q}\left(1 + \frac{C_{it1}}{C_{BOX}}\right) ln\left[\frac{1}{t_{Si}}\sqrt{\frac{2kT\epsilon_{Si}}{q^2 n_i}}\right] \tag{2.5}$$

where ϕ_{fb} symbolizes the difference between the film and substrate Fermi levels ($\phi_{fb} \approx 0$ in our case, since the Si film and the Si substrate below the BOX are equally doped), $C_{it1} = qD_{it1}$ is the capacitance associated to the trap density existing at the Si film/BOX interface, C_{BOX} represents the BOX capacitance, ϵ_{Si} defines the Silicon permittivity, q is the electron charge and, finally, n_i is the intrinsic carrier concentration.

2.2.1.2 Model for non-passivated Ψ-MOSFET

On the other hand, in the case of **non-passivated surfaces** (top oxide is grown spontaneously), the trap density at the top surface is no longer negligible and takes high values (typically $D_{it2} = 2 \times 10^{13} cm^{-2} eV^{-1}$ [HAHC07]). In these samples the top-surface field becomes quite significant[3]. The Gauss law establishes a new boundary condition and the resulting expression for the threshold voltage is [RCG09]:

$$V_T = \phi_{fb} + 2\phi_F \left(1 + \frac{C_{it1}}{C_{BOX}} + \frac{C_{Si}C_{it2}}{C_{BOX}(C_{Si} + C_{it2})}\right) \tag{2.6}$$

where the dependence with the the traps density at the top surface is included by the capacitance $C_{it2} = qD_{it2}$.

To conclude, Figure 2.10 shows a comparison [RCG09] between the updated models and the experimental results in order to demonstrate the validity of the Eq. (2.5) and (2.6).

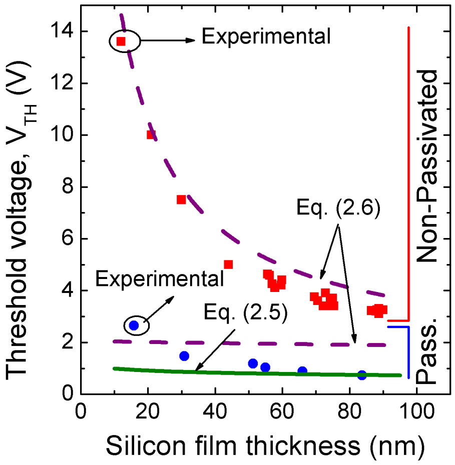

Figure 2.10. Threshold voltage versus film thickness. Comparison between models and experimental data: (squares) non-passivated surface with $D_{it2} = 2 \times 10^{13} cm^{-2} eV^{-1}$ and (circles) passivated surface with $D_{it2} = 2 \times 10^{11} cm^{-2} eV^{-1}$. $D_{it1} = 2 \times 10^{11} cm^{-2} eV^{-1}$, $t_{Si} = 20$ nm, $t_{BOX} = 145$ nm.

2.2.2 Three-interfaces model

The model presented before can be extended to ultrathin BOX layers. In this case, the quality of the BOX/substrate interface can also affect the channel properties. For instance, Figure 2.11 shows the relative error of the threshold voltages extracted numerically when the third interface is neglected or not. The results show that the error increases with the decrease of the BOX thickness. The effect is even more noticeable for the passivated case, where the error reaches an unacceptable 20% in an standard 145nm-thick BOX.

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[3] The impact of the top surface on the device performance will be deeply examined in terms of effective field in Chapter 4.

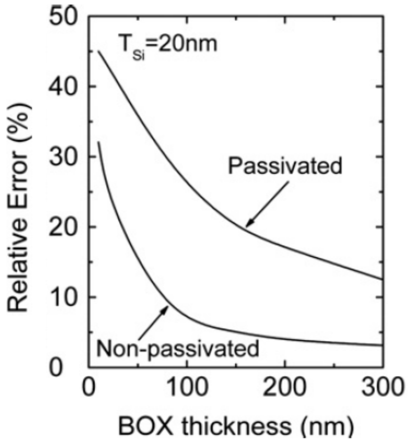

Figure 2.11. Relative error calculated from threshold voltages obtained through simulations when third interface BOX-substrate is accounted for and when is not (adapted from [RCM+11]).

Two different approaches to model this situation were proposed by Rodriguez *et al.* [RCM+11]: the first case is based on the boundary conditions at the BOX interface; the second one takes advantage of the capacitive structure associated to any SOI substrate.

2.2.2.1 Analytical model

Figure 2.12 shows the energy-band diagram associated to a SOI wafer with ultrathin BOX and Si film layers. The difference found here with respect to the Figure 2.6 is that band bending at the BOX-substrate interface, D_{it3}, becomes important.

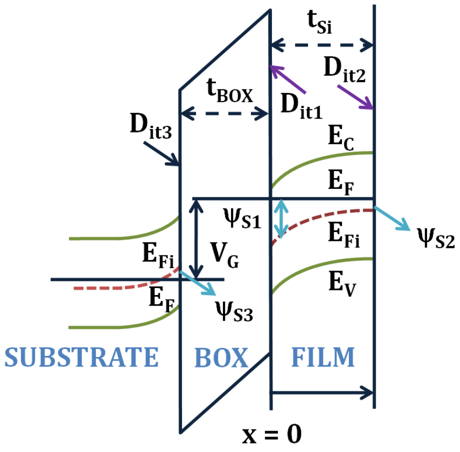

Figure 2.12. Ψ-MOSFET energy-band diagram for positive values of V_G taking into account the effect of BOX-substrate interface (D_{it3}).

After solving Gauss Law, now considering new boundary conditions at both extremes of the BOX, and the non-existence of charge inside the insulator, the final formula for the threshold voltage at threshold condition ($\psi_{S1} = 2\phi_F$) resulted [RCM+11]:

$$V_T = \phi_{fb} + 2\phi_F \left(1 + \lambda + \frac{C_{it1}}{C_{BOX}} + \frac{C_{Si}C_{it2}}{C_{BOX}(C_{Si} + C_{it2})}\right) \tag{2.7}$$

where λ symbolizes a *coupling factor* that relates the potential ψ_{S1} and ψ_{S3} and it is obtained by numerical simulations.

2.2.2.2 Capacitive model

Another standpoint considers the Pseudo-MOSFET as a stack of capacitors controlling the electrostatic potential at each interface (Figure 2.13.(a)). In this case, the threshold voltage is obtained from the following approximated formula [RCM+11]:

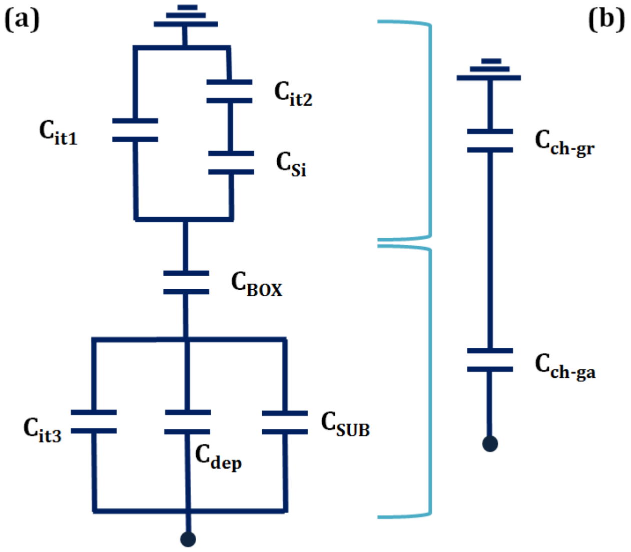

Figure 2.13. Equivalent three-interface capacitance model of a Ψ-MOSFET: (a) general and (b) simplified circuit (after associating some capacitances).

$$V_T = \phi_{fb} + 2\phi_F \left(1 + \frac{C_{ch-gr}}{C_{ch-ga}}\right) \tag{2.8}$$

where C_{ch-gr} represents the total capacitance between the channel and ground (source probe), and C_{ch-ga} is the total capacitance between the channel and the gate terminal (Figure 2.13.(b)):

$$C_{ch-gr} = C_{it1} + C_{it2}||C_{Si} = C_{it1} + \frac{C_{it2}C_{Si}}{C_{it2} + C_{Si}} \tag{2.9}$$

$$C_{ch-ga} = C_{BOX}||\left(C_{it3} + C_{DEP} + C_{SUB}\right) = \frac{C_{BOX}(C_{it3} + C_{DEP} + C_{SUB})}{C_{BOX} + (C_{it3} + C_{DEP} + C_{SUB})} \tag{2.10}$$

$C_{it3} = qD_{it3}$ is the capacitor originated by the traps at the BOX/substrate, C_{SUB} is the substrate accumulation capacitance created when $V_G > 0$ V[4], and C_{DEP} is the substrate depletion capacitance. Replacing the expressions, the final threshold voltage equation obtained is [RCM+11]:

$$V_T = \phi_{fb} + 2\phi_F(1 + \frac{C_{it1}(C_{BOX} + (C_{it3} + C_{DEP} + C_{SUB}))}{C_{BOX} + (C_{it3} + C_{DEP} + C_{SUB})} + \\ + \frac{C_{Si}C_{it2}C_{BOX} + (C_{it3} + C_{DEP} + C_{SUB})}{(C_{Si} + C_{it2})C_{BOX}(C_{it3} + C_{DEP} + C_{SUB})}) \tag{2.11}$$

For this work, all the previous formulas have been used in order to contrast the experimental results obtained in the laboratory with their theoretical values[5].

To conclude this part, Figure 2.14 depicts the accuracy of the models with experimental values of the threshold voltage. The two-interface model (Eq. (2.6)) leads to a lower value of the threshold voltage, since the electrostatic potential drop in the substrate is not captured. If experimental data are fit with this model an overestimation of the density of states at the BOX/Si interface would be obtained.

By contrast, the three-interface models (Eqs. (2.7) and (2.11)) avoid any misleading conclusion extracting the value of the density of states at the film/BOX and substrate/BOX interfaces ($D_{it3} = 10^{11} cm^{-2} eV^{-1}$) [RCM+11]).

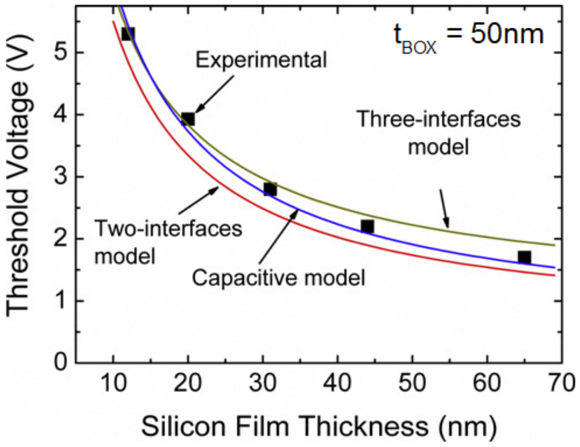

Figure 2.14. Threshold voltage versus Si film thickness. Comparison of the two models described for ultrathin BOX and the existing two-interface model explained in Section 2.2.1 with experimental data from non-passivated wafers. $D_{it1} = 2 \times 10^{11} cm^{-2} eV^{-1}$, $D_{it2} = 2 \times 10^{13} cm^{-2} eV^{-1}$, $D_{it3} = 10^{11} cm^{-2} eV^{-1}$.

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[4] If $V_G < 0$ V the capacitance would be created by inversion.

[5] Furthermore, the capacitive model will be used in Section 3.2.2 to justify the impedance model adjusted in the impedance analyzer when Split-C(V) measurements are performed.

2.3 Impact of the setup parameters on experimental current characteristics

In the following sub-sections, the effect on the experimental current characteristics caused by varying the parameters involved in the Pseudo-MOSFET configuration will be described [WC92].

2.3.1 Implications by changing the probe pressure

When dealing with as-grown SOI samples, it is necessary to carry out an initial adjustment of the probe pressure in order to avoid a degradation of the experimental results due to the perforation of the BOX layer. This initial calibration is an important part of any point-contact measurement and it should not be skipped in any case.

Figures 2.15.(a) and 2.15.(b) show the different V_{TH-E} and g_{max} values obtained in two 145 nm-thick BOX samples when the needle pressure is varied from 10 g to 100 g[6] (for $V_G > 0$ V, electron channel). As observed, whereas V_{TH-E} is practically not modified for all pressure values, g_{max} reflects an improvement when the pressure is increased, being this effect more noticeable for passivated wafers. This transconductance increment is a direct consequence of the reduction of the series resistance associated to the contacts [ISD$^+$09]. Nevertheless, there exists a determined pressure for which g_{max} becomes saturated and applying higher pressure on the probes only may cause damage to the samples. In all the experiments, caution must be called in order not to overcome this limit.

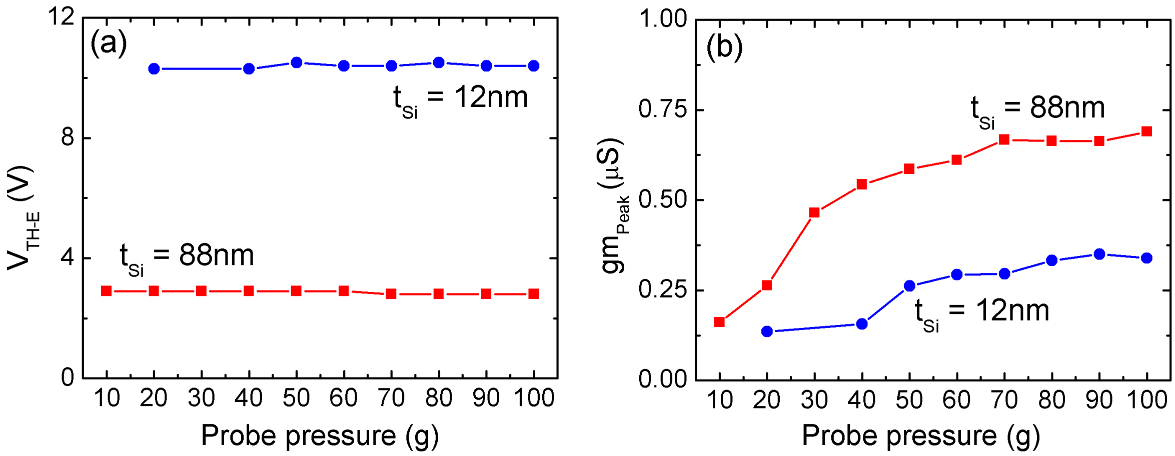

Figure 2.15. Variation of (a) the threshold voltage and (b) the peak value for the transconductance as a function of the probe pressure when an electron channel is induced in two of non-passivated samples. $V_D = 20$ mV

On the other hand, when the layer dimensions are scaled down, the risk of perforating the BOX with the needles and, consequently, reaching the substrate increases [ISD$^+$09]. The phenomenon is illustrated for a 25nm-thick BOX wafer in Figure 2.16. The I-V curves start degrading at a certain pressure, until they no longer show the usual behavior (at 80 g). Thus, when the substrate is drilled, two possibilities are observed depending on the gate bias values:

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[6] The pressure used for the needles is referred by the equivalent weight in grams applied on them.

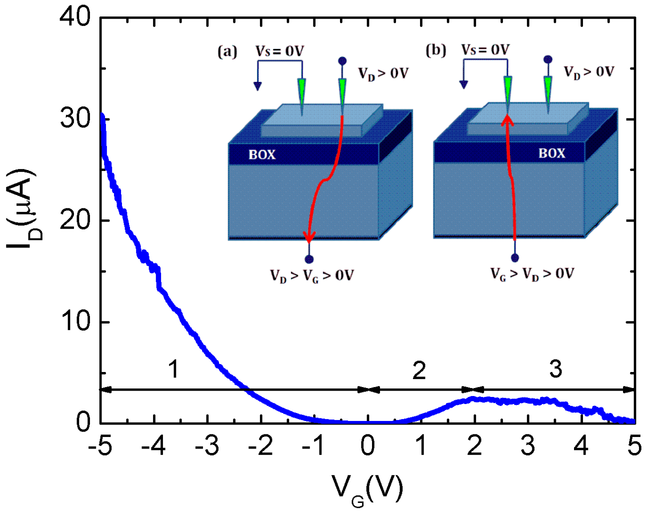

Figure 2.16. Current characteristics obtained as a function of the gate bias. At 80g the needles penetrate totally into the substrate. $t_{Si} = 88$ nm, $t_{BOX} = 25$ nm, $V_D = 20$ mV.

- If the gate bias takes negative values ($V_G < 0V$), the voltage drop between drain and gate exceeds that corresponding to the difference between drain and source. Because of that, most of the leakage current goes from gate to drain (region 1 in Figure 2.16).
- On the other hand, when the gate is positively biased ($V_G > 0V$), the $I_D(V_G)$ characteristic begins to increase (region 2 in Figure 2.16 case (a)) until the voltage drop between gate and source exceeds that relative to drain and source (Figure 2.16 case (b)). When that occurs the drain current decreases dramatically at the same time that the gate current strongly increases (region 3 in Figure 2.16).

Finally, it is worth mentioning the fact that V_{TH} is much higher for the wafer whose Si film thickness is lower (Figure 2.15.(a)). The reason comes from the existence of defects or interface traps in the top native oxide. Although the effect of the top surface on the channel properties will be widely explained in Chapter 4, it could be mentioned that, when the film is reduced, the traps have more influence on the channel carriers and the electrostatic potential across the film is modified [HAHC07]. To compensate the deviation and to be able to create the channel between source and drain, a higher gate bias is required.

In short, the optimum pressure does depend on the Si film and BOX thicknesses and it has to be always calibrated prior to perform the measurements.

2.3.2 Implications of changing the probes interdistance

The minimum distance between two needles in the Jandel station employed in this work was 1.59 mm. Nevertheless, it was also possible to achieve larger distances as 3.18 mm and 4.77 mm in the equipment by simply leaving one or two needles spare between the experimental contacts used (Figure 2.17 left).

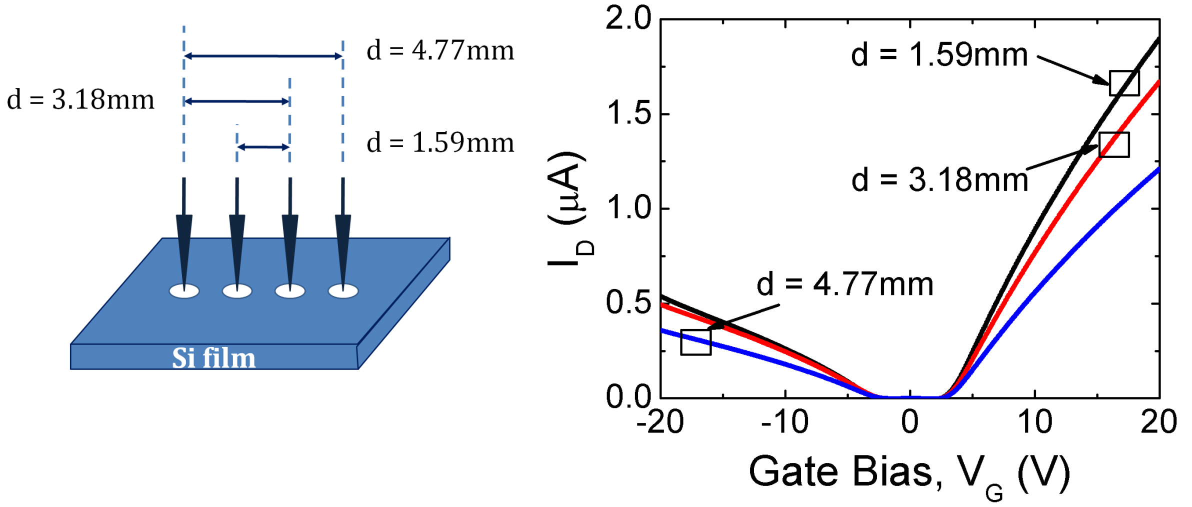

Figure 2.17. (Left) Distance between probes selection. (Right) Current characteristics obtained as a function of the gate bias for different probe interdistances. Non-passivated wafer, $t_{Si} = 88$ nm, $t_{BOX} = 145$ nm, $V_D = 20$ mV, P = 80 g.

Static $I_D(V_G)$ measurements were obtained for SOI wafers varying the probe interdistance (Figure 2.17). In the three cases presented, the results show the same tendency: the larger the distance is, the lower current levels are achieved for the same gate voltage. This is because the geometric factor, f_{g2p} changes when the separation between the needles is modified.

2.3.3 Measurements on different cells

The implementation of a statistical study about how electrical parameters changed along the different cells that compound a Pseudo-MOSFET wafer was also carried out. For that, thirty cells from three samples[7] fabricated at two different institutions, Microelectronics National Center in Barcelona (Spain) and SOITEC in Grenoble (France), were examined by performing I-V characteristics at 80 g probe pressure (Figure 2.18). The dimensions of all substrates were approximately 15nm-thick Si film and 145nm-thick BOX (see Table 2.1).

Sample name	t_{Si} **(nm)**	t_{BOX} **(nm)**	**Surface**
1-A	17.3	146.9	Passivated $t_{Ox\_Sup} = 21.1$ nm
MU003	12	145	Non-passivated
MU005	12	145	Passivated, $t_{Ox\_Sup} = 4$ nm

Table 2.1. Specifications of the wafers used in the statistical study.

Several histograms were plotted after the extraction of the threshold voltages from the peak of the transconductance and the carrier mobility by applying the Y-function (Section 2.1.4). Figure 2.19 illustrates the histograms associated to threshold voltages as an example.

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[7] The description of the complete batch of wafers is found in Appendix B.

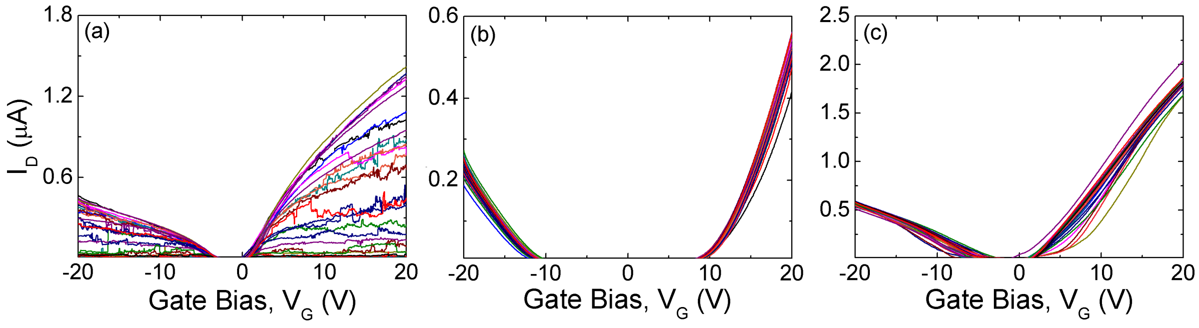

Figure 2.18. Current characteristics obtained as a function of the gate bias for the samples: (a) 1-A (t_{Si} = 17.3 nm, t_{BOX} = 146.9 nm); (b) MU003 (t_{Si} = 12 nm, t_{BOX} = 145 nm, Non-passivated surface), and (c) MU005 (t_{Si} = 12 nm, t_{BOX} = 145 nm, Passivated surface). $V_D = 20$ mV, P = 80 g.

Table 2.2 includes an overview of the main statistical parameters considered in this study: the mean ($< V_{TH} >$ or $< gm_{Peak} >$), the standard deviation (σV_{TH} or σgm_{Peak}), and the range (the difference between the maximum and minimum value extracted), R_{VTH} or R_{gmPeak} [HDH05]. Some considerations are observed from the different results:

Sample name	$< V_{TH-H} >$ (V)	σV_{TH-H} (V)	R_{VTH-H} (V)	$< V_{TH-E} >$ (V)	σV_{TH-E} (V)	R_{VTH-E} (V)
1-A	-3.64	0.58	3.15	0.41	0.31	1.25
MU003	-11.47	0.38	2.10	10.59	0.75	2.60
MU005	-5.14	1.05	4.60	1.41	0.30	1.20
	$< gm_{PeakH} >$ (nS)	σgm_{PeakH} (nS)	$R_{gmPeakH}$ (nS)	$< gm_{PeakE} >$ (nS)	σgm_{PeakE} (nS)	$R_{gmPeakE}$ (nS)
1-A	-34.36	18.53	60.01	84.35	39.39	118.95
MU003	-31.34	12.15	71.97	81.15	14.26	54.27
MU005	-56.08	7.44	31.43	116.50	4.92	16.80

Table 2.2. Statistical data extracted from the experimental measurements.

- Most of the graphics follow a normal distribution where a peak value corresponds with the mean of the data. Nevertheless, the curves are not entirely symmetrical and this is related to the large variability existing in the I-V characteristics performed for the 30 cells (Figure 2.18).
- Although the wafer 1-A presents the lowest values for the threshold voltages, its deviations and ranges are the worst in comparison with those from the rest of the samples.
- In wafers MU003 and MU005 it is noted that the passivation process reduces the V_{TH-H} by 66% and the V_{TH-E} by 87%. Due to the diminution of the traps density at the top surface of the sample: a lower threshold voltage is required to create the channel [HAHC07].

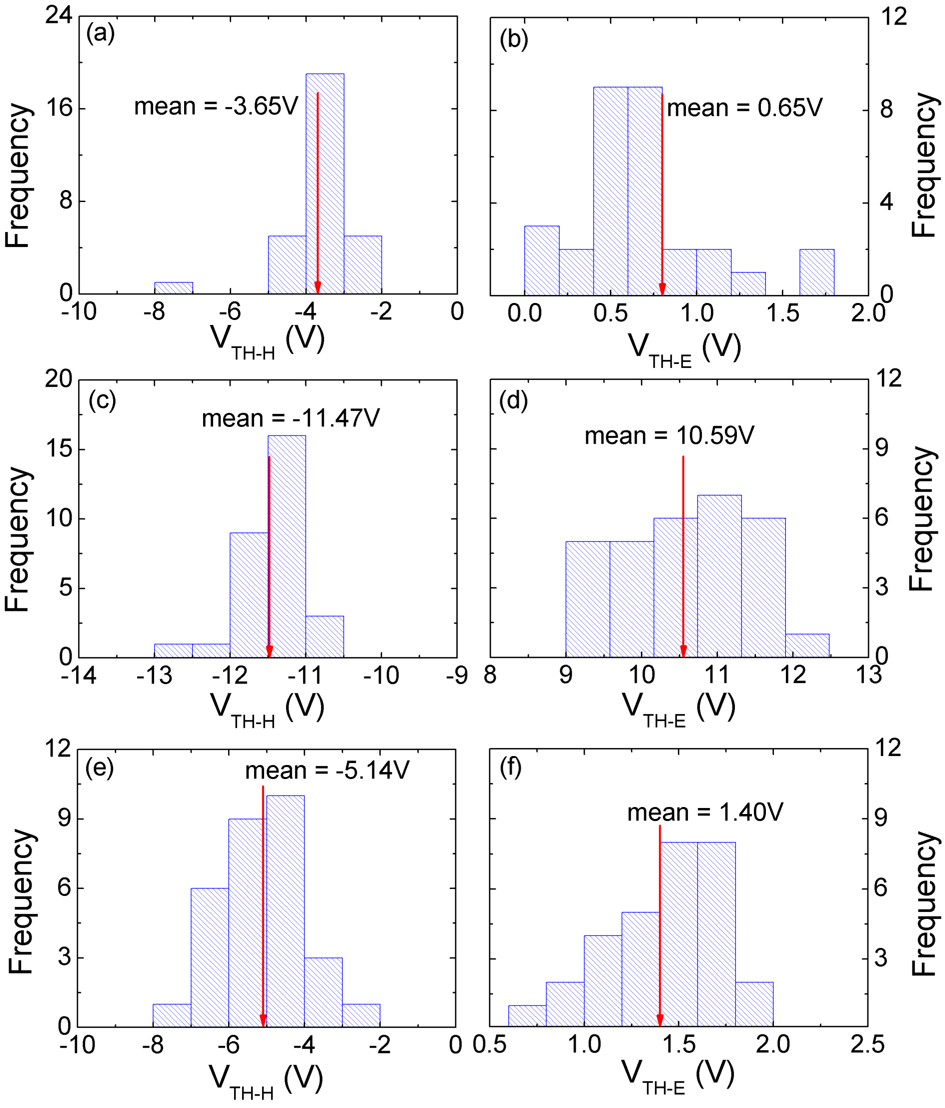

Figure 2.19. Histograms associated to the threshold voltages extracted from I-V characteristics for (a)-(c)-(e) holes and (b)-(d)-(f) electron channels. Samples: (a)-(b) 1-A (t_{Si} = 17.3 nm, t_{BOX} = 146.9 nm); (c)-(d) MU003 (t_{Si} = 12 nm, t_{BOX} = 145 nm, Non-passivated surface), and (e)-(f) MU005 (t_{Si} = 12 nm, t_{BOX} = 145 nm, Passivated surface). V_D = 20 mV, P = 80 g.

Others electrical parameters such as the carrier mobility were only compared between wafers MU003 and MU005 (Figure 2.20, Table 2.3) because of the bad results obtained in the current curves for the sample 1-A.

Sample name	$<\mu_P>$ (V)	$\sigma\mu_P$ (V)	R_{μ_P} (V)	$<\mu_N>$ (V)	$\sigma\mu_N$ (V)	R_{μ_N} (V)
MU003	28.01	3.17	15.01	59.33	5.39	24.78
MU005	145.48	13.05	56.42	373.86	23.99	94.10

Table 2.3. Statistical data extracted from the experimental measurements.

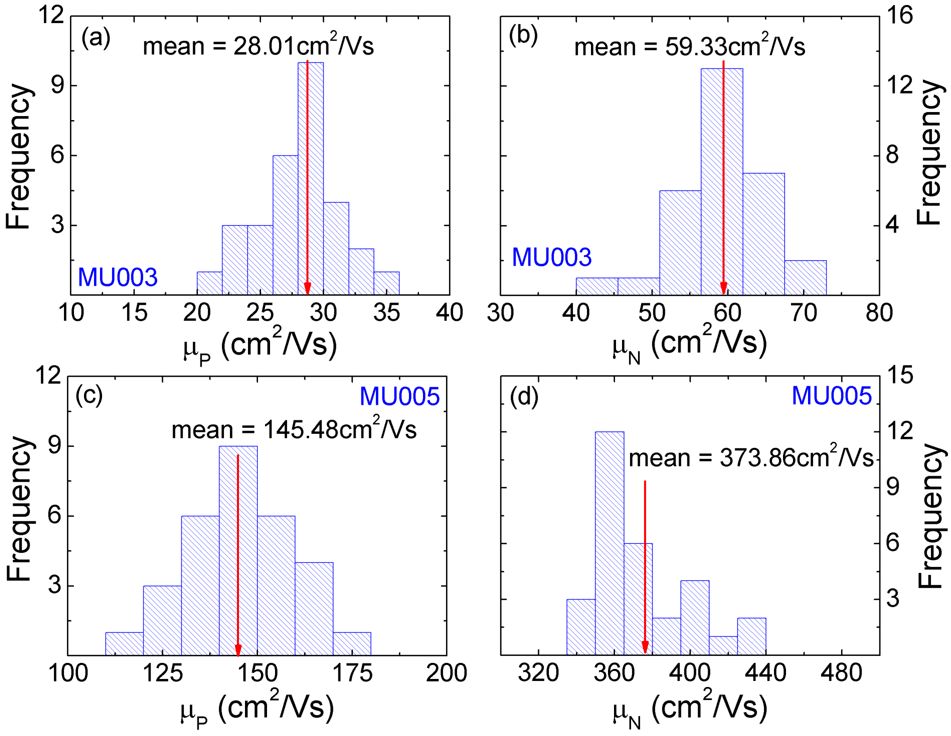

Figure 2.20. Histograms associated to the carrier mobility extracted from I-V characteristics for (a)-(c) holes and (b)-(d) electron channels. Samples: (a)-(b) MU003 (t_{Si} = 12 nm, t_{BOX} = 145 nm, Non-passivated surface), and (c)-(d) MU005 (t_{Si} = 12 nm, t_{BOX} = 145 nm, Passivated surface). V_D = 20 mV, P = 80 g.

The main effect to emphasize with respect to mobility results is the impact of the surface passivation on wafers MU003 and MU005 [HAHC07]. In these samples, the hole mobility increases five times after the passivation. Regarding electron mobility, the gain is even more significant, since it is multiplied by a factor of six. This achievement demonstrates again how the quality of the top surface affects directly the electrical behavior of the wafers, issue widely covered in Chapter 4.

In short, the two samples MU003 and MU005 present, in general, better electrical behavior than the wafer 1-A in terms of variability in the static curves. Because of that, it would be discarded from any work where parameters as the carrier mobility will play a crucial role. Nevertheless, all of the samples show similar behavior with respect to the threshold voltage values, so they all could serve for other studies, for instance, where the interest is focused on how this parameter varies when a charge is deposited on the top surface (Section 5.3). In any case, it has been demonstrated that the cells which form a Pseudo-MOSFET present a non-negligible variability in their electrical characteristics depending on the cell measured.

2.3.4 Implications of repeating the measurement

The last work described in this Chapter consisted of the study of the impact of the needles when successive measurements are carried out in the same region of the cell. Figures 2.21.(a) and 2.21.(b) depict the results produced when 50 measurements were done repeatedly by applying the probes both at the same pressure (80 g) and (approximately) the same position. The outcomes reveal that the slope can be slightly modified due to the degradation of the contacts by successive measurements.

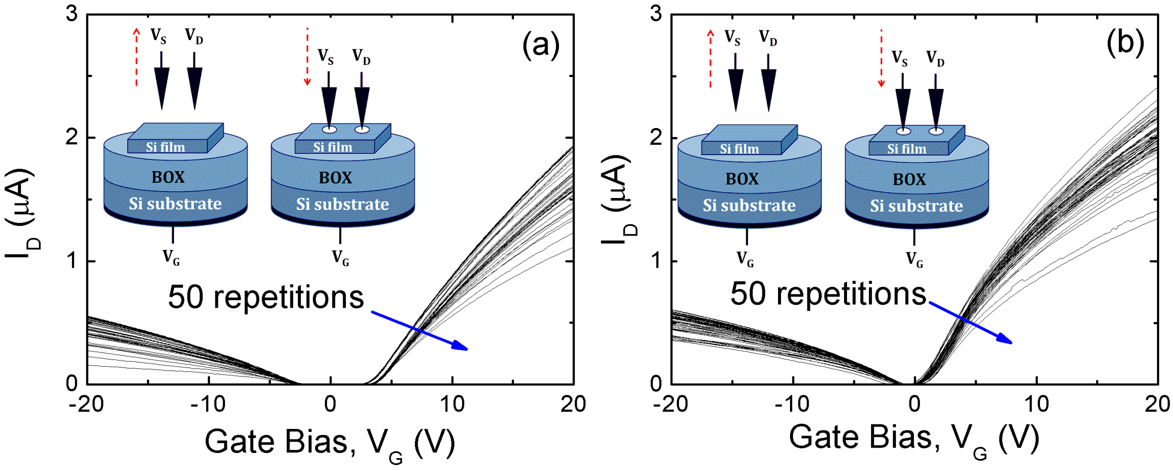

Figure 2.21. Fifty consecutive current characteristics extracted as a function of the gate bias for two different wafers at the same location. (a) Non-passivated and (b) passivated wafers. $t_{Si} = 88$ nm, $t_{BOX} = 145$ nm, $V_D = 20$ mV.

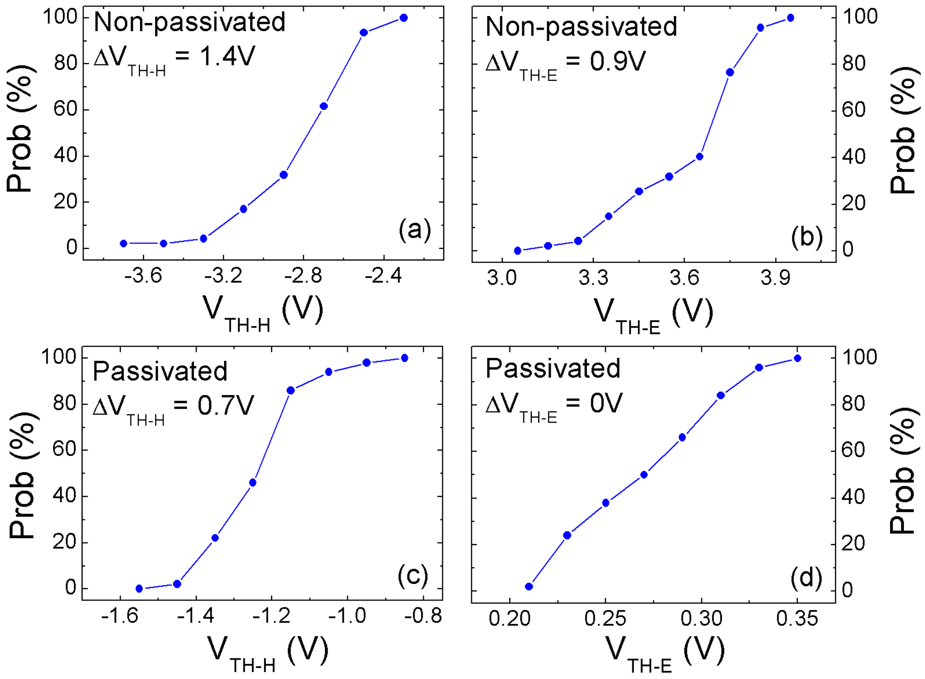

Figure 2.22. Cumulative representations of V_{TH-H} and V_{TH-E} for two samples. (a) Non-passivated and (b) passivated wafer. $t_{Si} = 88$ nm, $t_{BOX} = 145$ nm, $V_D = 20$ mV, P = 80 g.

An statistical study was done based on the experimental data. Figure 2.22 depicts the cumulative representation of the V_{TH-H} and V_{TH-E} values extracted demonstrating that there is no *exact* value for this electrical parameters when the Pseudo-MOSFET technique is employed, but there exists a small variability of the data (independently of the quality of the top surface). The reason comes from the method setup itself: the needles create different stress regions in the structure each time they contact the sample surface; this degradation is translated into the generation of physical defects affecting the current flow for each measurement, that modifies slightly the electrical parameters (such as the threshold voltages).

Because of that, for successive studies, a minimum number of measurements (typically ten) were performed in order to evaluate the mean value of experimental data extracted.

2.4 Conclusions

When dealing with Pseudo-MOSFET configuration, the experimental setup has an important relevance on the electrical characteristics. Aspects, such us the pressure of the needles or the distance between them, cause an significant change in experimental data and an initial calibration must be done.

On the other hand, the density of interface states localized at the interface between the buried oxide and the Silicon film is a critical factor for SOI technology since it degrades the performance of the CMOS circuits fabricated on it. It is also important to take into account the impact of the BOX-substrate interface when working with ultrathin BOX layers (below 25nm). To face this situation, the classical current models have to be updated. In this chapter new equations for both passivated and non-passivated surface have been proposed, which will be employed successively along this project to compare results.

Finally, as a consequence of employing a point-contact technique on bare substrates (without implanted contacts), a non-negligible variability in the electrical parameters between measurements was noticed, and a minimum number of curves will be always performed.

Chapter 3

Novel Insights In Pseudo-MOSFET Technique

Once the basic concepts of the Pseudo-MOSFET technique have been explained, this chapter presents and analyzes recent developments obtained by using this experimental tool. Although, traditionally, the Pseudo-MOSFET technique has been performed through static measurements, more recently, its application has been expanded to the dynamic characterization by combining the Pseudo-MOSFET configuration with Split-C(V) measurements.

3.1 Capacitance measurements

One of the most important studies carried out during the development of this work was the expansion of the Pseudo-MOSFET technique from a static (DC) to a dynamic (AC) characterization. This progress was achieved thanks to the SOI wafer structure, which allows to consider it like a capacitor. Considering a bare p-type SOI sample, if the top surface is grounded (through the needles) and, simultaneously, an AC signal with a negative (or positive) DC component is applied to the substrate (gate), an accumulation of positive charge (or inversion of negative charge) is induced in the channel (Si film/BOX interface). This charge will be compensated with some negative (or positive) charge at the bottom of the BOX (Figure 3.1) and, as consequence, an electric field will be created across the insulator. In short, the sample will have a *capacitor*-like behavior.

If bulk MOSFETs are considered, two kind of capacitive measurements can be performed depending on where the low and high potentials of the capacimeter are connected:

- Keeping the substrate of the transistor grounded, if the gate is connected to the high potential at the same time that the source and drain contacts are together connected to the low one, an *inversion charge* in the channel is induced (Figure 3.2.(a)). In this case, a *gate-to-channel capacitance* is measured [SB06].
- On the other hand, if the source and drain contacts are together grounded, when the substrate is connected to the low potential and the gate is connected to the high one, the variation of the *depletion charge* is analyzed (Figure 3.2.(b)). Then, a *gate-to-substrate capacitance* is induced.

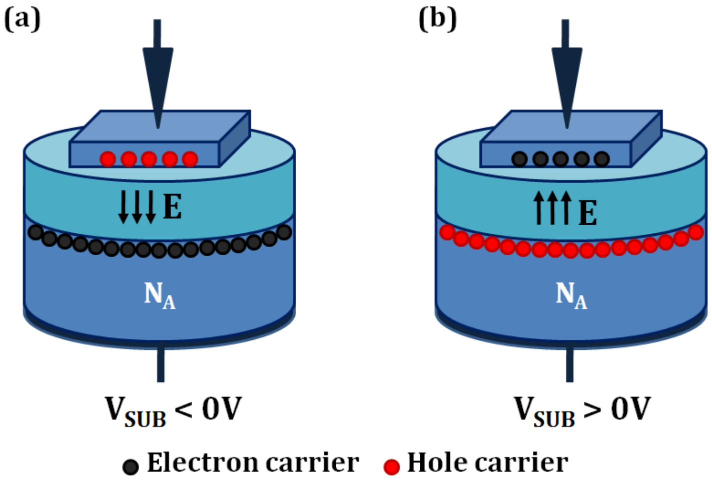
(a)
(b)
E
E
N_A
N_A
V_SUB < 0V
V_SUB > 0V
● Electron carrier
● Hole carrier

Figure 3.1. The SOI sample can be treated as a capacitor formed by the BOX and the Silicon layers. The direction of the electric field depends on the polarity of the DC bias applied through the impedance analyzer.

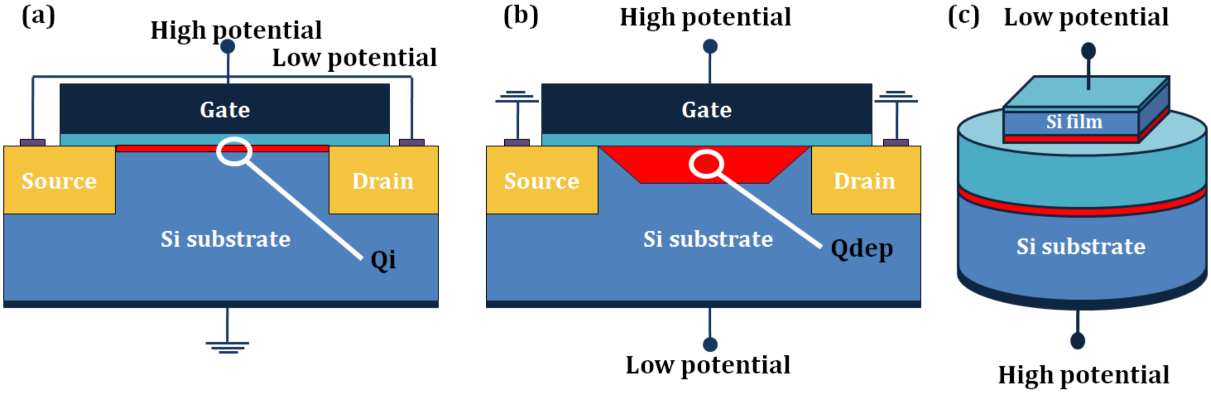
(a)
High potential
Low potential
Gate
Source
Drain
Si substrate
Qi
(b)
High potential
Gate
Source
Drain
Si substrate
Qdep
Low potential
(c)
Low potential
Si film
Si substrate
High potential

Figure 3.2. Schematic of the configurations used for the extraction of the (a) gate-to-channel and (b) gate-to-substrate capacitance in bulk MOSFETs. The connection of the low and high potentials are pointed out in each case. (c) Comparison with the SOI wafer case.

Due to the lack of both drain and source contacts in a Pseudo-MOSFET sample, only *gate-to-channel measurements* (hereinafter C_{GC}) are possible to be performed (Figure 3.2.(c)).

3.1.1 C-V characteristics

When capacitance measurements are carried out on a SOI wafer, it is possible to distinguish different parts in the characteristic depending on the electrical region in which the structure is biased. To facilitate the explanation, Figure 3.3 shows the $C_{GC}(V_G)$ curve of a n-channel MOS capacitor when a AC signal is applied to the gate [SB06] (for a PMOS, the curve will have a similar behavior). The curve is also depicted for two different frequencies: low (ranges from ∼1 Hz to 100 Hz), and high (at ∼1 MHz)[1].

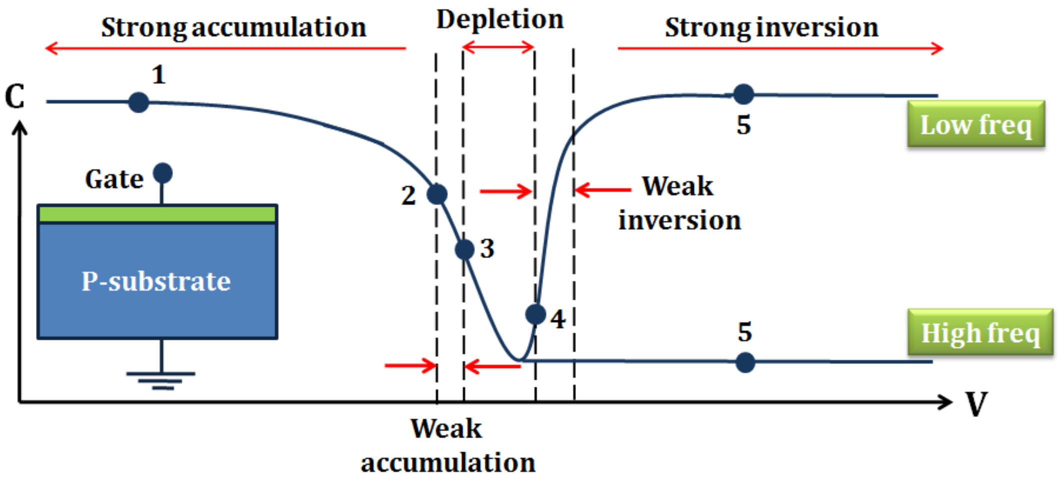

Figure 3.3. C-V relation for an n-channel MOS capacitor as a function of the bias applied to the gate.

- For negative voltages, holes are accumulated at the top of the substrate (channel zone) and the MOS structure appears almost like a parallel-plate capacitor, dominated by the insulator properties (point 1). In other words, the capacitance value in this region is that related to the gate oxide which, in the case of the Pseudo-MOSFET, corresponds to the BOX capacitance (hereinafter, C_{BOX}). For MOS transistors, this maximum value is obtained independently of the frequency used because the majority carriers (holes in a p-type substrate) can respond to AC signal much faster than minority carriers (electrons).
- As the voltage becomes less negative, the semiconductor surface is *depleted* and a depletion-layer capacitance is added in series[2].
- The capacitance decreases as the width of the depletion layer grows from flatband (point 2) to weak inversion (point 3).
- Finally, strong inversion is reached at threshold voltage (point 4).
- The capacitance value depends on whether the measurements are made at low or high frequency:
  - If the gate AC bias is changed *slowly*, there is time for the minority carriers (electrons in a p-type substrate) to be thermally generated, drift across the depletion region to the inversion layer, or go back to the substrate and recombinate. Because of that, the low frequency MOS capacitance in strong inversion is basically that formed by the gate oxide again (or C_{BOX} in SOI wafers).
  - If the gate voltage is varied *rapidly*, the electrons in the inversion layer cannot *follow* the oscillation signal and the MOS capacitance acquires a minimum value, corresponding to a maximum depletion width.

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[1] *low* and *high* terms are used with respect to the generation-recombination rate of the minority carriers in the inversion layer [SB06].

[2] Further explanation for the case of Pseudo-MOSFETs is added in Section 3.2.4

In the next Sections, it will be demonstrated how, when dealing with Pseudo-MOSFET samples with thick BOX layers, the low-doped Silicon substrate enables to obtain similar low-frequency responses for electron and hole channels[3].

3.2 Impact of experimental conditions on capacitance curves

The first task related to capacitance measurements carried out with Pseudo-MOSFET samples consisted of the observation and later discussion of how the different setup parameters may influence on the experimental $C_{GC}(V_{SUB})$ characteristics.

The laboratory equipment necessary for this work was the Agilent 4294A impedance analyzer which, through the 16048G module and four triaxial cables, was connected to the point-contact station[4]. Figure 3.4 shows the configuration setup performed in the laboratory to achieve this task: the substrate (gate) was connected to the two high potentials of the impedance analyzer (Hc, Hp)[5]. On the other hand, the two low potentials (Lc, Lp) were attached to the point-contacts of source and drain in direct contact with the wafer surface. In addition, in order to ensure that the potential from the analyzer is equally divided into the two needles, an extra cable will connect them.

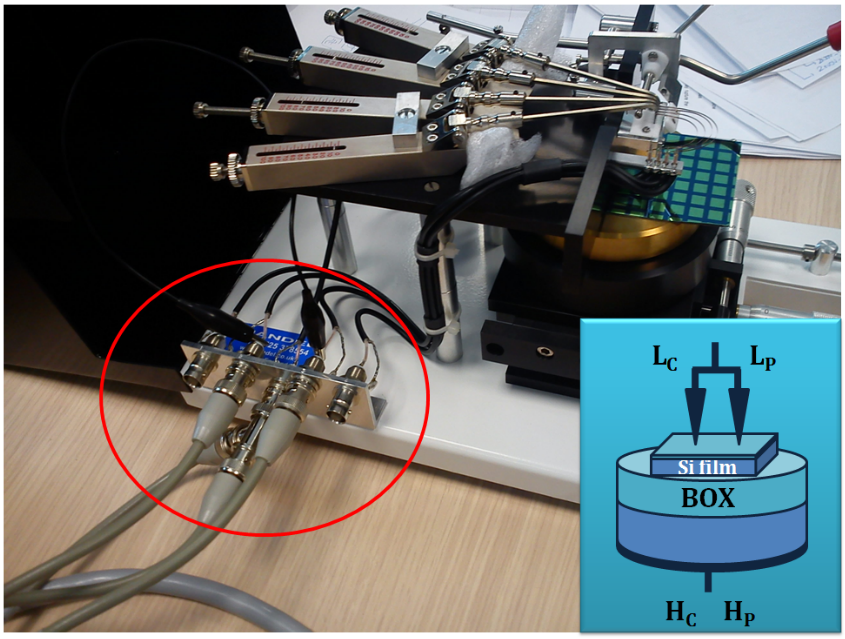

Figure 3.4. Experimental setup of how capacitance measurements were adapted to the Pseudo-MOSFET configuration.

The analyzer was properly calibrated with two corrections before the measurements, *open* and *short*, in order to eliminate the instrument errors and to guarantee the best accuracy for the absolute capacitance measurements [Tec13]:

1. At the *open procedure*, the needles were lifted during the test.

---

[3] The complete explanation for frequency behavior in a Pseudo-MOSFET is found in Section 3.4.1

[4] Appendix B contains more information about laboratory facilities and equipments.

[5] C and P represent the current and potential connections, respectively

2. During the *short* calibration, a piece of an Aluminium sheet with very low serie resistance ($\approx 17\ \Omega$) was placed on the chuck to connect the probes after going down.

Finally, it is worth mentioning that, unless the subsection specifies another BOX thickness, all the experimental results and conclusions shown below were extracted from 145 nm-thick BOX samples.

3.2.1 Variation of the AC input signal level

The first parameter modified was the oscillation level of the input signal generated by the analyzer. Figure 3.5 shows how the saturation value in the experimental curves, i.e. the BOX capacitance, C_{BOX}, as explained in Section 3.1.1, is not affected by this parameter, as well as the threshold voltages for electron and hole channels. From these results, it is concluded that the AC level is not a key setting in the setup while it is maintained in the range of milivolts.

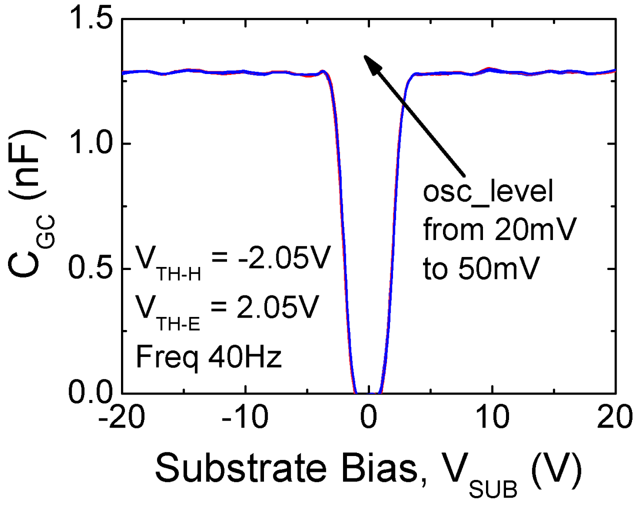

Figure 3.5. Gate-to-channel capacitance curves obtained using a two-needle configuration when the AC level is modified from 20 mV to 50 mV (step 10 mV). Non-passivated wafer, $t_{Si} = 88$ nm, $t_{BOX} = 145$ nm.

3.2.2 Variation of the probes pressure

In Section 2.3.1, the effect of this parameter on the static characteristics was already analyzed at the same time that certain limit values of pressure were established to avoid a perforation of the BOX layer of the samples. Here, the impact of the pressure on the C-V curves is studied further. Figure 3.6 demonstrates the dependence of the maximum value of the capacitance curves (C_{max}) with the needle pressure when a low frequency signal is established at the analyzer (100 Hz). The variation of the threshold voltage for hole and electron channels (V_{TH-H} and V_{TH-E}, respectively) is also depicted, both determined by the peak of the second derivative on the capacitance curves [CL95]. The results demonstrate that V_{TH-H} and V_{TH-E} remain constant regardless the probe pressure. A similar behavior is found for C_{max}: the values increase slightly for higher pressures (less than 5.4%) what indicates a contact improvement (by reducing the drain/source series resistance [ISD$^+$09]).

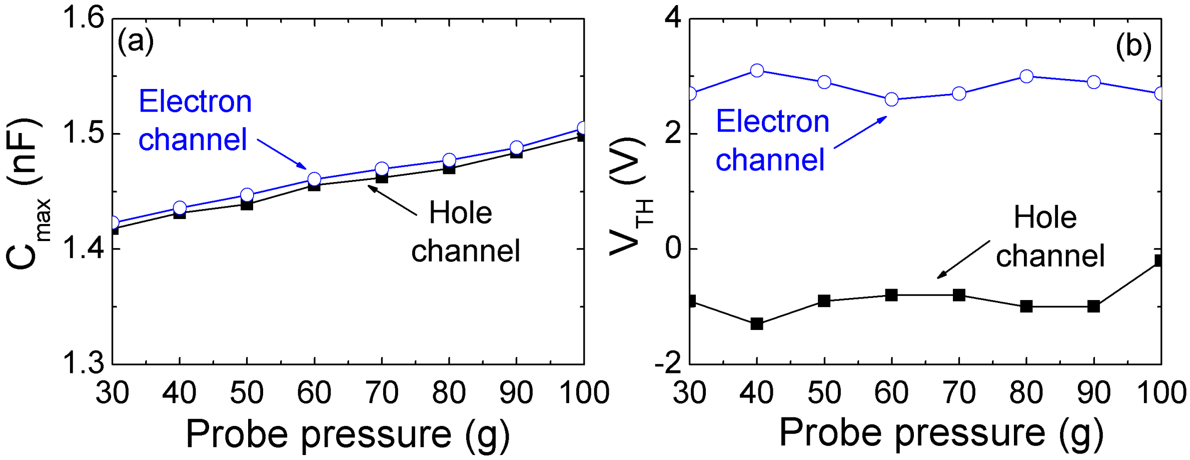

Figure 3.6. (a) Maximum capacitance values at 100Hz and (b) threshold voltages for hole and electron channels obtained as a function of the probe pressure in a two-needle configuration. Non-passivated wafer, t_{Si} = 88 nm, t_{BOX} = 145 nm, Freq. 100 Hz.

Theoretically, a capacitance scheme of a bare SOI wafer was already reported by Rodriguez *et al.* [RCM+11] and explained in Section 2.2.2.2. This model takes into consideration the capacitances associated to the trap densities existing in all the interfaces as well as the capacitances related to the different layers which conform the structure. Nevertheless, for the AC measurements performed in this work, a simplified impedance model was employed instead. The schematic is illustrated in Figure 3.7.(a) [Sch06] and it is formed by several components which model the different parts of the Pseudo-MOSFET configuration:

- a resistance associated to the point contacts (R_{CON})
- a resistance (R_{Si}) and a capacitance (C_{Si}) associated to the Silicon film
- a capacitance (C_{BOX}) associated to the buried oxide
- a resistance (R_{BOX}) associated to the substrate underneath the BOX

The capacitance associated to interface traps have been ignored [RCM+11]. Finally, a parallel resistance in the BOX was not considered due to the extremely low leakage currents in the thick BOX of the samples ($t_{BOX} = 145nm$).

The total impedance in this case is given by:

$$Z_T = R_{CON} + \frac{R_{Si}}{1 + j\omega R_{Si} C_{Si}} + \frac{1}{j\omega C_{BOX}} + R_{SUB} \tag{3.1}$$

It is worth mentioning that, if the pressure of the needles is very low (the minimum value possible with the probe station is about 5 g), the resistance associated to the point contact, R_{CON}, as well as the resistance of the film, R_{Si}, should be taken into account. Nevertheless, the pressure used during the measurements was always high enough to decrease them (higher than 60 g and lower than the limit extracted in Section 2.3.1). At this moment, the needles have practically reached the BOX and the total impedance given by Eq. [3.1] can be turned into

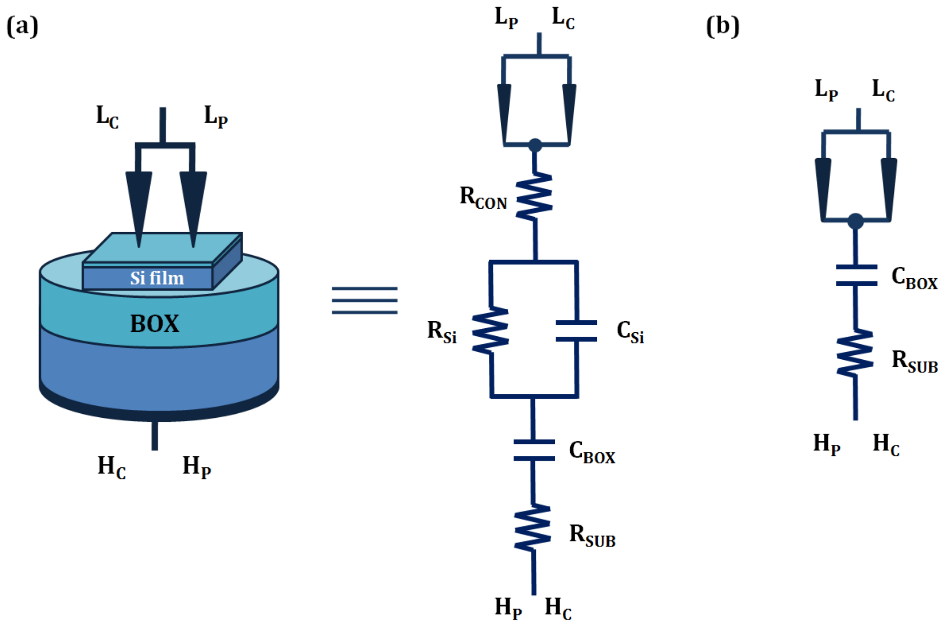

Figure 3.7. (a) Equivalent impedance circuit associated to a Pseudo-MOS structure. (b) Simplified impedance model used in this work.

a $C_{BOX} - R_{SUB}$ series model (Figure 3.7.(b)), where the maximum value of the capacitance correspond to the BOX capacitance. This is the reason why the Pseudo-MOSFET is assumed as a series $C_S - R_S$ impedance model in the impedance analyzer configuration. In fact, in order to verify this assumption, Figure 3.8 shows the capacitance as a function of the frequency for a Pseudo-MOSFET sample where it is clear to observe an RC circuit behavior or, in other words, a low-pass filter. This experimental result further confirms the validity of the model presented in Figure 3.7.(b).

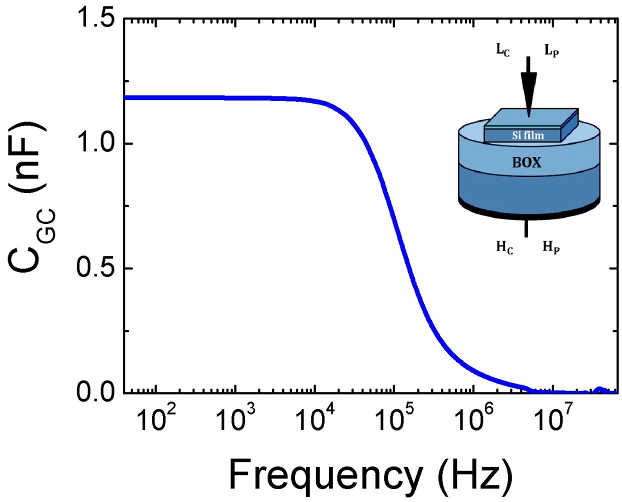

Figure 3.8. Capacitance curves measured using one needle on the surface as a function of the excitation signal frequency from 40 Hz to 60 MHz.

3.2.3 Variation of the number of probes and the probe spacing

Figure 3.9 shows the capacitance curves measured at 300 Hz with one, two and three needles on the surface by selecting two different distances between needles.

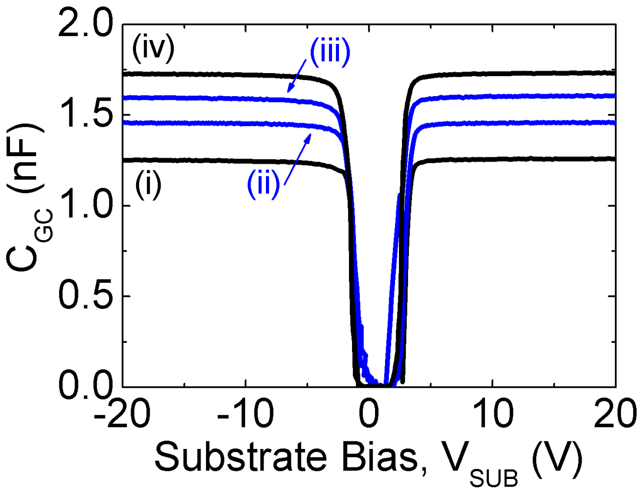

Figure 3.9. Experimental capacitance characteristics with: case (i), one needle on the surface; case (ii), two needles on the surface separated d = 1.59 mm; and case (iii), d = 3.18 mm; case (iv), three needles separated d = 1.59 mm. Non-passivated wafer, t_{Si} = 88 nm, t_{BOX} = 145 nm, oscillation level 20 mV.

As observed, the maximum capacitance varies depending on the number of probes used in the measurements. The reason is related to the *effective surface* concept [FDR+12], which will be studied in Section 3.4. Basically, there is a region in the film where the carriers contribute to the capacitance value, induced by each needle. So, the saturation value of C_{GC} will be higher as the probe number increases. Similarly, when the distance between needles increases, so does the capacitance because the effective areas will be less overlapped.

3.2.4 Variation of the BOX layer thicknesses. Substrate effect

If a thin-BOX wafer is used, a decrease in the maximum value of the capacitance is observed due to the series combination between C_{BOX} and the capacitance related to the substrate depletion layer below the BOX (C_{SUB}) (Figure 3.10.(a)). Unlike the BOX capacitance, the second capacitor is only manifested when the frequency is high enough.

The electrical circuit associated to this approach is shown in Figure 3.10.(b): two capacitors in series form the structure. From this scheme, the theoretical total capacitance can be represented as [DFO+13]:

$$\frac{1}{C_T} = \frac{1}{C_{BOX}} + \frac{1}{C_{SUB}} \tag{3.2}$$

Figure 3.11 shows the comparison between the capacitance curves obtained at a low frequency (600 Hz) with two Pseudo-MOSFETs samples in which, unlike the Si film thickness, the BOX

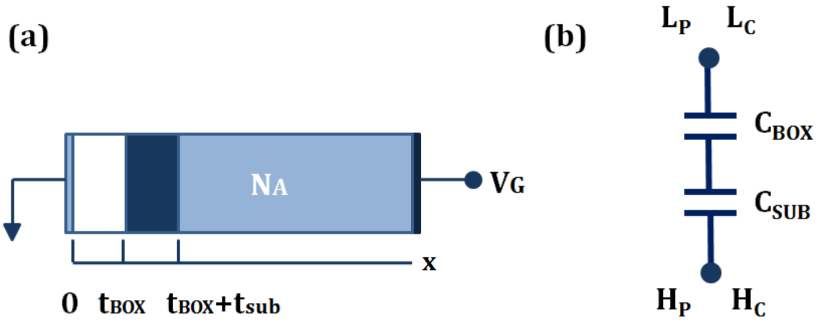

Figure 3.10. (a) When the frequency is high enough, a depletion region in the substrate of a SOI wafer appears. (b) Electrical equivalent circuit.

thicknesses varies (from t_{BOX} = 145 nm to t_{BOX} = 25 nm). A significant difference is found in the maximum values of C_{GC} in accumulation and inversion regions for the ultra-thin BOX sample (not observed for thick BOX layers).

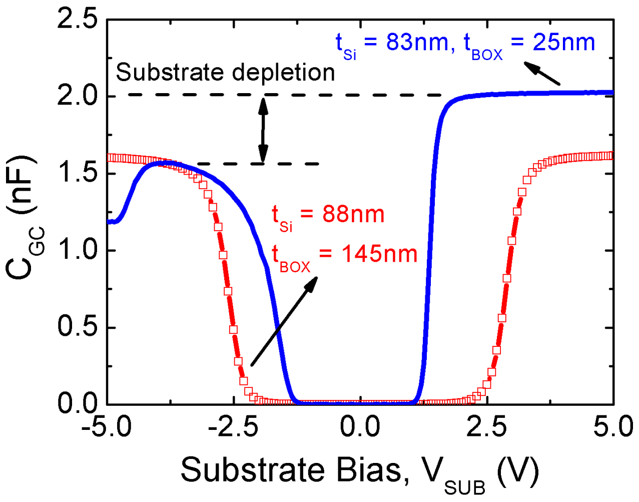

Figure 3.11. Comparison between C-V curves at 600Hz for two Pseudo-MOSFET samples: (line) $t_{Si} = 83$ nm, $t_{BOX} = 35$ nm; (line + symbols) $t_{Si} = 88$ nm, $t_{BOX} = 145$ nm.

This gap is related to the type of SOI substrate. Pseudo-MOSFETs samples are fabricated on Silicon low-doped p-type wafers. The p-type substrate is an inefficient supplier of electrons (minority carriers) and all of them are induced through thermal generation at a very slow rate. Because of that, when the substrate bias is negative ($V_{SUB} < 0$ V), there exists a weak supply of electrons by thermal generation below the BOX that increases the depletion region. As consequence, the maximum capacitance in the curves does not reach the maximum value achieved for positive biases (where holes, majority carriers, are generated below the BOX).

However, for this work only thick-BOX wafers (t_{BOX} = 145 nm) have been considered in order to avoid the substrate effect.

3.3 The Split-C(V) technique

The well-established Split-C(V) method has been used during decades for the characterization of the electrical transport in MOS transistors. Although initially it was developed for aims such as the calculation of the interface trap density or the substrate doping concentration [Koo73], nowadays, its main purpose is to offer a reliable way to determinate the effective mobility of the carriers by direct capacitance measurements [TT02].

Recently, the Split-C(V) method has been extended to the characterization of carrier mobility in bare SOI wafers using the point-contact configuration [DFO+12]. The main benefit is that the technique allows the independent extraction of the inversion or accumulation charge in MOSFETs from the direct measurement of the gate-to-channel capacitance:

$$Q_{acc}(V_G) = \frac{1}{S_{eff}} \int_{V_G}^{V_0} C_{GC}(V_G) dV_G \tag{3.3}$$

$$Q_{inv}(V_G) = \frac{1}{S_{eff}} \int_{V_0}^{V_G} C_{GC}(V_G) dV_G \tag{3.4}$$

where $V_0 = (V_{TH-H} + V_{TH-E})/2 \approx 0$ V since the Si film and the Si substrate below the BOX are equally doped and the interface state density (D_{it}) for electrons and holes have similar values.

S_{eff} is called *effective surface* and it represents the maximum area in a Pseudo-MOSFET sample where the electrons (or holes) are following the AC signal of the impedance analyzer during the capacitance measurements [NSS11]. Since the gate is emulated by the substrate, one may imagine that the inversion/accumulation layer cover the whole sample surface. This is not the actual case and S_{eff} must be considered in detail.

3.4 The effective area in point-contact capacitance measurements

When performing Split-C(V) measurements, there are some peculiarities associated to the Pseudo-Transistor configuration that are not present in a regular MOSFET [KBS+05]:

- On one hand, the transistor effective area during Split-C(V) measurements is not physically defined by a gate rectangle unlike the conventional MOSFETs where the dimensions of the channel are well determined by the gate mask size. On the contrary, in a Pseudo-MOS sample, the active region is limited by the spreading of the carriers [NSS11] and it must be determined experimentally.
- On the other hand, the distance between the needles plays an important role when it becomes comparable to the cell size because of the border effects [KBS+05].

The objective of this Section is to document and analyze these two effects in bare SOI samples. Later, a mathematical model to obtain the effective area will be proposed for both single and multiple-needle configuration.

3.4.1 Impact of the frequency on S_{eff}

The *effective area*, S_{eff}, in a point-contact capacitance measurement on a SOI wafer was previously defined as the maximum region where carriers are participating to the strong accumulation or inversion. Since SOI samples are made with semiconductor materials (Silicon), the spreading of the carriers is strongly dependent on the frequency of the excitation signal and, consequently, S_{eff} has not an fixed value [SB06]. The effect of the frequency of the excitation signal on the gate-to-channel capacitance characteristics is shown in Figure 3.12.(a) and the variation of the maximum value, C_{max}, is depicted in Figure 3.12.(b). Different behaviors are manifested:

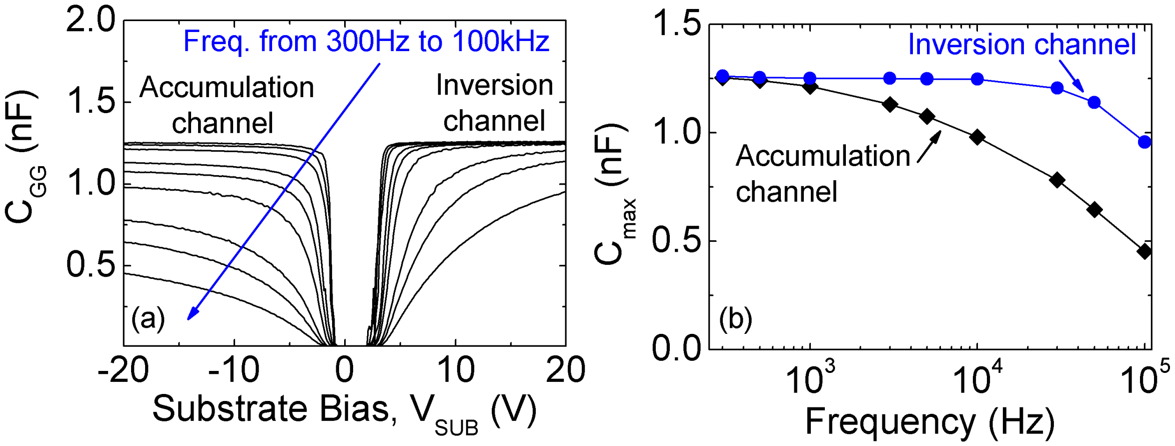

Figure 3.12. (a) Gate-to-channel capacitance curves as a function of the substrate bias obtained for different frequencies using one needle on the surface. (b) Maximum value of the curves obtained as a function of the frequency. Non-passivated wafer, t_{Si} = 88 nm, t_{BOX} = 145 nm, oscillation level 20 mV.

1. For frequencies below 1 kHz, the maximum values remain saturated and the capacitance curves are symmetrical for both holes and electrons[6].
2. In the region between the flat-band and threshold voltages for holes and electrons channels, the capacitance is close to zero, demonstrating that the film behaves as fully depleted. The results guarantee the validity of the Split-C(V) technique in the Pseudo-MOSFET since, under FD conditions, only the electrons (or holes) that form the channel are detected in the measurements.
3. Finally, at higher frequencies, the maximum capacitance decreases (being more remarkable for accumulation channels) and the curves tend to be asymmetrical for electrons and holes sides.

This frequency dependence is attributed to the under-reaction of the carriers that form the channel in the Si film to follow the potential changes caused by the AC signal [NSS11]. At higher frequencies, the spreading of the carriers injected from the needles by a drift mechanism is limited because carriers located far from the contacts are not able to follow the AC signal. The direct consequence is a clear decrease of the effective area, leading to a reduction of the total capacitance.

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[6] Measurements at very low frequency become difficult to perform due to interface-states detection and noise.

This explanation was verified by performing C-V curves when the wafer was illuminated with a wide-spectrum light. Figure 3.13.(a) shows the curves obtained by illuminating the wafer surface at 280lux and using an AC frequency at 5kHz, demonstrating that the p-type side of the curve ($V_{SUB} < 0$ V) is recovered by stimulating the generation of holes (in comparison with the curve obtained in dark conditions).

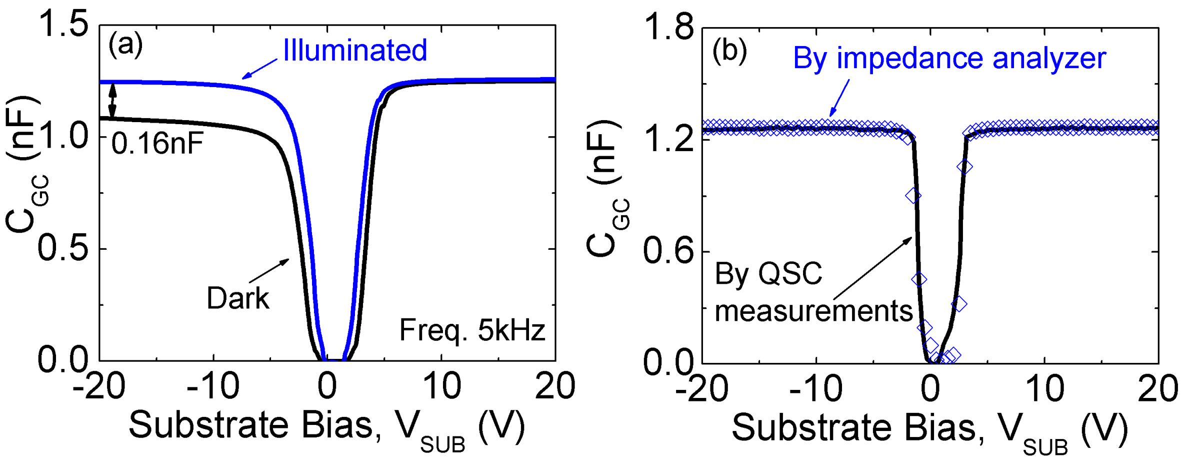

Figure 3.13. (a) Variation of the capacitance characteristics when the wafer is illuminated and when it is not. (b) Gate-to-channel capacitance curves as a function of the substrate bias obtained by the impedance analyzer at 300 Hz (dashed lines) and by QSC measurements (continuous line). Non-passivated wafer, $t_{Si} = 88$ nm, $t_{BOX} = 145$ nm, oscilation level 20 mV.

To conclude this section, quasi-static capacitance measurements (QSC) [Meg86] were performed in order to ensure that the measurements at low frequencies were free from frequency dependence in terms of maximum capacitance. This method measures the gate-to-channel capacitance as the ratio between a constant current driven into the Pseudo-Transistor gate and the variation in the gate/substrate voltage (assuming that the series resistance in Figure 3.7.(b) is independent of time and bias):

$$C_{GC} = \frac{i_G}{\frac{dV_{GB}}{dt}} \tag{3.5}$$

Since the samples had a BOX thick enough ($t_{BOX} > 10$ nm), the use of this technique is justified due to the negligible gate leakage current [Sch06].

Figure 3.13.(b) shows the comparison of the characteristics obtained by QSC method and those produced by using the impedance analyzer at 100 Hz with only one probe placed on the surface. The agreement of both curves demonstrates that, for frequencies below 100 Hz, the capacitance in the Pseudo-MOSFETs remains saturated because carriers have covered the maximum surface according to the potential distribution and the Silicon island dimensions.

3.4.2 Relation between C_{BOX} and S_{eff}

The simplest formula which allows to relate S_{eff} to the gate-to-channel capacitance, assumes that in strong inversion or accumulation (saturation zone in C-V curves) the carriers are able to cover the whole effective area in the MESA island of the wafer, and the value of C_{GC} matches with the BOX capacitance, C_{BOX}:

$$C_{GC} \approx C_{BOX} = S_{eff}\frac{\epsilon_{BOX}}{t_{BOX}} \tag{3.6}$$

where t_{BOX} is the BOX thickness and ϵ_{BOX} is the dielectric constant.

This approximation can be considered valid if C_{GC} is measured at relatively low frequencies as demonstrated by the QSC experiments. At higher frequencies, the total capacitance does not necessarily correspond with BOX capacitance due to the carrier diffusion (as explained in Section 3.4.1).

3.4.3 Carrier density determination

For low frequencies, when high values of $|V_{SUB}|$ are employed, the maximum of the capacitance (or the charge associated) remains saturated what indicates a constant value of S_{eff} due to the lack of frequency dispersion. This area can be also assumed as a constant for others lower V_{SUB} values (always higher than the threshold voltage to activate the channel). In order to exemplify this, Figure 3.14 compares the charge Q_{inv} obtained by integrating the C_{GC} curve of Figure 3.12 at 300 Hz (symbols) by Eq. [3.4], with a linear fitting (line) of Q_{inv} achieved for V_{SUB} values from 15 V to 20 V (where C_{max} does not vary). The agreement is good enough to validate that the S_{eff} remains as a constant for gate voltages $V_{TH-E} < V_G$.

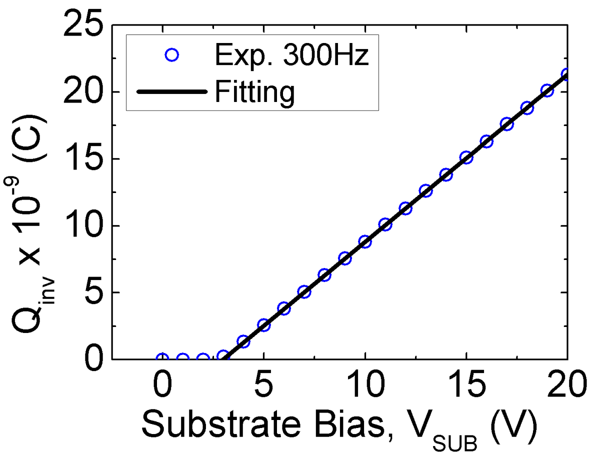

Figure 3.14. (a) Frequency dependence of Q_{inv} with the substrate bias. The difference of Q between 300 Hz and 1 kHz is within 2.1%. (b) Experimental data of Q_{inv} and the linear fitting extrapolated from the region between $V_{SUB} = 15$ V and $V_{SUB} = 20$ V. Non-passivated wafer, $t_{Si} = 88$ nm, $t_{BOX} = 145$ nm, oscillation level 20 mV.

In order to complete this study, we analyzed the carrier distribution during the measurements. The carrier density can be calculated as:

$$q \times N_S(V_{SUB}) = Q_{inv}/S_{eff} \tag{3.7}$$

where S_{eff} was obtained by Eq. [3.6]. Several simulations were performed to evaluate the carrier spreading using the 2-D device simulator ATLAS. The structure of an isolated cell of the wafer, as well as the needles, were simulated considering actual dimensions. The cell was surrounded by oxide and interface states were taken into account at the edges for more realistic simulations ($N_{IT} = 10^{11} cm^{-2}$). The needles were emulated by highly doped silicon pillars penetrating into the silicon film. This approximation is reasonable for static simulations and guarantees both an ohmic contact and a source of carriers. Figure 3.15 illustrates the distribution of electron concentration per surface unit, N_S, along the Si film at Si/BOX interface considering a one-needle configuration when the substrate bias is modified from 3 V to 10 V.

The results reveal that the concentration is maximum close to the needle, but drops at the edges as consequence of the border effects. The carrier concentration in the region covered by the effective radius of the needle centered on the 5 mm × 5 mm cell ($2.5mm - r_{eff} = 1.1mm < x < 2.5mm + r_{eff} = 3.9mm$) is larger than 95% of the carrier concentration just under the needle and can be considered almost constant. These experiments indicate the utility of Split-C(V) measurement to determine the carrier density for all V_{SUB} regions where the channel is active in a Pseudo-MOS configuration.

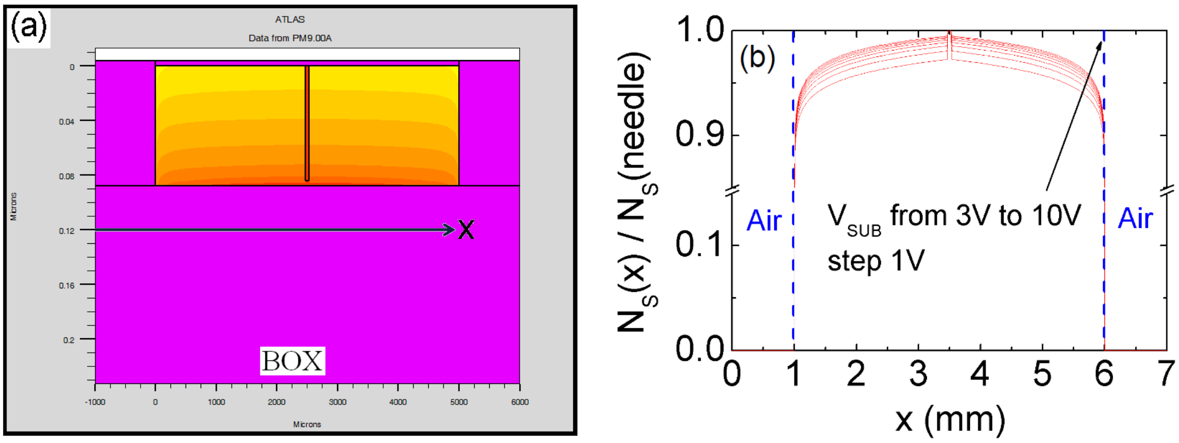

Figure 3.15. (a) Electron concentration simulated by ATLAS taking into account real dimensions of the cell and interface states at borders. t_{Si} = 88 nm, t_{BOX} = 145 nm, V_{SUB} = 10 V. (b) Ratio between the concentration along the film and the concentration in the needle (at 84 nm depth from the Si surface) for substrate biases from 3 V to 10 V. The doping concentrations for the silicon film and the needle region are per surface unit.

3.4.4 Model development

Assuming that the Silicon island is large enough to ignore border effects, the effective surface generated by one needle, S_{eff-1N}, can be modeled by a circular shape. It means that carriers are uniformly distributed around the needle covering a circular area (Figure 3.16.(a)) whose equation is given by:

$$S_{eff-1N} = \pi r_{eff}^2 \tag{3.8}$$

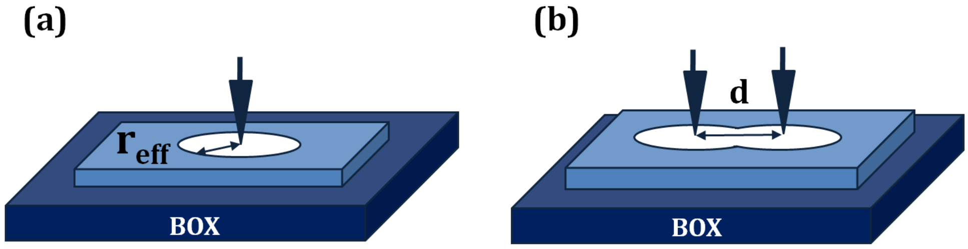

Figure 3.16. Schematic representation of the area covered by the carriers in (a) single-needle and (b) two-needle configurations.

The *effective radius*, r_{eff}, is the key value to account for the dependence of the area on the frequency. The effective area for a single-needle can be obtained from the maximum value of the C-V curves measured with the impedance analyzer by using Eq. [3.6]. So, with the capacitance curves of Figure 3.12 associated to a 88nm-thick Si film and 145nm-thick BOX non-passivated wafer, r_{eff} resulted approximately 1.4 mm at low frequencies (Figure 3.17).

This value is smaller than the dimensions of the cell (d_{cell} = 5 mm) and comparable to the nearest distance between two needles (d = *1.59* mm).

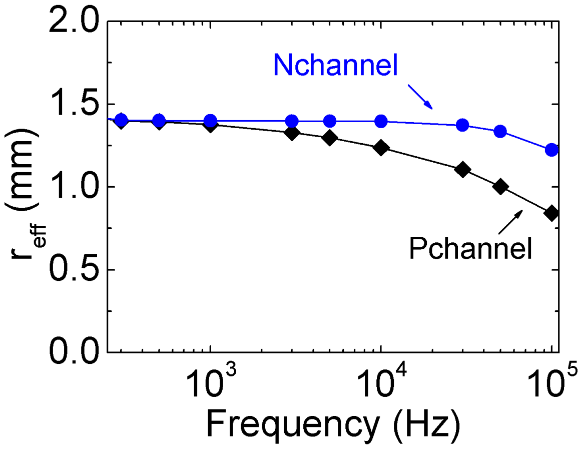

Figure 3.17. Effective radius extracted from capacitance curves used for Figure 3.12.(a). Non-passivated wafer, t_{Si} = 88 nm, t_{BOX} = 145 nm, oscillation level 20 mV.

If two needles are used on the wafer, the resulting surface corresponds to the geometrical superposition of the circles generated by each of them (Figure 3.16.(b)):

$$S_{eff-2N} = 2\pi r_{eff}^2 \tag{3.9}$$

Nevertheless, there are two aspects illustrated in Figure 3.18 to take into account in this first approach:

1. First, when two needles are employed, it is possible that an overlap of the circles occurs for specific frequencies. For these cases, the overlapped region (named A in Figure 3.18.(a))

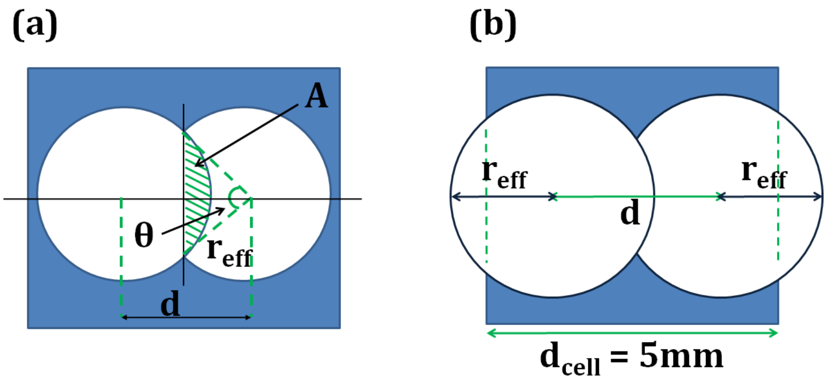

Figure 3.18. Schematics illustrating the definition of the effective surface, S_{eff} for two needles placed on the surface. (a) When an overlap occurs, the region A must be subtracted twice. (b) The physical boundaries of the etched silicon island limit the effective surface for large needle separation.

must be subtracted twice from the expression given by Eq. [3.9]. As this term is not always necessary, a fitting parameter, k_1, was defined to be 1 when the overlap occurs ($d < 2r_{eff}$) and 0 for non-overlap.

2. Secondly, when the separation between the needles increases, it is necessary to take into account the border effects, especially when the effective surface reaches the physical limits of the silicon island (Figure 3.18). So, a fitting parameter (α) was calculated fitting the geometrical relationships from Figure 3.18.(b) with experimental results. Another constant k_2 will determine when the border effects occur, and its value depends on the physical dimensions of the cell: k_2 will be 0 when $d_{cell} - d < 2r_{eff}$, and 1 otherwise.

These two aspects determine the final expression for the theoretical effective area in a two-needle configuration:

$$S_{eff-2N} = \alpha(2S_{eff-1N} - 2k_1 A) \tag{3.10}$$

where:

$$\alpha = \left(\frac{1}{\sqrt{2}}\right)\left[1 - k_2 \frac{(\gamma - \sin\gamma)}{2\pi - k_1(\theta - \sin\theta)}\right] \tag{3.11}$$

$$\gamma = 2\arccos\left(\frac{d_{cell} - d}{2r_{eff}}\right) \tag{3.12}$$

$$\theta = 2\arccos\left(\frac{d}{2r_{eff}}\right) \tag{3.13}$$

Having exposed the model for S_{eff} it is possible to explain further the results shown in Figure 3.9. The maximum of the capacitance by two-needle measurements (cases (ii)-(iii)) is not twice as large as that by one-needle configuration (case (i)) due to the overlapping between effective areas induced by each needle and the impact of the border effects.

Finally, Eq. (3.10) can easily be extended to an arbitrary number of probes aligned on the sample surface (uniformly separated). This expansion of the model requires accounting for the number of needles (N) used in the measurements and the number of overlapped regions (A). Then, the general equation is:

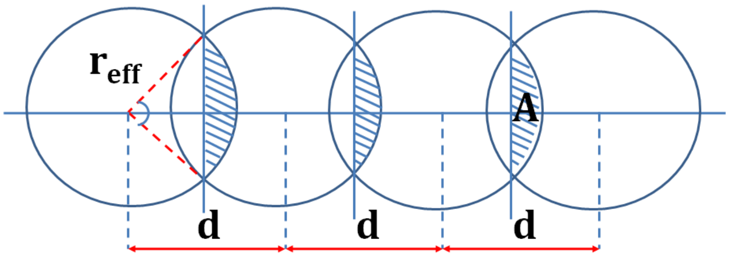

Figure 3.19. Schematic illustrating how the model can be extended to a multiple-needle configuration. To do this, it was necessary to take the number of the probes used in the measurements into account and also the number of the overlapped regions.

$$S_{eff-N} = \alpha(NS_{eff-1N} - 2(N-1)k_1 A) \tag{3.14}$$

3.4.5 Simulation results

In order to clarify the different possible situations, Figure 3.20.(a) shows the theoretical results for S_{eff} as a function of the distance between the needles calculated using the model given by Eq. (3.10). The considered frequency was 5 kHz and the size of the island was $5mm \times 5mm$. As observed, the effective area increases initially with the distance as a consequence of a reduction of the overlap region. Then, a maximum value is achieved at 2.5 mm approximately. For longer distances ($d > 2.5$ mm), the area decreases due to the limits imposed by the size edges of the Silicon island (border effects).

These theoretical results verify also the data discussed in Figure 3.9: as the distance gets larger, so does the area covered by the carriers; an increasing separation clearly implies a reduction of the overlap region, thereby higher values of effective area and capacitance.

In this context, Figure 3.20.(b) illustrates an example of the frequency dependence of S_{eff} with the distance between the probes, d, in a hole channel. Concerning the curve at 100 Hz, the area starts increasing with the distance at the expense of the reduction of the overlapped regions A. The maximum value of the effective area is achieved at 2.5 mm approximately and it reflects the distance at which border effects start to affect the S_{eff} since at longer distances, the area starts to decrease. Regarding the remaining curves, when the frequency rises, a *plateau region* is observed instead of a peak: the surface covered by each needle results so small that the maximum S_{eff} obtained (before the border effects begin to have influence on it) is the sum of the areas induced by each needle.

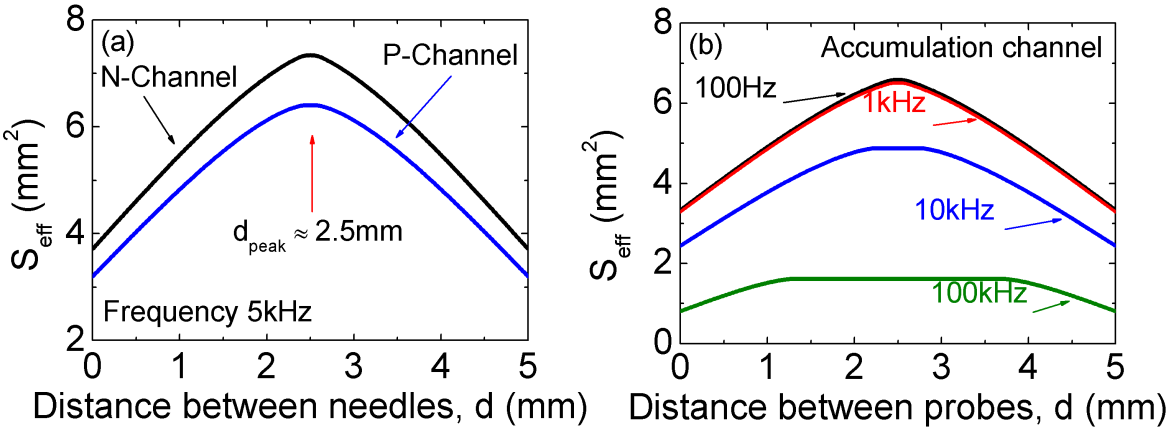

Figure 3.20. (a) Effective surface obtained using the model proposed in Eqs. [3.10]-[3.13]. S_{eff} increases and decreases depending on the influence of the overlap and border regions ($d_{cell} = 5$ mm). (b) Effective surface simulated with the model proposed considering several frequencies. If the frequency is high enough, the maximum value of S_{eff} will be the sum of the areas generated by each probe (a constant value in a certain range of distances).

3.4.6 Experimental results

3.4.6.1 Two-needle configuration

Figure 3.21.(a) shows the comparison between the S_{eff} results obtained experimentally and those calculated using the model for hole and electron channels when the distance between needles was d = 1.59 mm. The methodology followed was:

- To determine S_{eff} by the model, first, capacitance measurements were performed using only one needle on the surface to calculate the experimental effective radius r_{eff} from the maximum capacitance values. Then, S_{eff} was calculated theoretically by Eqs. [3.10]-[3.13].
- On the other hand, to obtain S_{eff} experimentally, new capacitance measurements were carried out using two needles on the surface and Eq. [3.6] was used with the maximum value of them.

The results confirm the validity of the model since the agreement between data is good enough in all cases. The same comparison was done for another distance between the needles (d = 3.18 mm, Figure 3.21.(b)) verifying again the model.

The theoretical model principles are based on the limited response of electrons and holes to the AC signal. The fitting between results clarifies that the capacitance decrease observed in Figure 3.12 is primarily due to surface carrier spreading and not to the substrate related capacitance (accumulation/depletion below the BOX). However, substrate depletion should be considered when dealing with thinner BOX layers [RCG09] [DFO$^+$12] as explained in Section 3.2.4.

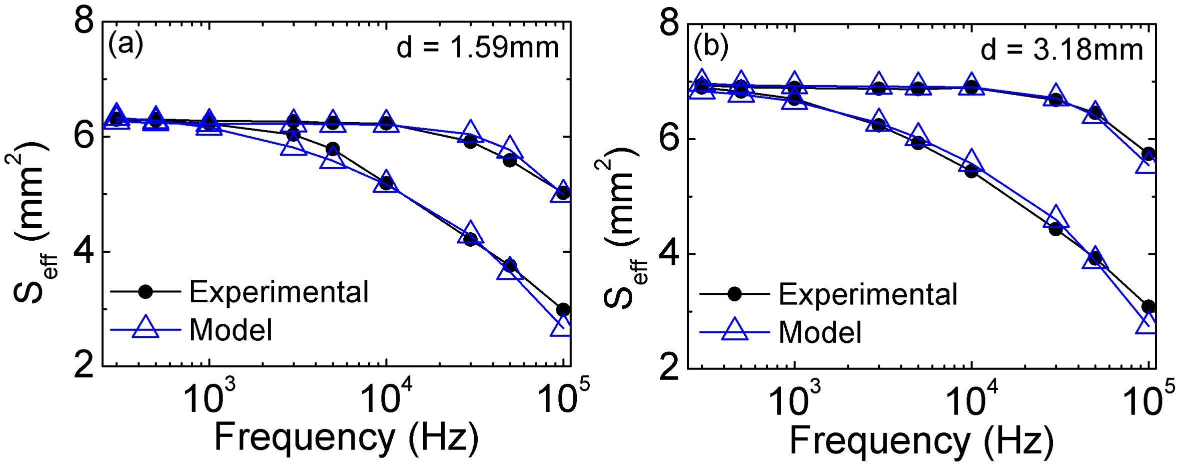

Figure 3.21. Comparison between the effective surface obtained in two-needle configuration extracted with Eq. [3.6] from experiments (filled dots) and the model proposed in Eq. [3.10] (open symbols). Distance between probes: (a) d = 1.59 mm, (b) d = 3.18 mm. Non-passivated wafer, $t_{Si} = 88$ nm, $t_{BOX} = 145$ nm.

3.4.6.2 Three-needle configuration

The same comparison was done using three needles on the surface (Figure 3.22.(a)) and now using Eq. [3.14]. Figure 3.22.(b) shows the results obtained when an electron channel is formed.

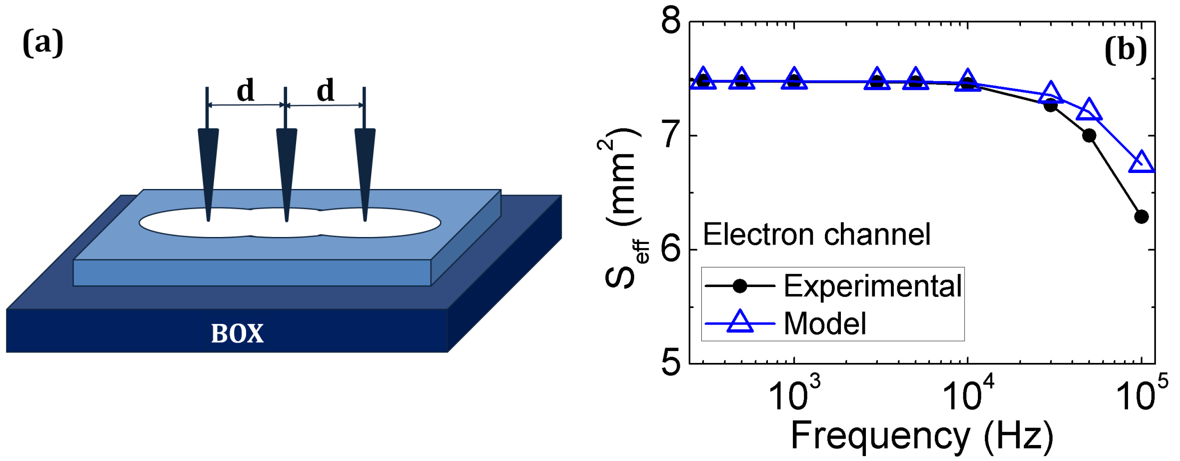

Figure 3.22. (a) Effective surface in three-needle configuration. (b) Extracted effective surface by using Eq. [3.6] with three needles placed on the wafer surface and the model proposed in Eq. [3.14]. Non-passivated wafer, $t_{Si} = 88$ nm, $t_{BOX} = 145$ nm.

The model is validated again. The values predicted fit perfectly with the experiment at low frequencies. Only at frequencies higher than 20kHz an slight deviation is observed (less than 7%). This deviation may be produced by the difficulty of the linear model to catch the physics of the potential distribution in the Si film when more than two needles are used [FDR+12].

3.4.7 Extraction of μ_{eff}

At present, the main use given to the Split-C(V) technique is the extraction and later study of the *effective mobility*, μ_{eff}, in MOSFETs. In particular for a Pseudo-MOSFET sample, the μ_{eff} characterizes the transport at the Si film/BOX interface and its expression results of the combination of the current characteristics with capacitance curves as follows [DFO+12]:

$$\mu_{eff} = \frac{I_D}{f_{g2p} V_D Q_{acc-inv}(V_G)} \tag{3.15}$$

where the geometrical factor f_{g2p} takes the value of 0.75 according to [KBS+05, CW92, KBS+05], and V_D was the drain bias equal to 20 mV in our measurements[7]. The experimental and theoretical values of the area S_{eff} (inserted in $Q_{acc-inv}$) were obtained as explained in Section 3.4.6.1 and Figure 3.23 illustrates an example where both mobility results coincide.

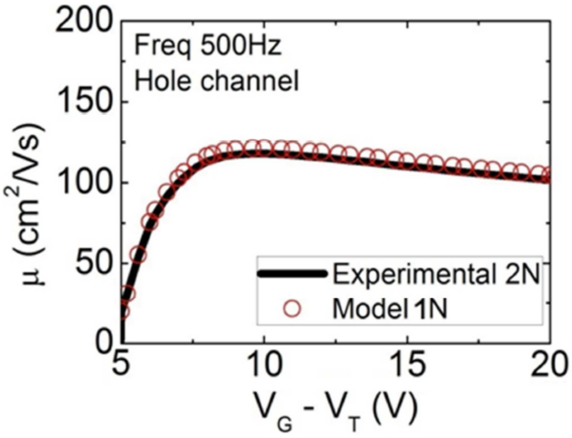

Figure 3.23. Comparison between mobility results obtained using in Eq. [3.15] the S_{eff} value measured by two-needle configuration (black line), and the theoretical S_{eff} value calculated using Eq. [3.10] where the effective radius was measured in one-needle configuration (open symbols). Non-passivated wafer, $t_{Si} = 88$ nm, $t_{BOX} = 145$ nm.

To conclude, the importance of the proper determination of the area for the extraction of the mobility is highlighted in the comparison presented in Figure 3.24. Mobility curves were produced by applying the Split-C(V) technique (S_{eff} is calculated from the model, Eq. [3.10]) and by assuming the usual Pseudo-MOSFET area ($S_{eff} = W \times d = 0.75d^2$ [KBS+05]) which takes into account the distance between the needles and the geometrical factor ($f_{g2p} = W/d = 0.75$). The results show that the difference between the effective areas may lead to either an underestimation of 70% or an overestimation of 9% in mobility curves depending on the separation between the needles.

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[7] Detailed investigation of the geometrical factor f_{g2p} will be presented in Section A.4

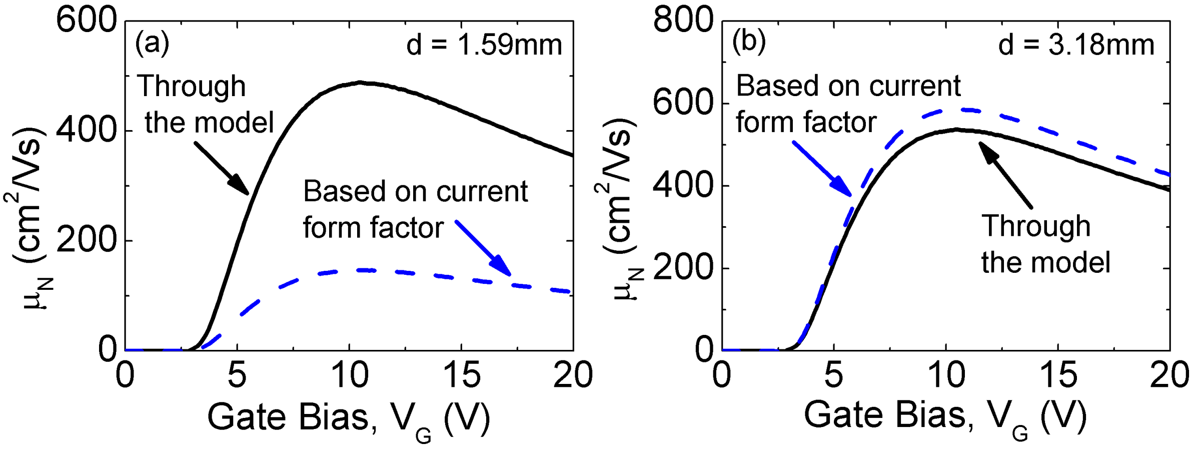

Figure 3.24. Comparison between mobility results obtained by Split-C(V) technique (S_{eff} calculated using Eq. [3.10], solid line), and by considering the Pseudo-MOSFET area ($S_{eff} = 0.75 \times d^2$, dashed line). (a) d = 1.59mm; (b) d = 3.18mm. Non-passivated wafer, $t_{Si} = 88$ nm, $t_{BOX} = 145$ nm, freq = 300 Hz.

3.5 Conclusions

In this chapter, the possibility of using the point-contact technique for capacitance characterization in bare SOI wafers has been shown through an adaptation of Split-C(V) method. The role of the different parameters such us number of the needles and distance between needles has been discussed. The area associated with measurements has been also investigated and clarified. A mathematical model to evaluate the effective area in single-needle and multiple-needle configuration has been proposed including the dimensional and measurements conditions of the experimental setup. The model has been validated by comparison with experimental results. It clarifies that the carrier spreading is the actual origin of the capacitance reduction in thick BOX SOI wafers. Finally, the effective mobility curves were analyzed probing that the effective area is different for Split-C(V) measurements than for regular $I_D(V_G)$ characteristics.

Chapter 4

Effective Mobility Extraction in Bare SOI Substrates

The strong impact of the quality of the wafer surface on characteristics extracted by the Pseudo-MOSFET technique had been already introduced and reported in previous works [DFO$^+$12, DFP$^+$13]. However, there are not studies relating the previous results to the effective electric field induced into the structure. The objective of this Chapter is to show a comparison between universal mobility curves (UMC) and mobility curves obtained from point-contact experiments in a SOI sample.

4.1 Introduction

As said in previous Chapters, point-contact techniques have been widely used over the years to characterize bare substrates since they offer the possibility to extract electrical parameters directly from the wafer [RCG09]. This fact awards these techniques an appealing advantage for manufacturers and research laboratories who look for fast and non-invasive characterization procedures.

In the case of SOI wafers, two variants of point-contact methods have been protagonist of most of the experimental results reported: the four point-contact (in-line) configuration (Figure 4.1.(a)), and the two point-contact configuration or Pseudo-MOSFET technique (Figure 4.1.(b)).

The attractiveness of the Pseudo-MOSFET approach lies on its simplicity because only two needles are used on the wafer, and no precautions need to be taken regarding the probe alignment or interdistance. However, this advantage turns also in its main drawback; since the contacts are used to drive the current and, simultaneously, to measure the voltage, the contact resistance should be accounted for or suppressed depending on the probe pressure on the surface [CML00]. Another additional disadvantage is the fact that there is no full modeling of the current form factor [KBS$^+$05], being mandatory an initial calibration of the method in most cases.

Chapter 3 described a recent application of point-contact techniques on bare SOI wafers: the determination of carrier mobility as a function of the substrate voltage or the inversion/accumulation charge density [DFO$^+$13]. To do so, Split-C(V) measurements (Figure 4.1.(c)) were combined with the MOS-like $I_D(V_G)$ characteristics (Section 3.4.7). For these experiments,

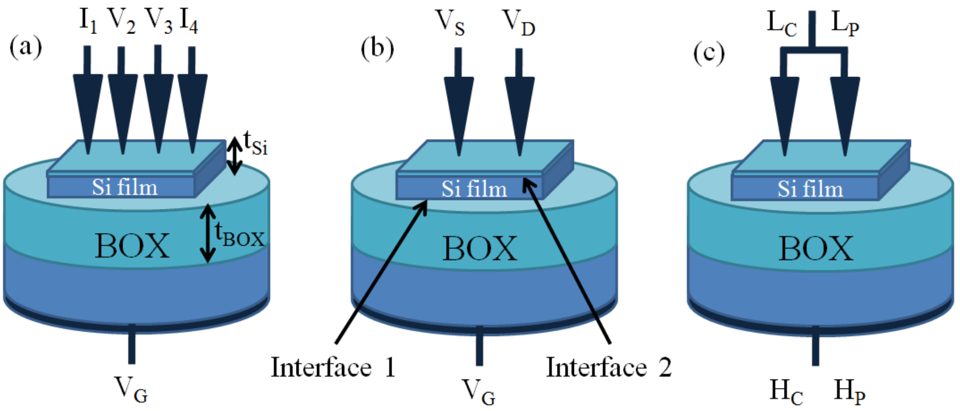

Figure 4.1. Point-contact characterization methods on bare SOI wafers: (a) four point-contact configuration, (b) two point-contact configuration (Pseudo-MOSFET technique), and (c) configuration for Split-C(V) measurements when two needles are employed. *C* and *P* represents the current and voltage connections respectively.

the quality of the native oxide of the top surface remarkably impacts on the electrical properties. Parameters such as the threshold voltage, the transconductance or the carrier mobility have been studied previously showing severe degradation when the top surface is left non-passivated [HAHC07] [ABB+05]. The source of the apparent mobility degradation observed at the Si film/BOX interface, motivated by the non-passivated surface, has been identified by Hamaide et al. [Koo73]. However, there is no systematic work showing comparison between Universal Mobility Curves (UMC) and mobility curves obtained from point-contact experiments. The correlation between both families of curves can contribute with valuable results regarding the quality of the as-fabricated SOI substrates, as well as, validating the extraction techniques. For the comparison, the accurate determination of effective electric field, E_{eff}, is mandatory. The difficulty in determining E_{eff} for point-contact measurements, comes from the accurate evaluation of the potential at the top free surface, and the impact of the surface quality on it.

In the following Sections all these aspects related to mobility degradation and effective electric field will be further studied and analyzed.

4.2 The role of the top-interface on the effective electric field

The mobility vs. effective electric field plot, $\mu(E_{eff})$, is a powerful representation for analyzing and benchmarking the transport properties of MOS-transitors or semiconductor substrates. However, the determination of E_{eff} should be addressed with great care out of standard bulk-transistors [CRG10]. In the case of a bare SOI structure, the amount of charge trapped at the top Silicon/native-oxide interface modifies the electric field and the electrostatic potential profile of the whole film. Hereinafter, it will be refered to interface 1 to identify the Si film/BOX interface in our mathematical notation, and interface 2 for the Si film/Surface-oxide interface, located between 10 and 100nm away from the channel. The density of interface traps at the free surface is typically in the range of $D_{it2} > 10^{13} cm^{-2} eV^{-1}$ for non-passivated samples, and $D_{it2} < 2 \cdot 10^{11} cm^{-2} eV^{-1}$ for passivated ones [HAHC07].

In the incoming paragraphs six bare SOI wafers, containing 5 mm × 5 mm MESA isolated cells, will be considered for the experiments: two samples with 12nm-thick Si-film; two samples with 50nm-thick Si-film, and two samples with 88nm-thick Si-film. All of them featuring a 145nm-thick BOX. Each set containing one sample with non-passivated surface, and one sample with a passivated one.

4.2.1 Discussion of the electrostatic potential

The first task was focused on examining the electrostatic potential at the two interfaces of the Si film (ψ_1, BOX/Si-film interface; ψ_2, Si-film/native-oxide interface). The potential profiles were obtained numerically by solving Poisson's equation in the whole SOI structure.

Since the results were compared with experimental data, the simulation parameters such as the density of interface states, thickness of the layers and dopings, were adjusted for the calibration of the simulator (see Table 4.1). Figures 4.2.(a) and 4.2.(b) show examples of the accuracy of the comparison between the experimental accumulation/inversion charge per area unit (calculated from the integration of the substrate-to-channel capacitance curves, Figure 4.1.(c)), and the calibrated simulations. The frequency of excitation for the measurements was established at 100 Hz in order to avoid a capacitance reduction due to the limited response of the carriers in the Si film [NSS11].

Table 4.1. Calibrated parameters for the numerical simulations (N_A: Si-film doping, P_{ch}: hole channel, N_{ch}: electron channel)

	Non-passivated	**Passivated**
$t_{Si}(nm)$	88	
$t_{BOX}(nm)$	145	
$N_A(cm^{-3})$	5×10^{14}	5×10^{14}
$D_{it1}(cm^{-2}eV^{-1})$	2×10^{10}	5×10^{10}
$D_{it2}(cm^{-2}eV^{-1})$	3×10^{13}	5×10^{10}
	Non-passivated	**Passivated**
$t_{Si}(nm)$	50	
$t_{BOX}(nm)$	145	
$N_A(cm^{-3})$	5×10^{14}	5×10^{14}
$D_{it1}(cm^{-2}eV^{-1})$	5×10^{10}	5×10^{10}
$D_{it2}(cm^{-2}eV^{-1})$	3×10^{13}	5×10^{10}
	Non-passivated	**Passivated**
$t_{Si}(nm)$	12	
$t_{BOX}(nm)$	145	
$N_A(cm^{-3})$	5×10^{14}	5×10^{14}
$D_{it1}(cm^{-2}eV^{-1})$	8×10^{10}	8×10^{10}
$D_{it2}(cm^{-2}eV^{-1})$	5×10^{12} (P_{ch}) 2.5×10^{12} (N_{ch})	8×10^{11} (P_{ch}) 2×10^{11} (N_{ch})

Figures 4.3.(a)-(d) show the electrostatic potentials, extracted from the numerical simulations, at the BOX/Si-film interface, ψ_1, and at the Si-film/top-oxide, ψ_2, as a function of the substrate voltage. The potential ψ_1 reaches the threshold condition when increasing $|V_G|$

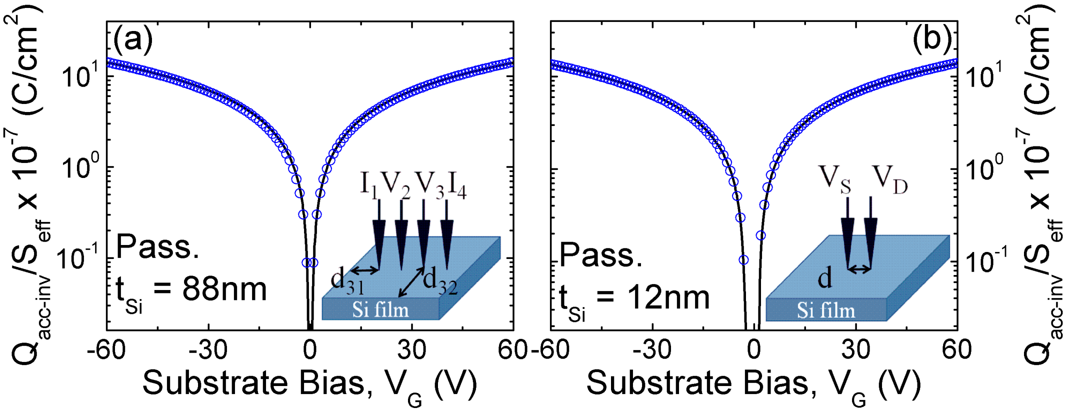

Figure 4.2. Comparison of the accumulation/inversion charge per area unit obtained from experimental results by the Split-C(V) technique (solid lines) and from simulations after calibration (open symbols), as a function of the substrate bias for the passivated wafers considered. (a) Four-needle configuration, $t_{Si} = 88$ nm. The distances $d_{31} \approx 0.12$ mm and $d_{32} \approx 2.5$ mm represent the separation between the contacts and the Si-island edges. (b) Pseudo-MOSFET configuration, $t_{Si} = 12$ nm. Distance between contacts $d = 1.59$ mm. $t_{BOX} = 145$ nm.

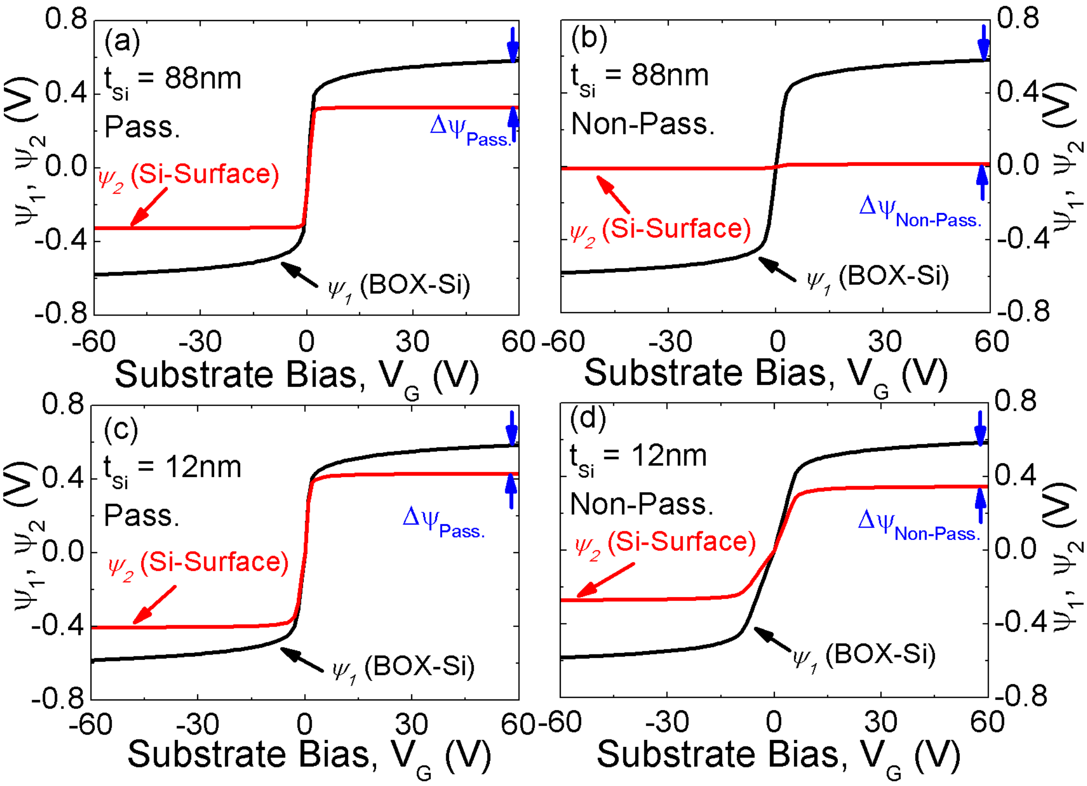

Figure 4.3. Electrostatic potential obtained from numerical simulations at BOX/Si-film (ψ_1) and Si-film/native oxide (ψ_2) interfaces as a function of the substrate bias. Passivated wafers (a) & (c), non-passivated wafers (b) & (d). $t_{Si} = 88$ nm (a) & (b), $t_{Si} = 12$ nm (c) & (d). $t_{BOX} = 145$ nm.

($\psi_1 \approx 2\phi_F \approx 0.6$ V), unlike ψ_2, which is intrinsically determined by the trap density of the native oxide. The difference between both potentials at $V_G = 60$ V, $\Delta\psi = |\psi_1$ - $\psi_2|$, reveals the importance of the quality of the surface (passivated or not). In particular, for the 88nm-thick Si-film, $\Delta\psi_{Pass.}(88nm) \approx 0.254$ V, when the surface is passivated (Figure 4.3.(a)), whereas $\Delta\psi_{Non-Pass.}(88nm) \approx 0.571$ V for the non-passivated case (Figure 4.3.(b)), due to the pinning of the surface potential at the top interface.

The large difference in the electrostatic potential between the interfaces, generated in the non-passivated samples, yields also a larger electric field inside the Si-film. A similar situation is observed for the thinner Si film, ($t_{Si} = 12$ nm, $\Delta\psi_{Pass.}(12nm) \approx 0.163$ V and $\Delta\psi_{Non-Pass.}(12nm) \approx 0.247$ V). In this case, the difference is lower, but, since the thickness of the SOI layer is also thinner (a factor of seven), the resulting electric field is even larger than in the thicker film.

These results were directly linked with the mobility vs. effective field plot (Section 4.3) where the top interface electric field will play a fundamental role.

4.2.2 Effective electric field model

The electric field at a given position, z, inside the Silicon film, can be calculated according to the Gauss surface shown in Figure 4.4. The charge inside this surface is related to the difference in the electrical displacement:

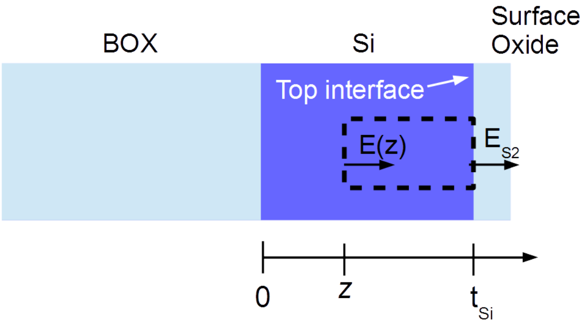

Figure 4.4. Vertical cross-section of the Silicon-On-Insulator structure (BOX/Si/Surface-Oxide). A Gauss surface (dashed lines) enclosing the Si/surface-oxide interface and the Silicon film is considered to determine the local electric field at a position z.

$$\begin{aligned} \nabla \cdot \mathbf{D} = \epsilon_{Si}E(z) - \epsilon_{Si}E_{S2} = \\ = qN_A\left(t_{Si} - z\right) + q\int_z^{t_{Si}} c(y)dy \end{aligned} \tag{4.1}$$

where N_A is the doping concentration and $c(y)$ is the mobile charge concentration. The top interface electric field, E_{S2}, is related to the density of states at the top surface as follows [RCG09]:

$$\epsilon_{Si}E_{S2} = qD_{it2}\psi_2 = C_{it2}\psi_2 \tag{4.2}$$

where a linear potential profile inside the film can be assumed [RCG09]:

$$E_{S1} = E_{S2} = \frac{\psi_{S1} - \psi_{S2}}{t_{Si}} \tag{4.3}$$

Eq. (4.2) and Eq. (4.3) results in:

$$E_{S1} = E_{S2} = \frac{\psi_{S1}}{t_{Si}} \left[1 - \frac{C_{Si}}{C_{Si} + C_{it2}} \right] \tag{4.4}$$

Combining (4.1) and (4.4) at threshold condition ($\psi_{S1} = 2\phi_F$) the resulting local electric field is given by:

$$\begin{aligned} E(z) = \frac{1}{\epsilon_{Si}} \left(qN_A \left(t_{Si} - z \right) + \int_z^{t_{Si}} c(y)dy \right) + \\ + \frac{2\phi_F}{t_{Si}} \left(1 - \frac{C_{Si}}{C_{Si} + C_{it2}} \right) \end{aligned} \tag{4.5}$$

The effective electric field, E_{eff}, is calculated as the average electric field (absolute value in the Si film) with respect to the carrier concentration, *c(z)* [SH99]:

$$E_{eff} \left(V_G \right) = \frac{\int_0^{t_{Si}} \left| E \left(z, V_G \right) \right| c(z)dz}{\int_0^{t_{Si}} c(z)dz} \tag{4.6}$$

where $E(z, V_G)$ is the vertical electric field. The variables required in Eq. (4.6) are not accessible from an experimental prospective, but including Eq. (4.5) in Eq. (4.6) yields a tractable semi-empirical solution:

$$\begin{aligned} E_{eff} = \frac{1}{\epsilon_{Si}} (\eta Q_{acc-inv} + Q_d) + E_{S2} = \\ = \frac{1}{\epsilon_{Si}} (\eta Q_{acc-inv} + Q_d) + \frac{2\phi_F}{t_{Si}} \left(1 - \frac{C_{Si}}{C_{Si} + C_{it2}} \right) \end{aligned} \tag{4.7}$$

where Q_d is the total depletion charge, usually negligible in advance non-intentionally doped SOI substrates. η is a coefficient that represents the weighting of the mobile charge depending on the type of carrier (electrons or holes) induced at the Si film/BOX interface as well as the substrate crystallographic orientation. It has been verified in our experiments that $\eta \approx 0.33$ when holes conform the channel ($V_G < 0V$) and $\eta = 0.5$ when electrons do ($V_G > 0V$). These values agree with previous works on a (100) crystallographic orientation [IKKT04].

Eq. (4.7) includes the correction needed to account for the opposite-interface electric field E_{S2} (Si-surface field in our case, second term in the formula) [SSCA94]. Figure 4.5.(a) shows a comparison of E_{S2} calculated by the model and from numerical simulations for a 12nm-thick Si-film wafer when an electron channel is induced. A good agreement is achieved above the threshold voltage ($\psi_1 \approx 2\phi_F$, $V_{TH} \approx 2.94$ V for the passivated wafer and $V_{TH} \approx 11.48$ V for the non-passivated one).

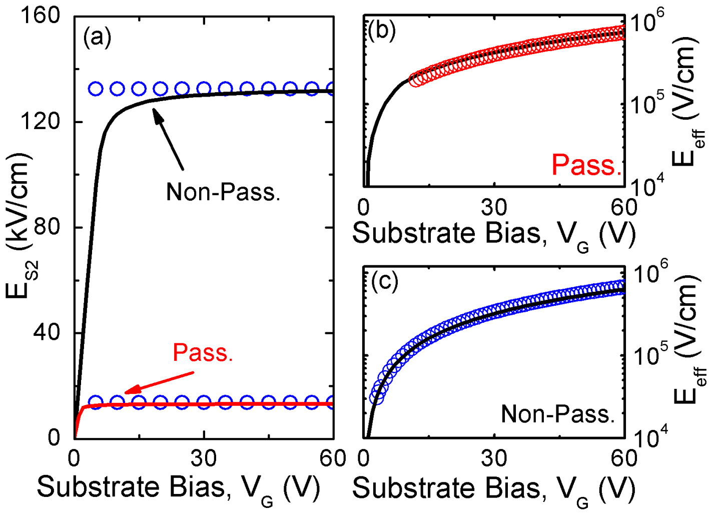

Figure 4.5. (a) Comparisons between E_{S2} as a function of the substrate voltage for passivated and non-passivated SOI wafers from simulation data (solid line), and using the semi-empirical model of Eq. [4.7] (open symbols). (b) & (c) Comparisons between the effective electric field obtained by Eq. (4.6) using the simulation results (solid line), and by Eq. (4.7), employing the experimental data above the threshold condition (open symbols). t_{Si} = 12 nm. t_{BOX} = 145 nm.

The difference of E_{S2}, between passivated and non-passivated surfaces exceeds 130 kV/cm. The main consequence of this difference will be its impact on the values of the effective field given by Eq. (4.7).

Finally, Figures 4.5.(b) and 4.5.(c) show the complete evaluation of the effective electric field given by Eq. (4.7), and the definition given by Eq. (4.6) (evaluated from numerical simulations) in passivated and non-passivated cases respectively. The results verify the accuracy of the proposed model as long as the surface potential ψ_1 reaches the threshold condition ($\psi_1 \approx 2\phi_F$).

4.3 Results on mobility

Once the tools for an accurate evaluation of the effective electric field are established, the results on the effective mobility will be presented. The methodology consists of acquiring current and Split-C(V) capacitance characteristics from all the samples. Then, the carrier mobility is extracted from the combination of both. Initially, four point-contact measurements were conducted. In this case, the effective mobility is extracted from [Sch06]:

$$\mu_{eff} = \frac{I_{14} S_{eff}}{f_{g4p} V_{23} Q_{acc-inv}} \tag{4.8}$$

where the term $Q_{acc-inv}$ was obtained by the integration of the mobile charge as a function of the substrate bias, using the four probe variant of Figure 4.1.(c) [Meg86]. S_{eff} corresponds with the effective area (Section 3.4.1) covered by the carriers [FDR$^+$12].

The correction factor f_{g4p} is determined according to the features of the sample considered and the parameters of the experimental configuration, such us the separation between the needles and the edges. This form factor is, in turn, the product of several independent correction factors [Sch06]:

$$f_{g4p} = \frac{2\pi d}{t_{Si}} F_1 F_2 F_{31} F_{32} \tag{4.9}$$

where d corresponds with the separation between the point-contacts ($d = 1.59$ mm, Figure 4.2.b).

F_1 represents the thickness correction factor and it takes into account the finite Silicon film thickness. It was extracted from data interpolations described by [Wel01] resulting in $F_1 = 6.58 \cdot 10^{-6}$ for the wafers with $t_{Si} = 12$ nm, $F_1 = 3.41 \cdot 10^{-5}$ for the wafers with $t_{Si} = 50$ nm, and $F_1 = 6.58 \cdot 10^{-5}$ for $t_{Si} = 88$ nm.

On the other hand, F_2 corrects for the lateral cell dimensions and it is calculated by the following equation [Smi57]:

$$F_2 = \frac{ln(2)}{ln(2) + ln\frac{[(D/s)^2+3]}{[(D/s)^2-3]}} \tag{4.10}$$

We tested square cells with sides of $D = 5$ mm and keeping a distance between needles of $s = 1.59$ mm, leading a value of $F_2 = 0.6$.

Finally, F_{31} and F_{32} were both related to the separation of the contacts with respect to the sample edges ($d_{31} = 0.115$ mm, and $d_{32} = 2.5$ mm in Figure 4.6). Their values [Val54] were $F_{31} = 0.72$ and $F_{32} = 0.93$.

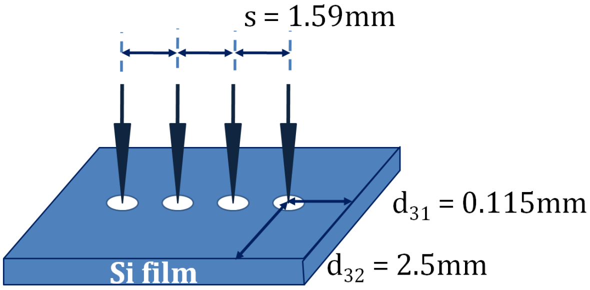

Figure 4.6. Distances from the needles to the edges of the cell when a 4-point configuration is performed.

The resulting geometrical factor from Eq. (4.9) was $f_{g4p} = 2.2$ for 12nm-thick Si-film samples, $f_{g4p} = 2.7$ for 50nm-thick Si-film samples and $f_{g4p} = 3.0$ for 88nm-thick Si-film samples.

Figures 4.7.(a)-(d) show the four point-contact mobility curves (noted as *4p*) obtained as a function of the effective electric field calculated by the model proposed in Eq. (4.7). The curves were extracted for hole (Figures 4.7.(a)-(c)) and electron (Figures 4.7.(b)-(d)) channels including results on both passivated and non-passivated, 88nm-thick and 12nm-thick Si-film samples. Universal Mobility Curves [TTIT94] are also included for comparison.

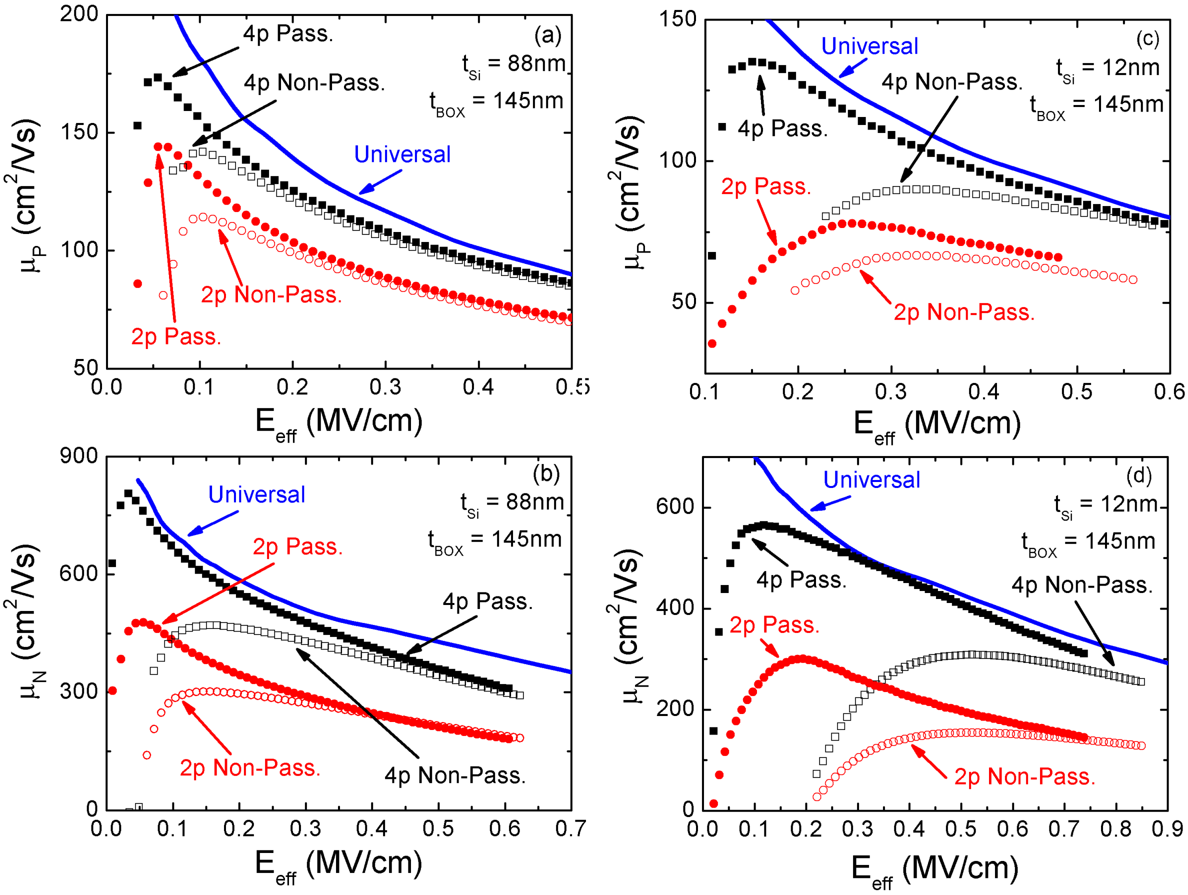

Figure 4.7. Experimental mobility curves for (a)-(c) holes and (b)-(d) electrons versus the effective electric field for passivated (solid symbols) and non-passivated (open symbols) SOI samples employing four (4p, square symbols) and two (2p, circular symbols) point-contact configurations. Substrate bias was modified from -60V to +60V. (a)-(b) t_{Si} = 88 nm, t_{BOX} = 145 nm. (c)-(d) t_{Si} = 12 nm, t_{BOX} = 145 nm. UMC curves are included for comparison [TTIT94].

Both for hole and electron channels, the peak values of the carrier mobility result higher when dealing with passivated surfaces (reaching a difference above $400 cm^2/Vs$ for electrons in the 88nm-thick Si case, Figure 4.7.b). At this low effective electric field regime, Coulomb scattering is the main limiting mechanism, being this effect magnified by the Coulomb scattering induced by the defective top-interface of the non-passivated samples. The thinner the film the lower the peak mobility value. The role of the top-interface is clearly manifested as a shift of the mobility curves towards the region of higher effective electric field (and therefore lower mobility).

In the case of the 88nm-thick Si-film samples (Figure 4.7.(a)-(b)) the passivated and non-passivated curves merge quickly as the effective field (substrate bias) increases. In contrast, the convergence of the curves of the thinner 12nm-thick samples, only occurs at much higher effective field (see Figure 4.7.(c)-(d)) as consequence of, not only the intensity of the top surface electric field, but also a more predominant role of the Coulomb scattering [TTIT94]. Nevertheless, when E_{eff} reaches its maximum values, passivated and non-passivated mobility curves coincide since, at high electric fields, the interface roughness prevails as the limiting scattering mechanism [WM04] at the Si/BOX interface where the carriers are confined. This effect is especially observable in the graphics for hole channels (Figures 4.7.(a) and (c)).

This study was also completed by extracting the effective mobility by using the two point-contact Pseudo-MOSFET technique, maintaining the same distance between needles ($d = 1.59$ mm). For this experiment, the pressure of the needles and the geometrical current form factor, f_{g2p}, must be carefully selected because, otherwise, the mobility values could be erroneously extracted.

Initially, the current form factor, f_{g2p} [KBS+05] was fixed to the value of 0.75 [CW92]. Results obtained from Pseudo-MOSFET (noted as *2p*) in Figures 4.7.(a)-(d) show the inaccuracy of this standard value since it leads to an important underestimation of the carrier mobility in all cases.

The precise determination of f_{g2p} must be carried out through the comparison of current characteristics extracted from two and four point-contact configurations in the ohmic region of operation. The corresponding formulas are given by:

$$I_D = f_{g2p} C_{BOX} \mu (V_G - V_{TH}) V_D \tag{4.11}$$

$$I_{14} = f_{g4p} C_{BOX} \mu (V_G - V_{TH}) V_{23} \tag{4.12}$$

where V_{TH} is the threshold voltage, and it was calculated from the peak of the second derivative of the $I_D(V_G)$ characteristics.

The values of f_{g2p} obtained for the different cases (including also results for $t_{Si} = 50$ nm) are summarized in Table 4.2. As observed, these values are in general far below the conventional geometrical factor, 0.75, used for the Pseudo-MOSFET. If the form factors of Table 4.2 are applied, the *2p* mobility curves in Figures 4.7.(a)-(d) fully run into the four-probe ones. According with these results, the Pseudo-MOSFET technique can be perfectly used for the extraction of the carrier mobility. However, a proper calibration of the experimental setup (needle pressure and current form factor) by comparing with *4p* measurements is mandatory, entailing an obvious inconvenient that the four-point configuration circumvents.

Table 4.2. Geometrical factors obtained by comparing $I - V$ characteristics from two- and four-needle configurations.

$t_{Si} = 88nm$	**Non-passivated**	**Passivated**
$f_{2pPChannel}$	0.61	0.63
$f_{2pNChannel}$	0.49	0.47
$t_{Si} = 50nm$	**Non-passivated**	**Passivated**
$f_{2pPChannel}$	0.59	0.61
$f_{2pNChannel}$	0.45	0.42
$t_{Si} = 12nm$	**Non-passivated**	**Passivated**
$f_{2pPChannel}$	0.56	0.55
$f_{2pNChannel}$	0.38	0.38

To conclude, Figure 4.8 shows a comparison of mobility curves (holes and electrons) extracted from non-passivated wafers using the Pseudo-MOSFET experimental setup with well calibrated form factors (Table 4.2). For the case of hole channels (Figure 4.8.(a)), the mobility at low effective electric field, reflects clearly the role of the Coulomb scattering dominating the mobility curve, with a severe impact of the non-passivated interface for the thinner film ($t_{Si} = 12$ nm). At higher effective electric field, all curves converge to the Universal Mobility Curve regardless the Silicon film thickness. Similar behavior is observed for electron channels. However, for the range of voltage bias applied to the substrate, the effective field is not high enough to reach the values of the Universal Mobility Curve. This is not the case of the passivated surfaces where the UMC is easily reached (i.e. see Figure 4.7.(d)).

The results presented constitute the validation of the Pseudo-MOSFET technique for the extraction of mobility with the proper calibration of the experimental setup. Nevertheless, it is worth noting that the Pseudo-MOSFET approach can be used without accurate determination of the form factor, as a simple method for extracting other electrical parameters where it is not involved (such us the threshold voltages or density of states), or comparing relative changes of mobility (i.e. between different wafer lots) where an absolute value is not needed.

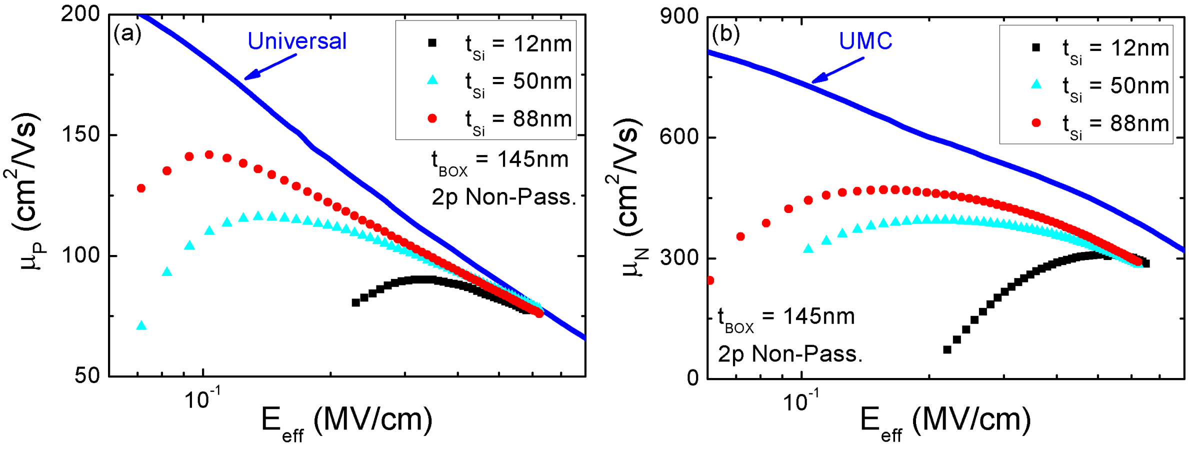

Figure 4.8. Experimental mobility curves for (a) holes and (b) electrons versus the effective electric field (logarithmic scale) for three different non-passivated SOI samples. The extraction is based on a two point-contact (Pseudo-MOSFET) setup with the adequate geometric factors *fg* from Table 4.2. Substrate bias was modified from from 0 to −60 V and from 0 to +60 V for the hole and electron channels characterization respectively. $t_{BOX} = 145$ nm. UMC curves are included for comparison [TTIT94].

4.4 Conclusions

In this Chapter the impact of the effective electric field on the carrier mobility extracted by in-line point-contact measurements on bare SOI wafers has been analyzed. The large difference of the density of interface states between passivated and non-passivated samples, conditions the maximum value of the low field mobility extracted at a low effective electric field regime and limited by Coulomb scattering. This difference is magnified for the thinner SOI wafers. In the non-passivated samples, the top-interface electric field adds a non negligible contribution to the effective field shifting the μ_{eff} curve to lower mobility values. This is pointed as the main source of the mobility reduction observed in non-passivated samples.

Finally, the comparison between four point and two point (Pseudo-MOSFET) measurements, allowed us to obtain precise form factors for the current flow validating the Pseudo-MOSFET configuration for the extraction of the $\mu(E_{eff})$ characteristics.

Chapter 5

Applications of Point-Contact Techniques

Over the years, new applications associated to point-contact techniques have been developed by taking advantage of the simplicity of the configuration setup. Similarly, in order to explore new business opportunities, new substrates have appeared in which the Silicon layer has been replaced by another material, such as graphene. This chapter introduces several studies carried out during the development of this work which demonstrate the adaptation capacity of the point-contact methods to evolve with emerging substrates.

5.1 Poly-silicon samples

Polycrystalline Silicon has been an important component of Silicon technology for nearly two decades, being used first in MOS integrated circuits and then becoming prevalent in bipolar circuits [Kam12]. During this time, a great deal of information has been published about Poly-Si, always focused on the enhancement of the device and integrated-circuit performance. In this Section, a point-contact method is described to characterize Poly-Si substrates.

Poly-Si substrates differ from usual Silicon wafers in the internal crystalline structure (Figure 5.1): in Silicon, atoms form regular patterns repeated in the whole material; in the Poly-Si material, a lot of crystalline structures with different orientations are found [SB06].

The four samples studied in this Section are the result of a collaboration with the Microelectronic National Center in Barcelona (Spain), where they were fabricated. Their dimensions are specified in Table 5.1.

5.1.1 Electrical characterization

The static characterization of Poly-Si samples were carried out through the extraction and subsequent analysis of the I-V curves as a function of the gate voltage. The bias was modified from -40 V to + 40V.

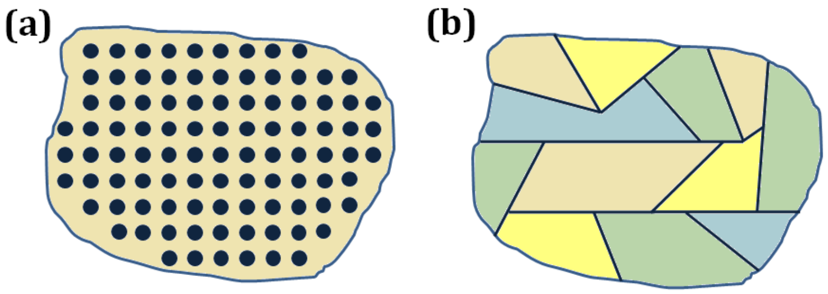

Figure 5.1. Schematic illustration of (a) crystalline and (b) poly-crystalline atomic structures. In (a) the atoms form regular repeating arrangements. (b) is composed by numerous crystalline structures with different orientations.

Sample name	t_{Si}**(nm)**	t_{BOX} **(nm)**	t_{Ox_Sup} **(nm)**
1	15	145.3	20
2	22	145.3	6
3	40	145.3	20
4	47	145.3	6

Table 5.1. Specifications of the Poly-Si wafers from the batch 6383-GRA fabricated by CNM company.

5.1.1.1 Dependence on the probe pressure

The first test carried out with the samples was the search of the optimum probe pressure to get ohmic contacts. Figure 5.2.(a) shows an example of the different curves extracted for sample No. 1 ($t_{Si} = 15$ nm, $t_{BOX} = 145.3$ nm, $t_{OxSup} = 20$ nm) when the pressure was changed from 50 g to 100 g. As observed, a minimum of 70 g was required in order to obtain clear characteristics.

The threshold voltages calculated using the Y-function are also depicted in Figure 5.2.(b) demonstrating that there is no dependence of V_{TH} on the pressure. So, 70 g was considered as the limit pressure for the samples since all of them have the similar BOX thickness dimensions.

It is worth noting that V_{TH} values are higher in comparison with those extracted for the non-passivated Silicon sample with the similar thickness described in Section 2.3.1. It was to be expected since now the film is made by a poly-crystalline material and, in consequence, the traps density results very high. In addition, for this sample, the Silicon film thickness is only 15 nm, what does that the charge within the top surface has a considerable influence on the channel and a higher value for V_{TH} was necessary to create the channel between drain and source needles.

5.1.1.2 Dependence on the drain voltage

Several I-V curves were also performed varying the voltage applied between the point-contact needles. In particular, drain bias was modified from 50 mV to 100 mV while source voltage kept

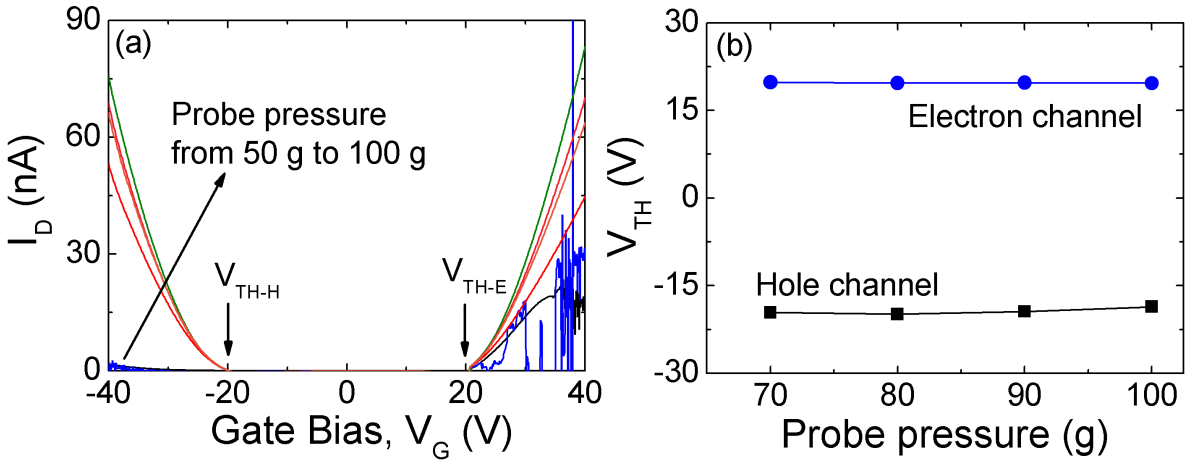

Figure 5.2. (a) Current curves as a function of the gate bias when the needle pressure varies from 50 g to 100 g. (b) Threshold voltage values obtained for the different probe pressures. V_D = 100 mV, V_S = 0 V.

to 0 V (Figure 5.3.(a)). The results, as well as the threshold voltages extracted (Figure 5.3.(b)), showed that the static behavior of these samples was not altered by the value V_D[1].

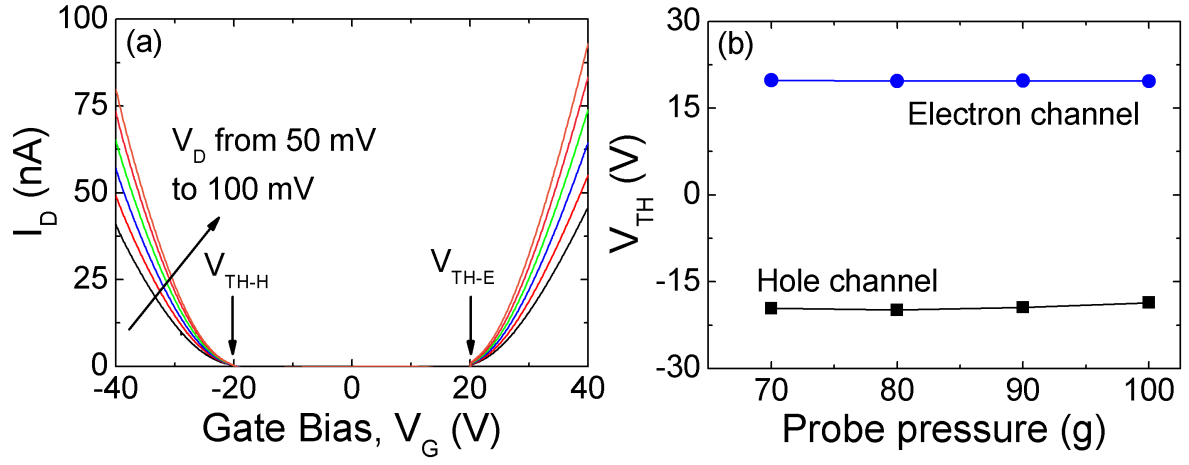

Figure 5.3. (a) Current curves as a function of the gate bias when the needle pressure varies from 50 g to 100 g for different V_D values. (b) Threshold voltage values obtained for the different probe pressures. V_S = 0 V, P = 90 g.

5.1.1.3 Dependence on delay time

One particular effect observed in the Poly-Si current characteristics was related to the high traps density existing in this material. It was noticed that, when the gate bias approximates to the threshold voltage (moment in which the channel is created) a noticeable hump in the curves is produced (Figure 5.4). However, if the delay time (time between each measurement) was increased, the traps achieved to be filled reducing considerably this slit.

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[1] As expected, there is no DIBL (Drain-Induced-Barrer-Lowering) effect.

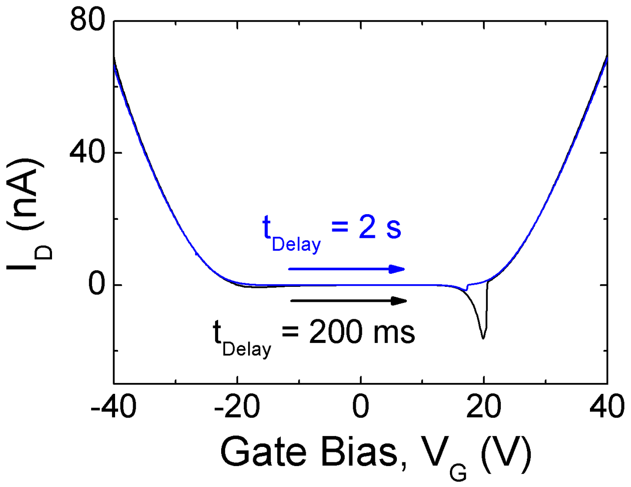

Figure 5.4. Current curves as a function of the gate bias when the delay time is modified at two values: 100 ms, and 2 s. V_D = 100 mV, V_S = 0 V, P = 90 g.

The reason comes from the nature of a Pseudo-MOS: the Si and oxide layers form a capacitor which is charged when the gate bias is modified. When V_G changes from negative values to zero, some charge is stored at both sides of the BOX (Figure 3.1). Then, if V_G continues increasing (to positive values), those carriers must to be released before the capacitor is charged again, now with opposite charge. This step implies certain time which is amplified if Poly-Si wafers are considered because the high trap density increases the amount of carriers to release. So, if the sweep time rises, the hump is reduced.

5.1.1.4 Mobility results

Finally, by making use of the Y-function, mobility values were extracted for the four Poly-Si samples and reported in Table 5.2.

Sample name	t_{Si} **(nm)**	t_{BOX} **(nm)**	t_{Ox_Sup} **(nm)**	$\mu_H (cm^2/Vs)$	$\mu_E (cm^2/Vs)$
1	15	145.3	20	7.22	7.77
2	22	145.3	6	5.18	6.51
3	40	145.3	20	7.06	7.41
4	47	145.3	6	7.04	7.52

Table 5.2. Mobility values calculated for Poly-Si wafers.

The low mobility results demonstrate once again the impact of the Poly-Si film on electrical characteristics.

5.2 Graphene-On-Insulator samples

Graphene is a promising candidate as a material for future electronics [GN07]. However, a long way has still to be run and, for example, new characterization tools to study and monitor its electrical properties have to be developed. This issue has been the subject of a large number of manuscripts devoted to study this promising material [Ruo13].

When the characterization targets electrical parameters, microsized graphene sheets with ad hoc fabricated contacts (electrodes) have been extensively used [FHBP12]. From an industrial monitoring perspective, this task requires complex post-processing of the samples, which takes time and cost. In this Section, an alternative method for the electrical characterization of as-fabricated large CVD Graphene-On-Insulator substrates is described.

5.2.1 Methodology

The Graphene-On-Insulator (GOI) samples employed in this study had a 10 mm × 10 mm graphene layer placed on a 20 mm × 20 mm of SiO_2 (insulator) with a thickness of $t_{Ox} = 90$ nm. Below the insulator, a highly p-type doped Silicon substrate was found. The samples were provided by AMO-GmbH and Figure 5.5 shows an actual image of one of them.

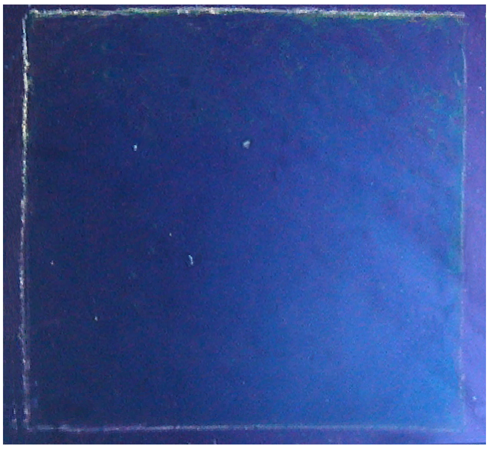

Figure 5.5. Image of the graphene in one of the samples used.

In order to carry out a detailed inspection of the possible defects at the surface substrates, they all were visualized using a Nikon Eclipse LV150N microscope[2]. Some of the captures taken are included in Figure 5.6. As observed, the samples are not totally free of imperfections since the surface presents several breaks.

The point-contact methods (two point-contact Figure 5.7.(a) and four point-contact Figure 5.7.(b)) were applied for the characterization of graphene samples. The configurations served also for capacitance measurements (Figure 5.7.(c)).

The equipments required were[3]: the Jandel probe station (Figure B.10), the Janis ST-500-2 probe station (Figure 5.8), and the Keithley 4200-SCS semiconductor analyzer (which has four SMUs to perform the measurements, Figure B.4). Two probe stations were used in these

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[2] A further description of this equipment is found in Appendix B

[3] A extended description of each machine is included in Appendix B

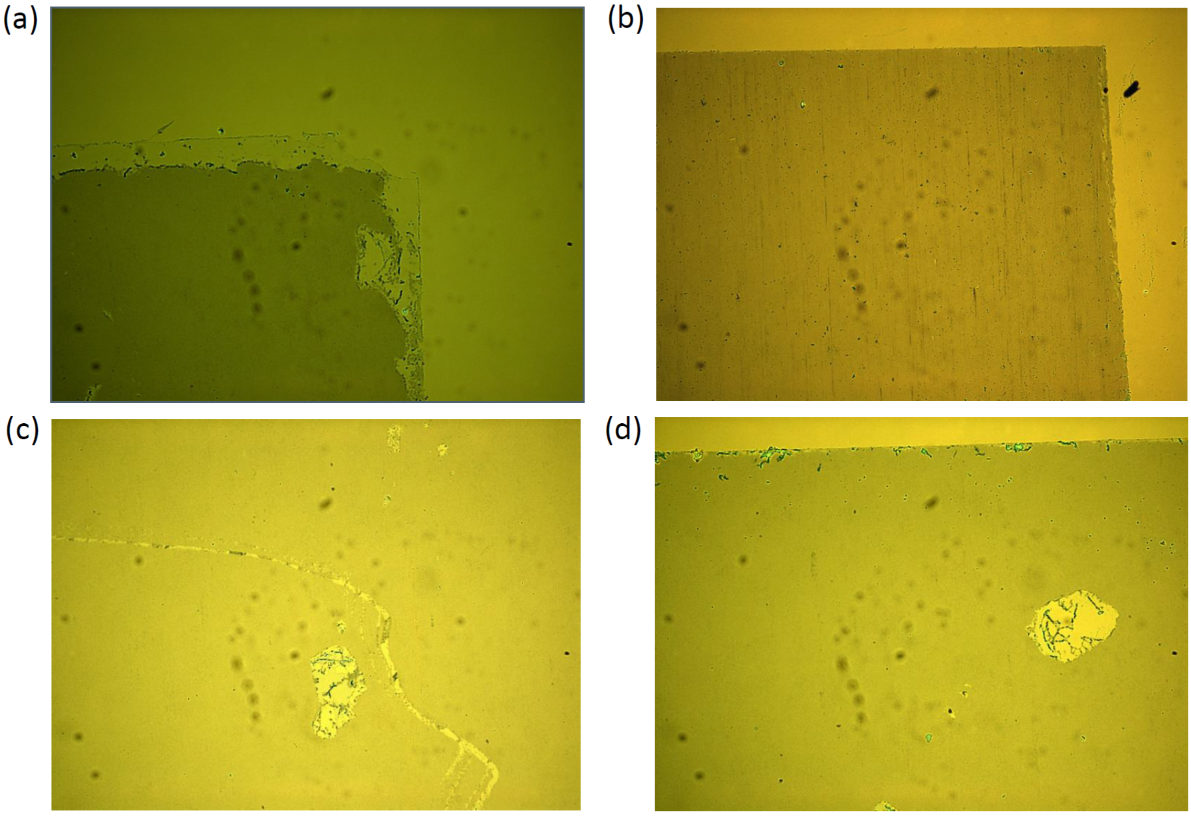

Figure 5.6. (a)-(d) Microscope images of the graphene in one of the samples used taken lens 100X objective.

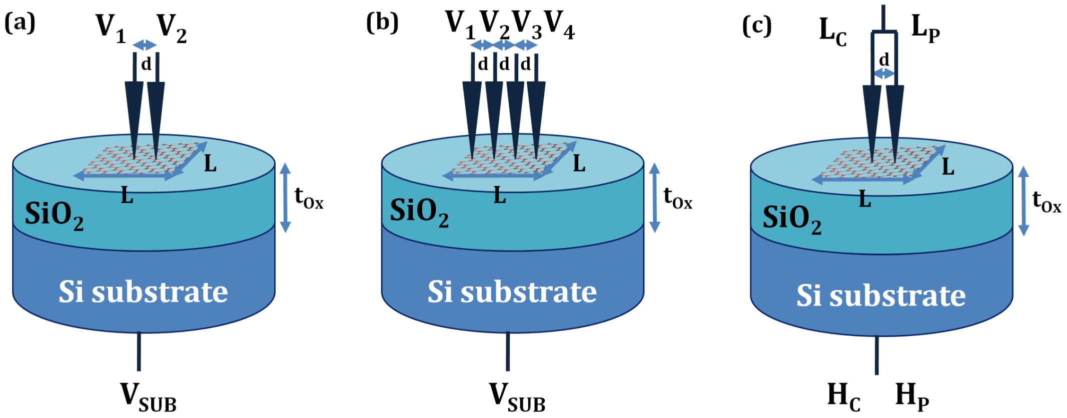
(a)
V_1 V_2
d
L
L
t_{ox}
SiO_2
Si substrate
V_{SUB}
(b)
$V_1 V_2 V_3 V_4$
d d d
L
L
t_{ox}
SiO_2
Si substrate
V_{SUB}
(c)
L_C L_P
d
L
L
t_{ox}
SiO_2
Si substrate
H_C H_P

Figure 5.7. Schematic of the (a) two point-contact and (b) four point-contact techniques used to extract I-V characteristics for electrical characterization of graphene layers. (c) Setup employed for capacitance measurements.

experiments because, although with the Jandel equipment the needle pressure is well controlled (to 5 g to 100 g), the distance between the probes is limited to certain values (1.59 mm, 3.18 mm, 4.77 mm). On the contrary, with the Janis station, the probes are manually located allowing a wide variety of separations (with the help of a microscope they can be moved in terms of microns), but the pressure cannot be exactly adjusted in a repetitive way. Because of that, in this second scenario, extra caution was paid in order to avoid the perforation of the samples.

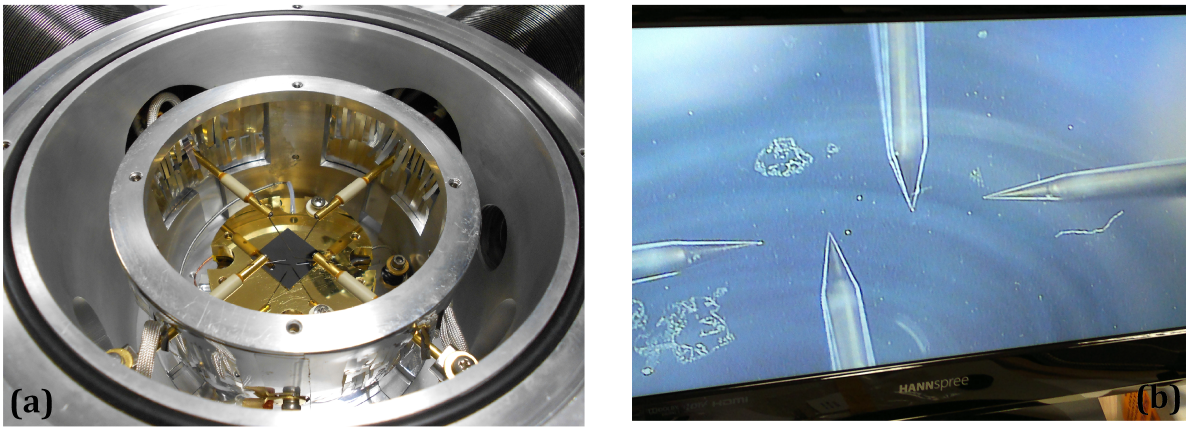

Figure 5.8. (a) Image of one of the graphene samples positioned on the metallic chuck of the Janis station. (b) The microscope facilitates the location of the needles on the sample.

5.2.2 I-V characteristics

5.2.2.1 Initial calibration

The first measurements performed had as objective to adjust the pressure of the needles in the two-needles method (Figure 5.7.(a)). Figure 5.9.(a) depicts the current curve obtained for $V_1 = 1$ V, $V_2 = 0$ V and V_{SUB} floating demonstrating the linear resistive behavior of the graphene layer. On the other hand, Figure 5.9.(b) shows the current between the probes for a certain V_{12} value as a function of the probe pressure. For a distance of 1.59 mm between needles a good saturation was achieved above a load of 50 g (approximately 250 MPa), and it was taken as the optimum pressure.

As in case of SOI samples studied in the previous Chapters (for example, in Section 2.3.1), this initial calibration is essential to guarantee reproducible measurements.

5.2.2.2 Impact of the substrate bias

Figure 5.10 illustrates the dependence of the driven current in a two-needle configuration with the substrate bias (vertical electric field) when $V_1 = 1$ V and $V_2 = 0$ V. As observed, it is minimal ($< 5\%$) as expected from a zero-band-gap material.

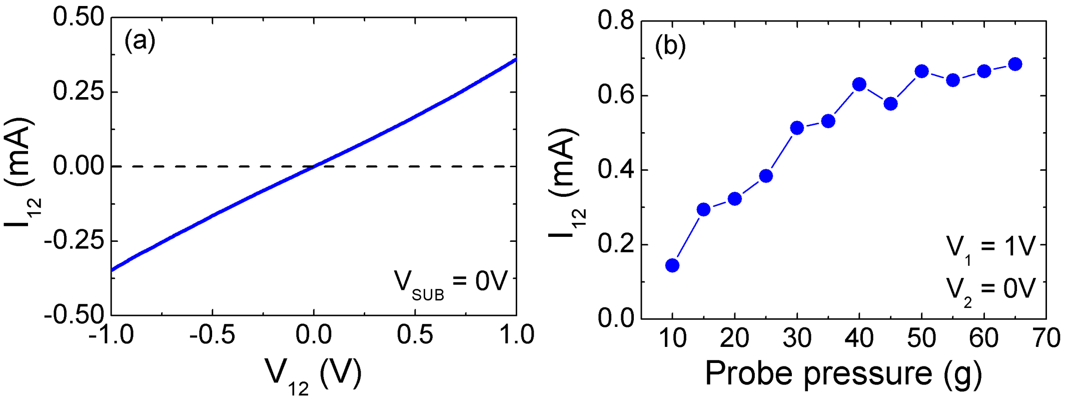

Figure 5.9. (a) Current obtained when a two-needle configuration is employed in a square shaped graphene layer on insulator layer satisfying $d << L$. (b) Current as a function of the needle pressure for $V_{12} = 1$ V. The current remains saturated above 50 g. Higher pressures only contribute to damage the underneath SiO_2 layer until physical breakdown. $V_{SUB} = 0$ V, d = 1.59 mm.

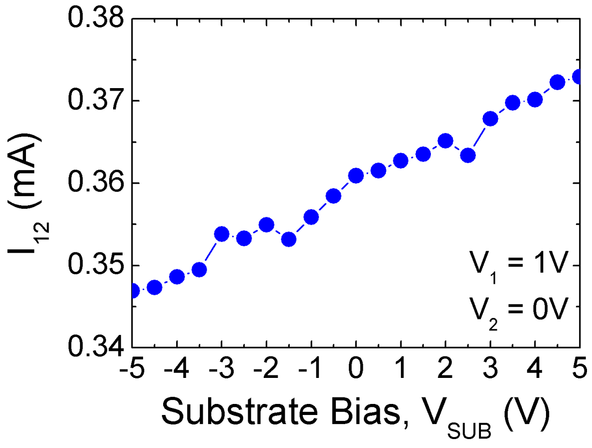

Figure 5.10. Drain current at a given bias point as a function of the substrate bias from -5 V to 5 V. $t_{BOX} = 90$ nm, $N_{D-substrate} = 10^{18} cm^{-3}$.

5.2.2.3 Resistance measurements

Considering the two point-contact configuration of Figure 5.7.(a), the circuit associated to these kind of I-V measurements is illustrated in Figure 5.11.(a), and the total resistance R_T can be expressed by Eq. (5.1) [Sch06]:

$$R_T = \frac{V_{12}}{I_{12}} = R_{graph} + 2R_{CON} + 2R_W = R_{graph} + R_{par} \tag{5.1}$$

where R_W is the wire or probe resistance, and R_{CON} is the contact resistance consequence of the simultaneous measurement of the voltage while the current is flowing. In these experiments, Tungsten-Carbide tips were used leading, potentially, to a large R_{CON} value due to the similar graphene work-function [NNKT10]. Finally, R_{grap} is the resistance of the device under test or

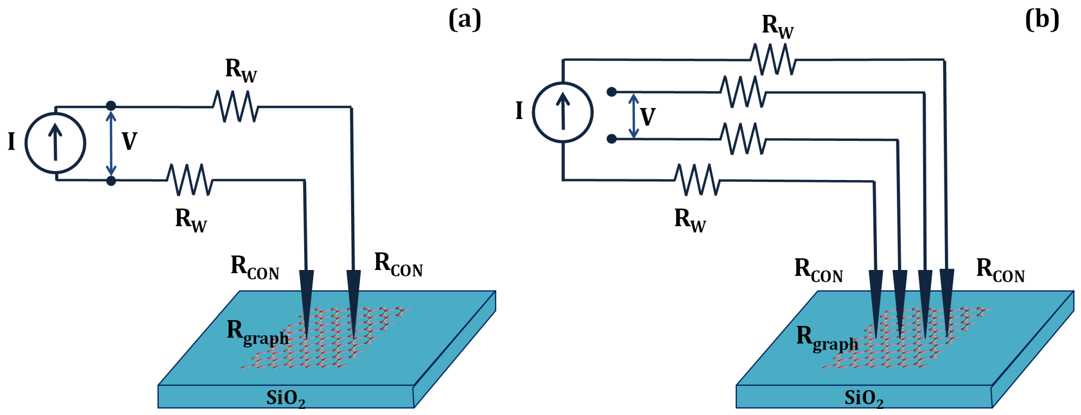

Figure 5.11. Schematic of (a) two-terminal and (b) four-terminal resistance measurements.

DUT, i.e. the graphene layer. Clearly, it is impossible to determine R_{graph} directly with this measurement arrangement due to extra resistances associated to the experimental setup which were grouped in a parasitic resistance called R_{par}.

A more accurate alternative is the four point-contact scheme of Figure 5.7.(b) whose equivalent is depicted in Figure 5.11.(b). With this setup it is possible to obtain the sheet resistance of the graphene, ρ_{Sgraph}, when the probes are located far away from the graphene borders through the formula [Sch06]:

$$\rho_{Sgraph} = R_{graph}\frac{W}{d} = \frac{\pi}{ln(2)}\frac{V_{23}}{I_{14}} \tag{5.2}$$

where W is the equivalent width of the current flow and d the separation between probes[4]. In this way, the total resistance for a two-needle configuration can be expressed combining Eq. (5.1) and Eq. (5.2) as follows:

$$R_T = \frac{V_{12}}{I_{12}} = \frac{\rho_{Sgrap}}{W}d + R_{par} \tag{5.3}$$

which corresponds with the equation of a line that will cross the axis at the point equal to R_{par} and whose slope will determine the value of ρ_{Sgrap}/W. It worths mentioning that R_{par} is a constant value in the setup, so it does not depend on the separation between contacts.

Figure 5.12.(a) shows the values for R_T obtained experimentally as a function of the separation of the needles, d. A regression line was also added. As observed, $R_{par} = 1250 \pm 50\Omega$. This result is relatively high and it is essentially because of the large difference between the work functions of the graphene and the tungsten [NNT13].

On the other hand, further exploitation of the two-needle configuration requires the determination of the form factor for the current flow between the needles ($f_g \approx d/W$). So, through the values of the sheet resistance ρ_{Sgrap} by four point-contact technique and R_{par}, the geometric factor can be obtained from Eq.[5.3] as:

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[4] On first approach it was assumed a linear relation between resistance and probe separation.

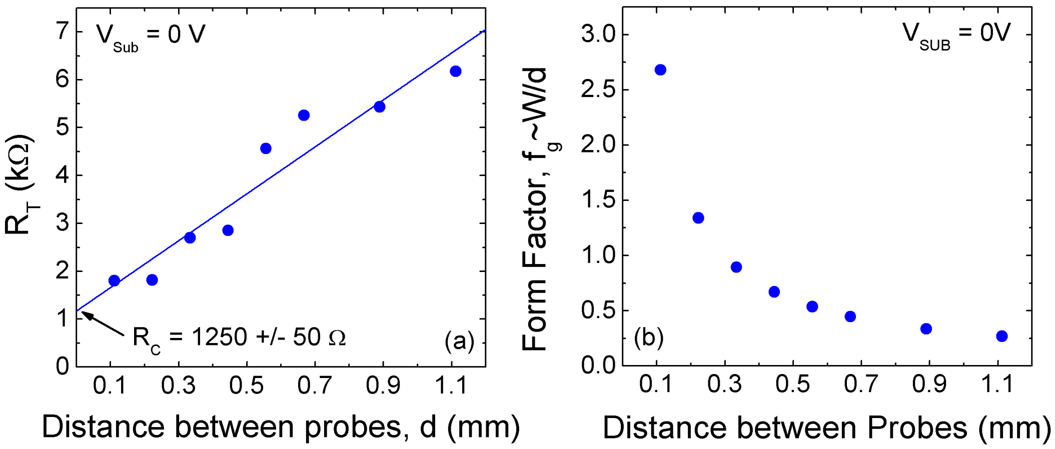


Figure 5.12. (a) Total resistance between probes for two-point contact configuration as a function of the probe separation. Linear regression for $d = 0$ allows the extraction of the contact resistance. (b) Form factor of the current flow for two-point contact configuration extracted combining four-probe and two-probe measurements. $V_{SUB} = 0$ V, $t_{BOX} = 90$ nm, $N_{D-substrate} = 10^{18} cm^{-3}$.

$$\frac{W}{d} = \frac{\rho_{Sgrap}}{R_T - R_{par}} \tag{5.4}$$

Figure 5.12.(b) depicts the values extracted for the form factor. It is observed that, when the separation between needles increases, f_g is reduced, resulting a constant of approximately 0.25 for large probe separation ($d > 1$ mm). This results satisfies the assumption that the current lines flow more straight (less dispersed) to larger distances d. The primary actor in the form factor, f_g, is the distance d, since $f_g \times d$ is basically a constant.

5.2.2.4 Obtaining of the carrier mobility

One useful application of the technique is the fast monitoring of graphene quality by extracting parameters such as the carrier mobility through the expression of the conductivity [Sch06]:

$$\sigma_{grap} = qn\mu_{graph} \tag{5.5}$$

$$\mu_{graph} = \frac{\sigma_{graph}}{qn} = \frac{1}{\rho_{Sgraph} qn} \tag{5.6}$$

where q is the electron charge (1.6×10^{-19} C) and n is the carrier density which was assumed as $10^{12} cm^{-2}$ [CJX+08].

The conductivity results using a four point-contact configuration when the substrate bias is modified are shown in Figure 5.13. Two separations between needles were considered (called d). The conductivity values are independent of the probe distance and decreases until the Dirac point is achieved.

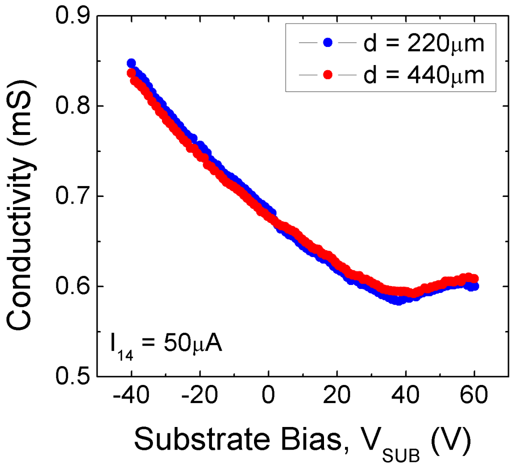


Figure 5.13. Conductivity as a function of the substrate voltage obtained from four-probe contact measurements for two different probe separation: $d = 220\mu$ m and $d = 440\mu$ m. $t_{BOX} =$ 90 nm, $N_{D-substrate} = 10^{18}cm^{-3}$.

The results obtained for two graphene samples (clean and contaminated) are presented in Figure 5.14. The extracted value for the surface conductivity was 0.75μS which turns into a mobility of $4400cm^2/Vs$. This value is lower than expected if only the optical phonon scattering due to the SiO_2 substrate (BOX) would be considered, and may reflect the impact of the needles to graphene contacts. On the other hand, as the number of defects increases, graphene mobility values reduce dramatically more than 60%. This method can be used for vendors and research laboratories for the fast characterization of samples.

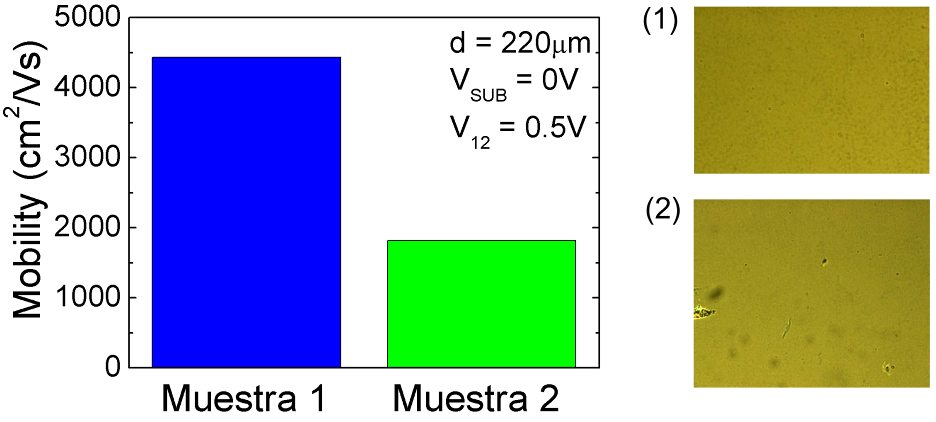


Figure 5.14. Carrier mobility extracted by the proposed four-point contact configuration for clean and contaminated samples of graphene and the actual microscope images of them. $t_{BOX} =$ 90 nm, $N_{D-substrate} = 10^{18}cm^{-3}$.

5.2.3 C-V characteristics

Capacitance measurements were performed with the impedance analyzer and a series resistance model (as explained in Chapter 3). For these measurements, the surface needles were short-circuited acting as low electrodes (Lc, Lp) and the substrate was connected to the high (Hc, HL) electrode [Sch06]. The resulting capacitance curves as a function of the frequency of the AC excitation signal are shown in Figure 5.15.a.

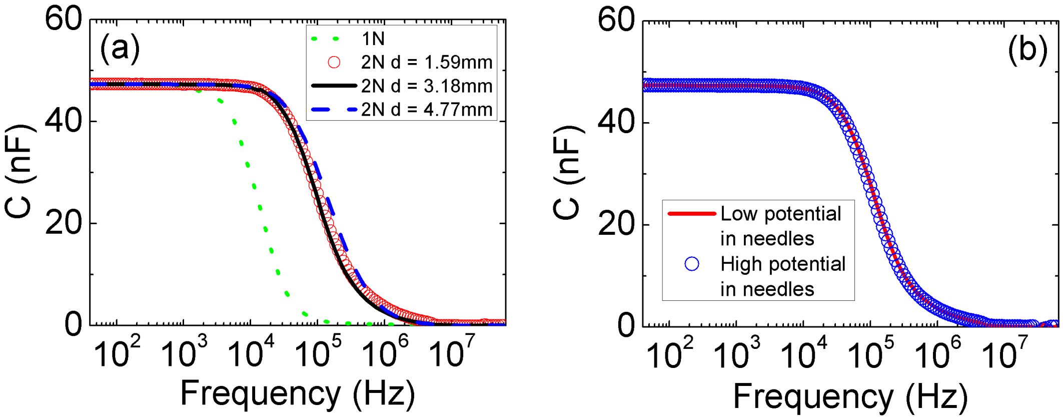


Figure 5.15. (a) Capacitance curves as a function of the excitation signal frequency. (a) Using one and two needles and considering several distances between them. (b) Exchanging the high and low potentials in the experimental setup. $t_{BOX} = 90$ nm, $N_{D-substrate} = 10^{18} cm^{-3}$.

Different configurations of the surface needles (single needle, two-needle with different inter-distances) have been considered. For a given sample, the maximum value of the capacitance is independent of the needle distribution confirming the reliability of the technique. It is worth noting that, for defective-free graphene layer, the capacitance obtained corresponds to that of an ideal plate capacitor ($C = S_{Graph} \epsilon_{SiO_2} / t_{BOX} = 45$ nF). The different cut-off frequencies must be further investigated and may be attributed to limited carrier spreading effects.

Finally, Figure 5.15.(b) shows the capacitance curves obtained when the high and low potentials are exchanged. The results are identical demonstrating no impact of the Silicon substrate.

5.3 Determination of ad hoc deposited charge on bare SOI wafers

In Chapter 4 the importance of the quality of the top surface in bare SOI wafers was widely studied for passivated and non-passivated Pseudo-MOSFET samples. In this Section, an alternative work is explained which evaluates the variation of the channel properties when an amount of charge is deposited intentionally on the surface.

As said, the top surface plays a crucial role on the channel properties through the top density of interface traps (D_{it2} in Figure 5.16) [HAHC07]. The effect of the traps is particularly noticeable when the Silicon film thickness is scaled down to the decananometer range and the coupling between the channel and the surface is strengthen [CC07]. This impact is amplified for non-passivated surfaces where D_{it2} can reach values over $10^{13} cm^{-2} eV^{-1}$ [HAHC07].

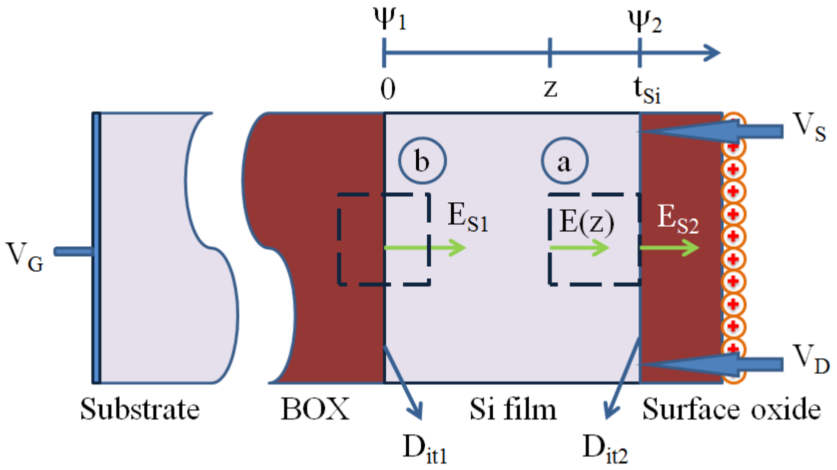


Figure 5.16. Simplified cross-section of a SOI wafer for Pseudo-MOSFET characterization technique: V_S is the source voltage and V_D is the drain voltage, both applied by pressure adjustable probes; V_G is the gate (substrate) voltage. D_{it1} and D_{it2} represent the density of interface states at BOX/Si film and Si film/top surface interfaces respectively. Two Gaussian surfaces in both edges of the Si film (dashed line, (a) and (b)) are represented

In contrast, the density of interface states at the Si/BOX interface takes a minor role on the electrical characteristics of the induced channel since D_{it1} is typically well below $5 \times 10^{13} cm^{-2} eV^{-1}$.

It has been shown by Ionica et al. [IDC11] that the ad hoc deposition of charged particles on the free surface of the wafer, influences additionally on the Pseudo-MOSFET electrical parameters by modifying the conduction of the electron or hole channels. In this Section a theoretical model has been derived to calculate the amount of deposited charge on the surface by its impact on the shift of the threshold voltage observed in static I-V curves. This model can be used to establish a closed protocol to correlate the change in electrical parameters with the concentration of a charged solution.

5.3.1 Development of the model

Firstly, Gauss law was applied to the first closed-surface shown in Figure 5.16 (noted as surface (a)) in order to establish the boundaries conditions at the top oxide/Si film interface [Sch06]. The continuity of the electrical displacement at $x = t_{Si}$ yields:

$$-\epsilon_{Si}\left(\frac{\partial \psi}{\partial x}\right)_{x=t_{Si}} = Q_{x=t_{Si}} \tag{5.7}$$

where ψ is the electrostatic potential along the z direction. If we assume that traps are uniformly distributed in terms of energy, the associated interface charge can be considered proportional to the potential [RCG09]; the electric field at the top oxide/Si film is:

$$E_{S2} = \frac{qD_{it2}\psi_{S2} + Q_{SUP}}{\epsilon_{Si}} \tag{5.8}$$

Q_{SUP} represents the ad hoc deposited charge (uniformly distributed on the surface) and ψ_{S2} is the potential at the top surface.

Similar conditions were also applied to the surface (b) in Figure 5.16 (BOX/Si film interface) resulting:

$$\epsilon_{BOX}E_{BOX} - \epsilon_{Si}E_{S1} = Q_{x=0} \tag{5.9}$$

Developing Eq. (5.9) and assuming a linear drop of the electrostatic potential inside the BOX we obtain:

$$\frac{V_G - \phi_{fb} - \psi_{S1}}{t_{BOX}} - \epsilon_{Si}E_{S1} = qD_{it1}\psi_{S1} \tag{5.10}$$

where ϕ_{fb} is the flatband voltage ($\phi_{fb} = 0$ in our case and ψ_{S1} is the potential at the channel interface.

Lastly, the potential profile inside the Silicon film can be approximated by a linear law for non-passivated samples, since the field tends to be constant across the film [Sch06]:

$$E_{S1} = E_{S2} = \frac{\psi_{S1} - \psi_{S2}}{t_{Si}} \tag{5.11}$$

Combining Eq. (5.8), (5.10) and (5.11) the expression for the threshold voltage of the induced channel accounting for the surface charge is given by Equation (5.12).

$$\begin{aligned} V_G = \left[\phi_{fb} + \psi_{S1}\left[1 + \frac{C_{it1}}{C_{BOX}} + \frac{C_{Si}C_{it2}}{C_{BOX}(C_{Si}+C_{it2})}\right]\right] + \\ + Q_{SUP}\frac{C_{Si}}{C_{BOX}(C_{Si}+C_{it2})} \end{aligned} \tag{5.12}$$

where $C_{BOX} = \epsilon_{BOX}/t_{BOX}$ is the buried oxide capacitance, $C_{Si} = \epsilon_{Si}/tSi$ is the Silicon film capacitance, and $C_{it1} = qD_{it1}$ and $C_{it2} = qD_{it2}$ are the capacitances associated to traps in each interface of the Si film.

The first term in the second part of the Eq. (5.12) corresponds with the formula of the threshold voltage in a Pseudo-MOSFET structure [4]. So, for the threshold condition ($\psi_{S1} = 2\phi_F$, $V_G = V_{TH}$) the charge deposited at the surface on the sample can be related to the threshold bias shift (ΔV_{TH}) with respect to the untreated surface by the lowing equation:

$$Q_{SUP} = \Delta V_{TH}\frac{C_{BOX}(C_{Si}+C_{it2})}{C_{Si}} \tag{5.13}$$

The final expression for Q_{SUP} takes into account not only the thickness of the SOI sample, but also the quality of the top oxide. The densities of states D_{it1} and D_{it2} can be determined experimentally on a previous stage by calibrating Eq. (5.12) when $Q_{SUP} = 0$ [Sch06].

5.3.2 Experimental results

In order to check the validity of the model, several experiments were carried out depositing a charged solution on the SOI samples and performing Pseudo-MOSFET measurements.

A total of 15 cells of a non-passivated SOI sample were measured (INSET of Figure 5.17) with 12nm-thick Si film and 145nm-thick BOX. This sample was chosen because of its ultrathin Si film since the ad-hoc charge will have a stronger influence on the channel electrical characteristics leading to a noticeable shift in $I_D(V_G)$ curve. The experimental methodology followed was:

1. Calibration of the probe pressure was done on first stage. At 80 g the transconductance peak saturates so this pressure was established as the optimum.
2. All the cells involved in the study were characterized as detailed in Section 2.3.4 to extract the threshold voltage reference values.
3. Then, the sample was introduced into a 2% solution of Amino-Propyl-Tri-Ethoxy-Silane (APTES) [com14] diluted in acetone for 30 sec. Next, it was cleaned with distilled water and left into a class-10 clean cabin for 24 hours.
4. Finally, the threshold voltage is extracted again, and the value of Q_{SUP} is calculated from the model (Eq. (5.13)). Both hole and electron channels are probed taking the statistical mean of threshold voltages for the 15 cells.

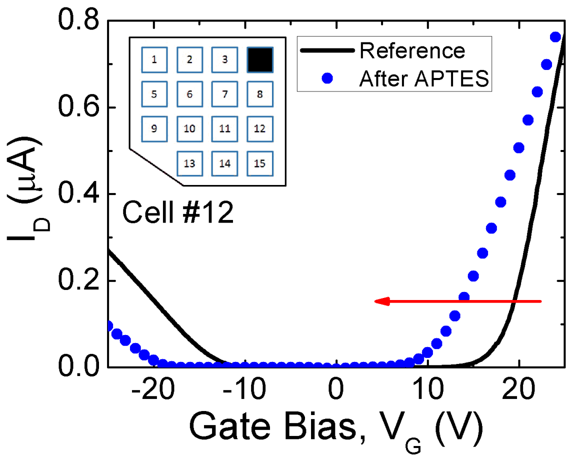


Figure 5.17. When a positive charged layer is added on the wafer surface, a shift of the current curves is produced (pointed by the arrows). The gate bias, V_G, was modified from -25V to 25V and the sweep total time was approximately 60s. INSET: Schematic of the sample containing the MESA isolated SOI cells. t_{Si} = 12 nm, t_{BOX} = 145 nm.

Figure 5.17 shows an example of the voltage shift observed in the current characteristics obtained for one of the SOI cells. The APTES treatment creates an amino-terminated layer on the surface which is positively charged [com14]. It reduces the electrostatic potential inducing negative charge below the surface oxide (capacitive coupling). The film inversion is favored (the threshold voltage for electrons decreases) whereas the film accumulation is lessened (residually doped p-type wafer). The average values of V_{TH-H} and V_{TH-E} were also monitored for the

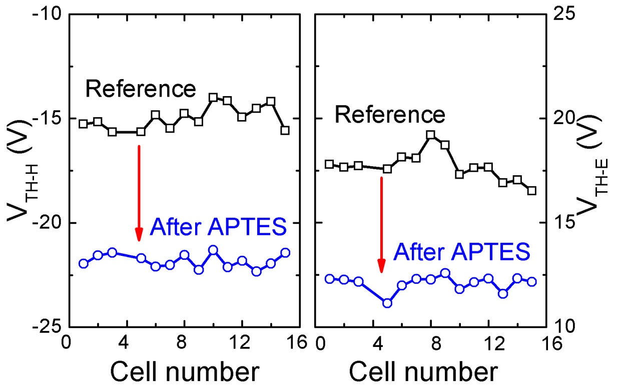


Figure 5.18. Threshold voltages for hole (left) and electron (right) channels extracted from the $I_D(V_G)$ curves before (squares) and after (circles) the APTES layer is created on the native oxide of the cells. 15 cells were probed. $t_{Si} = 12$ nm, $t_{BOX} = 145$ nm.

Table 5.3. Set of data employed to extract Q_{SUP} through the model given by Eq. (5.13). The different intermediate parameters extracted for hole and electron channel are presented.

Hole channel	**Reference**	**After APTES**
$< V_{TH-H} > (V)$	15.38	-22.25
$< D_{it2-H} > cm^{-2}eV^{-1}$	1.47×10^{13}	1.47×10^{13}
$< Q_{SUP} > C/cm^2$	-	3.32×10^{-6}
Electron channel	**Reference**	**After APTES**
$< V_{TH-H} > (V)$	17.02	12.11
$< D_{it2-H} > cm^{-2}eV^{-1}$	2.37×10^{13}	2.37×10^{13}
$< Q_{SUP} > C/cm^2$	-	3.76×10^{-6}

fifteen as-fabricated cells (reference) and the cells after the APTES deposition. Results are shown in Figure 5.18.

To conclude, Table 5.3 summarizes the absolute value of the extracted surface charge Q_{SUP} by applying Eq. (5.13) from the average values of Figure 5.18. The value of D_{it2} was calibrated from the models in [RCG09] using $D_{it1} = 2 \times 10^{11} cm^{-2}eV^{-1}$ (obtained for non-passivated samples).

The agreement between the values of Q_{SUP} extracted for hole and electron channels demonstrate the usefulness of the model to evaluate charge deposited on the surface of the wafer and measured by a simple point-contact method.

5.4 Conclusions

In this Chapter several novel applications for point-contact techniques have been described. Firstly, Pseudo-MOSFET method has been employed on Poly-Silicon wafers (not studied until now) in order to compare the results with those obtained from Silicon substrates.

Then, a new method of electrical characterization of Graphene-On-Insulator samples has been introduced demonstrating that the point-contact technique is reliable to extract electrical parameters and that it may serve to determine the quality of graphene samples (density of impurities, defects on surface, etc.).

Finally, a theoretical model to obtain the surface charge in a Pseudo-transistor when a certain charge solution is intentionally deposited on the bare surface has been presented. The model is based on Gauss law applied to both interfaces of the Silicon film and its accuracy has been tested over several SOI samples. The results point the Pseudo-MOSFET technique as a potential and simple platform for sensing applications.

Chapter 6

Conclusions and Future Steps

This final chapter summarizes the main achievements and conclusions obtained from this thesis. Future work and possible improvements based on the results are also commented.

6.1 Main achievements

This work has been focused on a deep and systematic study of the point-contact pseudo-MOSFET characterization technique. From the basics to its potential applications beyond SOI wafers characterization, the main contributions of this work are listed next:

1. Theoretical models for the Pseudo-MOSFET have been described and developed for ultrathin Si wafers, and for those with also ultrathin BOX. In these models, the presence of traps at the interfaces have been taken into account since, when the dimensions of the layers are scaled down, the coupling effects become more noticeable.
2. In order to validate the proposed models, several Pseudo-MOSFETs with different dimensions have been simulated using SILVACO software. In addition, the impact of the charge on the surface has been studied allowing the analysis of passivated and non-passivated samples.
3. In the laboratory, some Pseudo-MOSFET samples with distinct thicknesses and surface conditions (passivated/non-passivated) have been analyzed and characterized. For all of them, the optimum needle pressure to carry out the measurements has been determined, as well as other electrical parameters such as the threshold voltage (V_{TH-H}, V_{TH-E}) or the carrier mobility.
4. The impact of the setup parameters on experimental current characteristics have been also studied. So, measurements changing the probe pressure and varying the probe interdistance were performed on a same cell. Futhermore, the implications of repeating the experiment many times at the *same* positions of the cell or the variations observed by performing the same measurement in all the cell of a sample were analyzed.
5. Capacitance measurements were carried out directly on the SOI wafer due to the intrinsic capacitor structure of the SOI stack. The impact of experimental conditions on CV curves were also studied.

6. The role of the area associated with the Pseudo-MOSFET capacitance for Split-C(V) measurements was clarified. The area dependence with the AC frequency, in single-needle and multiple-needle configuration, was reproduced with a simple intuitive model. Then, the model has been extended to N-needle configuration proving its validity by comparison with experimental results.

7. The impact of the effective electric field on the carrier mobility extracted by in-line point-contact measurements on bare SOI wafers was analyzed. The comparison between four point and two point measurements has also allow us to obtain precise form factors for the current flow validating the Pseudo-MOSFET configuration for the extraction of the $\mu(E_{eff})$ characteristics.

8. Others measurements were performed using different substrates in which the Silicon film was replaced by another material. In this work, Poly-silicon substrates were characterized. Furthermore, Graphene-On-Insulator samples were explored demonstrating that the Pseudo-MOSFET technique can be applied (not only to Silicon wafers) with the same reliability.

9. A theoretical model to obtain the surface charge in a Pseudo-MOSFET when a certain charge solution is intentionally deposited on the bare surface was presented and its accuracy was tested over several SOI samples. The results point out the Pseudo-MOSFET technique as a potential and simple platform for sensing applications.

10. The study about the effective electric field was also carry out in FD-SOI MOSFETs. Here, the return point of the effective field was presented as a convenient tool for the selection and understanding of the optimal bias conditions to enhance the mobility in these transistors by using back-gate bias.

11. Finally, the steps in the fabrication process of Pseudo-MOSFET cells were studied, and applied for the fabrication os several samples during a visit to IMEP-MINATEC clean-room.

6.2 Future research topics

Based on this work, there are still open questions and improvements to be developed in future research projects:

1. Extend the study of the geometrical factor f_g in the two-needle configuration measurements.

2. Development of a three-interface model based on the electrostatic potential for high resistivity SOI substrates.

3. Study the impact of the material of point-contact electrodes on the contact resistance to corroborate the field emission approximation.

4. Evaluate the need to include quantum corrections in the Pseudo-MOSFET models for ultrathin SOI films.

5. Complete the analysis of the Pseudo-MOSFET as a sensor platform through the functionalization of the top surface with specific analytes.

Appendix A

Expansion of the Effective Mobility Study to FD-MOSFETs

A.1 Introduction

Thanks to the equipments available in the Nanoelectronics Laboratory, it is not only possible to carry out the characterization of SOI substrates, but also a device-level study. The laboratory facilities are equipped with two semi-automatic probe systems (detailled in Appendix B.1.8) that were used during this part of the work. The objective was to perform a wide study of the effective electric field (similar to that presented in Chapter 4) but with SOI transistors.

A.2 Fully-Depleted SOI transistors

Fully-Depleted (FD) SOI technology offers excellent electrostatic control, which translates in better scalability and performance, from low-power to high-speed applications. In planar SOI MOSFETs with thin buried oxide (BOX) and ground-plane (GP), the GP biasing is an effective option for boosting the device characteristics. The GP or back-gate voltage, V_{G2}, is tuned to adjust the threshold voltage in OFF and ON states. But, V_{G2} can also serve for triggering the volume inversion regime, where mobility enhancement has been demonstrated [CMG+07]. Recent works have demonstrated that back-gate biasing leads to unusual *multibranch* mobility behavior in FD-SOI MOSFETs and have shown qualitatively that the mobility can sometimes be improved [NRO+12]. In this study, the bias regions where the mobility is enhanced (or not) were determined quantitatively and practical guiding rules are given to select the proper bias range for mobility boost.

A.3 Return point of effective field

The effective field in a MOS transistor, E_{eff}, is defined as the average of the local transverse electric field, $E(z)$, weighted by the local density of inversion carriers, $n_{inv}(z)$[SH99]:

$$E_{\mathrm{eff}}(V_{\mathrm{G1}}, V_{\mathrm{G2}}) = \frac{\int |E(z, V_{\mathrm{G1}}, V_{\mathrm{G2}})| n_{\mathrm{inv}}(z, V_{\mathrm{G1}}, V_{\mathrm{G2}}) dz}{\int n_{\mathrm{inv}}(z, V_{\mathrm{G1}}, V_{\mathrm{G2}}) dz} \tag{A.1}$$

where z corresponds to the transversal direction within the limits of the device channel (Si film in SOI MOSFETs).

A higher field accentuates the carrier confinement at the interface which in turn degrades the mobility. According to the Universal Mobility Curves (introduced in Chapter 4) were $\mu(E_{\text{eff}})$ is represented [TTIT94], the mobility decreases with increasing either the electric field, the inversion charge or the gate bias (Figure A.1). Indeed, in bulk-MOSFETs the field always increases with gate bias.

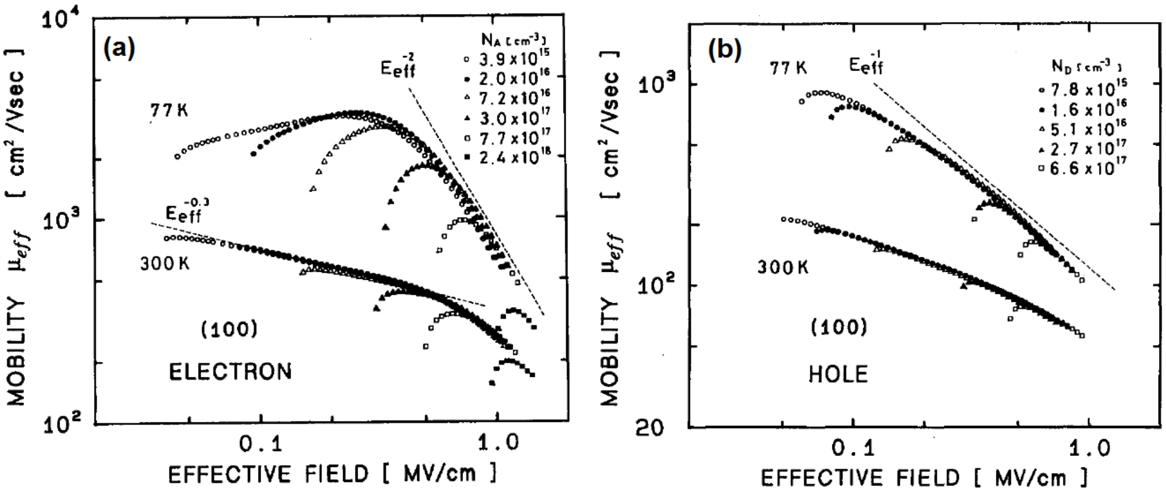


Figure A.1. UMC curves from [TTIT94]. (a) Electron mobility in the inversion layer at 300 K and 77 K versus effective field E_{eff}, as a function of substrate acceptor concentration N_A. (b) Hole mobility in the inversion layer at 300 K and 77 K versus effective field E_{eff}, as a parameter of substrate donor concentration N_D.

However, this conventional view is not necessarily true in FD-SOI transistors. While increasing V_{G1}, there is a bias range where the effective field actually decreases so that the mobility improves [CRG10]. So, the aim here was to exploit this bias window for enhancing the mobility. The ideal case would be to have the electric field decreasing for higher values of the gate bias (instead of increasing as usual). This situation does not exist in bulk MOSFETs but can be obtained in FD-SOI MOSFETs via the proper selection of the bias at the front- (V_{G1}) and back-gates (V_{G2}). To understand how this condition can be achieved, firstly the evolution of the effective field under different biasing conditions was examined.

The magnitudes of $E(z)$ and $n(z)$ involved in Eq. (A.1) are not directly accessible from the experiments, thus E_{eff} was evaluated by combining measurements and simulations done with a Poisson-Schrödinger self-consistent solver [GRCC+99]. Split-C(V) measurements were also performed from which the inversion charge was determined, by integration, as a function of gate bias [TT02]. Then, the effective mobility was obtained as:

$$\mu = \frac{I_{\text{D}}}{(\frac{W}{L} V_{\text{D}} Q_{\text{inv}})} \tag{A.2}$$

where V_{D} is the drain voltage [OCC07].

On the other hand, the initial parameters of the simulator were fine calibrated to reproduce the experimental $Q_{\mathrm{inv}}(V_{\mathrm{G1}})$ curves for each transistor, as exemplifies the Figure A.2 for a 2nm-thick Si film and 10nm-thick BOX SOI transistor. The simulation provides the inversion charge value as a function of the gate bias. Then, these results were directly compared with those calculated through Split-C(V) measurements and calibration parameters were modified until the best accuracy between curves was achieved.

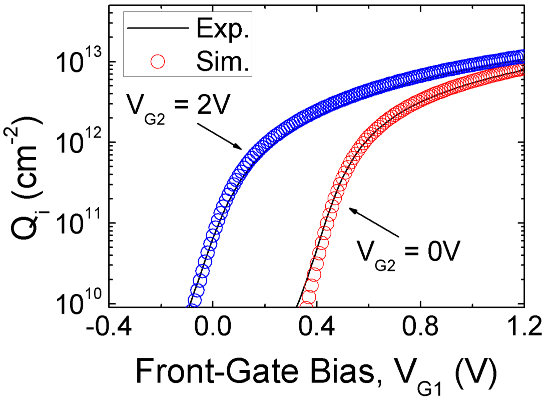


Figure A.2. Comparison of the inversion charge concentration as a function of the front-gate bias between the experimental results (open-symbols), calculated by the Split-C(V) technique, and simulation results (solid-lines) obtained after the calibration of the solver. Back-gate bias: $V_{\mathrm{G2}} = 0$ V and $V_{\mathrm{G2}} = 2$ V. $t_{\mathrm{Si}} = 8$ nm, $t_{\mathrm{BOX}} = 10$ nm, $L = W = 10$ μm, EOT = 1.3 nm.

Likewise, the simulator provides the profiles of field, $E(z)$, and the carrier density, $n_{\mathrm{inv}}(z)$, which are needed in Eq. (A.1) to calculate E_{eff}.

It is worth remarking that the mobility values showed in this study were genuinely experimental. The simulations just served to determine the effective field. This method was used in other works to generate unusual, multibranch mobility curves unaccounted by the universal mobility [NRO$^+$12, CRG10]. The same methodology was carried out here for determining the practical back-gate bias range where the mobility is maximized.

Figure A.3 shows the effective field as a function of V_{G1} for different back-gate biases. For positive V_{G2}, there is a range where two different front-gate biases can lead to the same value of effective field. Note also, for V_{G1} fixed in strong inversion ($V_{\mathrm{G1}} \geq 0.6$ V), the remarkable drop in electric field (by 0.15 – 0.2 MV/cm) achieved by turning the back-gate voltage from zero to a modest positive value ($V_{\mathrm{G2}} \cong 1.5$ V). This field reduction directly translates in improved mobility (see also Figures A.5.(b) and A.6.(b)). Even more importantly, when increasing the front-gate bias the effective field decreases until a minimum point is reached (named *return point*, V_{ret}). Beyond this point ($V_{\mathrm{G1}} > V_{\mathrm{ret}}$), the field increases monotonically due to the buildup of the front channel.

On the other hand, Figure A.4.(a) compares the potential profiles at $V_{\mathrm{G1}} = 0$ V and $V_{\mathrm{G1}} = V_{\mathrm{ret}}$ for $V_{\mathrm{G2}} = 1.5$ V demonstrating that the body potential is much flatter at the return point due to the electric field reduction. Finally, Figure A.4.(b) verifies that the effective electric field at the return point remains moderate even for relatively high back-gate bias.

The idea behind this study was to take advantage of the initial decrease in the effective field. So, the bias conditions which enable the transistor to operate in the region where E_{eff} decreases

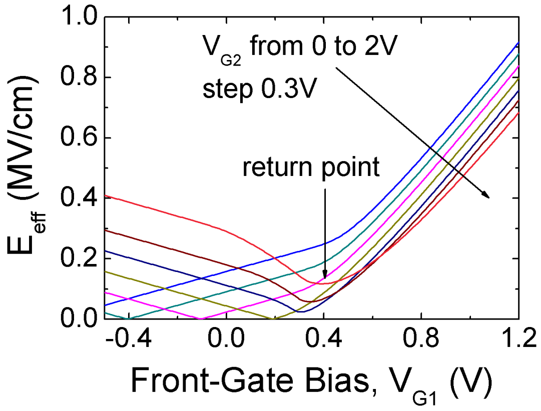


Figure A.3. Effective field evaluated with Eq. (A.1) versus front-gate bias for different values of V_{G2} (0 V, 0.3 V, 0.6 V, 0.9 V, 1.2 V, 1.5 V, 2 V). For $V_{G2} > 0$ V, two different front-gate biases lead to the same E_{eff} value. $t_{\text{Si}} = 8$ nm, $t_{\text{BOX}} = 10$ nm, $L = W = 10$ μm, EOT = 1.3 nm.

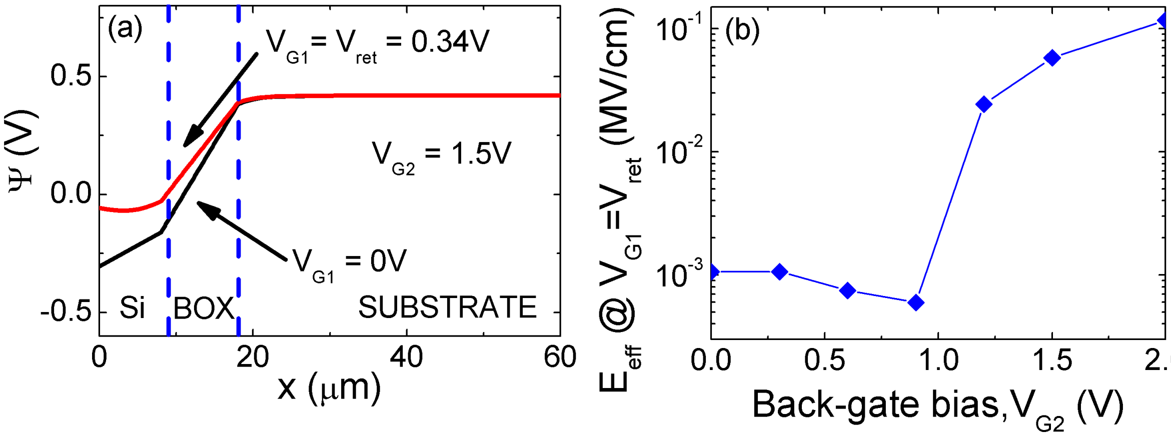


Figure A.4. (a) Electrostatic potential cross section for two values of front-gate bias ($V_{G1} = 0$ V and $V_{G1} = V_{\text{ret}} = 0.34$ V) when $V_{G2} = 1.5$ V. (b) Effective field evaluated at the return point as a function of back-gate bias. $t_{\text{Si}} = 8$ nm, $t_{\text{BOX}} = 10$ nm, $L = W = 10$ μm, EOT = 1.3 nm.

with increasing V_{G1} were investigated. The final objective was to achieve a mobility boost tunning the value of E_{eff}.

A.4 Map of bias regions

A.4.1 Ultrathin FD-SOI transistors

To exemplify the methodology explained before, transistors with ultrathin body and BOX ($t_{\text{Si}} = 8$ nm, $t_{\text{BOX}} = 10$ nm) fabricated at STMicroelectronics [FBDP^{+}09] were selected. The optimum bias range for the transistor was defined by two critical parameters, the threshold voltage, V_{TH}, and the return point voltage of the effective electric field, V_{ret} ($\partial E_{\text{eff}}/\partial V_{G1}|_{V_{G1}=V_{\text{ret}}} = 0$). The representation of V_{TH} and V_{ret} as a function of the back-gate voltage constitutes the bias map shown in Figure A.5.(a). As observed, the threshold voltage decreases linearly with V_{G2} as established by the Lim-Fossum model [LF83] for FD-SOI MOSFETs. In contrast, the return point voltage increases with V_{G2} due to the larger electrostatic potential at the back interface. A higher V_{ret} means a wider bias window where the effective field decreases and the mobility improves with increasing V_{G1}.

Three different bias possibilities for the back-gate were considered, which are illustrated by arrows in Figure A.5.(a).

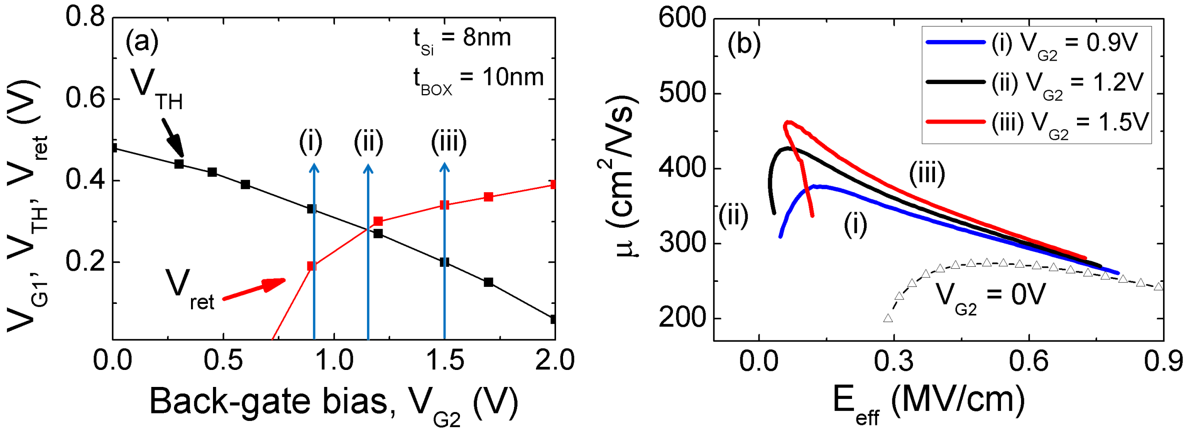


Figure A.5. (a) Bias map of experimental threshold voltage and simulated return point voltage as a function of the back-gate bias. Different regions can be distinguished: *(i)* $V_{\mathrm{G2}} = 0.9$ V: the transistor reaches the return point before the onset of the channel; *(ii)* $V_{\mathrm{G2}} = 1.2$ V: the threshold voltage and return point are reached simultaneously; *(iii)* $V_{\mathrm{G2}} = 1.5$ V: the front channel is in strong inversion before the field is minimum. (b) Experimental multibranch curves of mobility versus effective electric field for the three back-gate biases shown in (a). By comparison, the curve measured for $V_{\mathrm{G2}} = 0$ V shows lower mobility. $t_{\mathrm{Si}} = 8$ nm, $t_{\mathrm{BOX}} = 10$ nm, $L = W = 10$ μm, EOT = 1.3 nm.

- For $V_{\mathrm{G2}} = 0.9$ V (case *(i)*), increasing V_{G1}, the transistor first reaches the return point ($V_{\mathrm{ret}} \approx 0.19$ V) before the threshold voltage ($V_{\mathrm{TH}} = 0.33$ V). From the return point to the channel activation, the effective field increases. Consequently, the scattering mechanisms are amplified limiting the mobility values as observed in Figure A.5.(b).
- For $V_{\mathrm{G2}} = 1.2$ V (case *(ii)*), the device reaches the threshold voltage and the return point of the effective field simultaneously ($V_{\mathrm{G1}} = V_{\mathrm{TH}} = V_{\mathrm{ret}} = 0.28$ V, in Figure A.5.(a)). This means that, as soon as the channel is activated, the effective field increases and the mobility drops.
- More interesting is the situation $V_{\mathrm{G2}} = 1.5$ V (case *(iii)*), where the threshold voltage is reached before the return point. The front channel operates in strong inversion before the effective electric field has reached its minimum value. The consequence is outstanding: increasing the front-gate bias from $V_{\mathrm{G1}} = V_{\mathrm{TH}} = 0.2$ V to $V_{\mathrm{G1}} = V_{\mathrm{ret}} = 0.34$ V, the effective field is reduced despite the channel being enriched with minority carriers. Only when the return point is exceed ($V_{\mathrm{G1}} > V_{\mathrm{ret}}$), does the effective field start to increase.

Figure A.5.(b) shows mobility curves as a function of the effective field measured for the generic cases *(i)*, *(ii)* and *(iii)*. The beneficial effect of a positive back-gate bias is evident when comparing these curves with the mobility measured at $V_{G2} = 0$ V. If the back gate is grounded, the mobility is lower simply because the effective field is much higher, as already noted in Figure A.3.

It is noted that the case *(iii)*, where $V_{TH} < V_{ret}$, is the most favorable for mobility enhancement: the maximum mobility is boosted by a 70% (from 273 cm^2/Vs at $V_{G2} = 0$ V to 462 cm^2/Vs at $V_{G2} = 1.5$ V). The mobility gain decreases as E_{eff} increases and, apparently, all curves merge for $E_{eff} > 0.8$ MV/cm. But, such a critical field is not accommodated for the same V_{G1} voltage. For a given front-gate bias (i.e. $V_{G1} = 1.2$ V) the transistor operates with much reduced effective field ($E_{eff} = 0.73$ MV/cm) at $V_{G2} = 1.5$ V compared to $V_{G2} = 0$ V ($E_{eff} = 0.92$ MV/cm). This difference explains the significant gain in mobility.

A.4.2 Thick-BOX FD-SOI transistors

This biasing method was also applied to thick-BOX ($t_{BOX} = 145$ nm) transistors fabricated at CEA-LETI [AWM+10]. Figure A.6.(a) shows the bias map indicating the threshold voltage and return point voltage as a function of V_{G2}. Three back-gate bias conditions were again analyzed and compared with the case at $V_{G2} = 0$ V:

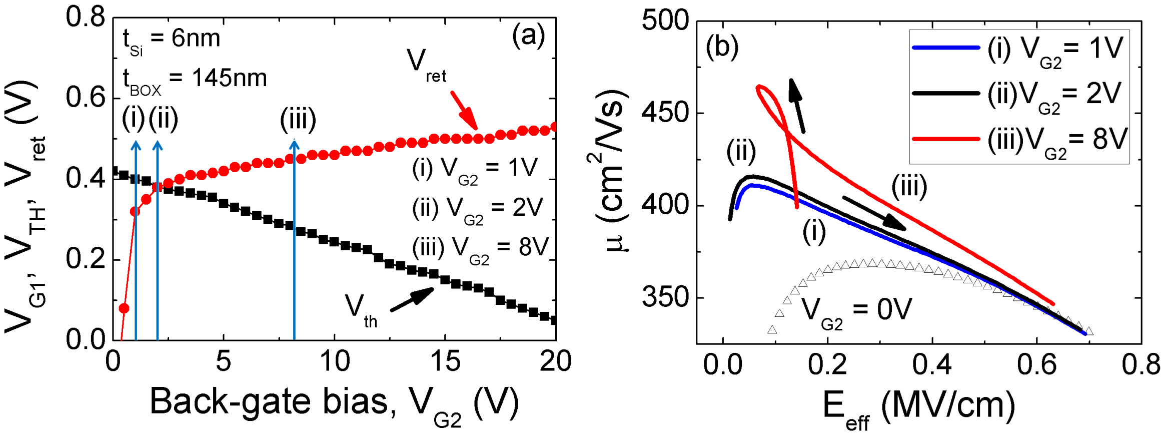


Figure A.6. (a) Experimental threshold voltage and simulated return point voltage versus back-gate bias. Three bias paths are illustrated: *(i)* $V_{G2} = 1$ V, *(ii)* $V_{G2} = 2$ V, and *(iii)* $V_{G2} = 8$ V. (b) Corresponding mobility curves. $t_{Si} = 6$ nm, $t_{BOX} = 145$ nm, $L = W = 10$ μm, EOT = 1.3 nm.

- Case *(i)*: $V_{th} > V_{ret}$ for $V_{G2} = 1$ **V**.
- Case *(ii)*: $V_{th} = V_{ret}$ for $V_{G2} = 2$ **V**.
- Case *(iii)*: $V_{th} < V_{ret}$ for $V_{G2} = 8$ **V**.

The use of the back-gate bias, instead of a grounded substrate, rises the peak mobility by about 10% in cases *(i)* and *(ii)*. It is again the case *(iii)* where the mobility gain is more pronounced (Figure A.6.(b)): 24% from 376 cm^2/Vs at $V_{G2} = 0$ V to 464 cm^2/Vs at $V_{G2} = 8$ V. Note the particular knot-like shape of this curve *(iii)*, which shows a sharp increase in mobility as the effective field decreases to the minimum value (~ 0.1 MV/cm).

The impact of the mobility enhancement is directly visible on the output current and transconductance: for a given gate bias, i.e. $V_{\mathrm{G1}} = 0.45$ V results $I_{\mathrm{D}} = 0.64$ μA and $g_{\mathrm{m}} = 6.26$ μS for $V_{\mathrm{G2}} = 0$ V, while for $V_{\mathrm{G2}} = 8$ V, the gain is significant ($I_{\mathrm{D}} = 1.09$ μA (+70%) and $g_{\mathrm{m}} = 10.60$ μS (+69%)) ultimately leading to improved circuit performance. Similarly, for a given overdrive voltage, i.e. $V_{\mathrm{G1}} - V_{\mathrm{th}} = 0.8$ V, it was measured $I_{\mathrm{D}} = 7.50$ μA and $g_{\mathrm{m}} = 7.81$ μS for $V_{\mathrm{G2}} = 0$ V, and for $V_{\mathrm{G2}} = 8$ V, $I_{\mathrm{D}} = 8.30$ μA (+9%) and $g_{\mathrm{m}} = 8.66$ μS (+11%). The difference between g_m and mobility gains is due to the shift of g_m peak with V_{G2}.

The bias map representation (combining V_{ret} and V_{TH} vs. V_{G2}) is general and allows the selection of the optimal bias condition for the mobility enhancement. The method can, in principle, be implemented for mobility gain in any FD-SOI MOSFETs but, it is best suited in planar ones with thin BOX and GP, where the back-gate voltage can be maintained in the practical 1–2 V range. Furthermore, the bias map can be enriched by adding the benefits of mobility gain and modified values of off-state leakage current and threshold voltage. The combination of these assets is realistic when GP bias is adjusted dynamically to provide high V_{T} and low leakage in off-state mode and to achieve low V_{TH}, high current and improved mobility in on-state mode.

A.5 Conclusions

This study introduced the concept of bias-engineered mobility which aims at operating the transistor in the region of minimum effective field. The return point of the effective electric field resulted in a convenient tool for the selection and understanding of the optimal bias conditions to enhance the mobility in FD-SOI MOSFETs by using back-gate bias. The combined representation of the threshold voltage and return point voltage indicates the bias range where the effective field decreases while the front-gate bias is increasing. In this bias window, the mobility is maximized. In fact, the experiments show a mobility gain of 70% in FD-SOI MOSFETs with 10 nm thick BOX and ground plane.

Bias-engineering of carrier mobility is a simple, pragmatic method which comes together with the V_{TH} tunning and can be combined with other types of mobility engineering based on strain, crystal-orientation or Si replacement.

Appendix B

Nanoelectronics Laboratory

B.1 Introduction

In this Appendix, the different equipments employed during the development of this work will be detailed. All the instruments are placed in the Nanoelectronics Laboratory at the CITIC-UGR building (Figure B.1).

Figure B.1. Photography of the front of the CITIC-UGR building.

B.1.1 Semiconductor device parameter analyzer

The *Agilent B1500A Analyzer* is an instrument (Figure B.2) used to carry out measurements on semiconductor based devices. For that, it provides four integrated Source Monitor/Measure Units (SMUs) which are able to generate and measure synchronously currents and voltages at the same time. It is possible, for example, to bias four-terminal SOI MOSFETs (source, drain, gate and substrate) as well as biasing the Pseudo-MOSFET samples (source, drain and gate/substrate, leaving one SMU open).

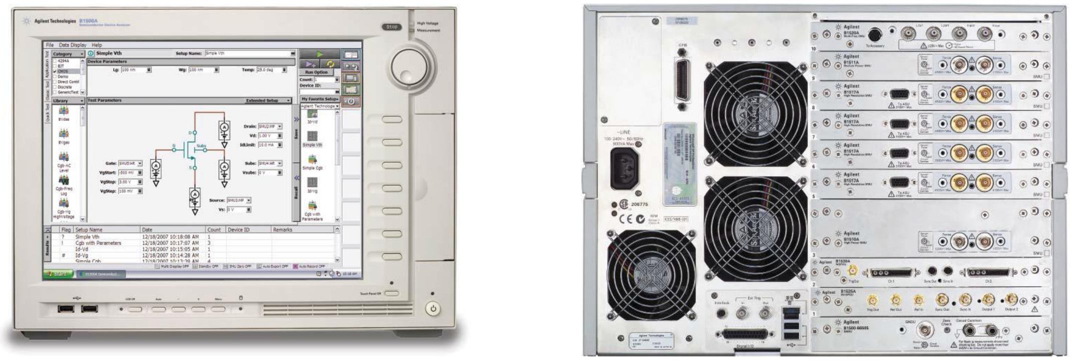
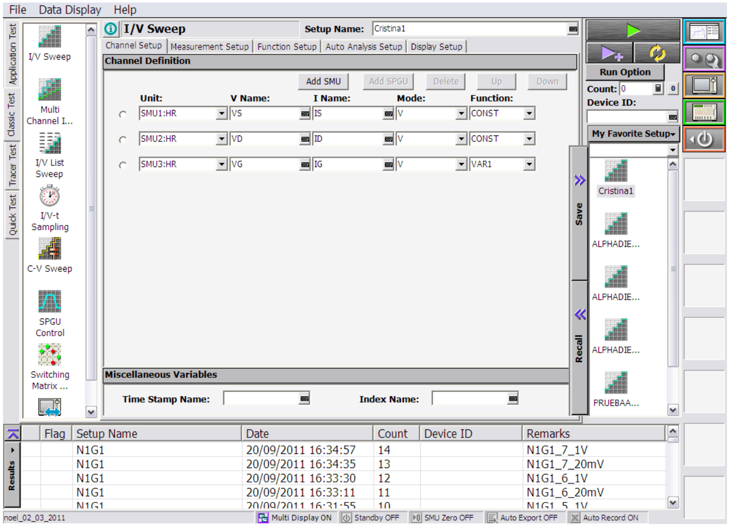


Figure B.2. Front and back view of the Agilent B1500A Semiconductor Analyzer.

Between the specifications, the maximum voltage and current values allowed stand out, which are 40 V and 1 A respectively, being the resolution of 0.5 μV and 0.1 fA in each case.

Respect to the software supported, the analyzer is based on the Windows O.S. It is provided with the EASYExpert program with several measurement setups for many of the most usual configurations: IV and CV sweeps, high speed IV samplings, pulse measurements...


File
Data Display
Help
Application Test
Classic Test
Tracer Test
Quick Test
I/V Sweep
Multi Channel I...
I/V List Sweep
I/V-t Sampling
C-V Sweep
SPGU Control
Switching Matrix ...
Channel Setup
Measurement Setup
Function Setup
Auto Analysis Setup
Display Setup
Channel Definition
Add SMU
Add SPGU
Delete
Up
Down
Miscellaneous Variables
Run Option
My Favorite Setup
Save
Recall
Results
Cristina1
ALPHADIE...
ALPHADIE...
ALPHADIE...
PRUEBAA...

I/V Sweep **Setup Name:** Cristina1

Unit:	V Name:	I Name:	Mode:	Function:
SMU1:HR	VS	IS	V	CONST
SMU2:HR	VD	ID	V	CONST
SMU3:HR	VG	IG	V	VAR1

Time Stamp Name:
Index Name:

Count: 0
Device ID:

Flag	Setup Name	Date	Count	Device ID	Remarks
	N1G1	20/09/2011 16:34:57	14		N1G1_7_1V
	N1G1	20/09/2011 16:34:35	13		N1G1_7_20mV
	N1G1	20/09/2011 16:33:30	12		N1G1_6_1V
	N1G1	20/09/2011 16:33:11	11		N1G1_6_20mV
	N1G1	20/09/2011 16:31:55	10		N1G1_5_1V

noel_02_03_2011 Multi Display ON Standby OFF SMU Zero OFF Auto Export OFF Auto Record ON

Figure B.3. EASYExpert software.

B.1.2 Parameter analyzer

The *Keithley 4200-SCS Analyzer* is a modular, fully integrated parameter analyzer (Figure B.4) that performs electrical characterization of materials and semiconductor devices. It allows to perform from I-V and C-V measurement sweeps or transient I-V measurements.

Through SMUs, which are configured by an intuitive software (Figure B.5), it can supply voltage or current and measure voltage or current from 0.1 fA to 1 A and from 1 μV to 210 V.

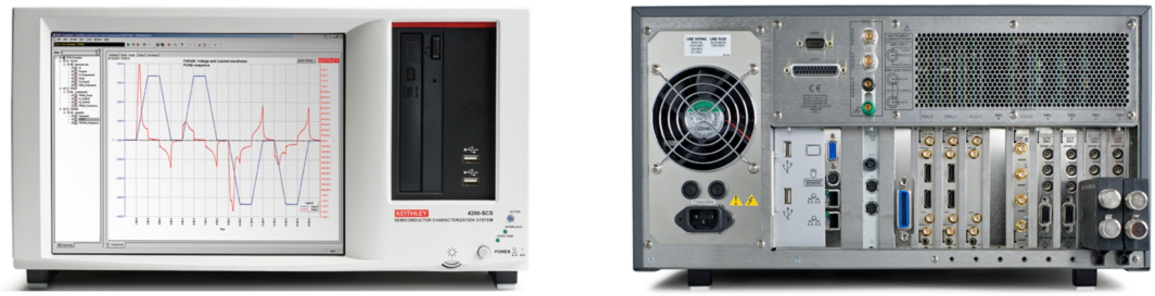
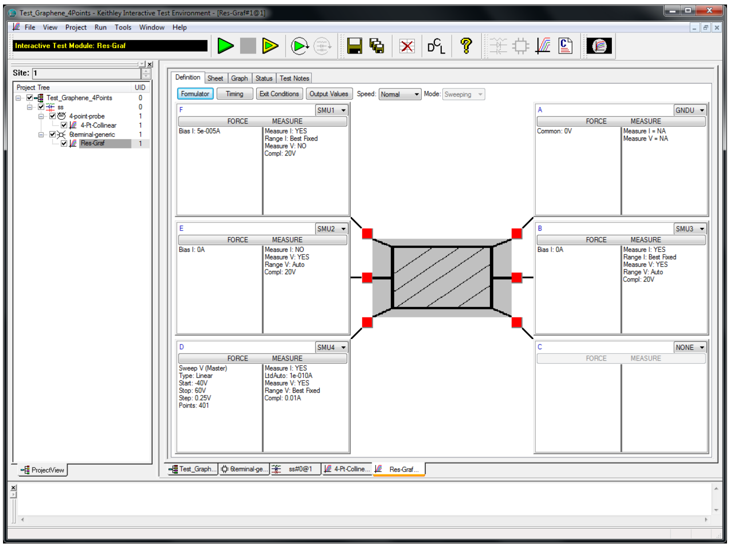


Figure B.4. Front and back view of the Keithley 4200-SCS Parameter Analyzer.


Test_Graphene_4Points - Keithley Interactive Test Environment - [Res-Graf#1@1]
File
View
Project
Run
Tools
Window
Help
Definition
Sheet
Graph
Status
Test Notes
Formulator
Timing
Exit Conditions
Output Values
ProjectView
Test_Graph...
6terminal-ge...
ss#0@1
4-Pt-Colline...
Res-Graf...

Interactive Test Module: Res-Graf

Site: 1

Project Tree — UID
Test_Graphene_4Points 0
ss 0
4-point-probe 1
4-Pt-Collinear 1
6terminal-generic 1
Res-Graf 1

Speed: Normal
Mode: Sweeping

F — SMU1
FORCE: Bias I: 5e-005A
MEASURE: Measure I: YES; Range I: Best Fixed; Measure V: NO; Compl: 20V

E — SMU2
FORCE: Bias I: 0A
MEASURE: Measure I: NO; Measure V: YES; Range V: Auto; Compl: 20V

D — SMU4
FORCE: Sweep V (Master); Type: Linear; Start: -40V; Stop: 60V; Step: 0.25V; Points: 401
MEASURE: Measure I: YES; LtdAuto: 1e-010A; Measure V: YES; Range V: Best Fixed; Compl: 0.01A

A — GNDU
FORCE: Common: 0V
MEASURE: Measure I = NA; Measure V = NA

B — SMU3
FORCE: Bias I: 0A
MEASURE: Measure I: YES; Range I: Best Fixed; Measure V: YES; Range V: Auto; Compl: 20V

C — NONE
FORCE
MEASURE

Figure B.5. Keithley interactive test environment.

B.1.3 Triaxial cables

The SMUs have *triaxial outputs* rather than the usual BNC (Figure B.6) because they enable to get very low current ranges, at the level of fA ($\approx 10^{-15}$A) [Tec13].

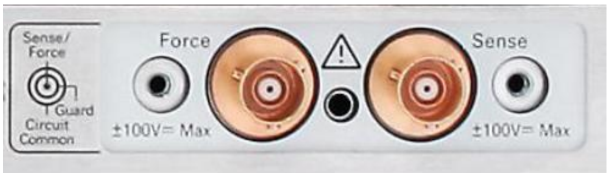

Sense/
Force
Guard
Circuit
Common
Force
±100V= Max
Sense
±100V= Max

Figure B.6. SMU plug-in module from B1500A equipment.

The triaxial cable connected to the SMU output has three internal conductors (Figure B.7). The *Driven Guard* has the same voltage than the *Force/Sense Line* so the leakage current is reduced to fA levels. Then, the noise is almost eliminated achieving measurements of very low current. Finally, the external conductor serves to protect the others and it is usually connected to ground (the reference potential).

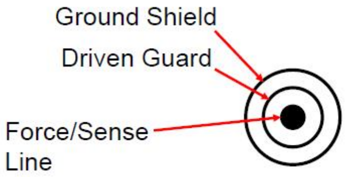


Figure B.7. Conductors inside a triaxial cable.

B.1.4 Impedance analyzer

The *Agilent Impedance Analyzer 4294A* (Figure B.8) is able to measure a wide range of impedance values with high precision. It works with frequencies from 40 Hz to 110 MHz and with amplitudes of the AC signal from 5 mV to 1 V. Regarding DC voltage it can reach until ±40 V.

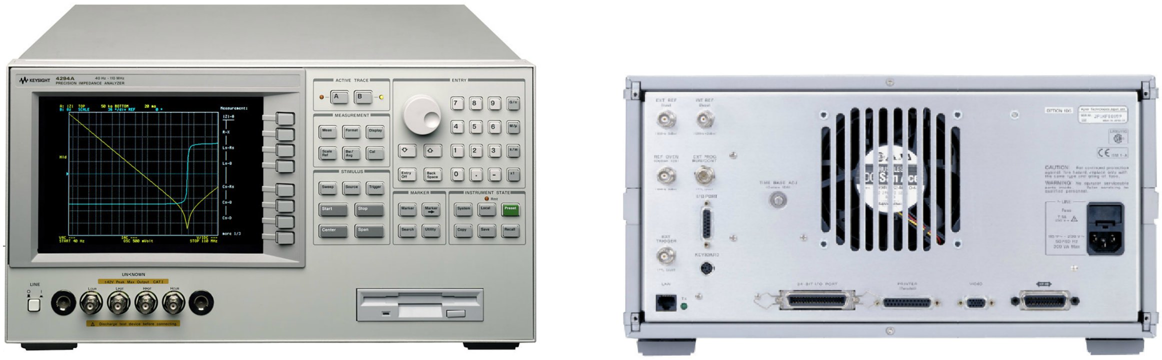


Figure B.8. Front and back view of the Impedance Analyzer 4294A.

The *Agilent Extension cable 16048G* (Figure B.9) is used to connect the analyzer to the probe station. This module is placed to the frontal part through four BNC outputs (Lc, Lp, Hc, Hp) and holds other four coaxial cables to be linked with the Pseudo-MOS station.

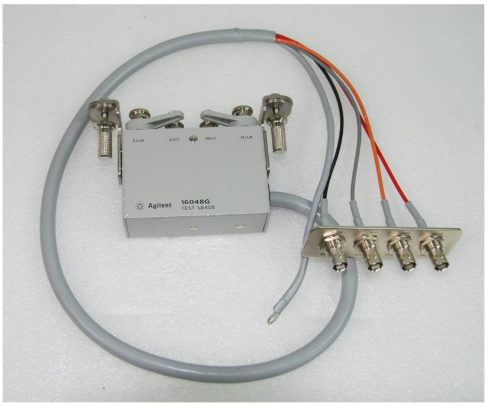


Figure B.9. Agilent extension cable 16048G.

B.1.5 JANDEL universal probe station

The point-contact Ψ-MOSFET measurement equipment is based on an standard *JANDEL universal probe station* employed for electrical testing (Figure B.10). Basically, it is formed by a conductive chuck where SOI samples are placed. Through this platform, a bias is applied at the bottom of the wafer.

The station has also four tungsten carbide probes whose pressure is indicated in terms of equivalent weight and it can be modified manually by integrated dynamometers from 0 g to 100 g. The separation between two consecutive needles is 1.59 mm and the tip radius is 25 μm. The bias of each part of the system was controlled externally by the B1500A analyzer through the SMUs cables (see Figure2.2 in Section 2.1.2).

In this station the number of probes needed in a measurement can be modified by the user as convenience. Because of that, it is possible to compare directly four-point measurements with two-point (Pseudo-MOSFET) characteristics (Section 4.3) simply keeping lifted some of the needles.

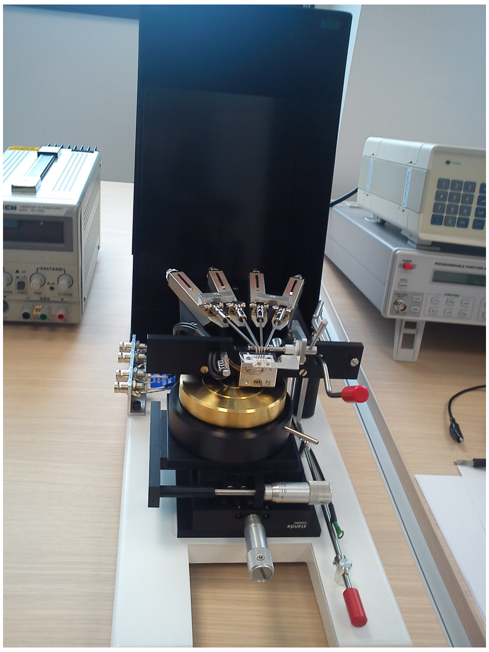


Figure B.10. Jandel point-contact system where Pseudo-MOSFET technique is carried out.

It is worth mentioning that, before performing the measurements, the system was cleaned by a compressed air supply to remove any particles of dust from the surface. User-level precautions were also taken into account for achieving the best accuracy in the measurements, so the manipulation of the equipment always was done with a pair of globes and a mask on.

B.1.6 Janis probe station

The *Janis ST-500-2 probe station* aims the non-destructive electrical testing in an extended temperature range. It provides a vacuum measurement setup although, in this work, it has not

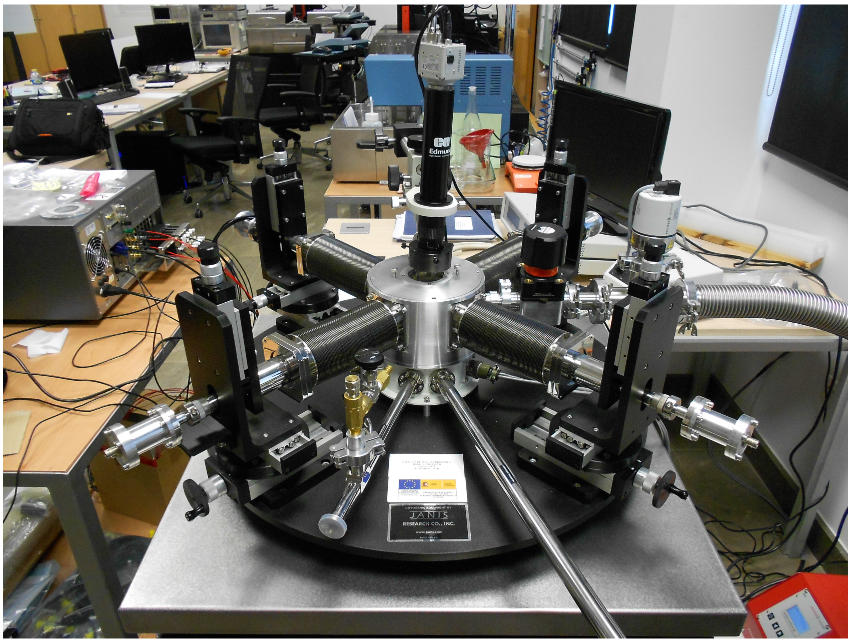


Figure B.11. Janis micro-manipulated probe station.

been required, being the use of this station limited to extract I-V characteristics through four SMUs available.

The main reason for using the Jandel or the Janis station in this work is found in their physical features. On one hand, the Jandel equipment allows a well-control of the needle pressure (from 5 g to 100 g) but the distances achieved between the probes are limited to certain values (1.59 mm, 3.18 mm, 4.77 mm). On the other hand, the Janis station offers the possibility to move the probes in a wide variety of separations (in terms of microns).

Finally, Janis station provides a low vibration level and the temperature can be modified from ≈ 3.5 K to 475 K with the help of a temperature controller; it is possible to carry out electrical measurements from DC to 67 GHz, and the radius of the tungsten tips is 25 μm.

B.1.7 BNC-Triaxial adapters

As the probe stations has BNC outputs (for the needles and the chuck), *adapters* are required to connect them to the triaxial cables. Figure B.12 exemplifies one of the adapters used, whose extremes are male BNC and female triaxial, and how the internal connection is done.

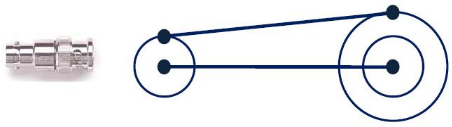


Figure B.12. BNC-triaxial adapter.

B.1.7.1 Pseudo-MOSFET samples

During the development of this work different Pseudo-MOSFET samples have been employed. The following tables describe the dimensions of each wafer available at the laboratory including those used in this thesis and Figure B.13 illustrates one of them.

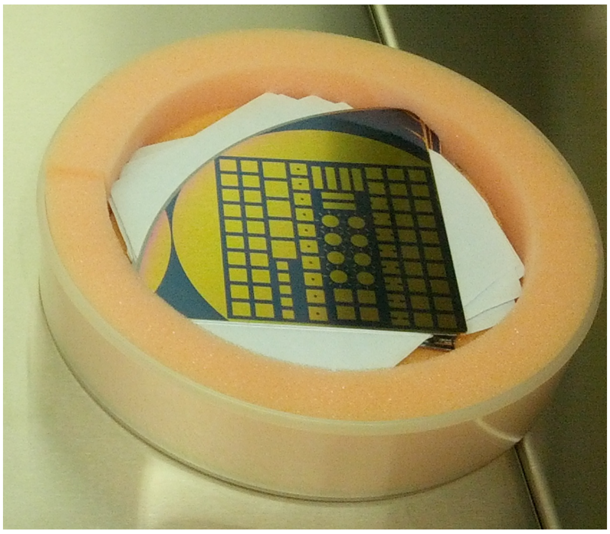


Figure B.13. One of the Pseudo-MOSFET samples available in the nanoelectronics laboratory.

Sample name	t_{Si}**(nm)**	t_{BOX} **(nm)**	t_{Ox_Sup} **(nm)**
1-A	17.3	146.9	21.1
1-B	43.1	144.6	21.1
1-C	17.4	146.7	21.1
1-D	43.1	144.6	21.1
2-A	22.6	146.8	6.3
2-B	48.7	144.5	6.3
2-C	22.6	146.6	6.3
2-D	48.3	144.4	6.3

Table B.1. Specifications of the Silicon wafers from the batch RUN 6493-GRA fabricated by CNM.

B.1.8 Semi-automatic probe system

The semi-automatic probe system used during the work, mentioned in Appendix A, was the *Suss Microtec PA300 PS-MA* [Cas12] (Figure B.14). It permits the measurements for pine-pitch probing of pads down to 30 μm × 30 μm.

Sample name	t_{Si}**(nm)**	t_{BOX} **(nm)**	**Surface**
MU001	88	145	Non-passivated
MU002	88	145	Non-passivated
MU003	12	145	Non-passivated
MU004	88	145	Passivated (4 nm)
MU005	12	145	Passivated (4 nm)
MU006	83	25	Non-passivated
MU007	83	25	Passivated (4 nm)
MU008	83	25	Passivated (4 nm)
MU009	83	25	Non-passivated
MU0010	12	145	Passivated (4 nm)
MU0011	12	145	Non-passivated
MU0012	88	145	Passivated (4 nm)

Table B.2. Specifications of the Silicon wafers available in the laboratory fabricated by SOITEC company.

Sample name	t_{Si}**(nm)**	t_{BOX} **(nm)**	t_{Ox_Sup} **(nm)**
1	15	145.3	20
2	22	145.3	6
3	40	145.3	20
4	47	145.3	6

Table B.3. Specifications of the Poly-Si wafers from the batch 6383-GRA fabricated by CNM.

This probe system employs the *ProbeShield technology*, enabling accurate low-noise measurements of atto-amperes and femto-farads. It is also prepared to make studies in a the temperature range from -60 °C to +300 °C.

Finally, it enables the automatic measurements of a specified pattern along all the wafer. To do so, a previous calibration (to take into account non-idealities in the surface of the wafer measuring its deviation) and adjustment is required (the initial contact is performed manually).

B.1.9 Microscope

The *Industrial Microscope ECLIPSE LV150N* provided by Nikon is an optical-digital microscope (Figure B.15) mainly used in the lab to visualize the sample surface, to check the quality of the layers, or to determine the possible causes of unexpected behavior.

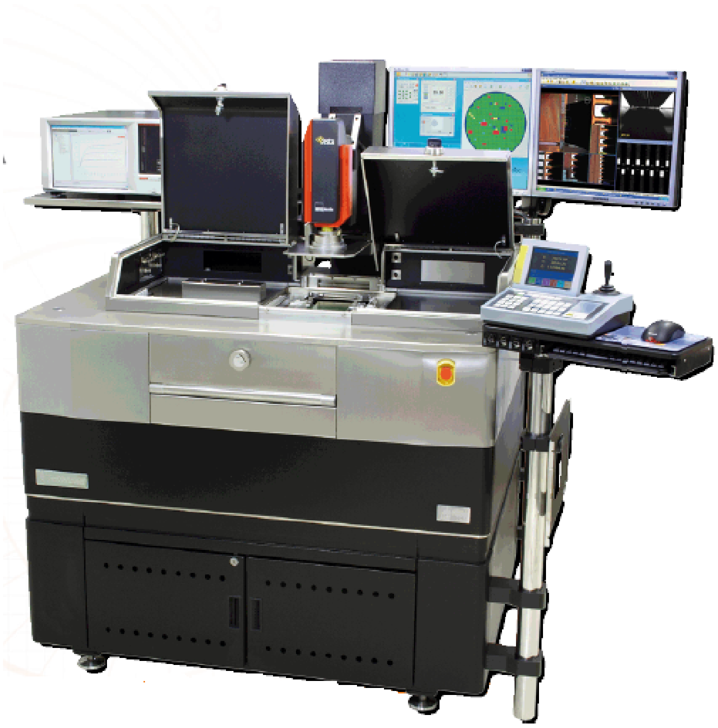


Figure B.14. Semi-automatic probe system by Suss Microtec. This equipment provides a perfect environment for an accurate wafer current and capacitance low-noise measurements.

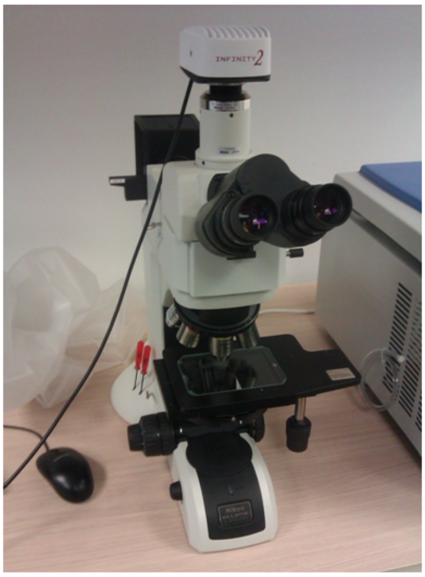


Figure B.15. Nikon Microscope ECLIPSE LV150N.

Some of the remarkable features of this instrument are that it is possible to select dark field, bright field, polarization and LED illumination. Moreover, it disposes of several objectives ($5\times$, $10\times$, $20\times$, $50\times$, $100\times$) to increase the magnification of the images.

Appendix C

Fabrication Process of Pseudo-MOSFET Samples

C.1 Description of the procedure

During the development of this work, one-month stay at L'Institut de Microelectronique Electromagnetisme et Photonique et le Laboratoire d'Hyperfrequences et de Caracterisation (IMEP-LAHC) in Grenoble (France) was done. The objective was to learn how the different square cells of a Pseudo-MOSFET sample were fabricated. So, taking a SOI substrate as a starting point, the steps followed in the process will be described here and are summarized in Figure C.1:

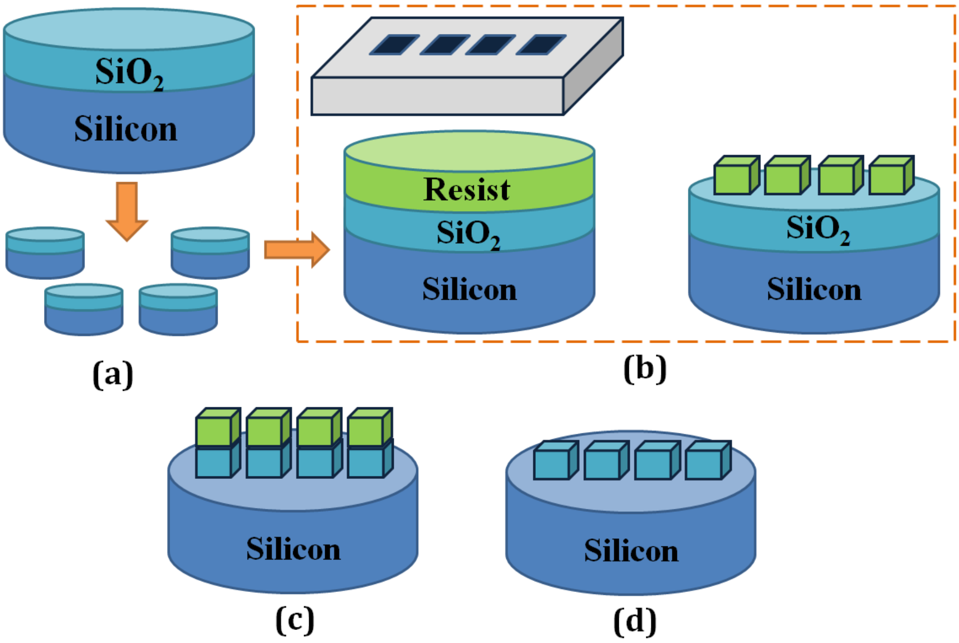


Figure C.1. Schematic of the different processes carried out at the IMEP-LAHC centre to made the cells which form the Pseudo-MOSFET samples: (a) cut the bare SOI wafer in smaller samples; (b) perform a photolithography on each sample; (c) make a RIE etching, and (d) final chemical clean of the sample.

(a) Cut the wafer into samples

(b) Perform a photolithography step

(c) Carry out a RIE etching of Silicon Dioxide

(d) Remove of the residual resin

C.1.1 Step 1. Cut the wafer into samples

As the initial dimensions of the SOI wafer are too big, it was not possible to insert the samples in the lithography equipment. Thus, a previous cut process was required. For that, the *Disco DAD 321 Automatic Dicer* was utilized (Figure C.2).

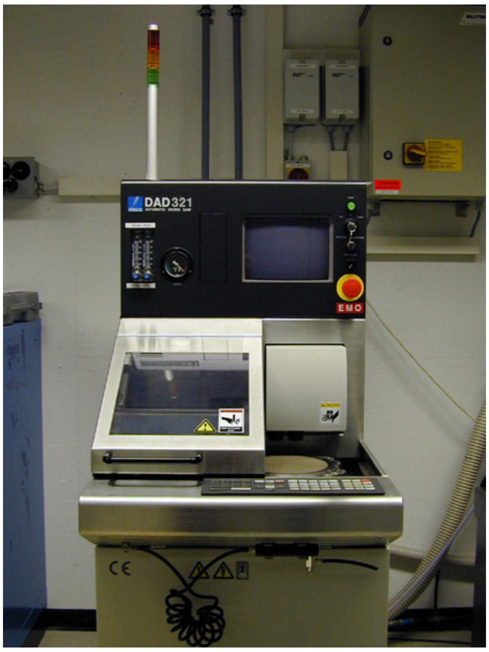


Figure C.2. Dicing saw (Disco DAD 321 machine) used to cut the substrate in smaller samples.

The machine contains a blade which was able to cut Silicon and similar substrates. Between its specifications it is found that [Nan10]:

- The chuck can support 6-inches wafer (approximately 150 mm for full size) and anything smaller than that.
- The substrates can be bare, with thin films or without, patterned or etched.
- If there is a delicate device on the substrate, thin layer of photoresist can be used for protection.

The wafer was then placed on the chuck and, after turning on the substrate vacuum, the plate was load inside the machine. The different cuts followed to obtain the samples are illustrated in Figure C.3.

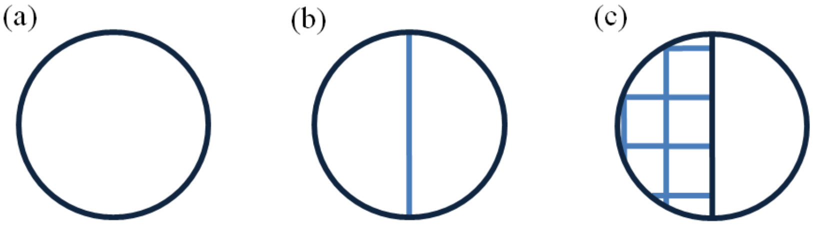


Figure C.3. The whole SOI wafer was cut into small samples in several steps. (a)-(c) shows the sequence followed.

C.1.2 Step 2. Photolithography

The *photolithography* is the process of transferring patterns of geometric shapes on a mask to a thin layer of photosensitive material (called *photoresist*) covering the surface of a semiconductor wafer [MS04]. These patterns will define the different islands of the Pseudo-MOSFET samples.

1. The wafer was placed on a vacuum spindle (Figure C.4) inside a clean room to carry out the deposition of the photoresist. In order to ensure satisfactory the adhesion of this resist, firstly the top oxide was altered by a deposition of an adhesion *promoter* through a Pasteur pipette. In particular, the sample was rapidly accelerated for about 30 seconds.

Figure C.4. The sample was placed in a vacuum spindle to carry out the application of the resist.

2. After the application of this adhesion layer, a certain amount of resist was applied to the center of the sample by another pipette and again it was accelerated.
3. Later, the wafer was *soft baked* to remove the solvent from the photoresist film as well as to increase the adhesion of the resit to the wafer. Specifically, the samples were put on the surface of a *VWR Digital Dry Block heater* (Figure C.5) at 90 °C for 90 seconds.
4. One by one, each sample was introduced in a *Mask aligner Suss Microtec-type MA6* where the resist was exposed to UV light (Figure C.1.(a)). The type of photolithography applied

Figure C.5. The sample was placed in a vacuum spindle to carry out the application of the resist.

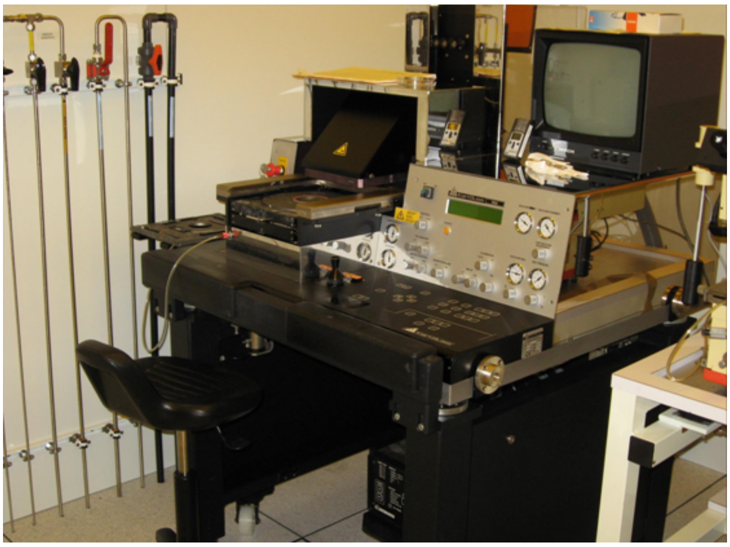


Figure C.6. Each sample was introduced into an optical lithographic system.

in this process was *positive* [MS04]: the resist exposed to the UV light changes its chemical structure by absorbing radiation what makes it more soluble in a solution called *developer*. The exposed resist is then removed (Figure C.1.(b)) by immersion of the sample into a beaker with this developer (Figure C.7).

Figure C.7. If a positive photoresist is used, the exposed resist is dissolved in the developer.

5. Then, the sample is cleaned with deionized water and dried with a diffusor.
6. To conclude this step, the sample is again *post baked* on the *VWR Digital Dry Block heater* to increase the adhesion of the resist to the substrate. In this case was heated at 110 °C for 5 minutes.

C.1.3 Step 3. Reactive-Ion Etching (RIE) of Silicon Dioxide

The next stage was completely carried out by a *Corial 200IL ICP Dry Etcher* (Figure C.8) and it consisted of the etching of the oxide present on the top surface following the patterns previously *drawn* on the photoresist (Figure).

In short, each sample was put in an ambient that etches the exposed insulating layer but does not attack the resist.

C.1.4 Step 4. Removal of the residual resin

Finally, the residual resist is stripped by immersion into a *remover* dissolution during a few minutes. Later, the samples were extracted, cleaned with deionized water and dried with a diffusor.

C.2 Characterization of the samples achieved

Sixteen was the number of the Pseudo-MOSFET samples fabricated during the process explained before (Figure C.9) with 55nm-thick Si film, 145-nm thick BOX and non-passivated

LEM
CORiAL
200IL

Figure C.8. The inductively coupled plasma etcher employed during the fabrication process.

surface. Some of them were characterized subsequently in order to check that the procedure was successful. The results are included in the following subsections.

The specifications of the two-needle setup configuration are summarized in Table C.1:

I-V curves	**C-V curves**
-20 V $< V_G <$ +20 V	-20 V $< V_G <$ +20 V
$V_D = 20$ mV	$V_{osc} = 20$ mV
$V_S = 0$ V	Cs-Rs model
	Frequency 1 kHz
	$t_{delay} = t_{hold} = 100$ ms

Table C.1. Specifications of the setup parameters.

C.2.1 I-V characteristics as a function of the probe diameter

Current curves were performed in one determined cell for three different probe diameter (25 μm, 40 μm and 100 μm) when the pressure of the needles was modified to 50 g to 100 g (Figure C.10).

It was observed that the best results were obtained for the needles with less diameter, i.e. 25 μm. It worths saying that the optimum probe pressure was also calculated from these curves after representing the peak of the transconductace (derivative of I-V curves). Then, 85 g was obtained as limit for 25 μm and, approximately, 90 g for 40 μm and 100 μm.

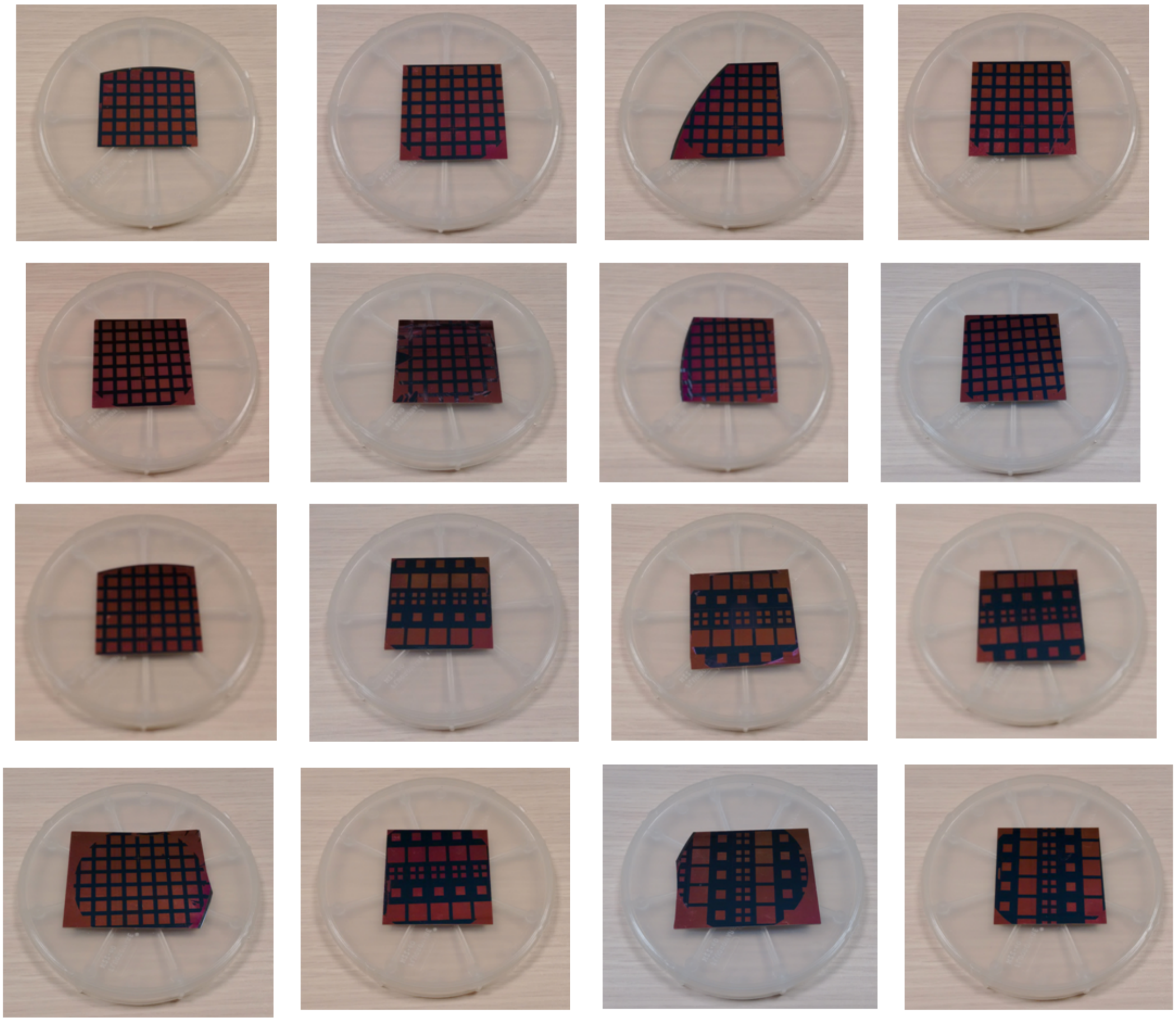


Figure C.9. Pseudo-MOSFET samples fabricated at IMEP-LAHC during the one-month stay.

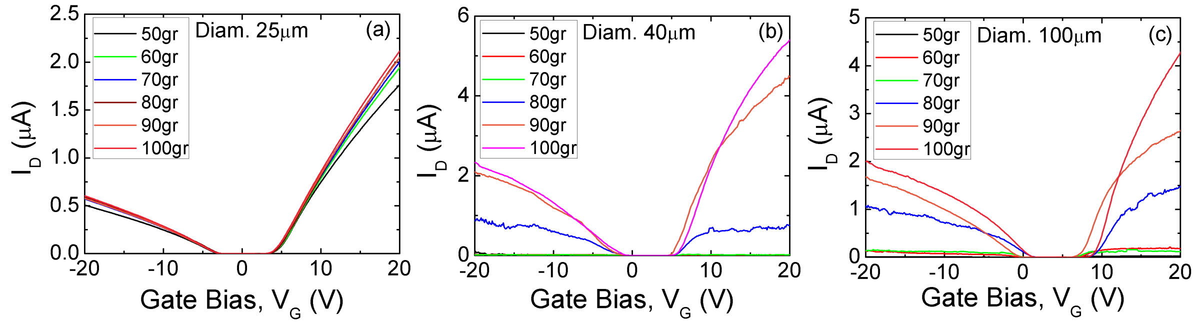


Figure C.10. Current characteristics extracted as a function of the probe pressure for needles with (a) 25 μm, (b) 40 μm and (c) 100 μm of diameter.

C.2.2 Successive measurements on the same cell

The objective of this experiment was to examine how sensitive was the point-contact system to the threshold voltage variability for successive measurements. So, twenty consecutive I-V characteristics were performed on the same cell of a sample using the optimum probe pressure and moving the chuck as little as possible between measurements (needles were lifted and applied successively). The methodology was similar to that explained in Section 2.3.4.

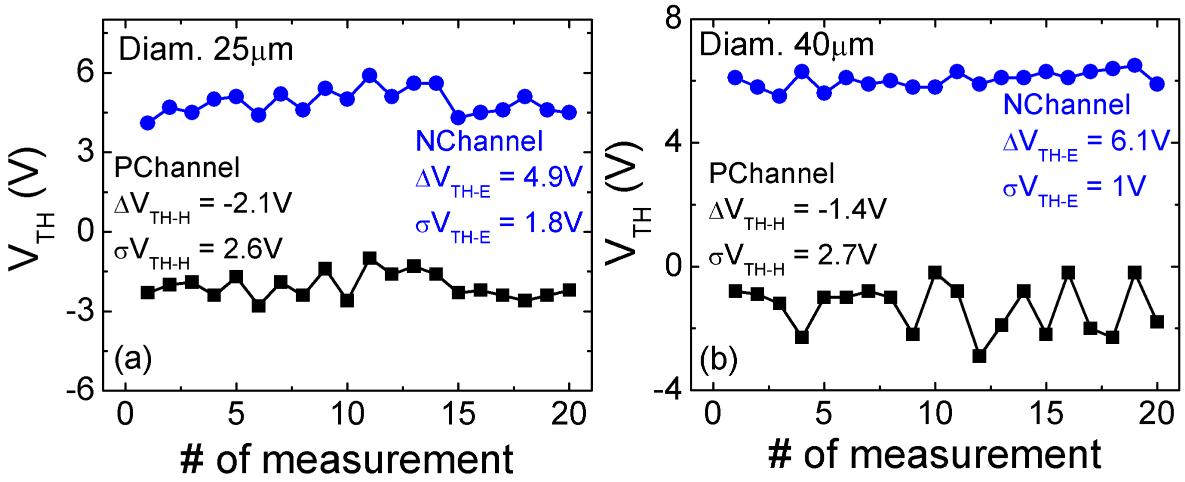


Figure C.11. Threshold voltages extracted from twenty current characteristics performed on the same cell for needles with (a) 25 μm and (b) 40 μm of diameter.

It was observed that, for both probe diameters, the results for V_{TH-H} (hole channel) present a higher variation than V_{TH-E} values (electron channel). In addition, 40μm-diameter probes achieved worse results in terms of variability.

C.2.3 I-V measurements with different probe inter-distances

Using 25μm-diameter probes, five I-V curves were performed varying the distance between the needles (1.59 mm, 3.18 mm, 4.77 mm).

The results verified those values extracted in Section 2.3.2: border effects are intensified as the point contacts move closer to the edges what causes a reduction of the current I_D.

C.2.4 C-V Measurements with different probe inter-distances

A similar methodology explained before was carried out but performing C-V characteristics instead, and taking just one measurement.

Again, the data satisfied the results described in Section 3.2.3: as the distance between needles increases, so does the capacitance as a consequence of that the effective areas induced in the needles are both less overlapped.

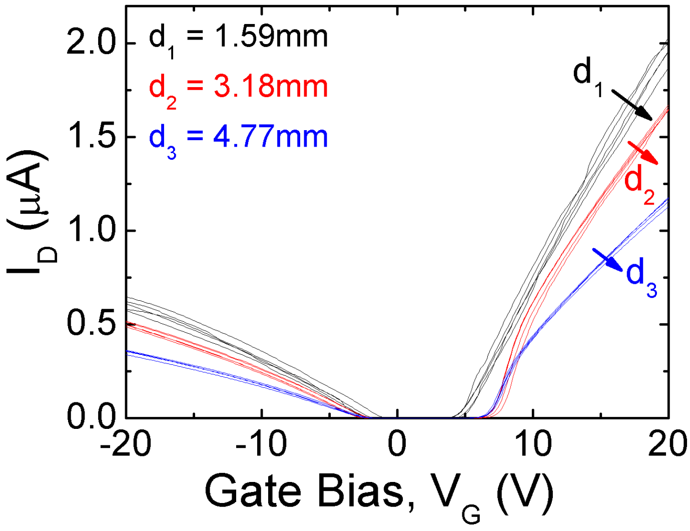


Figure C.12. Five I-V characteristics were obtained for three different separation between the needles. $d_1 = 1.59$ mm (black lines), $d_2 = 3.18$ mm (red lines), and $d_3 = 4.77$ mm (blue lines).

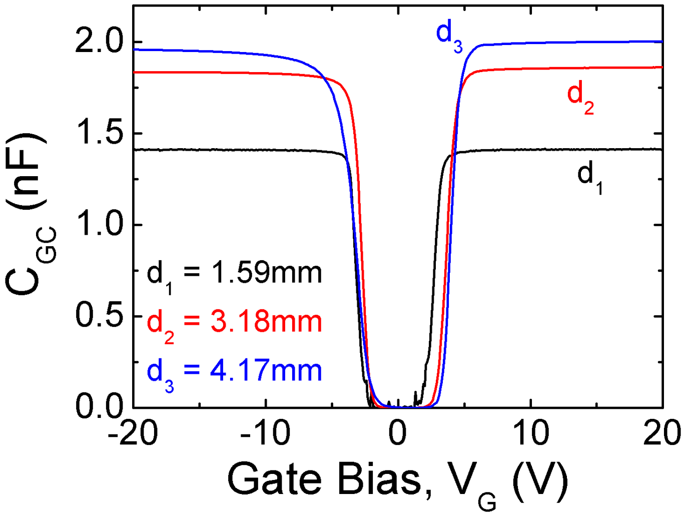


Figure C.13. C-V characteristics were obtained for three different separation between the needles. $d_1 = 1.59$ mm (black lines), $d_2 = 3.18$ mm (red lines), and $d_3 = 4.77$ mm (blue lines).

C.2.5 Obtaining of the carrier mobility

Finally, the carrier mobility when an electron channel is induced in the structure, μ_{eff} , was calculated using two different configuration: two-point and four-point contact setup. The process followed was the same explained in Section 4.3, employing the mobility equations given by:

$$\mu_{eff} = \frac{I_{14} S_{eff}}{f_{g4p} V_{23} Q_{acc-inv}} \tag{C.1}$$

if four needles are placed on the surface (Figure 4.1.(a)), or:

$$\mu_{eff} = \frac{I_D S_{eff}}{f_{g2p} V_D Q_{acc-inv}} \tag{C.2}$$

if only two probes are used (Pseudo-MOSFET configuration, Figure 4.1.(b)). Nevertheless, in order to simplify the experiment, here the geometric factor was taken as 0.75 [KBS+05] when two needles were employed, and 4.53 [Sch06] for four-point case. Thus, the final mobility data are represented in Figure C.14:

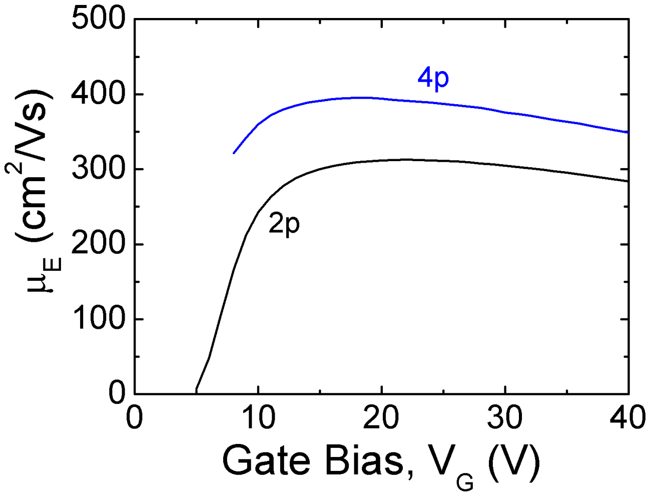


Figure C.14. Carrier mobility curves as a function of the gate bias for a two-needle (black line) and four-needle (blue line) configurations.

It is observed that, when four point contacts are used, a peak value of 395 cm^2/Vs is achieve for the mobility, almost a quarter larger than the result achieved with two probes, 311 cm^2/Vs. These outcomes agree with those extracted in Chapter 4 where it was deduced that an incomplete determination of the geometrical factor f_{g2p} yields to a wrong estimation of the carrier mobility.

Appendix D

List of publications

Journal Papers

A. Diab, **C. Fernandez**, A. Ohata, N. Rodriguez, I. Ionica, Y. H. Bae, F. Allibert, F. Gamiz, G. Ghibaudo, C. Mazuré, S. Cristoloveanu, "A new characterization technique for SOI wafers: Split C(V) in pseudo-MOSFET configuration", *Solid-State Electronics*,90, pp. 127:133, 2013.

C. Fernandez, N. Rodriguez, A. Ohata, F. Gamiz, F. Andrieu, C. Fenouillet-Beranger, O. Faynot, S. Cristoloveanu, "Bias-Engineered Mobility in Advanced FD-SOI MOSFETs", *Electron Device Letters*, 34(7), pp. 840:842, 2013.

C. Fernandez, N. Rodriguez, A. Ohata, F. Gamiz, S. Cristoloveanu, "Effective Capacitance Area for Pseudo-MOSFET Characterization of Bare SOI Wafers by Split-C(V) Measurements", *ECS Journal of Solid State Science and Technology*, 53(5), pp. 209-217, 2013.

C. Marquez, N. Rodriguez, **C. Fernandez**, A. Ohata, F. Gamiz, F. Allibert, S. Cristoloveanu, "In Situ Characterization of Bias Instability in Bare SOI Wafers by Pseudo-MOSFET Technique", IEEE Transaction on Electron Devices, 14(3), pp. 878:883, 2014.

C. Fernandez, N. Rodriguez, C. Marquez, A. Ohata, F. Allibert, "On the effective mobility extraction by point-contact techniques on silicon-on-insulator substrates", *Journal of Applied Physics*, 117, 035707, 2015.

Conference Contributions

A. Diab, **C.Fernandez**, A. Ohata, N. Rodriguez, I. Ionica, Y. H. Bae, W. Van Den Daele, F. Allibert, F. Gamiz, G. Ghibaudo, S. Cristoloveanu, "A New Characterization Technique for SOI Wafers: Split C(V) in Pseudo-MOSFET Configuration", *EUROSOI Conference* (La Grande Motte, Montpellier, France, 2012), pp. 127:133.

C. Fernandez, A. Diab, N. Rodriguez, A. Ohata, F. Allibert, I. Ionica, F. Gamiz, S. Cristoloveanu, "Impact of Effective Capacitance Area on the Characterization of SOI Wafers by Split-C(V) in Pseudo-MOSFET Configuration", *International Semiconductor Conference Dresden-Grenoble (ISCDG) Conference* (Grenoble, France, 2012), pp. 123:126.

A. Diab, **C.Fernandez**, L. Pirro, N. Rodriguez, I. Ionica, A. Ohata, Y. H. Bae, W. Van Den Daele, F. Allibert, F. Gamiz, G. Ghibaudo, D. Delprat, C. Mazuré, S. Cristoloveanu, "Effective Mobility in Extra-Thin Film and Ultra-Thin BOX SOI Wafers", *EUROSOI Conference* (Paris, France, 2013), pp. 2:4.

C. Fernandez, N. Rodriguez, A. Ohata, A. Diab, F. Gamiz, S. Cristoloveanu, "Determination of Effective Capacitance Area for Pseudo-Transistor based Characterization of bare SOI wafers by Split-C(V) measurements", *223rd ECS Meeting*, (Toronto, Canada, 2013), 53, pp. 209:217.

C. Fernandez, N. Rodriguez, C. Márquez, B. Biel, F. Gamiz, "Two Point-Contact Method for the Electrical Characterization of Graphene-On-Insulator Samples", *ImagineNano* (Bilbao, España, 2013).

C. Fernandez, N. Rodriguez, F. Gamiz, "Substrate effect on Pseudo-MOSFETs capacitance curves", *I Congreso Nacional Multidisciplinar de Jóvenes Investigadores* (Granada, España, 2014), pp. 21:25.

L. Segura, N. Rodriguez, **C. Fernandez**, A. Ohata, C. Márquez, F. Gamiz, "Direct Electrical Characterization of Graphene-On-Insulator by Multiple-Point Contact Configuration", *Graphene International Conference and Exhibition* (Toulouse, France, 2014).

C. Fernandez, N. Rodriguez, C. Marquez, F. Gamiz, "Determination of ad hoc deposited charge on bare SOI wafers", *Joint International EOROSOI Workshop and International Conference Ultimate Integration on Silicon (EUROSOI-ULIS)* (Bolonia, Italia, 2015), pp. 289:292.

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