An analytical model for the inversion charge distribution in square GAA MOSFETs with rounded corners

Trabajo Investigación Tutelada
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por

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Foreword

In this work we introduce an analytical model for square Gate All Around (GAA) MOSFETs with rounded corners including quantum effects. With the model developed it is possible to provide an analytical description of the 2D inversion charge distribution function (ICDF) in devices of different sizes and for all the operational regimes. The accuracy of the model is verified by comparing with data obtained by means of a 2D numerical simulator that self-consistently solves the Poisson and Schrödinger equations. The expressions presented here are useful to achieve a good description of the physics of these transistors; in particular, of the quantization effects on the inversion charge. The analytical ICDF obtained is used to calculate important parameters from the device compact modeling viewpoint, such as the inversion charge centroid and the gate-to-channel capacitance, which are modeled for different device geometries and biases.

Chapter 1

Introduction

Multiple-gate (MuG) MOSFETs are considered a serious alternative for keeping up with the continuous reduction in device dimensions described by Moore's law. These structures show promising possibilities in relation to the control of short channel effects (SCEs) and the achievement of ideal subthreshold swing values [1, 2, 3].

Making use of technologies based on these new geometries, channel lengths could be shrunk below 20nm accordingly to the latest edition of ITRS [1]. In this respect, their capacity to reduce SCEs and the possibility of using undoped channels are essential features for the achievement of this goal. The latter, in particular, is critical since random impurity effects are by no means negligible in nanometric devices [4, 5]. These effects produce a dispersion of fundamental parameters such as the threshold voltage and the sub-threshold slope [4, 5, 6, 7]. Moreover, MuG MOSFETs are part of the Silicon-On-Insulator (SOI) transistor family, which demonstrates unique features that look promising for future mainstream CMOS technologies [3, 6, 7]. The use of ultra-thin-body (UTB) and MuG SOI structures allows the fabrication of fully-depleted devices that offer not only extremely good control of SCEs but also a very good behavior with respect to drain-induced barrier-height lowering (DIBL), threshold voltage roll-off, and off-state leakage [3, 6, 7].

Both square and cylindrical Gate-All-Around (GAA) MOSFETs are currently under intense study from the simulation and modeling viewpoint [3, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17]. One key area in these structures is the study of quantum mechanical effects (QMEs), since both structural and electrical confinement (produced by a square gate in the quadruple-gate device and by a circular gate in the cylindrical one) make these devices (nanowires FETs) quasi-1D transistors, where transport occurs in a set of loosely coupled propagating modes.

In this work we focus on square GAA MOSFETs. These devices have not been subject of many modelling efforts due to their particular geometrical complexities. The concentration of inversion charge close to the corners of the silicon body makes a bi-dimensional

description of the inversion charge distribution and other important magnitudes imperative from the compact modeling viewpoint. The analytical description of cylindrical GAA MOSFETs is simpler since the symmetry of the structure around the rotation angle allows a 1D description, accounting for just the radial component [11, 13, 10, 16]. In the case of square GAA MOSFETs, other modeling strategies are necessary, moreover if we take into account that real life devices are not perfectly square. When a square GAA device is manufactured, the result is usually a rounded corner square shaped structure, as can be seen in figure 1.1. Because of the manufacture process, the materials suffer from chemical attacks which lead to the aforementioned shape. This effect, althought undesired, is unevitable because of the collateral effects caused by the current technology. For a better understanding of the manufacture of this GAA devices see [18].

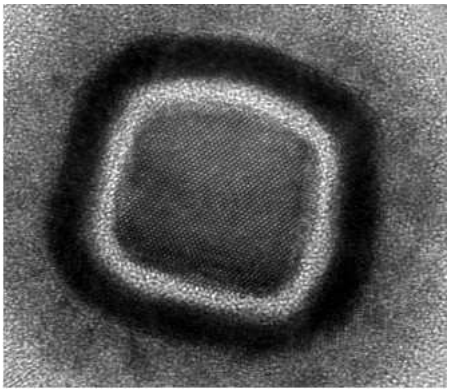
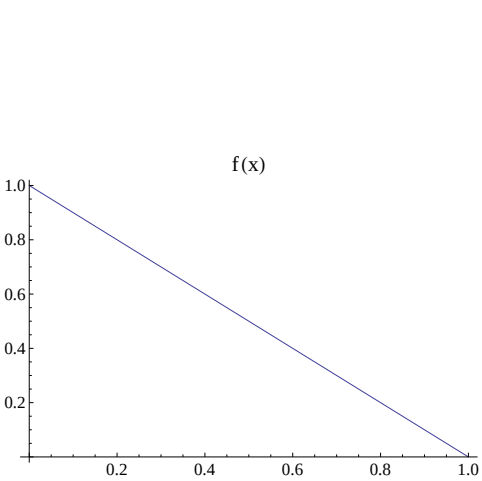


FIGURE 1.1: Cross sectional TEM image of 3D-stacked square NW with HfO_2/TiN and W/H=15nm/15nm (reference [19]).

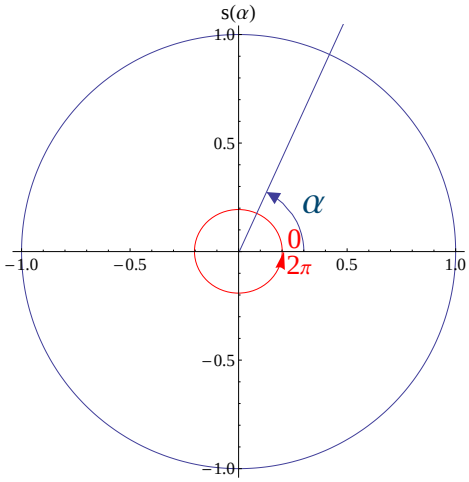
In order to develop an inversion charge analitycal model for this device, first of all, we introduce a 1D analytical function $f(x)$ that accurately reproduces the inversion charge distribution function (ICDF) from the center silicon core to the device side, for different device sizes and applied gate voltages. Secondly, we define a parametric function $s(\alpha)$ (with α being the rotation angle as shown in 1.2(b)). This function defines the external shape of the device to model. By combining $f(x)$ and $s(\alpha)$ we are able to model a 2D function $f(x, \alpha)$ that reproduces the ICDF in the active region of the structure as shown in figure 1.2. As it will be shown below, we will make use of a numerical simulator to accurately characterize $f(x, \alpha)$.

The resulting ICDF is related to the inversion charge density as follows, $n(x, \alpha) = N_{\text{inv}} \mid f(x, \alpha) \mid^2$, N_{inv} (cm^{-1}) being the value of the total electron density integrated over the square area of the silicon channel. Once we have the ICDF function, we will be able to model the inversion charge centroid (ICC) and the gate-to-channel capacitance (C_{GC}), making use of this analytical function.

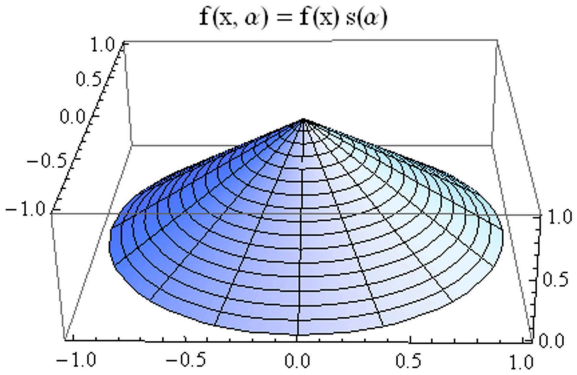
The paper is organized as follows: in chapter 2 we describe the main features of the simulator used. We deal with the ICDF modeling in chapter 3. The definition, calculation



(a) $f(x) = -x+1$ used as an example of 1D model.



(b) Example of a parametric representation of the shape of the device for a cylindrical GAA: $s(\alpha) = 1$.



(c) $f(x, \alpha) = f(x)s(\alpha)$ is a combination of both functions and returns the parametric 2D model of the ICDF.

FIGURE 1.2: Example of the combination of the 1D model function with a parametric representation of the external shape of the device, resulting in a 2D representation of the ICDF.

and modeling of the ICC and the C_{GC} are presented in chapters 4 and 5, respectively. Finally, the main conclusions are given in chapter 6.

Chapter 2

Simulator description

The simulation data presented in this work have been obtained by using a simulator developed within our research group [8, 12]. The geometry and cross-section of the GAA MOSFET studied is shown in figure 2.1, where t_{ins} and t_{si} are the insulator thickness and the silicon body thickness, respectively. It can be seen that the gate completely surrounds the square silicon channel where conduction takes place. To reach a fast convergence, the 2D Poisson and Schrödinger equations, the latter solved for each energy valley, have been self-consistently solved using the predictor-corrector scheme proposed by Trellakis et al. [20] including the energy valley degeneration of the silicon conduction band. The simulator achieves accurate results for different structures, materials and gate voltages if the number of energy levels and their corresponding wave functions employed in the calculation is high enough to capture all the occupied levels.

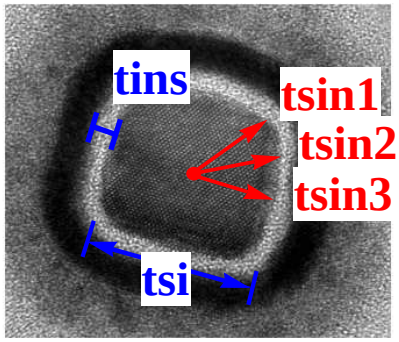


FIGURE 2.1: Different parameters of the device.

The geometry of the device shown in figure 2.1 confines the electrons in the plane perpendicular to the transport direction, which means that we are dealing with a 1D electron gas. The quantum charge density is therefore obtained by evaluating the following expression [8, 20]:

$$\rho(y,z) = \frac{q}{\pi}\left(\frac{2mk_{\mathrm{B}}T}{\hbar^2}\right)^{\frac{1}{2}} \sum_n \Psi_{\mathrm{n}}^2(y,z)\Im_{-\frac{1}{2}}\left(\frac{E_{\mathrm{F}}-E_{\mathrm{n}}}{k_{\mathrm{B}}T}\right) \qquad \left[\frac{C}{cm^3}\right] \tag{2.1}$$

where q is the electron charge, E_{F} is the Fermi level, Ψ_{n} is the wave function belonging to energy level E_{n}, $\Im_{-1/2}$ the complete Fermi-Dirac integral of order -1/2 and the remaining symbols have their usual meaning.

The simulator uses finite elements for the discretization of the equations. More details of the code can be found in the following references [8, 12, 21]. In all the simulated devices, we have considered an undoped substrate ($N_{\mathrm{A}} = 10^{14}$ cm^{-3}), a metal gate with a work-function of 4.61 eV and an insulator thickness of 1.5 nm. The t_{si} values considered in our work were 10, 15 and 20 nm.

Chapter 3

Inversion charge modeling

3.1 1D modeling $f(x)$

As a first step, we propose a 1D analytical model to describe the ICDF of square GAA MOSFETs (bidimensionality will be introduced later). To do so, we use the approach followed by Ge et al. for the symmetrical Double Gate MOSFETs (DGMOSFETs) (equation (4) in Reference [22]). In connection with this, for a perfect square device, in [23], a 2D analytical model for the ICDF was presented as a generalisation of the 1D eigenfunctions proposed by Ge el al. Following a similar approach, we will use the 1D model proposed in [22], adapting it in a parametric approach as we will show in the next chapter. The 1D model chosen was the following:

$$\Psi(x) \approx f(x) = \cos^a\left(\frac{\pi x}{t_{sin}}\right)\cosh\left(\frac{xb}{t_{sin}}\right) \tag{3.1}$$

$$|\Psi(x)|^2 \approx f^2(x) \tag{3.2}$$

As we can see, this model depends solely on 3 parameters:

- t_{sin}, distance from the center of the device to the oxide interface at a given angle α, see figure 2.1. Note that t_{sin} at $\alpha = 0$ equals $\frac{t_{si}}{2}$.
- b, a parameter that depends on the gate voltage Vg and t_{si}.
- a, depends on the shape of the device. While in [23] it was used $a = \frac{1}{2}$ for a perfect square device, in [22] $a = 1$ is used for a 1D MOSFET device. For our model, and for the shake of simplicity, we are going to assume a to be constant. An intermediate value that minimizes the total mean square error when compared with simulation data is chosen.

For the complete 2D model, we also need $s(\alpha)$, the parametric function introduced in the previous chapter. By combining this function with our 1D ICFD model, we can correctly reproduce the behaviour of the device.

3.2 Shape modeling function $s(\alpha)$

By rotating 360 degrees the 1D $\Psi(x)$ function we can model a circular device just using the model for every angle.

For a cylindrical device, we just need $s(\alpha) = 1$, as can be seen in figure 1.2. For a non-circular shaped device, we must take into account that the distance from the center of the device to the opposite side (the parameter we called t_{sin}), depends on the angle α. As the parameters of the model depend on t_{sin}, we need to recalculate t_{sin} and b (b is dependant on t_{si} as well), for every angle. Because of that, in order to change the shape of the device, we must model the boundaries of the device by reproducing the shape we are going to deal with.

As we explained before, there are no perfectly square devices, the corners are rounded because of the technological processes used in their fabrication. An example of a real device is shown in figure 1.1.

We can quantify this "rounding" by means of the curvature of the corners. We measure this curvature by the ratio between the minimum distance between the center of the device to the oxide interface and the maximum (from now on t_{sinmin} and t_{sinmax} respectively). For a square shaped device, we can find the minimum length at $\alpha = 0$ and the maximum at $\alpha = \frac{\pi}{4}$. Supposing $t_{si} = 1$ the maximum length is $\sqrt{2}$, as can be seen in figure 3.1.

Taking into account that for square devices t_{sinmin} is by definition $\frac{t_{si}}{2}$, we can calculate the "rounding" percentage C as the ratio between the difference of t_{sinmax} and t_{sinmin} for a perfect square ($\frac{t_{si}}{2}(\sqrt{2}-1)$) and our shape ($\frac{t_{si}}{2}(\sqrt{2}-t_{sinmax})$):

$$C = \frac{100}{\frac{t_{si}}{2}(\sqrt{2}-1)}\left(\frac{t_{si}}{2}\cdot\sqrt{2} - t_{sinmax}\right) \tag{3.3}$$

With t_{sinmin} and t_{sinmax} being the length of the channel from the center to the oxide for $\alpha = 0$ and $\alpha = \frac{\pi}{4}$ respectively. This equation gives us the curvature percentage of the corners, so a 100% means that we get a perfectly rounded device and a 0% means a perfect square device. For more information on this calculation, see appendix A.

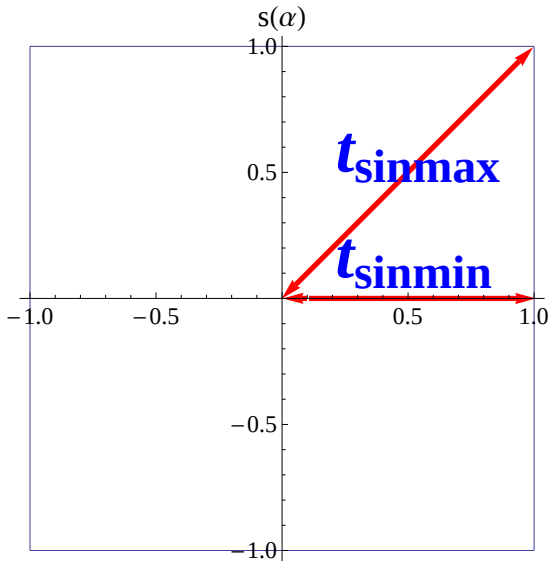
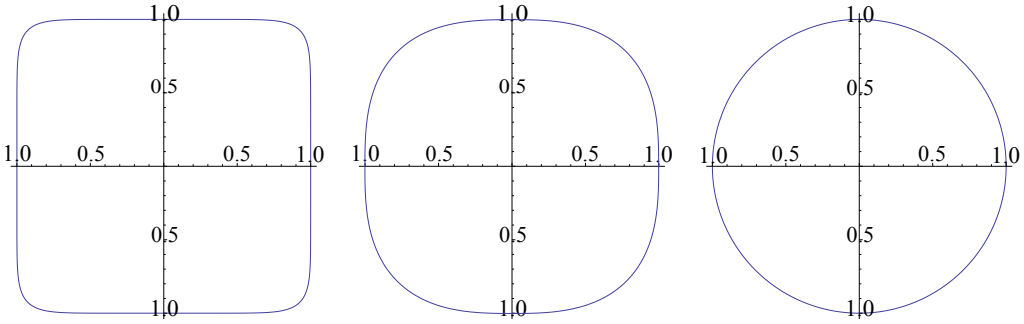


FIGURE 3.1: Distance between the center of the device to the oxide interface at angles $\alpha = 0$: $t_{sinmin} = \frac{t_{si}}{2}$; $s(\alpha = 0) = 1$ and $\alpha = \frac{\pi}{4}$: $t_{sinmax} = \frac{t_{si}}{2} \cdot s(\alpha = \frac{\pi}{4}) = \frac{t_{si}}{2} \cdot \sqrt{2}$. This distances will give us the rounding of the device using equation 3.3.



(a) $C = 25\%$, $n = 9.1152$ (b) $C = 75\%$, $n = 2.7945$. (c) $C = 100\%$, $n = 2$

FIGURE 3.2: Representation of squircle model for different corners curvatures. Parameter n of function $s(\alpha)$ has been calculated for every curvature using 3.5.

Once we can characterize the roundness of the corner, we can model the device shape. For this task, we use the superellipse formula. This formula allows a parametric representation of a square with rounded corners, also called *squircle*, in terms of a few parameters that control not only the curvature, but also the number of corners:

$$s(\alpha) = \left\{ \left| \frac{\cos(\frac{\text{sides}}{4} \cdot \alpha)}{r_a} \right|^{n_2} + \left| \frac{\sin(\frac{\text{sides}}{4} \cdot \alpha)}{r_b} \right|^{n_3} \right\}^{-\frac{1}{n_1}} \tag{3.4}$$

Parameter *sides* control the number of corners, and r_i the ratio between the height and the width of the rectangle. Obviously, for a square device we use $sides = 4$ and $r_a = r_b = 1$. Parameters n_i control the curvature of the corners. For our model, we will use $n_1 = n_2 = n_3$, so we get a squircle. To calculate the n_i parameters, we will use equation 3.3. Then, working out $n_1 = n_2 = n_3 = n$ from equation 3.4 for $\alpha = \frac{\pi}{4}$ (a

square device), we obtain the relation between the parameter n and the percentaje of corner rounding (equation 3.5). For more details, see appendix B.

$$n = n(C) = \frac{\text{Log}[2]}{\text{Log}\left[\frac{1}{1+\frac{1}{200}(-2+\sqrt{2})C}\right]} \tag{3.5}$$

Once we have the parametric representation of the device shape, we can combine it with our 1D modeling function for a complete 2D model of the ICDF, as will be shown below.

3.3 2D Modeling for different square GAA shapes

To get a complete 2D model, we adapt the 1D function given in equation 3.1 by calculating every slice of the 2D model for every angle from the silicon core center to the oxide interface. With the assumption that our 1D model solely depends on the distance between the center of the device and the oxide interface, at any given angle, we can calculate the ICDF once we know the t_{sin} distance. This distance can be easily calculated by multipliying t_{si} by our squircle function at the required angle:

$$t_{sin}(\alpha) = \frac{t_{si}}{2} \cdot s(\alpha) \tag{3.6}$$

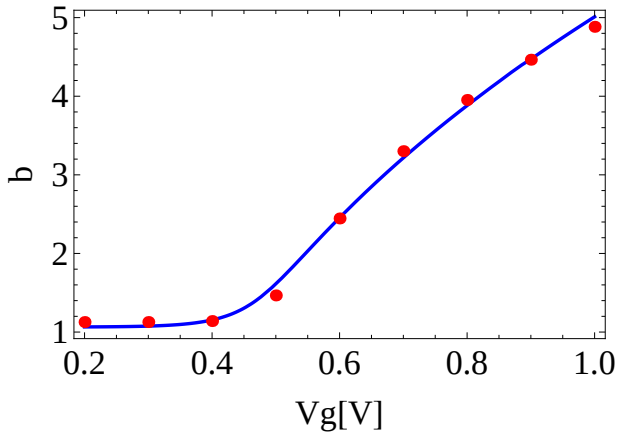
Consequently, $\Psi(x)$ will be defined in the interval $[0, t_{sin}]$. In this way, for every angle, we will get different values of t_{sin}. Because the other model parameters (b and a) also depend on t_{sin}, we will need to describe their dependencies. To obtain these dependencies, we compare the simulated resuls with the the model, for different values of b and a. These values have been selected to fit the simulation data using an iterative algorithm that minimizes the quadratic error between the simulated and the modeled data.

For the a parameter, even though it depends on the shape of the device and the t_{sin} distance, we chose it constant to maintain the simplicity of the model. The final value, after minimization of the cuadratic error is:

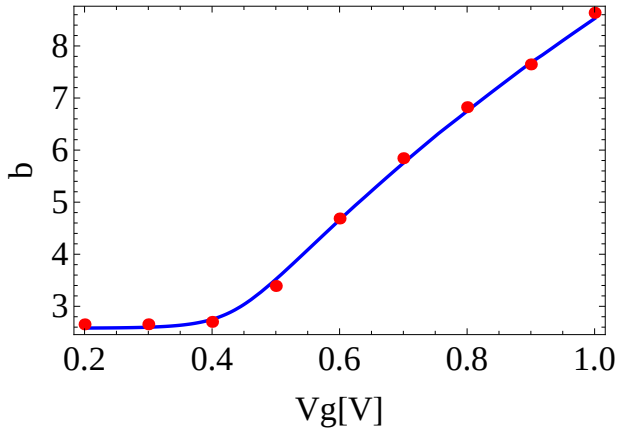
$$a = 0.65 \tag{3.7}$$

For b parameter, we performed an empirical fitting to obtain an analytical expression (see figure 3.3):

$$b = -0.45 + 0.15t_{si} + (0.001 - 0.00004t_{si})N_{inv}^{(0.47+0.006t_{si})} \tag{3.8}$$



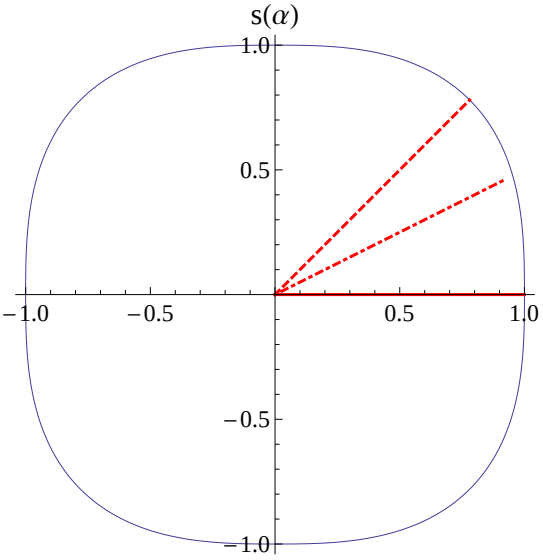
(a) b parameter calculation for $t_{si} = 10nm$.



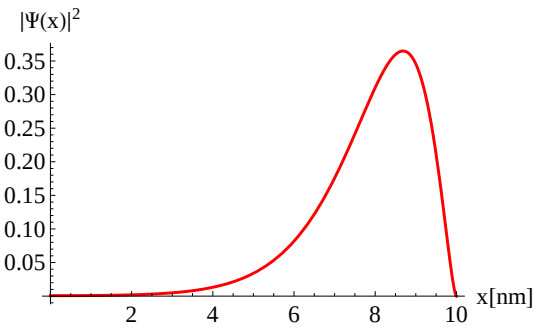
(b) b parameter calculation for $t_{si} = 20nm$.

FIGURE 3.3: Parameter b for different values of t_{si} and Vg as calculated by equation 3.8.

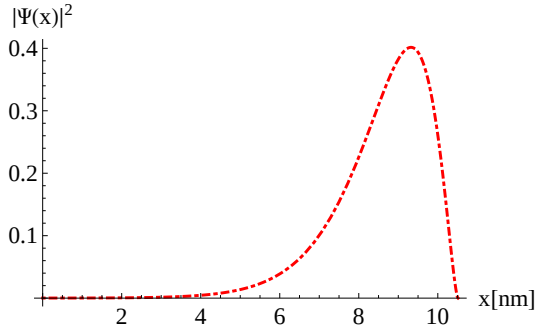
Combining all the analytical expresions, we were able to describe the 2D model. In figure 3.4, we plot few 1D sections of the ICDF.



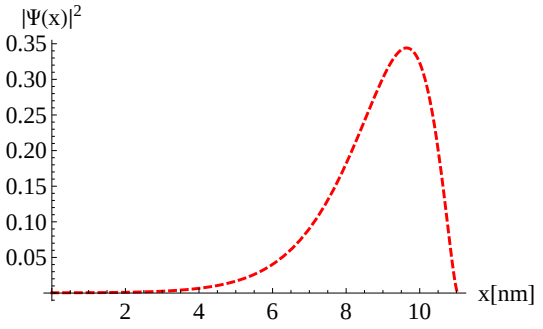
(a) parametric representation of $s(\alpha)$.



(b) $\alpha = 0$



(c) $\alpha = \frac{\Pi}{8}$



(d) $\alpha = \frac{\Pi}{4}$

FIGURE 3.4: ICDF of differents angles cuts for a squircle shaped device. $t_{si} = 20\text{nm}$, $Vg = 1V$ and $C = 75\%$.

Doing so, the resulting equation is:

$$f(x, t_{sin}) = A\left[\cos\left(\frac{\pi x}{t_{sin}}\right)\right]^{a} \cosh\left(\frac{b \cdot x}{t_{sin}}\right) \tag{3.9}$$

Note that f depends on α by means of t_{sin} which is calculated $t_{sin} = \frac{t_{si}}{2}s(\alpha)$, A is the normalization constant and b, a the parameters previously discussed.

Below, we can see a 2D representation of the ICDF:

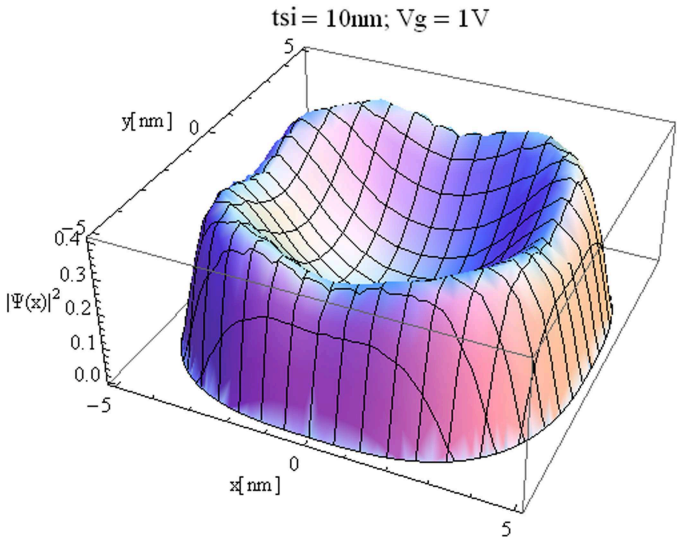


FIGURE 3.5: 2D plot of the function given in equation 3.9 applied for $\alpha\epsilon[0, 2\pi]$; C=75%

In the next figure, we plot the first cuadrant with the simulated data superimposed:

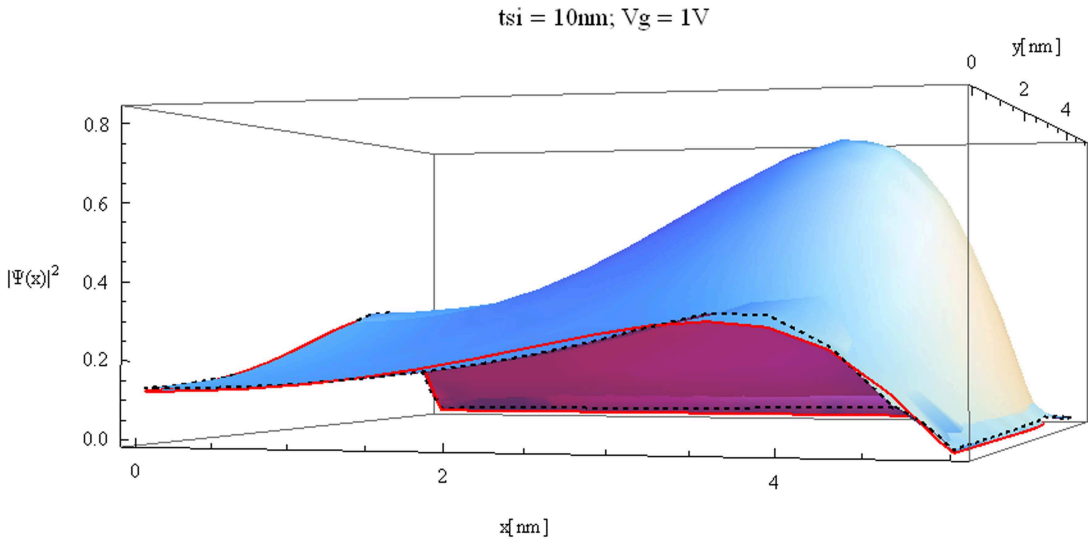


FIGURE 3.6: 2D plot comparison of first cuadrant between simulated (indicated with the black dashed border) and modeled (indicated with the red lines) data. C=25%

As can be seen, the model function fits the simulated data very well even in the 2D representation.

3.4 Comparison with the simulation results

In figure 3.7 and 3.8, we can see a comparison between the modeled ICDF and the simulated data. As can be observed, the fitting is better at middle and lower Vg values. As can be seen, the model reproduces reasonably well the simulation data for a wide range of technological parameters and gate voltages.

In the following chapters, we will use equation (3.9) to model the square GAA MOSFET ICDF in order to deal with the inverse charge centroid and the gate-to-channel capacitance modeling.

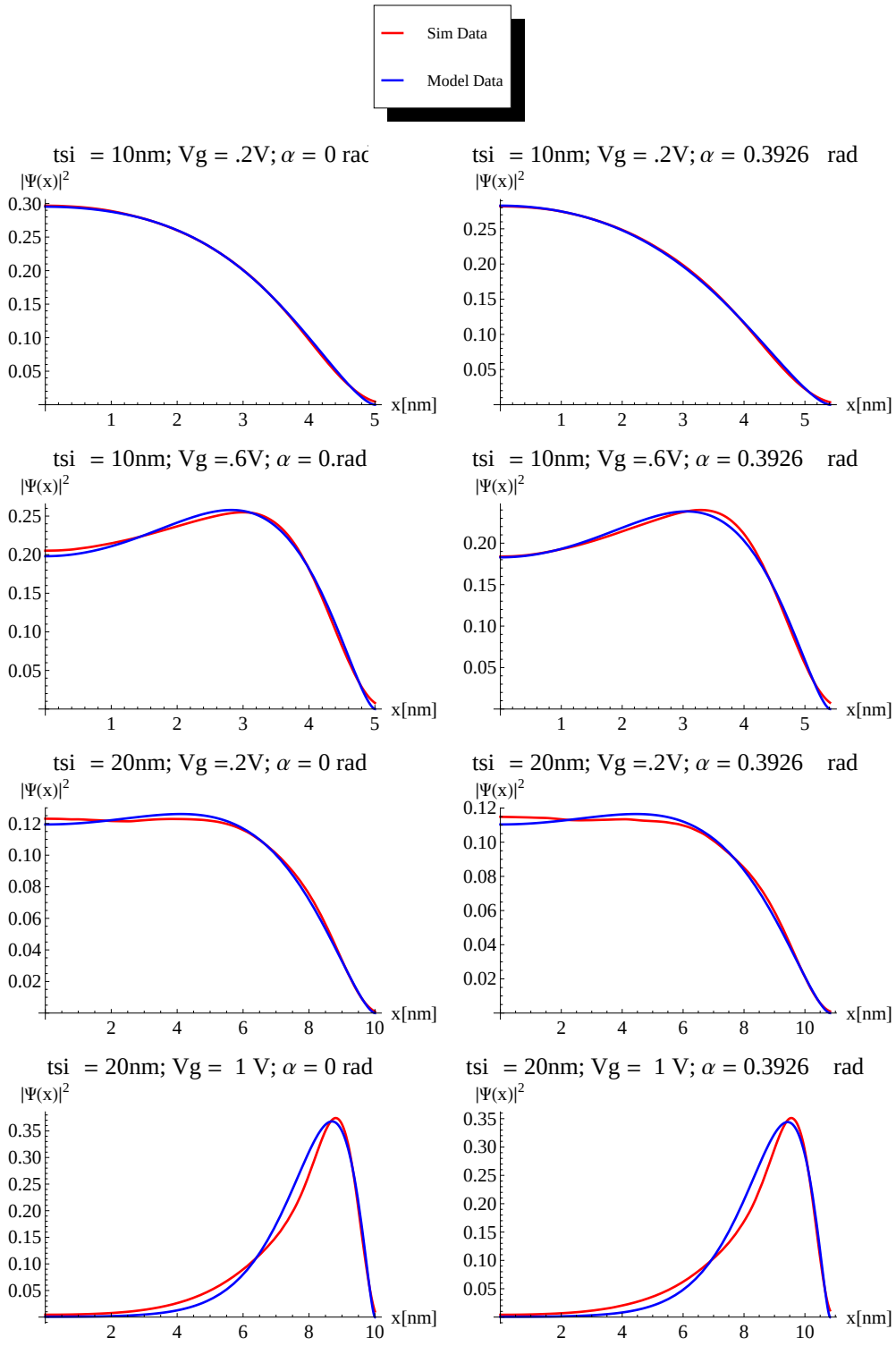


FIGURE 3.7: Comparison of modeled and simulated data for a device with curvature C=25% for differents values of t_{si}, Vg and α values.

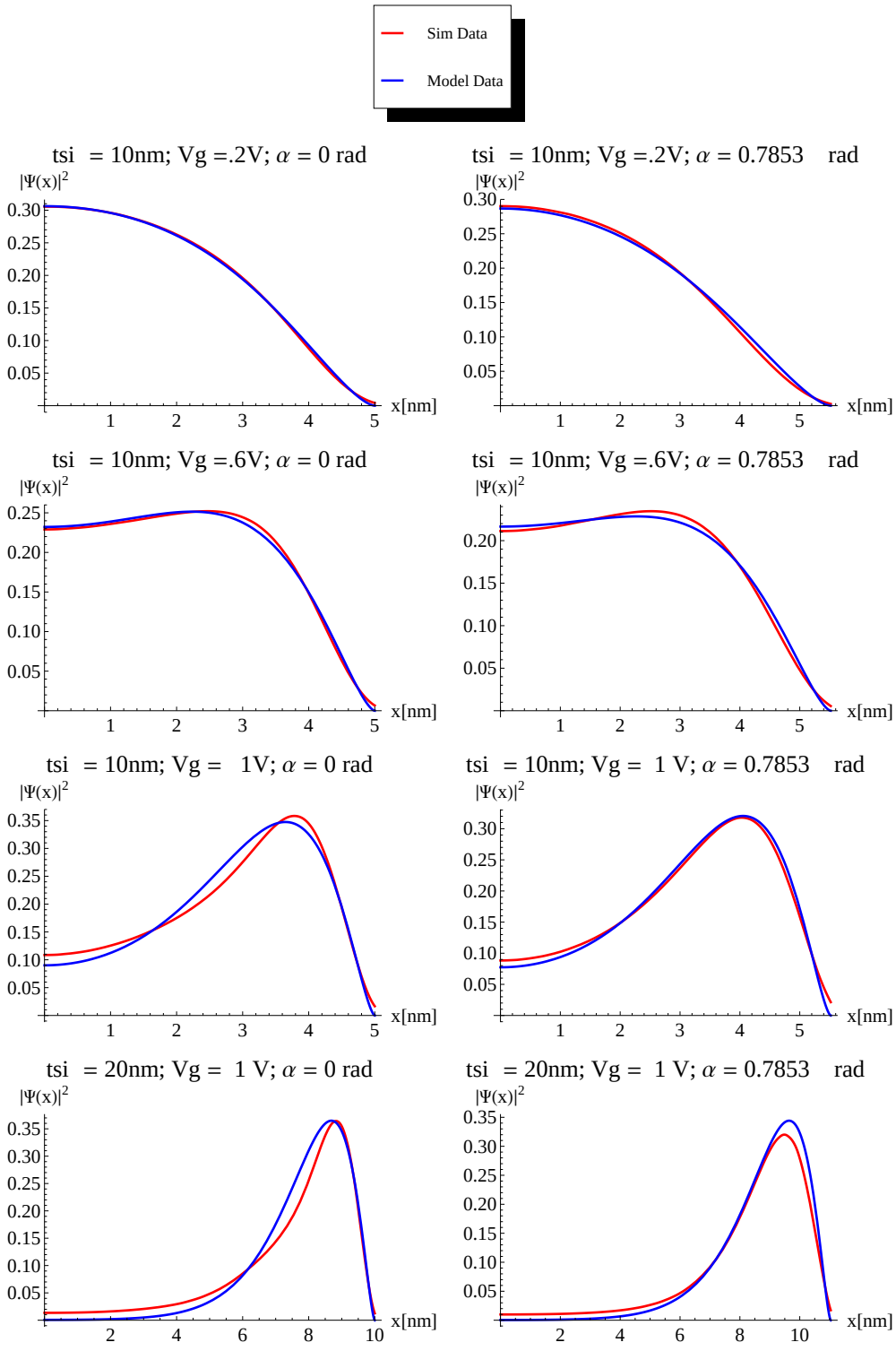


FIGURE 3.8: Comparison of modeled and simulated data for a device with curvature C=75% for differents values of t_{si}, Vg and α values.

Chapter 4

Inversion charge centroid calculation

The inversion charge centroid (ICC) is defined as the first momentum of the inversion charge distribution in conventional bulk MOSFETs [24, 25, 26]. If we compare this parameter with the physical gate insulator thickness, we can estimate the influence of quantum mechanical effects (QMEs) on the inversion charge spatial distribution. The 1D definition of the ICC is intuitive, as reported in [24, 25, 26], and its modeling was carried out in bulk, double-gate and cylindrical surrounding gate MOSFETs [11, 24, 25, 26] (note that cylindrical 2D devices can be analyzed as 1D by means of an appropriate choice of coordinate system [11]). However, the definition of a useful ICC for square GAA MOSFETs is not simple. Some attempts towards this definition have been made previously [27, 28, 23].

To characterize the ICDF, its first momentum $R(\alpha)$ has been calculated (with α being the angle discussed in the last chapter). The mathematical expression for the $R(\alpha)$ calculation is the following:

$$R(\alpha) = \frac{\int_0^{t_{sin}} x^2 \cdot f^2(x,\alpha)dx}{\int_0^{t_{sin}} x \cdot f^2(x,\alpha)dx} \tag{4.1}$$

where t_{sin} is the distance from the center of the silicon core to the semiconductor-insulator interface for each α value (note that due to the device symmetry, only $0 \leq \alpha \leq \frac{\pi}{4}$ has to be considered in the calculation of $R(\alpha)$).

We calculate $R(\alpha)$ making use of the ICDF model introduced in the previous section. In order to establish the accuracy of our model, we define an error function, $E_{rr}(\alpha)$, as the relative difference between the $R(\alpha)$ values obtained with the simulator and the model:

$$E_{rr}(\alpha) = \frac{\Delta R(\alpha)}{R_{\max}} \times 100(\%) = \frac{|R_{\text{Model}}(\alpha) - R_{\text{Sim}}(\alpha)|}{\frac{t_{\text{si}}}{2} \cdot s(\alpha)} \times 100(\%) \tag{4.2}$$

For each applied gate voltage, we calculate the maximum $E_{rr}(\alpha)$ by solving:

$$\left.\frac{\mathrm{d}E_{rr}(\alpha)}{\mathrm{d}\alpha}\right|_{\alpha=\alpha_{max}} = 0$$

for each t_{si} value. The results are given in table 4.1. As can be seen, the model works well (in relation to the calculation of $R(\alpha)$) for all the devices under study and for the whole bias voltage range considered.

t_{si}	10nm	20nm
$E_{rr}^{MAX}(C = 25\%)$	1.10%	1.87%
$E_{rr}^{MAX}(C = 50\%)$	0.97%	1.88%
$E_{rr}^{MAX}(C = 75\%)$	1.92%	1.79%

TABLE 4.1: Maximum value of the $E_{rr}(\alpha)$ function for the GAA MOSFETs studied.

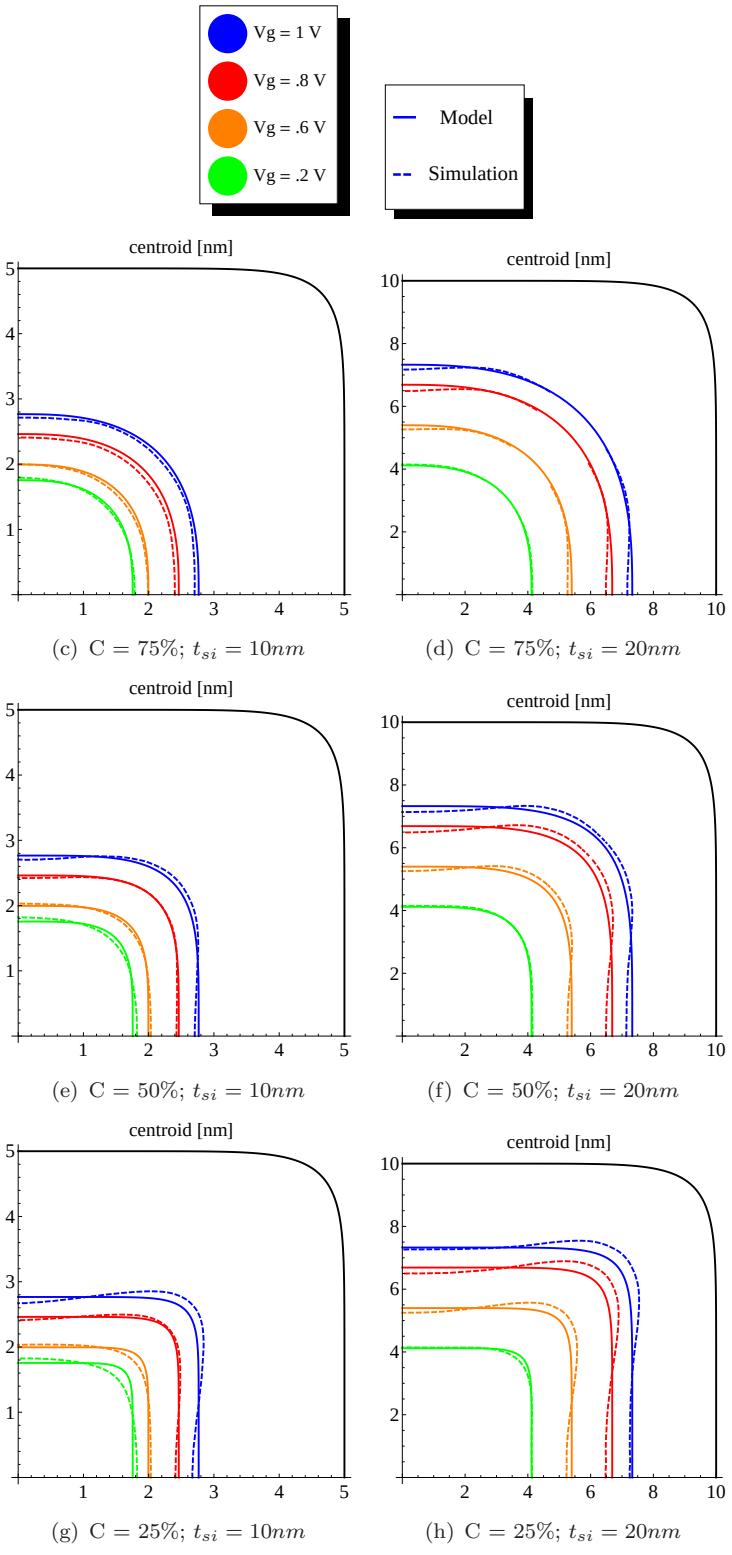
Also, in order to calculate the gate-channel capacitance, we will use the superellipse formula again to calculate the distance between the charge centroid and the oxide interface for all the values of α (Δ_I). This value will be necessary to calculate the gate-to-channel capacity as wil be studied in the next chapter.

$$\Delta_I = \frac{1}{2\pi} \int_0^{2\pi} \left(\frac{t_{si}}{2} \cdot s(\alpha) - R(\alpha) \right) d\alpha \tag{4.3}$$

In the same way, the mean distance between the center of the device and the charge centroid can be calculated:

$$R_I = \frac{1}{2\pi} \int_0^{2\pi} R(\alpha) d\alpha \tag{4.4}$$

In the next figures, we plot a comparison between the $R(\alpha)$ calculated using the modeled and the simulated data.



(c) C = 75%; $t_{si} = 10nm$ (d) C = 75%; $t_{si} = 20nm$

(e) C = 50%; $t_{si} = 10nm$ (f) C = 50%; $t_{si} = 20nm$

(g) C = 25%; $t_{si} = 10nm$ (h) C = 25%; $t_{si} = 20nm$

FIGURE 4.1: Centroid of modeled and simulated data for different curvatures, t_{si} and Vg values.

Chapter 5

Gate-to-channel capacitance modeling

After having developed the model for the ICDF we can use it for calculating other interesting magnitudes. One important parameter is the gate-to-channel capacitance C_{GC}, which determines the transconductance of the transistor [29]. In 1D devices, C_{GC} can be calculated as the series combination of the gate insulator capacitance C_{ins} and the channel capacitance C_{ch} [29, 30, 31, 32]:

$$C_{\mathrm{GC}} = \left(\frac{1}{C_{\mathrm{ins}}} + \frac{1}{C_{\mathrm{ch}}} \right)^{-1} \tag{5.1}$$

However, in the case of square GAA MOSFETs, several approximations are needed to achieve our goal of developing a simple analytical expression for C_{GC}. First, the semiconductor-insulator interface is not isopotential, making equation (5.1) an approximate expression [8, 21, 28]. Moreover, there are no closed analytical expressions either for C_{ins} or for C_{ch}. For the insulator capacitance term, an empirical expression has been obtained for these square GAA MOSFETs with rounded corners, following the line of previous expressions for perfectly square devices [23] and SGT devices [33].

$$C_{\mathrm{ins}} = \frac{\frac{P(t_{si},C)}{t_{si}} F(C) \varepsilon_{\mathrm{ins}}}{\ln\left(1 + F(C)\frac{t_{\mathrm{ins}}}{t_{\mathrm{si}}}\right)} \tag{5.2}$$

With $P(t,C) = 4t(1 + \frac{C}{100}(\frac{\pi}{4} - 1))$ being the perimeter and $F(C) = -0.3(\frac{C}{100})^2 + 1.05(\frac{C}{100}) + 1.25$ a fitting function. It should be noted that if $t_{\mathrm{si}} >> t_{\mathrm{ins}}$, the C_{ins} value is that of a conventional bulk MOSFET.

Regarding the channel capacitance, an approximate expression can be achieved, using the expression corresponding to DGMOSFETs [34], which can be calculated as:

$$C_{\mathrm{ch}}^{-1} = \frac{\mathrm{d}\phi_{\mathrm{s}}}{\mathrm{d}Q_{\mathrm{inv}}} = \frac{\mathrm{d}\left(\phi_{\mathrm{s}} - \phi_{\mathrm{c}}\right)}{\mathrm{d}Q_{\mathrm{inv}}} + \frac{\mathrm{d}\phi_{\mathrm{c}}}{\mathrm{d}Q_{\mathrm{inv}}} \tag{5.3}$$

ϕ_{s} and ϕ_{c} being the electrostatic potential at the surface and the center of the silicon body, respectively, and Q_{inv} the inversion charge per unit length ($Q_{\mathrm{inv}} = qN_{\mathrm{inv}}$). The former equation can be rewritten as [34, 35]:

$$C_{\mathrm{ch}}^{-1} = \frac{x_{\mathrm{i}}}{W\varepsilon_{\mathrm{si}}} + \frac{Q_{\mathrm{inv}}}{W\varepsilon_{\mathrm{si}}}\frac{\mathrm{d}x_{\mathrm{i}}}{\mathrm{d}Q_{\mathrm{inv}}} + \frac{\mathrm{d}\phi_{\mathrm{c}}}{\mathrm{d}Q_{\mathrm{inv}}} = \frac{1}{C_{\mathrm{inv}}} + \frac{1}{C_{\mathrm{c}}} \tag{5.4}$$

where x_{i} is the charge centroid position, defined in [25], and W is the transistor width (necessary to calculate the capacitance per unit length). A description of the physical meaning of each of the capacitance terms can be found in [35].

In order to model the gate capacitance of the devices we are considering, a term equivalent to each of (5.4) is needed. First, a model of the electric potential within the silicon body is needed to calculate C_{c}. Due to the lack of symmetry of this kind of devices, an alternative option is to make use of the similarities found between the potential behavior in cylindrical and square GAA devices [36]. It can be seen that the behaviour of $\mathrm{d}\phi_{\mathrm{c}}/\mathrm{d}Q_{\mathrm{inv}}$ is almost identical between these two antagonist cases. Analytical models for the electrostatic potential of cylindrical GAA devices are available in the literature [9, 37, 38], and here we have modeled the potential at the center of a rounded cornered square GAA MOSFET making use of the expression proposed in [9]. Thus, the C_{c} term can be calculated as [35]:

$$C_{\mathrm{c}}^{-1} = \frac{Q_0 k_{\mathrm{B}} T}{qQ_{\mathrm{inv}}\left(Q_0 + Q_{\mathrm{inv}}\right)} \tag{5.5}$$

where $Q_0 = (k_{\mathrm{B}}T/q)8\pi\varepsilon_{\mathrm{si}}$ and the remaining parameters keep their usual meaning. In [23], it was shown that the derivative of the electric potential with respect to the inversion charge at the center of the silicon body is approximately the same for a cylindrical and a square GAA devices.

To calculate the inversion capacitance term in (5.4), C_{inv}, the DG MOSFET centroid definition was first replaced by the one introduced in the previous section. Then, the planar capacitance formula $W\varepsilon_{\mathrm{si}}/x_{\mathrm{i}}$ was replaced by its square quadruple-gate counterpart (found from (5.2) where t_{ins} and t_{si} are replaced by Δ_{I} and R_I, respectively). Finally a fitting parameter K replaced the channel width W in the second part of the C_{inv} term, to appropriately take into account the 2D confinement effect. The resulting expression for square GAA MOSFETs C_{inv} is:

$$C_{\mathrm{inv}}^{-1} = \left(\frac{\frac{P(2R_I,C)}{2R_I}F(C)\varepsilon_{\mathrm{si}}}{\ln\left(1 + F(C)\frac{\Delta_{\mathrm{I}}}{2R_{\mathrm{I}}}\right)}\right)^{-1} + \frac{Q_{inv}}{K\varepsilon_{\mathrm{si}}}\frac{\mathrm{d}\Delta_{\mathrm{I}}}{\mathrm{d}Q_{\mathrm{inv}}} \tag{5.6}$$

We have chosen a K parameter (by means of an empirical fitting) whose value is of the order of the one used in reference [23] ($2 \cdot 10^{-6} cm$). Nevertheless, for these devices, the second term on the right in equation 5.6 does not contribute much to the final capacitance value.

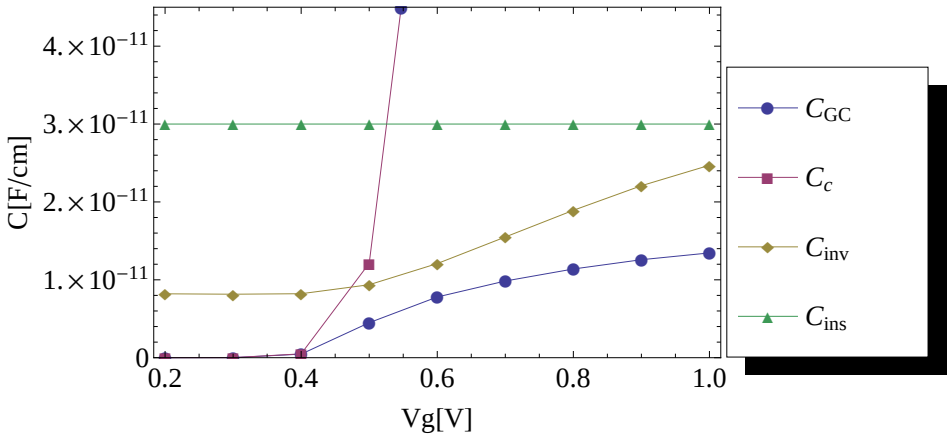
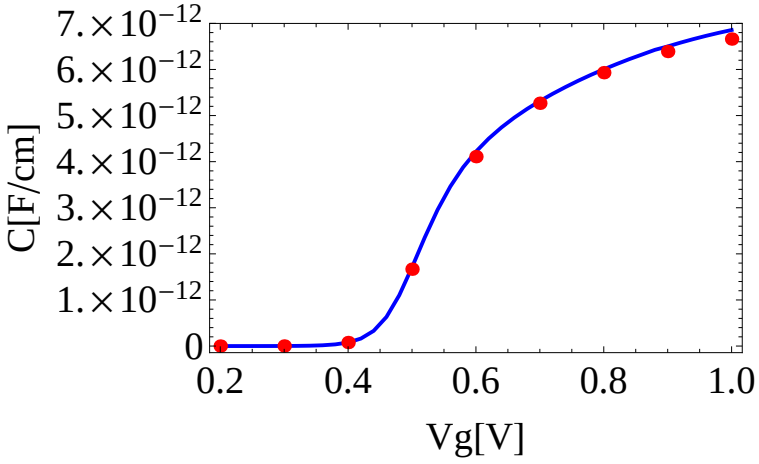
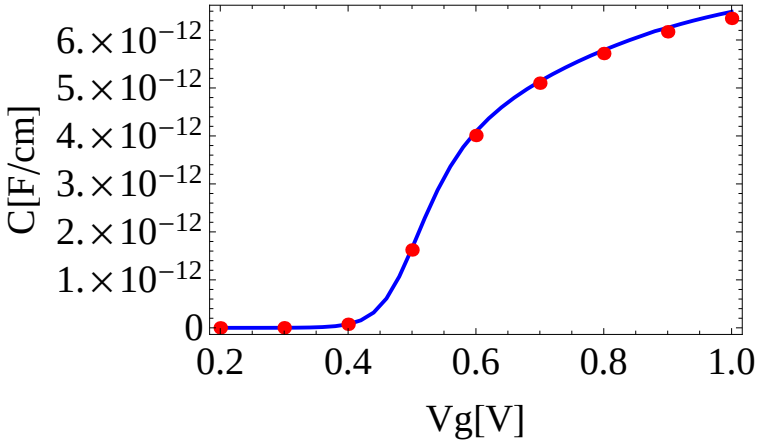


FIGURE 5.1: Factors of gate-to-channel capacity (C_{GC}) for t_{si}=20nm and C=25%.

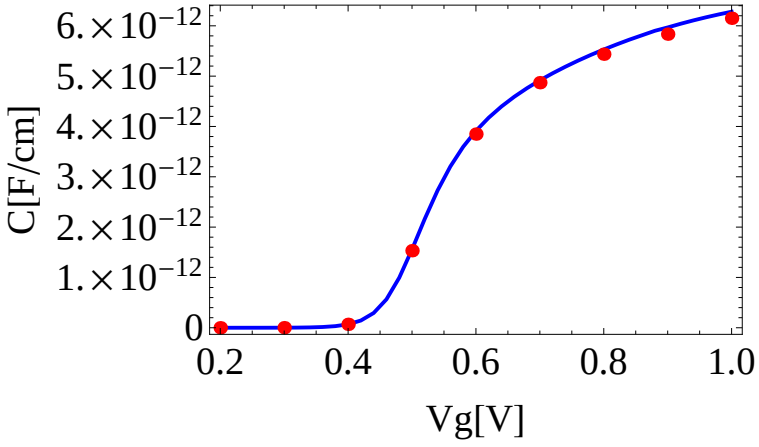
In the next figures, the modeled gate-to-channel capacitance is compared with simulation data. As can be seen, the C_c term controls the behavior of the device in the weak inversion regime, while C_{inv} is responsible for the gate capacitance degradation with respect to the ideal limit value C_{ins}. A very good agreement between the model and the simulated data is achieved.



(a) C=25%

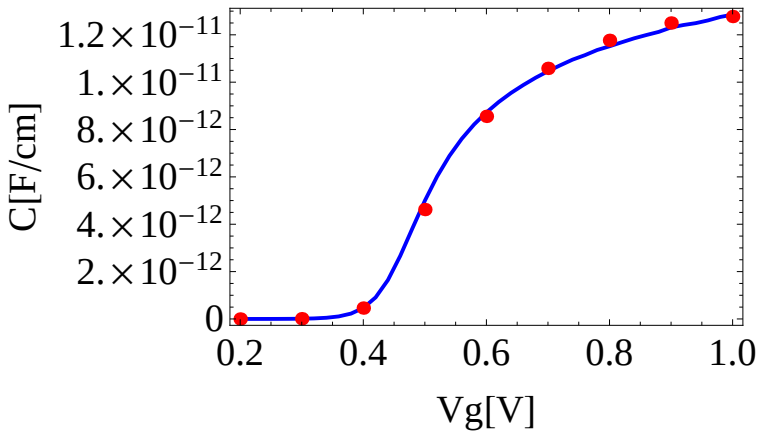


(b) C=50%

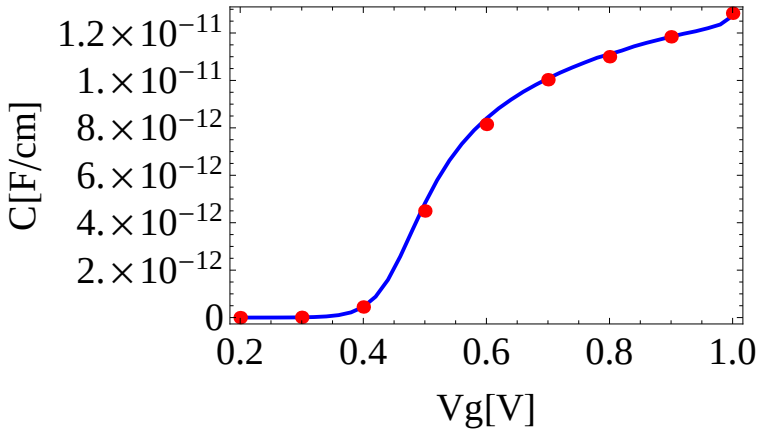


(c) C=75%

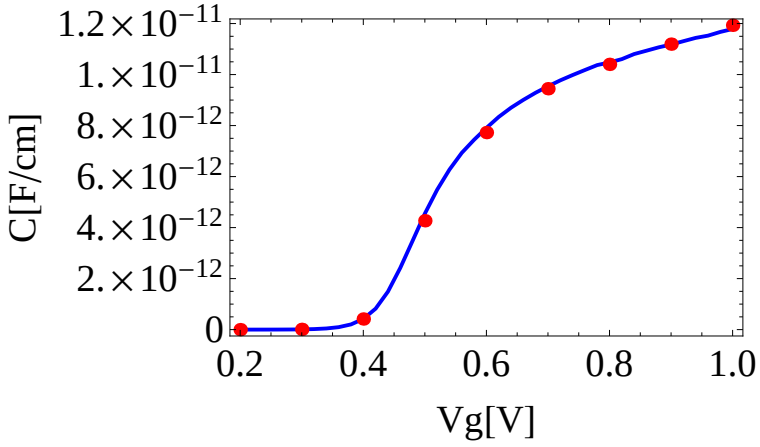
FIGURE 5.2: Gate-to-channel modeled capacitance C_{GC} (blue line) versus simulated data (red dots) for t_{si}=10nm and different curvatures.



(a) C=25%



(b) C=50%



(c) C=75%

FIGURE 5.3: Gate-to-channel modeled capacitance C_{GC} (blue line) versus simulated data (red dots) for t_{si}=20nm and different curvatures.

Chapter 6

Conclusions

We have introduced an analytical model for the inversion charge distribution function of square GAA MOSFETs with rounded corners where quantum effects have been taken into account. The model has been tested by means of a comparison with simulation data obtained by self-consistently solving the 2D Schrödinger and Poisson equations for a wide variety of device sizes, corner curvatures and bias ranges.

We have also calculated the inversion charge centroid and gate-to-channel capacitance by using the inversion charge distribution function developed previously. A very good agreement between the simulated and modeled data was achieved both for the ICC and the C_{GC} for different device geometries and biases. The simplicity and accuracy of the models presented are very promising from the compact modeling point of view since GAA MOSFETs are considered good candidates for future sub-20nm integrated circuit technologies.

Appendix A

Rounding percentage calculation

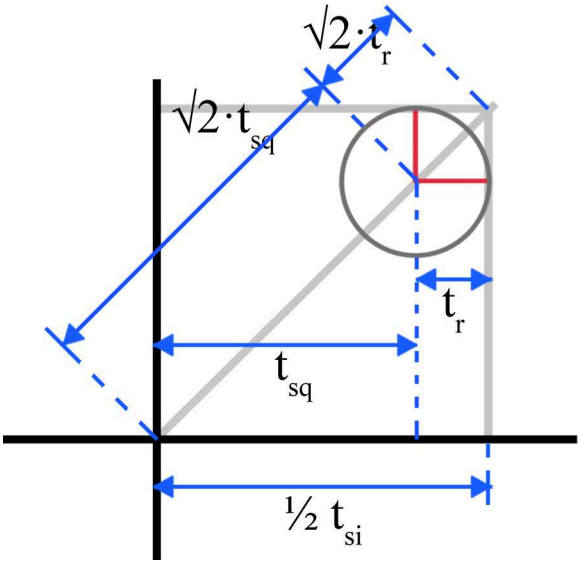


FIGURE A.1: Definition by parts of a rounded corner in a square GAA MOSFET.

In this appendix we are going to prove that the definition of corner curvature used in the numerical simulator is equivalent to the one based on equation 3.3, which is adapted to be used in the squircle function definition. In the numerical simulator, the roundness of the corners is defined as follows (see figure A.1):

$$t_r = \frac{C'}{100} \cdot \frac{t_{si}}{2} \tag{A.1}$$

It can be seen that for $C' = 100$ we are considering a circular device and for $C' = 0$ it is a perfectly square device (this numbers are coherent with the definition based on equation 3.3). In order to show the equivalence of both definitions, we are going to show that the diagonal length of these devices calculated with the two different methods is

the same. See the equation below, where half of the diagonal length is calculated with the squircle formula.

$$\frac{t_{si}}{2}s(\frac{\pi}{4}) = \sqrt{2}\frac{t_{si}}{2} + t_r(1-\sqrt{2}) \tag{A.2}$$

On the left hand side, we have the diagonal length given by our superellipse formula. On the right hand side the one given by the function defined by parts (deduced using figure A.1 and equation A.1). Substituting equation A.1 in A.2

$$s(\frac{\pi}{4}) = \sqrt{2} + \frac{C'}{100}(1-\sqrt{2}) \tag{A.3}$$

If we use the definition given in equation 3.3 and taking $t_{sinmax} = \frac{t_{si}}{2}s(\frac{\pi}{4})$, we can see that:

$$C = \frac{100}{\frac{t_{si}}{2}(\sqrt{2}-1)}\left(\frac{t_{si}}{2}\cdot\sqrt{2} - t_{sinmax}\right) = \frac{100}{(\sqrt{2}-1)}\left(\cdot\sqrt{2} - s(\frac{\pi}{4})\right)$$

So, substituting A.3 in the equation above,

$$s(\frac{\pi}{4}) = \sqrt{2} + \frac{C}{100}(1-\sqrt{2}) = \sqrt{2} + \frac{C'}{100}(1-\sqrt{2}) \Rightarrow C = C'$$

However, we can use the definition used in the simulator to avoid unnecesaries complications and easily calculate the perimeter. We can calculate the perimeter as the combination of the perimeter of the sides of the square t_{sq} and the one given by the circle radius t_r:

$$t_{sq} = (1-\frac{C}{100})\sqrt{2}\cos\frac{\pi}{4}t_{si} = (1-\frac{C}{100})\frac{t_{si}}{2} \tag{A.4}$$

$$t_r = \frac{t_{si}}{2} - t_{sq} \tag{A.5}$$

So the perimeter can be calculated as:

$$P(C) = 2\pi t_r + 8t_{sq} = 4t_{si}(1 + \frac{C}{100}(\frac{\pi}{4} - 1)) \tag{A.6}$$

Appendix B

Rounding parametric representation

In this appendix we show in detail the steps to obtain the relation between n and the percentaje of corner rounding C, given by Eq. (3.5). Let us point out that, for a square shaped device, $t_{\text{sinmax}} = s\left(\frac{\pi}{4}\right)\frac{t_{\text{si}}}{2}$, where $s(\alpha)$ is the parametric representation of the squircle given by Eq. (3.4):

$$\begin{aligned} s\left(\frac{\pi}{4}\right) &= \left[\left\{\cos\left(\frac{\pi}{4}\right)\right|^n + \left|\sin\left(\frac{\pi}{4}\right)\right|^n\right\}^{-\frac{1}{n}} \\ &= \left[2\left(\frac{\sqrt{2}}{2}\right)^n\right]^{-\frac{1}{n}} \end{aligned}$$

where we have taken into account that sides $= 4$, $r_a = r_b = 1$, and the parameters n_i which control the curvature of the corners are equal, $n_1 = n_2 = n_3 = n$.

With this assumptions, the rounding percentage C (Eq. (3.3)) has the form

$$\begin{aligned} C &= \frac{100}{\sqrt{2}-1}\left(\sqrt{2} - s\left(\frac{\pi}{4}\right)\right) \\ &= \frac{100}{\sqrt{2}-1}\left(\sqrt{2} - 2^{-\frac{1}{n}}\frac{2}{\sqrt{2}}\right) \\ &= \frac{200}{2-\sqrt{2}}\left(1 - 2^{-\frac{1}{n}}\right) \end{aligned}$$

working out the term dependant on n,

$$2^{-\frac{1}{n}} = 1 - \frac{2-\sqrt{2}}{200}C;$$

$$-\frac{1}{n}\log 2 = \log\left(1 + \frac{\sqrt{2}-2}{200}C\right);$$

So, the relation betwen n and the percentaje of corner rounding C is given by Eq. (3.5):

$$n = n(C) = \frac{\text{Log}[2]}{\text{Log}\left[\frac{1}{1+\frac{1}{200}\left(-2+\sqrt{2}\right)C}\right]}$$

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List of Figures