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CHARACTERIZATION, MODELLING AND SIMULATION OF DECANANOMETER SOI MOSFETs

Doctoral Thesis

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CERTIFY:

that the research work contained in the present report, entitled *Characterization, Modelling and Simulation of Decananometer SOI MOSFETs*, and presented by **Mr. Noel Rodriguez Santiago** to obtain the Doctor Degree by the Universidad de Granada and the Institut National Polytechnique de Grenoble with the *Doctor Europeus* mention, has been made under our full supervision at the Departamento de Electrónica y Tecnología de Computadores of the Universidad de Granada and the Institut de Microélectronique, Électromagnétisme et Photonique of the Institut National Polytechnique de Grenoble.

Granada, 10th of December, 2007

Prof. Dr. Francisco J. Gámiz Pérez	Prof. Dr. Sorin Cristoloveanu
Professor of Electronics UGR	Director of Research CNRS

To my parents, brother
and... future girl friends

I never paint dreams or nightmares,
I paint my own reality.

Frida Kahlo (1907-1953)

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Abbreviations and acronyms

1D, 2D, 3D Uni, Bi,Tri-Dimensional.

BJT Bipolar Junction Transistor.

BOX Buried OXide.

BTE Boltzmann Transport Equation.

CMOS Complementary MOS.

CYNTHIA Cylindrical Thin Pillar.

DC Direct Current.

DD Drift Difussion.

DG Double Gate.

DGSOI Double Gate SOI transistor.

DIBL Drain Induced Barrier Lowering.

ELTRAN Epitaxial Layer Transfer.

EMC Ensemble Monte Carlo.

EME Effective Mass Equation.

EOT Effective Oxide Thickness.

FDSOI Fully Depleted SOI Transistor.

FET Field Effect Transistor.

GAA Gate All Around transistor.

GeOI Germanium On Insulator.

ITOX High temperature Internal Oxidation.

ITRS International Technology Roadmap for Semiconductors.

JFET Junction Field Effect transistor.

LDMOS Lateral Double-Diffused MOS.

LIGBT Lateral Insulated Gate Bipolar Transistor.

MC Monte Carlo.

MEMS Micro Electro-Mechanical Systems.

MIS Metal Insulator Semiconductor.

MODFET Modulation-doped Field Effect Transistor.

MOS Metal Oxide Semiconductor.

MR Magnetoresistance.

PDSOI Partially Depleted SOI transistor.

SCE Short Channel Effects.

SDE Source Drain Engineering.

SDE-DC Source Drain Engineering and Doping Compensation.

SSDOI Strain Silicon Directly On Insulator.

SSi-GeOI Strain Silicon on Germanium On Insulator.

sSi/SiGeOI Strain Silicon on Silicon Germanium On Insulator.

SET Single Electron Transistor.

SG Single Gate.

SGSOI Single Gate SOI transistor.

SHG Second Harmonics Generation.

SIMOX Separation by Implantation of OXygen.

SIMOX MLD Modified Low Dose SIMOX.

SOI Silicon On Insulator.

SOR Succesive Over Relaxations.

SR Surface Roughness.

SSDOI Strain Silicon Directly On Insulator.

ULSI Ultra Large Scale of Integration.

UTB Ultra Thin Body.

VCBM Voltage-Controlled Bipolar MOS Device.

VDMOS Vertical Lateral double-diffused MOS.

VM Velocity Modulation.

VMT Velocity Modulation Transistor.

Prologue

For many years, inside the Electronic World, the best way to explore the future has been to concoct it. Since in 1947 Dr. John Bardeen and Dr. William Shockley invented the transistor at Bell Labs, the Electronics has experimented a vertiginous advance. Six years after the revolutionary device saw the light, in 1954, Texas Instruments built the first transistorized radio receiver. In 1958, the American engineers Jack Kilby and Robert Noyce developed the first integrated circuit merging, in the same silicon chip, different components by means of gold connections: the first solid state circuit was born.

At the end of 1961 Dr. Steven Hofstein and Dr. Frederic Heiman, from RCA Princeton Lab., built the first operating MOSFET transistor. Although initially it was slower than the junction bipolar transistor, the MOSFET was smaller, cheaper and it needed less power to operate, allowing a higher number of transistors in the same area and reducing the power dissipation problems.

Currently most of the electronic integrated circuits are built with MOSFETs as basic component. The take off of the electronics industry has been exponential: adaptive automatic equalizers, the pocket calculator, the CD-ROM, computers on chip... The performance of the commercial applications has improved spectacularly due to the underlying increment in the device performance. This improvement is linked to the progressive transistor miniaturization, making possible a higher integration level, a higher operation speed and reducing the cost.

Nevertheless, the device miniaturization causes a set of problems with complex solution. Nowadays feature dimensions of the transistors are in the range of few atomic layers. The discrete nature of the matter and the quantum limitations make these effects, ignored a few years ago, to be included in the current design and

modelling.

This work studies the impact, chances and challenges of the decananometric miniaturization on the performance of the incoming transistor generation (45nm node [ITR06]).

Two are the main research task accomplished:

1. The characterization and modelling of the quantum effects revealed when the device dimensions are exploited to the physical limits.
2. The introduction of the FD SOI technology as one of the best candidates for the future technology, extending the life of the MOSFET based world.

The structure of the work is described as follows:

PART I: THE ULTIMATE MOSFET TECHNOLOGY

Chapter 1. MOSFET quantum simulation: A brief review of the quantum mechanical description of the MOSFET structure is depicted. Also in this chapter, the Poisson-Schrödinger self-consistent solver is introduced and the effective mass evaluation method is explained.

Chapter 2. Crystallographic orientation influence on static properties: The inclusion of quantum effects in MOSFETs models is motivated to accurately describe the behavior of today's devices. An empirical expression is developed for the inversion layer centroid and the polysilicon-gate depletion region for bulk MOSFETs with different crystallographic orientations. In particular, results for the most commonly used wafer orientations, i.e., (100), (110), (111), are given. These expressions are used to accurately model the inversion charge and the gate-to-channel capacitance of MOSFETs with oxides of nanometric thickness (T_{ox}<1nm) and different surface orientations. The Poisson and Schrödinger equations are self-consistently solved for different values of silicon and polysilicon doping concentrations in these devices. The results show important reductions both in the inversion charge and the gate-to-channel capacitance. It is possible to include these effects in accurate

MOSFET models by means of a corrected gate-oxide thickness, which accounts for both the effect of the inversion layer centroid and the polysilicon depletion thickness.

Chapter 3. Accumulated carrier quantization and its effects on silicide-gated MOSFET: The electrical behavior of MOSFETs with polysilicon gates in accumulation and inversion is studied when the silicon doping concentration is increased up to a level emulating the metallic limit for silicides. It is showed that poly-accumulation/depletion effects are still present in metal gate. Poisson-Schrödinger simulations reveal a lower capacitance in the case of the silicide-gate when compared to the ideal metal-gates; as a consequence, the assumption that silicided gates behave like ideal metals leads to an overestimate of the physical thickness of the extracted insulator. Polysilicon quantization produces a shift of the flat-band voltage when is compared to the classical flat-band voltage value. This quantum shift increases as the polysilicon doping increases, up to 10^{21}cm^{-3}. However, for higher doping, this flat-band shift decreases. Finally analytical models are used to interpret the highly doped silicide limit.

Chapter 4. Remote scattering mechanisms in ultra-thin gate-oxide MOSFETs: The effect of remote scattering mechanisms (such as remote coulomb scattering and remote surface-roughness scattering) on electron mobility in ultra-thin oxide MOSFETs is studied. The important role these scattering mechanisms play in the state-of-art devices, mainly at low temperature is highlighted. A mobility model which takes into account the contribution of these remote mechanisms is developed. The proposed expression allows to reproduce the Monte Carlo simulations of mobility.

PART II: THE SOI PARADIGM

Chapter 5. SOI technology: This chapter introduces Silicon On Insulator technology (SOI). The main motivations to develop this technology are commented followed by the description of the processes to obtain SOI wafers. Then, the main advantages to the conventional bulk technology are discussed finishing with the taxonomy of the different kind of devices that can be fabricated from SOI wafers.

Chapter 6. SOI wafers characterization: In this chapter, two of the most advanced and reliable wafer characterization techniques are presented: the second harmonic generation and the pseudo-MOSFET (Ψ-MOSFET). Numerical simulations clarify the influence of the free surface quality on the Ψ-MOSFET characteristics, shedding light on the dramatic threshold voltage shift experimentally observed when the SOI layer thickness is reduced below 50 nm. Analytical and empirical models are proposed.

Chapter 7. Mobility extraction for SOI transistors: The methodology of mobility extraction is revisited in the context of SOI MOSFET transistors including the genuine magnetoresistance technique. The Y-function is proposed like a reliable characterization technique. Based on a simple 2-channels model the biasing conditions enabling the Y-function to be applied to both single-gate (SG) and double-gate (DG) modes are discussed. In SG-mode, the mobility is overestimated as soon as the opposite channel is activated. In partially depleted or relatively thick fully-depleted MOSFETs, the two channels are separated, hence the total apparent mobility in DG-mode is the sum of the front and back channel mobilities.

In the second part of this chapter, Systematic mobility measurements in thick and ultra-thin SOI transistors are presented for the front- channel, back-channels and in quasi double-gate mode. The validity of the model is checked on PD and relatively thick FD MOSFETs. By contrast, the 2-channel model fails in ultra-thin transistors, where the two channels become strongly coupled and volume inversion occurs. Volume inversion is reflected in a remarkable increase of the apparent mobility in DG mode.

Chapter 8. Mobility simulation results: The electron transport is studied by the Monte Carlo method. The chapter starts studying the behavior of electron mobility in bulk MOSFETs and SOI MOSFETs with different surface *(hkl)* orientations and channel <hkl> directions, using a Monte Carlo simulator. For each surface orientation, different channel directions are also considered. In the case of the (110) surface, a strong anisotropy of electron mobility with the channel direction is observed: when the channel is built in the (110)/<001> direction, electron mobility is 50% higher than in (110)/<$1\bar{1}0$>, and is closer to the mobility for a (100)/<001> direction. This anisotropic behavior with channel orientation is not observed in the

(100) or (111) surface orientations. The study with silicon thickness also revealed some interesting consequences of the volume inversion effect.

The second part of this chapter is dedicated to the electron transport in strained double gate silicon on insulator transistors. Poisson and Schrödinger equations are self-consistently solved in these devices for different silicon layer thicknesses both for unstrained and strained silicon channels. The results show that the strain of the silicon layer leads to a larger population of the no-primed subbands, thus decreasing the average conduction effective mass. However, strain also contributes to a larger confinement of the charge close to the two Si/SiO_2 interfaces, thus weakening the volume inversion effect, and limiting the potential increase of the electron mobility.

Finally, the geometric magnetoresistance is reproduced by Monte Carlo simulations and used to accurately extract the carrier mobility. This original method allows comparing the transport mechanisms in various cases of interest: Single-Gate (SG) versus Double-Gate (DG) operation, Si-high-k versus Si-SiO_2 interfaces, in-depth inhomogeneous transport.

Part I

THE ULTIMATE MOSFET TECHNOLOGY

Chapter 1

MOSFET quantum simulation

The inclusion of quantum effects in MOSFET simulators is essential to accurately describe the electrical behavior of today's devices [LVCCB+97], [RGLVC97], [RGLV+01], [TT95], [FL93]. However, the need for simulation tools fast enough to take into account the great number of simulations required to deal with the first stages of a design process creates an incentive for introducing modifications in classical simulators. Accounting in this way, for quantum effects by means of simple empirical or semi-empirical models [LVCCB+97], [RGLV+01]. Monte Carlo techniques are very reliable and accurate, but excessively time-consuming and cannot be used in massive simulations due to the huge computational power required. In this case, the use of analytical and empirical models is imperative. Both the drift-diffusion approach for device simulation and the compact modelling approach for circuit simulation strongly depend on accurate models to describe the physical behavior that takes place in present devices or in future devices developed under more aggressive dimension reduction schemes.

1.1 Introduction: The Schrödinger equation

External electric fields or charges can change the properties of semiconductor surfaces significantly. An n-type inversion layer is produced at the surface of a p-type semiconductor when the energy bands near the surface are bent down enough so that the bottom of the conduction band lies near or below the Fermi level.

This band bending is achieved by applying an electric field to the surface (1.1). The inversion channel can also be created by the presence of positive charges at or near the surface.

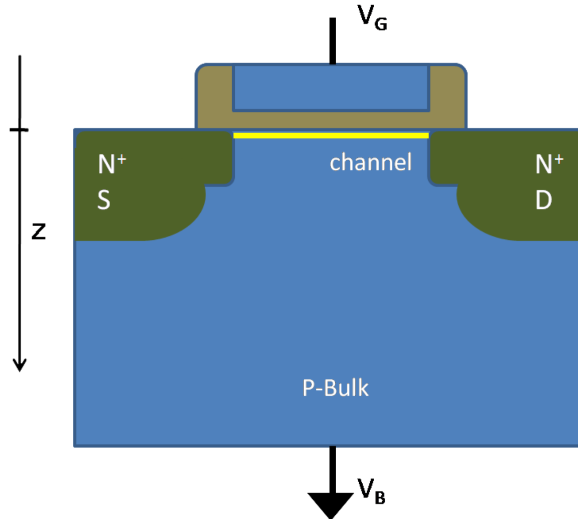


Figure 1.1: Schematic MOSFET structure.

When the potential well in the z direction, perpendicular to the interface is produced, the energy levels for the electrons are split in electric subbands. Each of them corresponds to a quantized level of motion in the z direction with a continuum of motion in the plane parallel to the surface.

The band bending at the semiconductor surface can be characterized by an electrostatic potential $V(z)$.

The effective-mass equation (EME) provides an accurate, easy way to implement the Hamiltonian. In the effective-mass approximation, the electronic wave function for the *i-th* subband is the product of the Bloch function at the bottom of the conduction band and the envelope function:

$$\Psi_i(x,y,z) = \psi_i(z)\, e^{j\theta z} e^{jk_1 x + jk_2 y} \tag{1.1}$$

where k_1 and k_2 are measured relative to the band edge, θ depends on k_1 and k_2

and $\psi_i(z)$ is the solution of

$$\frac{d^2\psi_i}{dz^2} + \frac{2m_3}{\hbar^2}\left[E_i + eV(z)\right]\psi_i(z) = 0 \tag{1.2}$$

We are interested in the bounded solutions. Each eigenvalue E_i is found from the solution of Eq. 1.2 and it is the bottom of a continuum of levels called subband with energy levels given by:

$$E_i\left(\overrightarrow{k}\right) = E_i + \frac{\hbar^2 k_1^2}{2m_1} + \frac{\hbar^2 k_2^2}{2m_2} \tag{1.3}$$

where m_1 and m_2 are the principal effective masses for the motion parallel to the surface.

1.2 Effective-mass approximation for arbitrarily oriented MOSFETs

It is necessary to extend the application of EME to analyze NMOSFET for arbitrary wafer orientations.

The conduction band minima of cubic semiconductor materials appear either at a single point (for direct band-gap materials such as GaAs) or at multiple equivalent points (for indirect band-gap materials such as Si and Ge) within the first Brillouin zone (Figure 1.2). The constant energy surfaces become nonparabolic and warped for energies away from the band minima; close to the band edges, however, the relevant electronic states for transport calculations can be described by simple ellipsoidal surfaces. Under these circumstances, the constant energy surface for electrons in a direct band-gap material is spherical, centered on the Γ point and described as:

$$E\left(k\right) = \frac{\hbar^2 k^2}{2m_{eff}} \tag{1.4}$$

with a constant, isotropic effective mass m_{eff}. For indirect semiconductor materials, the conduction band minima are located at multiple equivalent points: six points near X along the Δ or <100> crystallographic directions for silicon, and eight equivalent points at L along Λ or <111> for germanium.

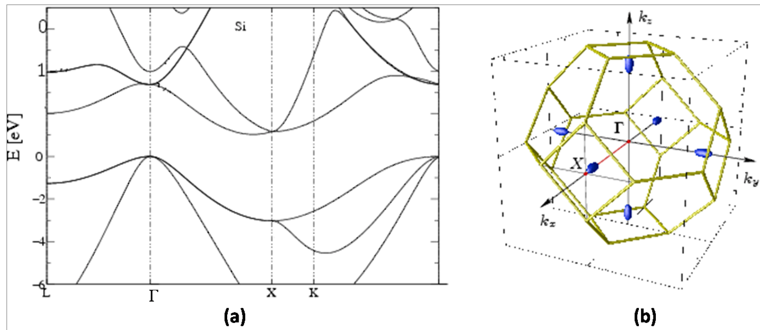


Figure 1.2: **(a)** Silicon band structure. **(b)** First Brillouin zone and associated isoenergetic ellipsoids for silicon. *Source http:\\iue.tuwien.ac.at.*

In indirect semiconductors, the constant energy surfaces are ellipsoids of revolution around Δ and Λ axes, respectively, requiring two effective masses, longitudinal m_l and transverse m_t, for description (Figure 1.2(b)). In general, the nonalignment of the ellipsoids principal axes with the device coordinate axes causes the effective mass to become a 3×3 tensor quantity in the device coordinate system [See97].

The case of silicon (100) wafers devices is substantially simplified by the fact that the principal axes of the sixfold-degenerate conduction-band ellipsoids are aligned along the device coordinates axes, effectively decoupling the kinetic energy along the device coordinate axes. In general, however, the principal axes of the conduction band ellipsoids are not aligned with the device axes so that the associated kinetic energies becomes coupled and the EME equation becomes non trivial.

Such situation arises for transistors that employ germanium as a high-mobility material as well as for alternative wafer orientation.

Following the procedure depicted in Ref. [RLG05], the following evaluation method for the effective-mass has been implemented in our simulators for arbitrary oriented devices.

The matrix R_{CD} transforms the device coordinate system (DCS) into the crystal coordinate system (CCS). Each column defines direction of transport, "x", transversal, "y" and confinement, "z":

$$R_{CD} = \begin{pmatrix} \hat{x}_x & \hat{y}_x & \hat{z}_x \\ \hat{x}_y & \hat{y}_y & \hat{z}_y \\ \hat{x}_z & \hat{y}_z & \hat{z}_z \end{pmatrix} \tag{1.5}$$

The matrix defining the transformation from the device axes to the ellipse coordinate system is calculated through the matrix product:

$$R_{ED} = R_{EC} R_{CD} \tag{1.6}$$

R_{EC} establish the transform from the crystal coordinate system to the ellipse coordinate system; for the Δ valleys case, these matrix are given by:

$$R_{EC}^{\Delta_1} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{pmatrix} \tag{1.7}$$

$$R_{EC}^{\Delta_2} = \begin{pmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{pmatrix} \tag{1.8}$$

$$R_{EC}^{\Delta_2} = \begin{pmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{pmatrix} \tag{1.9}$$

The inverse effective-mass tensor on the device coordinate system is:

$$\left(M_D^{-1}\right)_{ij} = \frac{(R_{ED})_{1i}\,(R_{ED})_{1j}}{m_l} + \frac{(R_{ED})_{2i}\,(R_{ED})_{2j} + (R_{ED})_{3i}\,(R_{ED})_{3j}}{m_t} \tag{1.10}$$

where m_l and m_t are the longitudinal and transversal effective-masses. For silicon in the Δ valleys:

$$m_l = 0.91 \tag{1.11}$$

$$m_t = 0.19 \tag{1.12}$$

It should be noticed that there exists one M_D^{-1} tensor for each valley because the R_{EC} matrix is different in each valley.

Using the values of M_D^{-1}, the effective masses in each direction and in each valley can be obtained. Calling $m_{ij}= (M_D^{-1})_{ij}$, we have:

for the "x" transport axis:

$$m_x = \frac{1}{\frac{1}{m_{11}} - \frac{m_{33}}{m_{31}^2}} \tag{1.13}$$

for the "y" transversal axis:

$$m_y = m_2^{''} \tag{1.14}$$

$$\frac{1}{m_2^{''}} = \frac{1}{m_2^{'}} - \frac{m_1^{'}}{m_{12}^{'2}} \tag{1.15}$$

$$\frac{1}{m_2^{'}} = \frac{1}{m_{22}} - \frac{m_{33}}{m_{23}^2} \tag{1.16}$$

$$\frac{1}{m_{12}^{'}} = \frac{1}{m_{12}} - \frac{m_{33}}{m_{23}m_{31}} \tag{1.17}$$

and for the "z" confinement axis:

$$m_z = m_{33} \tag{1.18}$$

Special attention must be paid in the numerical implementation to avoid dividing by zero in the previous equations.

The flowchart of the software implementation for the effective mass calculation is shown in Figure 1.3.

1.3 Poisson-Schrödinger Self-Consistent solver

For the self-consistent numerical solution of the Poisson and Schrödinger equations we made use of a non-uniform adaptive mesh and for the device structure an iterative Newton numerical scheme. These equations are also solved inside the dielectric layer in order to take into account the wavefunction penetration effect,

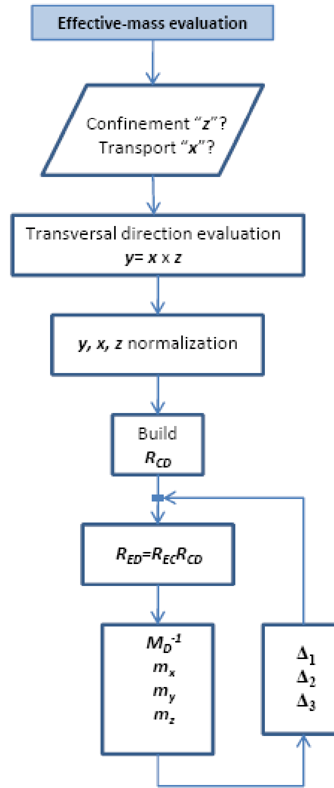


Figure 1.3: Flowchart for the effective-mass evaluation.

i.e., the non-zero value of the electron probability density inside the insulator.

The penetration of the wavefunctions inside the oxide has an important effect on the charge distribution as shown in Ref. [MR01], [HK02]. The wavefunction penetration inside the gate insulator is a function of the barrier height between the silicon and the insulator [HK04]. This means that when different insulator materials are used (this is becoming popular with the use of high-k materials), the wavefunction penetration, and therefore the centroid, will depend on the insulator used. However, in actual MOSFET devices there is usually a thin silicon dioxide layer between the silicon and the high-k dielectric in order to improve the quality of the interface. This means that the potential barrier seen from the silicon to the

dielectric is in fact the barrier of the silicon dioxide. Following the work of Mudanai et al. (Figure 4 in Ref. [MR01]) it is shown that the electron distribution (and therefore the centroid) does not depend on the oxide thickness if the same material is used (SiO_2).

To accurately model the polysilicon depletion effect, the free-carrier density in the polysilicon region is described by Fermi–Dirac statistics and a complete ionization model [SAS06]. As usual, very high doping concentrations have been considered in the polysilicon gate. However, the assumption of incomplete or complete ionization of impurities in the poly-gate does not have an important influence on the results in the inversion region of operation. The band-bending in the polysilicon at the interface poly-oxide makes all the impurities to be ionized in the poly depletion region (regardless of the assumption of complete or incomplete ionization used). Some simulations have been repeated using a incomplete ionization model, and the only effect we have found is a slight modification of the flat band voltage (this agrees with the results published by Watanabe and Takagi [WT01]).

A non-parabolic band model was utilized for the silicon conduction band. The Kane model is used, and a parameter α, for including non-parabolicity in the $E(k)$ dispersion relationship, Ref. [FL93]. Non-parabolicity parameter is taken into account in the evaluation of the two dimensional density of states (DOS) as explained in Ref. [LVGM+93], and in the solution of the Schrödinger equation following the procedure developed in Ref. [LVMJT93].

Silicon effective masses are calculated for the specific crystallographic orientations in every case, following the procedure depicted in Section 1.2. The procedure developed in reference [RLG05] does not consider non-parabolicity effects. However, as mentioned above, the non-parabolicity correction is an "a posteriori" empirical correction in the model. Therefore, we applied the procedure developed in Ref. [RLG05] to calculate the corresponding effective mass for our system (i.e. for the chosen crystallographic and channel orientations) assuming parabolic bands. Then, a correction factor α, is empirically added following Kane's model and the procedure explained above:

$$E(1+\alpha E) = \frac{\hbar^2 k^2}{2m_{eff}} \tag{1.19}$$

The non-parabolicity factor has been considered to be the same regardless of the crystallographic orientation ($\alpha = 0.5eV^{-\mathbf{1}}$) in the present work [FL93]. However, as shown by Yamaji et al. [YTH96], the non-parabolicity parameter, α, could have an anisotropic behavior. In any case, the non-parabolicity correction is not going to be very important in our results since we are considering here equilibrium properties (centroid, gate-channel capacitance, etc.).

1.4 Conclusions

In this chapter a brief review of the quantum mechanical description of the MOSFET structure was depicted. The Poisson-Schrödinger self-consistent solver used along this work was introduced and the effective mass evaluation method implemented for arbitrarily oriented devices was explained.

Chapter 2

Crystallographic orientation influence on static properties

2.1 Introduction

In state-of-art devices, gate-oxide thickness approaches T_{ox}=*1nm*, and classical MOSFET models are not good enough to reproduce the total channel charge Q_{inv} (which in other words determines the drain-current) or the inversion capacitance C_{gc} (which contributes to the transconductance of the device)

The total electron charge in the inversion layer is classically given by:

$$Q_{inv} = C_{ox}\left(V_G - V_{FB} - \psi_s - \frac{Q_D}{C_{ox}}\right) \tag{2.1}$$

where V_G is the gate voltage, V_{FB} the flat-band voltage, ψ_s the surface potential, C_{ox} the oxide capacitance and Q_D the depletion charge in the silicon substrate [Tsi99]. The classical model (Equation 2.1) reproduces with accuracy the inversion charge for thick oxides, but it fails when small oxide thicknesses are used as a consequence of quantum effects, which must be taken into account in the models.

Figure 2.1 shows the inversion charge versus the gate voltage in a Metal-Oxide-Semiconductor (MOS) structure for two values of the gate-oxide thickness (the thicker, T_{ox}=*40nm*, right-hand side and the thinner, T_{ox}=*1nm*, left-hand side). The substrate doping was considered to be $N_A=10^{17}\,cm^{-3}$, and a n^+-polysilicon gate was

assumed with a doping concentration of N_{D-poly}=$10^{20}cm^{-3}$. Closed squares are calculated from the self-consistent solution of Poisson and Schrödinger equations in the MOS structure, while open triangles are obtained using Equation 2.1.

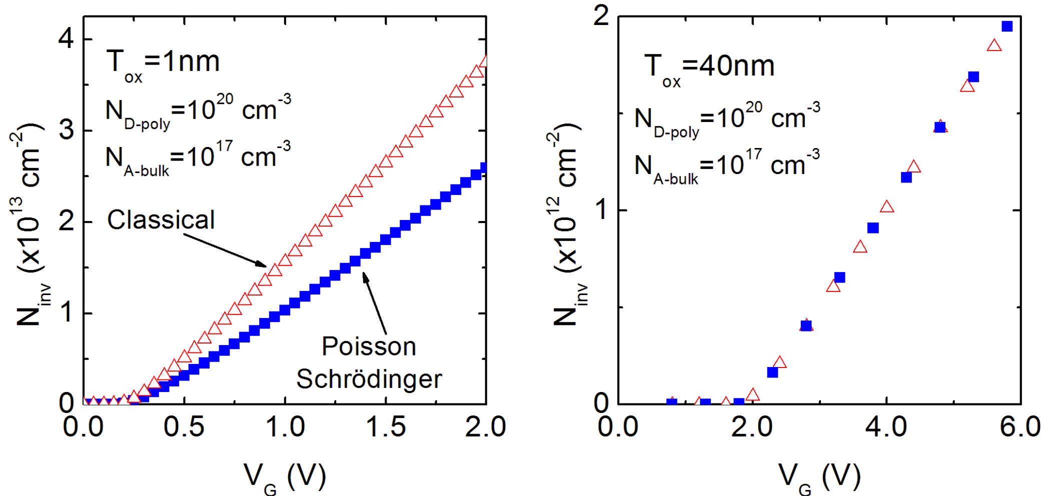


Figure 2.1: Electron density versus gate voltage in a MOS structure for two values of the gate oxide thickness. Classical modeling (Expression 2.1, open symbols) fails dramatically when oxide thickness is reduced due to inversion charge penetration in the silicon bulk and polysilicon depletion effect. Closed symbols are calculated from the self-consistent solution of Poisson and Schrödinger equations.

Having a look to Figure 2.2 will help us to determine the reasons for this behavior. This figure shows the charge distribution in a MOS structure, both in the silicon bulk and in the polysilicon gate, obtained from the self-consistent solution of Poisson and Schrödinger equations. The oxide thickness was assumed to be $T_{ox} = 1nm$, the silicon doping $N_A = 3 \times 10^{18}cm^{-3}$, $N_{D-poly} = 10^{21}cm^{-3}$, and $V_G = 2.4V$. The bulk region extends from $z = 0$ to positive values.

Figure 2.2 shows two important effects which are ignored in classical models and which are responsible for the inaccurate behavior of Eq. 2.1 when the oxide thickness approaches 1nm:

1. It is well known that as a consequence of quantum effects, electron density does not reach its maximum at the oxide-semiconductor interface but inside

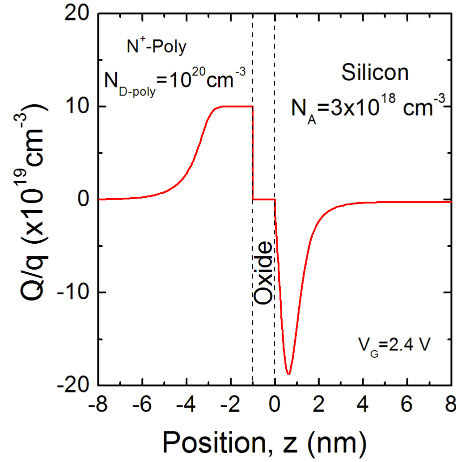


Figure 2.2: Charge distribution in a MOS structure obtained from the self consistent solution of Poisson-Schrödinger equations.

the semiconductor, while it almost vanishes right at the interface. If $n(z)$ is the 3D electron density in the inversion layer, the average penetration depth is defined as:

$$Z_I \equiv \frac{\int z\, n(z)dz}{\int n(z)dz} \tag{2.2}$$

2. Figure 2.2 also reveals the formation of a depletion layer (positive charge) near the polysilicon/SiO_2 interface [ARH98]. As a consequence of this charged layer, the poly-gate is a non-equipotential area, and there is a voltage drop in the gate. In fact, some authors have modeled this effect by taking into account the voltage drop in the polysilicon gate [HS90]. This effect produces a decrease in the channel charge and a decrease in the gate-to-channel capacitance (Figure 2.3). However, it will be shown that the polysilicon depletion effect can also be modeled as an increase in the effective gate oxide thickness and thus a reduction in the device drain current [HA93] and transconductance.

These effects were known early and have been considered by the modelling

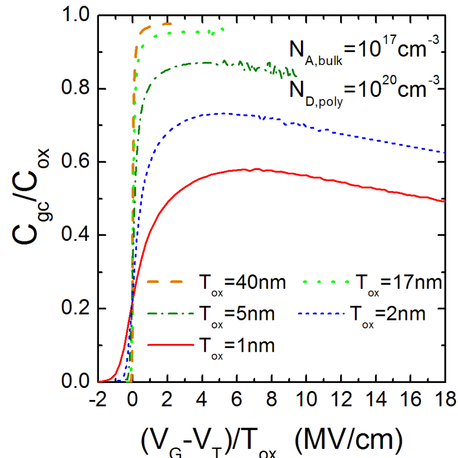


Figure 2.3: Gate-to-channel capacitance versus $(V_G - V_T)/T_{ox}$ in a n-channel MOSFET for various gate-oxide thicknesses.

community. In particular, the effect of polysilicon depletion has been modeled by [ARH98], [HS90], [HA93], [LLP+92], [LBT99]. Classical models worked reasonably well with previous generations of transistors. In those transistors, gate oxides were relatively thick ($T_{ox} > 10nm$), and therefore, most of the gate voltage drop was produced in the oxide, making the error in the interface potential relatively unimportant since the average distance of the electron density from the interface, the inversion layer centroid, Z_I, and the poly depletion region width, $Z_{D,}$ were small compared to the oxide thickness, T_{ox}. However, when gate oxide is scaled down, both Z_I and $Z_{D,}$ become comparable to T_{ox}, and therefore their effects must be incorporated in accurate models for the inversion charge, Q_{inv}, and gate-to-channel capacitance, C_{gc}.

The inversion layer centroid, Z_I, shows the influence of quantum effects on the inversion charge distribution. These quantum effects depend on the semiconductor effective mass perpendicular to the $Si - SiO_2$ interface, m_z [TT95], [Ste72], [Ste70]. In addition, m_z depends on the surface orientation [TT95], [SH70], [Ste72], [RLG05]; therefore quantum effects depend on the surface orientation. To show this, Figure

2.4 represents Z_I (calculated by self-consistently solving Poisson and Schrödinger equations and equation 2.2) as a function of the total inversion charge concentration for the three common surface orientations (100), (110) and (111). Note that smaller Z_I values are obtained for the (100) orientation, since in this orientation a higher perpendicular effective mass is obtained, $m_z = m_l$. Silicon effective masses are calculated for the specific crystallographic orientations in every case, following the procedure depicted in the previous chapter. The values of the effective mass tensor used in the calculations are presented in Expressions 2.3, 2.4, 2.5. Note that the rows (representing each valley) are ordered with the minor effective mass for the z direction (the confinement direction; third column).

$$\mathbf{m}_{eff}^{(100)} = \begin{pmatrix} 0.916 & 0.190 & 0.190 \\ 0.190 & 0.916 & 0.190 \\ 0.190 & 0.190 & 0.916 \end{pmatrix} \tag{2.3}$$

$$\mathbf{m}_{eff}^{(110)} = \begin{pmatrix} 0.916 & 0.190 & 0.190 \\ 0.190 & 0.553 & 0.315 \\ 0.190 & 0.553 & 0.315 \end{pmatrix} \tag{2.4}$$

$$\mathbf{m}_{eff}^{(111)} = \begin{pmatrix} 0.232 & 0.553 & 0.258 \\ 0.232 & 0.553 & 0.258 \\ 0.432 & 0.190 & 0.258 \end{pmatrix} \tag{2.5}$$

Once more, this dependence on the crystallographic orientation is not captured by classical models, making them, inadequate for current devices.

Interest in using different crystallographic alignments to augment Si field-effect transistor (FET) performance has been described recently [YIS+03], [IKKT04]. Here, the fabrication of hybrid substrates with different crystal orientations is suggested, since hole mobility is more than doubled on (110) silicon substrates with current flow direction along ⟨110⟩ in comparison with conventional (100) substrates and ⟨100⟩ channels [YIS+03]. This fact has given rise to a new kind of technology based on transistors fabricated in different crystal orientated substrates, HOTs (Hybrid Orientation Transistors) [YCC+06]. In this context, the study of channel orientation can be included in the optimization processes linked to the design of the

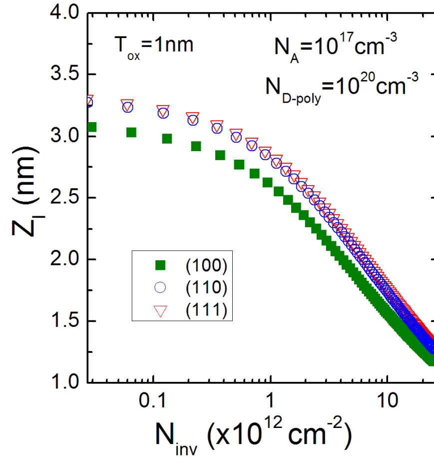


Figure 2.4: Inversion charge centroid versus the inverson electron concentration in a MOS structure for three common silicon crystallographic orientations.

transistor gate and full advantage can be taken of carrier mobility dependence on surface orientation [Van06]; in this respect, choosing the best orientations in terms of mobility suggests that the introduction of new materials could be delayed for some time. The study of MOSFET devices fabricated in arbitrary crystal orientated substrates is also interesting in relation with new devices like DG-MOSFETs and FinFETs, where different channel orientations can be found in the same film [LIT+03], [LMI+04]. A mobility study of these devices will be presented in Chapter 8.

The effect of the inversion layer centroid also has to be considered in the modelling of gate-to-channel capacitance, C_{gc}. It has a significant influence on the performance of scaled MOSFETs with thin gate oxides [TT95] since it determines the transconductance of the MOSFET. According to the classical model and with the channel operating in the inversion region, C_{gc} should approach its maximum value, i.e., $C_{gc,\max} = C_{ox}$, given by:

$$C_{ox} \equiv \frac{\epsilon_{ox}}{t_{ox}} \tag{2.6}$$

However, in the inversion condition, C_{gc} is generally given by

$$C_{gc} = \frac{\partial Q_{inv}}{\partial V_G} = \left(\frac{1}{C_{ox}} + \frac{1}{C_{inv}}\right)^{-1} \tag{2.7}$$

where Q_{inv} is the inversion charge; therefore, C_{gc} is the series combination of the gate oxide and the inversion capacitance, C_{inv},

$$C_{inv} = \frac{\partial Q_{inv}}{\partial \psi_s} \tag{2.8}$$

ψ_s being the surface potential. According to Ref.[TT95] there are two physical limitations to C_{inv},

1. the finite effective density of states (DOS) of the conduction band,
2. the finite inversion layer thickness, due to the quantum behavior of the inversion layer. As the gate oxide thickness decreases pushed down by the device scaling rules, C_{ox} increases making it comparable to C_{inv}, and as a consequence, C_{gc} becomes significantly lower than C_{ox}:

On the other hand, if we study the effect of the substrate orientation on C_{gc}, Figure 2.5 shows the low-frequency gate-to-channel capacitance obtained from the self-consistent solution of Poisson and Schrödinger equations for different confinement directions. The penetration of the inversion charge inside the bulk degrades C_{gc}, and the values obtained for C_{gc} are much smaller than C_{ox}, as T_{ox} decreases [LBT99]. This important effect of the substrate crystallographic orientation agrees with the experimental results of Takagi et al [TT95]. As can be seen, the values of the C_{gc} associated to the (100) crystallographic orientation are greater than for the (110) and (111) orientations. This is due to the lower values of the inversion charge centroid obtained for the (100) orientation (see Figure 2.4), and this fact is related to the higher confinement effective mass (the effective mass perpendicular the interface) in the (100) orientation [RLG05]. All these effects should be taken into account in MOSFET models if one wants to reproduce the experimental behavior of today's devices [LVCCB+97].

However, as mentioned above, this is not the only effect we have to deal with when oxide thickness is reduced: the use of highly doped polysilicon gates is a great

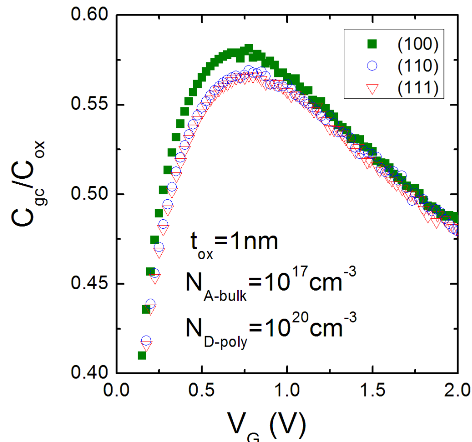


Figure 2.5: Gate-to-channel capacitance versus the gate voltage in an ultrathin-gate-oxide NMOSFET for various silicon crystallographic orientations. As shown, C_{gc} is greater for the (100) crystallographic orientation due to the lower value of the centroid of the inversion charge associated with this orientation.

advance in CMOS technology, since it allows the source and drain regions to be self-aligned to the gate, thus eliminating parasitic effects from overlay errors [TN98]. Not all the effects are beneficial however, since the use of a polysilicon gate can also cause various problems which seriously limit the operation of ultrashort devices [GGR+03], [GF03].

The first negative effect of poly-depletion is the appearance of an additional capacitance in series with the oxide capacitance. This fact limits the total capacitance of the structure in inversion and leads to a reduced inversion charge density and therefore to a degradation of the MOSFET transconductance. When the substrate becomes inverted, and therefore the poly-gate becomes depleted, the capacitance of the polysilicon in depletion adds to the oxide capacitance in series, according to:

$$\frac{1}{C_{gc}} = \frac{1}{C_{ox}} + \frac{1}{C_{inv}} + \frac{1}{C_{poly}} \tag{2.9}$$

where C_{poly} is the capacitance of the polysilicon depletion region. C_{poly} is a func-

tion of the total charge in the polysilicon gate, Q_{poly}, and of the polysilicon doping concentration, N_{D-poly}. The higher the Q_{poly}, the lower the C_{poly}, and according to expression 2.9, the lower the C_{gc} [HS90], [LBT99], as observed in Figure 2.5. In this figure we see that in inversion regime, C_{gc} reaches a maximum, and instead of increasing towards C_{ox}, it decreases as V_G (i.e. Q_{inv} and therefore Q_{poly}) increases [ARH98], [GGR$^+$03]. In order to make the poly-depletion effects negligible, C_{poly} must be sufficiently greater than C_{ox}. This can be achieved by increasing the polysilicon doping concentration for a given oxide thickness, T_{ox} (which makes C_{poly} increase) or by increasing T_{ox} for a given N_{D-poly} value, which makes C_{ox} to decrease [RA94].

In summary, both the finite extension of the inversion charge inside the silicon bulk and the width of the poly-depletion region degrade the inversion charge and gate-channel capacitance in MOS structures with ultrathin oxide thickness. As a consequence, classical MOSFET models are no longer valid. However, it will be shown next that it is possible to extend the range of application of these models by means of a corrected gate-oxide thickness, T^*_{ox} which includes both the effect of the inversion layer centroid, Z_I, and the poly depletion region thickness, Z_D. To do this, we have developed an accurate model for Z_I as a function of the inversion charge concentration, the depletion charge concentration and the silicon doping concentration for the (100), (110) and (111) crystallographic wafer orientations. The validity of the model can be easily extended to other crystallographic orientations following the scheme used in this work. Similarly, we provide an expression for the depletion zone width in the polysilicon, as a function of the poly doping concentration, the inversion charge, and the silicon doping.

In order to allow the inclusion of these quantum effects in MOSFETs fabricated on arbitrarily oriented wafers we have enhanced a previous inversion layer centroid model for the conventional surface orientation (100) and in-plane channel direction $\langle 110 \rangle$ [LVCCB$^+$97]. To do this, we followed a procedure similar to the one previously developed and included the modifications needed in our quantum simulator in order to account for different surface orientations and in-plane channel directions following the steps described in [RLG05]. We made use of a MOSFET simulator including quantization to verify that the inversion layer centroid model presented works sufficiently well. The range of validity has been checked for the

doping concentrations used ($10^{17}cm^{-3} - 3 \times 10^{18}cm^{-3}$), the kind of values employed in deep-submicron devices, and for polysilicon doping concentrations ranging from N_{D-poly}=5×10^{18}cm^{-3}-5×10^{21}cm^{-3}. In such cases, thin gate oxides are used to control the threshold voltage values and consequently, corrections to their thicknesses by the average inversion layer penetration and poly-gate depletion region width are significant.

2.2 Inversion layer centroid model

The starting point for the model was the one introduced previously for bulk MOSFETs fabricated in the conventional crystallographic orientation, $Si-(100)$ [LVCCB+97]. To obtain the inversion-layer centroid, an accurate solution of the Poisson and Schrödinger equations is obtained. After the first variational calculation by Stern and Howard [SH70], these equations were self-consistently solved in the pioneering work by Stern [Ste70], [Ste72] where the most important features of the quantization were shown. The self-consistent solution has been used to obtain the electric potential, the inversion and the depletion charges, the energy of the lowest subband minima, and the inversion layer centroid as a function of the applied gate voltage or the effective electric field.

The total electron density has a shape similar to the electron density contained in the ground subband, although multisubband occupation causes the total electron density to widen, and the centroid of the total density is therefore different from the ground subband centroid. This similarity in shape is the reason for the relatively good behavior of the variational expression, which was obtained by Stern and Howard by considering occupation of the ground subband [SH70], even in the case of multisubband occupation at room temperature, as reported by several authors [TT95], [RA94]. According to this approximation, the centroid position Z_I depends on the depletion and inversion charges as:

$$Z_I = C_1 \left(Q_D + \frac{11}{32} Q_I \right)^{-1/3} \tag{2.10}$$

where Q_D and Q_I are the modulus of the depletion and inversion-charge densities per unit area, respectively, and C_1 is a fitting parameter.

A more general expression was obtained in 1997 by Lopez-Villanueva et al. [LVCCB+97] accounting for the multisubband occupation. In that case, the expression obtained for the inversion charge centroid was:

$$Z_I = Z_{IO}\left(1\frac{MV}{cm}\right)^{1/2}\left[\sqrt{\frac{Q_D}{\epsilon_{Si}}}\left(\frac{Q_D}{\epsilon_{Si}}+\frac{1}{2}\frac{Q_I}{\epsilon_{Si}}\right)\right]^{-1/3} \tag{2.11}$$

where ϵ_{Si} is the silicon permittivity and Z_{IO} is a fitting parameter.

A good agreement between the self consistent solution of the Schrödinger-Poisson equations and the model was achieved in conventionally oriented silicon MOSFETs for a value of $Z_{IO} = 1.2nm$ and for the doping concentration values we are considering here, as shown in Figure 2.6. In the previous work, the Z_{IO} parameter did not show dependencies on the substrate doping and for that reason it was considered to be a constant for the range of doping concentrations used. However, if we want to keep the same functional dependence shown in Equation 2.11 when the inversion layer centroid is plotted versus inversion charge, there is an important dependence on the doping concentration for the (110) and (111) wafer orientations.

This dependence has been taken into consideration in our model so that the simulation results can be reproduced. To do so, a doping concentration dependent term has been included in the expression of the Z_{IO} fitting parameter. The expressions obtained are the following:

$$Z_{IO}^{(100)} = 1.2\ nm \tag{2.12}$$

$$Z_{IO}^{(110)} = 1.284\left(1+\frac{N_A}{1.673\times10^{19}}\right)\ nm \tag{2.13}$$

$$Z_{IO}^{(111)} = 1.303\left(1+\frac{N_A}{1.567\times10^{19}}\right)\ nm \tag{2.14}$$

where N_A concentrations are expressed in cm^{-3}.

The inversion layer centroid has been plotted versus inversion charge at room temperature (Figures 2.7 and 2.8) for MOSFETs fabricated on (110) and (111) wafers. The data obtained using our model are plotted in symbols and the simulation results in solid lines. It can be seen that the model reproduces well the simu-

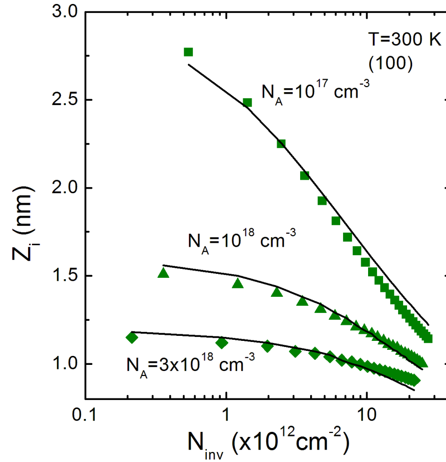


Figure 2.6: Inversion charge centroid versus the inversion charge concentration for MOSFETs on (100) wafers at room temperature for different substrate doping concentrations. The results obtained from the Poisson-Schrödinger solution are shown in solid lines, and the data calculated with the model (Eq. 2.11) are shown in symbols.

lation data for the different substrate doping concentrations and wafer orientations considered in this work.

At this point, it is important to consider why there is no dependence of the Z_{IO} fitting parameter on the substrate doping concentration in (100) wafers while this dependence is clear in the (111) and (110) crystallographic orientations. It is well known that if the doping concentration and the inversion charge are fixed, a unique potential profile is obtained, so the Z_{IO} doping concentration dependence obtained on (111) and (110) wafers is counterintuitive. The explanation for this is related to the definition of the inversion charge centroid, which is calculated taking into account that the total density of electrons in the inversion layer is:

$$n(z) = \sum_i n_i(z) = \sum_i N_i \left|\psi_i\left(z\right)\right|^2 \tag{2.15}$$

where $n_i(z)$ is the population of the *i-th* subband, N_i the density of electrons per unit area in the *i-th* subband, and ψ_i the wave function in the *i-th* subband. If

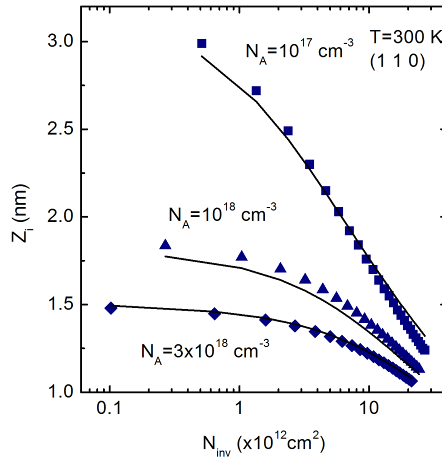


Figure 2.7: Inversion charge centroid versus inversion charge concentration for MOSFETs on (110) wafers at room temperature for different substrate doping concentrations. The results obtained from the Poisson-Schrödinger solution are shown in solid lines and the data calculated with the proposed model in symbols.

Expression 2.15 is combined with the centroid definition (Equation 2.2), we obtain:

$$Z_I = \frac{\sum_i N_i \int z_i \left|\psi_i\left(z\right)\right|^2 dz}{\int n(z)dz} \tag{2.16}$$

which is connected with the first momentum of the electron density within each subband. For the same potential well the only difference that could be found in MOSFETs fabricated on differently oriented wafers relates to the effective masses included in the Schrödinger equation and associated with each subband. Because of this, different wave functions and consequently different inversion charge centroids are expected. The function shown in squared brackets in Equation 2.11 is calculated by using the depletion and inversion charges and is based on the definition of the effective field on (100) wafers. It should probably be changed to include the particularities of the effective masses associated with the subbands in MOSFET structures

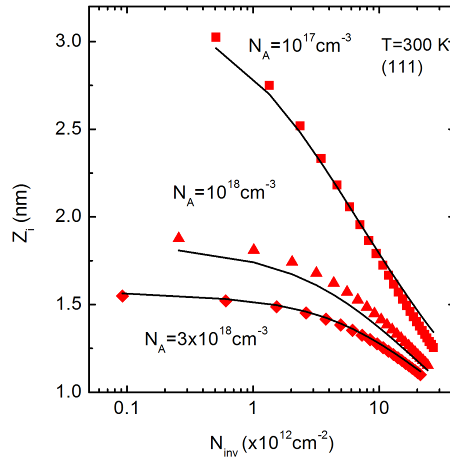


Figure 2.8: Inversion charge centroid versus inversion charge concentration for MOSFETs on (111) wafers at room temperature for different substrate doping concentrations. The results obtained from the Poisson-Schrödinger solution are shown in solid lines and the data calculated with the proposed model in symbols.

based on the (111) and (110) oriented wafers. However, we decided not to follow this strategy in order to simplify the model and retain the original algebraic expression. Therefore, in order to fit the simulation data we had to introduce a dependence on the doping concentration in the Z_{IO} fitting parameter as can be observed in Expressions 2.13 and 2.14.

The dependence of the inversion layer centroid on the transport direction for several fixed confinement orientations has been studied considering several gate voltages ($V_G = 0.2{-}1V$). To do so, the conventional transport directions for each confinement orientation have been used, i.e., [110] for (001) wafers, [001] for (110) and [$\bar{2}$11] for (111), a 90 degree rotation of the transport directions has been performed in each case, see Figure 2.9 where the first Brillouin zone showing the in-plane transport direction variation for a (110) wafer is sketched.

The simulation results for the inversion charge centroid corresponding to Figure 2.9 are shown in Figure 2.10. As can be seen, the centroid does not depend on the in-plane transport direction. The same results were obtained in all confinement

orientation directions used even in the conventional (100). Therefore the model presented can be considered valid for any channel orientation on the wafer orientations considered here. By contrast, differences will be revealed when Monte Carlo simulations are performed to study the transport since the different conductivity effective masses associated to the subbands in each in-plane transport direction will make a difference (Chapter 8).

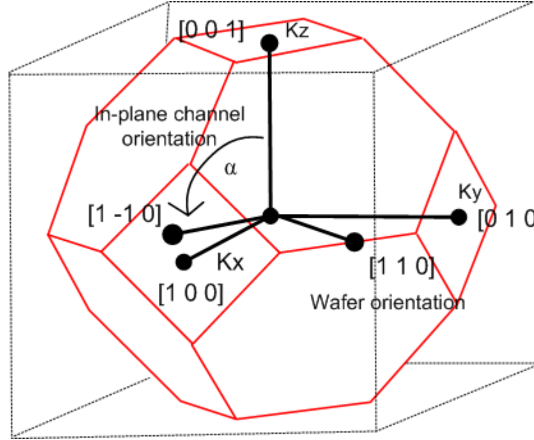


Figure 2.9: First Brillouin Zone showing the in-plane transport direction variation angle for a (110) wafer.

It is already shown in a previous work that it is possible to incorporate the effects of Z_I for the evaluation of the inversion charge concentration, Q_I, by means of a modified expression for C_{ox} [LVCCB$^+$97].

$$Q_I = C^*_{ox}\left(V_G - V_{FB} - \psi_s - \frac{Q_D}{C_{ox}}\right) \tag{2.17}$$

$$C^*_{ox} = \frac{\epsilon_{ox}}{t_{ox} + \frac{\epsilon_{ox}}{\epsilon_{Si}} Z_I} \tag{2.18}$$

This expression accurately reproduces the numerical simulation results with gate oxide thickness in the range of 10nm [LVCCB$^+$97]. When the oxide thickness is reduced to 1nm, the model given by Equations 2.17 and 2.18 only works for devices with metal gates or with very high polysilicon doping concentrations as shown in

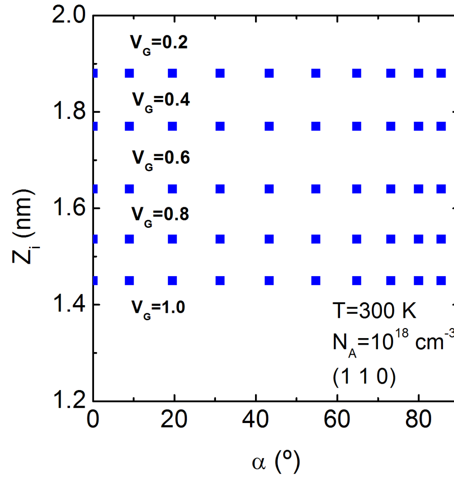


Figure 2.10: Inversion charge centroid versus in-plane transport direction variation angle for different gate voltages in a MOSFET fabricated on a (110) wafer.

Figure 2.11(a). The inversion charge is represented in a MOS structure with an oxide thickness of 1nm obtained numerically from the self-consistent solution of Poisson and Schrödinger equations (solid line) and with the classical model given by Expressions 2.1 and 2.6 (dashed line). The results provided by Expressions 2.17 and 2.18 are shown in open squares (□). The silicon doping concentration was assumed to be $N_A = 3 \times 10^{18} cm^{-3}$ and the polysilicon doping $N_{D-poly} = 1 \times 10^{21} cm^{-3}$. The oxide thickness is $T_{ox} = 1nm$. As observed, the agreement is excellent. However, the situation is considerably worse when the polysilicon doping is lower.

Figure 2.11(b) shows the same results as Figure 2.11(a) but for a polysilicon doping concentration of $N_{D-poly} = 5 \times 10^{19} cm^{-3}$. In this case, the correction given by Expression 2.18 is not enough to capture the actual behavior, as a consequence of the poly depletion effect. Therefore, the model given by Expressions 2.17 and 2.18 should be improved, taking into account the effect of the charged layer formed in the polysilicon gate, near the oxide interface.

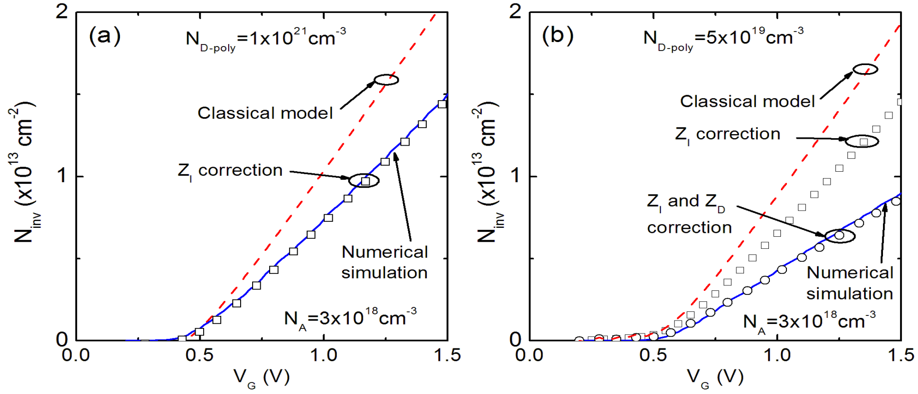


Figure 2.11: Electron concentration versus gate voltage in an n-channel MOSFET with T_{ox}=*1nm* and the following polysilicon doping levels: **(a)** N_{D-poly}=*1*$\times$*10*^{21}*cm*$^{-3}$; **(b)** N_{D-poly}=*5*$\times$*10*^{19}*cm*$^{-3}$; A comparison among different models and the self-consistent solution of Poisson and Schrödinger equations (solid line) is shown.

2.3 Polysilicon depletion effect

As shown in Figure 2.2, even in the case of a high doping concentration in the poly-gate, the polysilicon depletion region width is comparable to the inversion-charge centroid values. To take into account the effect of the charge distribution in the poly-gate, we have defined, Z_D, as

$$Z_D \equiv \frac{\int z\, Q_{poly}(z)dz}{\int Q_{poly}(z)dz} \tag{2.19}$$

where Q_{poly} is the charge distribution in the gate (see Figure 2.2). Figure 2.12 shows Z_D for different values of the polysilicon doping concentration in a MOS structure with a gate oxide thickness of $T_{ox} = 1nm$ and $N_A = 3 \times 10^{18} cm^{-3}$. As shown in Figure 2.12, Z_D is comparable to the inversion layer centroid, Z_I, and increases as N_{D-poly} decreases. These results explain why Expressions 2.17 and 2.18, which do not take into account the effect of polysilicon depletion, cannot reproduce the $N_{inv} - V_G$ curves with ultrathin gate oxides. Therefore a new correction must be

introduced to include the effects of Z_D. This is done by adding the contribution of the polysilicon depletion region, Z_D, in the same way as for Z_I:

$$C_{ox}^{*} = \frac{\epsilon_{ox}}{t_{ox} + \frac{\epsilon_{ox}}{\epsilon_{Si}}(Z_I + Z_D)} \tag{2.20}$$

Figure 2.11(b) shows that this correction is now enough to reproduce the numerical N_{inv} results even in the worst conditions, high N_A and low N_{D-poly} values. The curve with open circles accurately reproduces the results obtained from the self-consistent solution of Poisson and Schrödinger equations.

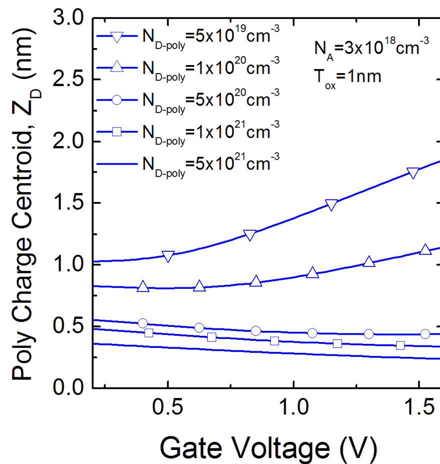


Figure 2.12: Polysilicon charge centroid in an n-MOSFET versus gate voltage, for different values of polysilicon doping.

We have evaluated Z_D by applying the Expression 2.19 to the data obtained by the self-consistent solution of Poisson and Schrödinger equations for different MOS structures with different values of the silicon doping concentration, N_A, and different values of the poly-doping concentration, N_{D-poly}. After considering different possibilities, the following model has been obtained for Z_D:

$$Z_D\left(N_A, N_{D-poly}, N_{inv}\right) \equiv Z_{D0}\left(N_A, N_{D-poly}\right)+\alpha\left(N_{D-poly}\right)\times 10^{-15}\times\left(N_{inv}\right)^{\beta\left(N_{D-poly}\right)} \tag{2.21}$$

with

$$Z_{D0}\left(N_A, N_{D-poly}\right) = 5.75\left(\frac{N_A}{10^{17}}\right)^{2.78} N_{D-poly}^{-\left(0.4+7\times 10^{-20}N_A\right)} \tag{2.22}$$

$$\alpha\left(N_{D-poly}\right) = 56 - 2.3\log\left(N_{D-poly}\right) \tag{2.23}$$

$$\beta\left(N_{D-poly}\right) = 1.65 - 0.056\log\left(N_{D-poly}\right) \tag{2.24}$$

(in Expression 2.21, Z_D is given in cm and all doping concentrations are expressed in cm^{-3}).

Using these expressions for Z_D in the model given by Equation 2.17 and 2.20 we are able to reproduce the $Q_{inv} - V_G$ curves for a wide range of N_{D-poly} and N_A values and for different silicon crystallographic orientations as shown in Figure 2.13. Solid lines correspond to the self-consistent solution of Poisson and Schrödinger equations, and symbols correspond to data obtained with the proposed model. For the sake of clarity, curves corresponding to poly doping concentrations higher than $N_{D-poly} = 5\times 10^{19}cm^{-3}$ have been vertically drifted by a fixed amount, i.e., we added $5\times 10^{12}cm^{-2}$ to the curve corresponding to $N_{D-poly} = 1\times 10^{20}cm^{-3}$ (down triangles), $1\times 10^{13}cm^{-2}$ to the curve corresponding to $N_{D-poly} = 5\times 10^{20}cm^{-3}$ (up triangles) and so on. In fact, all the curves should coincide in the lower left-hand corner of the graph.

Finally, Figure 2.14 shows that the model proposed here also takes into account the possible different crystallographic orientation of the silicon substrate. In all cases, the oxide thickness was assumed to be $T_{ox} = 1nm$.

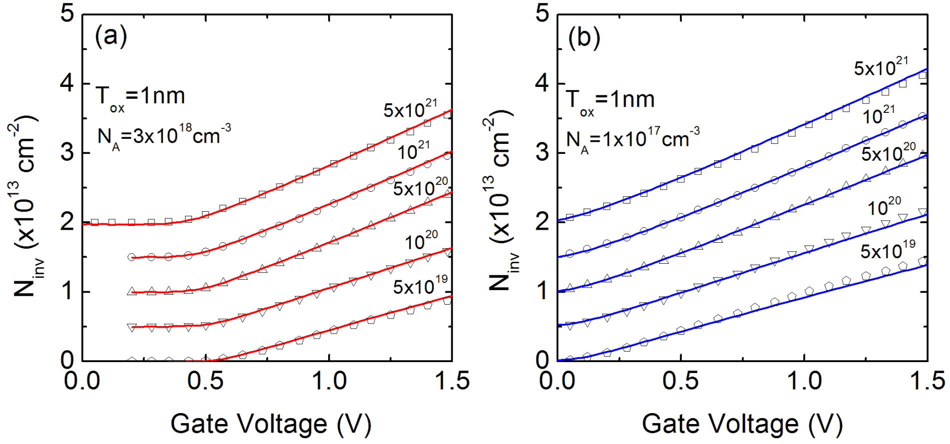


Figure 2.13: Inversion electron concentration versus the gate voltage in an n-channel MOSFET for different values of the polysilicon doping concentration. Two different values of the silicon doping concentration have been considered: (a) N$_A$ = $3 \times 10^{18} cm^{-3}$, (b) $N_A = 10^{17} cm^{-3}$ Solid lines correspond to the self-consistent solution of Poisson and Schrödinger equations, and symbols correspond to data obtained with the proposed model (Eqs. 2.20 & 2.21). For the sake of reading clarity, curves corresponding to poly doping concentrations higher than $N_{D-poly} = 5 \times 10^{19} cm^{-3}$ have been vertically drifted by a fixed amount, i.e., we added $5 \times 10^{12} cm^{-2}$ to the curve corresponding to $N_{D-poly} = 1 \times 10^{20} cm^{-3}$ (down triangles), $1 \times 10^{13} cm^{-2}$ to the curve corresponding to $N_{D-poly} = 5 \times 10^{20} cm^{-3}$ (up triangles) and so on. In fact, all the curves should coincide in the lower left-hand corner of the graph.

2.4 Gate-to-channel capacitance modelling

As mentioned in the Section 2.1, the gate-to-channel capacitance is also strongly affected by Z_I, and, Z_D, i.e., by the finite thickness of the charges in the silicon substrate and in the polysilicon gate. The effect of Z_I has already been considered in a previous work [LVCCB+97]. On that occasion, the following analytical expression for C_{gc} was provided:

$$C_{gc} \approx \left[\frac{1}{C_{ox}} + \frac{k_B T}{f \times q \times Q_I} + \frac{3}{2} \frac{Z_I}{\epsilon_{Si}} \right]^{-1} \tag{2.25}$$

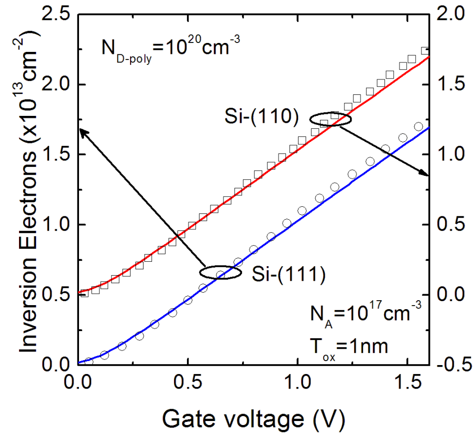


Figure 2.14: Inversion electron concentration versus gate voltage in an n-channel MOSFET for different silicon crystallographic orientations.

where f is a fitting factor depending on the bulk doping concentration, N_A and is given by:

$$f = \frac{1862}{(N_A)^{0.2}} \tag{2.26}$$

with N_A in cm^{-3}. This model was shown to be useful for oxide thicknesses down to $T_{ox} = 10nm$.

However, expression 2.25 does not take into account polysilicon depletion, and a non-negligible error is introduced, as it has already been proved. We have proposed a new empirical model with polysilicon depletion correction by adding a series capacitance term to expression 2.25:

$$C_{gc} \approx \left[\frac{1}{C_{ox}} + \frac{k_B T}{f \times q \times Q_I} + \frac{3}{2}\frac{z_I}{\epsilon_{Si}} + \eta Q_I\right]^{-1} \tag{2.27}$$

where η is given by the following relationship:

$$\eta = \frac{10^a}{[N_{D-poly}]^b}\left(\frac{V}{C^2}\right) \tag{2.28}$$

a and b parameters are obtained by fitting the model with the simulations. They show a dependence on the substrate doping, N_A, given by the following expressions:

$$a = 19.05\,(N_A)^{0.01} \tag{2.29}$$

$$b = 0.52\,(N_A)^{0.016} \tag{2.30}$$

(In expressions 2.28, 2.29 and 2.30, doping concentrations must be expressed in cm^{-3}.)

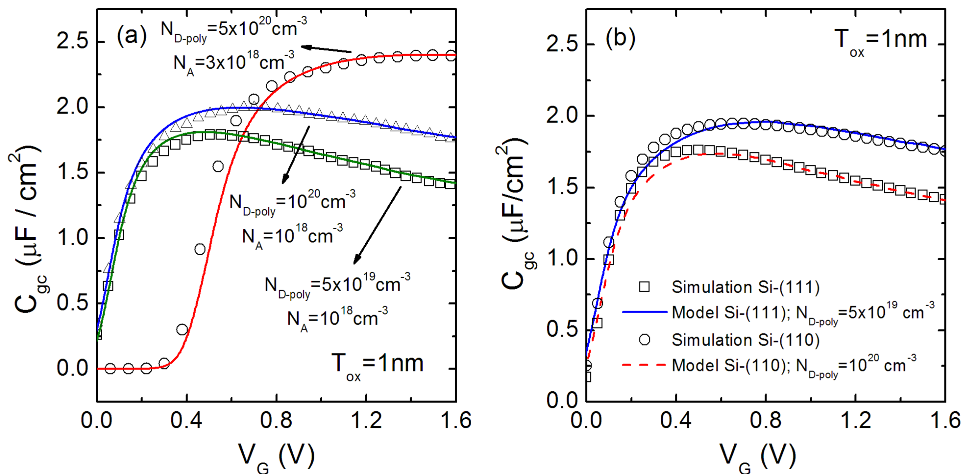


Figure 2.15: **(a)** Gate-to-channel capacitance versus gate voltage in an n-channel MOSFET with $T_{ox} = 1nm$. Solid line: model results Eq. 2.27). Symbols: simulation results. **(b)** Gate-to-channel capacitance versus gate voltage in an n-channel MOSFET with $T_{ox} = 1nm$ for different silicon crystallographic orientations ($N_A = 10^{17}cm^{-3}$).

Figure 2.15(a) shows a comparison between the modelling and the simulation results. Gate-to-channel capacitance is plotted versus gate voltage. Solid lines represent model results and numerical simulation results are plotted in symbols.

A good agreement has been obtained for N_{D-poly} ranging from $5 \times 10^{19} cm^{-3}$ to $5 \times 10^{21} cm^{-3}$, and for different crystallographic orientations (as shown in Figure 2.15(b)).

2.5 Conclusions

The influence of the inversion layer centroid and the polysilicon depletion effect on the inversion charge concentration (Q_{inv}) and the gate-to-channel capacitance (C_{gc}) of MOSFETs with gate oxides of nanometric thickness ($T_{ox} \leq 1nm$) have been studied in this chapter. The Poisson and Schrödinger equations were self-consistently solved in these devices for different values of the silicon and polysilicon doping concentrations.

Our results show important reductions of both Q_{inv} and C_{gc} because of the polysilicon depletion effect and the displacement of the inversion charge centroid from the interface towards the silicon bulk as a consequence of quantum effects, which degrade the device behavior (both drain current and transconductance are negatively influenced by these effects). The effects are very noticeable for gate oxide thicknesses around 1nm and must be taken into account in the development of accurate MOSFET models. We show that this can be done by means of a corrected gate-oxide thickness which includes both the effect of the inversion layer centroid, Z_I, and the poly depletion zone thickness, Z_D. To do so, we have developed an accurate empirical model for Z_I as a function of the inversion charge concentration, silicon doping concentration and the crystallographic wafer orientation.

The validity of the model has been checked for the three common wafer orientations (100), (110), (111). Similarly, an expression for the depletion region width in the polysilicon has been provided, as a function of the poly doping concentration and the substrate doping. Using these expressions, an effective oxide thickness, T^*_{ox} is defined, which makes possible to reproduce the actual behavior of $Q_{inv} - V_G$ for a wide range of substrate doping concentrations, polysilicon gate doping concentrations, and different crystallographic orientations in ultrathin gate oxide MOSFETs ($T_{ox} \approx 1nm$). A model which satisfactorily reproduces the gate-to-channel capacitance (C_{gc}) for these devices has also been provided.

Finally, gate-to-channel capacitance was also carefully analyzed as a function of

the substrate and poly-gate doping concentrations and silicon surface orientations.

Chapter 3

Accumulated carrier quantization and its effects on silicide-gated MOSFET

3.1 Introduction

After more than 40 years of silicon-dioxide/polysilicon gates, the industry is facing a challenging transition to higk-k/metal gate stacks. Metal gate electrodes are currently being investigated as a replacement for conventional SiO_2/poly-Si electrodes in today's shrinking devices [ITR06]. Thus, INTEL is introducing metal gates in their 45nm products [M$^+$07].

Traditionally, a polysilicon gate electrode with an overlying silicide was used for gate electrodes in CMOS devices. However as we approach to the end of the Roadmap, polysilicon gate sheet resistance and poly-depletion become serious issues [ARH98].

To overcome these problems, the metal silicided gate has been proposed as an alternative (FUSI process): a metal is deposited over the polysilicon gate; when the silicidation step takes place, the metal reacts and completely consumes the polysilicon, resulting in a fully silicided metal gate rather than a deposited metal gate [KLP$^+$05].

Accurate modeling of the quantum-mechanical charge distribution in MOSFETs has received considerable attention, resulting in analytical or semi-analytical models to correct the device characteristics. However, quantization has always been described in correspondence with the oxide/substrate interface, where considerable band bending occurs either in strong inversion or accumulation. On the other hand, the oxide/polysilicon interface has been described classically. In fact, due to its very high doping level, a small band bending occurs in accumulation, and polysilicon enters the depletion region when the device is biased in inversion. In both cases quantum effects are often taken as negligible.

Chapter 2 is extended here focussing the study on the accumulation and flat-band operation regions. A self-consistent Poisson-Schrödinger solver is used to emulate the electrical properties of silicided gates and actual metal gates by artificially extending the polysilicon doping to its metallic limit (some 10^{22}cm^{-3}) where each atom behaves like a doping atom [AM76]. Quantization of electrons and holes is accounted for in both the polysilicon and silicon layers. Schrödinger equation is solved whenever the bias conditions result in a potential well (for electrons or holes). The effective mass approximation is used on the Si-(100) surface: a) two non-primed valleys with longitudinal effective mass perpendicular to the interface, and four primed-valleys with transversal effective mass perpendicular to the interface in the case of electrons; b) heavy-holes, light-holes and split-holes model for the valence band when the quantization of positive carriers is taken into account [SH70].

3.2 Higher polysilicon doping

In Section 2.1 essential non-metallic effects to predict the behavior of the state-of-art devices with gate-oxide thickness approaching to $T_{ox} = 1nm$ where described [LVCCB+97], [TT95], [RGR07]. Those limitations (basically the inversion layer centroid and the polysilicon depletion) are intrinsic problems when the device is operated in inversion. However, there exits another non-classical effect not taken into account in the classical MOSFETs models when the device is operated in accumulation or at flat band condition: the quantization of the majority carriers both in the polysilicon and in the substrate.

The presence of an abrupt potential barrier at the polysilicon/SiO_2 interface

causes the drop of the electron concentration a few nanometers from the interface [APP99], [SPL00] even if carriers are not spatially confined. This effect, also referred to as “dark space” (see Figure 3.2), is responsible for the extraction inaccuracy in oxide thickness when ultrathin insulator devices are considered due to its strong impact on the gate capacitance. In other words, the decrease in the capacitance due to the “dark space” can be expressed as an increase in the effective oxide thickness and thus a reduction in the device drain current and transconductance of the device [APP99], [SPL00].

It is expected that metal gates (like TiN or TaC) or fully silicided gates (NiSi) will make disappear the poly-accumulation/depletion effects, but this is not really true. Even a metal gate has a finite number of atoms, and for this reason cannot be considered as an ideal metal gate. The free electron density in a metal is a factor in determining its electrical conductivity. It is involved in the Ohm’s law behavior of metals on a microscopic scale. Because electrons are fermions and obey the Pauli exclusion principle, then at 0 K temperature the electrons fill all available energy levels up to the Fermi level (the top of that "Fermi sea" of electrons").

The conduction electron population for a metal is calculated by multiplying the density of conduction electron states, $\rho(E)$, times the Fermi function *f(E)*. The number of conduction electrons per unit volume after integration in energy is [AM76]:

$$n = \frac{8\sqrt{2}\pi\left(mc^2\right)^{3/2}}{\left(hc\right)^3}\left(\frac{2}{3}E_F^{3/2}\right) \qquad (3.1)$$

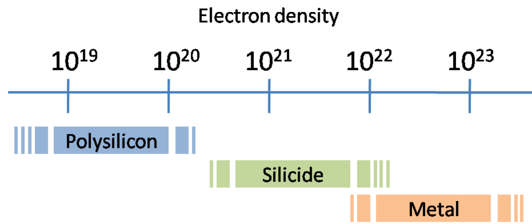


Figure 3.1: Estimated free electron density range in polysilicon, silicide and metals [AM76].

In Eq. 3.1, c is the light speed in the vacuum, m, the free electron mass and h the Planck’s constant. The direct evaluation of 3.1 yields $n=1.8\times10^{23}cm^{-3}$ for alu-

minium or $n{=}8\times10^{22}cm^{-3}$ for copper. Figure 3.1 shows the estimated free electron density rage in polysilicon, silicides and metals.

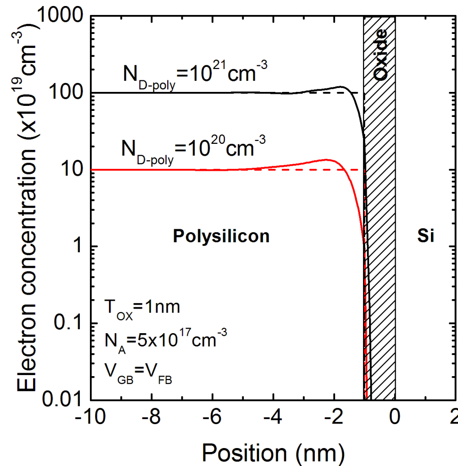


Figure 3.2: Cross section electron concentration of the Metal-Oxide-Semiconductor structure at flat-band bias for two different polysilicon doping levels. Classical solution: dashed line, full-quantum: continuous line.

Figure 3.2 shows the cross-section electron distribution of the MOS at a flat-band voltage, V_{FB}, defined here as the gate voltage needed to have space charge neutrality in the semiconductor. Classical (dashed line) and full-quantum (continuous line) solutions are presented for two polysilicon doping values. Whereas the electron distribution along the axis corresponds with the doping level for the classical solution (full ionization of doping impurities was assumed [SAS06]), the full-quantum approach reveals the presence of a dark space depleted of carriers. Since at flat-band, the total charge in the gate must be zero, the quantum electron distribution in the poly exhibits a peak (negative accumulated charge) to compensate for the positive depleted region near the interface. This charge distribution in the poly at flat-band produces a non-zero electric field, and a shift of V_{FB}.

The important consequences of non-metallic effects are especially visible when the gate capacitance curve is evaluated.

Figure 3.3 shows the simulated low-frequency gate-to-channel capacitance re-

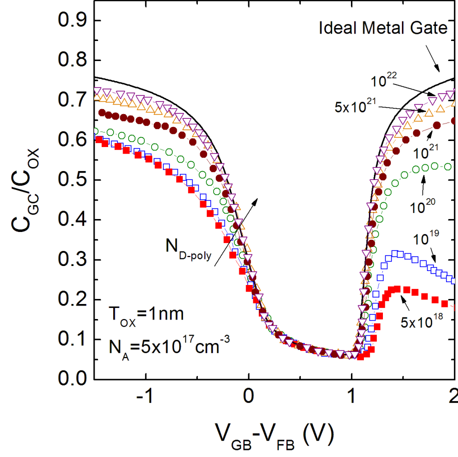


Figure 3.3: Low-frequency gate-to-channel capacitance normalized by the physical oxide capacitance for different polysilicon doping levels. Ideal metal behavior is never reproduced.

lative to the insulator capacitance for a NMOS capacitor with ultrathin-oxide of T_{ox}=1nm and substrate doping of N_A=5×10^{17}cm^{-3}, for different values of the polysilicon doping. The parasitic effects add to the oxide capacitance according to:

$$\frac{1}{C_{GC}} = \frac{1}{C_{ox}} + \frac{1}{C_{\mathrm{Si}}} + \frac{1}{C_{poly}} \tag{3.2}$$

where C_{ox} is the insulator capacitance ($C_{ox} = \varepsilon_{ox}/T_{ox}$); C_{Si} and C_{poly} the series capacitances corresponding to the non-metallic behavior of silicon and polysilicon. The capacitance reduction compared to the metal gate curve in the inversion region (positive $V_{GB} - V_{FB}$ values over 1 V), is the result of both the penetration of the inversion electron layer into the semiconductor and the polysilicon depletion. For higher doping values in the gate, the polysilicon depleted layer is reduced and C_{GC}/C_{ox} increases. In any case, C_{GC} cannot achieve the theoretical values of C_{ox} because the inversion layer centroid effect is always present.

For negative $V_{GB} - V_{FB}$, when the structure is in accumulation in both the polysilicon and substrate sides, the capacitance reduction is, essentially, the direct consequence of the polysilicon dark space and the quantization of holes accumulation

layer in the substrate. If gate non-metallic effect can be ignored (ideal metal curve in Figure 3.3), the physical oxide capacitance is not recovered ($C_{GC}/C_{ox}<1$)due to the effect of the accumulated holes in the substrate.

It is worth noting, that even for extremely high free electron density, when silicide is supposed to behave like a metal, the ideal metal gate curve is never recovered, leading to a capacitance loss around 8%. As an important consequence, the extracted physical insulator thickness tends to be overestimated in silicided gates where an ideal metal is assumed; *i. e.* when the voltage boundary condition is applied directly to the oxide.

3.3 The role of the majority carriers

Many times the role of the holes tends to be neglected or just considered minor in NMOS transistors. These statements could involve a mistake if we have to deal with the accumulation operation region of the transistors and ultrathin oxide layers. Figure 3.4(a) represents the energy-band diagram of the NMOS structure for $V_G = -2V$ (accumulation of electrons in the polysilicon and accumulation of holes in the bulk). The corresponding charge density is superposed on the bands.

As a consequence of the quantum treatment of the polysilicon, the maximum of the charge distribution is no longer at the interface. In addition, the quantum solution betrays that the holes play an important part in the substrate.

The influence of the centroid of the holes is clearly revealed in the gate-to-channel capacitance curve (Figure 3.4(b)). For $V_G > V_{FB}$, both the full-quantum solution and the classical solution for the holes yield the same capacitance values as a consequence of the negligible population of holes. The situation is quite different if $V_G < V_{FB}$, resulting in up to 15% of error.

3.4 Flat-band voltage shift

The flat-band condition is defined as the gate voltage needed to have space charge neutrality in the semiconductor ($Q_{Si} = 0$) (Figure 3.5). For uniformly doped substrates this means that bands are flat in the semiconductor. Since the total charge in the MOS capacitor must be zero and under the assumption of no trapped charge

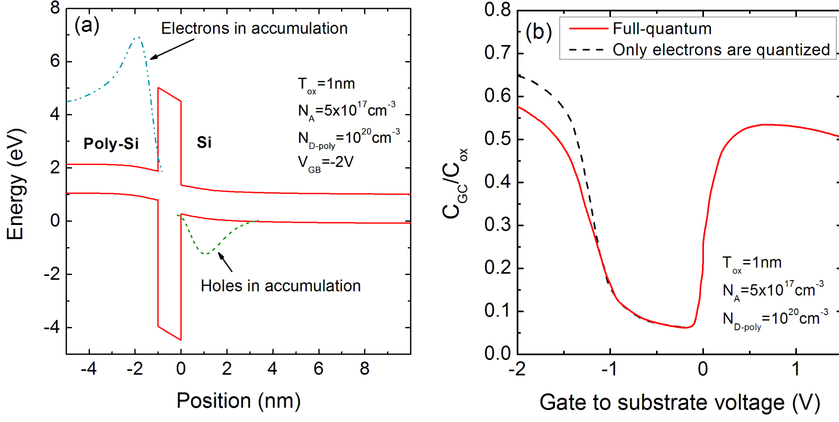


Figure 3.4: (a) Energy-band diagram (maximum of the valence band and minumum of the conduction band) of the MOS structure in accumulation for $V_G = -2V$. The corresponding charge density in superposed. (b) Low-frequency gate-to-channel capacitance normalized by the physical insulator capacitance. Classical solution for holes and quantum for electrons: dashed line. Full-quantum: continuous line.

in the oxide, $Q_{poly} = Q_{Si}$, therefore at flat band conditions, $Q_{poly} = 0$. However, this does not mean *flat* bands in the polysilicon as classical theory predicts for uniformly doped materials. In fact, the combination of high doping levels and polysilicon quantization produces interesting results. The insulator barrier at the polysilicon-SiO_2 interface induces an almost-zero majority carrier concentration at the interface ("dark space" effect) leading to an electrical dipole and therefore a non-zero electric field distribution to achieve the flat band condition, $Q_{poly} = 0$ (Figure 3.2). This effect has been previously reported by different authors [SCG02] until 10^{20}cm^{-3} poly-gate doping levels. However, exploring the physical limits of the polysilicon doping reveals new intriguing features.

The electric field in the polysilicon leads to an additive voltage drop which shifts the classical flat-band voltage up to $\Delta V_{FB} = V_{FB-cla} - V_{FB-q} \approx 200mV$.

Figure 3.6(a) presents the simulation extracted flat-band voltages for different polysilicon doping levels when classical (dashed line) and full-quantum (continuous line) approaches are used. Up to $N_{D-poly} = 10^{21}cm^{-3}$ the full-quantum solution shift, V_{FB-q}, is more noticeable than the classical solution. But once this doping

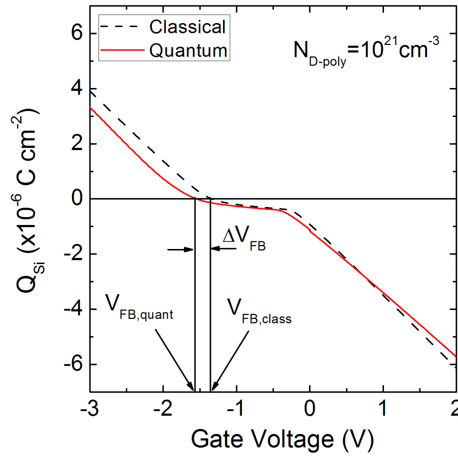


Figure 3.5: Total charge in silicon versus gate voltage for the classical (dashed-line) and full-quantum (continuous-line) solution. Flat-band voltage is defined for zero charge the silicon.

limit is exceeded both solutions tend to merge again. This is more remarkable when the difference of the flat-band voltage is plotted (Figure 3.6(b)). As reported previously ([SCG02], open circles) V_{FB-q} decreases faster than V_{FB-cla} at least up to some critical value when the trend is inverted and both V_{FB-q} and V_{FB-cla} tend towards the same value. For the sake of comparison, it is also shown in Figure 3.6(b) the quantum flat-band voltage shift in the case of an ideal metal gate. In this case, the quantum corrections are very small since the only contribution comes from the quantization of the substrate, which has a very low doping compared to the polysilicon doping values.

Although its validity has not been checked until now, this interesting effect can be analyzed using the analytical model suggested in [SCG02], where the quantum model induces flat-band. A flat band voltage shift ΔV_{FB}:

$$\Delta V_{FB} = V_q + V_s = q\frac{N_D \lambda_q^2}{2\varepsilon} + q\frac{N_D \lambda_q \lambda_s}{\varepsilon} \tag{3.3}$$

where V_q represents the voltage drop in the dark-space region and V_s the voltage

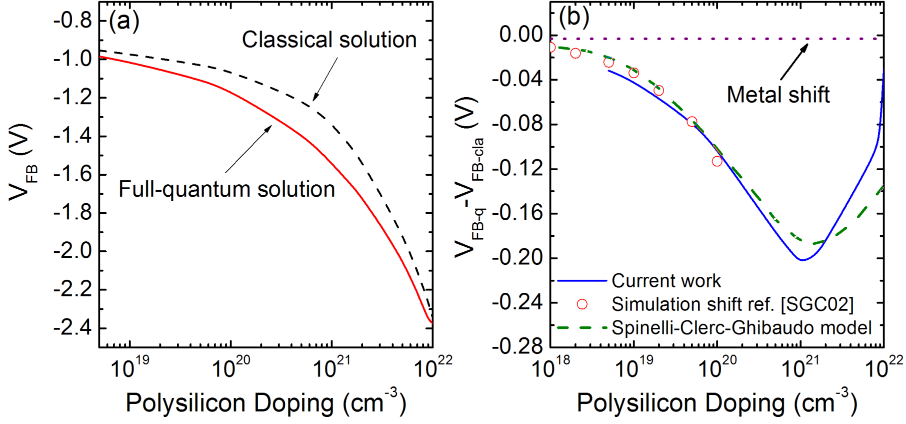


Figure 3.6: **(a)** Simulation extracted flat-band voltage for different polysilicon doping levels. Solid line: from full-quantum solution; dashed line: from classical solution. **(b)** Comparison between simulation results (continuous line and circles) and the model (dashed line) for the shift in the flat-band voltage as a function of the polysilicon doping.

drop in the remaining polysilicon region, λ_q is the carrier depleted region assumed after an exponential relaxation, and λ_s is the screening length:

$$n(x) = N_D + \Delta n e^{\frac{-(x-\lambda_q)}{\lambda_s}} \tag{3.4}$$

Using the standard carrier concentration dependence of λ_q and λ_s [SCG02] we plotted in Figure 3.7 enables a qualitatively good interpretation of the ΔV_{FB} variation with doping level to be obtained with Eq. 3.3. In particular, it explains the tendency observed at very high doping level for the ΔV_{FB} amplitude reduction (Figure 3.6). This feature can be understood by the faster decrease of λ_q^2 and $\lambda_q \lambda_s$ in Eq. 3.3 with doping concentration N_D.

The metal shift (also indicated in Figure 3.6(b)) is constant in all the doping range since the only contribution comes from the substrate (independently of the polysilicon doping).

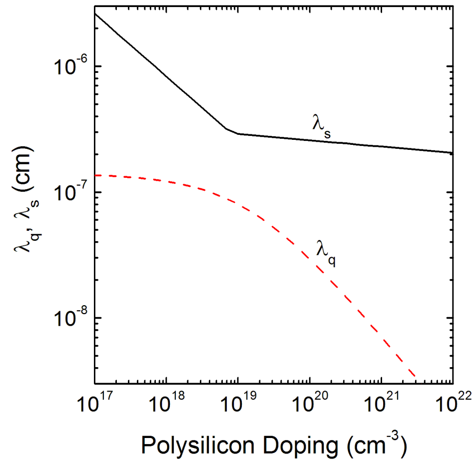


Figure 3.7: λ_q and λ_s variation as a function of the polysilicon doping.

3.5 Conclusions

The electrical behavior of MOSFETs with polysilicon gates at the silicided doping limit was studied. Poisson and Schrödinger equations were self-consistently solved throughout the structure taking into account quantization of both electrons and holes.

Although their effects are weaker than in polygate, poly-accumulation/depletion effects are still present in actual deposited and fully silicided gates. Simulations show that assuming an ideal metal behavior leads to an overestimated extracted insulator physical thickness and a capacitance loss. The important role of the holes in accumulation has been revealed. Flat-band voltage definition was revisited; different values of the flat-band voltage have been obtained for classical and full-quantum approaches, showing that both values converge on the nearly same shift as the polysilicon doping increases to the silicided limit. Finally, Spinelli-Clerc-Ghibaudo analytical model for this shift was corroborated through comparison to simulated data.

Chapter 4

Remote scattering mechanisms in ultra-thin-gate-oxide MOSFETs

4.1 Introduction

The International Technology Roadmap for Semiconductor (ITRS) imposes very hard restrictions on the gate oxide thickness of MOSFETs transistors for new technology nodes [ITR06]. As a consequence, the emerging decananometer MOSFETs technology with channel lengths of less than 50nm require oxide thickness of less than *1nm*. Such ultrathin oxide layers impose important limitations on MOSFET operation, including the following [GGR+03]:

1. Non-negligible tunnelling currents.

2. Long-range Coulomb interaction between the carriers in the channel and the ionized impurities to be found in the heavily doped areas corresponding to the gate, source and drain, which strongly reduces the mobility in MOSFETs with oxides thinner than 3nm.

3. Channel mobility decrease due to gate-oxide roughness.

4. Polysilicon depletion near the oxide interface, which produces a significant degradation of C-V characteristics (and MOSFET transconductance) if the polysilicon gate is not doped enough.

5. Remote Coulomb scattering due to the polysilicon charges, which also strongly degrades channel mobility [TT02].

These effects should be taken into consideration for an in-depth study of thin oxide MOSFETs. Among the limitations listed above, remote scattering mechanisms have been shown to play an important role on the channel mobility of the carriers [GR03]. These remote scattering mechanisms have already been introduced in previous works by means of Monte Carlo simulations [GGR+03], [GR03], [GCF+06]. However, Monte Carlo techniques are time-consuming and cannot be used in massive simulations due to the huge computational power required. In such cases, the use of analytical models is essential. The drift-diffusion approach for device simulation and the compact modelling approach for circuit simulation both depend on accurate models to describe the main physical interactions that take place in the devices (fabricated under current and future aggressive dimension reduction schemes). This is the case with remote polysilicon-oxide surface-roughness scattering and remote Coulomb scattering due to the polysilicon depletion charges. These two mechanisms are particularly relevant when the oxide thickness is reduced [GGR+03], [GR03], [GGJM+03]. Figure 4.1 shows a schematic representation of the two scattering mechanisms.

In this chapter, a model for the mobility component (obtained using the approximations related to the use of Matthiessen's rule) [Zim72] connected with these two remote scattering mechanisms is developed as a function of the oxide thickness (T_{ox}). To do this, a great number of Monte Carlo simulations have been performed in order to characterize and determine the dependences of this mobility component. Once the analytical expression for the mobility was obtained, it is used along with other well-known models to account for other mobility components, in order to reproduce the experimental results corresponding to a very thin oxide MOSFET.

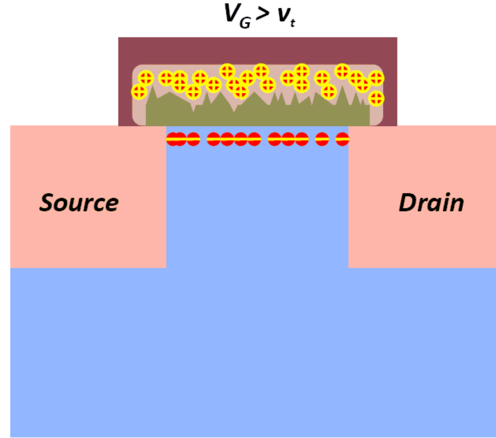


Figure 4.1: Schematic representation of the modeled scattering mechanisms. The polysilicon-SiO_2 roughness is equivalent to a change in the insulator thickness, while the depleted charges in the polysilicon cause remote Coulomb scattering.

4.2 Simulator description

A self-consistent Poisson–Schrödinger solution is developed making use of a non-uniform adaptive mesh and an iterative Newton numerical scheme for the structure. A non-parabolic band model was used for the silicon conduction band [FL93]. For more details see Section1.3.

Once the electron distribution was known, the effect of a constant longitudinal electric field, E_0, applied parallel to the $Si - SiO_2$ interface was considered by solving the Boltzmann transport equation by the Monte Carlo method [FL93]. The longitudinal electric field caused electrons to drift along the channel where they were scattered by different scattering mechanisms. The simulator includes intravalley and intervalley phonon scattering mechanisms as well as improved models to account for silicon-oxide surface-roughness and Coulomb scattering mechanisms in the channel [GR03], [FL93]. In addition, the remote poly-oxide surface-roughness scattering and Coulomb scattering due to the polysilicon depletion charges have been included [GGR+03], [GR03], [GGJM+03].

Remote interface roughness scattering is implemented in the Monte Carlo simulator, where, in addition, and simultaneously, the participation of phonon scattering,

Coulomb scattering and Si/SiO_2 interface roughness can be considered. Remote roughness scattering is assumed like a fluctuation of the oxide thickness from its average value, T_{ox}, as represented in Figure 4.2. So at a given position r in the plane parallel to the gate, it is assumed that the oxide thickness is given by

$$t_{ox}(r) = T_{ox} + \Delta(r) \tag{4.1}$$

where T_{ox} is the average oxide thickness and $\Delta(r)$ being the oxide thickness deviations from its average value, which are assumed to be correlated in an exponential law [GR03].

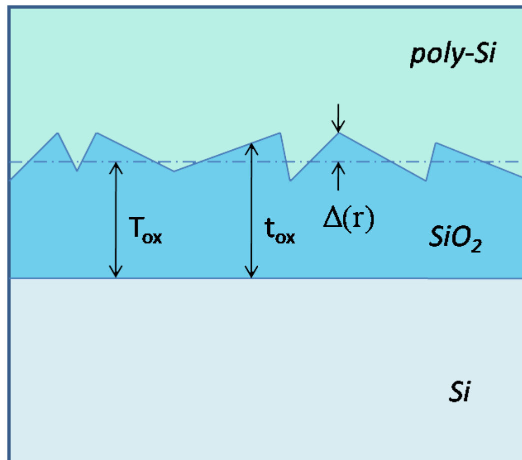


Figure 4.2: Schematics of the polysilicon-oxide interface roughness considered.

The basic simulated structure consisted of a conventional NMOSFET with an NPOLY gate with a doping concentration ranging from N_{D-poly}= $6 \times 10^{19} cm^{-3}$ to $10^{20} cm^{-3}$. The substrate doping concentration ranged from N_A= $3 \times 10^{16} cm^{-3}$ to $5 \times 10^{17} cm^{-3}$. This high doping permitted a reasonable control of short channel effects as the dimensions of the transistors were scaled down. The oxide thicknesses used were in the range of T_{ox} = 0.8 nm to 1.5 nm.

4.3 Remote scattering model

The important role that remote scattering mechanisms play in the channel mobility calculation is sketched in Figure 4.3. A comparison between Monte Carlo simulated mobility curves with and without remote scattering mechanisms is illustrated. A substrate doping concentration of N_A= $5 \times 10^{17} cm^{-3}$, and a polysilicon doping concentration of N_{D-poly}=$10^{20} cm^{-3}$ is assumed. The parameters for the surface roughness scattering were considered to be L_{sr} = *1.5 nm*, Δ_{sr} = *0.185 nm*, at both interfaces (polysilicon–SiO_2 and SiO_2–Si).

In the first group of curves (where remote scattering mechanisms are neglected) there is no oxide thickness dependence and all the curves merge (solid lines). However, when remote scattering mechanisms are included, the behavior of the mobility curves is different. As can be seen, the mobility drops at low and medium effective fields (0.5-1.5 MV/cm) as the oxide thickness is reduced.

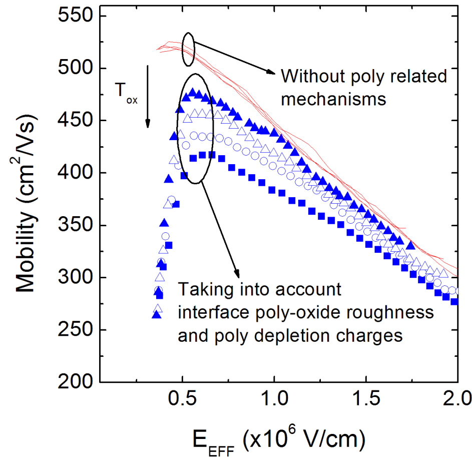


Figure 4.3: Electron mobility versus effective field for the MOSFET devices used. The mobility curves plotted in symbols are calculated taking into account the surface-roughness of the polysilicon–oxide interface as well as the polysilicon depletion charge by means of the remote surface-roughness and Coulomb scattering mechanisms. The curves shown in lines are calculated by neglecting these mechanisms. T_{OX}= 0.8 nm (■), T_{OX}= 1.0 nm (o), T_{OX}= 1.2 nm (△), T_{OX}= 1.5 nm (▲).

For the sake of clarity, Coulomb scattering due to substrate doping is not considered in these curves. As known, Coulomb scattering has a big impact on the mobility at low vertical effective fields, and looses its importance as the inversion charge concentration increases because of the screening by mobile carriers [FL93], [TIT94], [JR83]. When substrate doping concentration is high, it is seen that Coulomb scattering effects produced by the substrate doping partially mask the role of remote scattering mechanisms [GGJM$^+$03]. However, the contribution of Coulomb scattering produced by the substrate doping will have to be taken into account if one wants to reproduce experimental results (see Section 4.4 and Figure 4.7).

The different scattering mechanisms considered here (remote surface-roughness and remote Coulomb scattering due to the polysilicon depletion charges) play different roles depending on the effective field considered. Figure 4.4 shows mobility curves calculated by using these mechanisms independently. The following procedure was applied: to evaluate the mobility curve labelled 'remote interface roughness' ($\triangle$), we first calculated (using the Monte Carlo simulator) the phonon-limited mobility curve (i.e. assuming phonon scattering as the only scattering mechanism). We then calculated another mobility curve, but now when phonon and remote interface roughness scattering were simultaneously taken into account. Finally, the Matthiessen's rule is applied to both curves to extract the mobility limited by remote interface roughness. The same procedure is used to evaluate the rest of curves in Figure 4.4, activating the corresponding scattering mechanisms in the Monte Carlo simulation, and applying Mathiessen's rule to the resulting mobility curve and the phonon-limited mobility to isolate the contribution of the desired scattering mechanism.

As can be seen, remote surface-roughness is only predominant at low fields. Indeed it can be considered as a variation on the oxide thickness and therefore a variation on the threshold voltage; however, this is the most interesting effective field range to study because at higher fields other scattering mechanisms such as phonon and substrate-oxide surface-roughness play a major role [TT02]. By comparison, remote Coulomb scattering is rather constant with vertical field.

Having seen the results, an in-depth study to characterize and model the effects of these remote scattering mechanisms on the total channel mobility was performed. In particular, an analytical expression for the mobility as a function of the gate-oxide

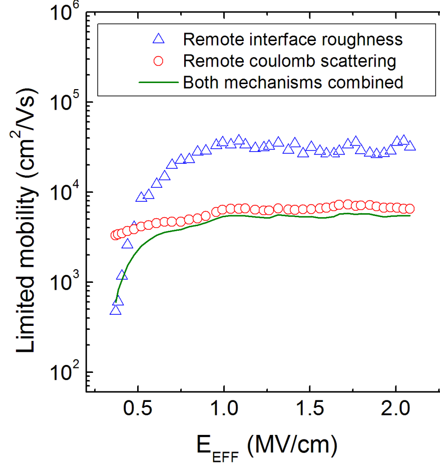


Figure 4.4: Mobility versus electric field showing the distinct remote scattering mechanisms obtained by means of Mathiessen's rule for a MOS structure ($N_{\text{D-poly}}$ $=10^{20}\,cm^{-3}$, $N_{\text{A}}=5\times10^{17}\,cm^{-3}$, $L_{\text{sr-remote}}$ $=$ $1.5nm$, $\Delta_{\text{sr-remote}}$ $=0.185nm$). Open triangles: remote surface-roughness scattering. Open circles: remote coulomb scattering.

thickness for heavily doped MOSFETs with ultra-thin oxides was developed. This is carried out using Mathiessen's rule whereby the following scattering processes were considered: phonon scattering (μ_{ph}), Si–SiO$_2$ surface-roughness scattering (μ_{sr}) and remote scattering (μ_{re}), including in this last component both remote polysilicon depletion charge Coulomb scattering and polysilicon–SiO$_2$ surface-roughness scattering (see equation 4.2) [Zim72].

$$\mu^{-1} = \mu_{ph}^{-1} + \mu_{sr}^{-1} + \mu_{re}^{-1} \tag{4.2}$$

For the sake of clarity, Coulomb scattering due to the substrate charges was not considered in the extraction of an analytical expression of the remote-scattering-limited mobility (μ_{re}). As explained before, Coulomb scattering due to doping impurities strongly affects the mobility at low electric fields, and thus, partially masks remote scattering effects. This makes the application of Mathiessen's rule (Eq. 4.2) a noisy procedure. To avoid this, and only for the extraction of the remote-scattering-

limited mobility model, we ignored the effect of the Coulomb scattering due to substrate doping. This procedure does not affect the extraction of μ_{re} under the assumption that the different scattering mechanisms are independent [JR83]. However, as shown in Section 4.4, this scattering mechanism will have to be necessarily taken into account in order to reproduce the experimental results.

In the course of this, we studied and characterized a great number of mobility curves. The phonon limited mobility (μ_{ph}) was calculated in order to isolate the remote (μ_{re}) and Si–SiO$_2$ surface-roughness (μ_{sr}) scattering components by means of Mathiessen's rule. After the calculation of μ_{re} for a great number of oxide thicknesses by this procedure, these curves were empirically fitted to an analytical expression given in Eq. 4.3. The remote mobility component model obtained is given in Equation 4.3

$$\mu_{re} = \frac{\exp\left(\frac{E_{EFF}-\frac{Q_D}{\varepsilon_{\mathrm{Si}}}}{b}\right)}{a + c\exp\left(\frac{E_{EFF}-\frac{Q_D}{\varepsilon_{\mathrm{Si}}}}{b}\right)} \tag{4.3}$$

where a, b and c are fitting parameters depending on temperature, substrate doping, oxide thickness, correlation length (L_{sr}) and rms values of the oxide thickness fluctuation (Δ_{sr}); they must be fitted for each technology; Q_D is the depletion charge and $\varepsilon_{\mathrm{Si}}$ the silicon dielectric constant. Equation 4.3 takes into account the strong variation of μ_{re} at low fields and also the saturation observed when the effective field rises (see Figure 4.4).

The inverse of the isolated remote scattering mobility component, μ_{re}, shown in Figure 4.5 is plotted versus $Q_I/(2\varepsilon_{\mathrm{Si}})$ following the well-known relation for the effective field (see equation 4.4) [TIT88], [TIT94]:

$$E_{EFF} = \frac{1}{\varepsilon_{\mathrm{Si}}}\left(Q_D + \frac{1}{2}Q_I\right) \tag{4.4}$$

where Q_I is the inversion charge. Due to the strong influence of remote scattering mechanisms at low effective fields, special care has to be taken in modelling this part of the mobility curve; the μ_{re}^{-1} representation plotted in Figure 4.5 is used in order to obtain greater resolution at low effective fields. Indeed, $\mu_{re}^{-1} \sim c + \exp(-Q_I)$,

which clearly shows the effect of remote scattering (c) and the screening effect of the inversion charge. The importance of the other scattering mechanisms at high effective fields in comparison with the contribution of remote scattering mechanisms makes high levels of accuracy unnecessary in modelling this part of the curve.

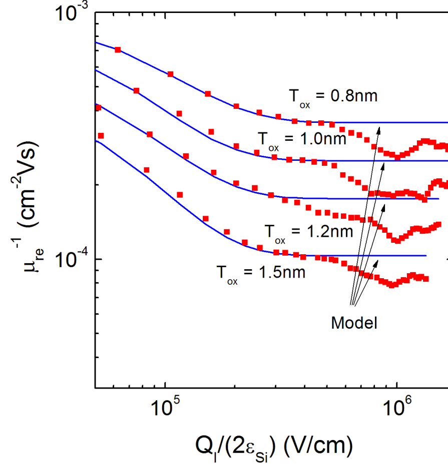


Figure 4.5: Remote scattering mobility component versus the inversion charge. Accuracy in modelling this component is only needed at low inversion charges; at high inversion charges its role is minor in comparison with other scattering mechanisms such as Si–SiO_2 surface-roughness scattering.

For the technological parameter of the simulated devices (N_{D-poly} = 10^{20} cm^{-3}, N_A= $5 \times 10^{17} cm^{-3}$, L_{sr} = 1.5 nm, Δ_{sr} = 0.185 nm) the algebraic expressions used for the set of constants included in the remote scattering model given in Equation 4.3:

$$a = -0.0071 + 0.0227T_{ox} - 0.0209T_{ox}^2 + 0.0061T_{ox}^3 \tag{4.5}$$

$$b = -671000 + 1.57 \times 10^6 T_{ox} + 1.33 \times 10^6 T_{ox}^2 + 371000T_{ox}^3 \tag{4.6}$$

$$c = 0.00148e^{-\frac{T_{ox}}{0.5632}} \tag{4.7}$$

in Equations 4.5, 4.6 and 4.7, T_{ox} is given in nm.

The validity of the model was checked not only by comparing with the Monte Carlo results for this mobility component but also by adding the different mobility components usually included in mobility models [VLPB98], making use of Mathiessen's rule and fitting experimental and simulated mobility curves. The models used for the different mobility components are as follows:

1. The Si–SiO_2 surface-roughness mobility component is described by using the analytical expression given in [MLPP99]:

   $$\mu_{sr} = \frac{\delta}{E_{EFF}^{\alpha}} \tag{4.8}$$

   where α and δ are fitting parameters depending on the temperature. The α parameter also depends on the correlation length of the SiO_2–Si surface-roughness (its value ranges from 2 to 1 at room temperature for correlation lengths from 5 to 25 Å in length) [MLPP99]. These parameters must be fitted for each technology used.

2. The phonon scattering was described in [GLV95]:

   $$\frac{1}{\mu_{ph}} = \frac{1}{\mu_{phB}} \left[\left(\frac{T}{300}\right)^{n} + \left(\frac{T}{300}\right)^{r} \left(\frac{E_{EFF}}{E_0}\right)^{\beta} \right] \tag{4.9}$$

   where T is the temperature and n and r are fitting parameters. The fitting parameters μ_{phB} and β depend on the temperature. Although the analytical expressions used to calculate their values were given in previous works, the thin oxide MOSFETs considered here and the high effective field associated with it led us to select a new set of parameters to fit the mobility values obtained for this scattering mechanism.

The results of the modelling performed by using Equations 4.3, 4.8 and 4.9 were compared with Monte Carlo simulations where phonon, Si–SiO_2 surface-roughness and remote scattering mechanisms were considered. Figure 4.6 shows the comparison between the Monte Carlo simulated mobility and the analytically calculated mobility for several oxide thickness values (N_{D-poly}=$10^{20}\,cm^{-3}$, N_A= $5 \times 10^{17}\,cm^{-3}$,

L_{sr}=$L_{sr-remote}$=1.5nm, Δ_{sr}=$\Delta_{sr-remote}$=0.185nm). As can be seen, the mobility reduction due to remote scattering mechanisms at low effective fields is now reproduced with a reasonable fit. (Coulomb scattering due to doping substrate is ignored in this figure.)

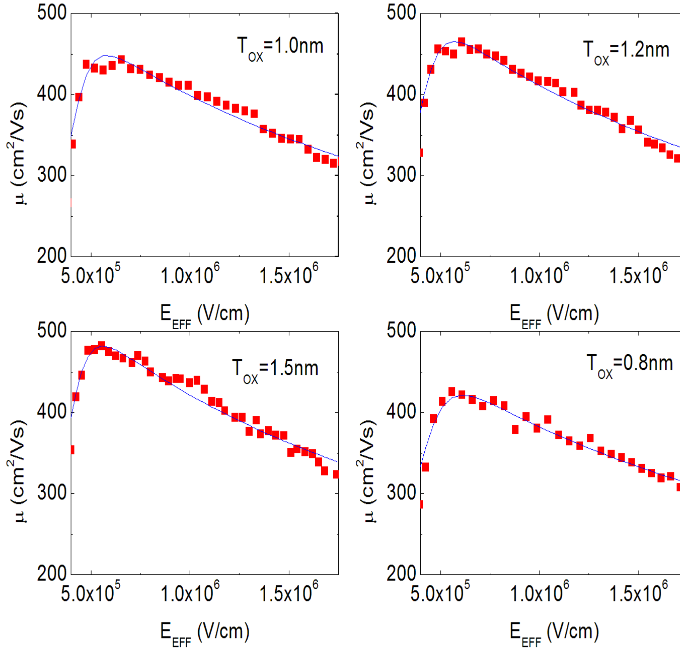


Figure 4.6: Electron mobility versus effective field for different oxide thicknesses at room temperature. Monte Carlo calculated results are shown in symbols and the data obtained using the analytical model are shown in solid lines.

It is important to note that the mobility curves calculated in this work are low-field electron mobility curves. In addition, we have used a one-electron Monte Carlo simulator. This kind of simulator does not allow us to describe the behavior of short channel devices [Tom93]. However, this does not mean that the expression obtained in this work could not be useful to simulate ultrashort devices in drift-diffusion-based simulators. In such a case, it is necessary, for example, to take into account

the effect of the longitudinal electric field [Tom93], [Sel84], [RGLV97].

4.4 Comparison with experimental results

After developing the remote scattering model, it is used along with the other mobility component models to compare with experimental data in order to check its validity. To do this, we used the electron mobility data reported by Takagi *et al.* [TT02] on T_{ox} =*1.5nm* and T_{ox}=*3.5nm* MOSFETs.

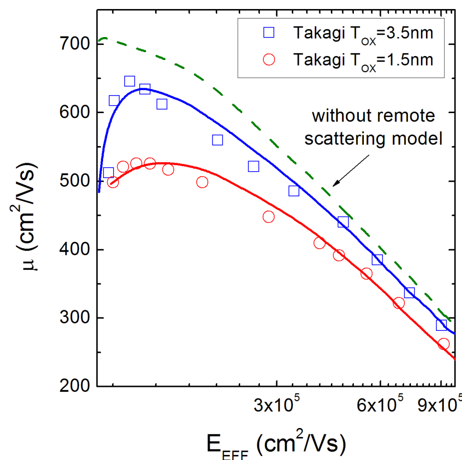


Figure 4.7: Electron mobility versus effective field at room temperature. The experimental electron mobility curves reported in [TT02] are shown in symbols. The mobility modelled including phonons, interface Si-SiO_2 roughness, Coulomb scattering, remote roughness and Coulomb scattering due to polysilicon depletion charges are shown in solid lines. The mobility modelled without taking remote mechanisms into account is shown in dashed lines. (N_A=$3\times10^{16} cm^{-3}$, N_{D-poly}= $6\times10^{19} cm^{-3}$, N_{it} = 5×10^{10} cm^{-2}, L_{sr} = *1.3 nm*, Δ_{sr}=*0.35nm*).

Firstly, the structure is simulated by using our Monte Carlo simulator and the different scattering mechanisms are modeled: phonon scattering (Eq. 4.9), substrate Coulomb scattering (which is absolutely necessary here), surface-roughness scattering (Eq. 4.8) and remote scattering (Eq. 4.3). Substrate Coulomb scattering was modelled with the model introduced by Takagi [TIT88], where mobility was con-

sidered to be linearly dependent on the inversion charge. The MOSFETs considered have the following technological features: $N_A=3\times10^{16}\,cm^{-3}$, $N_{D-poly}=6\times10^{19}\,cm^{-3}$, charge concentration at the SiO_2–Si interface: $N_{it}=5\times10^{10}\,cm^{-2}$; roughness parameters: $L_{sr}=1.3nm$, $\Delta_{sr}=0.35nm$; $T_{ox}=1.5nm$ in the first case and $T_{ox}=3.5nm$ in the second case.

Figure 4.7 shows the comparison between the experimental results and the mobility curve modeled. The experimental data are well fitted. The influence of remote scattering mechanisms can be observed by looking at the mobility curve plotted in dashed line where the remote scattering mechanisms are turned off. As can be seen, the effect of the remote interface roughness cannot be neglected at low fields, showing clearly the need to include this mobility component when modelling ultra-thin oxide MOSFETs. Neglecting remote scattering mechanisms in the curve corresponding to $T_{ox}=1.5nm$ leads up to 30% error.

4.5 Conclusions

A mobility model taking into account the remote scattering mechanisms in ultra-thin oxide MOSFETs was developed, including both polysilicon-oxide surface-roughness and Coulomb scattering due to the polysilicon depletion charge.

The proposed mobility expression allowed us to reproduce the Monte Carlo simulation results obtained for several of these ultra-thin gate oxide devices.

This expression is also used along with the previously developed models to account for the different scattering mechanisms usually included in mobility analytical models in order to reproduce the experimental results obtained with very thin oxide MOSFETs.

Part II

THE SOI PARADIGM

Chapter 5

SOI technology

The traditional integrated circuit technology is associated with the concept of integrated circuit conceived by Noyce [Noy77] and Kilby [Kil76], where multiple transistors could be made in the same piece of Si by insolating neighboring devices from each other with reverse biased *p*-*n* junctions, field oxides or stop channels. Despite the fact that the monolitic integration has revolutionized the technology and the World, as the microelectronics industry has evolved, it has become increasingly clear that junction insolation is not always the best approach to achieve monolithic integration. Among its damaging effects, extra capacitance, slowing down the circuit operation and the reduction of integration density in circuits should be mentioned. If the ambient temperature is high enough, leakage currents diminish the isolation between various circuit components.

Nowadays, the semiconductor industry follows Moore's law [Moo65]. According to it, the performance of the electronic circuits must double every eighteen moths. This improvement has been achieved by gradual miniaturization of the devices. However, as the featuring size of the devices becomes lower than $0.1\mu m$, new problems with non-trivial solution appear, questioning the possibility of maintaining this policy for a long term.

The solution of these problems demand a total reconsideration of the classical concepts that have been used in all design aspects until now. Therefore, it is necessary to optimize all the areas involved in the production, from the substrate manufacture, device improvement, new architectures for microprocessors and finishing

with the redefinition of the encapsulation and external interconnections.

The new innovative concepts must be compatible with the present processes and techniques to ensure a gradual reconversion of the current technology and recovering in that way, the huge amount of money invested in clean rooms.

5.1 SOI technology motivation

It is possible and in some cases advantageous, to build monolithic semiconductor circuits with dielectric, instead of junction, isolation. This is accomplished by utilizing silicon-on-insulator (SOI) wafers [Maz06]. Since one decade, commercial applications of SOI have grown exponentially, and entered the mainstream of ultralarge (ULSI) electronic circuits as shown in Figure 5.1.

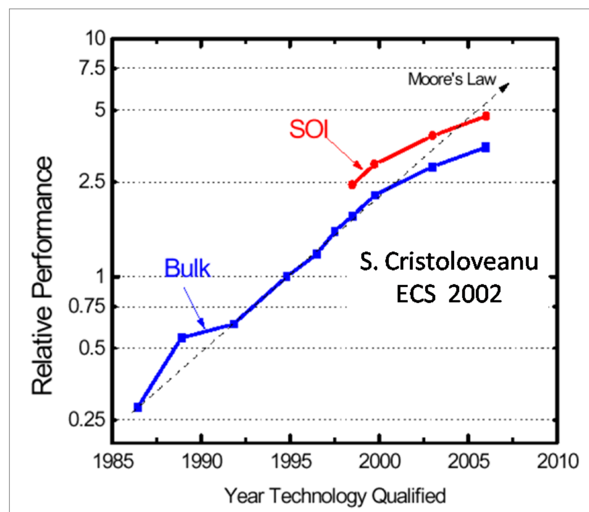


Figure 5.1: Comparison between Moore prediction and the perfomances of traditional bulk Si and SOI technologies.

Three have been the main reasons to motivate the development and use of SOI technology. In the 1970's and 1980's radiation hardness of SOI circuits was the main motivation for choosing these new substrates. The thin active films minimized the impact of ionizing radiation on device performance. The majority of charges generated, for example, by an alpha particle impinging on a Si substrate would be

stopped by the buried oxide, thus reducing the current surge in the active film.

In second place, currently, performance enhancement motivates many integrated circuit companies to use SOI wafers. For the same supply voltage, digital logic circuits, such as microprocessors, run faster in SOI than in bulk Si. Alternatively, it is possible to reduce power consumption of SOI chips by lowering their operating voltage, while still keeping the clock rate, *i.e.* their performance which is the same as in more power-wasteful circuits.

Finally, as we approach what is known as the "end of the Roadmap", SOI is needed to extend life of the traditional Si technology [CC03]. Transistors with gate lengths of 25nm or less do not perform well in bulk Si. The electric field in the transistor channel induced by the gate has to compete with the fields from the source and the drain regions. These short channel effects (SCE) are reduced or eliminated by using thin SOI structures.

The change from the technology hasn't been so critical as it was thought in the beginning. Once the technological challenge of making crystal silicon films on a dielectric substrate has been overcome, the circuit design is similar to the one used on the previous technology. In practice, it is not necessary to introduce heavy modifications in the design to translate a conventional bulk circuit into SOI. In fact, some of the layout structures that should be introduced to isolate the devices and avoid parasitic effects such as leakage current, photo-current induced by radiation or the so called *latch-up*, are not necessary due to the buried oxide (BOX) and the lateral electrical insulation [CC03]. The resulting circuits are simpler and more compact.

In parallel with purely electronic applications, SOI wafers are becoming the material of choice for many kinds of micro-electro-mechanical systems (MEMS) and microphotonic chips [CC03]. MEMS applications of SOI take advantage of mechanical properties of the monocrystalline films, which are superior to those of polycrystalline Si. Photonic applications rely on the high refractive index contrast between Si and SiO_2, which permits photon confinement in small waveguides with sharp bends [CL95], [CC03].

5.2 SOI wafers fabrication

The main problem to build a SOI wafer comes up when a crystalline silicon layer must be grown on a amorphous substrate. Numerous efforts have been made in that way without success. At the same time the knowledge of the structure and the morphology of the Si films has been improved.

On the next pages, the most advantageous SOI techniques for the commercial manufacture are presented.

5.2.1 SIMOX

The acronym SIMOX stands for "Separation by IMplanted OXygen". The principle of SIMOX material formation is quite simple, and consists in the synthesis of a buried layer of SiO_2 by implantation of oxygen ions beneath the surface of a silicon wafer. Processing conditions must be such that a single-crystal overlayer of silicon is maintained above the oxide. In contrast to conventional microelectronics implantation, in the case of SIMOX, ion implantation is used to synthesize a "new" material, namely SiO_2. This means that 2 atoms of oxygen have to be implanted for every silicon atom over a depth over which the silicon dioxide has to be formed. The implanted dose required to form a BOX, has to be from 100 to 500 times higher than the heaviest doses commonly used for microelectronics processing. As result, it is necessary to use an implantation dose in the order of $1.8\times10^{18}cm^{-2}$ at 200keV.

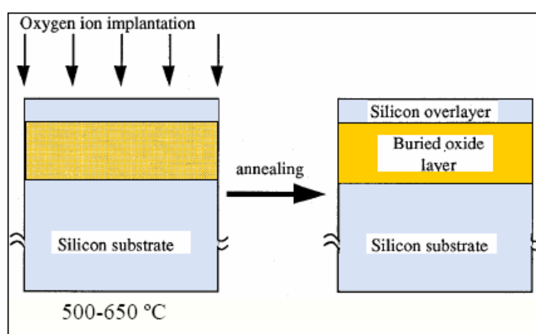


Figure 5.2: The principle of SIMOX: a heavy-dose oxygen implantation into silicon followed by a very high temperature annealing step produces a buried layer of silicon dioxide below a thin, single-crystal silicon overlayer.

The temperature at which the implantation is performed is also an important parameter which influences the quality of the silicon overlayer. Indeed, the oxygen implantation step does amorphize the silicon which is located above the projected range. If the temperature of the silicon wafer during the implantation is too low, the silicon overlayer gets completely amorphized, and it forms polycrystalline silicon upon further annealing, an undesirable effect. When the implantation is carried out at higher temperatures (above 500°C), the amorphization damage anneals out during the implantation process ("self annealing"), and a single-crystallinity of the top silicon layer is maintained. The silicon overlayer, however is highly defective.

At higher implant temperatures (700-800°C), SiO_2 precipitates in the silicon overlayer, mostly near its bottom interface, although large precipitates have been observed near the surface region of the silicon film. This effect seems to set an upper limit on the implantation temperature of approximately 700°C. Implantation temperatures most commonly used range between 600°C and 650°C.

In 1990, Nakashima ant Izumi [NI93] proposed the reduction of the implanted dose pursuing the drastic limitation of the dislocation density in the silicon layer over the BOX. The "low-dose" SIMOX is obtained by implanting O^{+} ions at a specific dose located in a very narrow window around 4×10^{17}cm^{-2}. With a single implantation and a 6 hour anneal at 1320°C, a continuous BOX having a thickness of 8nm is formed. In this way, thinner buried oxides were obtained waking up the interest in the thin layer devices. Moreover, carbon and heavy metal contaminants and wafer price were reduced since they were proportional to the oxygen implanted dose. For all these reasons, during the last years new techniques based on low-dose oxygen implantation have been derived like ITOX or SIMOX MLD.

Early SIMOX wafers typically had $10^{10}cm^{-2}$ threading dislocations intersecting the Si film. Formation of these defects depends on a complex interplay of many factors. Reduction to $10^{6}cm^{-2}$ threading dislocations was achieved by increasing implantation temperature to $\sim 600^{o}C$ [CC03]. A sequence of multiple partial-dose implants and anneals was shown to further reduce the defect density by an order of magnitude, but at the added cost of the process complexity [HFF88]. Further reductions in defect density relied on modifying the implanters.

Finally, the quality of the SiO_2 achieved through this technique is considerably lower than the native thermal oxide quality.

5.2.2 ELTRAN®

The Epitaxial Layer TRANsfer (ELTRAN®) is another approach that combines the formation of a porous layer and a wafer bonding to produce Bond-and-Etchback SOI (BESOI) material with good film thickness uniformity. This technique was developed by Canon in 1990 for the industrial production of SOI wafers [YSS94]. As presented in Figure 5.3 it is possible to grow a high-quality silicon epitaxial film on porous silicon. The porous silicon wafer with the epitaxial layer film can then be oxidized and bonded to another wafer. Polishing is then used to thin the SOI wafer down to porous silicon layer, and chemical etching is then used to remove the latter [Col04].

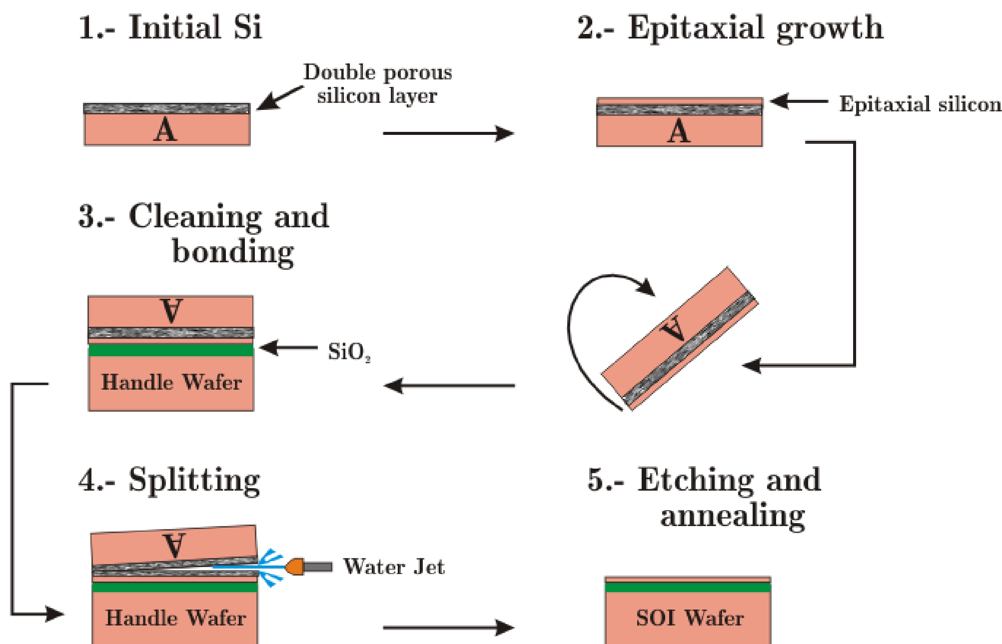


Figure 5.3: Schematic of the ELTRAN process.

Porous Si is formed by an electrochemical reaction when Si constitutes the anode of an electrolytic cell with an HF solution as the electrode. The etching process cuts a random network of nanometer scale pores in Si, producing a porous layer than has a fraction of the density of Si and a very large surface-to-volume ratio (200-

$1000\text{m}^2/cm^3$).

The ELTRAN® technique takes advantage of the fact that porous Si is mechanically weak, but still preserves the single crystalline quality of the wafer on which it was formed. As further refinement, instead of porous Si layer, two layers are formed with different pore morphology. By suitably changing current flow conditions during anodic etching, a layer with very fine pores is formed at the surface, with a second layer that has coarse pores positioned deeper into the substrate (Double porous silicon layer in Figure 5.3). Since there is considerable surface stress at the boundary between these two porous layers, a water jet causes cracking along the planar porous layers, leading to a more uniform cleavage.

After wafer cleavage, the residual porous Si on the SOI wafer is etched away, and the newly exposed SOI wafer surface is smoothed by a second application of hydrogen annealing at about 1100^oC. The wafer 'A' that donated the epitaxial film can be reclaimed, polished if necessary, and then reutilized.

The crystal quality of the SOI material obtained by wafer bonding and etch-back is, in principle, as good as that of the starting silicon wafer. The dislocation density, however increased in the case where epi is used on a P^{++} buried layer as an etch stop (instead of porous film).

5.2.3 Smart-CUT^{TM}

This process combines ion implantation technology and wafer bonding techniques to transfer a thin surface layer from a wafer onto another wafer or an insulating substrate. It was discovered in 1991 by M. Bruel from CEA-LETI [Bru95] who filled a patent application on a method of preparing thin silicon films that could be used to form SOI wafers. As applied to the fabrication of SOI, the method consisted of wafer bonding followed by splitting of a thin layer from one of the wafers.

Figure 5.4 shows the basic steps of this technique. The starting point are two conventional silicon wafers (A and B). The A seed wafer, from which a layer of Si will be removed, is oxidized to desired thickness. This oxide will become the buried oxide or BOX after bonding. The following step is hydrogen implantation through the oxide into Si with a dose that is typically $> 5\times10^{16}cm^{-2}$ producing fine microcavities in the Si lattice. After implantation, A wafer and B wafer (handle wafer) are carefully

cleaned in order to eliminate any particle and surface contaminants and to make both surfaces hydrophilic. Wafers pairs are aligned and contacted so that the fusion wave can propagate across the entire interface. A batch of bonded pairs is loaded into furnace and heated to a temperature of 400-600°C. The pressure builds up to a point of fracture and the wafers split along the hydrogen implanted plane. The size increase of the microcavities takes place along a <100> direction (i.e. parallel to the wafer surface).

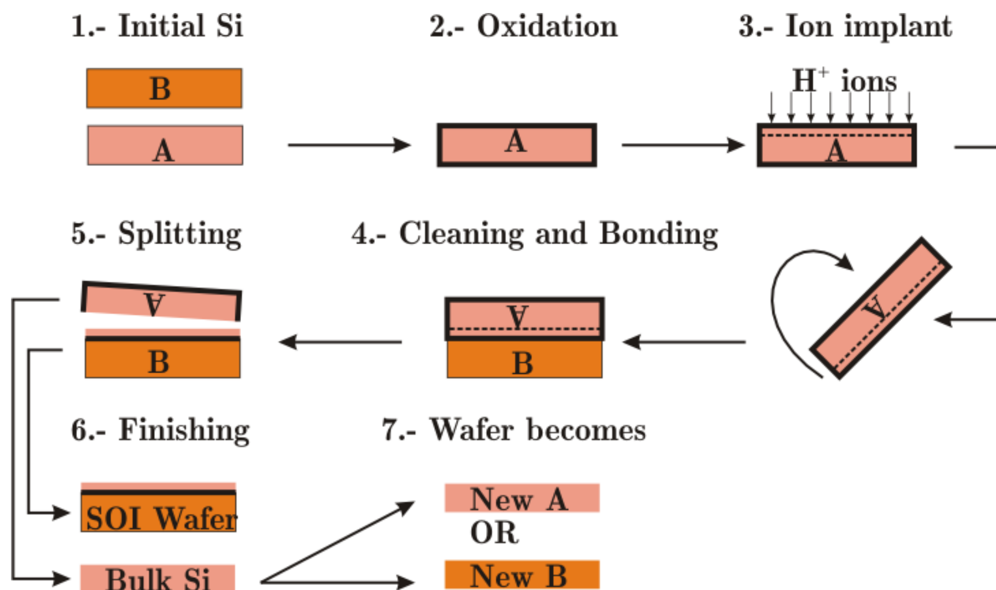


Figure 5.4: Obtaining SOI wafers by Smart-Cut^{TM} method.

A second heat treatment takes place at a higher temperature (1100°C) and is aimed at strengthening the bond between the handle wafer and the SOI film. Finally, chemo-mechanical polishing is performed on the SOI film to give it the desired mirror-like surface. Indeed, this layer exhibits significant micro-roughness after wafer A splitting, such that a final touch-polish step is necessary to reduce the surface roughness to less than 0.15 nm and consume a few hundreds of angstroms of the SOI film.

The Smart-Cut^{TM} process requires only *N+1* starting wafers to produce *N* SOI wafers, while other BESOI processes require *2N* wafers to produce *N* SOI wafers

[Col04]. This process has proved to be the most efficient and nowadays is the most utilized in the commercial production of SOI wafers [CC03].

There are other *wafer bonding* based methods to obtain monocrystalline silicon films on almost any substrate. In this way it is possible to fabricate circuits for certain applications where the properties of the mechanical support are important, like in the case of integrated circuits on flexible substrate, glass or plastic, allowing a best integration of embedded systems.

5.3 Advantages of the SOI technology

As shown is the previous sections, although most of the technological processes related to the SOI devices manufacture are compatible with the standards of the semiconductor industry, the final cost of the product is slightly higher than the conventional technology essentially due to the pre-processing of the wafers for each application. In spite of it all, the advantages of the SOI technology over bulk are important, and the cost increment is justified, even being the only alternative for certain architectures. Among the main advantages should be mentioned [CC03]:

- Reduction of parasitic capacitance and junction depth.
- Full compatible technology with the traditional processes.
- Steps reduction in the manufacture process.
- In some cases, increase of the level of integration due to the layouts simplification.
- Ionizing radiation hardness devices.
- Reduced power consumption of SOI chips by lowering their operating voltage, while still keeping the clock rate.
- Higher operation speed for the same supplied voltage.
- Short channel effects (SCEs) are reduced or eliminated by using thin SOI structures.

- Architecture flexibility.
- Integration of different structures in the same chip such as high speed devices, power devices, MEMS and optic elements.
- Three-dimensional devices.

5.4 SOI devices classification

In SOI technology, the MOSFET still remains as the most used part for conventional single gate devices. This fact and the technological compatibility has allowed the direct transfer of the conventional CMOS technology into SOI wafer based circuits. However, the existence of a buried oxide and the development of new techniques for obtaining SOI structures has opened a new scenario for new devices impossible to implement under the conventional CMOS technology. A new range of opportunities has appeared making possible the suitable device for each application. Such a huge lot of configurations and operation principle lead to multiple classifications.

In SOI MOSFETs, two inversion channels can be activated, one at the front Si-SiO_2 interface and the other at the back Si-BOX interface.

5.4.1 Partially depleted MOSFETs

In partially depleted (PD) SOI MOSFETs, the depletion region induced by the gates does not extend from one interface to another, and a neutral region subsists between the too insulators. The interface coupling effects are not present, but instead floating-body effects arise (Figure 5.5), inducing kink effect, transient variations of the potential, threshold voltage and current.

5.4.2 Fully depleted MOSFETs

Full depletion happens when the depletion region covers the whole transistor body. The depletion charge is constant and cannot extend further when the gate bias increases. The excellent coupling between the gate and the inversion charge offers improved current and subthreshold slope. The front and back surface potentials

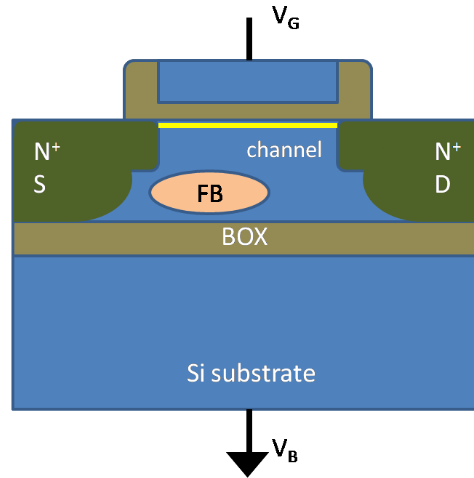


Figure 5.5: Configuration of a partially depleted SOI MOSFET.

become inter-related. Interface coupling means that the electrical characteristics of one channel vary with the opposite gate bias. In practice, the front-gate measurement may include contributions from the BOX and from the BOX/bulk interface, and highly depends on the back-gate bias. FD characteristics are complex, controlled by both gate voltages.

5.4.3 Multigate devices

One of the problems that the semiconductor industry has to deal with in the near future is the increase of the driven current by reducing the dimensions without losing the control of the charge by the gate (SCEs). Multigate devices arise from that necessity: If one gate is not enough, why don't we have more than one?

The dual-gate configuration is the intrinsic feature of SOI devices. The *double-gate* MOSFET is one step ahead of the context of the interface coupling. The two gates are simultaneously scanned. The first device based on this concept was the XMOS [SH84], Figure 5.6(a), taking its name from the greek letter Ξ. It presents better charge control than its single-gate counterpart. The first double gate ever fabricated was call DELTA [HKKT89], it became a vertical device, being the first precedent of the FinFET, Figure 5.6(c), which manufacture is simpler than in the

horizontal channel device. However, there are limitations between the ratio of the channel length, L_G, and silicon film thickness, T_{Si}.

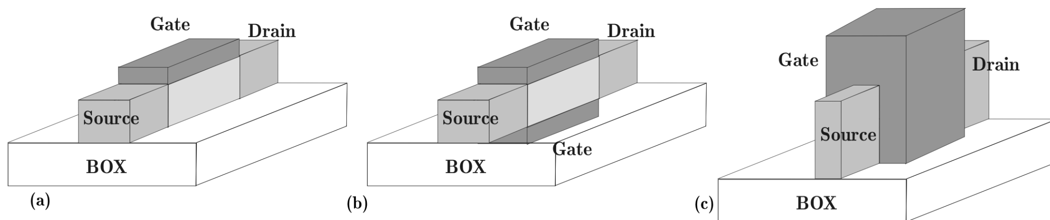


Figure 5.6: Schematic representation of SOI devices: (a)SGSOI, (b) DGSOI, (c) FinFET.

Once the advantages of a second gate were observed, the next step was the addition of another gate to increase even more the control over the charge in order to reduce the short-channel effects as the final premise. Thus, new devices called trigates appeared; a narrow and thin silicon island was surrounded by the oxide, Figure 5.7(a). There are more sophisticated devices situated between the three and four gates; the so-called *triple+*. The Π-*FET* and Ω-*FET* are two examples (Figures 5.7(b) and 5.7(c) respectively). In the first one, the gate penetrates into the buried oxide providing greater control over the charge. In the second one, the gate not only penetrates in the BOX, but also it extends laterally under the silicon film without closing. If the device is narrow enough, this configuration allows an additional *virtual-gate* below the silicon island induced by the field below the gate extensions [Col04].

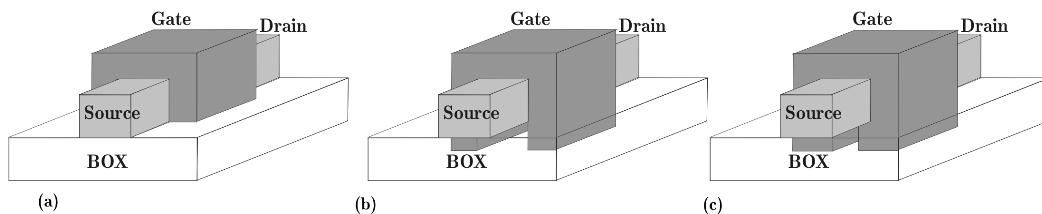


Figure 5.7: Schematic representation of SOI devices: (a) Trigate, (b) Π-Gate, (c) Ω-Gate.

Finally, if the silicon layer is completely surrounded by structures assigned to

the charge control the device is called four-gate. Different approaches have been proposed but no one is under manufacture. In one of them (GAA), the silicon film is completely covered. This structure reduces to the quantum wire [BCBG95] concept when the thickness and the width are small enough. Figure 5.8(a) shows the *gate-all-around* MOSFET (GAA) as a horizontal device with rectangular section completely surrounded by the gate. If the device is vertically conceived as a silicon pillar with circular section the device is called CYNTHIA (cylindrical thin-pillar) and if the section is rectangular it is called *pillar surrounding-gate*.

Another known option, the G^4-FET [CC03] (Figure 5.8b), consists in a device with two MOS gates on the up and low sides and two JFETs on the lateral sides. The G^4FET is operated in accumulation mode. The conductive path is modulated by mixed MOS-JFET effects: from tiny quantum wire, surrounded by depletion regions, to a strongly accumulated body. Each gate has the capability of switching the transistor on and off. The independent action of the four gates opens new perspectives for mixed-signal applications, quantum wire effects, and quaternary logic schemes.

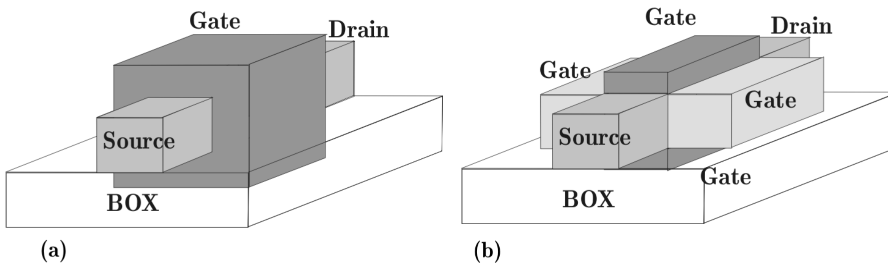


Figure 5.8: Schematic representation of SOI devices: (a) GAA, (b) G^4FET.

5.4.4 Non-conventional effects

In thick partially depleted double-gate films, increasing the gate bias simultaneously in both gates, $V_{G_{1,2}}$, has only the effect of forming two channels instead of one. The two channels grow independently, whereas the undepleted central region of the film is controlled by majority carriers. The total current comes from the parallel

combination of two transistors. The case of fully depleted films is far more exciting; the whole film can reach strong inversion [BCB+87]. The minority carriers are no longer confined at interfaces, and many of them can fly in the silicon film volume (Figure 5.9) being less affected by the presence of interface traps, oxide charges, surface roughness, and other surface-related scattering events.

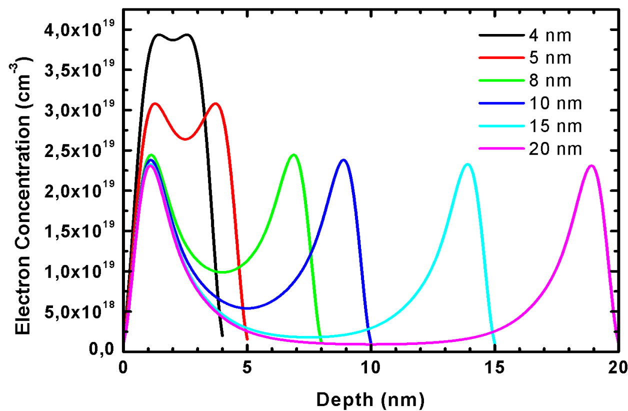


Figure 5.9: Charge density dependence along the silicon thickness in double gate devices. The interaction between both channels (volume inversion) is revealed being specially significant below 10nm.

One of the goals of this work is to show the expected increase in mobility and transconductance previously anticipated by Monte Carlo simulations [GF01]. Figure 5.10 shows the electron mobility as a function of the silicon thickness when the SOI transistors are operated in single-gate and double-gate mode. The beneficial effect of the volume inversion is clearly seen for silicon films thinner than 10nm.

Another important effect caused by the reduction of the silicon film thickness is the subband modulation effect [GRCC+99]. This effect is related to the split of the degeneracy of the Si conduction-band minima. The self-consistent solution of the Poisson and Schrödinger equations shows that the populations of the non-primed subbands increase at the expense of the primed subband population as the silicon layer thickness is reduced. Examples of this effect will be given in Section 8.2.2.2. As a consequence, the conduction effective mass of the electrons decreases as the

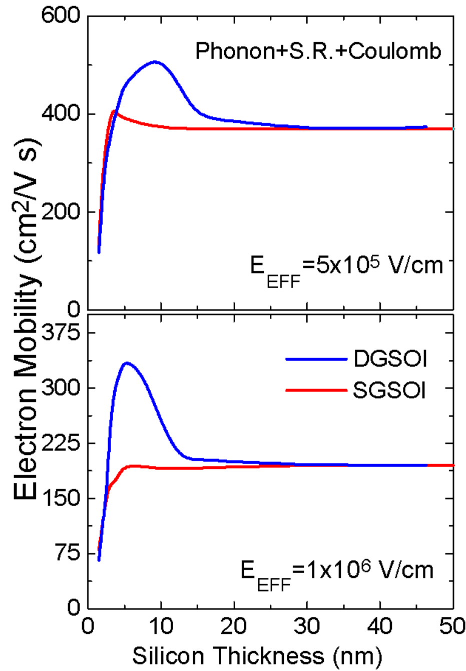


Figure 5.10: Monte Carlo simulated mobility dependence on the silicon film thickness. The effect of volume inversion is clearly seen leading to an important mobility increase for silicon films thinner than 10nm.

silicon layers thickness decreases and therefore the effective mobility increases.

5.5 Conclusions

In this chapter some essential aspects of the SOI technology have been treated. An in-depth study was already done by different authors ([CL95], [CC03], [Col04]). The future of SOI is bright: process compatibility with standard semiconductor industry, geometric flexibility for each application and the performance increase are claiming SOI as the base of the future semiconductor industry. SOI is facing the traditional bulk processes, gaining ground day by day and representing the best alternative to extend life of the traditional Si technology as we approach to the "end of the Roadmap".

Chapter 6

SOI wafers characterization

6.1 Introduction

The demand for SOI wafers with ultrathin silicon films, without degradation of their electrical properties, is strong. As for all products dedicated to device fabrication, these wafers require a quick, detailed, and reliable electrical characterization to asses their quality [HAHC07]. The list of evaluation techniques includes C(V), transport, photo-transport, Hall effect, deep level spectroscopy, etc [CL95]. The main problem is how to deal with fully-depleted films and coupling effects between multiple interfaces.

In this chapter, two are presented: the second harmonic generation which is being adapted to SOI an the pseudo-MOSFET which is the most advanced and reliable wafer characterization technique.

6.2 Second Harmonic Generation in Ψ-MOS

Although SOI devices are naturally resistant to transient photocurrents and single event upset, total-dose irradiation may induce a parasitic conduction path at the buried oxide (BOX) interface due to radiation-induced oxide and interface traps [JFS+03].

The Si/BOX interface quality has been studied electrically through various techniques such as *I-V* and *C-V*. Wafer-level measurements via the pseudo-MOS tech-

nique are frequently used for evaluation of partially-processed wafers. The limitation of this technique is that it damages the active device regions by directly probing the Si-film, and it is limited to the characterization of the top Si/SiO_2 interface.

Recently, the second harmonic generation (SHG) technique has been proposed as a nondestructive and non invasive probing technique since the SH signal detects the electric field at the Si/SiO_2 interface without directly contacting the surface [JSF+04].

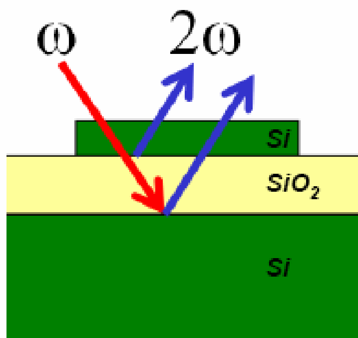


Figure 6.1: Schematic diagram of UNIBOND wafer structure for optical measurements: Incident fundamental beam and selected SHG signals.

Laser irradiation generates electron-hole pairs in the Si-region; some of the electrons acquire enough energy to overcome the barrier at the Si/SiO_2 interface and are injected into the oxide. Some of the injected electrons are trapped on free surface or at defects in the oxide regions. These electrons are responsible for the time-dependent electric field at the Si/SiO_2 interfaces

The time-dependent electric field-induced second-harmonic generation is governed by Eq. 6.1 for a single interface (Figure 6.1). As expressed in Eqs. 6.1-6.3, $E\left(t\right)$ is a quasi-static electric field related to the effective oxide surface charge density, σ, which is the integral of the oxide volume charge density, ρ over the normal axis.

$$I^{2\omega}\left(t\right) = \left|\Xi^{(2)} + \Xi^{(3)}E\left(t\right)\right|^2 \left(I^{\omega}\right)^2 \qquad (6.1)$$

$$E(t) = \frac{e\sigma(t)}{\varepsilon_{\text{Si}}} \tag{6.2}$$

$$\sigma(t) = \int_{o}^{T_{ox}} \rho(z,t)\, dz \tag{6.3}$$

where $I^{\omega}$and $I^{2\omega}$ are the fundamental and SHG signal intensities; $\Xi^{(3)}$ and $\Xi^{(2)}$ are the third-order susceptibility in silicon and the effective SHG susceptibility from other sources respectively.

For multi-interfacial structures, the total SH intensity includes contributions from all interfaces. The time-dependent electric field is created independently at each interface. The SH intensity $I^{2\omega}$ is described by Eq. 6.4 which includes the effects of the electric fields at the different interfaces.

$$I^{2\omega}(t) = \sum_i \left| \Xi_i^{(2)} + \Xi_i^{(3)} E_i(t) \right|^2 (I^{\omega})^2 \tag{6.4}$$

The electric field generated at each interface contributes to the total SHG intensity independently, yet it is also affected by an externally applied electric field. The SHG intensity including the contribution of the constant applied field is expressed in 6.5. Depending on the polarity of the external field, it can add or subtract from the existing field:

$$I^{2\omega}(t) = \sum_i \left| \Xi_i^{(2)} + \Xi_i^{(3)} \left(E_{ext} \pm E_i(t) \right) \right|^2 (I^{\omega})^2 \tag{6.5}$$

Transistor like curves are presented in Figure 6.2; the interface field can be associated with the channel inversion charge. The bias dependence is analogous to the I-V characteristics commonly obtained using the $\Psi - MOSFET$ technique [CML00].

Furthermore, the large penetration depth of the optical radiation allows to use SHG as a sensitive probe of electric field at deeply buried SOI interfaces. Therefore, SHG can be an attractive alternative to investigate carrier dynamics in SOI wafers.

The second harmonic generation constitutes a promising and useful noninvasive technique to characterize the radiation response of multi-interface SOI wafers

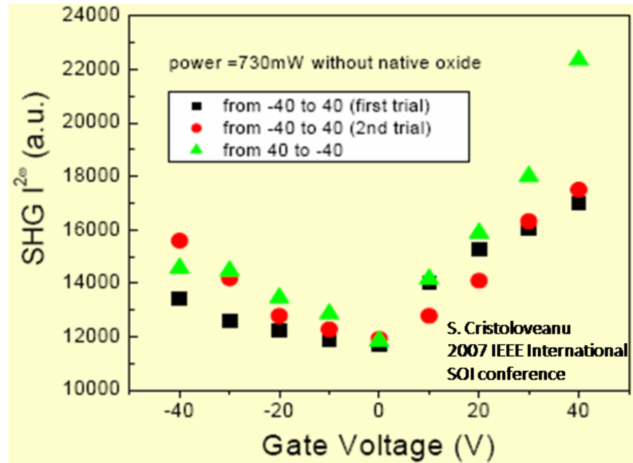


Figure 6.2: Transistor like contact less Ψ-MOSFET curves similar to drain-gate voltage curves.

providing information about charge carrier dynamics in SOI structures. Optical and electrical methods can be combined to separate the contributions of the signal from each interface to the total SHG intensity [JSF+04].

6.3 Pseudo-MOSFET

Any SOI material has a natural, upside-down MOS configuration (Figure 6.3). The silicon film represents the transistor body and the buried oxide serves as the gate insulator. The thick Si substrate plays the role of the gate and it can be biased through a metal support to induce a conducting channel at the interface between the film and oxide [CW92], [CML00]. Depending on the positive or negative "gate" bias, an inversion or accumulation channel can be activated. The source and drain electrodes can be formed by two point-contact tugsten carbide probes.

This device is named pseudo-MOSFET (Ψ-MOSFET) and represents a unique method allowing the wafer characterization before any CMOS device processing. Typical $I_D\,(V_G, V_D)$ curves characteristics are reproduced in Figure 6.4. The low-field carrier mobility (holes or electrons), threshold voltage, flat-band voltage, density of interface defects can be obtained combining this configuration with usual

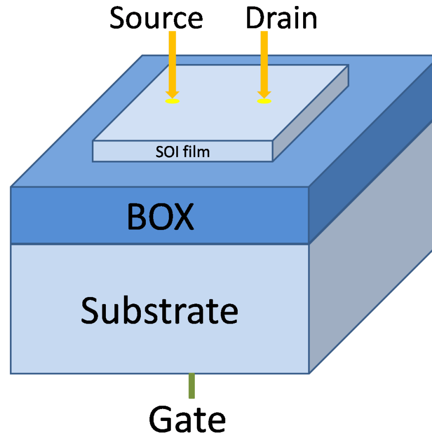


Figure 6.3: Schematic configuration of the Ψ-MOSFET.

extraction procedures [CW92], [CML00], [Hov03].

Previous studies indicated that pseudo-MOSFET characteristics are affected by silicon thickness. As the film gets thinner, the current level decreases (leading to a decrease of the transconductance), while the subthreshold swing and the absolute values of both threshold and flat band voltage increase.

In particular, the threshold (and flat band) voltage shift has been subjected to detailed discussions and some explanations have been offered [SKB+05], [HAHC07], [BC04].

6.3.1 Threshold voltage shift

In this section the outstanding increase in the threshold voltage that was experimentally observed in SOI films thinner than 50nm is investigated [BC04]. The symbols in figure 6.5 show the Y-function [Ghi88] extracted threshold voltage versus the silicon layer thickness in UNIBOND© wafers with $t_{BOX} = 145nm$. As observed, the threshold voltage (and also the flat-band voltage, not shown) increases as the film thickness is reduced.

This effect is not accounted in classical pseudo-MOSFET model which suggests an opposite variation. In fact conventional equations give:

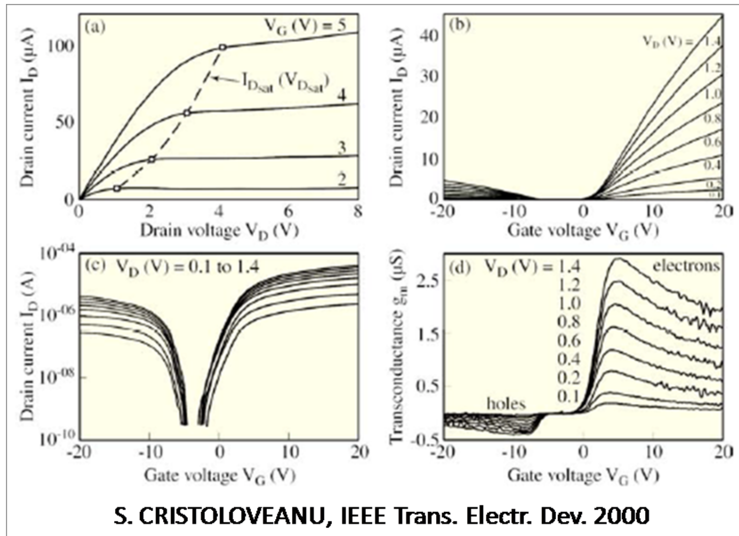


Figure 6.4: Typical Ψ−MOSFET characteristics in UNIBOND© material: (a) drain current versus drain voltage, (b) drain current versus gate voltage in strong inversion and strong accumulation, (c) weak inversion/ accumulation curves, and (d) transconductance curves.

$$V_{FB} \cong \frac{kT}{q} \ln\left(\frac{N_{film}}{N_{sub}}\right) - \frac{Q_{ox}}{C_{ox}} \tag{6.6}$$

$$V_T \cong V_{FB} + \frac{qN_{film}}{C_{ox}} t_{\text{Si}} + 2\phi_F \left(1 + \frac{qD_{it}}{C_{ox}}\right) \tag{6.7}$$

where N_{film} and N_{sub} are the doping levels in the silicon film and substrate (in Unibond wafers $N_{film} \approx N_{sub}$). Q_{ox} is the fixed charge in the oxide and D_{it} is the trap density at the film-BOX interface. These equations show no dependence of V_{FB} with the silicon film thickness, and suggest a decrease of the threshold voltage for thinner films. The discrepancy with the experimental data (reproduced in Figure 6.5) suggests that a corrected model is needed accounting for the coupling between the top and bottom interfaces.

The in-depth 1-D numerical solution of Poisson equation was calculated by considering that the gate voltage drops exclusively in the BOX and SOI film. Both buried interface (film-BOX) density of traps, D_{it_1}, and top (free surface of the film) den-

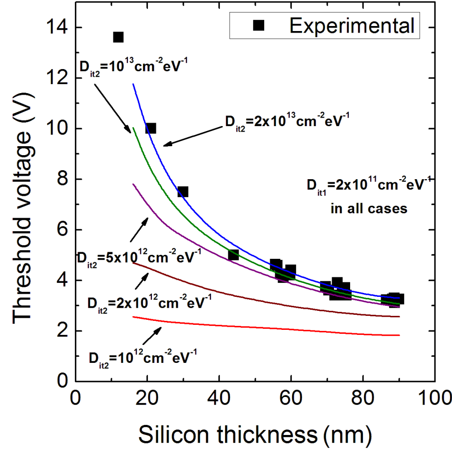


Figure 6.5: Experimental extracted (solid symbols) and simulated threshold voltage versus the silicon thickness for various trap densities of surface states. For D_{it2} =2×10^{13}$cm^{-3}eV^{-1}$ the simulation fits the experimental data. t$_{BOX}$=145nm.

sity of traps, D_{it_2}, were considered. Then the threshold voltage was extracted from the peak of the second derivative of the inversion charge versus substrate voltage characteristic.

The solid-lines in Figure 6.5 show the simulation-extracted threshold voltage versus the silicon layer thickness for different values of free surface density of states, D_{it2}. It is clear that the top surface density of charge is responsible for the threshold voltage shift with the film thickness. For $D_{it2} = 2 \times 10^{13} cm^{-2}eV^{-1}$ the simulation reproduces the experimental curve for non-passivated wafers, and this density of traps is in good agreement with suggested values [HAHC07]. The effect of the buried density of states (not shown) is just a vertical shift of the curves ($\sim qD_{it1}/C_{ox}$ as in the usual MOSFET transistor).

Figure 6.6 illustrates the threshold voltage extraction procedure used to obtain the data plotted in Figure 6.5. The charge density obtained from the numerical solution of Poisson equation is derived two times. The peak positions of this derivative correspond to the threshold voltage values [CL95]. Observe also the lateral shift of the charge curves as the top density of states increases due to the coupling effect.

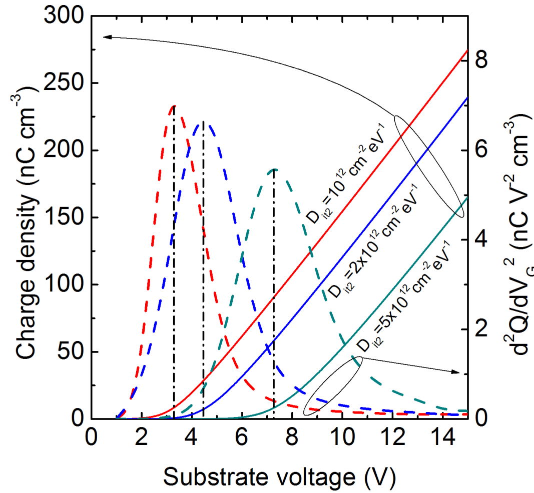


Figure 6.6: Charge density (continuous line) and second derivative of the charge density (dashed line) illustrating the threshold voltage extraction procedure. In all cases $D_{it1}=2\times 10^{11} cm^{-2} eV^{-1}$.

6.3.2 Vertical potential profile

Figure 6.7 explains the reason for this behavior governed by the density of states. The simulations reveal that the potential profile is severely dominated by the top interface when the trap density is high ($D_{it2} = 2 \times 10^{13} cm^{-2} eV^{-1}$, Figure 6.7a) and the film is ultrathin. This invalidated the usual thick-film Ψ-MOSFET model which assumes zero top-charges. It follows that the inversion condition (quasi-fixed BOX interface potential) requires a higher voltage than for lower free-surface charge. The potential profile corresponding to threshold is presented in dashed line. For $D_{it2} = 0\ cm^{-2} eV^{-1}$ (Figure 6.7b), the potential profile presents the usual parabolic-like shape. This contrasts with the case of high D_{it2} (Figure 6.7a), where the potential variation is quasi-linear; indeed, the field is roughly constant being imposed by the surface charge. The Ψ-MOSFET model [CL95] was developed for relatively thick SOI films where the top surface and native oxide are not relevant. The present simulation indicates the need for model reconsideration by including the coupling effect between the two interfaces of the film.

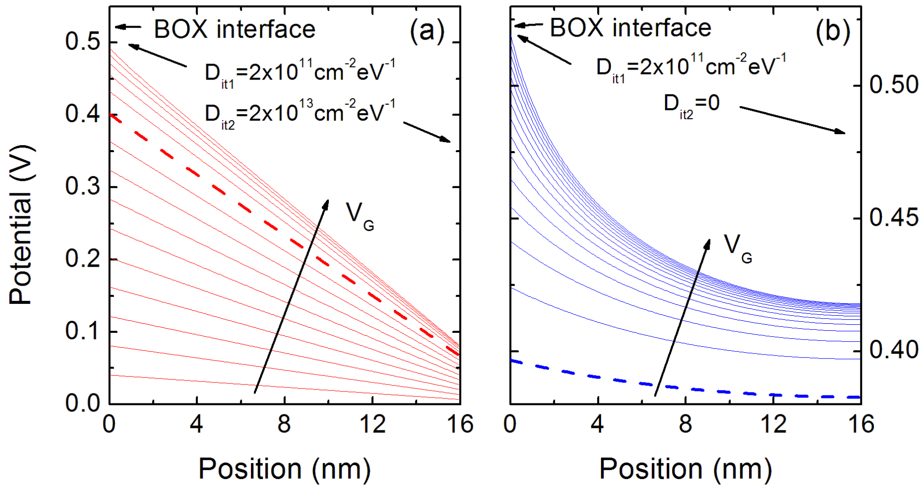


Figure 6.7: Potential profiles from BOX interface to free surface for a 16nm thick pseudo-MOSFET with (a) high and (b) zero density of states at the top surface. V_G increases from 1V by 1V steps. The portential profile corresponding to the threshold voltage is shown in dashed line.

As a consequence of the floating top potential the gate voltage must support an additional term accounting for the band shift. The total band curvature at inversion cannot be considered as $2\phi_F = 2kT/q\ln(N_{film}/n_i)$. This effect is the direct consequence of the absence of potential condition at the top interface.

A schematic energy-band diagram is presented in Figure 6.8. For simplification, the gate (wafer substrate for the pseudo-MOSFET case) is assumed to have the same Fermi level position as the film and therefore for $V_G = 0$ the structure is at flat-band (Figure 6.8a). For a positive gate bias (Figure 6.8b), the intrinsic Fermi level (E_{Fi}) never achieves the original equilibrium value (unlike the bulk MOSFET).

Figure 6.9 shows potential profiles similar to those presented in Figure 6.7 but for a silicon film thickness of 82nm. Note that in this case the threshold voltage difference is not so noticeable due to the lower coupling effect of the top interface. Figure 6.9a exhibits smaller top potential shift, ψ_0, than Figure 6.7a; this difference is also the consequence of the film thickness.

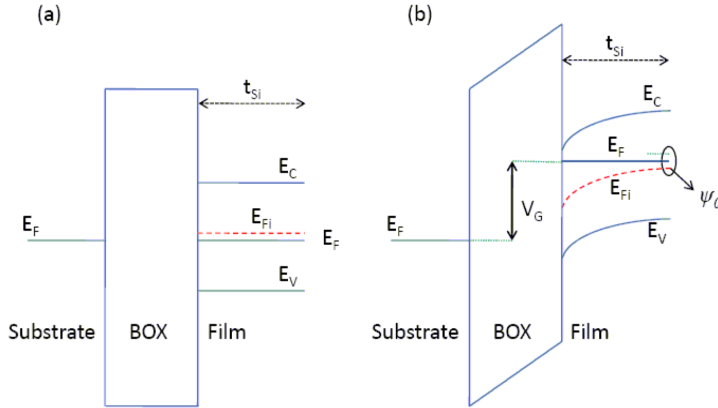


Figure 6.8: Schematic energy band diagram. (a) No bias is supplied. (b) For positive bias, as a consequence of the absence of top potential condition, the band shifts leading an additional potential term supported by the gate voltage (circled area).

6.3.3 Analytical model for the threshold voltage

Analytical current-voltage (I-V) models are indispensable in compact modelling and for the comprehension of the fundamentals of pseudo-MOSFET characteristics [CML00]. The starting point of the modelling task is Poisson's equation along a vertical cut perpendicular to the Si film:

$$\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon_{\mathrm{Si}}}\left(n_i e^{\frac{q\psi}{kT}} + N_A\right) \tag{6.8}$$

Models for the threshold voltage by always neglecting the minority carriers have been proposed [CW92], [Hov03]:

$$\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon_{\mathrm{Si}}} N_A \tag{6.9}$$

At present, ignoring the minority carriers in **ultrathin** layers is a delicate matter. An inaccurate expression of the threshold voltage is unable to reproduce the strong inversion current.

Our strategy was opposite: we tried to face the problem in an analytical way, solving Poisson's equation while neglecting the film doping ($\lesssim 10^{15} cm^{-3}$) and accounting for the minority carriers. Then, the Pao-Sah integrals are the straight

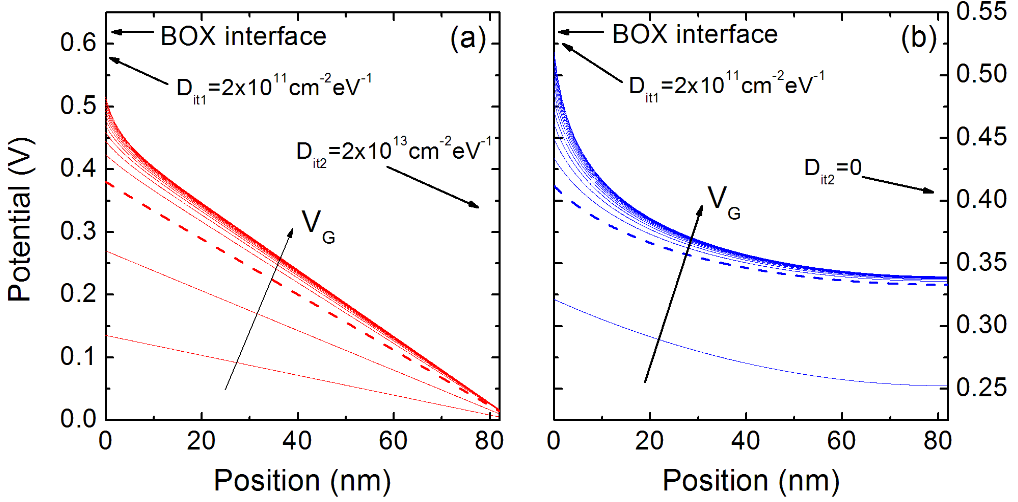


Figure 6.9: Potential profiles from BOX interface to free surface for a 83nm thick pseudo-MOSFET with (a) high and (b) zero density of states at the top surface. V_G increases from 1V by 1V steps. The portential profile corresponding to the threshold voltage is shown in dashed line.

forward way to obtain the current and therefore the threshold voltage ([Tau00]).

We considered Poisson's equation for minority carriers:

$$\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon_{\mathrm{Si}}} n_i e^{\frac{q\psi}{kT}} \tag{6.10}$$

where ψ is the potential, *i. e.* $\psi = E_{F_i} - E_F$ (Figure 6.8) A first integration yields:

$$\frac{d\psi}{dx} = \sqrt{\frac{2kTn_i}{\varepsilon_{\mathrm{Si}}}\left(e^{\frac{q\psi}{kT}} - e^{\frac{q\psi_0}{kT}}\right)} \tag{6.11}$$

In Eq. 6.11 the electrical field at the top free interface has been supposed to be zero. This is in accordance with Figure 6.7b where the potential profile becomes flat when no charges are considered at the top interface. By contrast no assumption is made about the top interface potential ($\psi_0 = E_{F_i}(t_{\mathrm{Si}}) - E_F(t_{\mathrm{Si}})$) leaving it like an open condition. After a second integration:

$$\frac{q\left(\psi-\psi_0\right)}{kT}=-2\ln\left[\cos\left(\sqrt{\frac{q^2n_i}{2kT\varepsilon_{\text{Si}}}}e^{\frac{q\psi_0}{2kT}}x\right)\right] \tag{6.12}$$

and now using the change of variable:

$$\beta=\sqrt{\frac{q^2n_i}{2kT\varepsilon_{\text{Si}}}}e^{\frac{q\psi_0}{2kT}}t_{\text{Si}} \tag{6.13}$$

Eq. 6.12 becomes:

$$\psi\left(x\right)=-2\frac{kT}{q}\ln\left[\frac{t_{\text{Si}}}{\beta}\sqrt{\frac{q^2n_i}{2kT\varepsilon_{\text{Si}}}}\cos\left(\frac{\beta x}{t_{\text{Si}}}\right)\right] \tag{6.14}$$

Figure 6.10 shows the potential profile comparison between Eq. 6.14 and the numerical solution of Poisson equation for (a) $T_{\text{Si}}=20nm$ and (b) $T_{\text{Si}}=100nm$ film thicknesses. As it was expected, the agreement is perfect since Eq. 6.14 represents the analytical solution of Eq. 6.10. Different values of the *gate* (substrate) bias are presented.

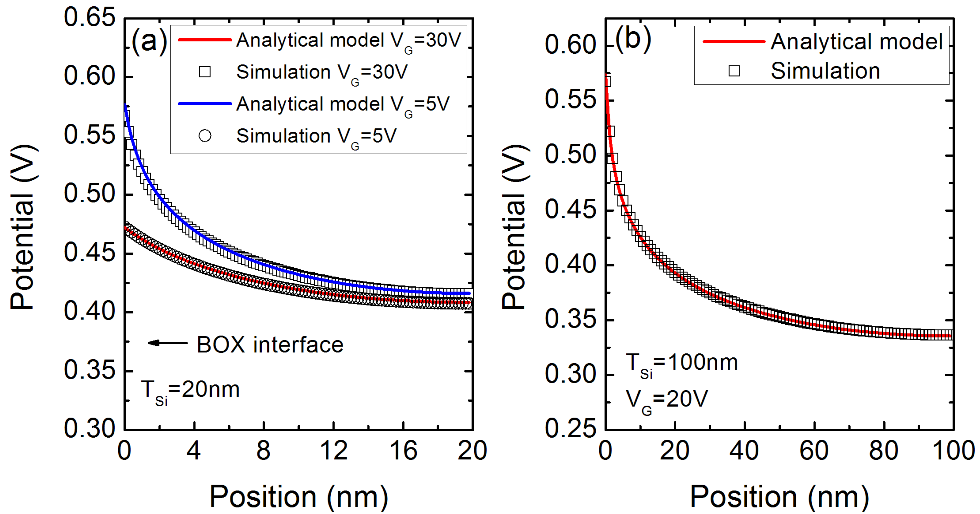


Figure 6.10: Potential profile comparison between Eq. 6.14 and the numerical solution of Poisson equation (Eq. 6.10).

The total inversion charge is easy to obtain from Gauss law (zero field at the top interface):

$$Q_{inv} = \varepsilon_{\mathrm{Si}} \left(\frac{d\psi}{dx} \right)_{x=t_{\mathrm{Si}}} = \varepsilon_{\mathrm{Si}} \frac{2kT}{q} \frac{\beta}{t_{\mathrm{Si}}} \tan\left(\beta\right) \tag{6.15}$$

Pao-Sah's integral [PS66] from source to drain can be written as:

$$I_D = \mu \frac{W}{L} \int_0^{V_{DS}} Q_{inv} dV = \mu \frac{W}{L} \int_{\beta_S}^{\beta_D} Q_{inv}\left(\beta\right) \frac{dV}{d\beta} d\beta \tag{6.16}$$

Above threshold, combining Eqs. 6.14, 6.15, 6.16 with the boundary condition referred to the continuity of the electrical displacement:

$$\varepsilon_{ox} \frac{V_g - \phi_{fs} - \psi\left(x = t_{\mathrm{Si}}\right)}{t_{ox}} = \varepsilon_{\mathrm{Si}} \left(\frac{d\psi}{dx} \right)_{x=t_{\mathrm{Si}}} \tag{6.17}$$

where ϕ_{fs} is the Fermi levels difference between the film and the substrate, *i.e.* $\phi_{fs} = E_{F-film} - E_{F-substrate}$. Using Eq. 6.17 after integrating in Eq. 6.16, yields:

$$I_D = f_g \mu C_{ox} \left[\left(V_g - V_T\right) V_D - \frac{V_D^2}{2} \right] \tag{6.18}$$

where f_g is the pseudo-MOSFET form factor and V_T plays the role of the threshold voltage:

$$V_T \equiv \phi_{fs} + \frac{2kT}{q} \ln \left[\frac{1}{t_{\mathrm{Si}}} \sqrt{\frac{2\varepsilon_{\mathrm{Si}} kT}{q^2 n_i}} \right] \tag{6.19}$$

This equation holds for ideal bottom and top interfaces (no charge).

The charge at the BOX-Silicon film interface (Q_{BOX} and D_{it1}) can be accounted in the continuity of the electrical displacement, Eq. 6.17, generating only a shift in the threshold voltage.

$$\varepsilon_{ox} \frac{V_g - \phi_{fs} - \psi\left(x = t_{\mathrm{Si}}\right)}{t_{ox}} + Q_{BOX} - qD_{it1}\psi\left(t_{\mathrm{Si}}\right) = \varepsilon_{\mathrm{Si}} \left(\frac{d\psi}{dx} \right)_{x=t_{\mathrm{Si}}} \tag{6.20}$$

This correction results in an improved expression of V_T.

$$V_T \equiv \phi_{fs} + \frac{Q_{BOX}}{C_{ox}} + \frac{2kT}{q}\left(1 + \frac{qD_{it1}}{C_{ox}}\right)\ln\left[\frac{1}{t_{\mathrm{Si}}}\sqrt{\frac{2\varepsilon_{\mathrm{Si}}kT}{q^2 n_i}}\right] \tag{6.21}$$

Equation 6.21 is analytical and it represents a very good approximation to evaluate the threshold voltage, but with limited validity (only for the case when the top interface charges can be neglected). Otherwise there is no way to perform the integration of Eq. 6.10 if the top field is not assumed as zero.

Equation 6.21 also reveals that under this analytical (and classical) approach the threshold voltage could become out of control in ultrathin layers as seen in the functional dependence of the logarithm in Eq. 6.21 when t_{Si} decreases. Note that this extreme case needs to be accounted for by including the thickness-related quantum effects (subband splitting and carrier confinement).

Figure 6.11 shows the comparison of the analytical threshold voltage expression (Eq. 6.12) with experimental results. The film and substrate are assumed to have the same doping level ($\phi_{fs} = 0$). The BOX-film interface features a density of interface states, D_{it1}=$2\times10^{11}cm^{-2}eV^{-1}$.

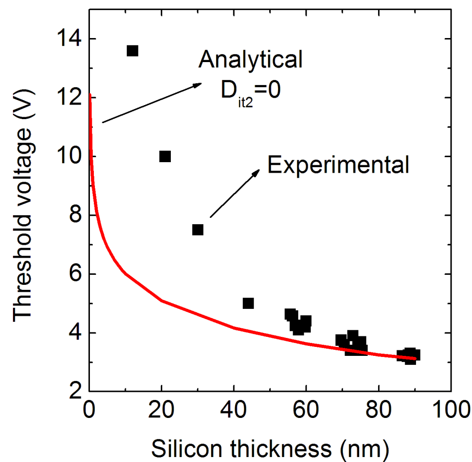


Figure 6.11: Comparison between the the analytical model (Eq. 6.21) considering a buried interface density of charge (BOX/Si-film interface) determined by D_{it1}=$2\times10^{11}cm^{-2}eV^{-1}$ and the experimental extracted values for the threshold voltage.

As observed the analytical model (Eq. 6.21) is only able to reproduce the experimental values of the threshold voltage for the thicker silicon films where the influence of the non-passivated top interface (with high density of charge) is reduced or it can be simply neglected.

6.3.4 Empirical model for the threshold voltage

Due to the difficulty to derive an analytical model, an alternative empirical model is proposed for the threshold voltage. Three parameters are used depending on the technology:

$$V_t\left(t_{\mathrm{Si}}\right) = V_{t0}\left(1 + \frac{V_q}{V_{t0}} e^{-Rt_{\mathrm{Si}}}\right) \tag{6.22}$$

V_{t0} is the conventional thick-film $\Psi - MOSFET$ threshold voltage, and V_q and R are thin film parameters depending on the density of staters D_{it2}. A good agreement with the numerical solution is observed in the whole charge and thickness range (Figure 6.12).

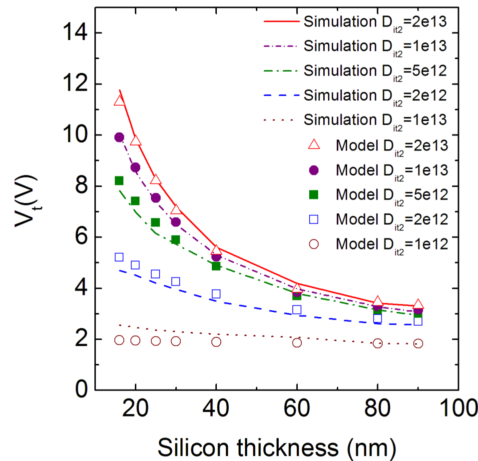


Figure 6.12: Comparison between the empirical model (symbols) presented in Eq. 6.22 and the simulation results (lines). D_{it1}=$2\times10^{11}cm^{-2}eV^{-1}$, t_{BOX}=$145nm$, for all the curves shown.

The model fits the experimental data (Figure 6.5) for $V_{t0} = 3.2V$, $V_q = 20V$ and $R = -0.053(nm)^{-1}$. Both V_q and R presents linear variation with the density of interface traps.

6.4 Conclusions

After presenting two of the most advanced in-situ wafer characterization techniques, attention has been focused on the pseudo-MOSFET technique. Numerical simulation clarify the influence of the free surface quality on the Ψ-MOSFET characteristics. The threshold voltage in pseudo-MOSFET depends on the density of states at the free-surface, which can be passivated or not. Poisson equation shows that in ultrathin silicon films the potential is strongly controlled by the quality of the top surface. For unpassivated wafers, the threshold voltage increase in thinner films is exacerbated.

We have developed a new approach in modelling the potential profile, where the charge is essentially due to mobile carriers, not ionized impurities. An analytical model has been derived for ideal top interface. It was completed with an empirical model for unpassivated surfaces.

Chapter 7

Mobility extraction for SOI transistors

7.1 Introduction

After the SOI wafer characterization, the next conceptual step is the device level characterization. The first part of this chapter is dedicated to introduce and extend the characterization techniques (mainly threshold voltage and mobility extraction) for the case of SOI technology taking advantage of the challenging introduced by the coupling between the interfaces when the film thickness decreases. In the second part the validity of the characterization tools developed is checked on actual SOI devices by means of experimental measurements. For the first time, volume inversion effect will be revealed from usual static I_D-V_G characteristics.

7.2 Characterization techniques

Although carrier mobility extraction methods are routine procedures in bulk MOSFETs, they must be reconsidered for application to thin SOI films in response to intrinsic problems (large values of the sheet resistance, full depletion,...) and new opportunities (substrate bias influence).

7.2.1 Threshold voltage

The threshold voltage is one of the most palpable monitors for any technology. In contrast to partially depleted technology, in fully depleted transistors, the threshold voltage is not restricted to a unique value and must be measured as a function of the back-gate bias.

Various characterization methods are frequently used to determine the threshold voltage.

7.2.1.1 $I_D\,(V_G)$ extrapolation

When the $I_D\,(V_G)$ curve has been measured for the ohmic region of operation, the tangent is drawn at the inflection point, where V_G corresponds to the maximum transconductance. The intercept of the tangent with the horizontal axis gives the "extrapolated" threshold voltage [CL95]. The procedure is sketched in Figure 7.1. The accuracy may be improved by repeating the measurements for several V_D values.

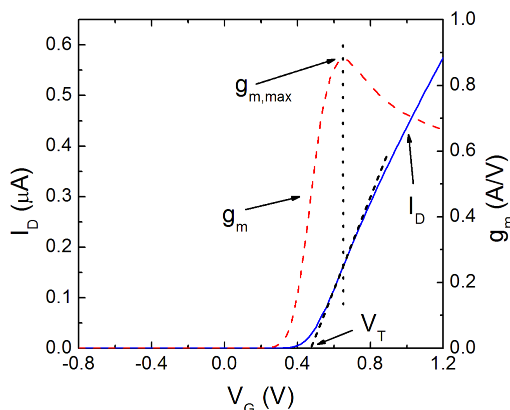


Figure 7.1: Threshold voltage extraction procedure from the drain current. A tangent is drawn at the inflexion point of the current curve. The intercept yields the extrapolated threshold voltage.

This method has been very popular for bulk Si and partially depleted SOI. Among the critical aspects, especially in fully depleted SOI, the extrapolated V_T

suffers from series resistance effects.

7.2.1.2 Constant-current V_T

In this case the threshold voltage is defined as the gate voltage allowing a certain amount of current (Figure 7.2); typically $0.1\mu A$ per μm width for a $1\mu m$ long channel and $V_D = 50mV$ [CL95]. This method has the advantage of avoiding any extrapolation error and may be used to monitor very small V_T fluctuations or shifts (such as those induced by short time radiation or hot-carrier degradation).

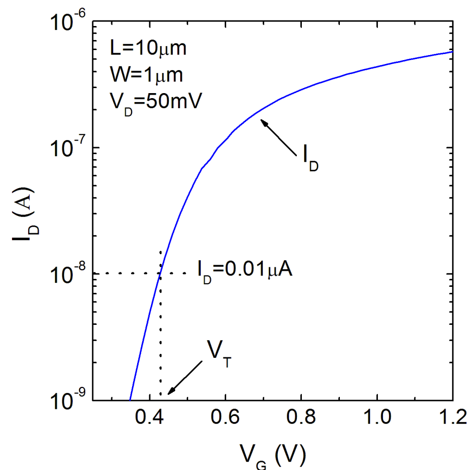


Figure 7.2: Constant-current threshold voltage extraction procedure.

It must be used very carefully in fully depleted SOI, where totally erroneous results may be derived. When the back interface is inverted, a current larger than the reference value ($0.1\mu A/\mu m$) flows in the device even if the front interface is depleted. This may lead to the wrong conclusion that the front threshold voltage steadily decreases, instead of being constant, when the back interface becomes more and more inverted. Additionally, the current may decrease, even at constant V_T, as a consequence of mobility degradation.

7.2.1.3 Y-function

Drawing the curve $I_D/\sqrt{g_m}$ in the ohmic region results in a straight line that intercepts the horizontal axis at $V_G = V_T$. This method will be discussed in detail in Section 7.3.

7.2.1.4 Peak of d^2I_D/dV_G^2

The peak of the second-order derivative of $I_D\,(V_G)$ curves, i.e., the inflexion point of the transconductance, occurs for a gate voltage that is close to $\psi_S = 2\phi_F$ [WWKB87]. This method has been validated by numerically calculating the derivatives of the inversion charge as a function of surface potential for various back gate voltages and technological options [ICR93]. Its reliability improves further in state-of-the art devices (thinner gate oxides and higher doping levels).

Nevertheless the application of this technique must be done carefully in fully depleted MOSFETs. When the back interface is inverted the transconductance curve is deformed due to the channel coupling. Figure 7.3 shows the front-channel transconductance curve measured for different values of the back-gate voltage. As soon as the back interface is inverted a characteristic plateau appears (for example for $-0.8<\mathrm{V}_{G1}<1.4$ and V_{G2}=40V in Figure 7.3).

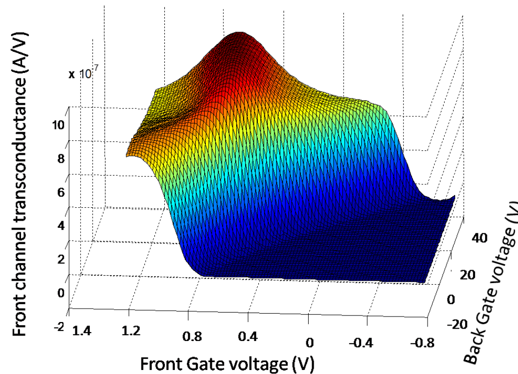


Figure 7.3: Experimental typical front-channel transconductance distortion versus front- and back-gate voltages. As soon as the back channel is inverted a characteristic plateau appears as a consequence of the channel coupling. $T_{\mathrm{Si}} = 10nm$, L=$10\mu m$, W=$1\mu m$, $T_{ox1} = 2nm$, $T_{ox2} = 145nm$, $N_A = 10^{15}cm^{-3}$.

The extraction technique is illustrated in Figure 7.4. For $V_{G_2} = 0V$ (triangles), the back interface is depleted leading to the usual transconductance curve with only one peak in its derivative. For high values of the back-gate voltage ($V_{G_2} = 25V$, squares), the back interface is inverted and two peaks are observed; the first peak corresponds to the back-channel activation (beginning of the transconductance plateau) and the second peak to the front-channel threshold voltage.

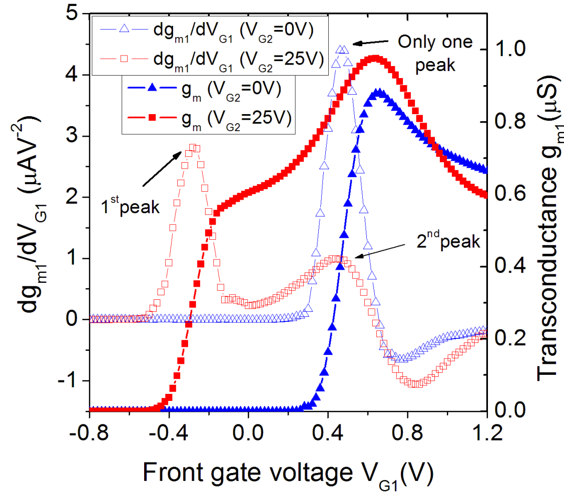


Figure 7.4: Front-channel threshold voltage evaluation from the transconductance inflexion point (second-order current derivative) for two different back-gate biases.

7.3 Mobility extraction

Increasing the carrier mobility is one of the engines to improve the device performance. New strategic approaches such as alternative oriented channels, strained materials, ultrathin volume inversion devices... are attempting to improve this parameter because in essence, the operation speed is proportional to the mobility.

The main characterization techniques are revisited in the following pages.

7.3.1 Transconductance peak

The rudest evaluation scheme is based on the maximum value of the transconductance measured at low V_D. The series resistance effects are neglected and the mobility is assumed to be:

$$\mu_0 = \frac{L}{W}\frac{g_{m,\max}}{C_{ox}V_D} \tag{7.1}$$

where $g_{m,\max}$ is the maximum value of the $\partial I_d/\partial V_G$ curve. This method rather constitutes a first order approximation and its practical use is quite limited in current technologies.

7.3.2 Split-CV

The behavior of the effective channel mobility (μ_{eff}) as a function of the effective transverse field ($E_{eff} = (0.5Q_i + Q_d)/\varepsilon_{\mathrm{Si}}$, being Q_d the depletion charge) has been extensively studied for fully depleted SOI devices for a variety of silicon film thicknesses and positive back-gate biases (V_{gb}). μ_{eff} is defined as [SEM82]:

$$\mu_{eff} = \frac{I_D}{\frac{W}{L}Q_i V_D} \tag{7.2}$$

where I_D is the drain current, V_D is the drain voltage (considering the source at 0 volts), W and L are the device width and length, respectively, and Q_i is the inversion charge density per area unit. The inversion charge can be calculated as a function of gate voltage:

$$Q_i\left(V_G\right) = \int_{-\infty}^{V_G} C_{GC}\left(V_G\right) dV_G \tag{7.3}$$

where C_{GC} is known as the gate-to-channel capacitance per unit area. Because the inversion charge is a function of drain voltage, this method of extracting mobility results in a slight overestimation of the inversion charge. The inaccuracy in the calculated Q_i results in a 10% underestimation of peak effective mobility at low E_{eff} values. At higher E_{eff} values, corresponding to the gate voltage for normal device operation, the underestimation of μ_{eff} can be neglected. The low field mobility, μ_0, is conventionally adopted as the maximum value of the effective mobility [CL95].

7.3.3 Magnetoresistance

The Hall effect is a well-known phenomenon that occurs when carriers move in the presence of a magnetic field perpendicular to the transport plane. The conventional theory is developed considering a rectangular device longer than it is wide. While the carrier motion is deflected by the Lorentz force, there cannot be any current in the transversal direction. Indeed the Lorentz force is balanced, on the average, by an electric field (Hall field) in the transversal direction. The corresponding Hall voltage V_H can be experimentally measured, and used to compute the Hall mobility through [CL95]:

$$\mu_H = \frac{V_H}{R_{\Box} B I_x} \tag{7.4}$$

where $R_{\Box}$ is the sheet resistance, B the magnetic field, I_x the device current.

The Hall mobility is related to the drift effective mobility μ_{eff} through the Hall factor r_H defined as:

$$\mu_H = r_H \mu_{eff} \tag{7.5}$$

If carriers are assumed to be monokinetic, this factor reduces to unity and the two quantities, μ_H and μ_{eff} coincide; when the carrier energy distribution is taken into consideration, r_H no longer equals one. An expression for r_H can be obtained in the relaxation time approximation, and involves the scattering rates dependence on energy for the different scattering mechanisms [See97].

If the device is short and wide, the lateral Hall field is short-circuited because of the contacts. In this case, a geometric magnetoresistance appears, due to the fact that the Lorentz force is no longer compensated be a lateral Hall field. The magnetoresistance is maximum for Corbino geometry with circular symmetry. To fulfill the Corbino condition, the sample length has to be much smaller than the width (typically $W/L > 5$). It can be shown that the current density along the x direction (along the channel) is [Loo85]:

$$J_x = \sigma_{xx} E_x \tag{7.6}$$

The conductance component σ_{xx} depends on the magnetic field. The current

density in the presence of a magnetic field, B, can be written as

$$J_x = \frac{\sigma_0}{1 + \mu_{MR}^2 B^2} E_x \tag{7.7}$$

where σ_0 is the conductivity under zero magnetic field. The semiconductor resistivity change by the applied magnetic field is:

$$\frac{R_B}{R_0} = \frac{\rho_B}{\rho_0} = 1 + \mu_{MR}^2 B^2 \tag{7.8}$$

A magnetoresistance factor r_{MR} can then be defined, relating magnetoresistance mobility and the drift mobility:

$$\mu_{MR} = r_{MR} \mu_{eff} \tag{7.9}$$

Once more, r_{MR} is equal to 1 on the assumption that all carriers have the same energy, otherwise it depends on the scattering mechanisms involved [DGCC07].

An accurate extraction of the effective drift mobility from Hall or MR experimental data depends on knowledge of the ratios r_H and r_{MR}. Unfortunately, approximations are usually employed for the calculation of these quantities.

The magnetoresistance methodology will be applied in a Monte Carlo simulator to compare the mobility at the *front* and *back* channels in advanced SOI MOSFETs in Section 8.4.

7.4 Y-function based extraction

The MOSFET mobility extraction is usually carried out in the strong inversion regime of the MOSFET linear operation region. Therefore it relies on the well know drain current relation:

$$I_D = \frac{W}{L} \frac{\mu_0}{\left[1 + \theta \left(V_G - V_t\right)\right]} C_{ox} \left(V_G - V_t\right) V_D \tag{7.10}$$

Due to the series resistance dependence included in the θ parameter the mobility is underestimated if a direct extraction from a linear regression is considered. Only if θ is equal to zero, the value obtained corresponds to the low-field mobility.

The transconductance is calculated differentiating Eq. 7.10 with respect to the gate voltage, V_G:

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{W}{L} \frac{\mu_0}{\left[1 + \theta \left(V_G - V_t\right)\right]^2} C_{ox} V_D \tag{7.11}$$

Figure 7.5 shows typical drain current, I_D, and transconductance, $g_m(V_G)$, characteristics. The activation of the transistor is observed in the abrupt change in the transconductance.

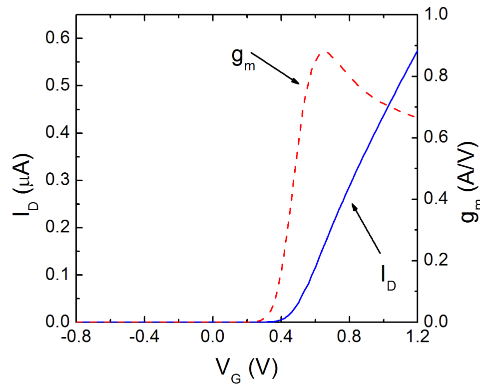


Figure 7.5: Experimental drain current, I_D, and transconductance, g_m, versus gate voltage, V_G. SOI-MOSFET characteristics: *L=10µm, T_{ox}=2nm, T_{si}=10nm, T_{box}=145nm, V_D=50mV.*

The basic idea of Ghibaudo's method [Ghi88] is to eliminate the influence of the mobility attenuation constant, θ, by means of the appropriate mathematical function through a suitable combination of Equations 7.10 and 7.11. This goal is achieved by dividing the drain current by the square root of the transconductance; the function obtained is called the *Y-function*:

$$Y = \frac{I_D}{\sqrt{g_m}} = \sqrt{\frac{W}{L} C_{ox} \mu_0 V_D} \left(V_G - V_t\right) \tag{7.12}$$

According to the previous relation, the plot $Y\left(V_G\right)$ comes out a straight line (Figure 7.6); low-field mobility, μ_0, and threshold voltage, V_t, can be obtained from

the slope and the intercept respectively, when W, L and C_{ox} are known.

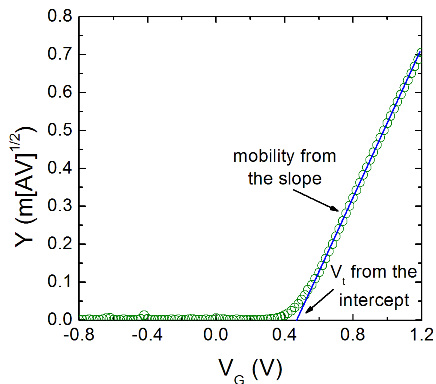


Figure 7.6: Experimental Y-function MOSFET characteristic ilustrating the parameter extraction. Same device as in Figure 7.5.

The mobility attenuation parameter, θ, can be determined from the *X-function*, defined as:

$$X = \frac{1}{\sqrt{g_m}} = \frac{1 + \theta\left(V_G - V_T\right)}{\sqrt{\frac{W}{L} C_{ox} V_D}} \tag{7.13}$$

According to Eq. 7.13, the plot X vs. V_G is a straight line with a slope proportional to θ.

7.5 Two-channel model

The goal of this chapter is to examine the usefulness of the Y-function method for the case of SOI MOSFETs with two activated channels (Figure 7.7).

In SOI MOSFETs it is also possible to emulate a DG transistor by sweeping the two gates simultaneously (Figure 7.7).

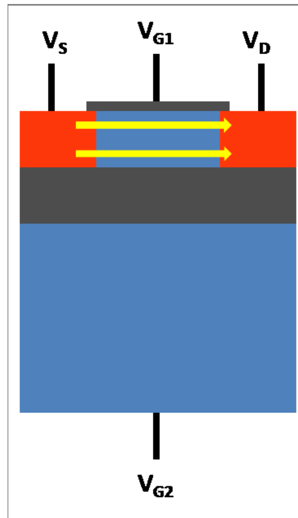


Figure 7.7: Double channel sketch for a SOI MOSFET.

7.5.1 PD MOSFETs: two independent channels

In PD-SOI transistors, the drain current adds together the contributions of the *front* and *back* channels, controlled by the *front* and *back* gates, respectively. Since the silicon film is thicker than the maximum depletion region induced by the gates, the middle of the transistor remains undepleted and the inversion channels are completely 'independent' of each other:

$$I_D = I_{D_1} + I_{D_2} \tag{7.14}$$

where subscripts *1* and *2* indicate the *front* and *back* channels, respectively.

Let's consider a case where the *back* gate is biased in inversion and the *front* gate is swept from depletion to inversion. The total current (Eq. 7.14) is the sum of the *front* and *back* currents, both given by Eq. 7.10 with the appropriate subscripts ($V_{G_{1,2}}$, $\mu_{01,02}$, $\theta_{1,2}$, etc.). Since I_{D_2} is fixed, the front-gate transconductance, $\partial I_D/\partial V_{G_1}$, is not affected by the back-channel conduction and reflects only the properties of the *front* channel. We ignore cases where the series resistance is modified by the activation of both channels [OCB92]. As far as the Y-function is concerned, its nominator is increased by the back-channel current, leading to an overestimation

of the carrier mobility:

$$Y = \frac{I_{D_1} + I_{D_2}}{\left(\frac{\partial (I_{D_1}+I_{D_2})}{\partial V_{G_1}}\right)^{1/2}} = \frac{I_{D_1} + I_{D_2}}{\left(\frac{\partial I_{D_1}}{\partial V_{G_1}}\right)^{1/2}} = Y_1 + \frac{I_{D_2}}{\sqrt{g_{m1}}} \tag{7.15}$$

It is clear from Eq. 7.15 that the last term, $I_{D_2}/\sqrt{g_{m1}}$, is responsible for the inaccuracy. The higher the *back* gate voltage or mobility of the back-channel, μ_2, the greater the error. Although I_{D_2} is a constant, in strong inversion, when V_{G_1} is increasing, $g_{m_1}$is decreasing and therefore the term $I_{D_2}/\sqrt{g_{m1}}$ is increasing causing the growth in the slope of Y. A detailed calculation using Eq. 7.15 reveals that the slope overestimation of the Y-function is given by the following expression:

$$\Delta slope_Y = \sqrt{\frac{W}{L} V_D} \frac{C_{ox_2}\mu_{02}}{\sqrt{C_{ox_1}\mu_{01}}} \frac{\mu_{02}\left(V_{G_2} - V_{T_2}\right)}{1 + \theta_2\left(V_{G_2} - V_{T_2}\right)} \theta_1 \tag{7.16}$$

which is directly proportional to the front channel series resistance attenuation factor, θ_1.

In order to validate the previous results, the current-voltage characteristics of SOI transistors were simulated using Equations 7.10 and 7.14. Then, for self-consistency, the Y-function was utilized for the mobility extraction. The input device parameters were: $t_{ox_1} = 2nm$, $t_{ox_2} = 145nm$, $V_{T_1} = 0.3V$, $V_{T_2} = 9V$, $\mu_{01} = 250cm^2/Vs$ (Si/high-k interface), $\mu_{02} = 350cm^2/Vs$ (Si/SiO$_2$ interface), $\theta_1 = 0.2V^{-1}$, $\theta_2 = 0.0028V^{-1}$ (unless otherwise specified).

In Figure 7.8, the extracted front-channel mobility versus the back-gate voltage is shown for different values of θ_1. As long as only the front channel is active, the correct mobility value ($\mu_{01} = 250cm^2/Vs$) is recovered. But, in accordance with Eq. 7.15, the Y-function-based mobility extraction fails when the back inversion channel is formed ($V_{G_2} > 9V$, the grey region in Figure 7.8). The extracted mobility is greater than the expected value ($250cm^2/Vs$). Increasing θ_1 causes a more severe overestimation that may reach 40% as is predicted in Eq. 7.16.

The above conclusions remain valid when the roles of the two gates are interchanged: μ_2 measurements by sweeping V_{G_2} and holding the front-channel in inversion.

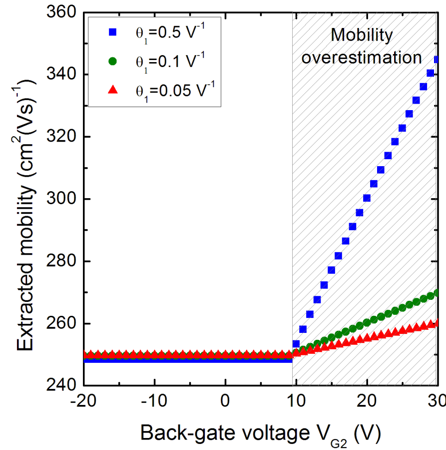


Figure 7.8: Extracted front-channel mobility versus back-gate bias for different values of θ_1. Y-function leads to an overestimation of the mobility when the back channel is opened (Eqs. 7.15 and 7.16).

7.5.2 FD MOSFETs with two separate, intercoupled channels

In relatively thick, fully-depleted SOI transistors, the neutral body region is suppressed but the *front* and *back* channels remain physically separated from each other. A coupling between the two channels occurs, which results in a variation of V_{T_1} with V_{G_2} and vice-versa in Eq. 7.10 and Figure 7.11. This case is far more complicated than in Eqs. 7.14 and 7.15. For example, the front-channel transconductance strongly depends on the back-gate bias and features a characteristic plateau (before the g_m peak) when the back channel is activated (Figure 7.3) [CL95], [OCB92]. Basically, the Y-function becomes meaningless because it mixes the carrier mobilities and threshold voltages at the front- and back-gate channels. Only in the particular case of a *back* channel accumulation, where the *front* channel is screened from V_{G_2} and V_{T_1} is constant, can the method still be applied safely, based on the single-channel Equation 7.10. However as pointed out by Eminente *et al.* [ECC+07], it may be difficult or even impossible in a sub-10nm thick film to sustain an accumulation layer facing the inversion channel.

The Y-function is also valid for depletion at the opposite interface but, in prac-

tice, caution is needed to avoid the accidental activation of the second channel. The mobility may depend on the opposite gate voltage via the change in the vertical field as shown in Figure 7.9 (see also for example Figure 7.8 where the simulated extracted mobility becomes overestimated as soon as the back channel is opened or Fig. 7.17 for experimental values).

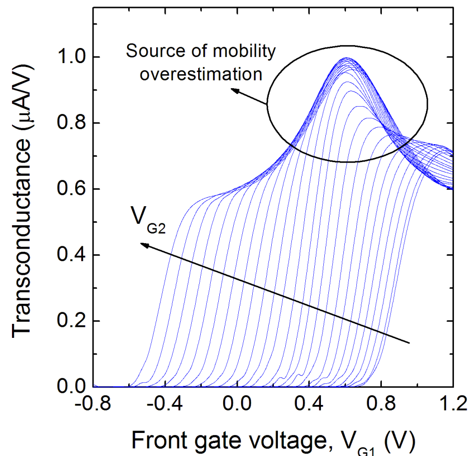


Figure 7.9: Experimental front-channel transconductance as a function of the back-gate bias. Note that the transconductance peak is artificially increased as a consequence of the back-channel activation. $T_{\mathrm{Si}} = 10nm$, L=*10μm*, W=*1μm*, $T_{ox1} = 2nm$, $T_{ox2} = 145nm$, $N_A = 10^{15}cm^{-3}$. V_{G2} starts in -20V with step of 2V up to 32V.

From the theoretical point of view of this study, FD-SOI transistors can be considered in the same way as PD transistors except that *front* and *back* currents Eqs. 7.10 and 7.14 are coupled through the threshold voltages. The variation of the threshold voltage of one channel with the bias of the other gate is shown in Figure 7.11.

Figure 7.10 shows the front-channel mobility, extracted by means of the *Y*-function technique and from the maximum transconductance (Eq. 7.1) versus the back-gate voltage. Before the back-channel is activated, the extracted value corresponds well to the assumed front-channel mobility.

After back-channel activation ($V_{G_2} > 2.5V$), an abnormal mobility rise is ob-

served, corresponding to the increase in the drain current and as a consequence in the transconductance. In this region (grey area in Figure 7.10), both mobility extraction methods become meaningless.

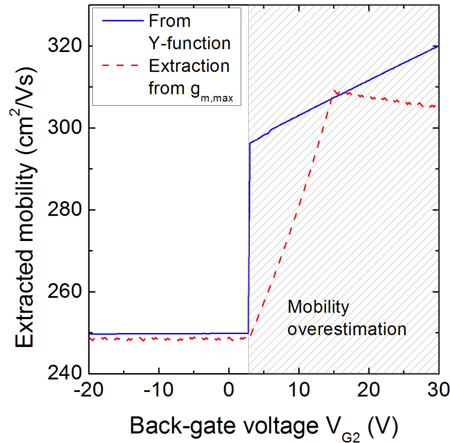


Figure 7.10: Extracted front-channel mobility from Y-function and from maximum value of the transconductance. A dramatic overestimation is observed as soon as the back channel is activated. Parameters: $t_{ox_1} = 2nm$, $t_{ox_2} = 145nm$, $V_{G_1} = 1V$, $\mu_{01} = 250cm^2/Vs$, $\mu_{02} = 350cm^2/Vs$, $\theta_1 = 0.2V^{-1}$, $\theta_2 = 0.0028V^{-1}$.

Another implication is that the threshold voltage extraction from Y-function is equally wrong. This explains a number of published results showing that the threshold voltage continues to drop when the back interface is in inversion whereas the theory gives a constant threshold voltage [LF84].

7.5.2.1 Back-channel mobility from front-gate *Y-function*

In one case of particular interest, the back-channel mobility can be extracted from the front-gate Y-function. For positive values of back-gate ($V_{T_2} > V_{G_2} > 0$), increasing V_{G_1} lowers V_{T_2} and opens the *back electron* channel first. This can easily be seen in Figure 7.11 where a theoretical dependence for the front and back threshold voltages versus the opposite gate bias is represented. A linear relationship for these dependences is assumed, according to the Lim-Fossum model [LF84].

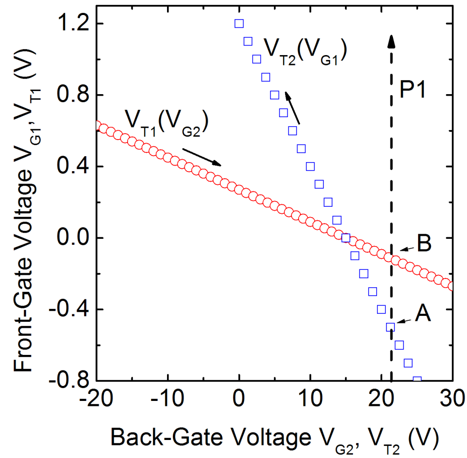


Figure 7.11: Analytical choice for the threshold voltage dependencies in the region of interest. Symbols show the variation of the front-channel threshold voltage with back-gate bias and back-channel threshold voltage with front-gate bias. *P1* bias: *Back* gate is positive and back-channel is activated first when front bias is increased (point *A*).

Considering $V_{G_2} = 22V$ (P1 bias), when V_{G_1} is swept, starting from negative values, V_{T_2} decreases and crosses the bias point A before the front threshold voltage is reached (point B). After the back channel is activated, V_{G_1} continues to increase, V_{T_2} decreases further, the drain current (given by the back channel) increases linearly with V_{G_1}, and the transconductance remains constant (plateau) [OCB92]. In the region between point A and point B, only the back channel operates and the current is given by:

$$I_D = \frac{W}{L} \frac{\mu_{02}}{1 + \theta_2 \left(V_{G_2} - V_{T_2}\right)} C_{ox_2} \left(V_{G_2} - V_{T_2}\right) V_D \tag{7.17}$$

Note that I_D depends on V_{G_1} through V_{T_2}. Considering a linear relation between V_{T_2} and V_{G_1}, the *front* channel Y-function, calculated using Eq. 7.17 gives:

$$Y = \sqrt{\frac{W}{L} \frac{C_{ox2} V_D \mu_{02}}{k}} V_{G1} + C \tag{7.18}$$

where C is a constant and k is the threshold voltage coupling factor (i.e., *-1/k* is

the slope of the V_{T_2} vs. V_{G_1} curve) [LF84], [CL95]:

$$k = \frac{C_{ox_2}\left(C_{ox_1} + C_{\text{Si}} + C_{it_1}\right)}{C_{ox_1} C_{\text{Si}}} \tag{7.19}$$

$C_{\text{Si}}= \varepsilon_{\text{Si}}/t_{\text{Si}}$ is the depleted-film capacitance and $C_{it_1} = qD_{it_1}$ is the front-interface trap capacitance.

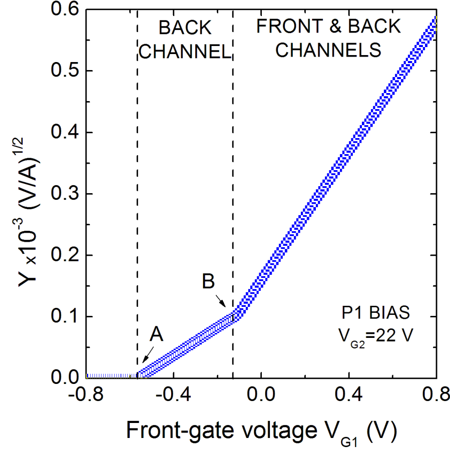


Figure 7.12: Front-gate Y-function for $V_{G_2} = 22V$. Back channel is activated first according to Figure 7.11. Point A: back-channel activation; point B: front-channel activation. The *back* channel mobility can be extracted in region A-B with the Y-function. Parameters: t_{ox_1}=2nm, $t_{ox_2} = 145nm$, $\mu_{01} = 250cm^2/Vs$, $\mu_{02} = 350cm^2/Vs$, $\theta_1 = 0.2V^{-1}$, θ_2=0.0028V^{-1}.

It follows that in the transconductance plateau region, μ_{02} can be safely extracted from the slope of $Y(V_{G1})$ curve (Eq. 7.18).

The back-channel mobility can be determined from $I_D(V_{G_1})$ curves, following the procedure given previously. For $V_{G_2} = 22V$ (P1 bias in Figure 7.11), the front-gate Y-function is represented in Figure 7.12. The *back* channel is activated first (point A) and then as V_{G_1} increases, the *front* channel is also activated (point B). Using Eq. 7.18, in region A-B, the extracted mobility is $\mu_{02} = 350cm^2/Vs$ as expected. This confirms the validity of the new method for safely extracting the back-channel mobility from the front-gate Y-function.

In references [CL95], [OCB92] an alternative method of extracting the back-channel mobility from the front-gate transconductance measurements is described. Using the plateau value of the front-gate transconductance ($g_{m,plat}$) in the region from A to B of the bias *P1* line in Figure 7.11, the value of the mobility is given by:

$$\mu_{02} = \frac{L}{W} \frac{k \cdot g_{m,plat}}{C_{ox_2} V_D} \tag{7.20}$$

Our Y-function based method (Eq. 7.18) beats Eq. 7.20 because it eliminates the series resistance effects. However, both techniques tend to the same extracted mobility value for lower $\theta_{1,2.}$

7.6 Balanced double-gate mode

7.6.1 Y-function for balanced double-gate operation

Compared with bulk silicon transistors, SOI MOSFETs are very attractive in terms of bias flexibility. Not only can the front gate be biased, but it is also possible to consider the Si substrate underneath the buried SiO_2 layer as a second gate emulating a double-gate transistor. In current SOI devices with buried SiO_2 layers around *150nm*, the bias applied to the back-gate is much greater than the front gate voltage.

In strong inversion, the charge per area unit in the channel is given by:

$$Q_{inv_{1,2}} = C_{ox_{1,2}} \left(V_{G_{1,2}} - V_{T_{1,2}} \right) \tag{7.21}$$

In order to obtain the same charge in both channels (*i.e.*, a perfectly balanced DG operation), the following equality must hold [OPCZ05]:

$$\frac{1}{t_{ox_1}} \left(V_{G_1} - V_{T_1} \right) = \frac{1}{t_{ox_2}} \left(V_{G_2} - V_{T_2} \right) \tag{7.22}$$

Attention to the threshold voltages must be paid in Eq. 7.22, because in FD-SOI transistors, the threshold voltage of one gate depends on the polarization of the other gate, $V_{T_{1,2}}(V_{G_{2,1}})$. Selection of the correct $V_{T_{1,2}}$ values to trigger the two channels simultaneously will be discussed in section 7.5.3.

We consider a transistor operating in balanced-DG mode (Eq. 7.22) and assume that the total current is the sum of the *front* and *back* channel currents (Eq. 7.14). In this case, the Y-function yields:

$$Y_B = \sqrt{\frac{W}{L} C_{ox_1} V_D \frac{\left(1+\theta_2 \frac{t_{ox2}}{t_{ox1}} \left(V_{G_1} - V_{T_1}\right)\right) \mu_{01} + \left(1+\theta_1 \left(V_{G_1} - V_{T_1}\right)\right) \mu_{02}}{\sqrt{\left(1+\theta_2 \frac{t_{ox2}}{t_{ox1}} \left(V_{G_1} - V_{T_1}\right)\right)^2 \mu_{01} + \left(1+\theta_1 \left(V_{G_1} - V_{T_1}\right)\right)^2 \mu_{02}}}} \left(V_{G_1} - V_{T_1}\right) \tag{7.23}$$

where $\mu_{01,02}$ are the low-field mobilities for the *front* and *back* channels. In order to derive a friendly expression for the Y-function, we assume an additional simplifying condition:

$$\theta_1 t_{ox1} \approx \theta_2 t_{ox2} \tag{7.24}$$

Condition 7.24 can be justified using basic premises. For a 'long' transistor, θ reduces to the intrinsic attenuation factor, θ^0, which is proportional to $1/t_{ox}$. The mobility attenuation factor θ can be approximated as follows [CL95]:

$$\theta = \theta^0 + R_{SD} \frac{\mu_0 C_{ox} W}{L} \approx \theta^0 \propto 1/t_{ox} \tag{7.25}$$

In this case, the Y-function reduces to:

$$Y_B = \sqrt{\frac{W}{L} C_{ox1} V_D \left(\mu_{01} + \mu_{02}\right)} \left(V_{G1} - V_{T1}\right) \tag{7.26}$$

We conclude that the Y-function is still useful and yields an apparent mobility which is the sum of the front and back channel mobilities.

It is worth emphasizing that the extracted mobility is not the real mobility of the device which, in balanced-DG mode, should be close to the average of the two channel mobilities. In a general double-gate device with two independent channels, the total current can be considered as the contribution of the two channels, each proportional to the mobility multiplied by the inversion charge:

$$I_D = I_{D_1} + I_{D_2} \sim \mu_1 Q_1 + \mu_2 Q_2 \tag{7.27}$$

If the device is considered like a "black-box" the total current is proportional to the product of the mobility of the whole device multiplied by its total charge:

$$I_D \sim \mu Q \tag{7.28}$$

Since the total inversion charge is $Q = Q_1 + Q_2$, combining Eqs. 7.27 and 7.28 yields:

$$\mu = \frac{\mu_1 Q_1 + \mu_2 Q_2}{Q_1 + Q_2} \tag{7.29}$$

This means that a low mobility channel can be partially compensated by an opposite high mobility channel; this is in fact the essence of the Velocity Modulation Transistor, VMT, an original proposal to reduce the switching time introduced by Sakagi in 1982 [Sak82]. The concept of velocity modulation transistor is based on a structure with two parallel channels with different transport properties. An ultra short switching time can be obtained taking advantage of the short perpendicular transit time between the two adjacent channels [SGG+05a], [SGG+05c].

If the two gates are biased in order to obtain the same charge in the front and back channels, Eq. 7.21 holds. According to Eq. 7.29, the total mobility, in this case, will be the average:

$$\mu = \frac{\mu_1 + \mu_2}{2} \tag{7.30}$$

7.6.2 Partially depleted transistor

Figure 7.13 shows the $I_D(V_{G_1})$ and $g_m(V_{G_1})$ analytical curves for a PD-SOI transistor operated in DG balanced charge mode. The corresponding V_{G_2} variation is calculated using Eq. 7.22. Taking a look at the V_{G_1} axis in Figure 7.13, the sweep range of the *front* gate voltage is relatively narrow. This may happen in balanced DG operation when the safety range of the voltage applied to one gate limits the voltage on the other gate.

As the two channels are activated and enriched at the same time, there is an increase in the drain current and transconductance compared to the SG operation. The apparent mobility extracted from the Y-function is $600 cm^2/Vs$. This value

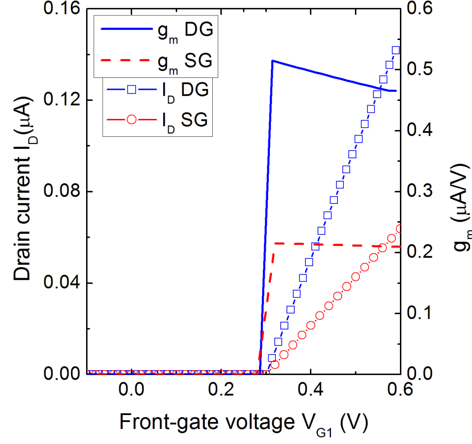


Figure 7.13: Modeled drain current and transconductance curves of a PD-SOI transistor operated in DG balanced charge mode. The back-gate bias is adjusted with Eq. 7.22. An increase in drain current and transconductance is observed in DG mode compared to SG operation. Parameters: $t_{ox_1} = 2nm$, $t_{ox_2} = 145nm$, $V_{T_1} = 0.3V$, $V_{T_2} = 9V$, μ_{01}=$250cm^2/Vs$, $\mu_{02} = 350cm^2/Vs$, $\theta_1 = 0.2V^{-1}$, $\theta_2 = 0.0028V^{-1}$.

corresponds to the sum of both mobilities $(\mu_{01} + \mu_{02})$ and is in perfect agreement with Eq. 7.26.

At this point, the influence of Condition 7.24 on the value of the extracted apparent mobility from the Y-function has been studied, for different reasonable values of θ_1.

As shown in Figure 7.14, a correct extracted value of mobility is obtained if $\theta_2 t_{ox2} \leq \theta_1 t_{ox1}$. For $\theta_2 t_{ox2} > 3\theta_1 t_{ox1}$, the apparent mobility is underestimated. This is due to the stronger impact of θ_2 on the drain current characteristic. In balanced DG mode, for the thicknesses of the front and back insulator considered here, a small change in V_{G_1} results in a significant variation in V_{G_2} that causes the asymmetrical behavior observed in Figure 7.14. For lowers values of θ_1 and θ_2 the underestimation is reduced. The same conclusions apply to FD-SOI transistors.

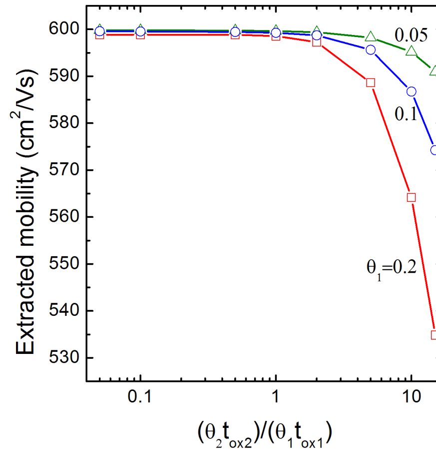


Figure 7.14: Extracted mobility sum when the condition (7.24) is more or less satisfied. Only when $\theta_2 t_{ox2} > 3\theta_1 t_{ox1}$ is the mobility underestimated. Transistor parameters: t_{ox_1}*=2nm*, t_{ox_2}*=145nm*, V_{T_1}*=0.3*, V_{T2}*=9V*, μ_{01}*=250cm*^{2}*/Vs*, μ_{02}*=350cm*^{2}*/Vs*.

7.6.3 Fully depleted transistor

When FD-SOI transistors are operated in balanced DG mode, special care must be taken in the selection of the correct threshold voltage to be used in Eq. 7.22. Figure 7.15(a) shows that the perfect V_{G1} vs V_{G2} bias line (*P2*) must meet the crossing point (DG) of the threshold voltage lines $V_{T_1}(V_{G_2})$ and $V_{T_2}(V_{G_1})$. In all other cases (for example, *P3* line), V_{T_1} and V_{T_2} are not properly defined because a balanced-DG operation implies that the two gates reach inversion together [OPCZ05].

From the simulations (not shown) with *P2* bias, the extracted mobility value with Y-function is 600cm$^2/Vs$ as would be expected from Eq. 7.26.

P3 dotted line corresponds to an incorrect choice where the threshold voltages are taken for zero bias on the opposite gate. Even when using Eq. 7.22, this choice leads to an unbalanced DG polarization and, as a consequence, the *back* gate is activated before the *front* gate. The effect of the wrong threshold voltage choice can also be seen in the transconductance versus front-gate voltage curves (Figure. 7.15(b)). The non-simultaneous channel activation yields two peaks in the transconductance

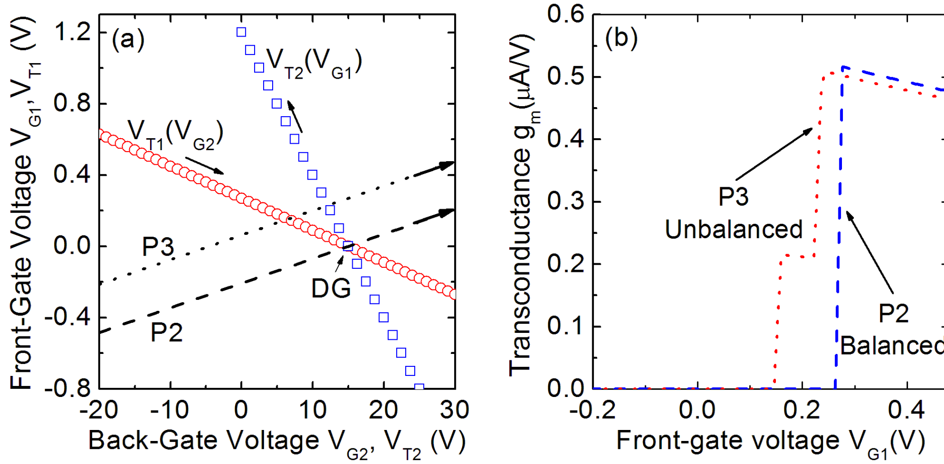


Figure 7.15: **(a)** Analytical choice for the threshold voltage dependencies in the region of interest. Symbols show the variation of the front-channel threshold voltage with back-gate bias and back-channel threshold voltage with front-gate bias. *P2* & *P3*: Balanced double-gate biasing polarization lines corresponding to Eq. (7.22). *P2* bias: Correct choice using the crossing point (*DG*) of the threshold voltage lines. *P3* bias: example of wrong choice defining the threshold voltages for zero bias at the opposite gate. **(b)** Transconductance versus front-gate voltage (the back-gate bias was adjusted with Eq. 7.22). *P2* dashed line: perfect balanced choice for the threshold voltages ($V_{T_1} = 0V, V_{T_2} = 15V$), the activation of both channels is achieved simultaneously. *P3* dotted line: Unbalanced line; back channel opens before front channel.

curves and also affects the current and Y-function. For the wrong choice (dotted line), the transconductance peak is underestimated, as reported in [OPCZ05].

7.7 Experimental results

Once the model basics were established, experimental measurements were performed on actual SOI devices. Both PD and FD transistors were investigated. All measurements were carried out at IMEP-MINATEC facilities in Grenoble (France). Semiconductor parameter analyzer HP4155A (Figure 7.16) was used together with Karl Suss four probe station (Figure 7.16).

45nm technological node wafers were provided by Freescale^{TM} semiconductors.

Figure 7.16: HP4155A Semiconductor parameter analyzer (leftt hand side). Karl Suss four probe station (right hand side).

7.7.1 Partially depleted transistors

PD-SOI transistors had the following characteristics: L=*1*μm, W=*0.15*μm, $T_{ox1} = 1.2nm$, $T_{ox2} = 145nm$, $T_{\mathrm{Si}} = 70nm$. First, the front and back channel mobilities were determined with the Y-function applied to *separate* measurements, $I_{D_1}(V_{G_1})$ and $I_{D_2}(V_{G_2})$, respectively. The values extracted with zero voltage on the opposite gate (depleted opposite channel) were $\mu_{01} = 272cm^2/Vs$ and $\mu_{02} = 384cm^2/Vs$.

The next step was to bias the devices in balanced-DG mode according to Eq. 7.22. Then the apparent mobility was extracted by means of Eq. 7.26. The extracted value is $\mu_{01} + \mu_{02} = 597cm^2/Vs$ which is only 9% lower than the theoretical sum. The small error can be attributed to a slight mismatch in the Condition 7.24 reflected in an underestimation of the apparent mobility as Figure 7.14 shows.

7.7.2 Ultrathin fully depleted transistor

Figure 7.17(a) shows experimental front-channel mobility measured in advanced ultrathin FD-SOI-NMOSFETs, for different back-gate voltages. The transistor parameters were: $T_{\mathrm{Si}} = 10nm$, L=*10*μm, W=*1*μm, $T_{ox1} = 2nm$, $T_{ox2} = 145nm$, $N_A = 10^{15}cm^{-3}$. Figure 7.17(b) shows reciprocal data for the back-channel mobility versus front-gate bias. In this case, the front and back channel mobilities extracted

with Y-function at zero volts applied to the opposite gate are $\mu_{01} = 225cm^2/Vs$ and $\mu_{02} = 381cm^2/Vs$.

Figures 7.17(a) and 7.17(b) fully confirm the results of our analytical study: when only one channel is activated, its low-field mobility remains almost constant (except the effect of the vertical field variation). Increasing the opposite gate bias, the extracted mobility is abnormally overestimated: the methodology fails. Note also that the mobility extracted from the transconductance peaks is underestimated due to the effect of the series resistances.

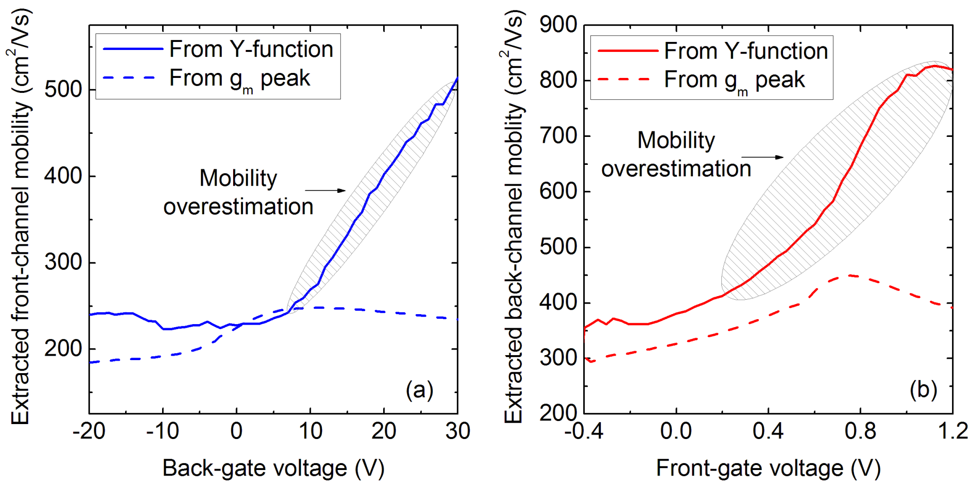


Figure 7.17: **(a)** Experimentally extracted front-channel mobility versus back-gate voltage using the Y-function or the transconductance peak. **(b)** Experimentally extracted back-channel mobility versus front-gate voltage using the Y-function or the transconductance peak. Ultrathin FD MOSFET: T_{Si}=*10nm*, L=*10*μ*m*, W=*1*μ*m*, T_{ox1}=*2nm*, T_{ox2}=*145nm*, N_A=$10^{15}cm^{-3}$.

Figure 7.18(a) shows the threshold voltages extracted from the second derivative of the drain current [CL95] for the *front* and *back* channels versus the opposite gate bias. These intricate coupling dependencies explain the unusual behavior of the back-gate transconductance reproduced in Figure 7.18(b). For $V_{G_1} = 0.1V$ (*B1* bias), when back-gate voltage is increased, the bias line never crosses the *front* threshold voltage curve in Figure 7.18(a) and only the back-channel is activated.

The transconductance features a normal (one peak) behavior.

But in the case of $V_{G1} = 0.7V$ (*B2* bias), the *front* threshold voltage curve is crossed first, implying that the front channel is activated before the back channel. As V_{G_2} is increasing, V_{T_1} is decreasing, so the front-channel current increases until V_{T_1} reaches the saturation value in Figure 7.18(a). The transconductance exhibits two distinct peaks instead of one peak and a plateau. Due to the very thin oxide, the transconductance peak related to the front-channel is higher compared to the second peak, which only reflects the back-channel activation. Of course, the first peak should not be associated with the back channel, otherwise the back mobility would be overestimated.

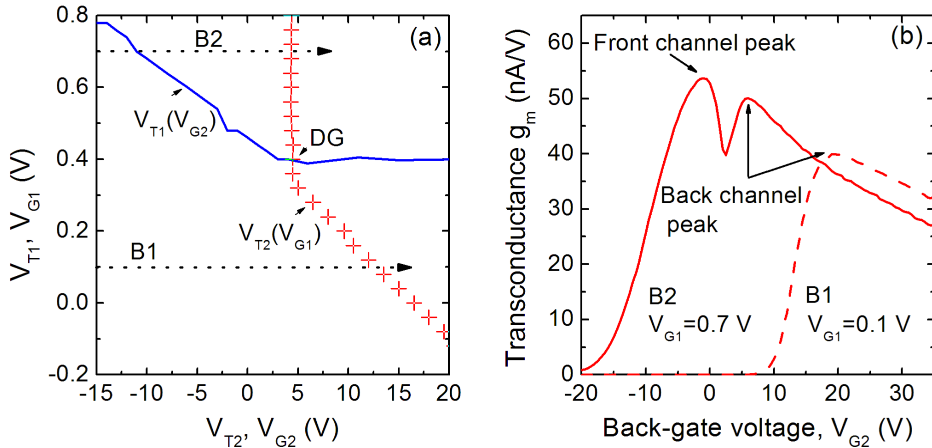


Figure 7.18: **(a)** Experimental threshold voltages (extracted from the peak of the second derivative of the drain current) for the *front* and *back* channels versus the opposite gate bias. *B1* & *B2* dotted lines: Bias conditions corresponding to continuous and dashed curves in Figure 7.18(b). Same device as in Figure 7.17. **(b)** Back-gate transconductance measured for two different front-gate voltages. The activation of *front* channel before *back* channel can be seen in the *B2* curve corresponding to the bias shown in Figure 7.18(a).

The alternative method explained in Section 7.5.2.1 is applied to extract *back*-channel mobility from the *front*-gate Y-function. From Figure 7.19(a) the coupling factor is $k = -\Delta V_{G1}/\Delta V_{T2} = 0.03$, in agreement with Eq. 7.19 which gives

k_{analytic}=*0.036* when $C_{it_1}$is neglected. After biasing the device at $V_{G2} = 17V$ (B3 bias line in Figure 7.19(a)) and selecting a suitable range of V_{G_1} (from point A to point B), we utilize Eq. 7.18. The extracted mobility is $\mu_{02} = 363cm^2/Vs$, about 5% lower than the value extracted from direct measurements with the back-gate Y-function.

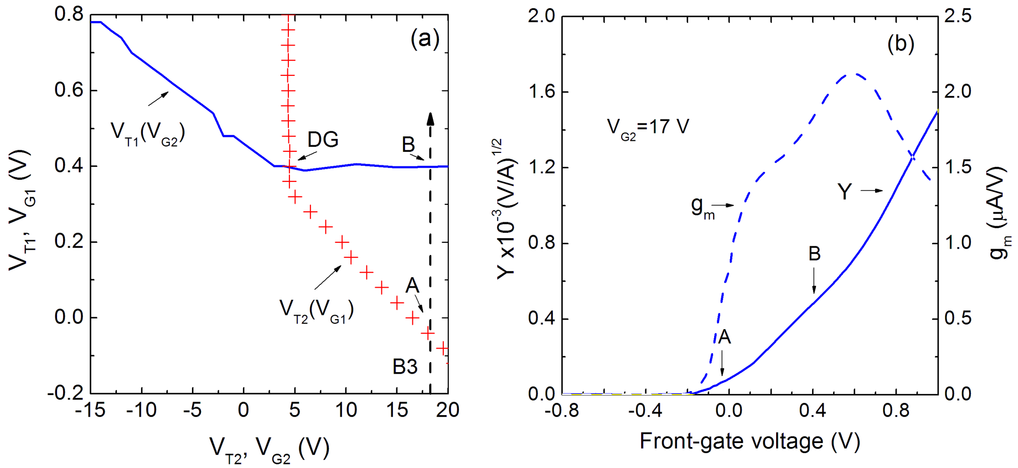


Figure 7.19: **(a)** Experimental threshold voltages extracted from the peak of the transconductance for the *front* and *back* channels versus the opposite gate bias. *B3* dashed line: Bias conditions for extracting the back-channel mobility from the front-gate Y-function. Same device as in Figure 7.17. **(b)** Front gate Y-function (continuous line) and transconductance (dashed line) corresponding to *B3* bias in Figure 7.19 (a).

The transconductance and the Y-function of *B3* bias are represented in Figure 7.19(b). The activation of the front channel can be seen in the slope change of the Y-curve and in the transconductance modification after point B. This figure compares well to the theoretical curves simulated in Figure 7.12.

Finally we contrasted this mobility with the value determined from the mobility "plateau" (Eq.(7.20) applied to region (AB) where $g_{plat} \cong 1.3{\cdot}10^{-6}A/V$). The value obtained, $\mu_{02} = 330cm^2/Vs$, indicates a more severe underestimation of the mobility when the transconductance plateau is used. Table 7.31 summarizes the results.

Method	Back Gate Mobility (cm^2/Vs)
Direct measurement (Eq. 7.12)	381
Front gate Y-function (Eq. 7.18)	363
From g_{plat} (Eq. 7.20)	330
From *back* gate g_{m2} (Eq. 7.1)	327

(7.31)

Table 7.31: Comparison of back channel mobility obtained by various methods.

Know that the mobility extracted from the back-channel transconductance peak (direct measurement) is also underestimated.

7.7.3 Balanced charge double-gate operation

The most interesting results are obtained when the device is probed in balanced-DG mode. The correct bias was selected according to Figure 7.18(a) (or 7.19(a)) and Eq. 7.22. The values of the attenuation parameters (Eq. 7.13) were determined from independent front- and back-channel measurements in order to check the validity of the Condition 7.24: $\theta_1 = 0.3V^{-1}$ and $\theta_2 = 0.0084V^{-1}$, hence $\theta_2 T_{ox2}/(\theta_1 T_{ox1})$= 2.01. Although this value is not equal to 1 as assumed in Eq. 7.24, we may consider, according to Figure 7.14, that the error introduced is low. More importantly, this error is expected to cause an *underestimation* of the apparent mobility.

Measurements in balanced DG mode (Figure 7.20) show an increase in transconductance multiplying the values by almost a factor of three and confirming earlier results [ECG+03]. This data was used to generate the Y-function given by Eq. 7.26. The striking result is that the apparent mobility ($759cm^2/Vs$) is indisputably higher that the sum of front- and back-channel mobilities ($606cm^2/Vs$, Table 7.32). This 25 % gain in mobility represents a very promising asset for FD DG operation, compared to previous cases of PD MOSFETs.

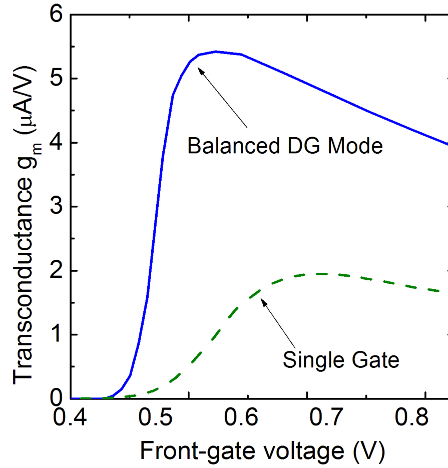


Figure 7.20: SG and DG transconductance measured in an ultrathin FD SOI MOSFET. An increment of 200% is observed for DG operation, which is induced by volume inversion and cannot be explained by a 2-channels model. Same device as in Figure 7.17.

Transistor Type	**Single Gate**		**Double Gate**	
	Extracted		**Theoretical**	**Extracted**
	μ_1 (cm^2/Vs)	μ_2 (cm^2/Vs)	$\mu_1 + \mu_2$ (cm^2/Vs)	$\mu_1 + \mu_2$ (cm^2/Vs)
PD-SOI	272	384	656	597
FD-SOI	225	381	606	759

(7.32)

Table 7.32: Comparison of front- and back-channel mobility in PD and FD transistors operated in single-gate and double-gate mode.

We now have to answer a fundamental question:

Why would the mobility increase in ultrathin FD MOSFETs operated in DG mode? The reason is that the basic hypothesis of our model –the coexistence of two separate channels– is no longer valid: the two channels interact and overlap,

giving rise to volume inversion, [BCB+87], [GRCC+99], [MJW98]. This means that numerous minority carriers in the film volume can move far from the interfaces. These carriers are less affected by surface roughness or remote scattering and benefit from a quasi-null vertical field in the middle of the body [ECG+03], [FL93], [RRG07], [GR03], [EMC+99]. Assuming that minority carriers are more mobile in the volume than at the interfaces, it is reasonable to conclude that the average mobility is higher in DG mode ($\mu > \mu_{01} + \mu_{02}$). An analytical model was proposed by Ernst et al. to explain the substantial transconductance enhancement in DG mode [ECG+03]. Experimental confirmation was obtained by split-CV [EMF+01] and geometric magnetoresistance [CMGC06] measurements.

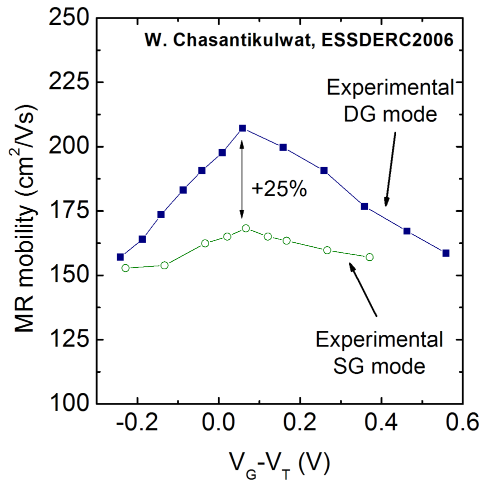


Figure 7.21: Magnetoresistance mobility of a DG transistor operating in DG and SG mode as a function of V_G-V_T. Transistor parameters: t_{Si} =*6nm*, t_{ox1}=t_{ox2}=*2nm*, L_g=*70nm*, *W=10μm.*

For example, in Figure 7.21 the results obtained by W. Chaisanttikulwat et al. [CMGC06] are presented. They used the magnetoresistance technique to extract the magnetoresistance mobility in devices with comparable parameters and technology. The extracted MR mobility at room temperature for SG and DG modes are compared as a function of $V_G - V_T$. The $V_G - V_T$ is used as a criteria for mobility comparison as, from a practical point of view, it corresponds to the real operation

of transistors in a circuit. At a constant $V_G - V_T$ bias, a remarkable mobility improvement is observed in DG mode. The low field mobility gain, just above the threshold voltage ($V_G - V_T = 0.07V$) is about 25%, the same value we obtained in this work. In any case, for a given inversion charge density, the DG mode mobility is significantly higher than in SG mode. At higher effective field, the carriers tend to concentrate near the interface, and the mobility curves for DG and SG mode converge as the mobility is limited by scattering with the interfaces.

Our results rested on the Y-function are the first demonstration of mobility increase in volume inversion, derived from the usual $I_D(V_G)$ characteristics. The advantage of this method resides in its simplicity at both theoretical and experimental levels.

7.8 Conclusions

In this chapter the methodology for mobility extraction in SOI devices has been revisited including the genuine magnetoresistance technique, presented here like a unique method allowing the characterization without needing precise information on the device architecture.

The Y-function has been also revisited. The method has been extended to the case of two separate channels. Simulations show that an accurate mobility value is obtained only if the opposite interface is accumulated or depleted, not inverted. The Y method remains valid in double-gate MOSFETs if adequate biasing conditions enable the same charge in both channels.

The electron mobility has been studied in thick and ultrathin SOI transistors operated in single-gate and balanced double-gate modes. The theoretical results derived in the first part of the chapter has been corroborated: in thick DG devices, Y-function remains valid and the DG apparent mobility is the sum of the front and back mobilities. However, in ultrathin DG transistors, a remarkable increase is observed, which cannot be explained through the two channel model and reveals the beneficial effect of the volume inversion. It has been found that the DG MOSFET structure fully benefits from the mobility gain at low field as a result of the volume inversion.

Chapter 8

Mobility simulation results

8.1 Introduction

In this chapter we complement the previous carrier mobility investigations by numerical simulations of advanced aspects. The electron transport is studied by means of the Monte Carlo method. Three are the main topics considered:

1. The chapter starts studying the behavior of electron mobility in bulk MOSFETs and DG SOI MOSFETs with different surface (hkl) orientations and channel <hkl> directions. For each surface orientation, different channel directions are also considered. In the case of the (110) surface, a strong anisotropy of electron mobility with the channel direction is observed: when the channel is built in the (110)/<001> direction, electron mobility is 50% higher than in (110)/$<1\bar{1}0>$, and is closer to the mobility for a (100)/<001> direction. This anisotropic behavior with channel orientation is not observed in the (100) or (111) surface orientations. The study with silicon thickness also revealed some interesting consequences of the volume inversion effect.

2. The second part of this chapter (Section 8.3) is dedicated to the electron transport in strained double-gate silicon on insulator transistors. Poisson and Schrödinger equations are self-consistently solved in these devices for different silicon layer thicknesses both for unstrained and strained silicon channels. The results show that the strain of the silicon layer leads to a larger population

of the non-primed subbands, thus decreasing the average conduction effective mass. However, strain also contributes to a larger confinement of the charge close to the two Si/SiO_2 interfaces, thus weakening the volume inversion effect, and limiting the potential increase of the electron mobility.

3. Finally, in Section 8.4, the geometric magnetoresistance introduced in Section 7.2.3 as a reliable characterization technique is reproduced by Monte Carlo simulations and used to accurately extract the carrier mobility. This original method allows comparing the transport mechanisms in various cases of interest: Single-Gate (SG) versus Double-Gate (DG) operation, Si-high-k versus Si-SiO_2 interfaces, in-depth inhomogeneous transport.

8.2 Carrier mobility in arbitrarily oriented bulk and SOI MOSFETs

It is well known that the hole mobility for a PMOSFET is much higher when it is formed on a silicon substrate with a top surface having a (110) crystal orientation (an "$Si-(110)$ surface or layer") than when it is fabricated on a silicon substrate with a top surface having a (100) crystal orientation (an "$Si-(100)$ surface or layer").

On the other hand, it is also well known that the electron mobility for an NMOSFET is degraded when it is formed on a $Si-(110)$ surface in comparison to when it is formed on a $Si-(100)$ surface. Because of this opposite behavior of electron and hole mobility, it is difficult to integrate an NMOSFET and a PMOSFET on the same substrate while maintaining satisfactory performance from both devices. For these reasons, the search of an intermediate situation, in terms of the optimal orientation is one of the interest areas of this work.

In addition, SOI technology is making possible new architectures such us double-gate and FinFETs, allowing the achievement of different crystallographic orientations for the active areas of the device without using non-standard wafer substrates [CIY04].

If we consider a DG-MOSFET on a standard (100) wafer, where the gate and active area are aligned either perpendicular or parallel to the wafer flat, the device

channel lies on the (110) plane. However if the transistor layout is rotated 45° in the plane of the wafer, then the resulting orientation of the device channel is (100). An intermediate rotation yields electron mobilities between those observed in the (100) and (110) orientations, imitating the behavior of a (111) surface [CIY04].

Thus, to achieve (100), (110), and (111) crystallographic orientations, the devices could simply be drawn at a different angle relative to the wafer flat or notch, as is represented in Figure 8.1. However, measured mobilities for (100), (110), and (111) bulk silicon surfaces [YGM+03] show that by shifting away from (100) surface orientation, hole mobility is improved while electron mobility is degraded.

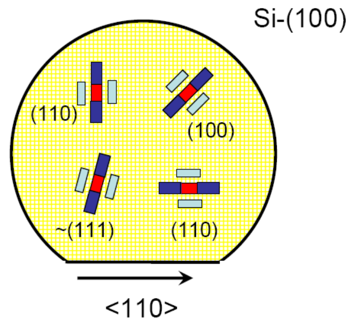


Figure 8.1: Different orientations of DG-MOSFETs on a Si-(100) wafer.

The study of the electron transport properties for different surface crystallographic orientations, and different channel directions is therefore timely and interesting for the further exploitation of the FET based technology.

When non-(100) surface orientations are used, the electron and hole mobilities are modified due to the anisotropy of the carrier effective masses in the silicon crystal lattice [STH71], [SH70]. Table 8.1 summarizes the values of the masses for the common surface orientations, *i.e.* (100), (110), and (111). m_3 is the effective mass perpendicular to the surface, while m_1 and m_2 are the principal masses of the constant energy ellipse in the surface. The degeneracy of each set of ellipses is n_v [SH70].

Wafer ($\mathbf{m_3}$) /channel ($\mathbf{m_1}$)	$\mathbf{m_1}$ (channel)	$\mathbf{m_2}$	$\mathbf{m_3}$ (confinement)	$\mathbf{n}_v$
(100) /[001]	m_t	m_t	m_l	2
	m_t	m_l	m_t	2
	m_l	m_t	m_t	2
(110) /[001]	m_t	$(m_t + m_l)/2$	$2m_t m_l/(m_t + m_l)$	4
	m_l	m_t	m_t	2
(111) /[$\overline{2}$$\overline{1}$1]	$(m_l + 2m_t)/3$	m_t	$\frac{3m_t m_l}{(m_t+2m_l)}$	2
	$\frac{(2/3)m_t(2m_l+m_t)}{m_l+m_t}$	$(m_l + m_t)/2$	$\frac{3m_t m_l}{(m_t+2m_l)}$	4

(8.1)

Table 8.1. Effective masses in the device coordinate system for (100), (110) and (111) surface orientations.

Assuming that in silicon, $m_l = 0.91m_0$ and $m_t = 0.19m_0$, with m_0 the free electron mass, the different effective masses have the numerical values shown in Table 8.2.

Wafer orientation ($\mathbf{m_3}$) /channel orientation ($\mathbf{m_1}$)	$\mathbf{m_1}$	$\mathbf{m_2}$	$\mathbf{m_3}$	$\mathbf{n}_v$
(100) /[001]	0.19	0.19	0.916	2
	0.19	0.916	0.19	2
	0.916	0.19	0.19	2
(110) /[001]	0.19	0.553	0.315	4
	0.916	0.19	0.19	2
(111) /[$\overline{2}$$\overline{1}$1]	0.432	0.19	0.258	2
	0.232	0.553	0.258	4

(8.2)

Table 8.2. Numerical values of the effective masses in the device coordinate system for (100), (110) and (111) surface orientations.

The constant-energy ellipsoids associated with the silicon lattice are presented in Figure 8.2 while the constant energy ellipses associated with motion parallel to the

interface for three common crystallographic surface orientations (100), (110), and (111) [SH70] are presented in Figure 8.3.

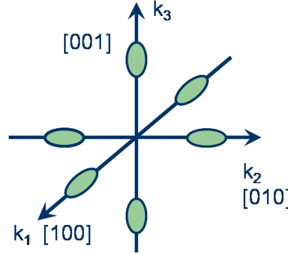


Figure 8.2: Constant energy ellipsoids for Si conduction band.

It is well known that in the case of Si-(100), two of the six bulk constant energy ellipsoids will give $m_3 = m_l$ (non-primed subbands) while the other four will give $m_3 = m_t$ (primed subbands). As $m_t < m_l$, non-primed subbands will have lower energy (also lower conduction mass) than primed subbands (Figure 8.3(a)).

Similarly, in the case of the (110) orientation, two sets of subbands are also obtained: two bulk energy ellipsoids have an effective mass perpendicular to the interface $m_3 = m_t$ while the other four have higher quantization masses: $m_3 = 2m_t m_l/(m_t + m_l)$. Therefore, these four ellipsoids will provide lower energy subbands (Figure 8.3(b)).

Finally, in the case of the (111) crystallographic orientation (Figure 8.3(c)), the six ellipsoids have the same quantization mass, and therefore only one set of subbands is possible. Due to the different quantization masses, electron distribution, subband energy levels, wavefunctions, form factors and scattering rates depend on the surface orientation.

In addition, as observed in Figure 8.3, the effective masses of the constant-energy ellipses associated with the motion in the parallel direction can be somewhat anisotropic. As a consequence, it is possible to see anisotropic conduction, *i.e.*, once the quantization direction is fixed, conduction, and therefore, mobility, depend on the direction of the drift electric field, i.e., the direction of the channel in the surface.

Section 8.2.1 will show the results obtained for Bulk MOSFETs while the results for SOI devices will be presented in Section 8.2.2. In both cases we obtained the

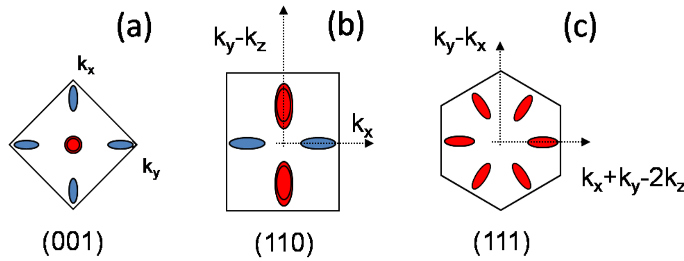


Figure 8.3: Two-dimensional schematic constant-energy ellipses for (001), (110), and (111) Si conduction band [SH70]. Lower energy subbands are shown in red.

self-consistent solution of Poisson and Schrödinger equations with different crystallographic orientations and mobility curves calculated using a Monte Carlo simulator, for different combinations of surface and channel directions. For the DG SOI MOSFETs case the impact of the silicon thickness is also considered.

8.2.1 Electron mobility in bulk MOSFETs

The electron mobility was studied using a one electron Monte Carlo simulator [GF01]. Only phonon scattering and surface-roughness scattering is taken into account. Coulomb scattering is not considered in the simulations due to the low doping level of the actual silicon films. The Si-SiO_2 interfaces were characterized by the following roughness parameters: $L_{sr} = 1.5nm$, $\Delta_{sr} = 0.4nm$.

8.2.1.1 (100) wafers

In conventional planar Si technology, (100) crystal orientation is generally used for MOSFETs and the device channel is usually oriented parallel to the primary flat (Figure 8.4). As can be seen in Figure 8.3(a) and Table 8.2 we can distinguish two set of subbands: two non-primed subbands with larger confinement mass (lower energy levels) and isotropic conduction mass, and four primed subbands with lower confinement mass (higher energy levels) and anisotropic conduction mass [SH70].

The relative electron population of the non-primed and primed subbands is represented in Figure 8.5(a). For low inversion charge, most of the electrons populate the primed subbands presenting anisotropic conduction mass. Although the ground

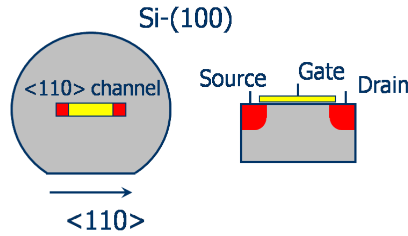


Figure 8.4: Schematic representation of a MOSFET transistor fabricated on a (100) Si wafer.

level of the primed subbands is higher than the corresponding to the non-primed, the four-degenerancy compensates this difference, giving for the total balance more population in the primed-ones.

As the inversion charge increases (i.e. the quantum well becomes narrower), the energy levels of the non-primed and primed subbands split up; the four primed ellipsoids with higher ground level can not compensate the population of the non-primed ones when the energy level differences rise: the relative population of the non-primed subbands increases and as a consequence the conduction mass becomes isotropic.

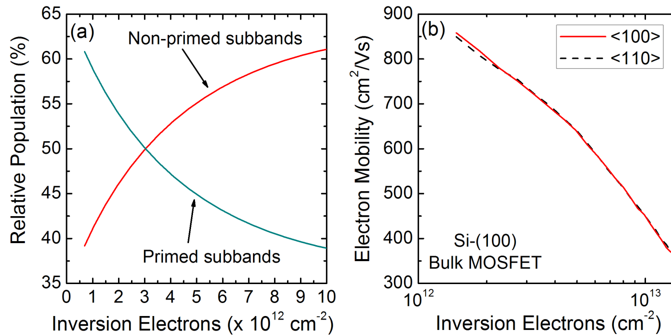


Figure 8.5: **(a)** Relative primed and non-primed subbands population as a function of the inversion electron density. For high inversion charge most of the electrons populate the non-primed subbands with isotropic conduction mass. **(b)** Electron mobility as a function of the inversion charge in a (100) −MOSFET for two channel directions.

The first result that is possible to observe is the weak dependence of the mobility

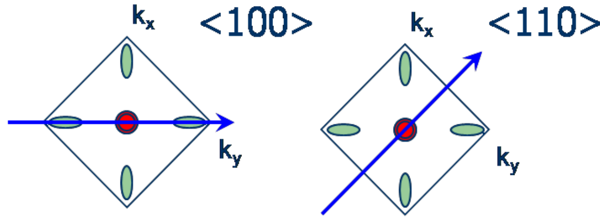


Figure 8.6: Two-dimensional schematic constant energy ellipses for (100) confinement crystallographic orientation. Channel ⟨100⟩ and ⟨110⟩ directions are presented.

with the channel orientation due to the high population of the non-primed subbands for high inversion density. Quantization mass does not change. When the mobility is evaluated for the ⟨100⟩ and ⟨110⟩ channel directions (Figure 8.6), the transport is not much affected and only a slight difference is seen at low inversion density when primed subbands are more populated (Figure 8.5(b)).

8.2.1.2 (110) **Wafers**

(110) substrates are very interesting from the technological point of view, since (110) wafers represent one of the mobility boosters for holes: hole mobility is more than doubled on (110) silicon substrates with current flow direction along ⟨110⟩ in comparison with conventional (100) substrates and ⟨100⟩ channels [YIS+03].

A look at Figure 8.7 will anticipate that the transport anisotropy will be the predominant fact for this wafer orientation. The quantization splits the Si conduction band minima into two groups of isoenergetic ellipses. Four low energy valleys with anisotropic mass over the $k_y - k_z$ axis ⟨011⟩ and two high energy valleys over the k_x axis.

The associated masses corresponding to the low energy valleys in the ⟨100⟩ and ⟨011⟩ transport directions are:

$$m^{(110)}_{\langle 100\rangle l} = m_t \tag{8.3}$$

$$m^{(110)}_{\langle 011\rangle l} = \frac{m_t + m_l}{2} \tag{8.4}$$

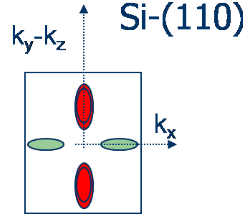


Figure 8.7: Two-dimensional schematic constant energy ellipses for (110) confinement crystallographic orientation. Channel ⟨011⟩ and ⟨100⟩ directions are presented.

and for the high energy valleys:

$$m^{(110)}_{\langle 100\rangle h} = m_l \tag{8.5}$$

$$m^{(110)}_{\langle 011\rangle h} = m_t \tag{8.6}$$

The relative subband population is represented in Figure 8.8(a). In contrast to the result of 8.5(a), the relative population is always higher in the non-primed subband for all the inversion charge range.

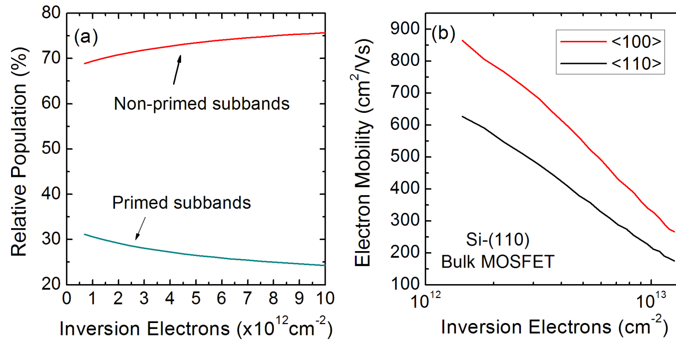


Figure 8.8: **(a)** Relative primed and non-primed subbands population as a function of the inversion electron density. For all the inversion charge range, most of the electrons populate the non-primed subbands with anisotropic conduction mass. **(b)** Electron mobility as a function of the inversion charge in a (110) −MOSFET for two channel directions.

Based on the previous results, it is easy to explain the evolution of the mobility

observed in Figure 8.8(b). The higher mobility values are obtained for ⟨100⟩ transport direction; this is in accordance with Figure 8.8(a) and Equations 8.3, 8.4, 8.5 and 8.6. The most populated subbands are the non-primed, which present lower effective conduction mass for the ⟨100⟩ channel orientation (Eq. 8.3) and therefore higher mobility.

8.2.1.3 (111) wafers

The special feature of (111) wafers is that the quantization does not split the degeneracy of the Si conduction band minima. The constant energy ellipses represent six equivalent valleys with anisotropic conduction mass (Figure 8.9). But, as a consequence of the isotropic position of the ellipses there is no effect on the mobility for different channel orientations (Figure 8.10).

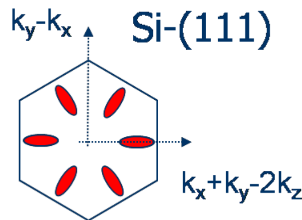


Figure 8.9: Two-dimensional schematic constant energy ellipses for (111) confinement crystallographic orientation. The quantization does not split the degenerancy of the Si conduction band minima.

Considering the results presented, the following conclusions hold:

1. Electron mobility strongly depends on quantization direction and channel orientations.

2. Electron mobility is higher in Si-(100) wafer orientation regardless of the channel orientation due to the lower conduction mass.

3. Isotropic conduction is observed in Si-(100) as well as in Si-(111).

4. Anisotropic conduction is observed in Si-(110) wafers.

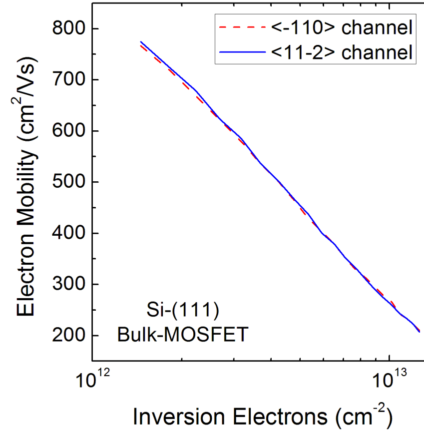


Figure 8.10: Electron mobility as a function of the inversion charge in a (111)-MOSFET for two channel directions.

8.2.2 Double Gate structures

With the adoption of double-gate structures it is possible to obtain different quantization directions and channel orientations easily. This fact opens a new range of possibilities for future improvement of the technology based on the most favorable selection of the device axis.

Figure 8.11 illustrates the flexibility of non-planar technology for the implementation of alternative orientations.

8.2.2.1 Silicon thickness and surface orientation

The self-consistent Poisson-Schrödinger solver was described in Section 1.3. For all the calculations, a DG-MOSFET with the following features was assumed: undoped silicon channel, gate oxide thickness equal to 1nm and different silicon thickness and surface orientations.

Figure 8.12 shows the electron distribution for the three common crystallographic orientations in a DG-MOSFET with silicon thickness of $T_w = 5nm$ and $T_w = 12nm$. The inversion charge concentration is $N_{inv} = 2.5 \times 10^{12} cm^{-2}$.

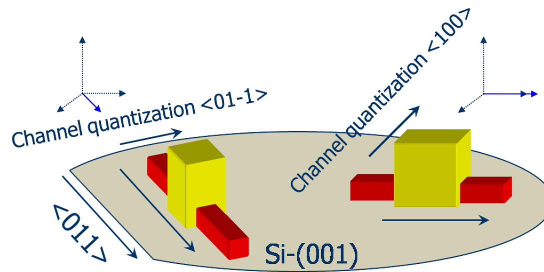


Figure 8.11: Schematic representation of alternative quatization and channel crystallographic orientations for DG-FETs on a (100) silicon wafer.

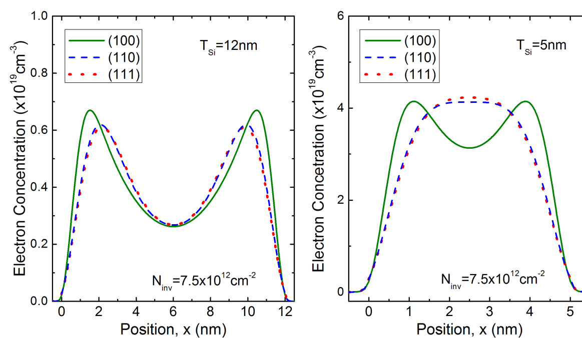


Figure 8.12: Electron distribution in a DG-MOSFET for different surface orientations and different silicon thicknesses.

As observed in Figure 8.12, the electron distribution for (110) and (111) crystallographic orientations is quite similar. However it is quite different from the electron distribution for (100). This fact can be explained by looking at Table 8.2. The quantization masses, m_3, for (110) and (111) crystallographic orientations are comparable, but very different to that for (100) The higher quantization mass in Si-(100) produces lower energy subbands in the two-valleys with a longitudinal mass perpendicular to the interface (Figure 8.3 and Figure 8.13). For thin silicon layers or high inversion charge concentrations (i.e. when quantum effects are more important) these two subbands are more populated than the others, and the electrons become more confined to the Si-SiO_2 interfaces (larger confinement mass).

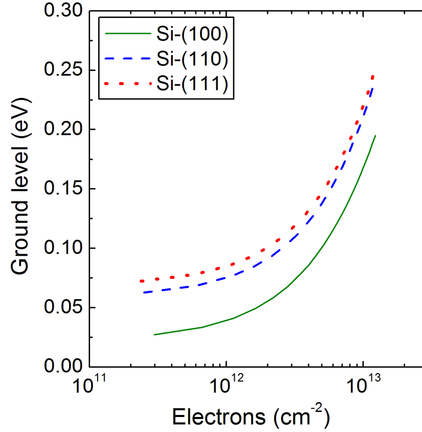


Figure 8.13: The higher quantization mass in the Si-(100) orientations produces lower sub-band - levels (electrons are more confined to the Si/SiO_2 interface).

8.2.2.2 Mobility results

As in the bulk section, mobility is studied for different orientations and DG-MOSFET film thicknesses. The same scattering mechanisms and parameters are used: only phonon scattering and surface-roughness scattering are taken into account. As usually, Coulomb scattering is not considered in the simulations due to the undoped silicon layers. The Si-SiO_2 interfaces featured the following parameters: $L_{sr} = 1.5nm$, $\Delta_{sr} = 0.4nm$.

As expected, the first result (Figure 8.14) is the strong dependence of the mobility with the surface orientation. Higher mobility values are obtained for the (100) wafers, corresponding to lower conduction mass, as shown in Table 8.2. The other two orientations have larger conduction effective masses and therefore lower mobility values. As observed experimentally [YGM+03], electron mobility can be degraded by a factor of two for the (110) / $\langle 1\bar{1}0 \rangle$ orientation. However this degradation is much less if a different channel direction (110) / $\langle 001 \rangle$ is selected for the same surface orientation (110).

As shown just above, one remarkable result is the strong anisotropy of the mobility in the (110) surface for different channel directions. The mobility value for a

⟨001⟩-channel orientation is 50% larger than that for a $\langle 1\bar{1}0 \rangle$ channel direction. Taking into account Figure 8.3(b) and Table 8.2 for the (110) case, the subbands with lower energy values (higher m_3) correspond to the four ellipses with major axes in the $\langle 1\bar{1}0 \rangle$ direction. Therefore these subbands become more populated and dominate the transport. If we apply a drift electric field in the ⟨001⟩ direction, these subbands have an effective mass in the drift direction equal to $m_{drift} = m_1 = 0.19 m_0$. On the other hand, if we apply a drift electric field on the $\langle 1\bar{1}0 \rangle$ direction, the conduction effective mass is $m_{drift} = m_2 = 0.553 m_0$, almost three times higher than in the ⟨001⟩ direction. This produces the remarkable difference in mobility shown in Figure 8.14 for these two channel directions. In addition, the anisotropy becomes stronger as the silicon thickness decreases. For the (100) orientation, as the layer thickness decreases, two opposite effect competed: the phonon scattering (decreasing the mobility) which is cancelled by the intersubband modulation (increasing the mobility). For the (110) and (111) orientations there is not intersubband modulation effect, being the phonon scattering increase responsible for the monotonous mobility decrease with the layer thickness.

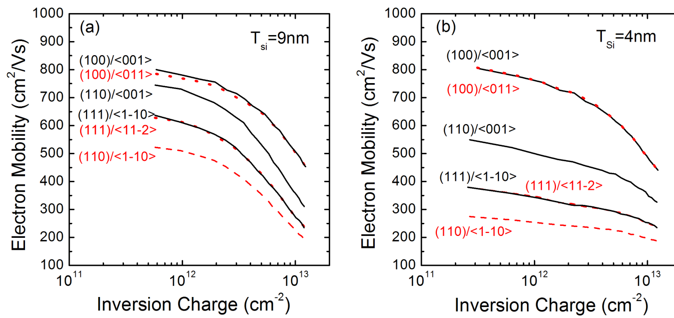


Figure 8.14: Electron mobility as a function of the inversion charge in a DG MOSFET for different surface orientations (hkl) and different channel orientations $\langle hkl \rangle$ for two different Si film thicknesses: (a) 9nm, (b) 4nm.

The anisotropy of the electron mobility with the channel orientation is not observed when we considered other surface orientations. In the case of the (100) surface orientation, as was mentioned for the bulk case, the subbands with lower energy correspond to the two bulk ellipsoids with $m_3 = m_l$, which are indicated by two circles

in Figure 8.3(a).

These two subbands showed the same drift mass (m_t) regardless of the drift electric field orientation. On the other hand, the other four subbands (corresponding to $m_3 = m_t$) present a different effective mass in the x and y directions. Only when the contribution of these four high-energy subbands to conduction becomes significant, we do observe a dependence of mobility on channel orientation. For example, a slightly anisotropic behavior can be seen in Figure 8.14(a): a slight dependence of the mobility curves for $< 001 >$- and $< 011 >$- channel directions at low inversion charge concentrations is observed for the (100) surface orientation. This effect does not appear in Figure 8.14(b), where the silicon thickness is T_{Si}=*4nm*.

No anisotropy is observed in the (111) surface orientation. In this case, the anisotropy shown in Figure 8.3(c) does not lead to an anisotropic conductivity because the ellipses are symmetrically placed.

The results of the evolution of electron mobility with silicon thickness for the different surface and channel orientations considered are shown in Figure 8.15. As in the case of DGSOI (100) devices [GF01], [EMC+03], electron mobility increases as the silicon thickness decreases until a maximum is reached, then abruptly falls for smaller silicon thicknesses [GF01]. As can be seen, for all surface orientations and channel directions, there is a range of fin thicknesses where electron mobility is higher than in bulk MOSFETs. However, the silicon thickness interval where electron mobility is improved depends on the particular surface/channel combination.

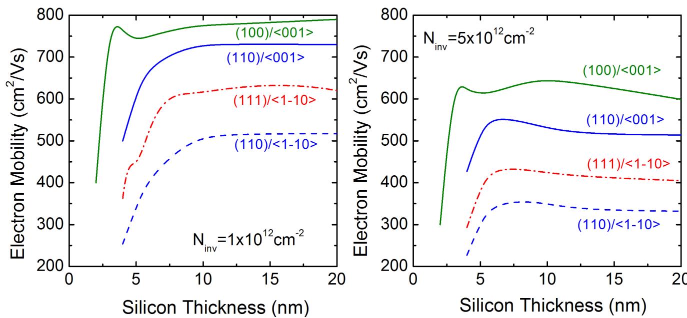


Figure 8.15: Evolution of the electron mobility in a DG MOSFET with the silicon thickness for different combinations of surface orientation (khl) and channel direction $\langle hkl \rangle$.(a) N_{inv} =$10^{12}\,cm^{-2}$; (b) N_{inv} =$5{\times}10^{12}\,cm^{-2}$.

The mobility peak observed for $Si-(100)$ below 5nm can be explained in terms of the subband population inversion. Figure 8.16 shows the non-primed and primed subbands population as a function of the silicon thickness for (100) and (110) confinement orientations. First, we focus our attention in the (100) orientation (Figure 8.16a). For high inversion charge (Figure 8.16(a), $N_{inv} = 1.5 \times 10^{13} cm^{-2}$) the non-primed subbands are always more populated due to the electrical confinement. By contrast, for low inversion charge (Figure 8.16(a) for $N_{inv} = 1.5 \times 10^{12} cm^{-2}$) and thick layers (i.e. wide physical potential well, $Tsi > 7nm$), the more populated valleys are the primed with higher conduction mass (Figure 8.3(a)). This is the same state observed in bulk MOSFET and explained in section 8.2.1.

For low inversion charge, as the layer thickness decreases, and therefore the potential well becomes narrower, the non-primed valleys become more populated (band population inversion) with lower conduction mass (m_t), responsible for the mobility peak at low inversion charge. This is a good example of how the physical confinement can play the role of the electrical confinement.

For (110) confinement orientation this effect does not appear because in any case non-primed subbands with multiplicity four are the most populated subbands.

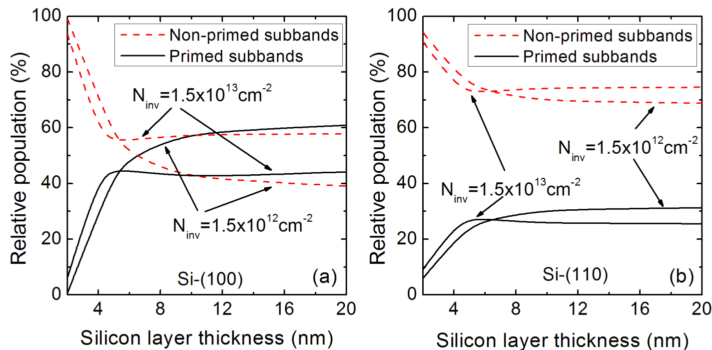


Figure 8.16: Subbands population as a function of the silicon thickness for two values of the inversion charge. Two confinement orientations are presented: **(a)** Si-(100), **(b)** Si-(110).

8.3 Low-field mobility simulation in strained double-gate SOI transistors

In the previous Section, the mobility improvement results, achieved by using alternative orientations, were presented. The other burning topic for mobility boostering based on conventional technology is the enhancement of carrier mobility in the MOSFET channel by the introduction of strained silicon. Both theoretical and experimental studies have shown spectacular electron mobility enhancements when silicon is grown pseudomorphically on relaxed $Si_{1-x}Ge_x$ [N+93], [TO97].

Figure 8.17 shows the lattice constant modification when the biaxial strained silicon is grown over $Si_{1-x}Ge_x$. The Ge lattice constant is larger than the Si one. As a consequence, the result is a monocrystalline Si with a lattice constant different from the relaxed crystal.

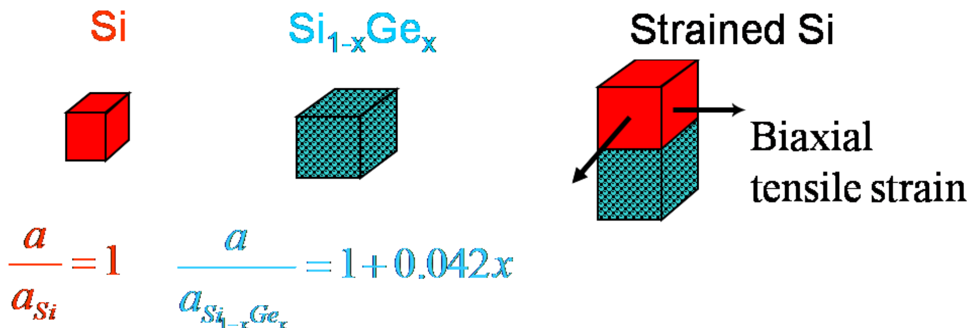


Figure 8.17: Lattice constant modification when Si is grown on $Si_{1-x}Ge_x$.

The strain causes the six-fold degenerate valleys of the silicon conduction band minimum to split into two groups: two lowered valleys with the longitudinal effective mass perpendicular to the interface and four raised valleys with the longitudinal mass parallel to the interface. This leads to a redistribution of the carriers between the different valleys. In the lowered valleys, which are more densely populated in the strained case, electrons show a smaller conduction effective mass (transverse mass, Figure 8.18).

In addition, the splitting between the valleys is enough to weaken the interval-

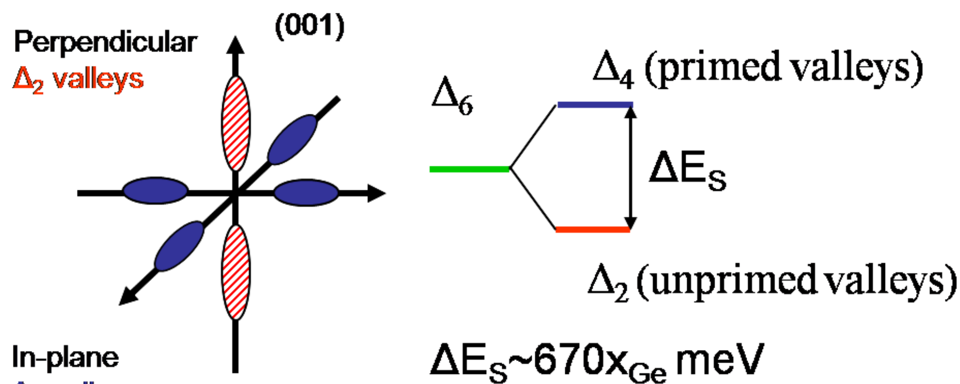


Figure 8.18: Schematic representation of the isoenergetic ellipsoids when biaxial strain is applied on the plane parallel to the channel.

ley transitions of electrons from lower valleys to upper valleys, thus reducing the inter-valley phonon scattering rate compared with that of unstrained silicon. The combination of a lower effective mass and reduced intervalley scattering gives rise to higher electron mobility. Moreover, the lower intervalley-scattering rates make energy-relaxation times higher, causing spectacular electron velocity overshoot, as shown in Reference [RGLVC96].

In spite of these important advantages, bulk strained $Si/Si_{1-x}Ge_x$ CMOS technology still suffers from some of the limitations of standard silicon CMOS technology for sub-0.1μm applications. In contrast to strained-Si/SiGe technology, SOI technology is fully compatible with existing standard silicon fabrication facilities and, a priori, CMOS circuit designs could be translated to ultrathin SOI technology without much difficulty. Recently these two options have been merged and ultra-thin body SOI devices with strained silicon have been proposed. In particular, the possibility of obtaining strained-silicon on insulator without the need for a SiGe layer has been demonstrated [YCM06], thus avoiding the drawbacks caused by the presence of this alloy and allowing thinner semiconductor layers to suppress short-channel effects [RCS+03].

On the following pages we present the simulation results for double-gate planar sSi devices.

8.3.1 Self-consistent solution of Poisson and Schrödinger equations

Self-consistent calculations have been performed for strained DGSOI for different values of the silicon thickness and different levels of strain. Conventional Si-(100) crystallographic orientation was considered. Following the experimental work of the IBM group [RCS+03] and previous results with single-gate strained-Si/SiGe-on-Insulator structures [RGLVC96], we consider in this work ultrathin strained Si directly on insulator and corresponding DGSOI MOSFETs (Figure 8.19).

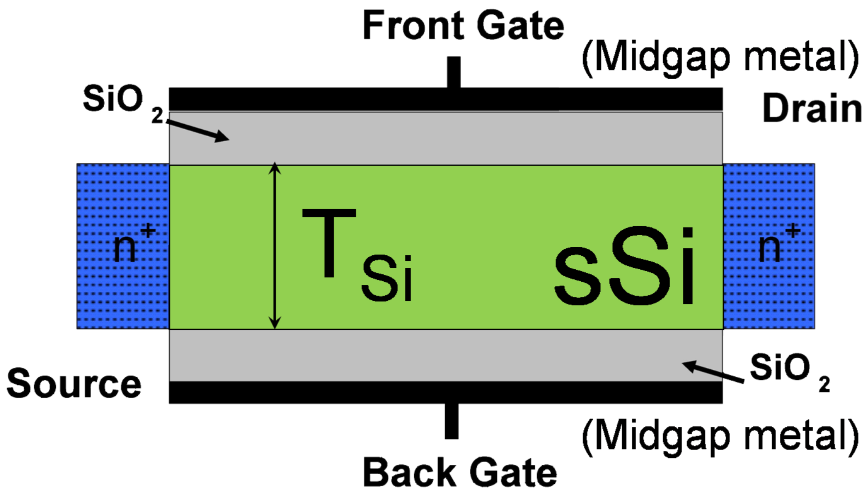


Figure 8.19: Schematic of a strained DGSOI MOSFET

In these devices, the strained-Si layer is directly sandwiched between two oxide layers and no $SiGe$ layer is needed. The structure is fabricated by the layer transfer technique ([RCS+03] and references therein): a thin layer of strained Si is epitaxially grown on a buffer layer of relaxed $Si_{1-x}Ge_x$.

The amount of strain in the Si layer will depend on the Ge mole fraction of the buffer layer. Once the strain layer is formed on the $SiGe$ buffer, it is separated from the $SiGe$ layer bonded to the handle substrate. In the following, Ge mole fraction of the buffer layer, is used to indicate the amount of strain in the Si layer. In all cases, two 1nm-thick silicon-dioxide layers and midgap metal gates are assumed.

Figure 8.20 shows the electron density and the potential well in a strained (100)-

DGSOI MOSFET. Figure 8.21 shows the electron distribution in a strained DGSOI MOSFET for a silicon thickness of $T_{\mathrm{Si}} = 3nm$ and a strain corresponding to $x_{Ge} = 0.4$. For the sake of comparison, the electron distribution for the unstrained case is also shown.

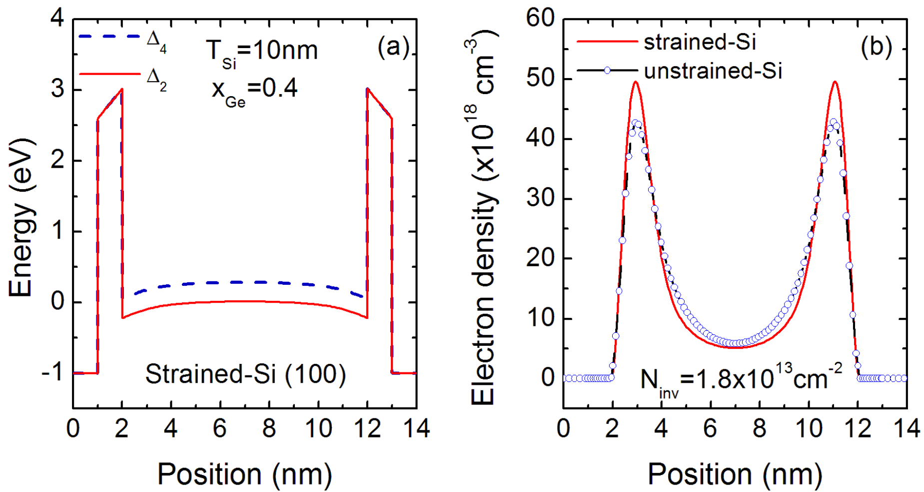


Figure 8.20: **(a)**: Potential well in a strained DGSOI MOSFET. Silicon thickness was assumed to be 10 nm. Solid line shows the conduction band edge for the two valleys with longitudinal effective mass perpendicular to the interface (Δ_2) while dashed line represents the conduction band edge for the four valleys with transverse effective mass perpendicular to the interface (Δ_4). **(b)**: Electron density in a strained DGSOI MOSFET (solid line) and an unstrained DGSOI MOSFET (symbols) for the same value of the inversion charge concentration.

A first result observed in Figure 8.20(b) and Figure 8.21 is that strain tends to slightly reduce the volume inversion effect since the electron concentration in the center of the channel decreases as the strain increases.

It can be observed that the strain produces a greater separation between unprimed and primed levels. The effect caused by the strain is similar to that produced in unstrained DGSOI devices as the silicon thickness decreases [GF01]. The greater separation between unprimed and primed valleys produces a redistribution of the carriers among the different subbands and as a consequence, the unprimed valley tends to be much more populated for all the inversion charge range.

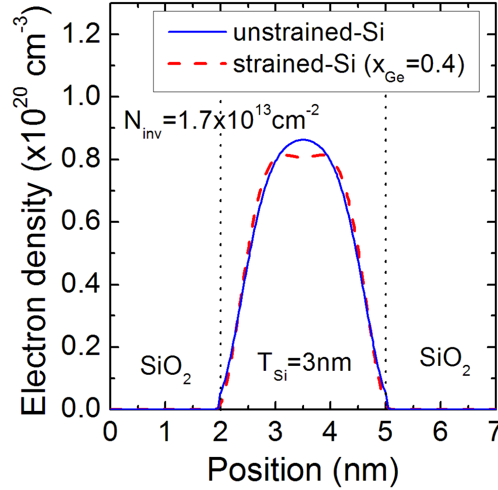


Figure 8.21: Electron density in a strained DGSOI MOSFET (solid line) and an unstrained DGSOI MOSFET (dashed line) for the same value of the inversion charge concentration.

Figure 8.22 shows the evolution of the energy level of the ground subband of each subband ladder (unprimed subbands, Δ_2, and primed subbands, Δ_4).

This effect is greater for the thinner silicon layers, which feature a larger population of the unprimed subbands even in the absence of strain. This redistribution of carriers among the different subbands has an important effect on the electron transport properties because the conduction effective mass of the electrons in unprimed subbands is much lower than the conduction effective mass in primed subbands and, as a consequence, the average conduction effective mass decreases as the strain increases.

Figure 8.23 shows the average conduction effective mass as a function of the strain (Ge mole fraction). The reduction of the conduction effective mass implies a decrease in the inertia of the carriers and therefore an increase in electron mobility. However, this effect saturates for Ge mole fractions greater than ~ 0.2, which means that for larger increases of the strain, the average conduction effective mass (which has reached its minimum value, m_t, i.e., most of the electrons populate the unprimed valleys) cannot decrease any further.

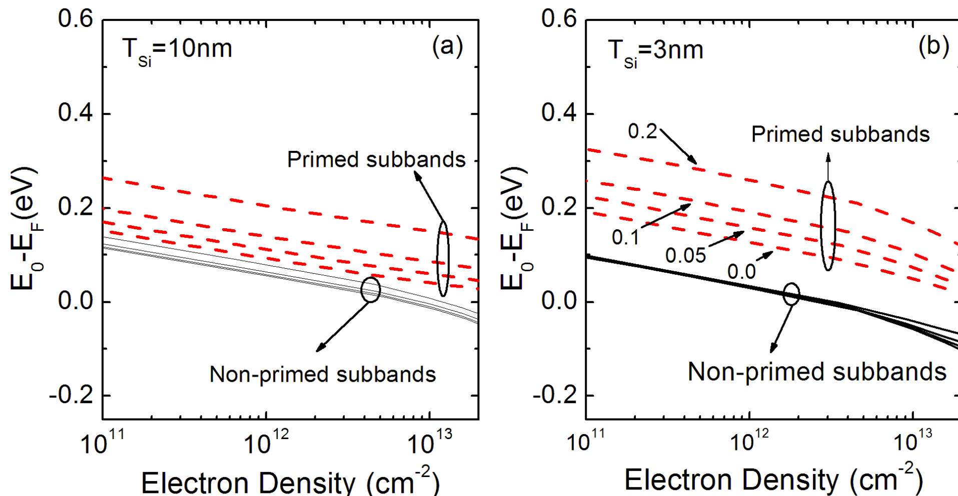


Figure 8.22: Difference between the energy level of ground subband for unprimed and primed valleys and the Fermi level as a function of the electron density. Different Ge mole fractions have been considered. Strained-Si thickness: (a) $T_w = 10nm$, (b) $T_w = 3nm$.

In addition to the reduction of the average conduction effective mass, the greater separation between unprimed and primed subbands also produces a decrease in the intervalley scattering rate between non-equivalent valleys.

Both facts, reduction of the conduction effective mass and reduction of the intervalley scattering rate imply an increase in electron mobility.

8.3.2 Monte Carlo mobility results

Figure 8.24 shows the phonon-limited electron mobility in strained DGSOI transistors for different values of silicon thickness and different values of strain, calculated using a Monte Carlo simulator [GF01].

From observation of Figure 8.24, the following facts can be deduced:

1. For the thicker sample (8.24a), electron mobility increases as the strain increases, although the increase tends to saturate for the higher amount of strain. The saturation of the average conduction effective mass shown in Figure 8.23 is the factor responsible for this behavior. This effect is more evident in the

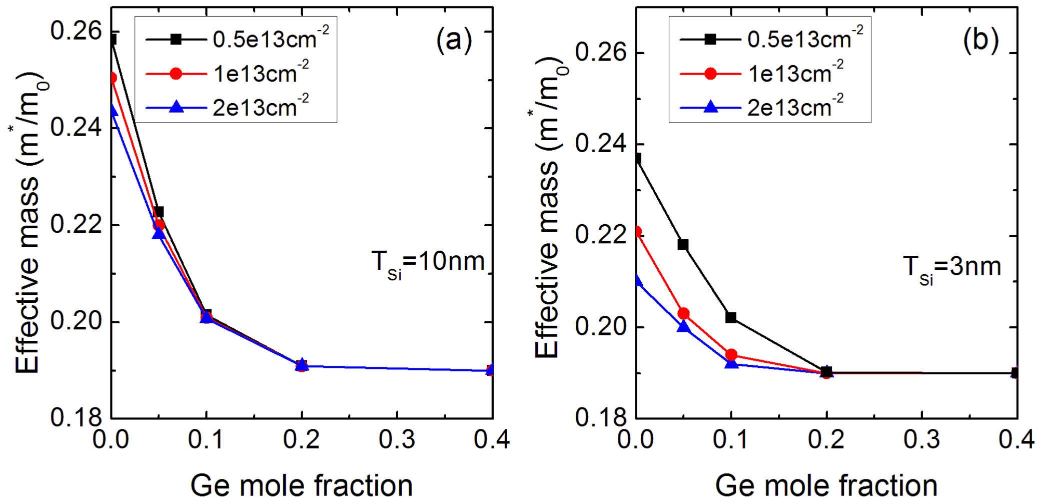


Figure 8.23: Evolution of the conduction effective mass with the strain in a sDGSOI transistor for two values of the silicon thickness and three values of the electron density.

thinner sample ($T_{\mathrm{Si}} = 3nm$) where mobility curves for $x = 0.2$ and $x = 0.4$ coincide as was observed for the same strain grade in Figure 8.23b.

2. If the phonon limited mobility curves for $T_{\mathrm{Si}} = 10nm$ and $T_{\mathrm{Si}} = 3nm$ are compared, it is observed that in the unstrained case (dashed line), the mobility in the thinner sample is higher than that in the thicker silicon layer.

   However, in the strained devices, the trend is the opposite, i.e., the electron mobility is higher in the thicker sample than in the thinner one. The increase in the mobility in unstrained double-gate transistors as T_{Si} decreases has been explained by volume inversion effect [GF01]. However, in Section 8.3.1 it was showed that volume inversion effect is weakened in strained DGSOI devices. This is why the change in the electron mobility in strained DGSOI devices as silicon thickness decreases is different than in unstrained devices.

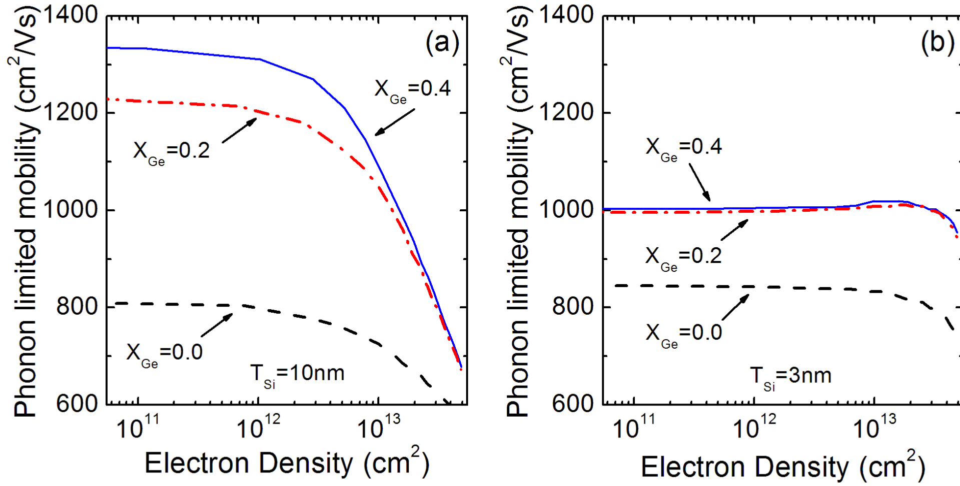


Figure 8.24: Phonon limited mobility in a strained-Si DGSOI MOSFET for two values of the silicon thickness ((a) T_w =10nm, and (b) T$_w$ =*3nm*) and different strain grade magnitudes (Ge concentration).

8.4 Magnetoresistance simulation and results

The performance of semiconductor devices strongly depends on the carrier mobility. The magnetoresistance technique is an unique extraction method, because the mobility is obtained in a *pure way* without assumption of the geometry of the device (Section 7.2.3. Eq. 7.8).

In this section this methodology is applied in a Monte Carlo simulator to compare the mobility at the *front* and *back* channels in advanced SOI MOSFETs. The subscript 1 represents the front gate and subscript 2 the back gate.

The conceptual setup is presented in Figure 8.25 where a DG SOI MOSFET is considered. The front interface is deliberately degraded to reproduce the typical roughness of the Si-high-k gate stack ($\Delta_1 = 0.25nm$ rms, $L_{sr1} = L_{sr2} = 1.3nm$). By comparison, the back Si-SiO$_2$ interface features conservative values ($\Delta_2 = 0.1nm$). Only phonon scattering and interface roughness scattering were considered in the Monte Carlo simulations.

To compute μ_{MR} we have to take into account he effect of a magnetic field

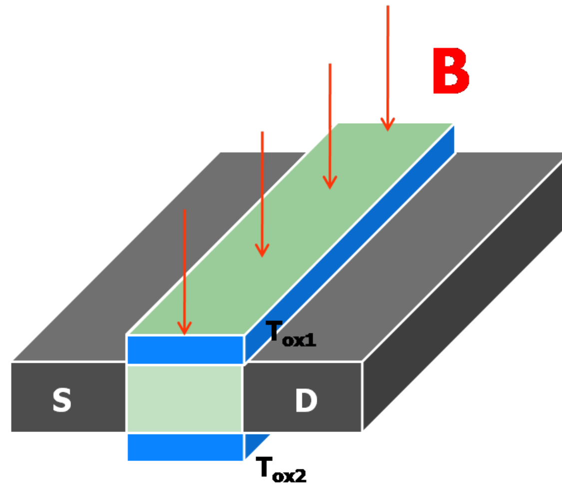


Figure 8.25: Schematic representation of the device considered for Monte Carlo simulations. Magnetic field is applied perpendicular to the gates when magnetoresistance measurements are required.

in the simulation. The inclusion of a magnetic field parallel to the confinement direction does not alter the results of the Schrödinger and Poisson solution because the equations are unchanged in that direction. Therefore the sub-band energies, the envelope functions, and, consequently, the scattering rates and the inversion charge are not affected. On the contrary, the effect of the magnetic field has to be taken into account in the transport simulation [DGC07] (the flights dynamics between the scattering events).

The motion of an electron in the inversion layer of a SOI device in the presence of both electric and magnetic fields can be simulated using a Monte Carlo simulator [GF01]. This allows us to extract the magnetoresistance mobility and, at the same time, compute the effective mobility in the same conditions. Under the effect of a magnetic field, the direction of current does not coincide with the applied field. Therefore we can interpret this electric field as the superposition of the drift field E_x parallel to the current, and the Hall field E_y perpendicular to it.

Typical curves are shown in Figure 8.26 where the quotient $(R_B - R_0)/R_0$ is plotted versus the square of the magnetic field; R_B and R_0 denote the magnetic field-dependent resistivity and the resistance in zero magnetic field respectively. These

curves confirm the quasi-linear variation of the magnetoresistance with B^2 from which μ_{MR} is calculated. The slope decrease with the gate voltage reflects the mobility dependence on the effective field, as described by the universal mobility law [TIT94]. Note that a magnetic field higher than 5T is suitable to reach significant values of magnetoresistance (>10%).

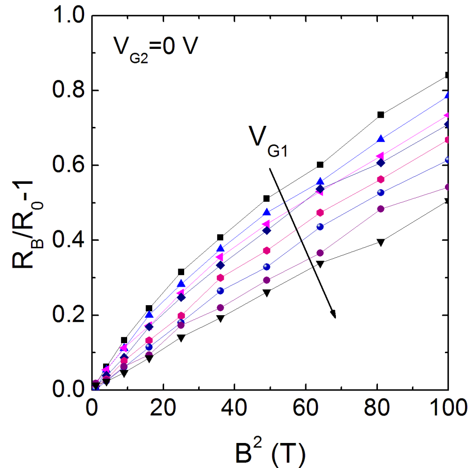


Figure 8.26: Normalized magnetoresistance $R_B/R_0 - 1$ versus the square of the magnetic field for different front-channel bias V_{G1}. Transistor parameters: t_{Si}=*20nm*, Δ_1=*0.25nm.* V_{G1} starts from -0.2V with step 0.2V.

The MR mobility is compared to the effective mobility, also available from the simulations. Figure 8.27 shows that μ_{MR} is higher than μ_{eff}, the ratio depending on the scattering mechanisms and the operation temperature [DGCC07]. The front channel mobility (Figure 8.27a) is lower than the back channel mobility (Figure 8.27b). It is also worth noting that the field-effect (*i.e.* mobility reduction versus gate voltage) is more pronounced at the high-k front interface due to the enhanced roughness scattering and larger field. This result explains recent experimental observations about the systematically larger mobility in the back channel extracted in usual SOI-MOSFETs operated in double-gate mode [OCCP04].

The difference in the front and back channel mobilities leads to characterization problems from $I_D\,(V_G)$ curves as was discussed in Section 7.4.1. By contrast, the

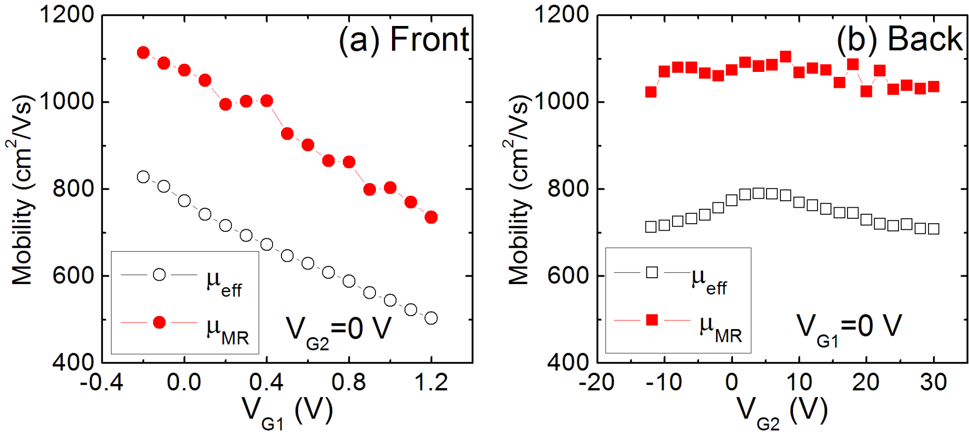


Figure 8.27: Front (a) and back (b) channel effective mobility and magnetoresistance mobility for a SOI MOSFET with $t_{\mathrm{Si}} = 20nm$, $\Delta_1 = 0.25nm$, $\Delta_2 = 0.1nm$.

magnetoresistance technique yields a realistic mobility value.

8.4.0.1 Double-gate operation

The MC results are presented in Figure 8.28. Note that the gate bias influence is reduced as a consequence of the effective field suppression in the middle of the DG MOSFET. The curves are less linear with B^2 than in Figure 8.26 because the MR effect is different at the front and back interfaces.

Monte Carlo simulations enable the separated extraction of the mobility in each channel (Figure 8.28b). As expected (Eq. 7.30) in DG mode, the total mobility is the average of the front and back channel values, confirming the model presented in Section 7.5.1 (Eq. 7.30).

8.5 Conclusions

We simulated the behavior of electron mobility and the effect of volume inversion in bulk MOSFETs and DG-MOSFETs with different surface (hkl) orientations and channel $< hkl >$ directions. In the case of the (110) surface, a strong anisotropy of electron mobility with channel direction is shown: when the channel is in the

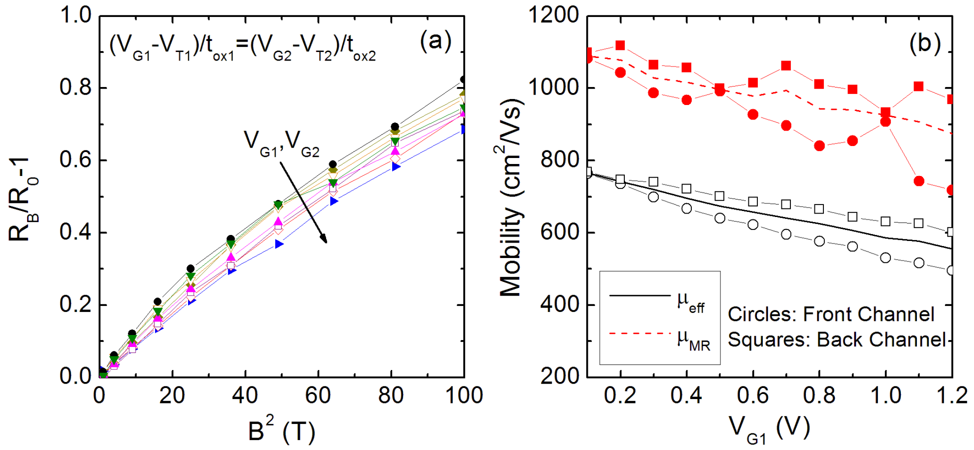


Figure 8.28: **(a)** Normalized MR $R_B/R_0 - 1$ versus the square of the magnetic field for different values of V_{G1} and V_{G2} in DG mode. V_{G1} starts from -0.2V with step 0.2V. **(b)** Front-channel, back-channel and total DG effective mobility (line) and magnetoresistance mobility (dashed line) for a DG MOSFET with $t_{\text{Si}} = 20nm$, $\Delta_1 = 0.25nm$, $\Delta_2 = 0.1nm$.

$(110)/ < 001 >$ direction, electron mobility is 50% higher than in $(110)/ < 1\bar{1}0 >$ and similar to the mobility for a $(100)/ < 001 >$ direction. This anisotropic behavior with channel direction is not observed in $(100)-$ or $(111)-$ surface orientations. The study with silicon thickness also reveals that, as a consequence of the volume inversion effect, a DG MOSFET film thickness range exists where electron mobility is higher than in bulk inversion layers.

Results for DGSOI devices show that the strain of the silicon layer leads to a larger population of the non-primed subbands, thus decreasing the average conduction effective mass and reducing the intervalley scattering rate. However, strain also contributes to a larger confinement of the charge close to the two Si/SiO_2 interfaces, thus weakening volume inversion effect.

For a given thickness of the silicon layer, it is shown that phonon limited mobility of electrons increases as the strain increases but with a saturation effect which is reached at lower values of strain as the silicon thickness decreases.

It has been also reported that the phonon limited mobility increases as silicon

thickness decreases in unstrained devices due to volume inversion effect, while it decreases as silicon thickness decreases in strained devices.

Finally, the transport in SOI MOSFETs was simulated by the Monte Carlo technique in the presence of the magnetic field. The magnetoresistance mobility has been calculated in SOI devices and compared with the effective drift mobility showing the usefulness of this technique.

Conclusions

In the following pages, the main achievements and conclusions obtained during the preparation of this Ph.D. work are summarized. Future work and possible improvements based on our results are also commented.

Main achievements

1. The inclusion of any crystallographic orientation has been implemented in a 1D Poisson-Schrödinger solver based on the coordinate decomposition proposed in [RLG05]. Charge and capacitance results are reported for the most commonly used wafer orientations, i.e., (100), (110), (111).

2. The polysilicon depletion effect and its influence on the charge and the low-frequency gate-to-channel capacitance in $\sim 1nm$ oxide thickness MOSFETs has been revealed.

3. Semi-empirical models were proposed to account for the inversion charge centroid in alternative crystallographic orientations and the polysilicon depletion effect in ultrathin gate-oxide MOSFETs. The models have been tested to reproduce the simulations results.

4. The carrier quantization was accounted for ultrahigh doped polysilicon silicided gates to study the importance of the carrier accumulation. The differences with the ideal metal behavior have been outlined and the role of the hole accumulation has been reported. As an important consequence, it has been shown that metal silicided gates are not exempt from poly-depletion/accumulation effects.

5. The impact of remote Coulomb scattering and remote roughness scattering mechanisms on the electron mobility in ultrathin oxide MOSFETs has been analyzed. A new model which takes into account the contribution of these remote mechanisms was developed and compared to the existing ones and used to reproduce Monte Carlo and experimental results.

6. The outstanding threshold voltage shift observed in thin films with the in-situ pseudo-MOSFET characterization technique has been explained as a consequence of the density of interface traps in non-passivated wafers. The analytical modeling limitations have been discussed and an empirical model, which accurately reproduces the experimental and simulation results, has been proposed.

7. The applicability of the Y-function in SOI devices has been extensively described. Simulations showed that an accurate mobility value is obtained only if the opposite interface is accumulated or depleted, not inverted. The method has been extended to the case of two separated channels with appropriate biasing conditions.

8. Systematic mobility measurements in thick and ultra-thin SOI transistors were presented for PD and ultrathin FD technologies. The two-channels model fails in ultrathin transistors, where the two channels become strongly coupled. For the first time the beneficial effect of volume inversion was reported from usual $I_D(V_G)$ characteristics.

9. The behavior of electron mobility has been reproduced with the Monte Carlo method in bulk and DG-SOI MOSFETs with different surface orientations and channel directions. In the case of the (110) surface, a strong anisotropy of electron mobility was observed: when the channel is in the (100)/<001> direction, electron mobility is up to 50% higher than in (100)/<$1\bar{1}0$>. The anisotropic behavior was not observed in (100)- or (111)- surface orientations. Simulations have shown that there is a DG-MOSFET thickness range where electron mobility is higher than in bulk inversion layers.

10. Monte Carlo results for DGSOI devices showed that the strain of the silicon

layer leads to a larger population of the non-primed subbands, thus decreasing the average conduction effective mass.

11. Strain also contributes to a larger confinement of the charge close to the two Si/SiO_2 interfaces, thus weakening volume inversion effect. It has been reported that the phonon limited mobility increases as silicon thickness decreases in unstrained devices due to volume inversion effect, while it decreases as silicon thickness decreases in strained devices.

12. The genuine geometric magnetoresistance has been reproduced by Monte Carlo simulations confirming the reliability of this technique by comparison with the common extraction of the effective mobility.

Future research topics

Based on this work, there are still open questions and improvements to the models that can be developed in future research projects.

1. Combination of the strain silicon Monte Carlo simulations with alternative crystallographic orientations.

2. Extend the results to alternative materials: germanium, etc, and structures: Trigate, GAAs, etc.

3. Extend the pseudo-MOSFET Poisson simulator to include the contribution of the substrate underneath the BOX. Study the impact of the bulk depletion and the buried charges at the bulk-Si/SiO_2 interface on the pseudo-MOSFET properties. Development of three interface model.

4. Inclusion of the Schrödinger equation in the pseudo-MOSFET Poisson solver to account for the quantum effects in ultrathin silicon films below 10nm.

Part III

APPENDIX

Appendix A

Short summaries

A.1 English

In this work, the impact and challenges of the decananometric miniaturization of today shrinking CMOS devices, fabricated on SOI and bulk Si, are studied.

The inclusion of quantum effects to accurately describe the behavior of the MOS transistors with single or multiple gates is studied. Poisson and Schrödinger equations are self-consistently solved in several cases of interest showing the consequences of the physical mechanisms when the decananometric limit is achieved. Among others, carrier quantization, charge centroids, darks spaces, polysilicon depletion, remote scattering mechanisms effects... are reported and modeled.

The electrical characterization techniques both at the wafer level and device level are revisited and studied in the framework of today 45nm technological node. Some recent results obtained using the as-fabricated wafer pseudo-MOSFET characterization technique are explained by means of numerical simulations. The reliable Y-function is extended for double channel devices and used to reveal the beneficial effect of volume inversion effect, for the first time, from usual static characteristics.

For many years, the mobility has been a hot issue surrounded by a lot of research effort. This struggle has continued until nowadays when the technology is approaching the end of the Roadmap. In this work, two conventional technology-compatible techniques are exploited as mobility boosters through Monte Carlo simulation: alternative crystallographic orientations for the device architecture and the use of

strained silicon as channel material.

This synopsis of the Ph.D. dissertation is not a closed work, since it rather establishes some of the guidelines and problems to deal with in a short term future.

A.2 Français

Dans ce travail, les incidences et les enjeux de la miniaturisation décananométrique des composants CMOS avancés, fabriqués sur SOI ou Si massif, sont étudiés.

L'inclusion des effets quantiques nécessaires pour décrire avec précision le comportement des transistors MOS avec grille unique ou grilles multiples est traitée. Les équations de Poisson et de Schrödinger sont résolues de manière self-consistante, dans plusieurs cas d'intérêt, démontrant les conséquences de la physique sous-jacente lorsque la limite décananométrique est atteinte. Parmi d'autres, la quantification des porteurs, les centroïdes de la charge, les zones d'exclusion, la déplétion du silicium polycristallin, les mécanismes de collision, etc... sont analysés et modélisés.

Les techniques de caractérisation électrique, à la fois au niveau des plaquettes en SOI et Si et au niveau du composant MOS, sont réexaminées et étudiées dans le contexte présent du noeud technologique 45nm. Certains résultats récents obtenus avec la méthode pseudos-MOSFET sur les plaquettes SOI sont expliqués au moyen de simulations numériques. La méthode basée sur la fonction Y est étendue pour le cas des doubles canaux. Nos résultats expérimentaux font apparaître, pour la première fois, l'effet bénéfique de l'inversion volumique à partir des caractéristiques statiques habituelles.

Depuis de nombreuses années, la mobilité a été un sujet brûlant entouré de beaucoup d'efforts de recherche. Cet intérêt s'est poursuivi jusqu'à aujourd'hui quand la technologie approche la fin de la feuille de route de la microélectronique VLSI. Dans ce travail, deux technologies prometteuses pour l'accroissement de la mobilité sont envisagées grâce à la simulation de Monte Carlo: des orientations cristallographiques alternatives pour l'architecture du dispositif et l'emploi du silicium contraint comme matériau du canal de conduction.

Ce document de thèse ne représente pas une synthèse ou une conclusion fermée, car les recherches se poursuivent. Il fournit des résultats importants, établit des lignes directrices et évoque certains problèmes supplémentaires à résoudre dans

l'avenir proche.

A.3 Español

En este trabajo se ha estudiado el impacto y las oportunidades abiertas por la miniaturización decananométrica de los dispositivos CMOS actuales.

Se ha abordado la inclusión de efectos cuánticos para describir de forma precisa el comportamiento de dispositivos MOSFET de una y múltiples puertas. En distintos casos de interés, se han resuelto de forma autocosistente las ecuaciones de Schrödinger y Poisson mostrando las consecuencias de los mecanismos físicos involucrados en los dispositivos cuando se alcanzan los límites decananométricos. Entre otros, se han estudiado y modelado: cuantización de portadores, centroides de carga, "espacios oscuros", deplexión de polisilicio, efectos de scattering remoto...

Las técnicas de caracterización eléctrica para SOI se han sometido a análisis y examen tanto a nivel de oblea como de dispositivo en el contexto del actual nodo tecnológico de 45nm. Algunos resultados recientes obtenidos mediante el procedimiento pseudo-MOSFET para caracterización para obleas se han explicado mediante simulaciones numéricas. El método basado en la función Y se ha extendido para dispositivos de dos canales; mostrando por primera vez el efecto beneficioso de la inversión en volumen a través de características estáticas habituales.

Durante muchos años, la movilidad de los portadores ha sido una materia candente, rodeada de un gran esfuerzo investigador. Esta lucha por mejorar ha continuado hasta hoy en día, cuando la tecnología está alcanzando el final de la "hoja de ruta". En este trabajo se han analizado, gracias a la simulación Monte Carlo, dos de las tecnologías promesa para el incremento de la movilidad compatibles con la tecnología actual: orientaciones cristalográficas alternativas en la arquitectura de los dispositivos y el uso de silicio tenso como material para el canal.

Este documento no representa un compendio cerrado; tras los significativos resultados obtenidos mas bien establece algunas de las líneas directrices y evoca ciertos problemas que deberán tratarse en el futuro próximo.

Appendix B

Résumé de la Thèse

La performance des circuits intégrés et des applications de la microélectronique s'est améliorée exponentiellement grâce à la réduction de la taille des transistors MOS.

La miniaturisation des dispositifs entraîne cependant une série de problèmes dont la solution est complexe. Aujourd'hui, les dimensions des transistors sont de l'ordre de quelques couches atomiques. La nature discrète de la matière et les limitations quantiques induisent des effets importants qui étaient encore ignorés, il y a quelques années, dans la conception et la modélisation.

Cette étude analyse l'impact, les chances et les défis de la miniaturisation décananométrique sur les performances des prochaines générations de transistors (nœud 45 nm et les suivants). Les deux axes principaux de recherche que nous avons abordés dans cette thèse sont les suivants:

1. La caractérisation, modélisation et simulation de certains des effets quantiques révélés lorsque les dimensions des dispositifs approchent la limite physique.

2. L'introduction de la technologie SOI comme l'un des meilleurs candidats pour l'avenir des technologies CMOS, prolongeant de cette façon la durée de vie du monde électronique basé sur les transistors MOSFET.

Nos principales réalisations sont résumées dans les pages suivantes.

B.1 Simulation quantique du MOSFET avec orientations cristallographiques alternatives et grilles de siliciurées (chapitres 1, 2 et 3)

La résolution auto-cohérente des équations de Poisson/Schrödinger est étendue au cas de différentes orientations cristallographiques. Nous proposons une amélioration aux modèles classiques du centroïde de charge et de la capacité grille-canal lorsque différentes orientations cristallographiques sont utilisées. L'effet de la déplétion du polysilicium, qui devient un problème sérieux lorsque l'épaisseur du SiO_2 du MOSFET diminue jusqu'aux dimensions nanométriques, est pris en compte dans la modélisation.

Comme solution aux problèmes de la déplétion du polysilicium, après plus de 40 années de succès avec grilles de poly-Si/SiO_2, l'industrie doit maintenant faire face à la transition vers la grille métal/high-k. La grille en métal siliciuré a été proposée comme une alternative. Cependant, notre travail montre que les effets quantiques sont toujours présents dans les grilles siliciurées et conduisent à des erreurs dans l'extraction de l'épaisseur de l'isolant (Figure B.1).

B.2 Mécanismes de dispersion dans MOSFETs avec oxyde de grille ultramince (chapitre 4)

L'une des conséquences de la réduction de l'épaisseur de l'isolant, lorsque les dispositifs sont miniaturisés, est l'augmentation de l'impact de certains mécanismes de collision sur la mobilité des électrons dans le canal: charges dues à la déplétion du polysilicium et effet de la rugosité à l'interface polysilicium–SiO_2.

La Figure B.2 montre la mobilité des électrons en fonction du champ électrique effectif pour MOSFETs avec différentes épaisseurs d'oxyde. L'importance des mécanismes de collision sur les défauts éloignés du canal dépend de l'épaisseur de l'isolant: les courbes de mobilité sont dégradées lorsque l'épaisseur d'isolant diminue.

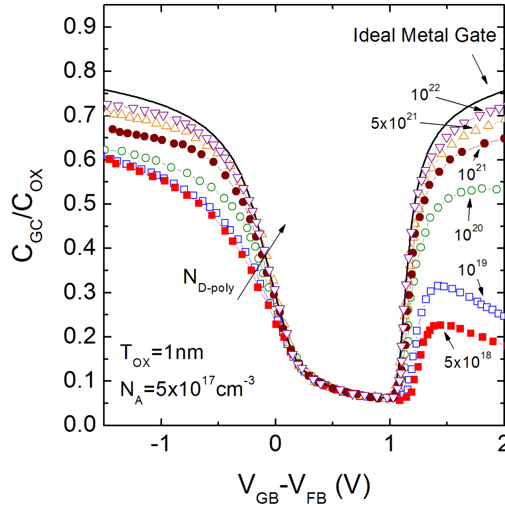


Figure B.1: Capacité grille-canal aux basses fréquences normalisée par la capacité de l'épaisseur physique de l'oxyde pour différentes concentrations d'électrons libres dans la grille. Le comportement idéal du métal n'est jamais atteint.

B.3 Technologie Silicium sur Isolant: caractérisation des wafers (chapitres 5, 6 et 7)

La filière Silicium sur Isolant (SOI) est proposée comme le prolongement naturel de la technologie CMOS basée sur Si massif. Après la présentation des matériaux et des dispositifs SOI, nous nous intéressons à la caractérisation des plaquettes SOI avec la technique Pseudo-MOSFET. Nous présentons les limitations des modèles existants et proposons des corrections utiles pour les couches SOI ultra fines. En particulier, nous expliquons la remarquable augmentation de la tension de seuil observée lorsque l'épaisseur du film de silicium est réduite en-dessous de 50nm. L'originalité de notre modèle vient de la prise en compte de la charge des porteurs minoritaires, plus importante que celle du dopage.

La méthode d'extraction de la mobilité électronique est réexaminée dans le contexte des transistors MOSFET SOI où les deux grilles peuvent être polarisées. Nous

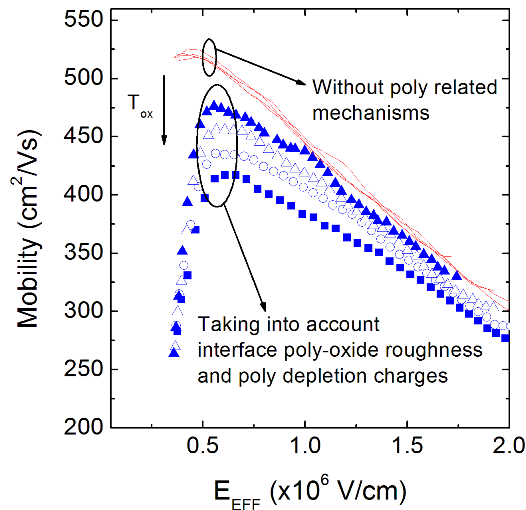


Figure B.2: Nous avons proposé un modèle empirique qui permet de reproduire les corbes de mobilité en fonction du champ vertical, obtenues avec la simulation Monte Carlo et avec des techniques expérimentales. Ce modèle combine les différents mécanismes de collision selon la loi de Mathiessen.

nous concentrons sur la technique de la fonction Y, initialement conçue pour un canal unique, et étendons son applicabilité au cas des transistors double-grille (DG). Des mesures systématiques de la mobilité dans transistors SOI épais et ultraminces sont présentées pour les modes simple-grille (SG) et quasi double-grille (DG).

Dans le mode SG, la mobilité est surestimée dès que le canal opposé est activé. Dans les MOSFETs partiellement déplétés ou relativement épais, les deux canaux sont séparés; pour cette raison, la mobilité totale pour le mode DG est la somme des mobilités des canaux avant et arrière. En revanche, pour les films ultra minces, nos résultats font apparaître une remarquable augmentation de la transconductance (Figure B.3) et de la mobilité apparente en mode Double-Grille. Ce gain de mobilité reflète l'effet bénéfique de l'inversion volumique, qui est ainsi mis en évidence de manière inédite avec la fonction Y.

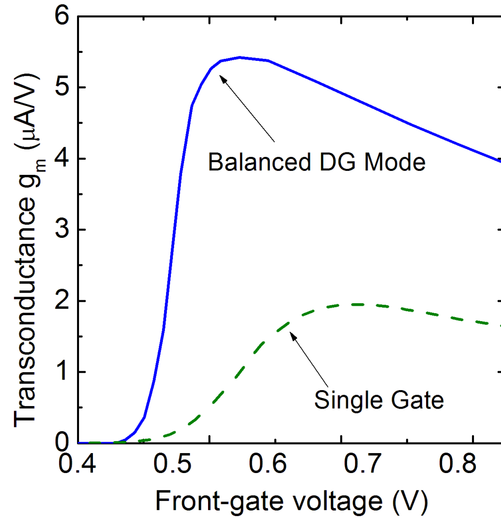


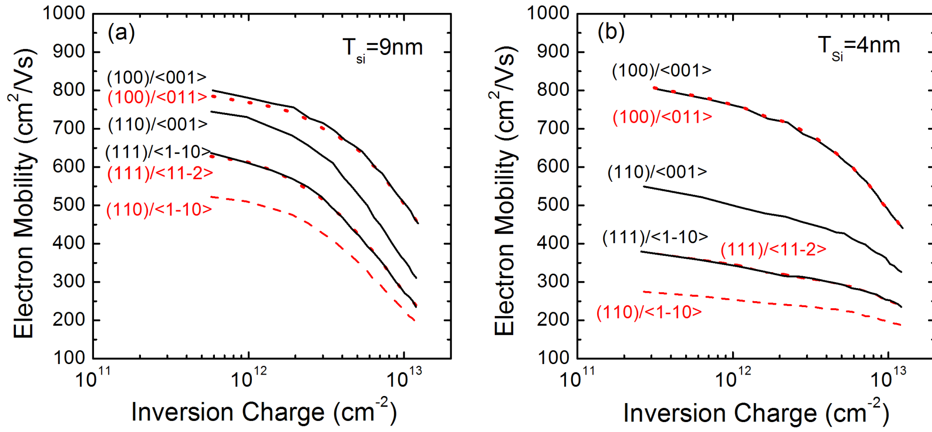
Figure B.3: Transconductance mesurée pour modes simple-grille (SG) et double-grille (DG) dans un transistor SOI MOSFET ultramince. Une augmentation de 290% est observée en mode DG, qui est induite par l'inversion de volume et ne peut pas être expliquée par un modèle classique de superposition des canaux.

B.4 Simulations de mobilité avec la technique Monte Carlo (chapitre 8)

Le transport d'électrons est étudié avec la méthode de Monte-Carlo. Nous commençons par examiner le comportement de la mobilité des électrons en MOSFETs bulk et SOI avec différentes orientations de canaux et de surfaces.

Dans le cas de la surface (110), une forte anisotropie avec la direction du canal est observée. Lorsque le canal est orienté dans la direction (110) / <100>, la mobilité des électrons est 50% supérieure à celle correspondant à l'orientation (110) / <1$\bar{1}$0> (Figure B.4). L'étude de l'épaisseur de silicium révèle également d'intéressantes conséquences de l'effet d'inversion volumique.

Nos résultats Monte Carlo pour les dispositifs DG-SOI montrent que la contrainte des couches de silicium conduit à une modification des populations dans les sous-bandes, ce qui entraîne un abaissement de la masse effective et donc une



amélioration de la mobilité. La contrainte contribue également à un plus grand confinement de la charge près des deux interfaces Si/SiO2, ce qui affaiblit légèrement l'effet de l'inversion de volume. Nous montrons que la mobilité électronique liée aux collisions avec les phonons augmente lorsque l'épaisseur de silicium est réduite, pour les transistors non-contraints, en raison des effets de l'inversion de volume. L'effet opposé est mis en évidence pour les dispositifs contraints.

Appendix C

List of publications

C.1 Referenced papers

N. Rodriguez, F. Gámiz, R. Clerk, G. Ghibaudo, S. Cristoloveanu, "Quantization impact of accumulated carriers in Silicide-gated MOSFETs", Submitted.

F. Gámiz, A. Godoy, C. Sampedro, N. Rodriguez, F.G. Ruiz, "Monte Carlo simulation of low-field mobility in strained Double Gate SOI transistors", *Journal of Computational Electronics*. To be published.

N. Rodriguez, S. Cristoloveanu, F. Gámiz, "Evidence for mobility enhancement in double-gate silicon-on-insulator metal-oxide-semiconductor field-effect transistors", *Journal of Applied Physics* 102, 1 2007.

N. Rodriguez, F. Gámiz, J. B. Roldán. "Modeling of inversion layer centroid and polysilicon depletion effects on ultrathin-gate-oxide MOSFET behavior. The influence of crystallographic orientation", *IEEE Transactions on Electron Devices*, Vol. 54, No. 4, Apr. 2007.

N. Rodriguez, J. B. Roldán, F. Gámiz, "An electron mobility model for ultra-thin gate-oxide MOSFETs including the contribution of remote scattering mechanisms", *Semiconductor Science and Technology*, vol. 22, 348-353. 2007.

L. Donetti, F. Gámiz, N. Rodriguez, F. G. Ruiz, "Phonon scattering in Si-based nanodevices" *Solid-State Electronics.* pp. 593-597. 51, 2007.

L. Donetti, F. Gámiz, N. Rodriguez, F. Jiménez, and C. Sampedro, "Influence of acoustic phonon confinement on electron mobility in ultrathin silicon on insulator layers" *Applied Physics Letters* 88, 122108. March 2006.

J.B. Roldán, F. Gámiz, A. Roldán, N. Rodriguez, "Characterization of electron transport at high fields in Silicon-On-Insulator devices. A Monte Carlo Study", *Semiconductor Science and Technology*, 21, No. 1, 81-86. Jan 2006.

C.2 Conference contributions

N. Rodriguez, S. Cristoloveanu, T. Nguyen, F. Gámiz, "Impact of the top surface density of states on the characteristics of ultrathin SOI pseudo-MOSFETs", *In proceedings EuroSOI conference 2008*, Cork, Ireland.

F. Gámiz, A. Godoy, C. Sampedro, N. Rodriguez, F.G. Ruiz, "Monte Carlo simulation of electron mobility in strained Double Gate SOI transistors", *In proceedings International Workshop on Computational Electronics 2007*, Amherst, USA.

N. Rodriguez, L. Donetti, F. Gámiz, S. Cristoloveanu, "Geometric Magnetoresistance and Mobility Behavior in Single-Gate and Double-Gate SOI Devices", *In proceedings SOI conference 2007* p.59, Indian Well, California. **Best Poster Award**.

N. Rodriguez, S. Cristoloveanu, L. Pham Nguyen, F. Gámiz, "Mobility Issues in Double-Gate SOI MOSFETs: Characterization and Analysis", *In proceedings ESSDERC 2007*, p. 271, Munich.

F. Gámiz, L. Donetti, N. Rodriguez, "Anisotropy of Electron Mobility in Arbitrarily Oriented FinFETs", *In proceedings ESSDERC 2007*, p. 378, Munich.

N. Rodriguez, F. Gámiz, J. B. Roldán, "Remote Scattering Mechanisms in Ultrathin Gate-Oxide MOSFETs: An extended mobility model", *In proceedings ULIS*

2007, p. 105, Leuven, Belgium.

L. Donetti, F. Gámiz, F. Jiménez-Molinos, N. Rodriguez, J. Roldán, "Phonon confinement and electron mobility in ultrathin SOI devices", *In proceedings EUROSOI 2006*, p. 63, Grenoble, France.

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