



High accuracy and cost-efficient ethernet-based timing system for the IFMIF-DONES facility

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Javier Díaz, jda@ugr.es, C. Megías, I. Casero, E. Ros, M. Rodriguez

Dep. Computer Engineering, Automation and Robotics, Universidad de Granada

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- 1) Introduction: IFMIF-DONES Overview
- 2) Timing system design alternatives
- 3) Experimental validation
- 4) IFMIF-DONES timing network new design
- 5) Conclusions and future work



Remote handling area



LIPAc-DONES area



Lab goal: research about key control technologies for the design and construction of the IFMIF-DONES facility.

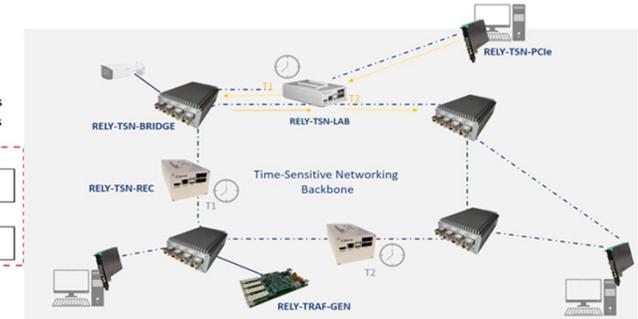
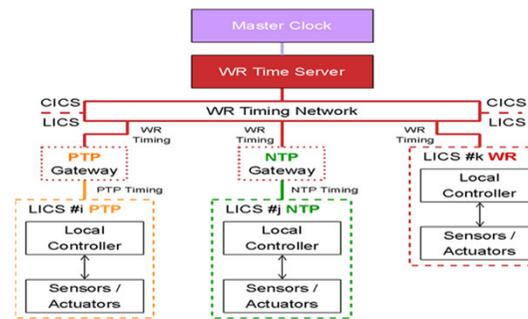
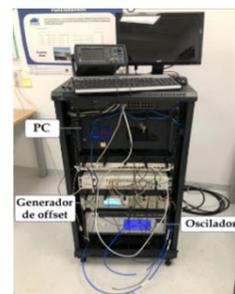
Main topics: control system requirements and use cases, remote handling robotics and automation, timing and communication, CICS & LICS control architectures, Digital Twin (virtual infrastructure)

Timing and Communication architecture exploration and setups

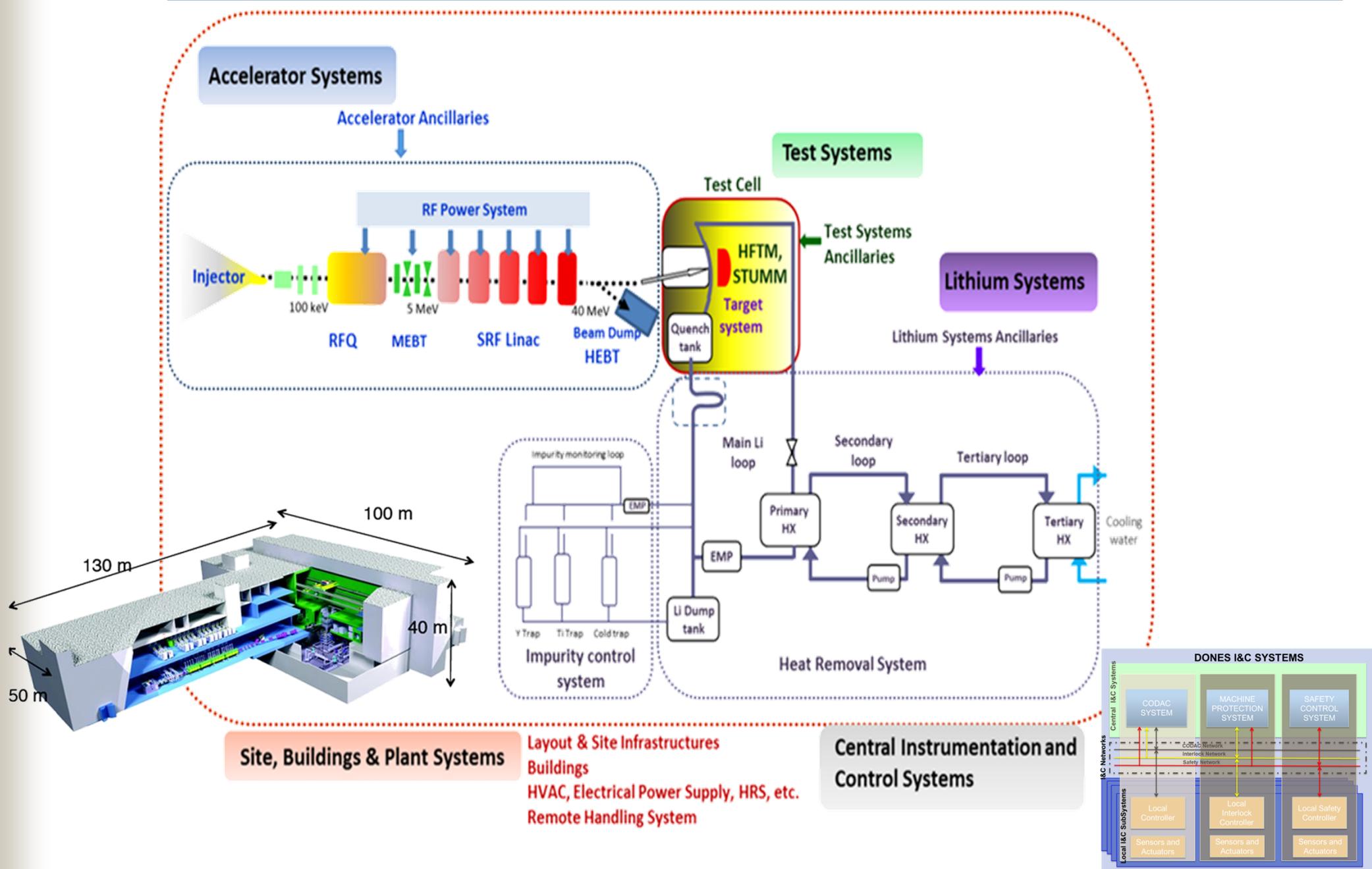


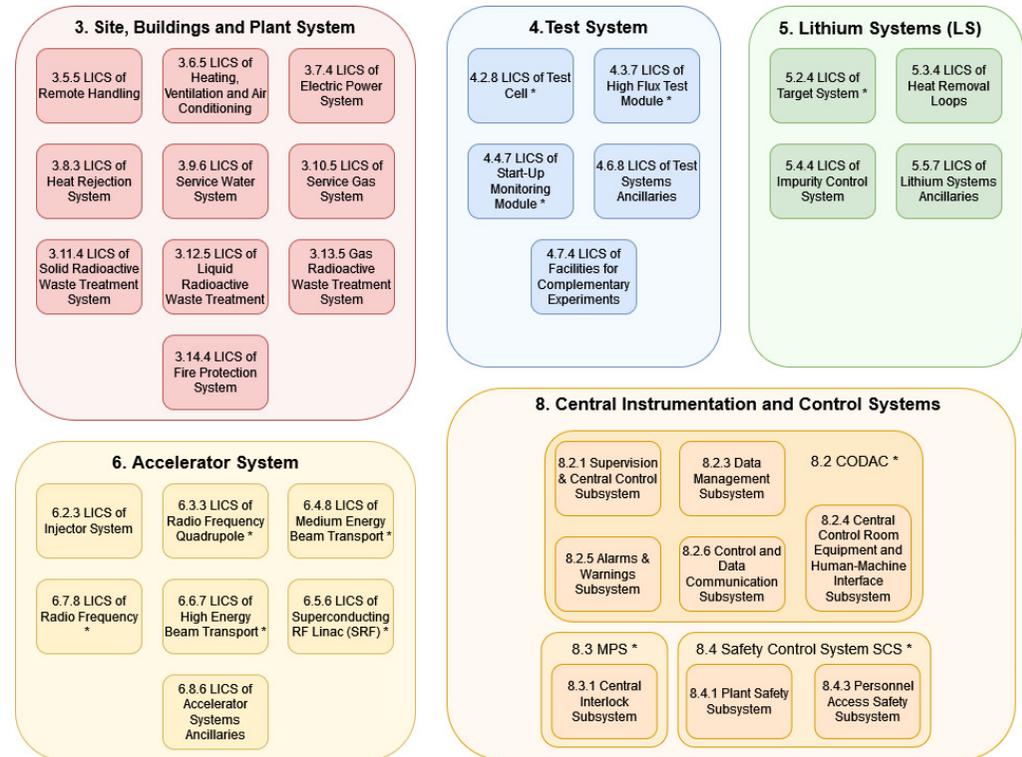
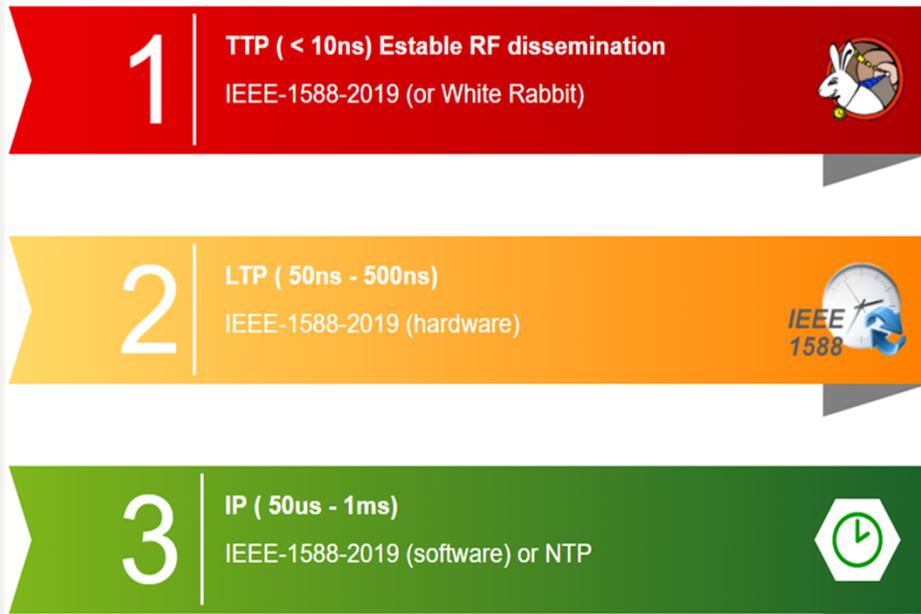
Videowall – Mirror Room

Lab's team



IFMIF-DONES at a glance



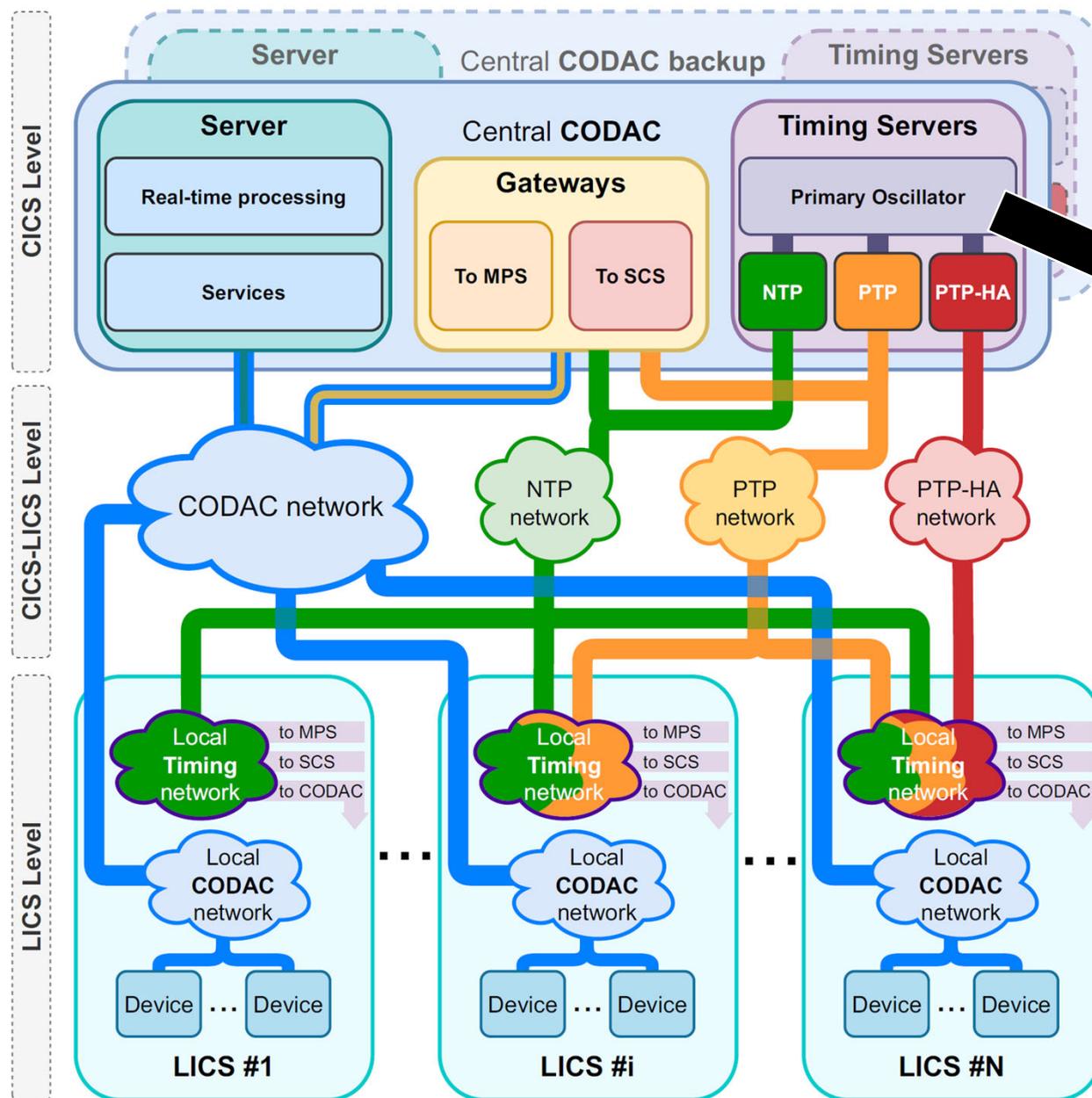


Timing requirements

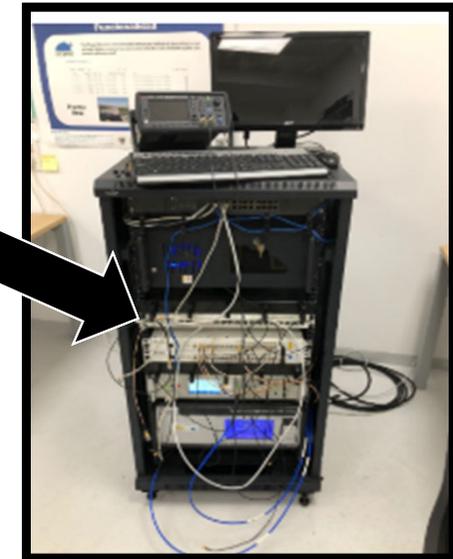
- Performance: time transfer (1ms, 1 us) and RF dissemination (<1ps phase noise)
- Resilience (redundant topologies)
- Deterministic performance (minimal PDV)
- Interoperability (Ethernet), no calibration, monitoring,

...

Sol. Independent networks

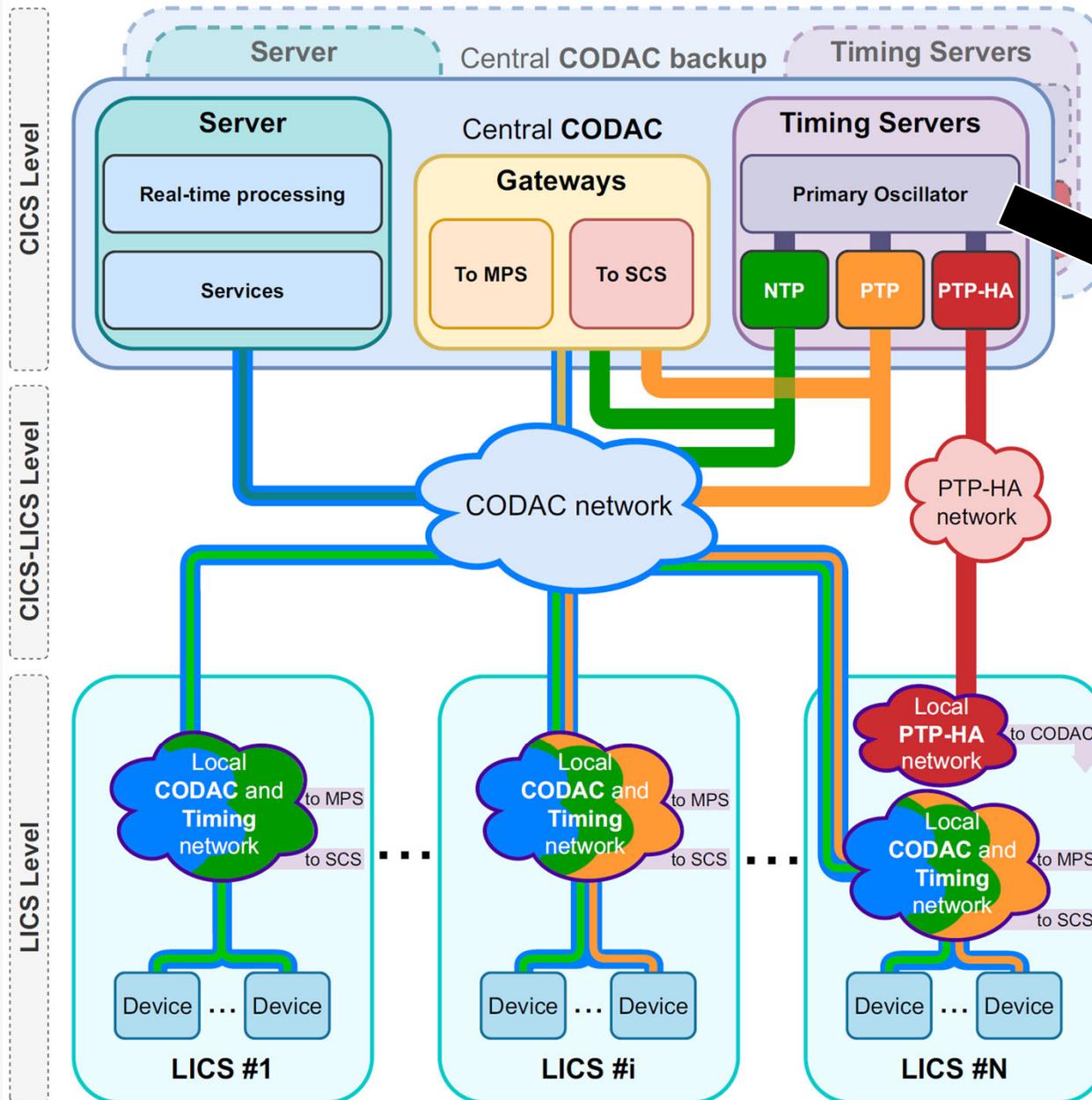


- **Master clock**

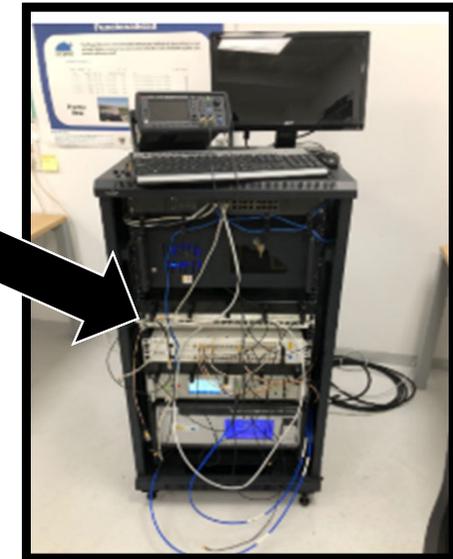


- One dedicated network per time protocol.
- No shared medium with data network
- Expensive but easy

Sol. Data & timing networks



- **Master clock**

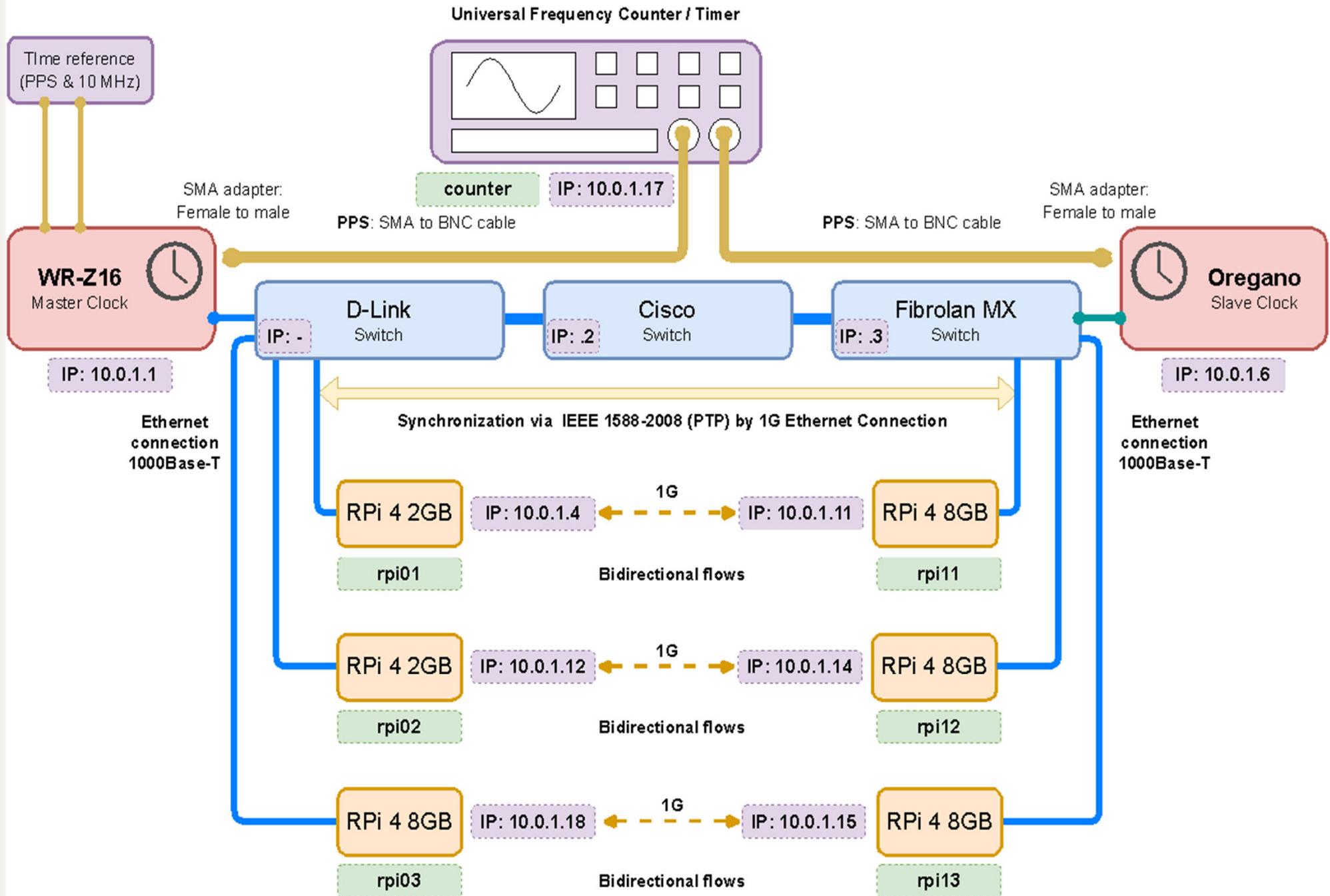


- One dedicated network for HA (WR)
- Shared medium with CODAC & Timing
- Cost effective

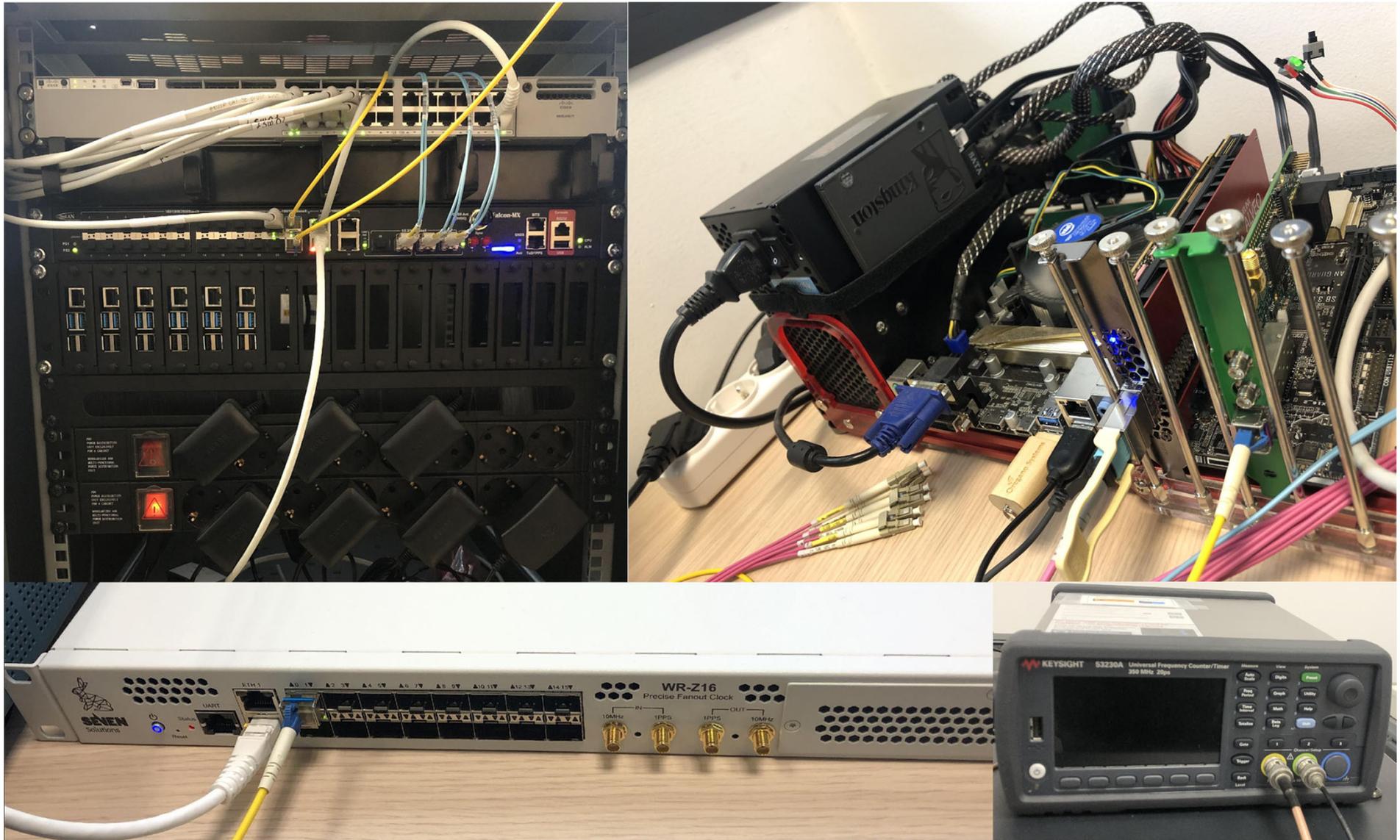
Experimental validation

- **Goals:** evaluate previous solution under realistic operating conditions (CODAC data traffic, hops, ...).
- **Experimental considerations:**
 - **Physical time error measurement** → **PPS** (Pulse Per Second). Counters instead of software measures.
 - IEEE-1588v2 based on default protocol
 - **Utilization of time-unaware and time-aware switches** to evaluate synchronization quality over the data (CODAC) network.
- **Technologies and equipment**
 - **Chrony** implementation for NTP
 - **PTPd/Oregano stack** implementation for IEEE-1588v2.
 - **Fibrolan** as time-aware switches (IEEE-1588v2)
 - White Rabbit open hardware and Safran proprietary devices
 - **Tools:** Wireshark, packeth, iperf3, etc,

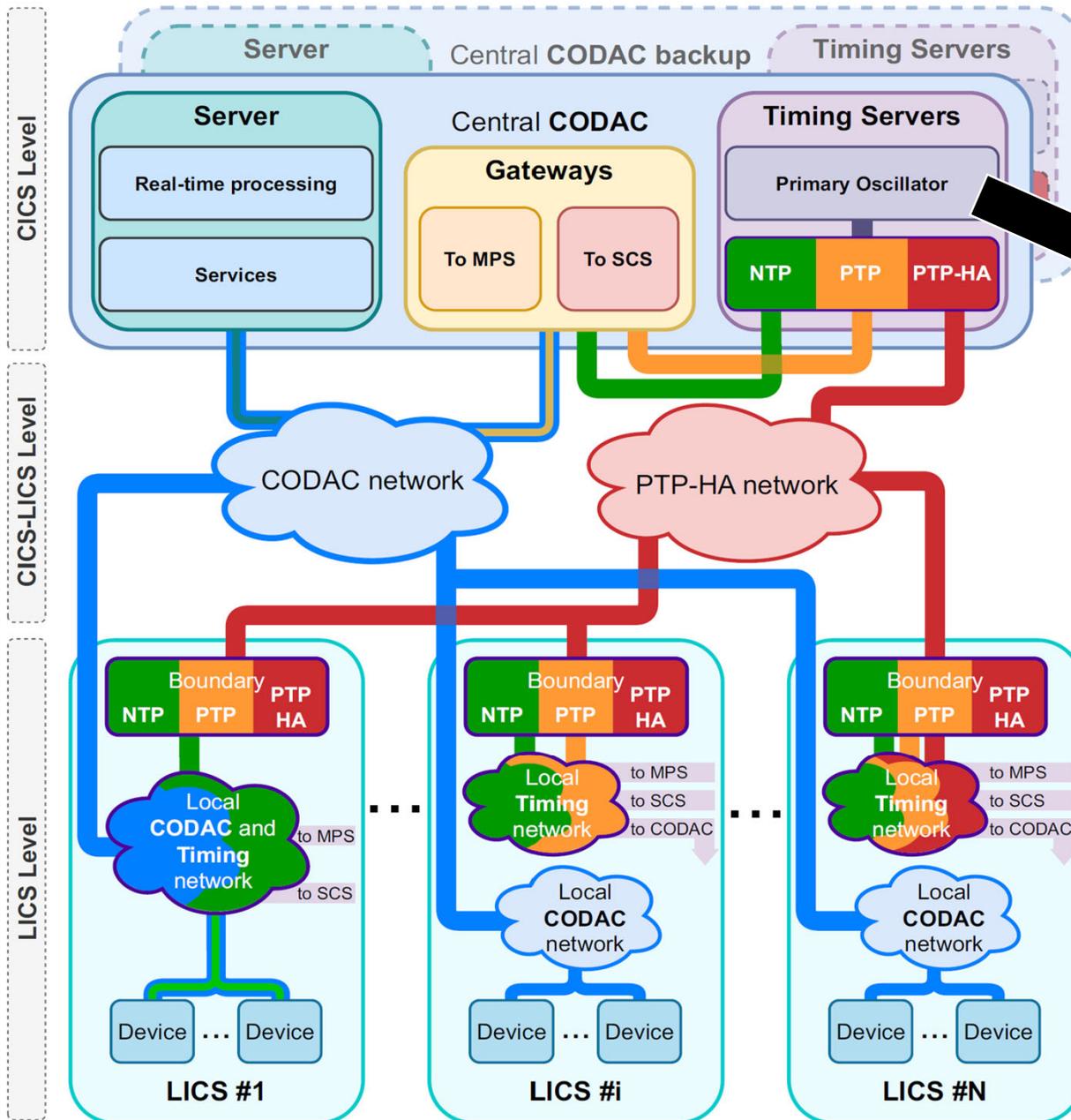
Setup configuration



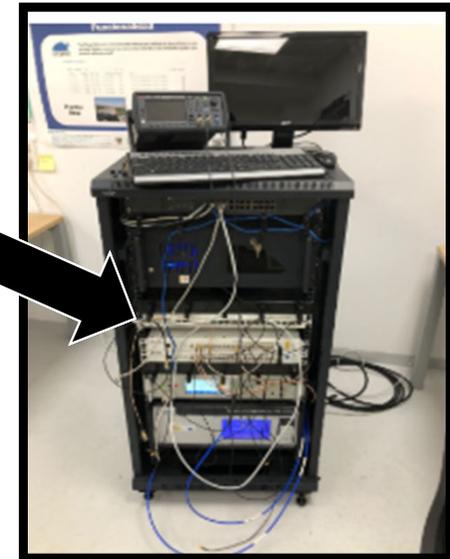
Experimental devices



Sol. HA timing networks



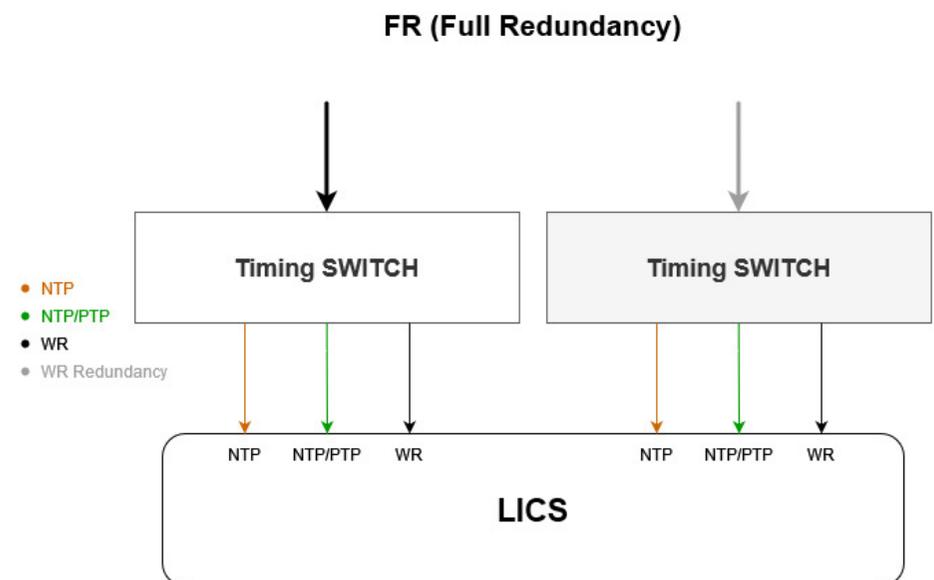
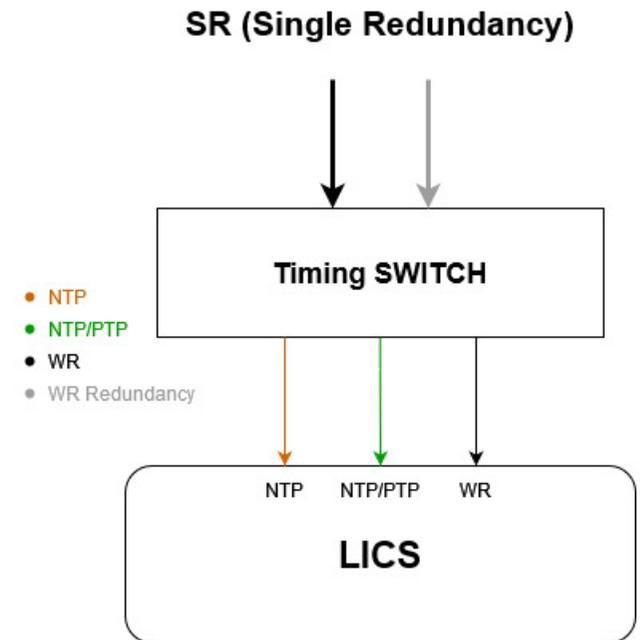
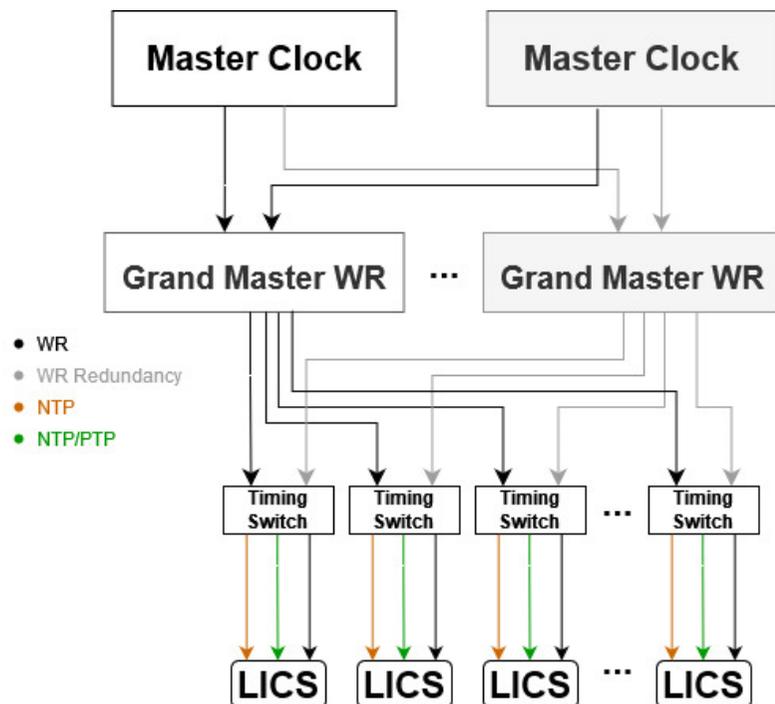
- **Master clock**



- Dedicated network per HA (WR).
- No shared medium with data network
- Three time protocols only used at LICS

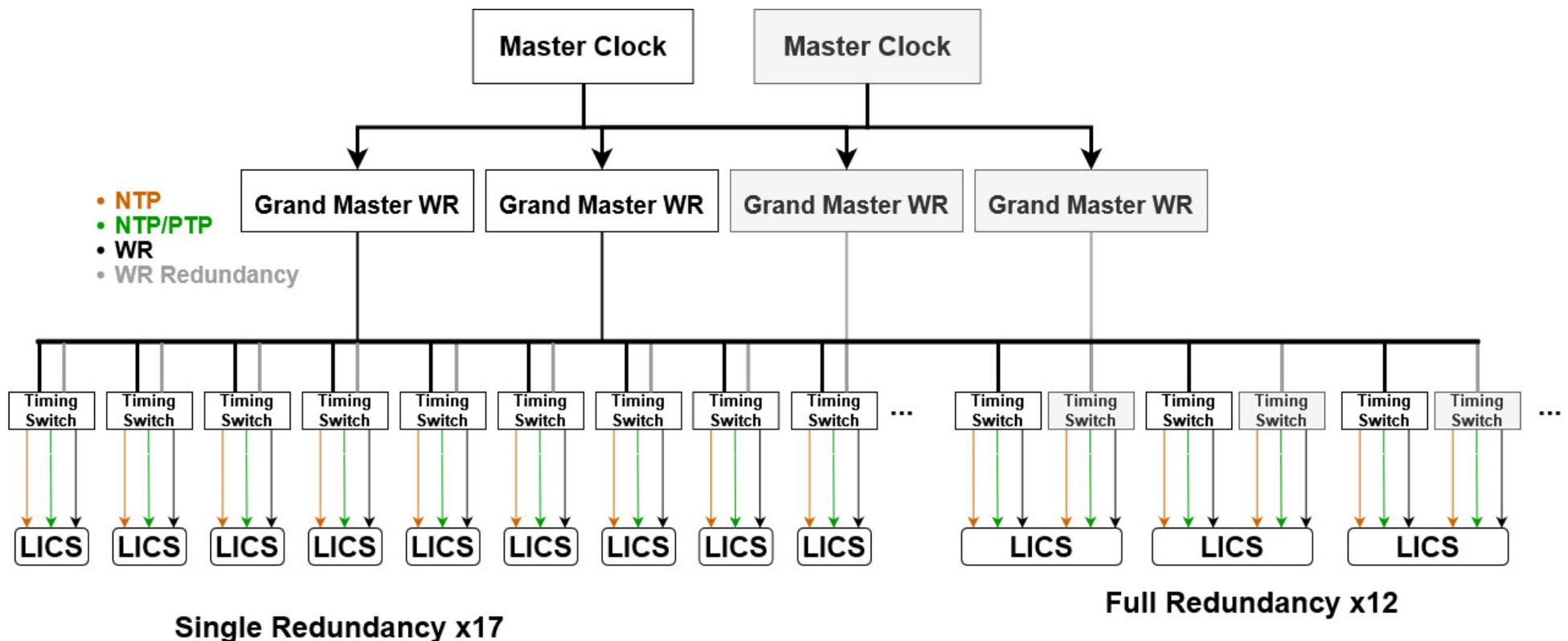
Timing network redundancy

- Redundancy with PRP-like protocol at the Timing CISC.
- Each timing device should receive two timing signals, each from a different grand master
- LICS can implement single or full redundancy depending on their dependability requirements



Final timing network

- 17 LICS with single redundancy and 12 with full redundancy.
- 41 switches and 58 WR ports. Therefore, with only 4 grand masters, PRP can be done. Note that GM mode can be implemented with the timing switches (same device).



Conclusions

- A solution based on standard Ethernet protocols has been proposed for IFMIF-DONES. Easy to design and deploy, allow data and timing propagation on the same networks
-  A shared medium imposes significant constraints on the CODAC network operations.
 - Experiments show that traffic above than 20% impact on the timing (unless careful timing design is used but flexibility requirement is not achieved)
-  A solution based on **redundant network using HA/WR timing protocol** has been proposed for CISC. It offers minimal impact on cost without performance penalties.
- **Future work** will focus on the timestamping & trigger devices to be used on the edge network devices

Thanks for your attention

jda@ugr.es



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