

TITLE: Comprehensive analysis and exploratory design of graphene-based subharmonic mixers operating at the gigahertz band.

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ABSTRACT: Ambipolar conductance in graphene field-effect transistors (GFETs), and in particular their quasi-quadratic I-V transfer characteristic, makes these devices excellent candidates for exploiting subharmonic mixing at high frequencies. Several realizations have already demonstrated the ability of GFETs to compete with, or even improve, state-of-the-art mixers based on traditional technologies. Nonetheless, a systematic analysis of the influence on performance of both circuit design and technological aspects has not been conducted yet. In this work, we present a comprehensive assessment of the conversion losses by means of applying radio-frequency circuit design techniques in terms of filtering and matching, along with the impact stemming from physical and geometric variations of a fabricated graphene technology.

Keywords: graphene field-effect transistor, ambipolar electronics, subharmonic mixing, radio-frequency, large-signal S-parameters, impedance matching.

1. Introduction

Research on 2D materials has garnered significant interest over the past two decades, with graphene emerging as the most promising candidate for high-frequency applications [1], primarily due to its exceptional carrier mobility [2, 3]. Some examples of the main advancements can be found among radio-frequency (RF) power detection applications [4, 5], antenna arrays [6], phase shifters [7], frequency multipliers [8-10], low noise amplifiers [11, 12], modulators [13] and even THz absorbers [14, 15]. Furthermore, the ambipolar electrical response of GFETs, i.e. their symmetric V-shaped transfer characteristics (I_{DS} versus V_{GS}) around the point of minimum conductivity, namely, the Dirac voltage (V_{Dirac}), enables the exploration of new functionalities as well as the redesign and simplification of conventional RF circuits [16, 17].

In the particular realm of mixers, the low transconductance of GFETs still hinders the deployment of active architectures with comparable performance to conventional technologies [1], [16]. The scenario is more favorable with subharmonic resistive mixers (taking advantage from the frequency doubling phenomenon enabled by graphene quadratic I_{DS} - V_{GS} response, see Fig. 1), which have demonstrated to be on par with state-of-the-art mixing performance [18-21]. Subharmonic mixers are especially convenient at high frequencies since they relax the frequency requirement of the high-power local oscillator (LO) source [22]. In addition, the larger frequency gap between the RF and the LO signals that generate a given intermediate frequency (IF) signal also eases the filter design for preventing the LO leakage through the gate-drain capacitance to the drain terminal, a concern that becomes more pronounced as the frequency is raised. Furthermore, the utilization of the GFET as the main building block of subharmonic mixers considerably reduces the complexity of the system as it avoids the need of i) two out-of-phase LO signals through a hybrid coupler that doubles the number of transistors [23,

24], or ii) a pair of anti-parallel diodes [25]; simplifying the fabrication process in an eventual integrated circuit (IC) implementation. Not only that, but this GFET mixer topology also features zero DC power consumption as the drain is left unbiased in the resistive mixer configuration. This characteristic paves the way for the ulterior development of ultra-low-power transceivers targeting the deployment of ubiquitous wireless communication systems in the IoT scene.

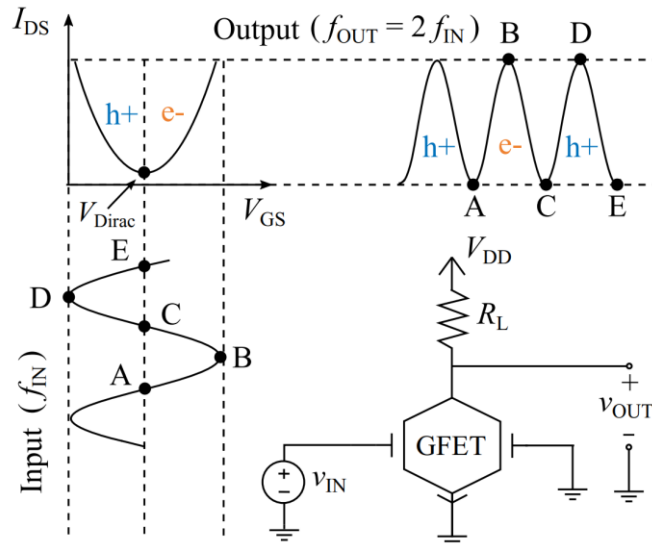


Fig. 1 Working principle of a GFET-based frequency doubler, relying on the intrinsic graphene ambipolar conduction. The same concept is leveraged in subharmonic mixers to generate a higher-frequency component at twice the LO frequency when gate biasing is centered at V_{Dirac}

Motivated by these auspicious features, this work focuses on two well-defined objectives: i) To realize an optimized design of a GFET-based subharmonic resistive mixer, particularly concerning the power ratio of the output IF signal to the input RF signal, namely, conversion losses (CL). With this, our aim is to contribute with a robust and systematic methodology for designing single-GFET mixers that also applies to other mixer architectures, incorporating innovative circuit-level techniques, related to the selective filtering of undesired frequency components and the matching between ports. ii) To analyze the impact of the GFET geometrical and technological parameters on the mixer performance. This analysis is particularly relevant due to the present challenges in achieving uniformity and technological control in GFETs [1], which complicate the development of graphene circuits and consequently impact in the progress of its Technology Readiness Level (TRL).

The study is organized as follows. The computer-aided design (CAD) tool based on fabricated GFET-technology is presented in Section 2. In Section 3, we outline the mixer design using RF techniques such as selective filtering and an approach for simultaneous conjugate matching the nonlinear circuit operating at different fundamental frequencies. Then, by using the proposed design, in Section 4 we undertake different performance predictions spanning critical GFET technological and geometrical parameters to assess its outcome through the analysis of CL. Finally, the main conclusions are drawn in Section 5.

2. Methods

The experimental results of the top-gated GFET technology reported in [19] are considered here as a reference to benchmark the results achieved by simulation, ensuring that the design process is feasible

and could be developed into a manufactured prototype. It consists of an exfoliated graphene flake ($1\text{ }\mu\text{m-long} \times 20\text{ }\mu\text{m-wide}$) with 25-nm Al_2O_3 as gate dielectric.

The main technological and material parameters are collected in Table 1, directly extracted from the fabricated devices reported in [19], where μ stands for the field-independent effective carrier mobility (considered identical for both electrons and holes); V_{g0} is the gate offset voltage comprising the work-function difference between the gate and the graphene channel as well as the effect of additional fixed charge owing to impurities or doping; n_0 is the residual mobile charge density in the graphene channel associated to electron/hole puddles; ρ_c is the metal-graphene contact resistivity (considered the same at the source and drain channel edges); ρ_g is the parasitic gate pad resistivity; L_g and W_g are the gate length and width, respectively; and t_{ox} and ϵ_{ox} are the gate oxide thickness and relative permittivity, respectively. Further information about the meaning of the CAD tool parameters can be found elsewhere [17, 26].

Note that these parameters will be used by default for the performance prediction throughout this work, except otherwise stated. To proceed with the predictive study of GFET subharmonic mixers performance, we consider the large-signal compact model developed by some of the authors in [26] and [27], and embedded into Keysight Advanced Design Systems (ADS©). Firstly, the model is validated at the device and circuit levels, combining experimental data and simulation. In particular, the DC characteristic $R_{DS} - V_{GS}$ of the considered GFET is compared against experimental measurements in Fig. 2, demonstrating excellent agreement in a wide range of bias around the Dirac point. In the following, we present and validate the GFET-based subharmonic mixer circuit.

Parameter	Value	Parameter	Value
μ	$2100\text{ cm}^2/\text{Vs}$	L_g	$1\text{ }\mu\text{m}$
V_{g0}	1 V	W_g	$20\text{ }\mu\text{m}$
n_0	$9.9 \times 10^{11}\text{ cm}^{-2}$	t_{ox}	25 nm
ρ_c	$560\text{ }\Omega \times \mu\text{m}$	ϵ_{ox}	8.4
ρ_g	$21\text{ }\Omega \times \mu\text{m}$		

Table 1 Input parameters for the CAD tool used to reproduce the measured data of the GFET reported in [19], where μ is the effective carrier mobility; V_{g0} is the gate offset voltage; n_0 is the residual charge density associated to electron/hole puddles; ρ_c is the metal-graphene contact resistivity; ρ_g is the parasitic gate pad resistivity; L_g and W_g are the gate length and width, respectively; and t_{ox} and ϵ_{ox} are the gate oxide thickness and relative permittivity, respectively

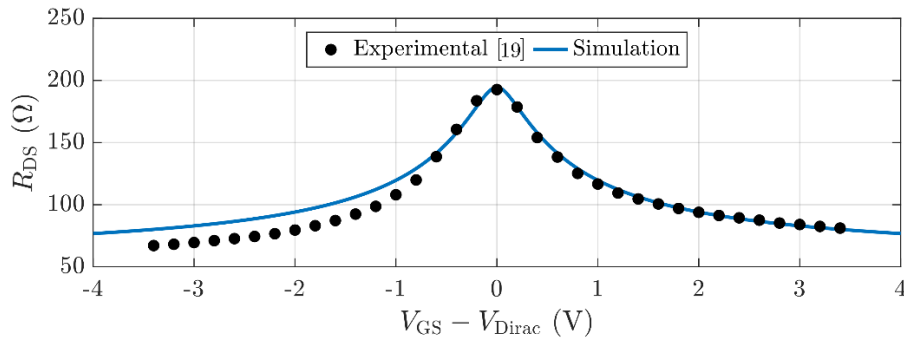


Fig. 2 Drain to source resistance, $R_{DS} = V_{DS}/I_{DS}$, versus overdrive gate voltage $V_{GS} - V_{Dirac}$

3. Theory and design of GFET-based subharmonic mixers

The schematic of the single-GFET mixer design proposed and studied in this work is depicted in Fig. 3. The resistive configuration implies that the LO signal is connected to the gate terminal of the GFET, whereas the RF and the IF signals are inserted and extracted, respectively, through the drain terminal. The input ports have associated frequencies f_{LO} and f_{RF} , so that the expected down-converted signal is $f_{IF} = f_{RF} - 2f_{LO}$, due to the frequency doubling achieved when $V_{GS} = V_{Dirac}$ (cf. working principle in Fig. 1). As displayed in the schematic, a DC voltage source at the drain is not required, and an RF choke (RFC) guarantees $V_{DS} = 0$ V, preventing DC power consumption. It is worth to note that a DC voltage source at the gate would neither be necessary if $V_{Dirac} = 0$ V. In a three-terminal GFET, for $V_{DS} = 0$ V, the Dirac voltage lies at $V_{Dirac} = V_{g0}$, which depends on the work-function difference between the gate metal and the graphene channel, as well as the possible presence of additional charges due to impurities or uncontrolled doping [28]. Indeed, intentional doping could be harnessed for GFET-based subharmonic mixing with no DC sources by properly tuning $V_{Dirac} = 0$ V. Naturally, this simple mixer topology requires proper filtering and impedance matching to mitigate port-to-port coupling, primarily caused by the LO large-signal, and to achieve the cleanest possible IF signal at its output port. These functions are satisfied by the blocks shown in the schematic, that will be addressed and detailed in the following subsections.

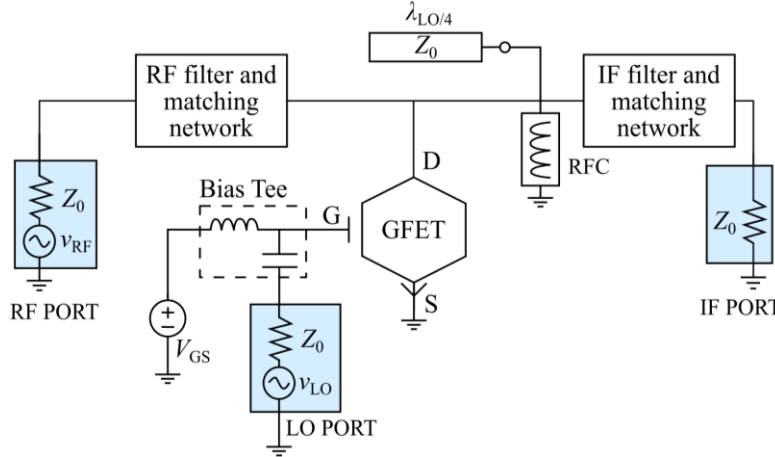


Fig. 3 Schematic showing the designed single-GFET subharmonic mixer, including a LO rejection filter. The RFC ensures zero drain voltage, while $V_{GS} = V_{Dirac}$. A bias tee is added to insert the LO signal, as well as low and high pass filters to isolate IF and RF components at the drain of the GFET

3.1. Selective rejection of spurious responses

A common rule in the design of single-FET resistive mixers (where the isolation between ports is weaker than that of the balanced structures) is to short-circuit the LO signal at the drain terminal [12, 17]. This feature becomes essential when the considered frequency range is high enough so that significant gate-to-drain coupling can be expected through the FET intrinsic gate-to-drain capacitance. A noteworthy feature in the design presented in Fig. 3 is the inclusion of an LO rejection filter, consisting in an open-loaded $\lambda_{LO}/4$ stub, to reduce the distortion of the output mixed signal without practically affecting neither the RF component nor the desired IF.

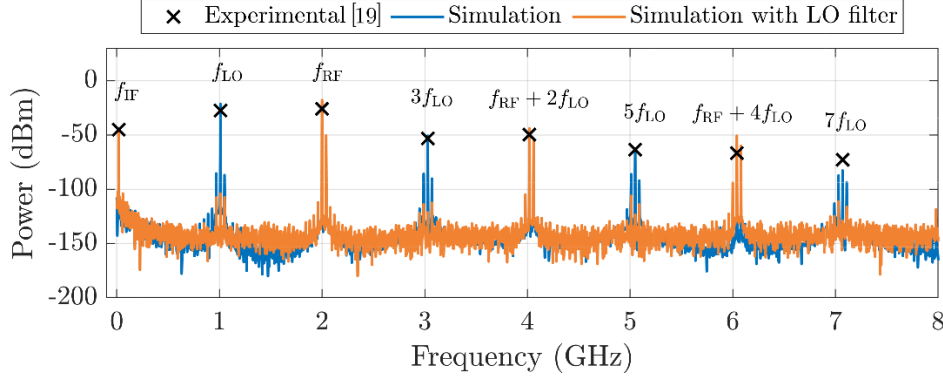


Fig. 4 Power spectral distribution obtained at the drain of the GFET, with $P_{LO} = 15$ dBm and $P_{RF} = -20$ dBm. Experimental data from [19] (crosses) and simulation, without (blue line) and with (orange line) the LO rejection filter, are compared. The simulation of the original topology properly fits the experimental data, while the modified circuit shows rejection of components involving odd LO harmonics, resulting in a less distorted mixed signal

Fig. 4 illustrates the resulting mixer output spectra for $f_{LO} = 1.01$ GHz and $f_{RF} = 2$ GHz (so that $f_{IF} = 20$ MHz), as derived from time-domain simulations of the topology shown in Fig. 3. Experimental data from [19] and the simulated result prior to the addition of the LO rejection filter reveal very similar power magnitudes, validating the model to an excellent agreement also at the RF regime. Furthermore, when considering the LO rejection filter, not only is the short-circuit of the fundamental LO frequency achieved, but, because of the periodic behavior of the distributed element, this short occurs at every odd multiple (f_{LO} , $3f_{LO}$, ...). Conversely, even-order components ($2f_{LO}$, $4f_{LO}$, ...) face an open-circuit impedance, so they are not affected by the filter. Due to the frequency proximity of f_{RF} and $2f_{LO}$, RF harmonics also remain unaltered. This aspect is critical to allow maximum RF power feed to the transistor to participate in the mixing process resulting in both unchanged CL and a less distorted mixed signal at the same time.

3.2. Simultaneous conjugate match of RF and IF ports

The inclusion of matching networks in mixers designs is essential in order to reduce power losses, especially in subharmonic topologies, where CL are usually higher than in fundamental architectures [29]. This task entails a challenging endeavor, mainly because of two key factors: 1) the inherent multi-frequency operation of mixers, resulting from the generation of numerous intermodulation frequency components, that precludes the correct loading conditions for all of them; and 2) the large-signal operation, that prevents the characterization in terms of small-signal parameters and therefore the direct application of the design theory associated with them.

To tackle this challenge, designers have sought, on the one hand, to minimize CL by terminating the idler frequencies at the RF and IF ports [22, 30, 31]. However, this approach calls for the introduction of more degrees of freedom into the circuit (to deal with these components impedance terminations) leading to increased complexity. Other authors have relied on the use of load-pull techniques [20, 21], but without offering a theoretical support to determine the optimal impedances. On the other hand, few authors have addressed the appropriate termination of the RF and IF ports at their respective RF and IF frequencies, pursuing conjugate impedance matching [34]. This approach represents the optimal solution when dealing with two-port linear time-invariant (LTI) networks [35, 36] but requires the adoption of some approximations for its application in the nonlinear and multifrequency nature

of mixers. Here we will seek to attain a feasible solution to the nonlinear and multifrequency conjugate matching problem, subsequently assessing its validity.

To do so, we first consider only two frequencies in the circuit for the purpose of impedance matching: the RF frequency and the IF frequency. These two signals play a fundamental role in determining the resulting CL of the mixer. Thus, generating optimal loading conditions for them (to improve transmission between their ports and minimize reflections) becomes crucial. The impedance mismatch of the LO port is less relevant [25], as long as we are able to compensate for the LO power waste to achieve optimum CL.

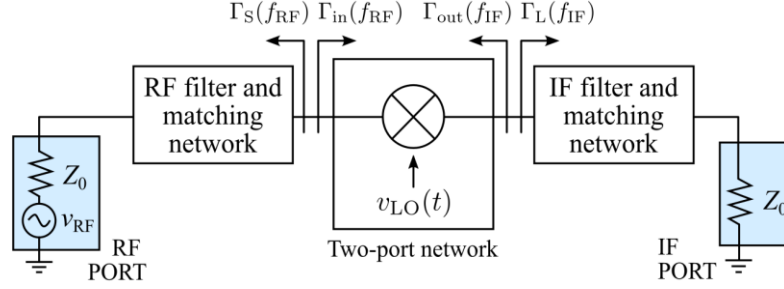


Fig. 5 Representation of a mixer as a quasi-linear time-variant two-port network, aiming at the impedance matching realization. The transistor, DC bias and LO source are included in the two-port network

Next, we will treat the circuit as a two-port system, which embeds the local oscillator, as shown in Fig. 5. In this way, the two-port network can be considered quasi-linear, since both ports (RF and IF) are subjected to small-signal excitations. Even so, we will characterize the system using large-signal S-parameters (LSSPs). Unlike small-signal S-parameters, which are derived from the linearization of a circuit under small-signal excitation, LSSPs are obtained through a harmonic balance (HB) simulation of the nonlinear circuit. Since HB is a large-signal simulation technique, LSSPs are power-dependent, making them suitable for evaluating the accuracy of the quasi-linear two-port approximation, particularly as the LO power level increases. Another motivating factor for employing LSSPs is their ability to represent the relationship between incident and reflected power levels at various frequencies, as required in the two-port system under consideration. In the following, S-parameters are defined as follows

$$S_{11} = \frac{b_{\text{RF}}}{a_{\text{RF}}} = |S_{11}| \angle \phi_{\text{b,RF}} - \phi_{\text{a,RF}} \quad (1)$$

$$S_{12} = \frac{b_{\text{RF}}}{a_{\text{IF}}} = |S_{12}| \angle 2\pi(f_{\text{RF}} - f_{\text{IF}})t + \phi_{\text{b,RF}} - \phi_{\text{a,IF}} \quad (2)$$

$$S_{21} = \frac{b_{\text{IF}}}{a_{\text{RF}}} = |S_{21}| \angle 2\pi(f_{\text{IF}} - f_{\text{RF}})t + \phi_{\text{b,IF}} - \phi_{\text{a,RF}} \quad (3)$$

$$S_{22} = \frac{b_{\text{IF}}}{a_{\text{IF}}} = |S_{22}| \angle \phi_{\text{b,IF}} - \phi_{\text{a,IF}}, \quad (4)$$

where a_{RF} and b_{RF} are the incident and reflected power waves at the RF port at f_{RF} ; a_{IF} and b_{IF} are the incident and reflected power waves at the IF port at f_{IF} ; and $\phi_{\text{a,RF}}$, $\phi_{\text{b,RF}}$, $\phi_{\text{a,IF}}$, and $\phi_{\text{b,IF}}$ are the phases associated with these waves.

Despite S_{12} and S_{21} are time-dependent quantities, it can be mathematically proven that the optimal reflection coefficients towards the generator and the load, Γ_{MS} and Γ_{ML} , respectively, are time-independent [34]. This is due to the fact that S_{12} and S_{21} appear in the Γ_{MS} and Γ_{ML} equations (see Appendix A) solely in the calculation of $\Delta = S_{11}S_{22} - S_{21}S_{12}$, i.e., as a product between them, where the time-dependence is cancelled: $S_{12}S_{21} = |S_{12}||S_{21}|\angle\Delta\phi_{\text{RF}} - \Delta\phi_{\text{IF}}$ and thus Δ is a time-invariant quantity. Therefore, for a specific LO power level, it is possible to implement the matching networks that satisfy (cf. Fig. 5)

$$\Gamma_{\text{MS}} = \Gamma_{\text{S}}(f_{\text{RF}}) = \Gamma_{\text{in}}^*(f_{\text{RF}}) \quad (5)$$

$$\Gamma_{\text{ML}} = \Gamma_{\text{L}}(f_{\text{IF}}) = \Gamma_{\text{out}}^*(f_{\text{IF}}) \quad (6)$$

Before the implementation of any impedance matching, the LSSP, depicted in blue solid lines in Fig. 6, are utilized to evaluate Γ_{MS} and Γ_{ML} , evidencing large mismatch reflections. Then, L-networks, simultaneously working as high and low pass filters for RF and IF, respectively, are employed to tune them. In a first step, the matching networks are designed for each P_{LO} value (i.e., adaptive matching, orange solid lines in Fig. 6). Based on the results, the reflection parameters (S_{11} and S_{22}) exhibit a significant improvement compared to the mismatched case, especially at low power levels. However, despite the matching networks being recalculated for each LO power, at high power levels S_{11} and S_{22} increase up to the point of reaching magnitudes similar to those without impedance matching (i.e., blue solid lines in Fig. 6). This is due to the fact that the implemented matching networks fail to achieve the expected impedance, as the small-signal approximation no longer holds.

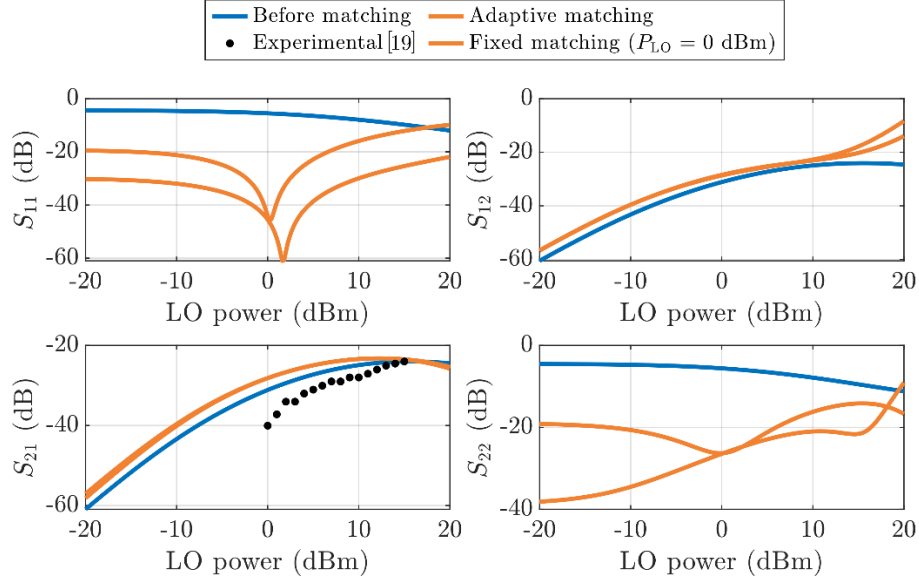


Fig. 6 Magnitude of the LSSP before (blue line) and after matching for a fixed input $P_{\text{LO}} = 0$ dBm (orange dashed line) and when adapting the matching networks for each P_{LO} (orange solid line) following the proposed implementation based on the two-port quasi-linear approximation. Black dots represent the measurement on the fabricated graphene-based subharmonic mixer [19]

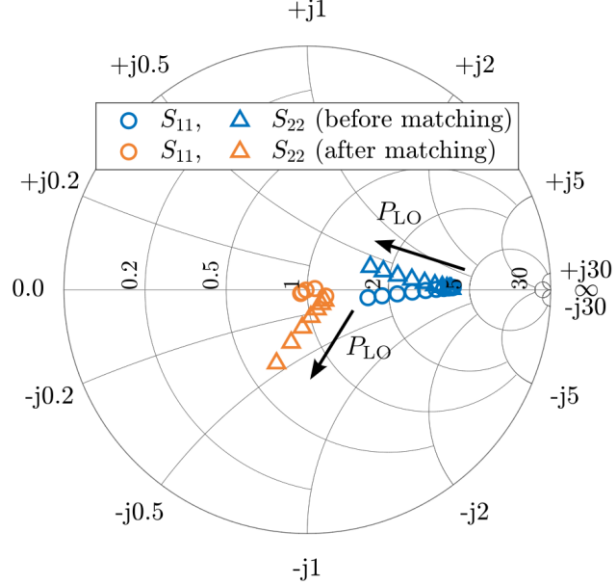


Fig. 7 Reflection LSSP before (blue) and after (orange) the introduction of adaptive impedance matching

To gain a deeper understanding of the underlying reason for the operational limitations of this matching approach, Fig. 7 depicts the Smith chart LSSP (S_{11} and S_{22}) of the designed mixer before and after the adaptive matching. Both parameters are, after the matching, shifted closer to the center of the chart for low P_{LO} , demonstrating the effectiveness of the matching networks. By contrast, as P_{LO} increases, a considerable deviation from the chart center occurs, which is much more noticeable for the reflection associated with the IF port (S_{22}).

Finally, as for a practical implementation, the impact on the LSSP when considering the fixed matching networks designed for $P_{LO} = 0$ dBm is also analyzed. In this case, S_{11} (dashed orange lines in Fig. 6) shows some significant variation for $P_{LO} \neq 0$ dBm, increasing roughly by 20 dB. S_{22} remains considerably stable across a wide range of power levels. Remarkably, both magnitudes are kept below -10 dB throughout the LO power window under test, reaching an acceptable matching for mixing operation. Concerning the transmission parameters (S_{12} and S_{21}), they both experience an enhancement (although of much lower magnitude) with matching, as depicted in Fig. 6. In particular, ~ 3 dB of improvement is achieved across a fairly wide range of power levels. An interesting observation is that the fixed matching design at $P_{LO} = 0$ dBm yields essentially the same results as the adaptive case, leading to the conclusion that S_{12} and S_{21} are mostly insensitive to the variation of P_{LO} at low power levels.

The behavior of losses can be analyzed looking at Fig. 6c, given that they are equivalent to the LSSP $-|S_{21}|$. As extracted from it, the CL can be improved by pumping the gate with higher LO level. However, its power cannot be increased indefinitely, since, at some point, the rectified voltage at the drain of the intrinsic device is enough to generate a significant shift of the transfer characteristic given by $V_{Dirac} = V_{g0} + V_{DS}/2$ [28], so that the second-order harmonic of LO is degraded and CL increases. The experimental data from Fig. 6c did not display this regime under the utilized LO power levels, but the simulation demonstrates the deterioration of CL as P_{LO} is higher than 15 dBm.

4. Results and discussion

We will explore now the influence of the GFET technological and geometrical variables on the mixer performance, paying particular attention to the CL and the on-off resistance ratio as main figures of merit (FoMs). Unlike transconductance mixers, the metric that needs to be optimized in a resistive mixer is not the time-dependent transconductance $g_m(t)$, but the time-dependent channel conductance $G_{DS}(t)$ [25]. This variable is related to the DC $I_{DS} - V_{GS}$ response, as long as the LO signal is able to bias the GFET around $V_{GS} = V_{Dirac}$, and thus generate a time-varying resistance $R_{DS}(t) = 1/G_{DS}(t)$. We will analyze the role of the main technological (i.e. gate offset voltage, effective carrier mobility, contact resistivity, and residual carrier density) and geometrical (gate length and oxide thickness) parameters on the device DC operation by inspecting the $I_{DS} - V_{GS}$ characteristics, and more importantly its eventual impact on the on-off resistance ratio and on the CL.

We first consider the effect of a shift in the V_{GS} bias around V_{Dirac} , which in single-gated GFET operating at $V_{DS} = 0$ V (as in the resistive mixer) corresponds to $V_{Dirac} = V_{g0}$ [28]. Fig. 8a shows CL as a function of $V_{GS} - V_{g0}$ for different local oscillator power levels. Minimum CL are obtained when the gate is precisely biased at V_{g0} , as the LO signal, $v_{LO}(t)$, takes full advantage from the graphene quadratic response. This can be better appreciated in Fig. 8b where $R_{DS} - V_{GS}$ is represented for different values of V_{g0} (corresponding to the blue circles in Fig. 8a) together with a sketch of a $v_{LO}(t)$ signal with an amplitude corresponding to $P_{LO} = 0$ dBm. As can be noted, CL strongly degrades as the $V_{GS} = 0$ V point is shifted from the vertex of the $R - V$ inverted parabola in Fig. 8b, i.e., when there is a large mismatch between V_{GS} and V_{g0} . This leads to the deterioration of the symmetrical quadratic behavior of the transfer characteristic in the range of the LO oscillator signal (red-shaded region in Fig. 8b), in such a way that the frequency doubling is not optimally achieved. In more detail, higher order harmonics different from the second order are generated, provoking a severe reduction of the down-converted IF signal output power. This results in an increment of the CL, as observed in Fig. 8a. Notably, the plateau in Fig. 8 where the CL remains small (e.g. below 30 dB) is larger for higher P_{LO} .

In other words, high P_{LO} values make the GFET mixer more tolerant to gate bias mismatching in terms of CL. This is explained by the fact that a larger v_{LO} amplitude eases the operation in the quadratic region of the GFET $I - V$ (i.e., within the graphene ambipolarity regime) for higher $|V_{GS} - V_{g0}|$ values. This is identified with a widening in the CL versus $V_{GS} - V_{g0}$ curves as P_{LO} increases (cf. Fig. 8a). This result gives critical insights on the tolerance needed for controlling the charge neutrality point (CNP) in GFETs for their ulterior application for subharmonic mixing depending on the available LO power.

The monotonic increase in CL with $|V_{GS} - V_{g0}|$ is interrupted (a discontinuity in the derivative of the CL is indeed observed) for $|V_{GS} - V_{g0}|$ values close to the amplitude of v_{LO} , i.e., when V_{Dirac} leaves the range of v_{LO} amplitudes. This behavior is related to the transition of the GFET channel from ambipolar to fully unipolar conduction. This is a remarkable result because it brings to light that graphene ambipolarity presents a very interesting nonlinear feature that can be exploited for nonlinear high-frequency applications [16], such as mixers and frequency multipliers [8]. The latter have already been demonstrated in the form of a frequency tripler [9] and quadrupler [10] by producing a mismatch between V_{GS} and V_{Dirac} , showing that other higher order harmonics different from the first and second orders can be produced within the ambipolar regime. It is worth to note that, beyond the biases at which the CL get their maximum value, the unipolar conduction retains a nonlinear behavior, making subharmonic operation still possible. Certainly, that region results on much higher CL than the minimum value reached at $V_{GS} = V_{g0}$, where the ambipolarity is fully exploited for frequency doubling.

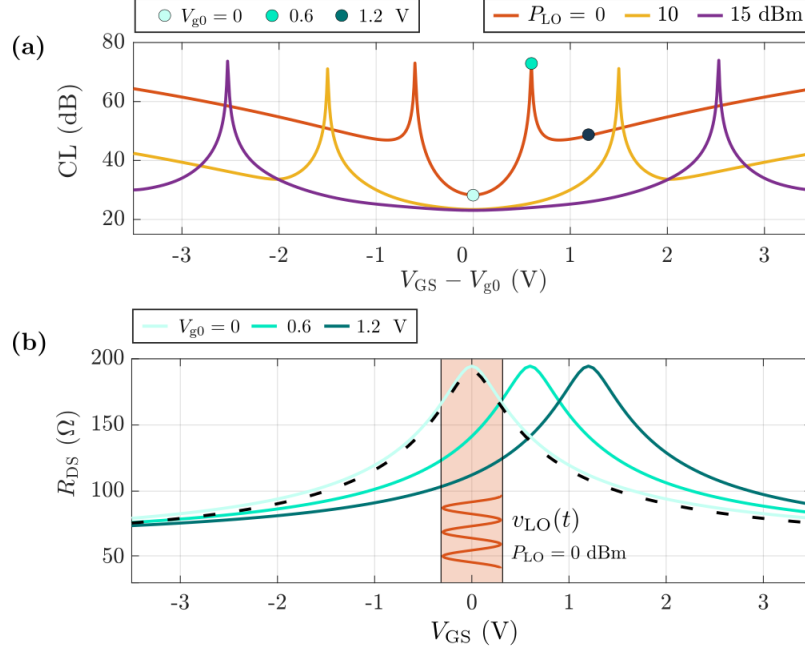


Fig. 8 Study of the effect of V_{GS} and V_{g0} mismatching on mixing performance. a) Conversion losses versus overdrive gate bias for different LO power levels. b) $R_{DS} - V_{GS}$ characteristics for different V_{g0} values; the time-varying LO input signal is depicted in orange, corresponding to $P_{LO} = 0$ dBm

Next, the influence of the carrier mobility on the performance of the mixer is evaluated. Fig. 9a shows the dependence of CL on the mobility for different LO power levels. In contrast to the conventional trend observed in transconductance mixers, in which g_m and consequently CL are limited by μ [37], losses in a GFET subharmonic mixer have a non-monotonic behavior with μ , giving rise to an optimum value dependent on the power of the local oscillator.

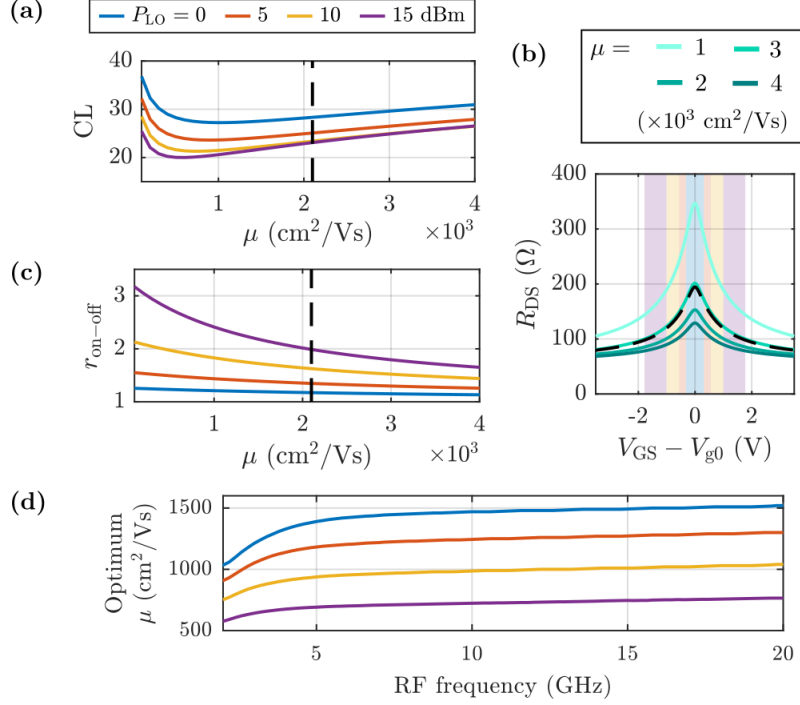


Fig. 9 Study of the effect of μ on mixing performance. a) Conversion losses for different LO power levels. b) $R_{DS} - V_{GS}$ characteristics for different μ values. c) On-off ratio calculated from the $R_{DS} - V_{GS}$ curves within the $\pm 3V$ gate voltage window. d) Optimum mobility value reaching the minimum conversion losses as a function of the frequency of the RF signal. A black dotted line indicates the mobility value for the device under consideration (Table 1)

In order to explain this behavior, it is worth to pay attention to a well-known performance metric in conventional resistive mixers, i.e. the on-off resistance ratio $r_{on-off} = R_{DS,off}/R_{DS,on}$ [38], which has been extended to contemporary realizations of GFET subharmonic designs [18, 19, 39-41]. Fig. 9b shows the GFET DC R - V characteristics for varying μ , exhibiting monotonic increases of both $R_{DS,off}$ and $R_{DS,on}$ with decreasing mobility. The on-off resistance ratio is then computed from the R - V curves, resulting in the trends observed in Fig. 9c. It must be noted that $R_{DS,on}$ and $R_{DS,off}$ vary with P_{LO} as the LO voltage oscillation ranges a different R - V window (cf. Fig. 8a). As can be observed, higher μ values result in a considerable reduction of r_{on-off} , explaining the strong deterioration in CL seen in Fig. 9a for the high carrier mobility region ($\mu \gtrsim 1000$ cm²/Vs). Nevertheless, the higher r_{on-off} seen in Fig. 9c for low mobility values is not translated into a reduction in CL, which, in fact, experience a trend change, increasing for $\mu \lesssim 200$ cm²/Vs and thus resulting in an optimum μ for minimum CL. This is due to the fact that the analysis of the CL based on the behavior of the DC r_{on-off} relies on the assumption that the GFET mixer operation frequency is lower than the transistor cutoff frequency in the nonlinear regime, $f_T^{NL}(\propto \mu)$, which sets the operating frequency limit. A significant decrease in f_T^{NL} is expected at very low μ , meaning that a non-negligible portion of the LO power will be leaked through the capacitive couplings between the GFET terminals. This unavoidably leads to an increase in the CL, as the effective power provided by the LO contributing to the mixing is reduced. In this regard, Fig. 9d depicts the optimum GFET mobility for minimizing CL as a function of the RF frequency, where higher operating frequencies require a rise of the optimal mobility. In addition, it must be highlighted that the larger the LO power, the lower the value of the optimum μ , indicating that the cutoff frequency for this nonlinear application increases with P_{LO} . This is beneficial as a lower value of the optimum μ , allows for higher resistance ratios that improve losses. Thus, it can be

concluded that for increasing P_{LO} , the mobility region where f_T^{NL} limits the mixer behavior, i.e., for mobilities lower than the optimum μ , diminishes; and consequently, the region dominated by r_{on-off} increases, i.e., for mobilities higher than the optimum μ .

The impact of the technological parameters is concluded with the study of the residual carrier density and the contact resistivity on both CL and r_{on-off} , evaluated in Fig. 10a-b. As can be seen, the increase of n_0 and ρ_c , portrays a continuous upward trend in losses, which aligns with the concurrent downward trend observed for r_{on-off} , meaning that this metric is able to anticipate the effect of the variability of these parameters.

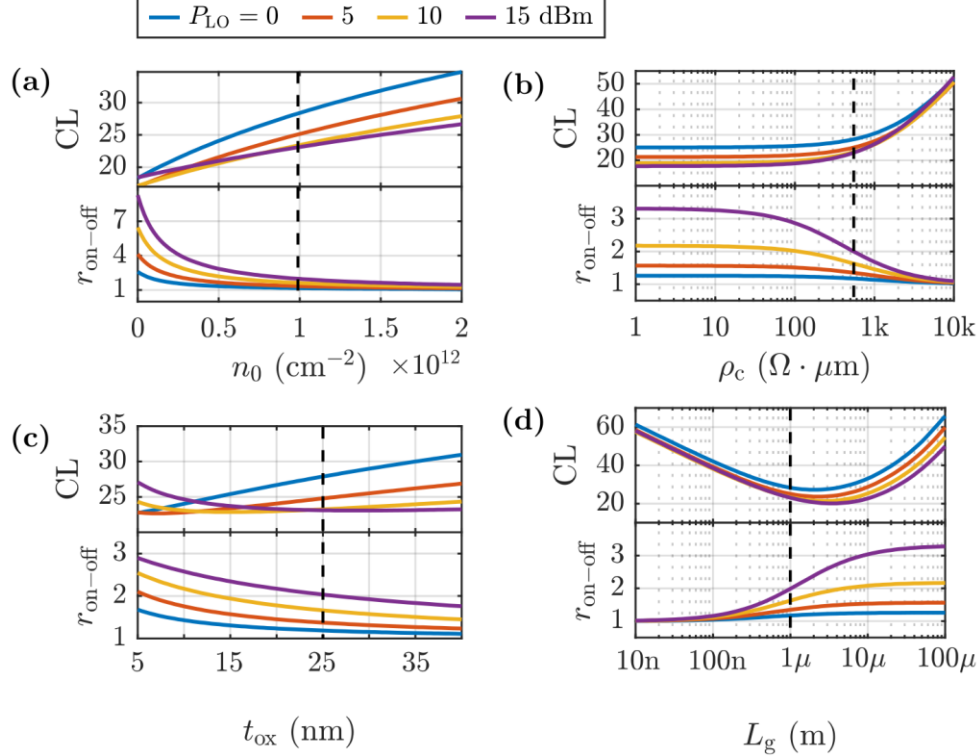


Fig. 10 Evaluation of CL (top) and r_{on-off} (bottom) as a function of (a) residual carrier density (n_0); (b) contact resistivity (ρ_c); (c) oxide thickness (t_{ox}); (d) gate length (L_g). Black dotted lines highlight the value corresponding to the device under consideration (Table 1)

Finally, we evaluate the role of the GFET geometrical parameters on the mixer performance. In particular, Fig. 10c-d shows the influence of the oxide thickness and gate length on CL and r_{on-off} . As can be noticed, while r_{on-off} increases monotonically with decreasing t_{ox} and increasing L_g , as well as with P_{LO} , the behavior is more irregular for CL. Losses follow a non-monotonic trend with these parameters, presenting a minimum which is shifted by P_{LO} . This evidences that the CL behavior cannot be predicted based solely on the analysis of r_{on-off} . Indeed, as explained before, if the operating frequencies involved in the mixing process are much higher than the transistor cutoff frequency, with qualitative trends of $f_T^{NL} \propto t_{ox}$ and $f_T^{NL} \propto L_g^{-2}$ [37], the AC large signal behavior becomes essential. In this regard, an increase in oxide thickness leads, in principle, to higher CL due to a decrease in the on-off ratio (Fig. 10c). However, decreasing t_{ox} rises the oxide capacitance C_{ox} , therefore causing part of the LO power to leak through the capacitive coupling rather than contributing to the modulation of R_{DS} . In fact, the same effect would occur if the operating frequency of the circuit were significantly

increased, as this would also reduce the impedance associated with the oxide, allowing for greater filtering of the LO power toward the output.

The non-monotonic behavior of CL vs. gate length, illustrated in Fig. 10d, can also be qualitatively split in two regimes. For short gate lengths, up to the optimum gate length reaching the minimum CL, the rising resistance ratio induces a negative slope in the CL vs. L_g curve, indicating potential enhancement of mixer performance through the design of longer gates. The reversal in this trend, observed for larger L_g values, is attributable once again to the device nearing the limit given by its cutoff frequency when operating as mixer. In addition, higher optimum L_g is observed due to the higher f_T^{NL} with increasing LO power.

5. Conclusion

A systematic design approach was developed for a single-GFET subharmonic mixer, ensuring the preservation of a straightforward topology featuring zero-drain bias, which renders the circuit a promising candidate for future ubiquitous frequency-conversion IoT systems. In more detail, we presented a novel circuit design approach, including the selective LO filtering using a quarter-wave resonator to optimize the rejection of LO-related spurious components, and the simultaneous conjugate matching strategy using a quasi-linear approximation achieving very low IF and RF reflection coefficients. These techniques can be directly applied to any other subharmonic mixer topology, contributing to the advancement of the state of the art for these circuits.

Furthermore, an in-depth examination of the GFET technology drivers and its correlation with the mixer performance has revealed the trade-off between a wider drain-to-source resistance range (i.e., the on-off ratio) and the overall increase in current resulting from higher carrier mobility or shorter gates, within the constraints imposed by the device dynamic response. Such findings mark a significant advancement in the present understanding of the GFET-based mixer behavior.

Declarations

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Competing interest The authors declare no competing interests.

Data availability Not applicable

Code availability Not applicable

Authors' contributions The conceptualization and methodology of the study were carried out by M. C. Pardo, F. Pasadas, and F. G. Ruiz. All authors contributed to the formal analysis, investigation, and writing of the original draft of the manuscript. Review and editing were performed by M. C. Pardo, F. Pasadas, E. G. Marin, A. Godoy, and F. G. Ruiz. Funding acquisition was secured by M.

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Appendix A

The expressions of optimum source and load reflection coefficients Γ_{MS} and Γ_{ML} that attain simultaneous conjugate matching in a two-port circuit are [36]:

$$\Gamma_{\text{MS}} = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \quad (7)$$

$$\Gamma_{\text{ML}} = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \quad (8)$$

where

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \quad (9)$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \quad (10)$$

$$C_1 = S_{11} - \Delta S_{22}^* \quad (11)$$

$$C_2 = S_{22} - \Delta S_{11}^* \quad (12)$$

$$\Delta = S_{11}S_{22} - S_{21}S_{12} \quad (13)$$

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