



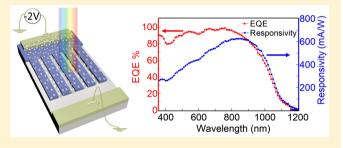
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# High Responsivity and Quantum Efficiency of Graphene/Silicon Photodiodes Achieved by Interdigitating Schottky and Gated Regions

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Supporting Information

**ABSTRACT:** Graphene/silicon (G/Si) heterostructures have been studied extensively in the past years for applications such as photodiodes, photodetectors, and solar cells, with a growing focus on efficiency and performance. Here, a specific contact pattern scheme with interdigitated Schottky and graphene/ insulator/silicon (GIS) structures is explored to experimentally demonstrate highly sensitive G/Si photodiodes. With the proposed design, an external quantum efficiency (EQE) of >80% is achieved for wavelengths ranging from 380 to 930 nm. A maximum EQE of 98% is observed at 850 nm, where



the responsivity peaks to 635 mA/W, surpassing that of conventional Si p-n photodiodes. This efficiency is attributed to the highly effective collection of charge carriers photogenerated in Si under the GIS parts of the diodes. The experimental data is supported by numerical simulations of the diodes. On the basis of these results, a definition for the "true" active area in G/Si photodiodes is proposed, which may serve toward standardization of G/Si-based optoelectronic devices.

KEYWORDS: graphene, Schottky diode, interdigitated contact, inversion layer, photocurrent, generation area

raphene optoelectronic devices typically show limited J photoresponsivity as a result of a weak optical absorption per layer (2.3%). Nevertheless, the material has great potential as a transparent and antireflective junction when combined with two-dimensional (2D) and three-dimensional (3D) semiconductors for a number of optoelectronic device applications.<sup>2-4</sup> Graphene/silicon (G/Si) is the most widely studied fundamental heterostructure, as it extensively utilizes the existing Si technology.<sup>2,5,6</sup> G/Si heterostructures are a basic component of many potential applications, such as rectifiers, chemical and biological sensors, solar cells, 11-14 and, in particular, photodetectors. The latter include G/Si Schottky photodetectors for near-infrared (NIR)25 and ultraviolet (UV)<sup>29</sup> light detection. Different strategies have been explored to enhance the performance of G/Si photodiodes. Chemical doping of graphene has been demonstrated by Miao et al. to shift the Fermi level in graphene down with respect to the Dirac point, thereby increasing the built-in potential in G/Si solar cells and resulting in an EQE of 65%. 14 However, chemical doping of graphene is unstable and unreliable when exposed to air and humidity.<sup>30</sup> Another approach is to utilize interfacial oxide layers on photodiodes.

Selvi et al. demonstrated that such interfacial oxides increase the Schottky barrier height (SBH) and lead to an enhancement in photovoltage responsivity, particularly for low light intensities.<sup>31</sup> Complex nanotip patterning of substrates was employed to improve the photoresponse of G/Si Schottky diodes.<sup>28</sup> Here, the nanotip surface enhances light collection due to multiple reflections, and the tip-enhanced electrical field enables photocarrier separation with internal gain due to impact ionization, resulting in a responsivity of 3 A/W under white-light illumination.<sup>28</sup> Recently, we have pointed out the significant role of insulating regions in parallel to the Schottky regions in achieving high photocurrents through scanning photo current (SPC) measurements.3 We have further provided a model for the physical mechanisms, i.e., the formation of an inversion layer in Si.<sup>3</sup> Similar conclusions have been reported in refs 21 and 23, where capacitance-voltage and current-voltage (I-V) measurements were carried out at different temperatures for validation. This fundamental

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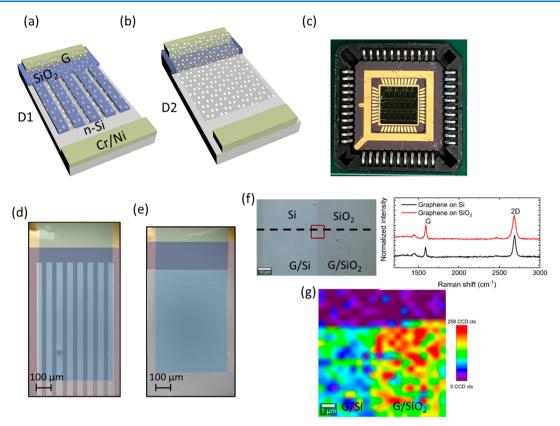


Figure 1. Schematics of G/Si photodiodes of types (a) D1 and (b) D2 (control device). (c) Photograph of a wire-bonded diode chip in a chip package. Scanning electron micrographs of two diodes of types (d) D1 and (e) D2. The SEM images are color-enhanced to show the position of the graphene film (blue), SiO<sub>2</sub> (purple), and the metal electrodes (yellow). (f) Optical micrograph of the region selected for acquiring a Raman area map (red square). Graphene covers the area below the dashed line. Single Raman spectra of graphene on Si (lower curve) and on SiO<sub>2</sub>/Si region (upper curve) acquired for  $\lambda = 532$  nm. (g) Raman intensity map of the 2D band in the area marked in (f).

observation of the origins of photocurrent generation is a key to further improve the performance of G/Si photodiodes.

In this work, we demonstrate that the graphene on interdigitated patterned SiO<sub>2</sub>/Si substrates harvests the carriers photogenerated in Si much more efficiently than the conventional G/Si diode structures, where only small areas of SiO<sub>2</sub> are used just to isolate graphene from Si in the non-Schottky regions. The investigated structures are compatible with the existing Si technology and require no specific process steps for fabricating G/Si diodes beyond graphene transfer. Our devices show an absolute spectral responsivity of 635 mA/W (calculated by considering the entire charge generation area, which includes oxide regions). This value is about 30% higher than that observed in commercial Si photodetectors and about 50% higher than recently reported for Si p-i-n photodiodes with complex photon-trapping microstructures at a wavelength of 850 nm.<sup>32</sup>

Motivated by our previous findings,<sup>3</sup> diodes with interdigitated G/Si (Schottky) and graphene/insulator/silicon (GIS) regions were designed, where the insulated regions made up a significant portion of the active device area. Two different types of diodes were fabricated per chip. In diode D1, graphene is in contact with interdigitated SiO<sub>2</sub>/Si structured substrates (Figure 1a), while in diode D2, the control device, graphene is mostly in contact with the Si substrate in a manner similar to conventional diode layouts and covers just a small SiO<sub>2</sub> area (Figure 1b). Detailed information about the geometry of the devices is presented in Figure S1. A number of D1-type diodes were designed with varying widths of the

GIS regions (Figure S1). The devices were fabricated by transferring large-area CVD graphene onto prepatterned substrates of lightly doped n-Si with a  $t_{ox} = 20$  nm SiO<sub>2</sub> layer (details in the Methods section) and can, in principle, be carried out at the wafer scale.<sup>33</sup> The reason for choosing the lightly doped n-type Si substrate is that Gr/Si diodes on the lightly doped n-type substrate result in a higher Schottky barrier and show higher rectification.<sup>34</sup> The final chips with different devices were inserted and wire-bonded into a chip carrier for optoelectronic characterization (Figure 1c). Figure 1d and e show color-enhanced scanning electron micrographs of diodes D1 and D2, respectively. The two distinct regions in each device, i.e., the G/Si Schottky junctions and the GIS structures, behave differently under illumination. However, charge carriers can only be extracted through the Schottky junction areas, which act as a collector. This region determines basic diode parameters such as ideality factor and SBH. The graphene quality was assessed through scanning Raman spectroscopy using a wavelength of 532 nm. Figure 1f shows an optical micrograph of the region where Raman spectra of graphene on Si and on SiO2 were acquired. A 2D/G intensity ratio >1 indicated the monolayer nature of CVD graphene transferred on the devices. We observed slightly sharper and less intense graphene Raman peaks on Si, as expected (Figure 1g, 2D band intensity). Such changes in Raman features of graphene on Si were not found to have a direct correlation to the performance of our devices, where graphene is merely acting as a transparent conductive contact.

*I–V* characteristics of the diodes under dark (solid lines) and illuminated (dashed lines) conditions are shown in Figure 2a in semilogarithmic scale. Both the diodes D1 and D2 clearly

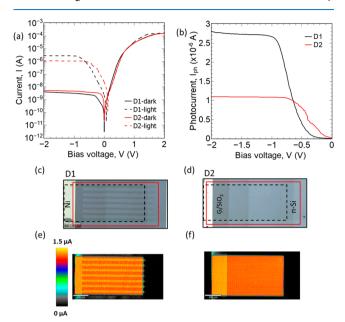


Figure 2. (a) Diode current in logarithmic scale as a function of bias voltages of G/Si photodiodes (D1 and D2) in the dark and under illumination. The effect of photocurrent generation can be observed for negative bias voltage, i.e., in reverse bias mode. (b) Photocurrents of G/Si photodiodes (D1 and D2). Optical micrographs of diodes (c) D1 and (d) D2. The area inside the red rectangle in (c) and (d) was scanned for photocurrent measurements. The graphene region is represented by the black dashed rectangle. Photocurrent maps of the scanned area for (e) D1 and (f) D2 at a laser wavelength of 532 nm, power of 5  $\mu$ W, and a reverse bias of -2 V. The scale bar in (c-f) corresponds to 200  $\mu$ m.

exhibit rectifying behavior in the dark with rectification ratios, defined as forward current at + 2 V)/reverse current at -2 V, of up to  $5 \times 10^4$  and  $4 \times 10^4$ , respectively. The general photoresponsivity of the diodes was measured under LED white-light illumination with an intensity of 30  $\mu$ W/cm<sup>2</sup> (see Methods). The forward I-V characteristics of the diodes were fitted using standard expressions, 35,36 which yielded ideality factors  $(\eta)$  of 2.08 and 2.3 and Schottky barrier heights (SBH) of 0.74 and 0.79 eV for diodes D1 and D2, respectively. Only the Schottky (collection) area has been employed for the estimation of these parameters. The details on the diode parameters evaluation are presented in Figure S2. The ideality factors  $(\eta)$  reported for G/n-Si Schottky junctions vary in the range of  $\sim$ 1.1 to 7.69, depending on the quality of the interface between the graphene and the semiconductor.<sup>2,14,37</sup> A significant variation in reported values of  $\eta$  can be attributed to inhomogeneities and impurities at the G/Si junction<sup>38</sup> originating from graphene-transfer related issues<sup>39</sup> or thin inevitable interfacial SiO<sub>2</sub> layers.<sup>2,31,40</sup> A small photovoltaic effect can be observed in Figure 2a for both devices. A slightly higher open circuit voltage in D2 (112 mV) compared to D1 (73 mV) can be attributed to a higher built-in potential in D2, as the SBH is greater in this device. It should be mentioned here that the SBH values in G/Si diodes strongly depend on the quality of the transferred graphene and on the interface properties between graphene and Si. Therefore, SBH values can significantly vary from device to device. The evolution of photocurrent, defined as  $I_{\rm ph} = I_{\rm light} - I_{\rm dark}$ , versus reverse voltage  $(V_R)$  for both diodes is shown in Figure 2b. Diode D1 exhibits higher photocurrent in most of the applied voltage range than the control device (D2), except below -0.6 Vwhere the two curves cross, and D2 yields higher photocurrent than D1. Similar bias voltage dependencies were observed in spectral response (SR) measurements of the devices (see below). This can be explained through the formation of an inversion layer under the GIS part of the devices, as shown for other oxide thicknesses in ref 3. The formation of such an inversion layer decreases surface recombination at the SiO<sub>2</sub>/Si interface. 41,42 It further forms a quasi PN junction with the regions covered by Schottky contacts, which facilitates the transit of the photogenerated carriers to the Schottky iunctions. 3,21,23 The so-formed inversion layer in the GIS region results in a higher photocurrent in diode D1 than in a purely Schottky junction of the same area (D2). In contrast, at lower voltage bias below -0.6 V, where the GIS region is either in depletion or in weak inversion, interface traps limit the transport of photogenerated charge carriers to the Schottky junction. Therefore, photocurrent generated at the Schottky junction is largely dominating below -0.6 V, resulting in a higher photocurrent in diode D2 than in D1, which has a larger GIS region.

Large-area scanning photocurrent (SPC) measurements provide insight into the spatial distribution of photocurrents. We recorded SPC maps of the diodes using a  $\lambda = 532$  nm laser with a spot size of 2.4 µm. Figure 2c,d shows optical micrographs of both devices, where the red rectangle indicates the scanned area, and the black dashed line represents the graphene area. The maps were obtained using a 10× objective over an area of  $1.3 \times 0.6$  mm with a scan speed of 0.4 s/line and integration time of 1 ms. Photocurrent maps of the devices obtained at -2 V with a laser power of 5  $\mu$ W are shown in Figure 2e,f. For both devices, higher photocurrents were recorded in the GIS region compared to the G/Si region. This observation is consistent with our previous findings<sup>3</sup> and attests the significance of the inversion layer in the GIS regions toward the total photocurrent. The devices even showed a significant photocurrent at low reverse biases, pointing toward their potential applicability as low-power and highly sensitive photodiodes (Figure S3). Moreover, it should be highlighted that the diodes did not show a significant degradation in their electrical performance, even without encapsulation, over a time span of nearly six months (Figure S4). The samples were kept in a simple vacuum desiccator during this time.

A figure of merit for photodetection, i.e., how a photodetector absorbs and responds to the incoming light, is responsivity. It is a measure of output current per unit of incident optical power. In conventional Schottky and PN photodiodes, the Schottky or PN region is considered as the active area for calculating the absolute SR or photoresponsivity. Here, "active area" is equivalent to the device's region, where charge carriers are generated by the absorbed incident photons. Conventional Schottky diodes consist of thin metal films in the active area and thick metal contacts, which are opaque to light. The latter regions are legibly not considered as photoactive areas. Graphene, in contrast, has broadband transparency of around 97%, which allows light to penetrate into the Si substrate in both the Schottky and the GIS areas. This enables illumination of silicon trough the G/ SiO<sub>2</sub> stack and generation of charge carriers therein. This is also confirmed in SPC measurements (Figure 2e,f) where

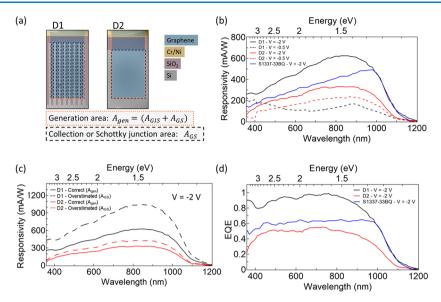


Figure 3. (a) Color-enhanced scanning electron micrographs indicating the photocurrent generation areas  $(A_{\rm gen})$  and the collection areas  $(A_{\rm GS})$  in devices D1 (left) and D2 (right). (b) Measured responsivity vs wavelength (lower x-axis) and energy (upper x-axis) of G/Si photodiodes for wavelengths ranging from 360 nm (3.4 eV) to 1200 nm (1 eV) at reverse biases of -2 V (solid lines) and -0.5 V (dotted lines) in comparison with a commercially available Si (S1337-33BQ) photodetector (blue line). (c) Overestimated responsivity (dashed lines) calculated by considering only  $A_{\rm GS}$  in comparison with correctly calculated responsivity by considering the entire  $A_{\rm gen}$  (solid lines) of D1 (black) and D2 (red) at reverse bias of -2 V. (d) External quantum efficiency (EQE) vs wavelength and energy of G/Si photodiodes at reverse bias of -2 V in comparison with S1337-33BQ photodetector (blue line).

significant photocurrent was detected underneath GIS regions because of light absorption in Si. Thus, both the GIS and the Schottky area have to be defined as active regions, which we propose to call "generation area"  $A_{\rm gen}$ , rather than active area, with

$$A_{\rm gen} = A_{\rm GIS} + A_{\rm GS} \tag{1}$$

where  $A_{\rm GIS}$  is the GIS area, and  $A_{\rm GS}$  is the G/Si Schottky junction area, which is marked with a dashed black line in Figure 3a. This consideration is of significant importance while measuring SR of the diodes where area consideration is warranted. The absolute SR was then measured taking into account  $A_{\rm gen}$ , marked with a dashed orange line in Figure 3a, through a comparative method to the known SR of a reference detector using a LabVIEW controlled setup. Details of the procedures are explained in the Supporting Information.

Figure 3b shows the SR of the diodes measured over a spectrum from  $\lambda = 360$  to 1200 nm and for two different applied reverse bias voltages of -2 V (solid lines) and -0.5 V (dashed lines). For a comparison, the responsivity of a commercial IR-enhanced Si PIN photodetector (S1337-33BQ: blue curve) at an applied reverse bias of -2 V (at its normal operating point) is also shown in Figure 3b. The responsivity values are reported by considering the proposed area given by eq 1. The highest absolute responsivity was obtained for the interdigitated device D1 with a maximum of 635 mA/W at  $\lambda$  = 850 nm, which is about 89% higher than that of D2 (maximum of 330 mA/W). It is further surpassing the SR of the commercial detector by about 28% (maximum of 490 mA/W) measured at -2 V under the same conditions. The enhanced SR of diodes with interdigitated structures was found to be consistent for different devices with varying GIS region widths (Figure S1). In all cases, the maximum response is well within the Si absorption spectrum. Both devices D1 and D2 showed an increase of the absolute spectral responsivity with the applied reverse bias, but D1 showed a lower responsivity than

D2 at an applied reverse bias of -0.5 V (Figure 3b, black and red dotted lines). D1 then outperformed D2 for a larger bias of -2 V (Figure 3b, black and red solid lines). This is in agreement with the measured  $I_{\rm ph}$  in Figure 2b. To demonstrate how much responsivity can be overestimated, the SR was recalculated for both devices by only considering the Schottky area ( $A_{\rm GS}$ ) as an active area, which is obviously smaller than  $A_{\rm gen}$ . The dashed lines in Figure 3c represent overestimated responsivity, while the solid lines were calculated by considering the entire  $A_{\rm gen}$ , resulting in correct responsivity. This clearly shows that ignoring the GIS area in G/Si diodes can lead to significant overestimation of responsivity, especially when the GIS area covers large parts of the device. Table S1 in the Supporting Information compares the responsivity of diode D1 with those of G/Si diodes reported in the literature.

External quantum efficiency (EQE) of the devices was calculated from the measured responsivity as  $EQE = \frac{Rhc}{c^2}$ . Here, q, h,  $\lambda$ , and c are electron charge, Planck's constant, wavelength, and speed of light, respectively. Figure 3d shows the EQEs of devices D1, D2, and the commercial Si photodetector over a broad spectrum at an applied reverse bias of -2 V. The EQE in D1 reached values above 80% in the wavelength range from 380 to 930 nm, covering the whole visible and near-infrared region, with a maximum value of 98%. As Si is the main absorber in these devices, EQE decays quickly for photon energies below the bandgap of Si. This very high EQE for the G/Si photodiodes has been achieved merely by interdigitating the GIS regions with the Schottky junctions, i.e., without complex device designs. This compares extremely well with pure Si p-i-n diodes, where an EQE of about 60% was achieved recently for a limited wavelength range from 800 to 860 nm, where complex micro and nanostructured holes were used for efficient light trapping.<sup>32</sup> With this design, we obtained a comparable EQE to that reported in ref 43, in which the authors used nanostructured black Si surfaces in

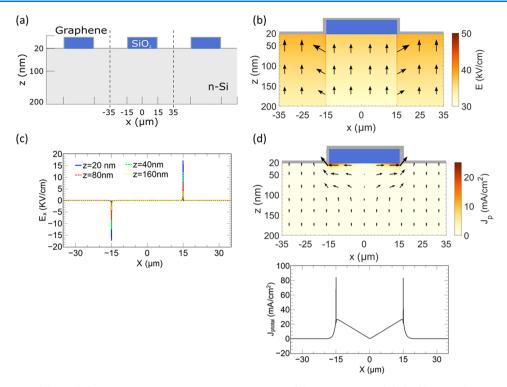


Figure 4. (a) Schematic of the multifinger structure representing a cross section of device D1. Vertical dashed lines enclose one finger from -35 to  $35 \,\mu\text{m}$ , with horizontal axis  $x = 0 \,\mu\text{m}$  located at the center of the finger. The  $\text{SiO}_2$  thickness is 20 nm, and  $z = 20 \,\text{nm}$  corresponds to the  $\text{SiO}_2/\text{Si}$  interface. (b) Total electric field in the simulated structure. (c) Lateral electric field ( $\text{E}_x$ ) at four different z locations: 20, 40, 80, and 160 nm, respectively. Positive and negative values indicate electric fields aiming to the right or left, respectively. (d) Hole current density under uniform illumination with light of  $\lambda = 800 \,\text{nm}$  and intensity of  $25 \,\mu\text{W/cm}^2$ . Black arrows indicate the direction and magnitude of  $J_{\text{ptotal}}$ . The lower half depicts the total current ( $J_{\text{ptotal}}$ ) at  $z = 20 \,\text{nm}$  along the simulated structure.

combination with conformal alumina coating to enhance the responsivity of Si-based photodiodes.

Numerical simulations were performed to understand the physics controlling the interdigitated structures, and in particular in the outstanding increase of I<sub>ph</sub>, SR, and hence the improvement in EQE. We have self-consistently solved the Poisson and continuity equations in a 2D section of the structures, shown between the vertical dashed lines in Figure 4a, including the GIS and G/Si regions (see Methods). For the simulation, a uniform illumination over the device surface with a wavelength of  $\lambda = 800$  nm and an intensity of 25  $\mu$ W/cm<sup>2</sup> was considered. This wavelength value was selected as it falls in the spectral region where maximum SR and EQE were measured in the experiments (Figure 3). An absorption coefficient of  $\alpha = 10^{3}$  cm<sup>-1</sup> was used in the Si substrate for such a value of  $\lambda$ .<sup>33</sup> Figure 4b shows the calculated electric field (E) in the selected region of the device. The highest values of E are located at the insulating SiO<sub>2</sub> and below the graphene. The electric field is directed toward the surface because of the negative applied bias to the graphene contact and the corresponding curvature of the bands along the z-axis. However, it should be highlighted that a relevant contribution of the lateral electric field  $(E_x)$  appears at the transition from the GIS to the G/Si region. This lateral component of E inside the Si substrate is represented in Figure 4c at different depths from the Si surface, with z = 20 nm (the SiO<sub>2</sub> thickness) indicating the top Si position (G/Si and SiO<sub>2</sub>/Si interfaces). Here, the lateral component of the electric field  $\mathbf{E}_{x}$  contributes only at the transition from GIS to the Schottky region.

Under these conditions, the total current flowing in the device was numerically calculated. Figure 4d presents the hole

current density distribution  $(J_{ptotal})$  in the simulated finger, showing that its highest contribution appears close to the GIS-G/Si junction. The holes photogenerated below the insulator are attracted to the surface by the electric field previously depicted, but as they encounter the barrier created by the insulator (tunneling is not allowed), they move laterally to the nearest G/Si Schottky contact. Black arrows represent the direction and magnitude of the hole current. As a result of the symmetry of the structure, the lateral contribution of  $J_{ptotal}$ in the center is minimum compared with the rest of the finger. The lower part of Figure 4d depicts the total hole current  $(J_{ptotal})$  at z = 20 nm.  $J_{ptotal}$  includes a vertical  $(J_{pz})$  and a lateral component  $(J_{px})$  of the hole current and it is equal to  $J_{ptotal} = \sqrt{J_{px}^2 + J_{pz}^2}$ . An increasing value of the current below the SiO<sub>2</sub> from the center to the edges can be seen, which is equal to the lateral hole current  $(J_{px})$ . The vertical hole current  $(J_{nz})$ , in contrast, is zero below the insulator and at its maximum at the G/Si region closest to the GIS junction (see Figure S5b). This high value of the injected current has its origin in the photogenerated holes below the insulator and represents the current injected into the G/Si contact (measured current). The hole current value then decreases just a few microns outside the GIS region and relaxes toward a constant value at a distance of about  $\Delta \underline{x} = 5 \mu \text{m}$  from the SiO<sub>2</sub> finger edges (lower part of Figures 4d and S5b). This value corresponds to the photogenerated holes below the G/Si contact, and  $\Delta x$  provides an estimation of the width of the G/ Si Schottky contact necessary to extract the photocurrent generated below the SiO<sub>2</sub> finger.

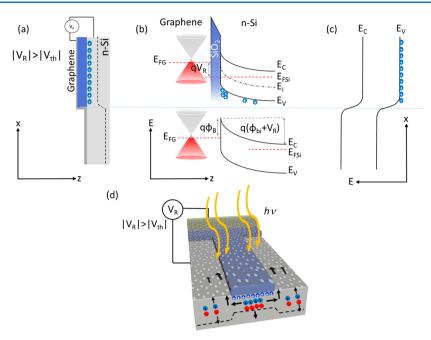


Figure 5. (a) Cross section of the device containing both G/Si and GIS regions at reverse bias above threshold voltage. Dashed line in n-Si substrate represents the limit/edge of the depletion region. (b) Schematic band diagram of the GIS (above) and G/Si (below) junctions along the z-axis in dark conditions. (c) Lateral band diagram along the surface of n-silicon (x-axis), just at the top interface with graphene and SiO<sub>2</sub> in reverse biased conditions.  $E_C$ ,  $E_V$ ,  $E_{FSV}$ ,  $E_V$ 

On the basis of the experimental observations and simulation results, qualitative energy band diagrams of D1 are proposed in Figure 5. The lateral cross section of the device along the length (x) and depth (z) dimensions under reverse applied bias is presented in Figure 5a. The energy band diagrams of the device at the G/Si and GIS regions under dark conditions are shown in Figure 5b. When the reverse bias voltage is increased above  $V_{th}$ , the depletion width of n-Si under graphene widens, whereas an inversion layer is formed in the n-Si substrate under the G/SiO<sub>2</sub> region, which limits the extension of the depletion region below the insulator.<sup>3</sup> The inversion layer causes a difference in the band alignment between the GIS and G/Si junctions along the n-Si substrate in the x-direction (Figure 5c). Consequently, a lateral electric field along the x-direction appears in the transition region between both junctions, driving minority charge carriers (i.e., holes) from the GIS to the G/Si region. Under this condition, when the device is illuminated, the photogenerated holes in the G/Si Schottky junction are extracted directly through the graphene contact. However, in the GIS junction, photogenerated holes need to traverse the distance from the point of generation to the G/Si Schottky junction, because the 20 nm thick oxide rules out the possibility of a significant tunnel current through the SiO<sub>2</sub>. Figure 5d shows a schematic diagram depicting generation, extraction, and collection of photogenerated charges carriers in one of the GIS fingers, according to the proposed band diagrams based on simulation studies.

The numerical study provides strong evidence that charge carriers photogenerated below the  $SiO_2$  fingers first drift to the  $SiO_2/Si$  interface and then diffuse laterally up to the transition region with the G/Si junction where a lateral field accelerates them toward the Schottky contact. Figures 5c and S5a show

that the bands are bent laterally at the transition between junctions and become flat inside the GIS region. This suggests that the GIS regions should be patterned with dimensions such that the photogenerated holes can be extracted effectively and efficiently, thereby making the width of interdigitated GIS region a critical parameter for improved performance of G/Si photodiodes. In this respect, we fabricated devices with varying widths of the GIS regions up to 100  $\mu$ m (see Figure S1). We found that the most efficiently designed structure is device D1 with the highest SR and EQE values, in which the GIS regions have been patterned to a width of 30  $\mu$ m. When the width of the GIS region is increased up to 100  $\mu$ m, the responsivity drops to around 500 mA/W but still exhibits a higher photoresponse when compared to the conventional structure, i.e., device D2. The decrease in responsivity for devices with fingers wider than D1 is explained by the fact that photogenerated carriers in the Si under G/SiO<sub>2</sub> are far away from G/Si junction and thus encounter a weaker or no lateral electric field. This increased the probability for carrier recombination before they can be extracted through the Schottky junction.

We demonstrated enhanced performance of G/Si photo-diodes over a broad range of wavelengths. This was achieved through a simple design of interdigitated regions, where Schottky diodes are in parallel to regions where graphene is separated from the silicon by an insulating oxide. This smart contact design with graphene as a transparent electrode enables the efficient extraction of photogenerated charge carriers and resulted in a maximum EQE of 98% and responsivity of 635 mA/W. Simulations confirmed the formation of an inversion layer under the insulated regions, which serve to passivate defects and limit recombination of photogenerated carriers. The extraction of minority carriers,

once the inversion layer is created, is efficiently enhanced by the stronger lateral electric fields derived by defining the G/Si contact geometry. Given the simple planar geometry of the fabricated devices and the availability of large-area CVD-grown graphene, the proposed fabrication process can easily be integrated into conventional semiconductor technology. The proposed interdigitated contact strategy can be further extended to other 2D–3D and 2D–2D heterostructures where graphene is used as one of the electrodes, and semiconductors other than Si are used.

#### METHODS

Device Fabrication. A phosphorus-doped Si wafer with a nominal doping concentration of  $2 \times 10^{15}$  cm<sup>-3</sup> was used as the substrate. A thermal oxidation process yielded 20 nm of high-quality SiO<sub>2</sub> on the silicon surface. For chip fabrication, the wafer was diced into  $20 \times 20 \text{ mm}^2$  samples. The oxide was etched with hydrofluoric acid (HF) after a first standard UV photolithography step in order to expose the n-Si substrate. The contact metal electrodes were defined by a second photolithography step followed by sputtering of 15 nm chromium (Cr) and 85 nm nickel (Ni) and a liftoff process. The metal electrodes were deposited immediately after the native oxide removal, ensuring the formation of ohmic contacts. Large-area graphene was grown on a copper foil in a NanoCVD (Moorfield, UK) rapid thermal processing tool. To transfer graphene films onto prepatterned substrates, ~7 mm<sup>2</sup> pieces of graphene-coated Cu foil were spin-coated with poly methyl methacrylate (PMMA) and baked on a hot plate at 85 °C for 5 min. A wet etch process was used to remove the polymer-supported graphene films from the copper surface. Iron(III) chloride (FeCl<sub>3</sub>) was used as an etchant to remove the copper. The native SiO<sub>2</sub> on the n-Si substrates was removed by HF prior to the graphene transfer to achieve an electrical contact between graphene and n-Si substrate. Afterward, the chip was baked at 180 °C for 35 min and then thoroughly immersed into acetone for 1 h, followed by cleaning with isopropanol and drying. Then, a last photolithography step was performed, followed by oxygen plasma etching of graphene to define the graphene areas. For packaging and wire-bonding, the patterned chip was diced into the  $6 \times 6$  mm<sup>2</sup> samples. Before the dicing step, the chip was spin-coated with AZ 5214 E photoresist to protect the photodiodes during the dicing process. This layer was removed after dicing by immersion in acetone. Finally, the chips were glued into a chip package, and the devices were wire-bonded.

**Electrical Characterization.** The chip package was inserted into a socket located inside a home-built chamber connected to a Keithley semiconductor analyzer (SCS4200) for electrical measurements under ambient conditions. The voltage for all devices was swept from 0 to +2 V for forward  $(V_F)$  and from 0 to -2 V for reverse  $(V_R)$  biasing. A white-light source (LED lamp) with a dimmer to control the light intensity was used to confirm that the diodes are generally sensitive to light. The LED-light spectrum can be found in Figure S6. The intensity of the light source was measured by a CA 2 laboratory thermopile.

**Optical Characterization.** The spectral response (SR) of the photodetectors was measured by comparing them to a calibrated Si reference diode using a lock-in technique (see Figure S7). A tungsten—halogen lamp with a wavelength ranging from 300 to 2000 nm was used as the light source. Specific wavelengths were selected by a monochromator. The

intensity of the light beam was modulated by a chopper with a frequency of 17 Hz. The current was measured by preamplifiers and lock-in amplifiers with 300 ms integration time and 0.4 Hz bandwidth at 17 Hz chopper frequency for detection of low currents down to 10 pA.

Scanning Photocurrent Measurements. Scanning photocurrent measurements were performed using a Witec Alpha300 R confocal microscope equipped with a piezoelectric scanning stage. The microscope was coupled to a 532 nm wavelength laser to generate spatially resolved photocurrent, which is converted into a voltage signal using a current preamplifier and is recorded by a lock-in amplifier.

**Numerical Simulation.** Simulations of the structures under investigation have been carried out by self-consistently solving 2D electrostatic and transport equations. In particular, we solve

• Poisson's equation

$$\nabla \cdot (\varepsilon \nabla \psi) = -q(p - n + N_D^+ - N_A^-)$$

where  $\varepsilon$  is the dielectric constant,  $\psi$  is the electrostatic potential, q is the electron charge, p(n) corresponds to the hole (electron) density, and  $N_D^+$  ( $N_A^-$ ) corresponds to the ionized donor (acceptor) doping density.

• Carrier continuity equation

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \vec{J}_n + G_n - R_n; \frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \vec{J}_p + G_p - R_p$$

where  $G_n\left(G_p\right)$  and  $R_n\left(R_p\right)$  are the electron (hole) generation and recombination terms, respectively.  $J_n$  and  $J_p$  are the electron and hole drift—diffusion equations expressed as

$$\vec{J_n} = qn\mu_n \nabla \psi + qD_n \nabla \mathbf{n}; \vec{J_p} = qp\mu_p \nabla \psi - qD_p \nabla \mathbf{p}$$

where  $\mu_n$  ( $\mu_p$ ) is the electron (hole) mobility, and  $D_n$  ( $D_p$ ) is the electron (hole) diffusion coefficient. Stationary conditions have been considered for this work.

Carrier recombination is expressed as

$$R_{SRH} = \frac{np - n_i^2}{\tau_n(n + n_i^2) + \tau_p(p + p_i^2)}$$

with  $\tau_n$  ( $\tau_p$ ) being the electron (hole) lifetime, and  $n_i$  ( $p_i$ ) being the intrinsic electron (hole) concentration.  $\tau_n = \tau_p$  was assumed in this work.

Generation of electron—hole pairs is produced by light absorption that follows Beer—Lambert's law

$$G_n = G_p = \frac{P_{\text{opt}}}{E_{\text{ph}}} \alpha e^{-\alpha x}$$

where  $P_{\rm opt}$  is the applied light power at the surface in W/cm²,  $E_{ph}=\frac{hc}{\lambda}$  is the photon energy, and  $\alpha$  is the absorption coefficient.

The current injection at the Schottky contacts has been modeled as

$$J_n = -qS_n(n - n_0); J_p = qS_p(p - p_0)$$

where  $S_n$  ( $S_p$ ) is the electron (hole) surface recombination velocity, and  $n_0$  ( $p_0$ ) is the electron (hole) density at the interface at equilibrium.  $S_n$  ( $S_p$ ) describes the electron (hole)-transfer rate between the Si substrate and the graphene

contact. The value of this parameter is affected by the quality of both materials, the presence of impurities, or an insulator barrier at the interface produced by the growing of a native  $SiO_2$ .

#### ASSOCIATED CONTENT

# S Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsphotonics.8b00951.

Figure S1: Geometry of the devices with a finger patterned SiO<sub>2</sub>-Si substrate, compared to the control device D2. Spectral response and scanning photocurrent measurements of the devices with varying widths of the GIS regions. Figure S2: A detailed discussion on extraction of diode parameters from the I-V measurements. Figure S3: SPC of D1, which shows a significant photocurrent at low reverse biases, indicating its application as low-power photodiodes. Figure S4: I-V curve and SPC map of D1 over a time period of six months showing consistent current levels, indicating that performance of the devices does not degrade with time. Figure S5: Energy band diagram and  $J_{nz}$  along the simulated structure. Figure S6: Spectral power distribution of white LED lamp used for I-V measurements under illumination. Figure S7: Schematic of SR setup. Details of the procedures for calculating the photoresponsivity of the photodiodes in the SR setup. Table S1: Responsivity of G/Si photodiodes reported in the literature compared to responsivity of G/Si photodiodes presented this work (PDF)

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Notes

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