Neuromorphic and logic circuit simulation using in-house fabricated GrAphene-based MEmristor (GAME)

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1. Introduction

Two-dimensional (2D) graphene-based materials are progressively occupying the central stage for *More Moore* and *More than Moore* applications. Implementing memristive devices based on 2D graphene could be a key enabler for efficient neuromorphic and non-von Neumann computing architectures. However, the high processing cost and routine use of rigid substrate limits the experimental exploration in this field to high-tech facilities. Here, we use a cost-effective, one-step process using a commercial laser to fabricate GrAphene-based MEmristors (GAMEs) on a flexible substrate [1], making more accessible the fabrication, and thus widening and boosting the experimental assessment on the potential of the technology. The electrical characterization shows non-volatile and stable resistive switching characteristics. A compact model is extracted based on the experimental data, and SPICE simulation of the Pavlovian conditioning and logic circuits shows the excellent suitability of the GAME as a synaptic element in neuromorphic circuits and non-von Neumann computing.

2. Methodology

Figure 1a shows a schematic representation of the fabrication process. A laser is used to engrave a flexible substrate (Dupont™Kapton®), producing reduced graphene-oxide regions and eventually memristive performance. Optical microscopic images of a GAME array, before and after depositing the metallic ink, are shown in Fig. 1b. Electrical characterization is performed using an EverBeing® C-4 Probe Station with Keithley® 4200A-SCS Parameter Analyzer. To demonstrate the potential application of the GAME, circuit simulations are performed. VTEAM compact model [2] is extracted using the experimental data, and the model parameter shown in Tab. 1 feds a SPICE program to simulate different circuits.

3. Results and Discussion

The current-voltage (I-V) characteristics of the GAMEs are shown in Fig.2a. Two different GAMEs, D1 and D2, are characterized for several I-V cycles. Note that data shown in Fig. 2a represent one I-V sweep for each device. The GAME features forming free, non-volatile bipolar switching. Fig. 2b shows the result of the VTEAM compact model matched to the experimental data. Two sets of parameters are extracted, one per device (D1 and D2), and the resulting I-V characteristics shows a good fit with the measurements.

Next, Memristor-Aided logic (MAGIC) circuits are simulated [3], as shown in Fig 3 corresponds to both AND-OR gates. Here, two GAMEs , with previously memorized data (R_{in1} and R_{in2}), act as the input. The output GAME can be set in specific conditions to resemble the functional output (i_{out}). Fig. 3 shows i_{out} for the AND-OR functions, for different combinations of R_{in1} and R_{in2}.

A simple circuit to mimic Pavlovian conditioning is also demonstrated [4]. Pavlovian conditioning deals with the acquisition of a conditioned response to a particular stimulus. Here, a simple circuit that mimics Pavlovian conditioning is simulated based on GAME. Fig. 4a shows the application of the input V_{bell} representing the bell, with the GAME acting as the synaptic element, where the post-synaptic response V_{out} is higher than the spiking threshold of a neuron (set here as 10 mV). Fig. 4b shows the network training, where the input voltage V_{bell} is interlaced with a higher amplitude V_{food}, gradually reducing the post-synaptic signal. This corresponds to the change of the resistive state of the GAME on the application of the input pulses, resembling the synaptic plasticity. The subsequent application of V_{bell} (Fig.4c) results in a post-synaptic V_{out} much lower than the threshold, which will not cause the spiking of the post-synaptic neuron.

4. Conclusions

A graphene-based memristor was fabricated on a flexible substrate using a low cost process. The electrical characterization showed non-volatile bipolar switching. The VTEAM compact model was extracted based on the experimental data and the SPICE simulation of logic gates and Pavlovian conditioning was demonstrated. The work proves the suitability of the memristor for neuromorphic and non-von Neumann computing applications.

Acknowledgments

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References

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[3] S. Kvatinsky et al., IEEE TCAS II, vol. 61, (2014).

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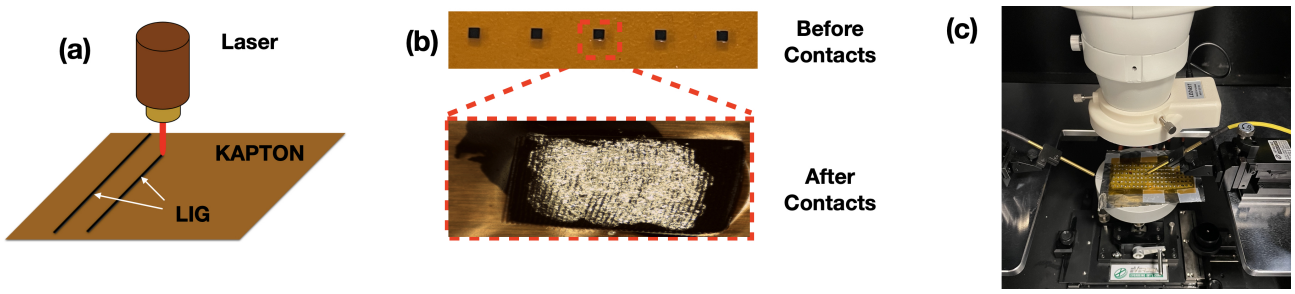

Fig. 1: (a) Schematic of the engraving process. (b) optical microscopy image of the engraved GrAphene-based MEmristor (GAME) before and after top contact and (c) the test setup for electrical measurements.

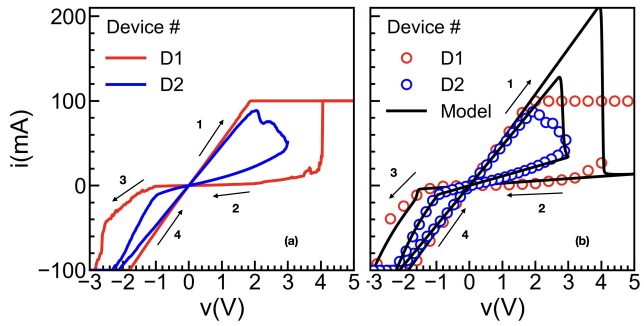

Fig. 2: Experimental Current-Voltage (I-V) characteristics of two GAME devices D1 and D2 and (b) extracted compact model matched to the experimental data.

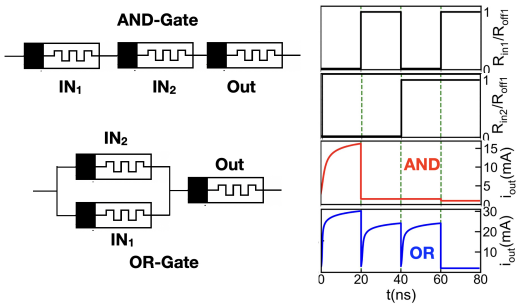

Fig. 3: (a) Memristor-aided logic (MAGIC) circuit. (b) Demonstration of AND-OR logic.

GAME	R_{LRS} (Ω)	R_{HRS} (Ω)	K_{on}	K_{off}	α_{on}	α_{off}	v_{on}	v_{off}	a_{on}	a_{off}
D1	18.56	1000.04	-0.5	0.05	17.20	115	-1.01	2.1	3.79e-06	4.7e-06
D2	21.16	690.16	-17.56	460.26	132.63	49.32	-0.48	1.66	5.66e-06	1e-07

Table 1: Parameter set of VTEAM model matched to the experimental GAME D1 and D2

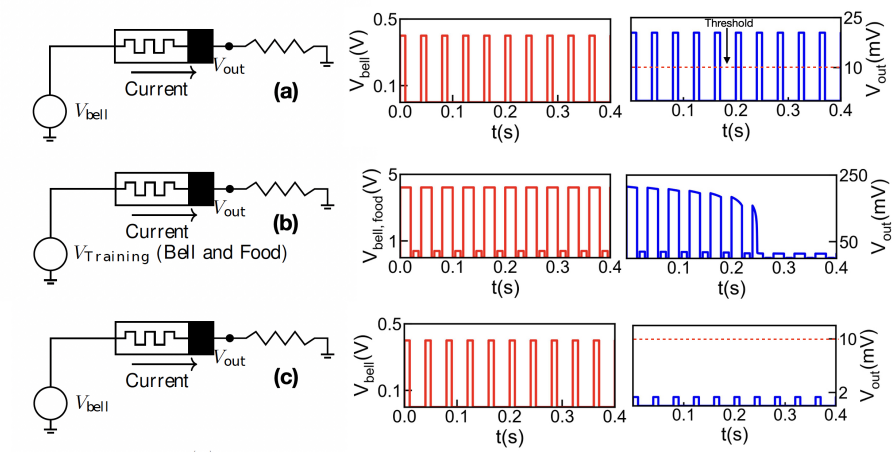

Fig. 4: Neuromorphic circuit mimicking Pavlovian conditioning. (a) Untrained post-synaptic output, higher than neuron spiking threshold; (b) training of the synapse by interlacing food signal; (c) post-synaptic output of the trained network with lower than spiking threshold output.