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Design, Simulation and Electrical Characterization of A2RAM Memory Cells

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Declaration of Authorship

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Guarantee by signing this thesis:

that the research work contained in the present report, entitled ***Design, Simulation and Electrical Characterization of A2RAM Memory Cells***, has been performed under the full guidance of the Ph.D supervisors and, as far as our knowledge reaches, during the work, it has been respected the rights of others authors to be cited, when their publications or their results have been used.

Granada, 23rd February, 2014.

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To my parents and my brothers...

"Doubt is uncomfortable, certainty is ridiculous."

Voltaire (1694 - 1778)

"Any sufficiently advanced technology is indistinguishable from magic."

Arthur C. Clarke (1917 - 2008)

Abstract

Facultad de Ciencias
Departamento de Electrónica y Tecnología de Computadores

Doctor degree

Design, Simulation and Electrical Characterization of A2RAM Memory Cells

by Carlos Navarro Moral

The main purpose of this study was to investigate the novel **A2RAM** (*Advanced 2 Random Access Memory*) cell as a possible **FB-DRAM candidate**. The research activity included the simulation, fabrication and electrical characterization of these memory cells. To do so, a basic overview of the DRAM state-of-the-art is initially presented with different technological alternatives. Once the basics ideas are explained, a detailed approach to the initial A-RAM and evolved A2RAM cells is featured. To overcome the main study of the memory cell, both TCAD simulations using Silvaco® software and rigorous experimental measurements with high-end characterization equipment have been performed. Finally, the main results and possible future steps are examined along this report.

The study developed in this work has been focused on the feasibility and advanced electrical characterization of this multi-body memory cell, allowing its implementation in typical bulk and extremely thin SOI wafers. The simulated and experimental results indicate that with its low-power operation and electrical properties, the A2RAM cell is an attractive and potential alternative for embedded DRAM applications, exhibiting high current ratio between states and reasonable retention time, superior to other proposed floating-body memories, even with shorter channel length and thinner silicon films.

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Abbreviations

1D	**O**ne **D**imensional
1T-DRAM	**S**ingle **T**ransistor **DRAM**
1T+1C-DRAM	**O**ne **T**ransistor **O**ne **C**apacitor **DRAM**
2D	**T**wo **D**imensional
3D	**T**hree **D**imensional
AC	**A**lternating **C**urrent
A-RAM	**A**dvanced **RAM**
A2RAM	**A**dvanced **2 RAM**
BEDO	**B**urst **E**xtended **D**ata **O**utput
BESOI	**B**onded **E**tched-back **SOI**
BG	**B**ack-**G**ate
BJT	**B**ipolar **J**unction **T**ransistor
BL	**B**it **L**ine
BOX	**B**uried **OX**ide
BR	**B**lue **R**ay
BtBT	**B**and **t**o **B**and **T**unneling
CAS	**C**olumn **A**ddress **S**trobe
CEA	**C**ommisariat l'**É**nergie **A**tomique
CET	**C**apacitance **E**quivalent **T**hickness
CD	**C**ompact **D**isc

CDRAM	**C**ache **DRAM**
CMOS	**C**omplementary **MOS**
CMP	**C**hemical **M**echanical **P**olishing
CNM	**C**entro **N**acional **M**icroelectrónica
CLK	**CL**oc**K** digital signal
CPU	**C**entral **P**rocessing **U**nit
CS	**C**hip **S**elect
CV	**C**apacitance **V**oltage
CVD	**C**hemical **V**apor **D**eposition
DC	**D**irect **C**urrent
DG	**D**ouble **G**ate
DIBL	**D**rain **I**nduced **B**arrier **L**owering
DRAM	**D**ynamic **RAM**
DDR	**D**ual **D**ata **R**ate
DPW	**D**ies **P**er **W**afer
EEPROM	**E**lectrically **E**rasable **P**rogrammable **ROM**
EDA	**E**lectronic **D**esign **A**utomation
EDO	**E**xtended **D**ata **O**utput
EDRAM	**E**nhanced **RAM**
ELTRAN	**E**pitaxial **L**ayer **TRAN**sfer
ELO	**E**pitaxial **L**ateral **O**vergrowth
EHP	**E**lectron **H**ole **P**air
EOT	**E**quivalent **O**xide **T**hickness
EPROM	**E**rasable **P**rogrammable **ROM**
ESD	**E**levated **S**ource **D**rain
ESDRAM	**E**nhanced **SDRAM**
ET	**E**xtremely **T**hin
FB	**F**loating-**B**ody
FBE	**F**loating-**B**ody **E**ffect

FD	**F**ully **D**epleted
FET	**F**ield **E**ffect **T**ransistor
FG	**F**ront-**G**ate
FPM	**F**ast **P**age **M**ode
FeRAM	**Fe**rroelectric **RAM**
GIDL	**G**ate **I**nduced **D**rain **L**eakage
GP	**G**round **P**lane
H	**H**old memory operation
HDD	**H**ard **D**isk **D**rive
IC	**I**ntegrated **C**ircuit
II	**I**mpact **I**onization
L	**L**ength
LETI	**L**aboratoire **E**lectronique **T**echnologies **I**nformation
LOCOS	**LOC**al **O**xidation **S**ilicon
LSPE	**L**ateral **S**olid **P**hase **E**pitaxy
M	**M**osfet
MCCM	**M**ultistable **C**harge **C**ontrolled **M**emory
MLC	**M**ulti **L**evel **C**ell
MOS	**M**etal **O**xide **S**emiconductor
MOSFET	**MOS F**ield **E**ffect **T**ransistor
MOX	**M**iddle **OX**ide
MR	**M**agneto**R**esistance
MRAM	**M**ulti Bank **RAM**
MSD	**M**eta **S**table **D**ip
NMOS	**N**-channel **MOS**
nRAM	**n**ext Generation **RAM**
NVRAM	**N**on **V**olatile **RAM**
PC	**P**ersonal **C**omputer
PD	**P**artially **D**epleted

PMOS	**P**-channel **MOS**
PN	**P**-type **N**-type
PROM	**P**rogrammable **ROM**
PSDRAM	**P**seudo **S**tatic **RAM**
QW	**Q**uantum **W**ell
R	**R**ead memory operation
RAM	**R**andom **A**ccess **M**emory
RAS	**R**ow **A**ddress **S**trobe
RDF	**R**andom **D**opant **F**luctuations
RDRAM	**R**ambus **DRAM**
RIE	**R**eactive **I**on **E**tching
ROM	**R**ead **O**nly **M**emory
RWL	**R**ead **W**ord **L**ine
RSD	**R**aised **S**ource **D**rain
RSU	**R**emote-**S**ense **U**nit
SCE	**S**hort **C**hannel **E**ffects
S/D	**S**ource/ **D**rain
SDR	**S**ingle **D**ata **R**ate
SDRAM	**S**ynchronous **DRAM**
SEG	**S**elective **E**pitaxial **G**rowth
SG	**S**ingle **G**ate
SGRAM	**S**ynchronous **G**raphic **DRAM**
SGVC	**S**urrounding **G**ate **V**ertical **C**hannel
SHE	**S**elf-**H**eating **E**ffect
SIMOX	**S**eparation **IM**plantation **O**xygen
SLC	**S**ingle **L**evel **C**ell
SLDRAM	**S**ync **L**ink **DRAM**
SMU	**S**ource **M**onitor **U**nit
SPICE	**S**imulation **P**rogram **I**ntegrated **C**ircuit **E**mphasis

SR	**S**can **R**ate
SR	**S**urface **R**oughness
SRAM	**S**tatic **RAM**
SRE	**S**eries **R**esistance **E**ffect
SRH	**S**hockley **R**ead **H**all
SS	**S**ubthreshold **S**wing
SSM	**S**olid **S**tate **M**emories
SOI	**S**ilicon **O**n **I**nsulator
SON	**S**ilicon **O**n **N**othing
SOS	**S**ilicon **O**n **S**aphire
STI	**S**hallow **T**rench **I**solation
Th	**Th**reshold
TCAD	**T**echnology **C**omputer **A**ided **D**esign
TEM	**T**ransmission **E**lectron **M**icroscopy
TFET	**T**unnel **FET**
TT	**T**win **T**ransistor
UMC	**U**niversal **M**obility **C**urve
UT	**U**ltra-**T**hin
UTBB	**U**ltra-**T**hin **B**ody and **B**OX
UTSOI	**U**ltra-**T**hin **SOI**
UV	**U**ltra**V**iolet
VLSI	**V**ery **L**arge **S**cale **I**ntegration
VRAM	**V**ideo **RAM**
W	**W**idth
W_0	**W**rite state '0' memory operation (erase)
W_1	**W**rite state '1' memory operation
WE	**W**rite **E**nable
WL	**W**ord **L**ine
WRAM	**W**indow **RAM**

WWL	**W**rite **W**ord **L**ine
ZMR	**Z**one **M**elting **R**ecrystallization
ZRAM	**Z**ero Capacitor **RAM**
Z^2**-FET**	**Z**ero SS **Z**ero II **FET**

Physical Constants

Boltzmann's constant	k_B	=	$1.380\ 648 \times 10^{-23}\ J/k$
Electron charge	q	=	$1.602\ 176 \times 10^{-19}\ C$
Free electron rest mass	m_0	=	$9.109\ 382 \times 10^{-31}\ kg$
Permittivity of vacuum free space	ϵ_0	=	$8.854\ 187 \times 10^{-12}\ F/m$
Relative permittivity BST	ϵ_{BST}	=	$320 - 1250$
Relative permittivity HfO_2	ϵ_{HfO_2}	=	$22 - 40$
Relative permittivity Si	ϵ_{Si}	=	11.9
Relative permittivity SiO_2	ϵ_{SiO_2}	=	3.9
Room temperature	T_R	=	$300\ k$
Planck's constant	h	=	$6.626\ 069 \times 10^{-34}\ J \cdot s$
Reduced Planck's constant	$\hbar$	=	$1.054\ 571 \times 10^{-34}\ J \cdot s$
Speed of light	c	=	$2.997\ 924 \times 10^{8}\ m/s$

Symbols

A	Area	cm^2
$\overrightarrow{B}$	Magnetic field	T
C	Capacitance	F/cm^2
C_{BL}	DRAM bit line parasite capacitance	F
C_{BOX}	BOX capacitance	F/cm^2
C_{GC}	Gate to channel capacitance	F/cm^2
C_{it}	Interface density states capacitance	F/cm^2
$C_{n,p}$	Auger recombination coefficient	cm^6/s
C_{ox}	Front oxide capacitance	F/cm^2
C_s	DRAM Storage capacitance	F
D_{it}	Density of interface states	$cm^{-2} \cdot eV^{-1}$
D_{Im}	Implantation dose	cm^{-2}
$D_{n,p}$	Electron or hole diffusion coefficients	cm^2/s
$\overrightarrow{E}$	Electric field	V/cm
E_{Break}	Breakdown electric field	V/cm
E_c	Conduction band edge	eV
E_v	Valence band edge	eV
E_{eff}	Effective electric field	V/cm
E_F	Equilibrium Fermi level	eV
E_g	Band gap energy ($E_c - E_v$)	eV

E_i	Intrinsic Fermi energy level	eV
E_{Im}	Implantation Energy	eV
$\overrightarrow{E_z}$	Vertical electric field	V/cm
EOT	Equivalent Oxide Thickness	cm
$\overrightarrow{F}$	Force	N
G_{BtBT}	Generation by BtBT	$1/cm^2 \cdot s$
g_m	Transconductance	A/V
k	Mobility temperature attenuation factor	-
I	Current	A
I_0	'0' State current	A
I_1	'1' State current	A
I_B	Base current	A
I_C	Collector current	A
I_{DS}	Drain to source current	A
$\Delta I_{1-0}(t)$	Memory cell current margin	A
$\Delta I_{1/0}(t)$	Memory cell current ratio	A/A
I_E	Emitter current	A
I_G	Gate current	A
I_{Off}	OFF state MOSFET current	A
I_{On}	ON state MOSFET current	A
I_s	Diode saturation current	A
$I_{Sensitivity}$	Sense amplifier current sensitivity	A
m	Slope	-
m_0	Free electron rest mass	kg
$m^*_{e/h}$	Effective mass for electron/hole	m_0
n	Electron concentration in E_c	cm^{-3}
n_i	Intrinsic concentration of carriers	cm^{-3}
n_o	Equilibrium concentration of electrons	cm^{-3}
N_A	Concentration of ionized acceptors	cm^{-3}

N_c	Effective density of states in E_c	cm^{-3}
N_D	Concentration of ionized donors	cm^{-3}
N_i	Inversion concentration of carriers	cm^{-3}
$N_{N-Bridge}$	A2RAM N-Bridge donor concentration	cm^{-3}
N_v	Effective density of states in E_v	cm^{-3}
L	Device length	cm
p	Hole concentration in E_v	cm^{-3}
p_i	Intrinsic concentration of holes	cm^{-3}
p_o	Equilibrium concentration of holes	cm^{-3}
p_z	Vertical inversion charge profile	cm^{-3}
Q	Charge	C/cm^2
Q_d	Depletion charge	C/cm^2
Q_i	Inversion charge	C/cm^2
R	Resistance	Ω
R_H	Hall coefficient	cm^3/C
R_{RSH}	Shockley-Read-Hall recombination rate	$1/cm^3 \cdot s$
SR	Scan rate	V/s
SS	Subthreshold swing	mV/dec
t	Thickness, Time	cm, s
t_{BOX}	Buried oxide thickness	cm
t_{MOX}	ARAM middle oxide thickness	cm
$t_{N-Bridge}$	A2RAM N-Bridge thickness	cm
t_{ox}	Front oxide thickness	cm
t_{ret}	Retention time	s
t_{Si}	Silicon film thickness	cm
t_{Si-P}	A2RAM top P-body thickness	cm
t^*_{Si}	Critical silicon film thickness	cm
t_{Wafer}	Wafer total thickness	cm
T	Temperature	k

$\overrightarrow{v}$	Velocity	m/s
V	Voltage, Bias	V
V_{BG}	Back-gate voltage referred to source	V
V_{BL}	DRAM Bit line voltage	V
V_{BS}	Body voltage referred to source	V
V_{DS}	Drain to source voltage	V
V_{DD}	Power supply voltage	V
V_{FB}	Flatband voltage	V
V_{FG}	Front-gate voltage referred to source	V
V_{GS}	Generic gate to source voltage	V
V_H	Hall voltage	V
V_{High}	Logic highest voltage	V
V_{Low}	Logic lowest voltage	V
V_{Pre}	DRAM pre-charge bit line voltage	V
V_{Th}	Threshold voltage	V
V_{WL}	DRAM word line voltage	V
W	Device width	cm
x_d	Junction depletion depth	cm
α	Coupling factor	-
ϵ_0	Vacuum free space permittivity	F/cm
ϵ	Relative dielectric permittivity	F/cm
η	Weighting constant for Q_i and Q_d	F/cm
θ	Mobility attenuation coefficient	V^{-1}
θ_0	Intrinsic mobility attenuation coefficient	V^{-1}
θ_{Im}	Implantation angle	$^\circ$
λ	Threshold voltage V_{DS} bias dependence	V/V
μ	Carrier mobility	$cm^2/V \cdot s$
μ_0	Low field carrier mobility	$cm^2/V \cdot s$

μ_{AC}	Mobility by acoustic phonons	$cm^2/V \cdot s$
μ_b	Mobility by optical intervalley phonons	$cm^2/V \cdot s$
μ_{eff}	Effective carrier mobility	$cm^2/V \cdot s$
μ_{FE}	Field-Effect carrier mobility	$cm^2/V \cdot s$
μ_{sr}	Mobility by surface roughness	$cm^2/V \cdot s$
μ_T	Final mobility (Matthiessen rule)	$cm^2/V \cdot s$
ρ	Charge volume density	C/cm^{-3}
ϕ	Potential	V
ϕ_F	Intrinsic to Fermi level potential	V
ϕ_S	Surface potential	V
Φ_X	Work-function potential of material X	V
Φ_{MS}	Metal-Semiconductor work-function	V
$\tau_{n,p}$	Electron/hole lifetime	s

Objectives

The situation of some widespread technologies related to the semiconductor industry that have been extensively used for many years are now facing a period where they are being questioned. Attending to the semiconductor memories, the scaling problems turn to be the main threat to Flash, SRAM, DRAM... In case of the DRAM, the **scaling of the capacitor** is the most limiting factor to continue with the traditional 1T+1C DRAM cell. A natural approach would be to avoid the use of this storage node, overcoming its scaling drawbacks, and use instead another element able to retain the information and more suitable for the required aggressive scaling. A better choice proves to be the use of a transistor. Firstly, because it is already demonstrated its feasibility beyond the 22 nm node and, secondly, because the memory cells are already using it so no extra element (and therefore area) would be required. So, in order to overcome all the scaling problems that 1T+1C DRAM cells suffer, a new type of memory cell based has been proposed where no additional capacitor is needed. Some of these cells, named ***1T-DRAM***, are mostly based on the use of the **SOI** (*Silicon On Insulator*) technology to benefit from the **floating-body** effects (**FB-DRAM**).

The **objective of this work is then to study a specific FB-DRAM candidate, the Advanced 2 RAM cell**, and verify if it features good

memory characteristics and solve the scaling problems that the traditional 1T+1C DRAM cell or others FB-DRAM designs cannot. In particular, the following questions will be answered in this work:

1. Can the Advanced 2 RAM cell theoretical concept be manufactured?
2. Does its performance allow this type of cell to be competitive?
3. Does this novel floating-body DRAM have any real contribution or innovation to the technological framework regarding dynamic memories today?

Methodology

Once the objectives have been established, a short review of the methodology followed in this report is discussed. In order to explore the Advanced 2 RAM cell, the following procedure has been followed:

- An introduction of solid state memories is initially carried out in Chapter 1. The traditional cell composed by one transistor + one capacitor is analyzed and its scaling problems are highlighted. This section provides the background and motivation of moving to new DRAM design concepts such as the 1T-DRAM.
- In Chapter 2 the main FB-DRAM candidates based on SOI technology and composed by a single transistor are summarized. Their operation principles, advantages and drawbacks are commented. First multi-body architecture FB-DRAMs like the A-RAM are introduced together with their scaling benefits.
- The Advanced 2 RAM cell fundamentals are initially described in Chapter 3. The fabrication process on bulk and SOI substrates is investigated and the assets and detriments that this cell features are discussed.
- Once the basis of the A2RAM are settled, advanced TCAD numerical simulations are performed using Silvaco® in Chapter 4. Simulations

results validate the theoretical concept outlined before and also serve as a reference for fabrication.

- Chapter 5 stands as the first experimental proof of concept of A2RAM in bulk and SOI wafers. Memory parameters extraction is carried out to determine the goodness and advantages of each substrate.

- Ultimate A2RAM SOI samples are analyzed in Chapter 6. Main static parameters are electrically characterized using state-of-the-art ET-SOI MOSFETs as benchmark to review the A2RAM properties as switch. Memory operation is verified with time dependent measurements to show the feasibility of functional scaled A2RAM cells.

- Finally, the main experimental results along the work are presented together with an analysis of the objectives established at the beginning of the report.

Part I

Floating-Body Memories

Chapter 1

Introduction to Solid State Memories

The constant evolution of information systems is deeply related to the possibility of managing large amounts of data. Along the last decades, many different systems and techniques have emerged with the sole purpose of improving this management, either by reducing the amount of data using compression techniques, using error detecting and correcting codes, increasing the transmission speed or simply improving the storage capacity. This chapter outlines the main features of solid state memories focusing mostly on one of the most widely used storage technologies in recent years, the Dynamic Random Access Memories.

1.1. Motivation of Memories

Today electronics surround everything, it is present everywhere; at home, with multimedia equipments as television, home cinema or all the electrical appliances; at work, with data systems and computers and even during free time, with smartphones, tablets, video games... The average number of electronic devices or equipments per person has risen incessantly. Moreover, the technology behind most of these devices has suffered a giant evolution demanding more and more resources in order to provide the highest possible performance. Now, the technology carried in the pocket has more computing power than the one employed during the *Apollo 11 Mission*, the first spaceflight that landed a human on the Moon on July 20th, 1969. This gives an idea of the extreme progress that electronics has overcome in all its dimensions during the last four decades.

The main promoters of electronic market have been: i) the increase in system requirements and ii) number of devices, iii) the voracious hunger of end-users to buy every new product and iv) the planned obsolescence (limited useful life by default), see Figure 1.1.

Since the vast majority of electronic equipments require some type of storage circuit for their proper operation, then the **memory becomes an essential module in any given design**. Scalability, bandwidth, access speed, power waste, endurance... they all turn to be key points that may act as a bottleneck limiting the performance of the system. The pursuit of an universal memory cell that deals with most of these constraints at the same time has become one of the holy grails that rest to be discovered. Meanwhile, the optimization of the already available designs and few revolutionary novel structures allow the industry to keep going.

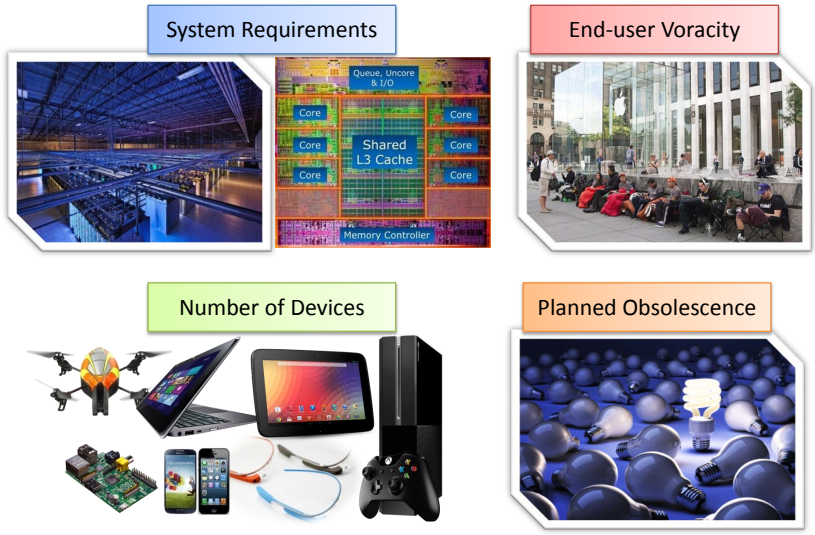


FIGURE 1.1: Main promoters of electronics today.

1.2. Different Types of Memories

Memories are all those circuits which are able to store certain volume of data for, at least, a short period of time. Regarding for example a system like a PC (*Personal Computer*), these elements are one of the most important pillars together with the CPU (*Central Processing Unit*) because they implement fundamentals blocks of *Von Neumann Architecture* model [Neu45], the most widely used since 1945.

Several boughs can be clearly differentiated when referring to a memory. A separation may be done based on the storage capacity, the retention time, the transfer speed... Historically, the split in different types used to be made as a function of whether the memory maintained its content unaltered even in the absence of external power or not. **If the data is saved even without power, the memory is called Non-Volatile**. Some examples of non-volatile memories are the non rewritable CD (*Compact Disc*), the HDD (*Hard Disk*

Drive), the punched paper cards... On the other hand, **if the memory loses**

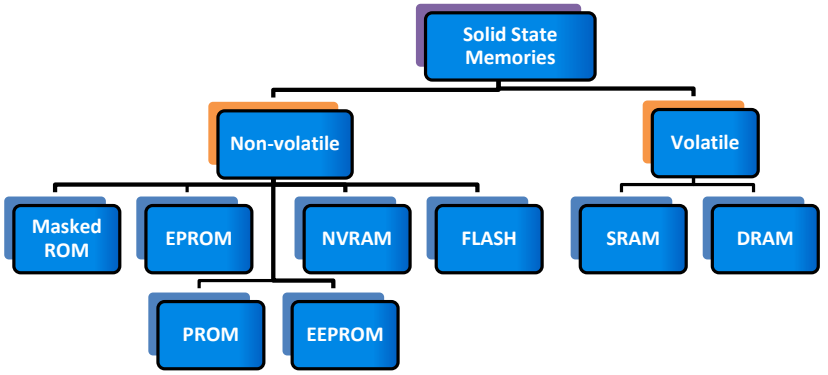


FIGURE 1.2: Types of solid state memories [Bar99].

A closer look into the main properties, together with the advantages and disadvantages, will be presented for every memory type in the following sections [Bar99].

1.2.1. Non-Volatile Memories

The characteristic that non-volatile memories share in common is the **ability to save indefinitely the information, even with a power failure**. First reports of these SSM memories were devices with a pre-programmed set of instructions. Their content should be specified before manufacturing so that during the fabrication process, transistors involved will be rightly

arranged according to the information to store. This type of memory is still in use nowadays under the name of **masked-ROM** and is especially cheap in mass production. **PROM** memories (*Programmable ROM*) appear one step ahead. They are sold without any information stored. To be written, they must be connected first to a programmer which is responsible for applying the appropriate bias pattern in order to modify the content of each memory cell individually. Once the memory chip is programmed and the information stored, it can not be rewritten and it behaves in all senses like a masked-ROM. If any change is desired regarding the information stored, it is mandatory to resort to a new PROM chip. Like PROM, **EPROM** (*Erasable and Programmable ROM*) memories need the use of a programmer for storing data, but the difference is that in this case a change in the stored data can be performed allowing to erase and write repeatedly. To erase the information, the device must be exposed to a strong UV (*UltraViolet*) light. To allow the radiation reach the silicon chip, the device presents a small window, see Figure 1.3. Photons of the UV light cause ionization within the silicon oxide dissipating the charge stored in a floating gate. This process resets the content in the memory chip to the initial state. Although the price of EPROM chips is larger compared to masked-ROM or PROM, their ability to be rewritten usually makes them desirable for certain applications. **EEPROM** (*Electrically Erasable and Programmable ROM*) are a natural evolution from the EPROM. They have the same structure but the reset of the data is much simpler and faster. Erasing can be carried out by applying an specific bias condition instead of using UV radiation.

On their side, **Flash** memories share most of their properties with EEPROM but they are a bit more advanced. They feature better scalability, lower cost, faster read and they can also be electrically erased and programmed. These properties have made them to suffer an incessant growth during last years favoring their use over other alternatives. The flash memory growth trend can be observed in Figure 1.4 [GF12] for **SLC** (*Single Level Cell*, only 1 bit of

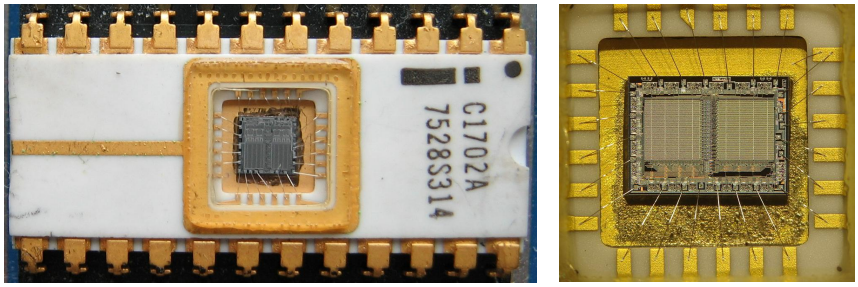


FIGURE 1.3: Example of EPROM memory. Detail of the window that allows the UV radiation to reach the Silicon to erase the memory content by ionization.

information is stored in each cell) and **MLC** (*Multi Level Cells*, the cell can save more than 1 bit at a time) demonstrating the enormous investment around this technology.

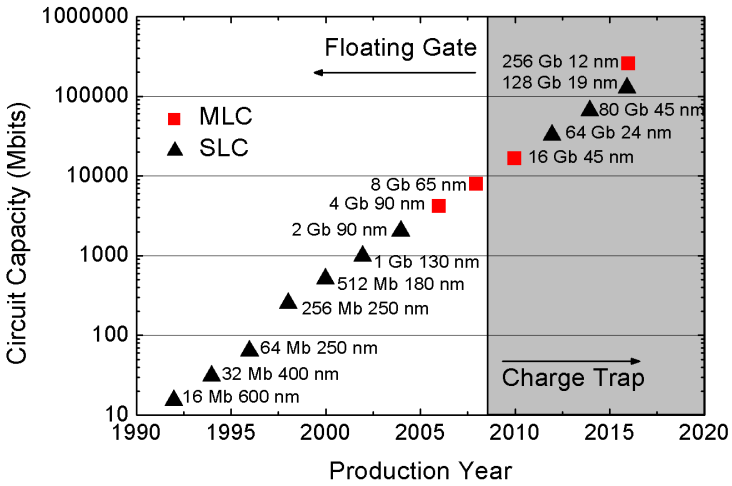


FIGURE 1.4: Flash memory growth trends for single and multi level cells [GF12].

The last non-volatile memory is the **NVRAM** (*Non Volatile RAM*). Each NVRAM cell is formed by a typical SRAM cell (see volatile memories below) which includes also a little battery to power itself in case of absence of an external energy supply. In other words, it behaves like a typical SRAM which is always powered.

1.2.2. Volatile Memories

Volatile memories enclose mainly two different types, static memories, known as SRAM (*Static RAM*), and dynamic memories, DRAM (*Dynamic RAM*). The main difference between them is the time while they can store the information without any loss. **SRAM** on one hand, keep the information as long as they are powered. Only if the power is unplugged their content is lost. On the other hand, **DRAM** cells store the data for a short period of time, around milliseconds. To avoid losing data with time, DRAM takes advantage of the block known as *DRAM controller*, which permits the memory to be refreshed before the data is corrupted and therefore irrecoverable. So, there exists a way to keep the data safe on a DRAM.

The advantage of DRAM compared to SRAM is that they consume less area. This reduced surface leads to memory chips with larger storage capacity and lower costs. Typical SRAM circuits have less than a hundred of MB while DRAM can easily arrive to GB, see Figure 1.5.

1.2.3. Memory Comparison

A comparison between the main SSM is summarized in Table 1.1 to obtain a more general point of view.

FIGURE 1.5: Dynamic RAM DDR4 prototypes of 16 GB presented by Hynix® fabricated using a 20 nm process.

Type	Volatile	Cost/Bit	Write Speed	Read Speed
ROM	No	Inexpensive	n/a	Fast
PROM	No	Moderate	Slow	Fast
EPROM	No	Moderate	Slow	Fast
EEPROM	No	Expensive	Slow	Fast
Flash	No	Moderate	Slow	Fast
NVRAM	No	Expensive	Fast	Very Fast
SRAM	Yes	Expensive	Fast	Very Fast
DRAM	Yes	Moderate	Moderate	Moderate

TABLE 1.1: Non-volatile and volatile solid state memory cells comparison.

In general, the choice of one type of memory or another will be determined by its purpose. The main advantage of volatile cells is their access speed. DRAM cells are often used when both fast access and high storage capacity are required. If the most important point is having very high access speed with/or higher retention time, the usual option taken is SRAM. On the other hand, non-volatile memories are widely used when systems require to save the information for long time. If the data is only going to be read, masked ROM are used when mass production and PROM for custom projects or prototyping. EPROM, EEPROM and Flash memories are reserved for such cases where the information stored will be modified. Flash is the best candidate due to its storage capacity and price. Lastly, the use of NVRAM is almost restricted to very demanding applications because of its high price which limits them to few hundreds of bytes.

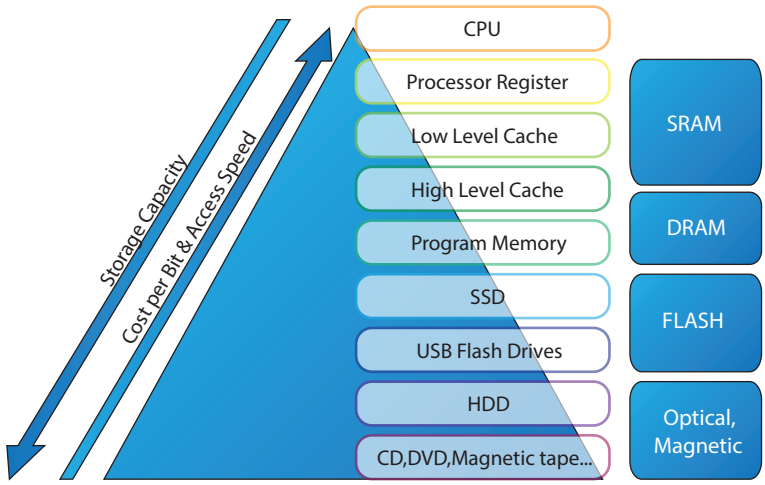


FIGURE 1.6: Pyramid memory hierarchy in a PC [BO03]. Arrows aim rising values while the pyramid shows distances from memories to CPU at its top.

In complex systems, e.g. a PC, several types of memories are present at the same time. This allows to obtain a better global performance taking

advantages of the best properties of each memory type. The computer typical pyramidal structure exhibiting the trade off between memory operation speed and storage capacity is depicted in Figure 1.6 [BO03]. Here, SRAM is reserved for very fast data access, typically processor register and low cache levels with low storage capacity. DRAM on its side, is almost always used as the main program memory and sometimes in high cache levels as eDRAM (embedded DRAM) since it has larger storage capacity but deteriorated access speed. Lastly, the slower HDDs and optical based storage systems, are used to save the information when it is not being addressed thanks to their larger and non-volatile storage capacity. The aim of this memory hierarchy is to emulate a large storage capacity with a very fast access time simultaneously.

Among all the memories previously discussed, there is one whose evolution has been especially interesting for computers and embedded systems. It provides very high integration leading to high storage capacity while also having low power consumption and low manufacturing cost. This memory is the Dynamic RAM and will be deeply reviewed in the next section.

1.3. Dynamic RAM Semiconductor Memories

When purchasing a commercial dynamic memory, not only the memory cells but also the power and control circuitry to manage all operations are provided. In order to reduce complexity and cost, DRAM cells are typically arranged in a **2D matrix**. So, each information bit is accessed using an unique column and row at a time. A general diagram of this structure is represented in Figure 1.7.

Commercial DRAMs are very complex. They are formed by several modules and have a lot of extra circuitry controlled by many different signals. Some of the required signals are used for example to select which memory

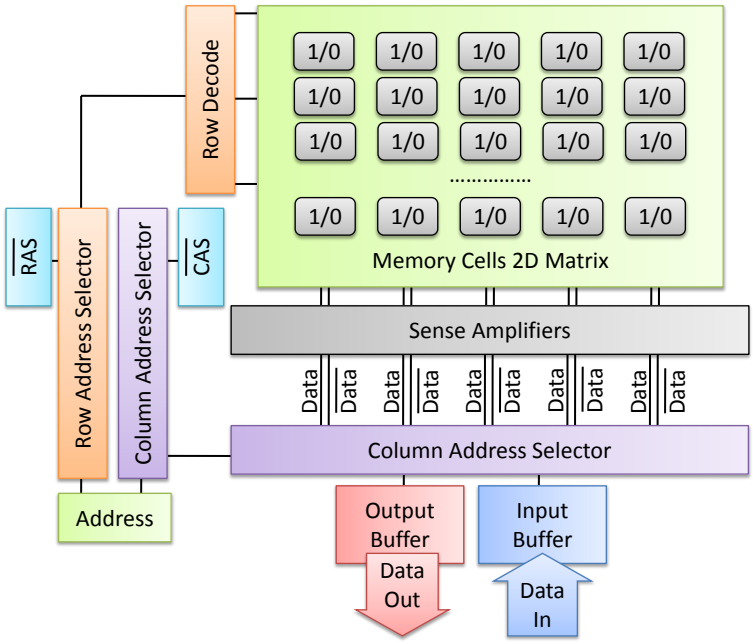


FIGURE 1.7: Typical DRAM structure. Memory cells are arranged in a 2D matrix structure. Each one is accessed with an unique row and column address [MS97].

module is accessed, **CS** (*Chip Select*), to indicate whether it is a writing or a reading operation, **WE** (*Write Enable*), or to define the row and column to access, **RAS** (*Row Address Strobe*) and **CAS** (*Column Address Strobe*).

Along the years, DRAM memories have evolved leading to many different varieties which differ in the use or in its basics. The most representatives DRAM types are listed in Table 1.2 [MS97]. The way information is accessed in the memory has evolved incessantly allowing to have more data and lower latency. The most important access modes are represented in Figure 1.8.

Although first DRAM designs read each cell one by one needing to explicitly indicate which one will be accessed (**Normal Mode**), memories have evolved a lot since then [Sid13]. Firstly, **FPM** (*Fast Page Mode*) DRAMs

Type	Name	Abbreviation
Standard	Fast Page Mode	FPM
	Extended Data Output	EDO
	Burst EDO	BEDO
	Audio RAM	ARAM
Cache	Enhanced RAM	EDRAM
	Cache RAM	CDRAM
Synchronous	Synchronous DRAM	SDRAM
	Double Data Rate SDRAM	DDR SDRAM
	Synchronous Graphic DRAM	GDDR
Cache Synchronous	Enhanced DRAM	ESDRAM
Video	Video RAM	VRAM
	Window RAM	WRAM
Pseudo Static	Pseudo Static RAM	PSDRAM
	Fusion	-
Other Configurations	Rambus	RDRAM
	SyncLink	SLDRAM
	3D	3D
	Next Generation	nDRAM
	Multi Bank	MDRAM
Other Technology	Ferroelectric RAM	FRAM

TABLE 1.2: Different Dynamic RAM memories [MS97].

allowed to read a whole page of the memory (all memory cells in the same row) without changing the RAS signal, only the CAS and address. After that **Nibble mode** memories were introduced. In this case, after specifying the initial cell address, 4 consecutive cells output their data following the change in the CAS signal. The **Static Column Mode** was equivalent to the Nibble Mode but the switch of the CAS signal is not necessary anymore. After these initial approaches, the **EDO** (*Extended Data Output*) memories, also called

hyper-page-mode, appear. This design enhanced the amount of time for which the data was available to read at the output. This was achieved by latching its value while new data was addressed. This time extension reduces the access cycle time with respect to previous designs. **BEDO** memories (*Burst EDO*) were quite similar to EDO but the reads or writes operations were done by sequences of 4 without changing the row address. BEDO never arrived to the market because vendors as Intel® bet for a synchronous design, the **SDRAM** (*Synchronous DRAM*). On their side, **Audio DRAMs**, **cache DRAMs** or **Enhanced DRAMs** feature different improvements that are mainly related to the access techniques to improve the bandwidth and/or latency.

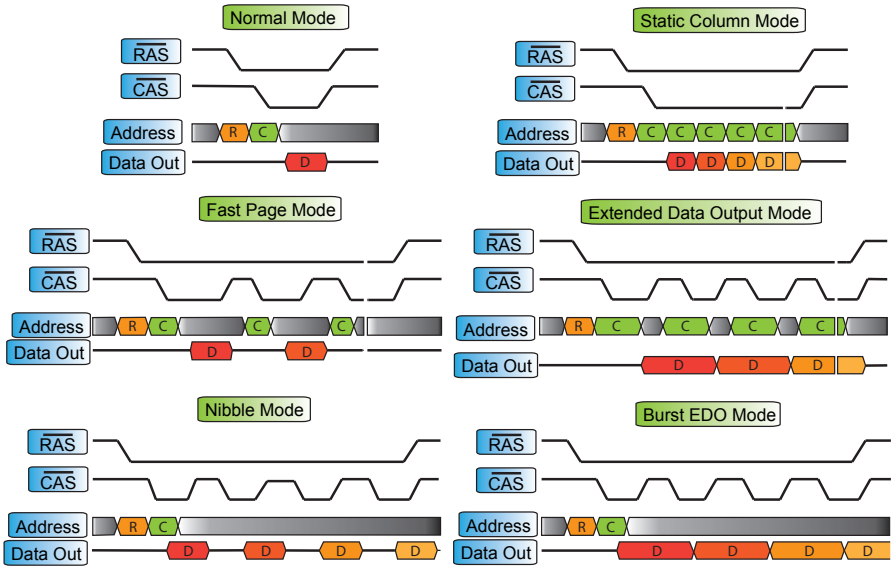


FIGURE 1.8: Comparison of some Dynamic RAM High Speed Access Modes [MS97]. The cycle time of EDO and BEDO schemes are reduced with respect to the others types.

In the last decade, SDRAM has clearly superseded any other type of dynamic random access memory. Until SDRAM appears, traditional memories including DRAM, operate in an asynchronous manner. They reacted to changes

in the control lines and they were only able to operate as the requests were presented to them, dealing with only one at a time. Synchronous DRAM memories on the other hand, are able to operate more efficiently. They are **synchronized with the processor CLK** (system *CLocK* signal), **enabling them to operate at much higher speed**. SDRAMs are usually built with two separate banks of cells. This structure allows them to have different rows active at the same time gaining concurrent access/refresh and recharge operations. For a *write* operation, the command can be immediately followed by another without waiting for the original data to be stored within the SDRAM memory itself. On the other hand, in case of a *read* operation, the requested data appears a fixed number of clock cycles after the instruction was presented.

There are more than one type of SDRAM but the most popular and widely used today are the **DDR** (*Double Data Rate*) SDRAMs. In contrast to **SDR** (*Single Data Rate*), **DDR allows the transfer of two words of data per clock cycle** (one word at each rising or falling edges of the CLK signal instead of using only the falling edge). This difference implies an important change in throughput of a factor 2 (+100%) maintaining the **same latency**. The differences between SDR and DDR are illustrated in Figure 1.9.

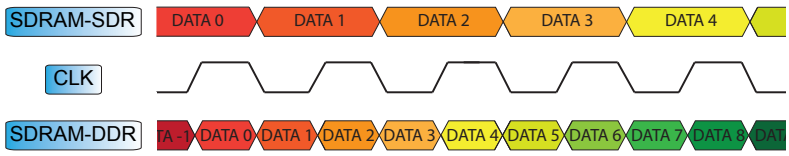


FIGURE 1.9: Comparison in accessed words between SDR and DDR memory types. The SDR memory outputs one data every falling edge of the CLK signal while the DDR outputs also data in the rising edge.

Once the general operation of a memory module has been addressed, a closer look into the memory cell itself is presented. There are two main designs

for DRAM memory cells: the three transistor and one capacitor design and the one transistor and one capacitor design. These two memory cells schemes use the charge stored in a capacitor to discriminate the information. If the capacitor is charged, the cell stores the '1' state and if it is discharged it stores the '0' state. This leads to a binary scheme of storage defining one bit of information per cell. The access to the bit stored is based on a **voltage sense**. Transistors are used to allow or not the charge to flow and sense whether the capacitor is charged or discharged. Nevertheless, **one problem arises in these schemes: the information is gradually lost with time due to non-idealities, the leakage current in the capacitor and the transistor**. It is then necessary to **refresh the data periodically** to ensure that the information is not corrupted. This is the reason why they are called *dynamic memories*.

First reports of these DRAM cells design appeared in the 60's. In 1966, Dr. Robert Dennard, an engineer working for IBM using the standard 6 transistors SRAM cell had the idea of storing each bit of information by using only a single transistor and one capacitor (**1T+1C scheme**). He received a patent for his *Field-Effect Transistor Memory* in June, 1968 [Den68]. The first DRAM integrated circuit commercialized was released in 1970 by Intel® [Kan10]. It was a 1024 bits memory and used instead the three transistors and one storage capacitor design (**3T+1C-scheme**) for each cell. The transition from the 3T+1C to the 1T+1C cell took place gradually during the 70's.

In the next sections, the main properties of these two DRAM cell designs will be presented.

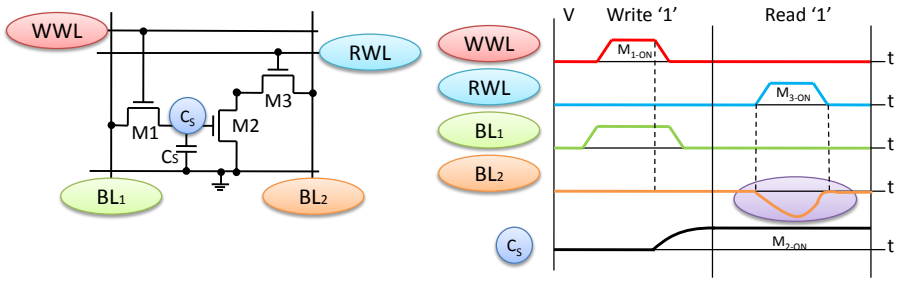


FIGURE 1.10: Scheme of the initial 3T+1C DRAM cell with its behavior.

In this design, the capacitor C_S stores the bit of information as charge and the three different transistors are controlled by four distinct lines to *write* and *read* the cell. Transistor M_1 is driven by line WWL (*Write Word line*) and is responsible of the *write* process. The voltage on WWL allows or not the capacitor C_S to be charged with the voltage applied on BL_1 (*Bit Line 1*). If V_{High} and V_{Low} are the highest and lowest logic voltages. When $WWL = V_{High}$, the voltage on the capacitor changes to $V_{C_S} = V_{BL_1}$. Otherwise the voltage on the capacitor remains unchanged. Once the information is written, i.e., the charge is stored in C_S, transistor M_1 should be cutoff to isolate the storage node preventing undesired discharges, $WWL = V_{Low}$.

The *read* process is on the other hand based on sensing the possible voltage drop on BL_2 (*Bit Line 2*), which should be always biased to high voltage $V_{BL_2} = V_{High}$. Turning on transistor M_3, achieved by rising line RWL (*Read Word Line*), allows BL_2 to be discharged through M_3 and through M_2 only if the level stored in the cell is high, $V_{C_S} = V_{High} > V_{Th2}$. In that case, BL_2 will discharge elsewhere it will retain its voltage since transistor M_2 will not drive

any current. By checking if V_{BL_2} changes its value or not, it can be known if the high level is stored, there is a voltage drop, or the low level, no significative voltage change on BL_2.

Although in this memory cell there is no constraint regarding the transistors ratio, it is important that the memory levels applied to BL_1 follow the voltage range defined in Equation 1.1 and 1.2 to ensure proper operation.

$$V_{DD} \geq V_{High} = V_{BL_1} > V_{Th_2}\ [V] \tag{1.1}$$

$$0 \leq V_{Low} = V_{BL_1} < V_{Th_2}\ [V] \tag{1.2}$$

The main advantage of this memory cell compared to others DRAMs is the **non destructive reading**. In contrast, it presents **low integration**

c

t

t

f

v

i

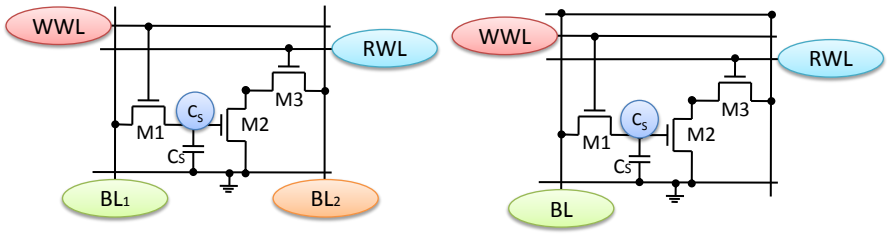


FIGURE 1.11: Comparison in schemes of 3T+1C DRAM memory cells with four and three control lines [Sun10].

1.3.2 1T+1C DRAM Cells

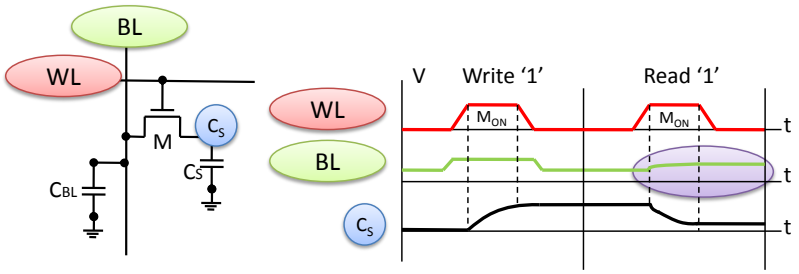


FIGURE 1.12: 1T+1C DRAM cell design with its operation [Sun10].

At first sight it is clear that both, the circuit and the behavior, are much simpler than the 3T+1C-scheme previously discussed. In this case, the WL controls both *readings* and *writings* by turning on the transistor M. BL on the other hand, is the line that contains the data to *write* or *read*. For example, to *write* a state '1' in the cell, the bit line is set to high, $V_{BL} = V_{High}$ and then M is switched ON ($V_{WL} = V_{High} > V_{Th}$). In this situation the capacitor is charged (this would be the same case as *refresh* the memory cell). After the charging, M is turned OFF isolating C_S to prevent the loss of its charge.

To *read* the value stored in the cell, it is necessary first to pre-charge BL to a value between high and low states, V_{Pre}. In order to do so, the parasitic capacitance of the bit line, C_{BL}, may be used. When turning M ON, there is a charge transfer between C_S and C_{BL} until the voltage across them is equal. The sense of charge flow depends on the value stored in the cell that is going to be read. The latter sensing of the voltage change in BL enables the state

discrimination. An increase in the bit line voltage, V_{BL}, reflects that the state '1' was saved in the capacitor while a decrease would indicate that state '0' was stored.

A fundamental aspect in this design is that the information in the storage node, charge in C_S, is modified when performing a read. This translates in a **destructive reading**. A *refresh* operation after reading to avoid corrupting the information is then a must.

The pre-charge voltage in the bit line before a reading (with $V_{WL} = V_{Low}$) is given by Equation 1.3.

$$V_{BL} = V_{Pre} = 0.5 \cdot (V_{High} - V_{Low})\,[V] \tag{1.3}$$

Assuming that the initial state of the memory cell is '1' ($Q_S = C_S \cdot V_{High}$) and that the '0' state voltage is zero volts ($V_{Low} = 0V$), if the transistor M is switched ON, there will be a charge transfer between capacitors (C_S and C_{BL}) until they both have the same voltage (see Equation 1.4).

$$V_{BL} = \frac{0.5 \cdot C_{BL} \cdot V_{High} + C_S \cdot V_{High}}{C_{BL} + C_S}\,[V] \tag{1.4}$$

An increase in the bit line voltage is observed. The voltage change is given by Equation 1.5.

$$\Delta V_1 = \frac{0.5 C_{BL} V_{High} + C_S V_{High} - 0.5 V_{High} \cdot (C_{BL} + C_S))}{C_{BL} + C_S} = \frac{0.5 V_{High} C_S}{C_{BL} + C_S}\,[V] \tag{1.5}$$

Equivalently, if the initial state of the memory cell is '0' ($Q_S = 0$ so $V_{C_S} = 0$), after pre-charging the bit line and switching on the transistor M, there will be again a charge transfer between capacitors. The final bit line voltage appears

in Equation 1.6.

$$V_{BL} = \frac{0.5 \cdot C_{BL} \cdot V_{High}}{C_{BL} + C_S} \; [V] \tag{1.6}$$

In this case, this translates in a voltage drop with respect to V_{Pre} as shown in Equation 1.7.

$$\Delta V_0 = \frac{0.5 C_{BL} V_{High} - 0.5 V_{High}(C_{BL} + C_S)}{C_{BL} + C_S} = \frac{-0.5 V_{High} C_S}{C_{BL} + C_S} = -\Delta V_1 \; [V] \tag{1.7}$$

These V_{BL} variations allow the discrimination of the state stored in the memory cell. V_{BL} changes with time when performing a reading, Figure 1.13. The second change in the voltage in Figure 1.13 happens due to the activation of the sense amplifiers, circuits in charge of the discrimination, with their parasitic capacitances.

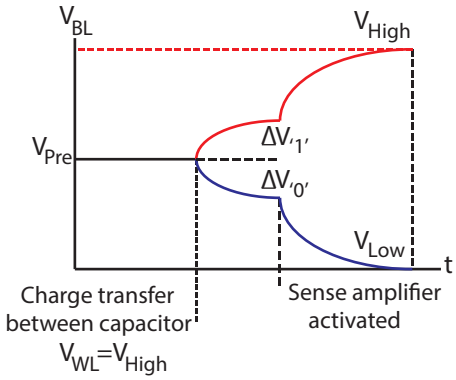


FIGURE 1.13: 1T+1C bit line voltage during reading [Kim98].

The main disadvantages of these cells are the need of the *refresh* after a reading cycle because the *destructive readings* and also the periodic refresh. In contrast, this cell design is very small in size leading to very **high integration**

and therefore reducing considerably costs during mass production, main reason of its success.

1.3.3. Evolution of the 1T+1C Cell

With very few exceptions, the clearly dominant factor in the evolution of any technology that has as its goal the marketing, is the price. Despite the advantages that may be obtained, if it is not profitable, no evolution step takes place: cost saving is always the first objective. Memory industry is not an exception, in fact, it is a clear example of cost reduction strategy achieved thanks to miniaturization. The cost of an integrated circuit is directly related to the area of Silicon it consumes, thus to the total amount of circuits that can be obtained per wafer. Two different saving paths has been followed. The first one is to **increase the wafer diameter**. Industry has gone from 25 mm (1 inch) in 1960 to 300 mm (11.8 inches) in 2001, and presumably soon to 450 mm (18 inches) around 2017-2020 [ICE98]. The second path consist in **reducing the size of the circuit** itself. New materials and fabrication processes have enabled the size reduction of the transistor and capacitor. These two approaches leads to an increase in the **DPW** (useful dies per wafer), see Equation 1.8 [RCN03], where d is the diameter in cm, and S the target integrated circuit size in cm^2.

$$DPW = \frac{\pi \cdot (d/2)^2}{S} - \frac{\pi \cdot d}{\sqrt{2S}} \, [useful\ dies\ in\ the\ wafer] \tag{1.8}$$

Although both of them are still in use, there is no doubt about which of them has motivated the largest reduction in the price per storage bit. Capacitor and especially transistors have shrunk their dimension incessantly leading to a cell size with less than $0.05\,\mu m^2$ [Sun10]. The increase in storage DRAM capacity has followed **Moore's Law** [Moo98]. The evolution of the memory

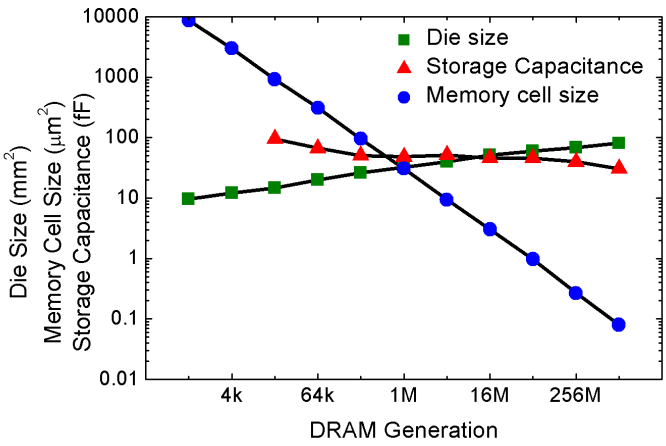


FIGURE 1.14: DRAM cell evolution, storage capacitance, memory and die size against the memory generation [Sun10]. The scaling of the memory cell (transistor and capacitor) is the main factor for obtaining larger storage capacity.

size and storage capacitance are depicted in Figure 1.14. The memory cell size has been gradually reduced while the die size has more or less remained constant.

In contrast to the cell size, the storage capacitance per cell has remained almost the same over the years (Figure 1.14). This constant capacitance, of around 25-30 fF in last nodes [MS97, Kim98, SK00], ensures the storage of enough charge for the proper discrimination of the memory states. Noise margin, access speed and power consumption are some of the specifications in a DRAM cell that are strongly related to the capacitor properties [Den84]. The capacitance depends on both the geometry and the properties of the material used in its fabrication. In general, for a planar capacitor the capacitance is

given by Equation 1.9.

$$C_S = \frac{\epsilon \cdot A}{t} \, [F] \tag{1.9}$$

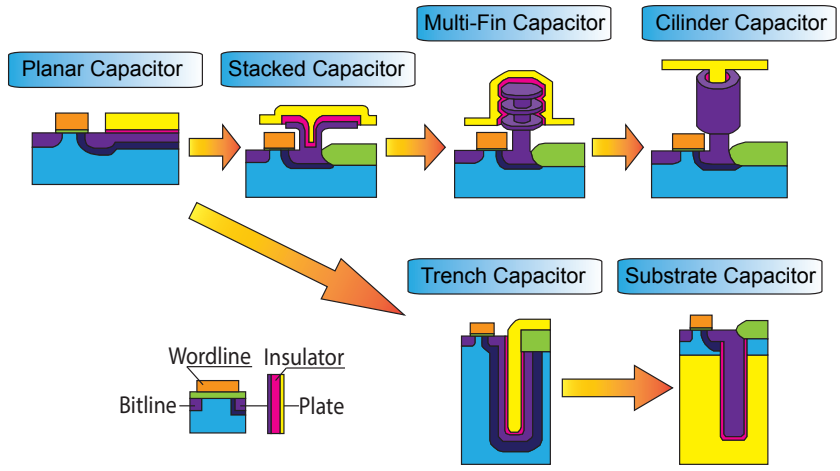


FIGURE 1.15: DRAM cell storage capacitor evolution [Sun10].

Where ϵ, A and t are respectively, the dielectric permittivity constant of the insulator used between the two plates, the total area of the plates and the thickness of the insulator layer. As the memory cell is scaled the capacitor geometry and shape are modified reducing the storage capacitance. **The hardest challenge to continue with the memory cell scaling is the capacitor real-state reduction while the minimum capacitance is maintained**. Several fabrication techniques has been proposed to ensure the adequate capacitor scaling, Figure 1.15. The three most significant architectures are detailed in the following sections.

Planar Capacitor

Planar capacitor design was used in the first DRAM cells architectures, Figure 1.16. It was conceived by Dr. Robert Dennard and was widely used between 1970 and 1980, for memory chips with less than 1 Mb. **The transistor is located beside the capacitor which lays horizontally**. In the beginning, the area consumed by the capacitor was around a 30 % of the cell size but this percentage was gradually increasing due to the transistor aggressive scaling [Sid13].

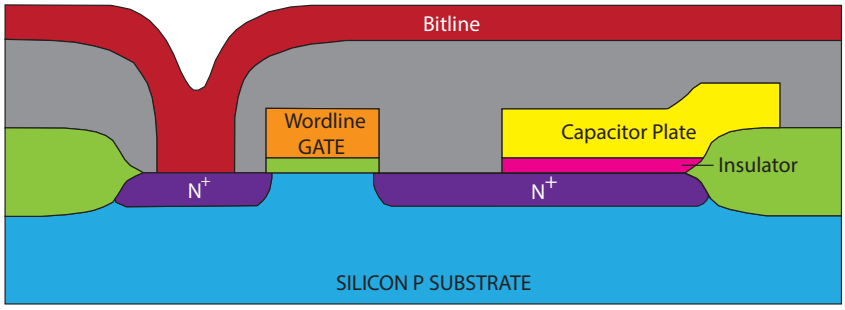


FIGURE 1.16: Typical planar capacitor structure.

Along with the shrink of the capacitor area, one of the first scaling engines was the reduction of the dielectric thickness [Tom04]. This process leads to higher capacitance maintaining the same area or same capacitance reducing the capacitor real state. The main issue that this scaling approach brings is that it is not possible to reduce the thickness of the insulator as desired. Firstly, due to technological issues related to very thin layers, deposition or epitaxial grows, and secondly, due to leakage and insulator dielectric strength [VK96]. As the oxide thickness is thinned to reduce the real state of the capacitor, the electric field across the plates increases. This process is limited by the maximum electric field the insulator can withstand without breaking down

($\overrightarrow{E}_{Break}$), that means without experiencing failure of its insulating properties [CHH85, DiS73].

To overcome the problems related with area that could not be solved only by slicing the insulator, a new structure was proposed in 1974 by Hideo Sunami based on highly efficient silicon solar cell with plural steep trenches [Sun10].

Trench Capacitor

In this design, **the storage capacitor is fabricated in a trench etched into the substrate**, Figure 1.17.

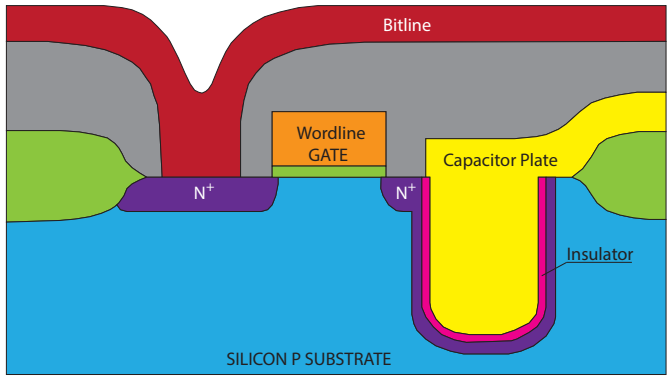


FIGURE 1.17: Simple trench capacitor structure.

The first integrated circuit that used this **trench capacitor** architecture appeared in 1982 with 1 Mbit of storage. The fabricated memory cell measured 4 μm by 8 μm with a 2.5 μm deep trench. The insulator was a triple layer of $SiO_2/Si_3N_4/SiO_2$ with an SiO_2 equivalent thickness of 15 nm. Resultant capacitance per unit area was 2.2 fF/μm^2 and the final capacitance per cell was around 45 fF [Sun10]. Figure 1.18 shows a cross section of a trench capacitor based memory cell.

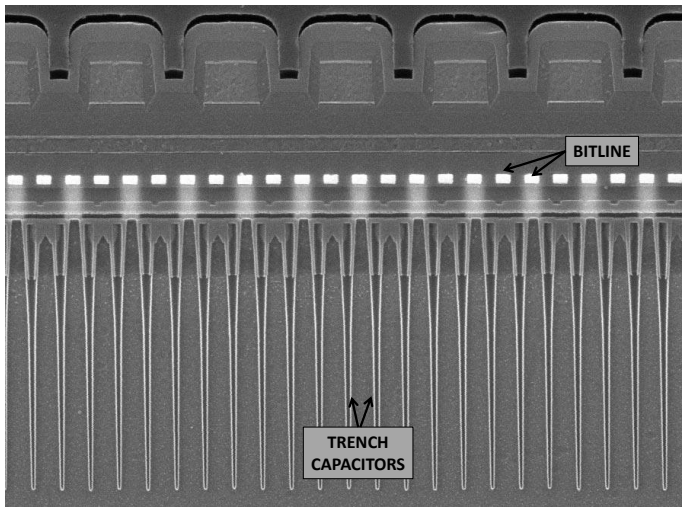


FIGURE 1.18: Detail of an actual DRAM matrix based on the trench capacitor design [ICE97].

Although the reduction in area consumption is remarkable, some problems arise with the use of these cells [Sun10]:

- Major problems when fabricating due to the need of high directional and anisotropic etches and very thin layer depositions.
- Degraded oxide uniformity on trench wall. Differences in crystallographic orientations lead to distinct oxidation rates and therefore different thicknesses. This finally implies a degradation of the oxide integrity.
- Trench to trench leakage attributed to a parasitic MOS transistor formed over adjacent two memory cells. Two trenches work as deep source and drain, capacitor plate is the gate and thick field oxide is the gate oxide. This issue can be avoid spacing the cells or using Boron implantations in-between.

- Increasing *soft error* (error in a signal or data that is wrong but it does not imply a mistake or breakage in the device) due to impact of high energy particles such as alpha particles.

Together with the trench capacitor, the **stacked capacitor** cell has also been extensively used in memory manufacturing.

Stacked Capacitor

Though and patented by Mistu Koyanagi [Koy02]. In **stacked capacitor** cells the capacitor is fabricated using a thin insulator rounded by two poly silicon layers as is shown in Figure 1.19. The usual **fabrication is done on top of the transistor** in order to reduce the area consumption and have higher integration. The immediate problem is related to the metals layers used to interconnect the different devices and the fabrication steps required to build this vertical structure.

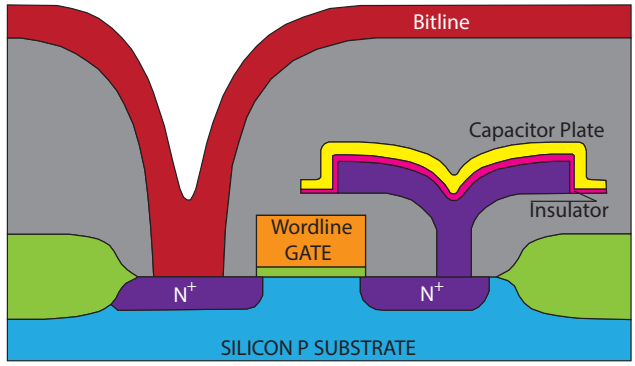


FIGURE 1.19: Stacked capacitor structure.

As the memory cell has shrunk, it has been necessary to complicate more and more the structure of the storage capacitor. Several stacked architectures

are shown in Figure 1.20. The aim is to reduce the real state and volume of the capacitor trying to maintain the minimum capacitance required for proper sensing. To do so, the design has changed to **very complex 3D structures** that enlarge the capacitors plate area by adding several folds or spikes but maintain the same cell area.

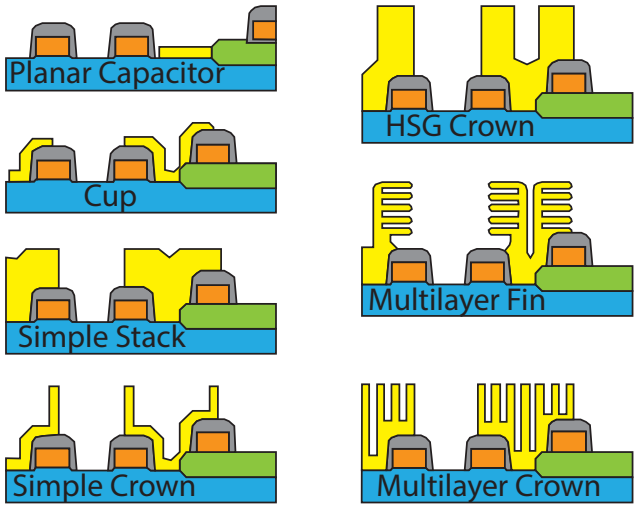


FIGURE 1.20: Several stacked capacitor 3D architectures.

Material revolution

Together with the evolution in the capacitor architecture and insulator slicing, another fundamental step that was taken is the use of **new insulating materials**. These new materials must fulfill many requirements [JSBCL06] (as SiO_2):

1. Large band gap to be considered as an isolating material, $E_g > 3$ eV.
2. High relative permittivity, $\epsilon_i > 10$.

3. Band energies position quasi symmetric with respect to silicon. High barrier for electrons in E_c and high barrier for holes in E_v.
4. Low density of interface states, $D_{it} < 10^{10}\ eV^{-1}cm^{-2}$.
5. No reaction with surrounding materials, as for example silicon and metal gate contacts.
6. Amorphous or single-crystalline lattice with no phase changes between room temperature and 1050 °C for at least 30 seconds.
7. Compatible elements to **CMOS** (*Complementary MOS*) technology.
8. Good adhesion to silicon, silicon dioxide, nitride...
9. Dry etch possible. All elements during the etch should build volatile compounds.
10. Selectively etchable to silicon, silicon dioxide, nitride...

Some of these new ***high-k* materials** materials, like **Hafnium Oxide** (HfO_2), are being already used for the front-gate oxide in MOSFETs [LAOK03, HKLH03]. A list of the most relevant appears in Table 1.3 [Tom04].

Dielectric Symbol	Relative ϵ_i $(-)$	C_{Crit} $(fF/\mu m^2)$
$SrTiO_3$	230	55.0
$(Ba_{1-X}Sr_X)TiO_3$ (BST)	320-1250	40.5-118.1
$Ba(Ti_{0.8}Sn_{0.2})TiO_3$ (BTS)	210	-
$(BaPb)(ZrTi)O_3$ (BPZT)	200	8.9
$(Pb_{1-X}La_X)TiO_3$ (PLT)	1400	24.8
$(PbLa)(ZrTi)O_3$ (PLZT)	1474	87
$(PbZr_{1-X})Ti_XO_3$ (PLT)	>1000	>70

TABLE 1.3: Comparison between different *high-k materials*.

Among this, **BST** (*Barium Strontium Titanate*) is the most promising insulator material in future DRAM cells [BOW+12] since it provides the highest capacitance per unit of area.

1.3.4. Problems and Limitations of 1T+1C DRAM cells

Although the essence of the 1T+1C DRAM cell has remained unchanged for more than thirty years, it has evolved to follow the aggressive scaling that face nano-electronic devices over time. However, the feasibility of scaling this same structure beyond the 22 nm node, is being widely questioned. The main problems encountered are related to the elements forming the memory cell. firstly, scaling the structure of the memory cells together with the sense amplifiers and circuitry, and secondly and foremost, the scaling of the cell transistor and the storage capacitor.

Transistor Scaling

The scaling of the transistor is proved beyond the 22 nm node but, a transistor used as a switching device for a 1T+1C cell should ensure some characteristics [MDB+02]:

- Low leakage current.
- High ON current.

The first factor is limited mainly by **subthreshold currents** and **leakage currents** like **tunneling current** through the gate oxide and **GIDL** (*Gate Induced Drain Leakage*). To ensure an adequate retention of data before refreshing, in every memory cell the mean average of the sum of these contributions (together with the capacitor leakage) should be much lower than

the usual leakage in a normal transistor (around nA). Lastly, the ON current defines the charging/discharging speed of the capacitor and then, the operation time of the cell. It is limited by the maximum voltage that can be applied to the gate. Since the gate oxide is sliced when scaling the device to effectively control the **SCE** (*Short-Channel Effects*), the maximum gate voltage is also reduced.

Capacitor Scaling

Among others problems as ensuring the minimum 30 fF of capacitance and low leakage, the storage node needs [MDB+02]:

- Low series resistance.
- Low inter-cell coupling.
- Feasible fabrication.

Low series resistance are desirable for fast memory operation. As the cell decreases in size, the series resistance of the capacitor starts to act as the bottleneck for efficiently transferring the charge from/to the capacitor. The **low inter-cell coupling is defined as the cell to cell interference**, as cells are fabricated closer to each other, the influence they provoke on the surrounded cells is enlarged. **The fabrication of the capacitor is the most important challenge that DRAM technology faced for future**. As the DRAM cell shrinks the aspect ratio (height over top dimension) of the capacitor in 3D structures (stacked or trench) is getting huge. These high directional structures are very extremely difficult to achieve in mass production.

1.4. Conclusions

In this first chapter a basic review around the most important solid state memories has been carried out. The main types of memory were described at the beginning showing their advantages and drawbacks to gain a better point of view when focusing on the dynamic RAM technology. It has been pointed out that the critical factor of the DRAM technology is the required refresh operation to avoid corrupting the information stored, and how this important drawback is accepted in order to gain a higher level of integration. The complex evolution of the structure in typical 1T+1C DRAM cells has been analyzed along the time. Finally, the main scaling problems of this DRAM design have been discussed for future technological nodes were discussed motivating the objective of this work, the study of one specific candidate of memory cell based on using only a single transistor on SOI.

In the next Chapter 2 the **SOI technology and the most relevant Floating Body DRAM cell candidates will be addressed**.

Chapter 2

Floating-Body DRAM Cells

The scaling limitations that the traditional DRAM cell design suffers due to the integration of the capacitor, previously discussed in Chapter 1, motivate the study of new cell architectures that do not include an external capacitor. No extra steps while manufacturing are needed to create this dedicated storage node and the overall size of each memory cell is highly reduced. This increases the integration and reduces the cost. The main question that appears is then: is a single transistor capable to store a bit of information? and if so, how can it be accomplished? To answer these questions, it is first necessary to introduce a technology that nowadays is taking major importance in the semiconductor industry. In this Chapter the main characteristics and properties of the Silicon On Insulator (SOI) technology are presented together with some of the most important memory cells based on it.

2.1. Silicon On Insulator Technology

Typical silicon wafers, also called **bulk wafers**, have a total thickness of less than 1 mm (usually 775 μm for 300 mm [RCN03]). Only a tiny slice of several micrometers at the top is used for fabricating nano-electronic devices, Figure 2.1. The unused bottom region of mono-crystalline silicon is necessary to ensure the structural feasibility of the wafer and the devices, providing strength and avoiding breaks [CL95].

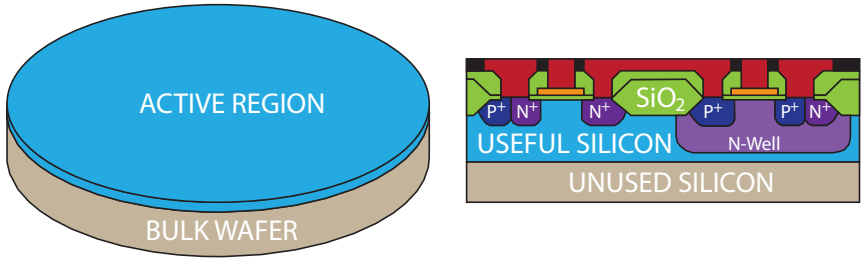


FIGURE 2.1: Detail of the useful layer thickness on a bulk Silicon wafer. Only the top region is used for fabricating devices while the thick bottom region remains unused providing mechanical strength and avoiding breaks.

But using a semiconductor substrate also contributes to some undesired parasitic effects such as:

- Implicit electrical connection between different devices. It is usually solved using lateral isolation techniques like **STI** (*Shallow Trench Isolation*), or channel stop implantations. These techniques consume area and require more fabrication steps.
- Appearance of parasitic capacitances and devices. A NPN **parasite BJT** can appear using the N+ diffusion of the source or drain of a N-MOSFET as emitter, the P-type well acts as the base and the N-type

well as collector. A PNP BJT can also appear the same way next to a P-MOSFET.

- Lower control over **SCEs**. The gate looses the electrostatic control over the channel due to source and drain region influence. This limits the minimum channel length of the device that can be fabricated. To overcome this problem, high body doping to reduce the depletion regions has been used. However, this increase in the body doping has a negative effect on mobility, threshold voltage, transconductance and device variability...

In order to solve these problems, the **SOI** (*Silicon On Insulator*) technology proposes the use of a new film made of dielectric. This insulator layer isolates the active region where devices will be fabricated from the silicon substrate. There are two different alternatives: using a thin insulator layer buried in the silicon wafer or using a wafer made of an insulator material and growing a thin layer of silicon on its top. Both types of approaches are depicted in Figure 2.2.

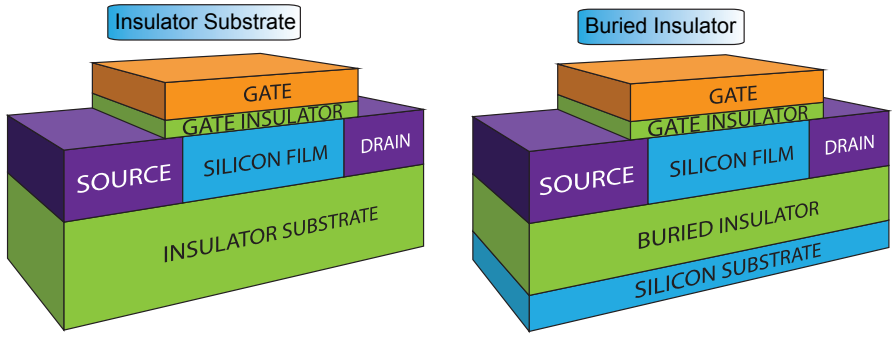


FIGURE 2.2: Different SOI wafer configuration depending on the buried oxide thickness. In the left, a thin Si-film layer is grown or deposited on top of a insulator substrate. In the right, only a buried thin layer of insulator separates the active area to the silicon substrate.

The most common option is to use the buried layer called **BOX** (*Buried OXide*). This enables substrate biasing when the insulator layer is not very thick, less than 200 nm. Nevertheless, to achieve an useful SOI wafer is very challenging. A thin mono crystalline layer of silicon needs to be grown on top of the insulator. The Si-film must feature the same quality and properties as those grown in volume:

- Low density of interface states.
- Uniform thin layers.
- Good performance of the dielectric.

2.1.1. Wafer Fabrication

There are several techniques that have been developed to fabricate SOI wafers. Figure 2.3 shows the most relevant.

Among all of them, the most important and used today is the **Unibond** technique or **Smart-Cut**®. This process is one of the most effective to produce commercial SOI wafers. The *Smart-Cut*® technique combines an **ion implantation** and **wafer bonding** to transfer a thin slice of one wafer to another wafer or insulator substrate. It was first developed in 1992 at CEA-LETI [CW03]. The main steps are illustrated in Figure 2.4 and summarized below:

0. Initially, two bulk silicon wafers, '*A*' and '*B*', are used. The surface of one of them should be completely oxidized, for example wafer '*A*'. This wafer will be used for the active layer on top of the BOX.

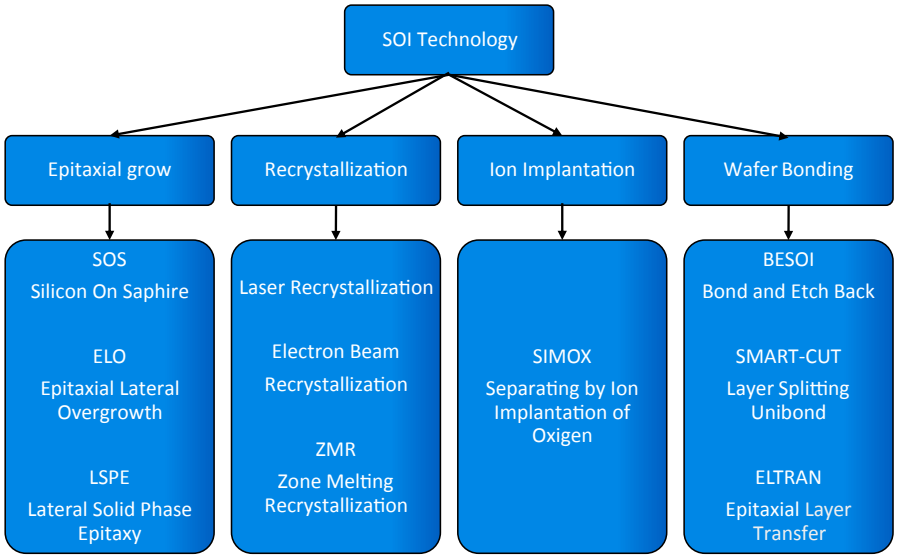


FIGURE 2.3: Different techniques to produce SOI wafers.

1. The next step consists on implanting positively charged hydrogen ions (protons) on the wafer '*A*'. The implantation's energy will define the silicon film thickness.

2. After this, the wafer is cleaned and then bonded onto wafer '*B*' using the SiO_2 previously grown to maintain them together.

3. Then, a first heat treatment is performed at around 400-600 °C. With this, the micro cavities produced by the implantation of protons split up the wafer into two pieces, one of them a bulk wafer, '*A*', and the other an SOI wafer, '*B*'. After this, a second heat treatment to improve the connection between the BOX layer and the wafer itself is carried out.

4. Finally a **CMP** (*Chemical Mechanical Polishing*) process is performed to achieve an uniform wafer surface and also to thin the Si-film to the desired final thickness.

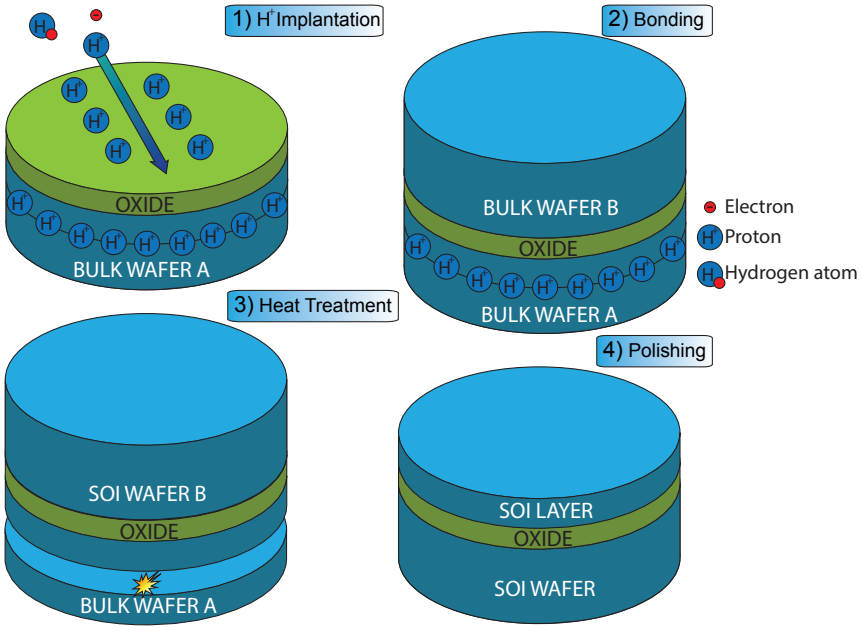


FIGURE 2.4: *Smart-Cut*®, advanced SOI wafer fabrication technique based on wafer bonding.

2.1.2. Advantages and Disadvantages of SOI

The main disadvantage of SOI is the higher price of the wafers due to the extra fabrication steps needed. However, it is worth noting that the final cost of an integrated circuit may be lower due to a simpler fabrication process with less manufacturing steps, it depends on the IC (*Integrated Circuit*). Nevertheless, even if it is more expensive, the advantages that SOI technology provides compared to bulk, are numerous and in many cases justify the overprice. Some of the improvements are [CW03]:

- Avoid the connection between device and substrate:
  - Area consumption reduction.

  - Avoid the latch-up.
  - Lower power consumption.
  - Better subthreshold swing.
  - Lower leakage currents.
  - Better transconductance.
  - Improve the control of SCEs.
  - Lower power voltage.
  - Better immunity to ionizing radiation.

- No need of body doping: lower **RDF** (*Random Dopant Fluctuations*), decreasing variability on threshold voltage and other parameters.
- Capability of integrating different devices on the same wafer such as, CMOS, power devices, bulk designs and optoelectronics.
- Possibility to stack more than one layer of devices (the drawbacks are the interconnection issues that appear and also self-heating related problems [BR07]).

Together with the extra price, there is another important drawback of SOI. The **SHE** (*Self-Heating Effect*) is more remarkable in SOI wafers since the SiO_2 is about two orders of magnitude less thermal conductive than silicon. Thin-film SOI MOSFETs are therefore prone to accumulate heat because it cannot be dissipated rapidly through the BOX. However, recent studies show that the SHE is present but it does not represent a limiting factor for the reliability in ultra-thin silicon films transistors, specially for fast switch operations [RNA+11].

Other constraints that SOI wafers may include are [LF83, WHF96, Col04]:

- The uniformity of the BOX and silicon layers is crucial to avoid high variability.
- **FBE** (*Floating-Body Effects*) [ONSF01, BCFU09, MNH+07]. Although this is not always a drawback, it may lead to abnormal behaviors.
- Inter-gate coupling effects between front and back-channels. As the FBE, it may be also an advantage.
- Large **series resistance** in thin film devices. This is normally reduced by raising the source and drain regions, **RSD** (*Raised Source Drain* also known as **ESD**, *Elevated Source Drain*) technique [WBCC84, CPC02].

2.1.3. Partially Depleted and Fully Depleted transistors

When referring to SOI transistors, the terms **PD** (*Partially Depleted*) and **FD** (*Fully Depleted*) are often used. Both of them make reference to the **depletion level of the silicon body of the transistor**, between the front-gate oxide and the buried oxide, see Figure 2.5. In case of PD transistors, the silicon film is not completely depleted of mobile charges. In contrast, for FD MOSFETs no charge accumulation or storage can be achieved without biasing the gates: there is no quasi-neutral region which serves as a potential well to store majority carriers. In general, the thickness of the silicon film that determines whether it is partially depleted or fully depleted depends mainly on the body doping concentration, $N_{A,D}$. Equation 2.1 indicates the depletion depth for one interface with no lateral influence (1D model).

$$x_d = \sqrt{\frac{2 \cdot \epsilon_0 \cdot \epsilon_{Si} \cdot \Phi_S}{q \cdot N_{A,D}}} \, [cm] \tag{2.1}$$

where ϵ_0 and ϵ_{Si} are the permittivity of vacuum free space and silicon relative permittivity respectively, q is the electron charge and Φ_S is the surface potential at the interface. Typically, commercial silicon films larger than 70 nm correspond to PD and below 30 nm to FD [CA10]. The main differences between both type of transistors are resumed in Table 2.1, [Cau10, YKH+94, DHL+03, MN02].

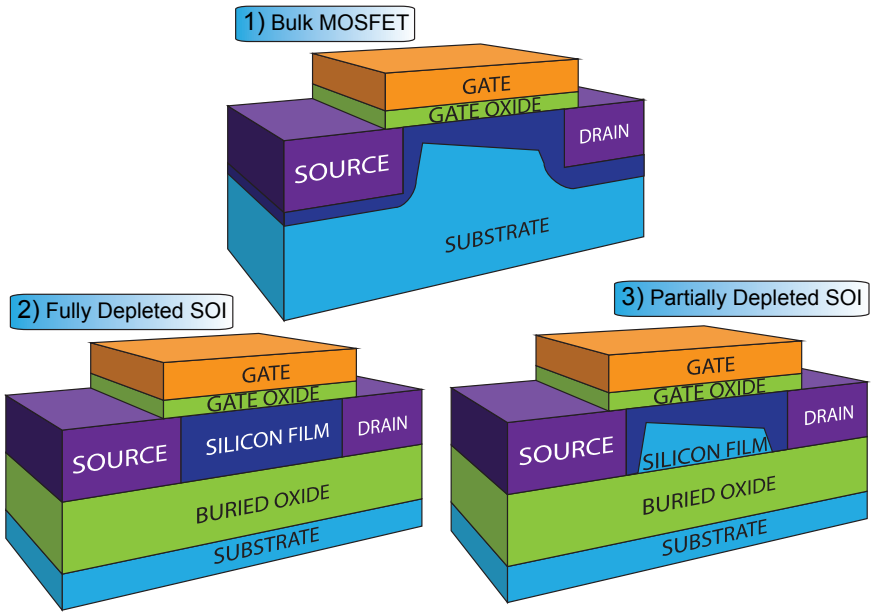


FIGURE 2.5: Depleted region (dark color in the silicon film) comparison between bulk, fully and partially depleted SOI transistors. The depletion region induced by the back-gate is not represented.

For long devices, PD transistors provide relaxed constraints about the silicon film thickness, lower **DIBL** (*Drain Induced Barrier Lowering*) but larger **SS** (*Subthreshold Swing*) and lower drain current with respect to FD. On the other hand, FD transistors allow better scalability (lower SCE thanks to the thinner Si-film) and lower SS. The most remarkable difference between PD and FD devices is the **inter-gate coupling effect**. FD-SOI transistors

Parameter	Partially Depleted	Fully Depleted	Bulk
Silicon Thickness	>70 nm (typ.)	<40 nm (typ.)	-
Source/Drain resistance	Moderate	High	Low
I_{on}	Moderate	High	High
I_{off}	Very Low	Low	Moderate
DIBL	Low	Very Low	Moderate
Subthreshold Swing	Moderate	Very Low	High
FBE	✔	✖*	✖
Kink Effect	✔	✖*	✖
History Effect	✔	✖*	✖
Coupling Channel	✖	✔	✖

TABLE 2.1: Partially depleted, fully depleted SOI and bulk transistors comparison [Cau10, YKH+94, DHL+03, MN02]. (*) Not intrinsically .

parameters depend on both front and back interfaces (threshold voltage, DIBL, effective mobility...). This can be used to tune or boost the device performance [NTJ+11].

2.1.4. Floating-Body Effect

SOI transistors provide some very interesting properties to enhance the performance with respect to bulk devices, but they also have some other peculiarities that depending on the application, may or not be beneficial. The most remarkable effect and one of the most challenging issues in PD-SOI technology, is the control of **FBEs**. These effects appear due to the perfect isolation of the silicon film obtained when using the buried oxide layer. They are motivated by the accumulation of mobile charge in the body of the device. These charges are confined since they cannot scape through the substrate as typically happens in bulk transistors.

Although this effect may be detrimental, it also allows MOSFET to exhibit very interesting properties such as memory capabilities, *floating-body memories* [BCFU09]. Some of the most important aspects of FBEs are summarized below [BR07, UR09]:

History effect and threshold voltage variability

The most prominent electrical property of the PD-SOI device is the **history effect**. The I-V characteristics of the transistor are no longer constant, but dependent on the amount of charge contained in the body of the device at any given time. The charge content of the body, and the distribution of that charge caused by gate, source and drain potentials determine the final behavior of the device. The magnitude of charge contained in the body depends on several factors which include:

- The previous state of the transistor.
- The device architecture (length, width, Si-film thickness...).
- The biases applied.
- The frequency of operation.
- The temperature.

Kink Effect

The ***kink effect*** is a direct consequence of the floating-body effect. It makes the drain current, I_{DS}, to show overshoot when applying a large V_{DS} voltage [BR07]. The charge stored in the body modifies the potential (increases in case of N-MOS), reducing therefore the threshold voltage and leading to a

sudden increase in the drain current. This effect tends to appear for a high drain bias where the charge is injected in the body by impact ionization. If the large drain bias is hold for a long time, more impact ionization would be obtained leading at the end to a higher increase in drain current (positive feedback effect). An example of this effect is represented in Figure 2.6.

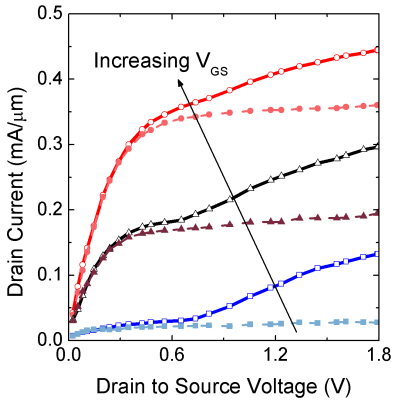


FIGURE 2.6: Kink Effect example due to floating-body effects for the same device with different V_{GS}. Dashed lines show same device without kink effect. It can be appreciated how this effect appears at large drain to source voltages and depends also on the gate voltage applied. For large front-gate biases the kink effect is reduced [BR07].

DIBL

DIBL is one of the short-channel effects that increases more sharply in case of PD-SOI with respect to typical bulk transistors. This effect is related to a decrease in the potential barrier between source and drain due to the influence of the biased drain: the gate losses the electrostatic control when the length of the device is very short leading to a dependence of the threshold voltage with the drain voltage. In PD-SOI MOSFETs the body potential barrier is also modified by the charge accumulation in the body thanks to the FBE. This

means that the threshold voltage depends on two different factors: the drain bias and the charge accumulation, thus DIBL may be overestimated if all the threshold voltage shift is attributed to it [BR07].

2.2. One-Transistor DRAM Cells on SOI based on FBE

In this section it will be detailed how a SOI transistor can operate as a Dynamic RAM cell without an external dedicated storage node thanks to the FBE. These cells are called floating body DRAM.

2.2.1. Floating-Body DRAM Basics

The basic principle of operation of a floating-body cell is to induce a **threshold voltage shift** in a PD-SOI MOSFET. This is achieved by **modifying the population of majority carriers in the body** [ICMM90]. This **transitory shift of the threshold voltage** leads to **two different drain current levels** at a given bias point, Figure 2.7. The '0'/'1' state would be associated to the lower/higher concentration of holes in the body respectively. For example, considering the injection of majority carriers to change the cell state (transient overpopulation of holes), at equilibrium (stable state), the floating-body of the PD-SOI transistor remains slightly charged; this situation defines the '0' state that features the default threshold voltage (solid line in Figure 2.7). The '1' state is forced by charging the body with holes. The consequence of the hole overpopulation after writing '1' is an increase in the potential of the body (V_{BS}) and, thus, a decrease in the front-gate threshold voltage: for the same reading biases, a larger current is then obtained (dashed line in Figure 2.7). **It is important to notice that FB-DRAM cells are**

read based on a current sense and not voltage sense like 1T+1C DRAM cells.

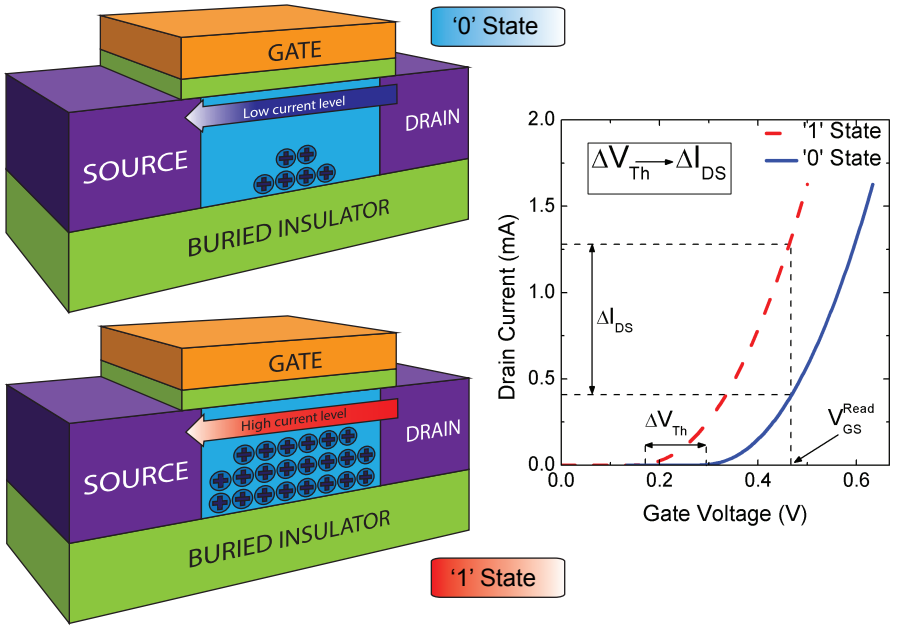


FIGURE 2.7: Basic level discrimination in floating-body DRAM cells. A change in the charge accumulated in the floating-body yields into a variation in the final drain current (for a given and fixed read bias) due to a threshold voltage shift. The arrows in the diagram represent the drain current through the PD-SOI MOSFET.

There exist **several methods to inject, *write* operation setting the '1' state, and to expel, *erase* operation, setting the '0' state, the charge of the transistor**. The most significant are commented below [HBG+10].

Hole injection by Impact Ionization

Impact ionization is a charge injection process. Minority carriers in the body (electrons in NMOS) are accelerated due to an intense lateral electric

field induced by a large V_{DS} [Cri11]. While most of carriers arrive to the drain and scape, a portion of these highly energetic carriers knock electrons from the crystalline net out of their bound state and promote them to a state in the conduction band, creating an **EHP** (*Electron-Hole Pair*) near to the drain. Electrons generated are then evacuated through the drain, while holes are stored into the neutral body of the silicon film, the region with lower potential from where they cannot scape thanks to the buried oxide, Figure 2.8.

As drawback, every **collision may provoke damage in the atomic structure of the device**. This damage accumulates with each new carrier hit during the lifetime of the device and finally means permanent variation in threshold voltage and drain current. In case of PMOS the threshold voltage decreases (being more negative) and the source current drops. On the other hand, for NMOS, the threshold voltage rises and the drain current is also reduced [BR07]. This charging method can induce permanent deterioration in the transistor leading to **reliability concerns** [MN03].

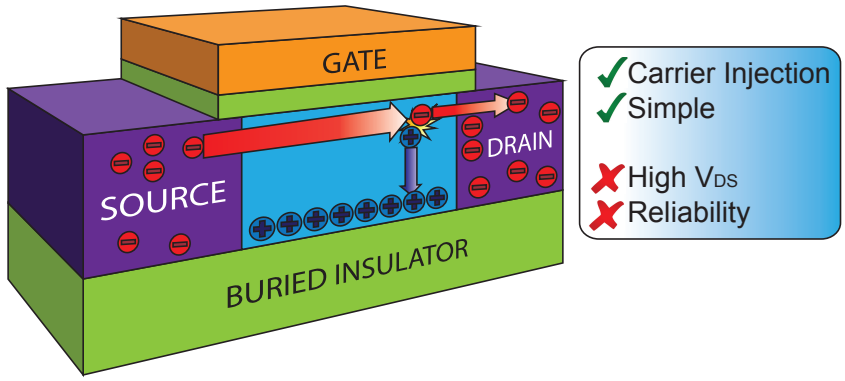


FIGURE 2.8: Example of a N-type MOSFET with impact ionization. Arrows represent the carriers motion. Electrons generated scape through the drain while holes are accumulated in the body.

Impact Ionization enhanced by Parasitic BJT

Instead of using the pure MOSFET operation to sense the cell state, it is possible to take advantage of the intrinsic **bipolar transistor** (NPN BJT) inherent to any MOSFET to program the memory cell. The N^+ source together with the P-type body and N^+ drain form the emitter, base and collector of the BJT respectively. The body of the MOS transistor (base) is used as a storage node. To inject the positive charges into the memory cell, the intrinsic bipolar transistor is triggered forward biasing the source-body junction (emitter-base) with a very large drain to source bias, $V_{DS} >> 0$. This causes a large current to flow throughout all the transistor body, known as volume conduction (emitter current, I_E). This current differs significantly from the MOS-like behavior where current flows only at the front/ back interface in a sheet-like channel. The increased electron drain current, thanks to the volume conduction, makes much more efficient the **impact ionization** resulting in a larger and faster injection of holes (very **short write time**). This impact ionization creates multiple EHP where holes are injected into the body (acting as the base current in a bipolar transistor, I_B) and electrons are collected by the drain (collector current, I_C). A simplified diagram of this behavior can be observed in Figure 2.9.

The holes generated are collected at the back interface since it acts as a potential well (minimum potential across the device) and they cannot scape due to the BOX. As holes are collected, the body potential rises and the drain current increases. This increasing I_{DS} turns into a larger impact ionization rate and hole population contained in the body. The final result is a positive feedback loop of increasing current and hole injection. Although this programming technique enhances the writing speed operation with respect to typical impact ionization, it also presents more remarked **reliability concerns** [CHMC10].

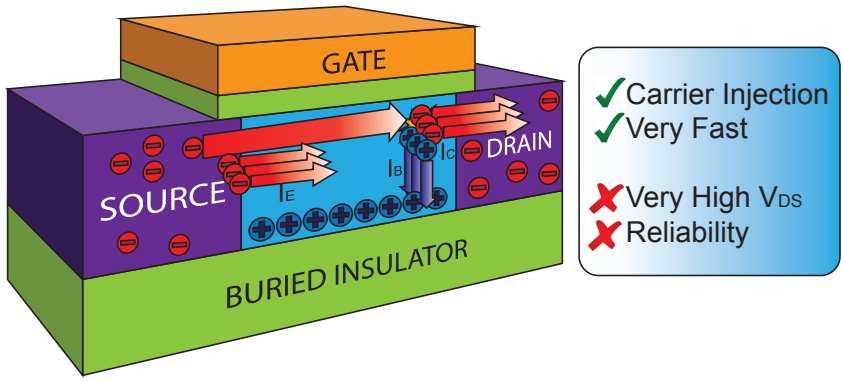


FIGURE 2.9: Diagram of the programming method based on the parasite BJT. Arrows represent the carriers motion. Equivalent BJT currents are labeled: the volume conduction acts as the emitter current, I_E; the injection of positive charge thanks to the enhanced impact ionization results in the base current, I_B; and finally, electrons escaping through the drain emulates the collector current, I_C.

Hole injection by Band-to-Band Tunneling

In silicon, the **BtBT** (*Band-to-Band Tunneling*) process occurs as a consequence of the particle-wave dual behavior of electrons. Because of the non-infinite barrier height that separates the valence and conduction bands, an electron in the valence band of the semiconductor may, with a certain finite probability, tunnel across the forbidden barrier to the conduction band without the assistance of traps generating an EHP [Esa74] (it may be also in the opposite sense). Regarding the carrier injection in a floating-body cell, there are two main processes that leads to BtBT:

- **GIDL** (*Gate Induced Drain Leakage*).
- Gate current.

In a MOSFET the **GIDL** current is a leakage component that appears during the OFF-state operation. It takes place when a large negative voltage is

applied between the gate and drain terminals (high V_{DG}) and the gate overlaps the drain region (it is also possible to use the source instead of the drain with a large V_{SG} voltage). The large bias applied generates an intense vertical electric field in the overlapped region that **bends the energy bands**. If the band bending is larger than the energy band gap, $E_g = E_c - E_v$, the BtBT may take place in the deep depletion drain (or source) region underneath the gate [TI91]. The transistor 3D structure with carriers generated by BtBT and their flux once created are shown in Figure 2.10.

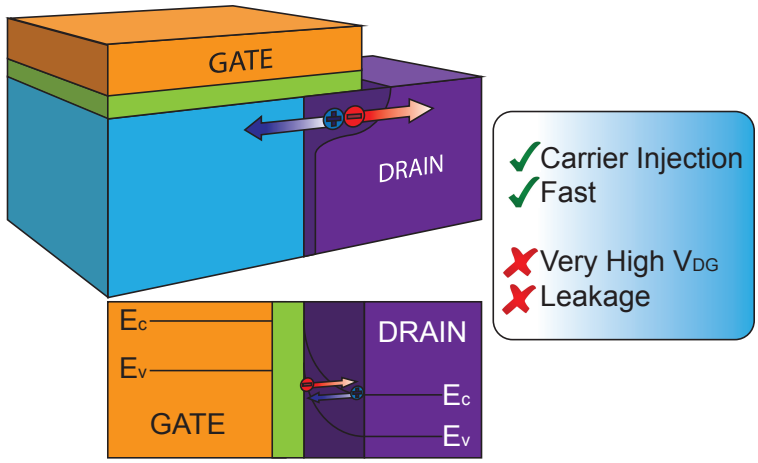


FIGURE 2.10: Diagram of BtBT mechanism induced by the drain bias. The large drain to gate bias bends the energy bands so that electrons from valence band in the drain can tunnel to the conduction band creating an EHP. The hole then moves to the body and the electrons remains in the drain.

The band energy structure is also illustrated in Figure 2.10 with an electron tunneling from the valence band in the drain up to the conduction band (also in the drain) generating an EHP; the hole will move to lower potential regions like the silicon body [ABSV07] while the electron will remain in the drain region. This process depends on temperature, doping concentration,

energy band gap, device structure but specially on the vertical electric field near the drain induced by the biases used [SPS02].

In the case of **BtBT through the gate oxide**, it is necessary to apply a high front-gate voltage. Electrons will tunnel from the valence band in the silicon body across the gate oxide to the conduction band in the gate terminal. This yields to a non-zero gate current I_G that is normally undesired (leakage) for typical transistor operation [RDC06]. The probability to tunnel gets larger as the front-gate oxide is thinned or the gate bias is enlarged. A simple scheme of BtBT through the gate oxide is sketched in Figure 2.11.

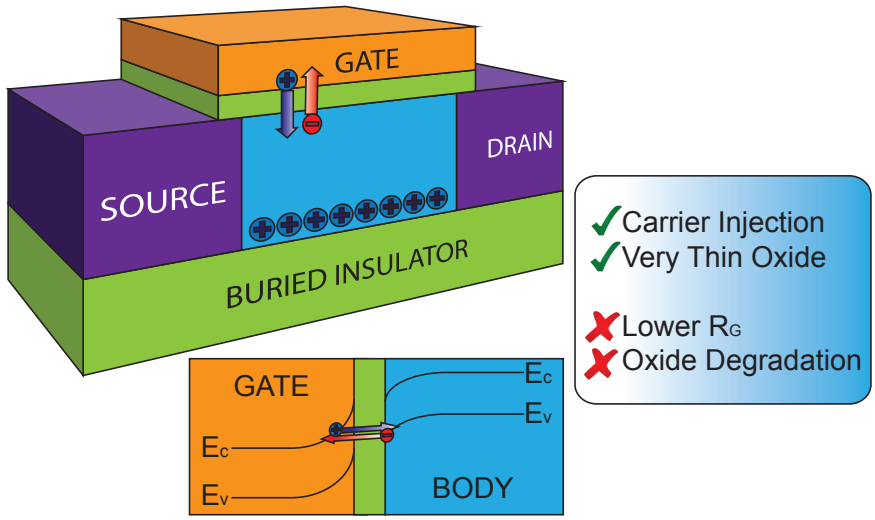


FIGURE 2.11: 3D Structure and Band Energy diagram representation of the BtBT through the gate oxide. The gate bias bends the energy bands allowing electrons in the body to tunnel across the gate insulator generating an EHP.

For $t_{ox} < 3$ nm carriers tunnel through the insulator easily and the gate current rises exponentially. This increase in the gate current affects the power consumption and energy saving [ECB+98]. There exists a **tradeoff between good electrostatic SCEs control and low gate current leakage**. **Gate**

oxide tunneling injection is not often used since it is responsible for the long-term front-gate oxide degradation of the device. Recently, the use of **high-k** materials has contributed to reduce the power waste. These materials are insulators with higher dielectric permittivity than silicon dioxide. They allow the use of thicker gate oxides to obtain a low gate leakage current while maintaining a high oxide capacitance for a good channel control driven by the gate terminal. Nevertheless, these high-k materials typically present worse interface properties than traditional SiO_2. When using different dielectrics materials from silicon dioxide, the **EOT** (*Equivalent Oxide Thickness*) referred to SiO_2 is often employed (Check Appendix A).

Finally, it is worth mentioning that there is also an important consequence regarding the gate oxide tunneling. The existence of this current has motivated the proliferation of the **non-volatile memory** market. These devices use the gate current to program and erase the charge on a 'floating' contact. Some devices such as Flash and EEPROM memories (see Chapter 1) rely on the physics of the tunneling process to work.

Carrier Recombination & Generation

There are several **generation** and **recombination** mechanisms that leads to an increase or decrease in the charge accumulated in the body of the transistor. In silicon, the dominant recombination/generation mechanism is through defects, also called **SRH** (*Shockley-Read-Hall*) recombination [SR52a]. It does not occur in perfectly pure, without defects, materials. SRH is a two-step process as inferred in Figure 2.12. The steps involved are:

1. An electron (or hole) is trapped by an energy state in the forbidden region which is introduced through defects in the crystal lattice. These defects

can either be unintentionally introduced or can have been deliberately added to the material, for example when doping the material.

2. If a hole (or an electron) moves up to the same energy state before the electron is thermally re-emitted into the conduction band, then it recombines.

The rate at which a carrier moves into the energy level in the forbidden gap depends on the distance of the introduced energy level from either of the band edges. Therefore, if an energy is introduced close to either band edge, recombination is less likely as the electron is prone to be re-emitted to the conduction band edge rather than recombine with a hole which moves into the same energy state from the valence band. For this reason, energy levels near mid-gap are very effective for recombination.

For a SOI transistor, the rate of recombination/generation will depend mostly on the PN junction area, silicon film thickness, density of interface states in both $Si - SiO_2$ interfaces, body doping concentration and the charge accumulated in the body.

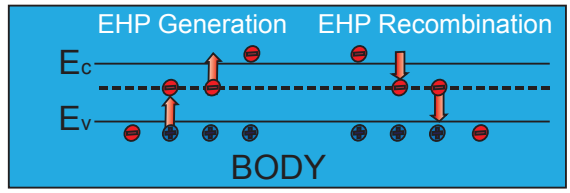


FIGURE 2.12: Simplified four steps diagram of generation and recombination processes through a defect in the middle of the band-gap (SRH).

Other Leakage Currents

There are some undesired currents that may gradually decrease or increase the stored majority charge in the body [RMMM03]. These currents are called **leakage currents** and may be due to several reasons:

- Subthreshold leakage.
- Reverse bias junction leakage.

The **subthreshold leakage** makes reference to the undesired diffusion current a transistor drives in weak inversion when the channel is not yet created, $V_{GS} < V_{Th}$ [SB05]. This current reveals the **non ideality of the transistor as a perfect switch** and depends on the bias applied (specially the gate voltage) and the subthreshold swing. During the switch of the transistor it drives some current. This unperfect behavior leads to a tradeoff between the off current (I_{Off}) to ensure low power consumption, and the current during on state, I_{On}, to provide fast operation. This balance can be appreciated in Figure 2.13 where the benefits of finding devices with higher subthreshold swing are evidenced. **The subthreshold leakage current injects minority carriers into the body (electrons in NMOS) that leads to higher recombination rates reducing the stored hole concentration**. Subthreshold leakage is then detrimental for the cell state with higher concentration of holes in the body ('1' state).

Another important source of leakage comes from **PN junctions**. During typical transistor operation, the two PN junctions, body-source and body-drain (N-type MOSFET), will be reverse biased. The resultant current has two contributions: drift of carriers generated in the space-charge region and drift of minority carriers that wander into the depletion region. All these carriers are swept by the electric field generated by the imbalance of hole-acceptor

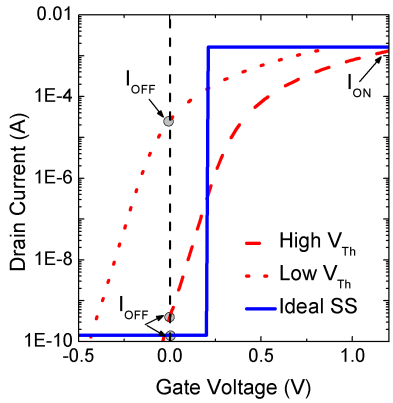


FIGURE 2.13: Comparison between perfect sharp switch (solid line) and $I_{DS}(V_{GS})$ MOSFETs curves for different threshold voltages (dashed for high V_{Th}, and dotted for low V_{Th}). It can be appreciated that lower threshold voltage means higher I_{On} but also higher I_{Off} currents. Meanwhile, an ideal perfect sharp switch benefits from negligible I_{Off} and large I_{On} at the same time[Wan12].

and electron-donor concentration. This electric field makes the carriers to flow across the junction becoming majority carriers. Since few minority carriers are swept, the current will not be therefore very large. In case of SOI transistors the junction area is smaller than bulk devices so the junction leakage is also lower, but not always negligible. For an ideal PN junction, the current is given by Equation 2.2 [SB05]. When reverse biasing, the voltage applied V is negative and the final current approaches the diode saturation current I_s in the opposite sense.

$$I(V) = I_s \cdot (e^{q \cdot V/k \cdot T} - 1) \rightarrow I(V < 0) \simeq -I_s \, [A] \tag{2.2}$$

where I_s, is related to the area of the junction and doping concentrations, as shown in Equation 2.3 [Sch06b].

$$I_s = q \cdot A \cdot \left(\sqrt{\frac{D_p}{\tau_p}} \frac{n_i^2}{N_D} + \sqrt{\frac{D_n}{\tau_n}} \frac{n_i^2}{N_A} \right) \ [A] \tag{2.3}$$

with $D_{n,p}$ and $\tau_{n,p}$ being the diffusion coefficients and carrier lifetimes of electron and holes respectively, $N_{A,D}$ the acceptor or donor doping concentration and n_i the intrinsic carrier concentration in Silicon. **The PN junction leakage current increases the hole injection from the N-type S/D regions, at the same time it helps evacuating minority carriers in the body which also reduces the recombination rate** [SR52a]. So, this leakage is detrimental for the cell state with lower concentration of holes in the body ('0' state) since it enhances the hole population.

Hole evacuation by Junction Forward Biasing through Capacitive Coupling

The previous processes to extract the charge from the body, carrier recombination and PN junction leakage current, are undesired since they cannot be controlled explicitly. The usual way to discharge the body from majority carriers is to bias in forward mode the PN junction/s. In case of N-MOS, to **forward bias** the junctions a positive front-gate voltage is used to increase the potential of the P-type body by capacitive coupling while grounding the drain. Equivalently, the gate remains grounded while a negative bias is applied to the drain and/or source terminals. Doing so, the built-in energy barrier in the junction decreases allowing **majority carriers of both sides to have enough energy to surmount the barrier and diffuse through the S/D regions**. Holes are evacuated from the silicon body which corresponds to a *erase* (*write* '0') operation.

It is important to mention that all the previous methods should be rightly controlled since they usually enhance the performance of one state of the memory cell while degrading the other. For example, the carrier recombination process is detrimental if it takes place when the memory cell is charged with holes ('1' state) because it reduces the hole population and the stability of the high current level; GIDL, on the other hand, is able to inject holes into the body which is undesired if the cell stores the low-charged level ('0' state). **The proper management of the charge inside the body yields into good memory capabilities, e.g., long retention time and large current margin between states** (more details about these parameters will be addressed in Chapter 4).

2.2.2. Types of FB-DRAM Cells

Several companies like Samsung®, Renesas®, Toshiba®, Innovative Silicon® and many universities as Stanford, Seoul National University, INP Grenoble or the University of Granada itself, have studied and proposed alternatives of memory cells designs based on FBE. The main candidates and their history is presented here [RGC]:

Origins of FB-DRAM cells

In 1990, a new phenomenon named **MCCM** (*Multistable Charge-Controlled Memory*), with potential application in the memory field, was reported in **ZMR** (*Zone Melting Recrystallization*) SOI technology [TGCD90] with silicon-film thickness of 450 nm. The back-gate of the SOI transistor was biased in accumulation ($V_{BG} < 0$ V) whereas the front-gate was set close to the threshold voltage ($V_{FG} \simeq V_{Th-FG}$); the drain bias was then swept from $V_{DS} = 0$ V to 7 V leading to different drain current output

characteristics in the first instance compared to the subsequent scans, Figure 2.14.

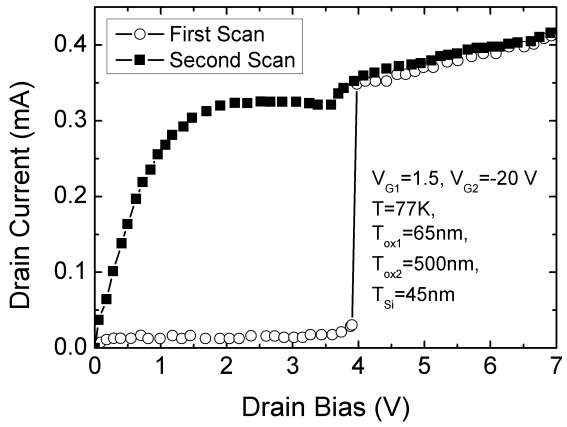


FIGURE 2.14: Output characteristics reported in early ZMR-SOI N-MOSFET operated at liquid nitrogen (77K) [TGCD90]. An abrupt jump of the current, due to non-equilibrium deep-depletion, was observed in the first measured curve [RGC].

The authors in [TGCD90] anticipated that tunneling mechanisms could be used for the fast injection of holes in the floating-body instead of using the impact ionization. One year later, this unexplored alternative was reported by the Berkeley group when they studied the time dependence of fully-depleted SOI MOSFETs subthreshold current [ECS+91]. In their experiments they used a different bias scheme on more advanced **SIMOX** transistors. The front-gate was used for hole accumulation, whereas the back (BOX) interface was biased to a value slightly higher than the back interface threshold voltage ($V_{BG} = 30$ V). They scanned the front-gate bias from $V_{FG} = -8$ V to 0 V trying to create accumulation. The curves obtained were different depending on the scan rate (Figure 2.15). For slow scan rate (3 mV/s), the drain current characteristic was as expected, but the surprising result occurred for fast scan rate (100 mV/s).

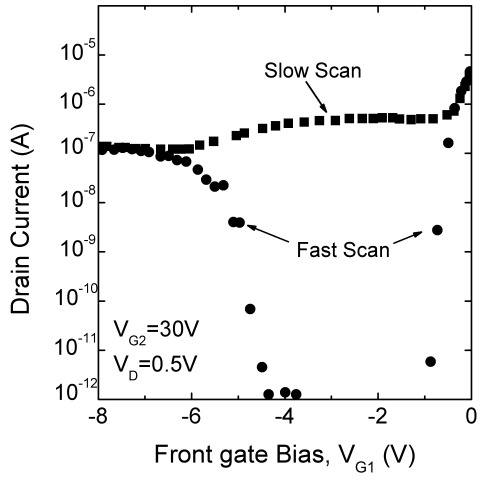


FIGURE 2.15: Experimental drain current as the front-gate bias is scanned and the back-gate bias is set to $V_{BG} = 30$ V with slow (3 mV/s) and fast (100 mV/s) scanning rates. $t_{ox} = 12$ nm, $t_{Si} = 70$ nm and $t_{BOX} = 400$ nm [ECS+91].

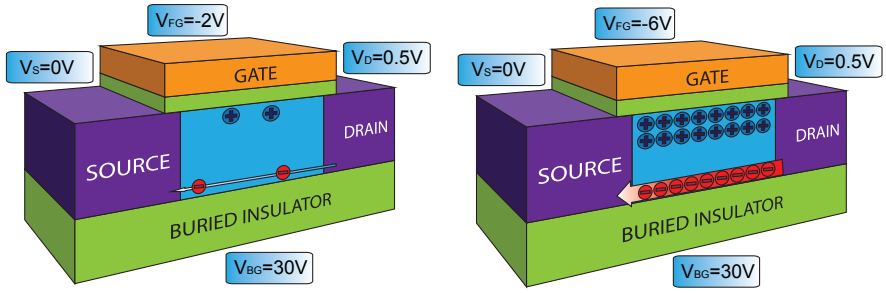


FIGURE 2.16: At the left, the deep-depletion regime at the front-gate interface reduces the minority carrier concentration at the back-interface. In the right, the band-to-band tunneling injection restores the population of holes at the front interface and raises the electrostatic body potential, which enhances the population of electrons at the back-interface and, thus the drain current flow. $t_{ox} = 12$ nm, $t_{Si} = 70$ nm and $t_{BOX} = 400$ nm [ECS+91].

The drain current suddenly drops, and increases again when a certain front-gate bias is reached saturating at the same values as for the slow scan rate. The explanation of this effect is schematized in Figure 2.16. When the front-gate bias is quickly reduced, the potential in the body of the transistor decreases promptly. The source-body and drain-body PN junctions become reverse biased and there is no source to provide the holes immediately, leading to a deep-depletion situation at the front interface. This implies a drop in the electrostatic potential at the back interface, cutting the electron channel. When a negative front-gate bias is reached ($V_{FG} < -4$ V in Figure 2.15), the injection of holes by GIDL starts. The holes accumulate at the front-interface allowing the recovery of the electron concentration at the back interface (and therefore an increase in the drain current, Figure 2.16 at the right).

Despite the attractive hysteresis window obtained by these mechanisms, this time dependence of the subthreshold current was not consider for memory applications until several years later. It was then renamed as **MSDRAM** (*Meta-Stable-Dip RAM*) [BCYF05, BCF06].

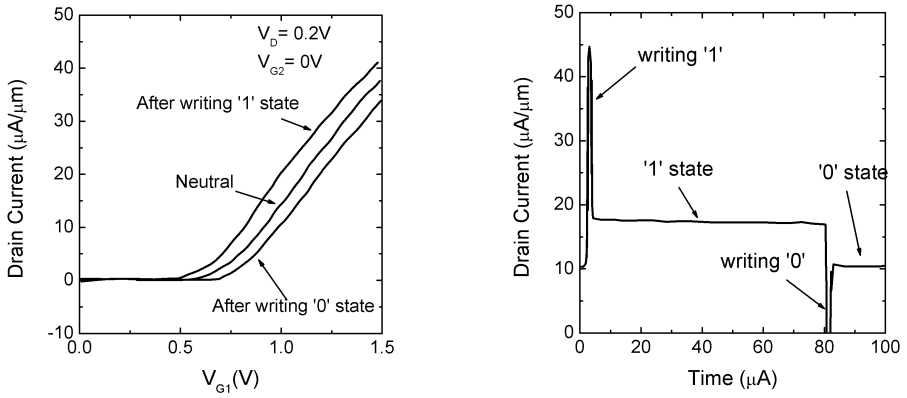
The retention time in the MSDRAM is governed by the parasitic repopulation of the front and back-channels. In long-channel devices the repopulation is mainly produced by slow parasitic thermal generation achieving retention times over 1 second and several orders of magnitude in current margin between states '0' and '1'. In case of short devices, the front-gate oxide scaling, to deal with the short-channel effects, enhances the injection of holes by BtBT. This injection is much faster than the thermal generation which leads to a decrease in the retention time for short devices [RGM$^+$13]. Nevertheless, the MSDRAM shows attractive performance in short devices if the film thickness is maintained above 25 nm [BCF08, HBG$^+$11].

Z-RAM and Z-RAM second generation (Z-RAM2)

The rise of the research activity around the FB-DRAM concept arrived with the birth of the start-up company Innovative Silicon® in 2003. By the end of the 90's, the UNIBOND® process for wafer production had contributed to the SOI technology as a huge step forward in terms of mass production, material quality and film scalability [Col04]. The idea of a FB-1T-DRAM memory cell resuscitated under the name of **Z-RAM** cell (*Zero Capacitor RAM*) [ONSF01, ONSF02, FSP06]. It was a more natural approach for the DRAM substitution since there was no need for a back-gate bias. With the standard DRAMs cell affected by the everytime more complicated three-dimensional trench or stacked capacitors [MDB+02], the Z-RAM promoted hope for future directions of the DRAM industry.

The Z-RAM was pretty much based on the overpopulation of holes in the floating body of the device (rather than on the creation of a deep depletion state). It was formed by a PD-SOI transistors where the threshold voltage is shifted to obtain two different current levels due to either the excess or the absence of holes in the floating-body of the transistor. The holes were injected by impact ionization using a large drain bias when the channel is inverted ($V_{FG} = 0.8$ V, $V_{DS} = 2$ V. Excess holes lower the threshold voltage ('1' state in Figure 2.17 **(a)**). The use of a large drain bias was always seen as a potential drawback for Z-RAM due to reliability concerns.

The holes were removed by forward biasing the body-drain PN junction by capacitive coupling; after the evacuation of the positive charge, the floating body remains depleted of holes, increasing the threshold voltage of the transistor ('0' state) above the value at thermodynamic equilibrium ("neutral" in Figure 2.17 **(a)**).



(a) Threshold voltage shift (b) Z-RAM transient response

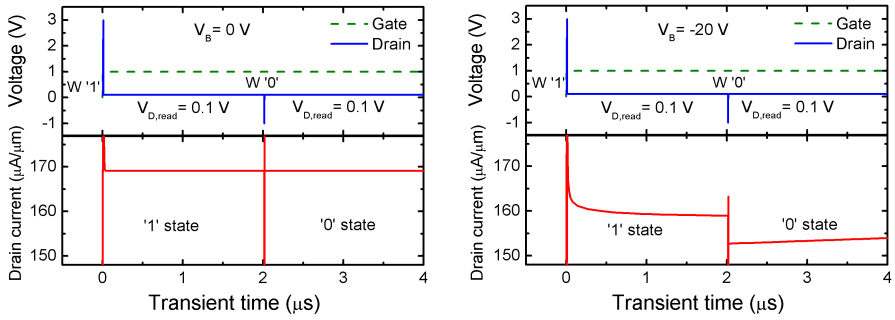
FIGURE 2.17: **(a)** Measured $I_{DS}(V_{FG})$ curves in a SOI transistor ($L = 0.5\ \mu m,\ W = 0.5\ \mu m$) showing the V_{Th-FG} variation due to the presence or the absence of charges in the floating body [ONSF01]. **(b)** Measured drain current demonstrating Z-RAM memory effect with two levels of current in a PD-SOI transistor ($L = 0.25\ \mu m$, $W = 0.25\ \mu m$). For writing '1' $V_{FG} = 0.8$ V and $V_{DS} = 2$ V; for writing '0' $V_{FG} = 0.8$ V and $V_{DS} = -2.2$ V; states reading at $V_{FG} = 0.8$ V and $V_{DS} = 0.5$ V [ONSF02].

The transient evolution of the readout drain current of the transistor after writing '1' and '0' states is shown in Figure 2.17 **(b)**. In the best cases Innovative Silicon® reported a current margin around 10 $\mu A/\mu m$ for Z-RAM cells based on large transistors.

Soon, the use of relatively thick transistor body (PD-SOI) started to be seen as a burden for the survival of the floating-body 1T-DRAM memory as the SOI community was pushing in the direction of SOI transistor with thin or ultrathin fully depleted bodies. Retention time, current margin and variability of FB-1T-DRAMs were not competitive enough to contest the 1T+1C DRAM from its throne in the semiconductor industry [HO08].

In order to reconcile the FB-1T-DRAM with the fully depleted technology the use of back-gate bias became a standard solution to store the holes in the

body of the transistor, creating a dedicated potential well [BA07]. An example of the viability of FB-1T-DRAM based on FD-SOI substrates is shown in Figure 2.18, where results of numerical simulations are presented corresponding to a sequence consisting of: writing '1' event followed by reading of 2 μs; writing '0' event, followed by reading of 2 μs. In Figure 2.18 **(a)** the substrate of the FD-SOI transistor (back-gate) is biased at $V_{BG} = 0$ V, whereas in Figure 2.18 **(b)** a back-gate bias of $V_{BG} = -20$ V has been used to create a potential well to accumulate the holes at the back interface.



(a) No memory effect ($V_{BG} = 0$ V) (b) Memory effect ($V_{BG} = -20$ V)

FIGURE 2.18: Simulation results of the operation of a Fully Depleted FB-DRAM. The bias pattern is shown on top of the figures whereas the driven current at the bottom. In **(a)** the substrate is biased at $V_{BG} = 0$ V; due to lack of floating-body effect there is no accumulation of holes and the readout current remain always the same. In **(b)** a back-gate bias is applied creating a potential well where the holes can be stored, producing a shift in the threshold voltage between the '1' and '0' states. $V_{FG} = 1$ V, $V_{DS} = 3$ V (writing '1'), $V_{DS} = -1$ V (writing '0' or erase), $V_{DS} = 0.1$ V (reading states). $L = 200$ nm and $t_{Si} = 70$ nm.

As observed, without the negative back-gate bias the memory effect is not manifested: the holes created by impact ionization during the writing '1' event recombine so quickly that the difference in current between states is no noticeable in this time scale. By contrast, if a back-gate bias is applied (Figure

2.18**(b)**), the accumulation of the majority carriers at the back-interface creates the two levels of current defining the '1' and '0' states.

A breaking approach was introduced in 2007 by Innovative Silicon®: the **bipolar triggering of the device** was utilized to create two different states as anticipated in [OGB+91]. This memory cell, named **Z-RAM generation 2** [ONC+07], attracted the interest of different semiconductor companies since the current margin and retention time was greatly enhanced with respect to the first generation [ECC+07]. Writing state '1' is based on the parasitic BJT volume conduction for injecting the positive charge by impact ionization. The '0' state is written by removing the holes from the storage node (forward biasing the drain-body junction). When the body does not accommodate accumulated holes, the bipolar action cannot be triggered using the same reading bias conditions, thus obtaining different current levels. The read operation is performed with negative gate voltages to check whether the BJT effect is active or not. The current margin is relatively larger than in competing FB-counterparts, but in contrast (for a given device dimensions) the large bias values required for the parasitic **BJT operation introduces reliability, cell disturbance, and power consumption issues**.

Z^2-FET

The **Z2-FET** is a recent device that shows attractive FB-1T-DRAM performance [WLZC12] based on **field effect-controlled charge regeneration**. It is actually a forward-biased PIN diode, where the fully depleted body is partially covered by the gate (Figure 2.19). The front and back-gates are biased such as to form potential barriers preventing the injection of electrons and holes from the N and P contacts respectively. The gate biasing emulates a thyristor configuration without needing any body doping concentration; front-gate is biased negatively to accumulate holes while

a positive voltage is used for the back-gate to collect electrons (there exists a variant where positive charges are injected in the uncovered region of the front-oxide to avoid the requirement of a back-gate bias).

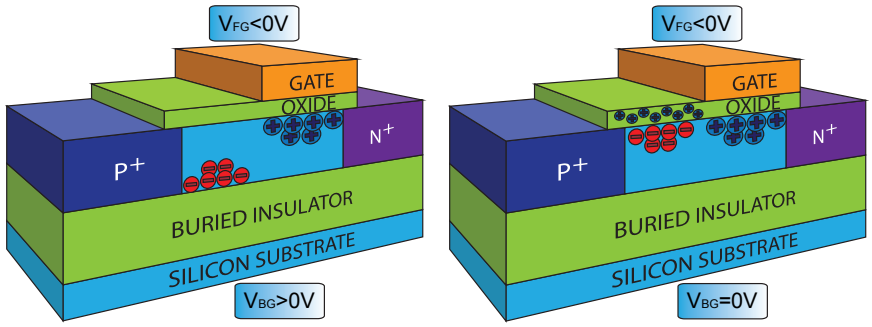


FIGURE 2.19: Diagram of the Z2-FET DRAM cell. There exist two different schemes, with back-gate biasing and without back bias (it uses trapped charge in the oxide).

The current remains low until V_{DS} increases enough to lower the electron injection barrier. Electrons injected from N contact into the channel flow to the source where they reduce the hole injection barrier. The holes flow from source to drain, causing positive feedback that turns on the device and eliminates the injection barriers. This mechanisms results in a strong $I_{DS}(V_{DS})$ hysteresis which is gate controlled and useful for capacitor-less memory. The states '1' or '0' are programmed by storing or not holes under the gate. Memory reading consists in discharging the gate. In '1' state, the discharge current is sufficient to turn on the Z^2-FET and the read current is high. In '0' state, there is no discharge current, hence the diode remains blocked (negligible read current). Very fast read pulse (1 ns) enables to minimize the amount of stored charge requested to trigger the device. The memory is scalable down to 30 nm gate length and offers **long retention time and regenerative (non-destructive) reading** [Wan12].

SGVC cell

The **SGVC** (*Surrounding Gate Vertical Channel*) cell was designed by Samsung [JSP+07]. An interesting characteristic is that its fabrication is feasible in both SOI and bulk substrates. It shows a very unusual vertical structure with the **gate surrounding all the body** of the transistor, as a gate-all-around silicon nanowire transistor [HWZ+11], with the source being shared between all cells. Since the body is isolated with the surrounding gate, **no buried oxide is required to achieve the floating-body effect** in the cell. A simple representation of this memory appears in Figure 2.20.

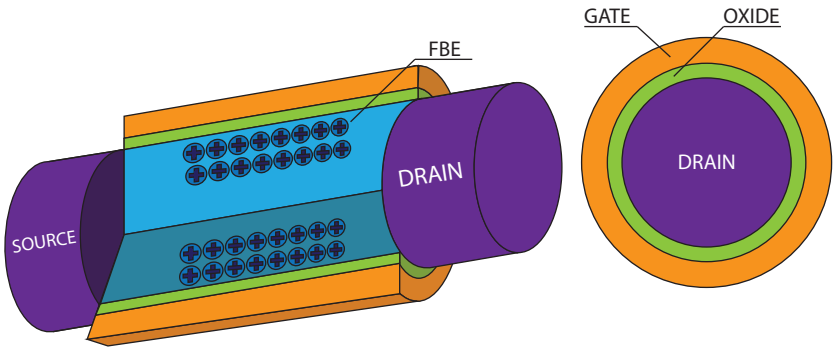


FIGURE 2.20: Diagram of the SGVC FB-1T-DRAM memory cell designed by Samsung [JSP+07].

The operation of this cell is similar to the previous $Z - RAM^2$ based on FBE, but the charging methods are impact ionization or GIDL.

Multi-body FB-1T-DRAMs

One of the questioned drawbacks of FB-1T-DRAMs is their scalability. In conventional transistor + capacitor memory cells, the bit of information relies in the amount of charge stored or consequently in the volume or area devoted to

this storage. Unfortunately, the scaling of FD-SOI transistors requires ultrathin film in order to suppress short-channel effects [CL95, Col04]. In the case of single-gate SOI MOSFET, the film thickness should follow Equation 2.4 [Dor11] (this condition can be relaxed to a factor of three in the case of double-gate devices).

$$L > 4 \cdot t_{Si}\,[cm] \tag{2.4}$$

This means that FB-1T-DRAMs have to be **compatible with body thicknesses below 10 nm** for competitiveness in future technology nodes. The condition involves a serious challenge for the FB-1T-DRAM family. Several studies have shown severe degradation in the margin between states when the body thickness decreases below 30 nm [ABKC08]. The first issue resides in obtaining such **thin silicon films on insulator with good uniformity**, which turns to be very challenging. *Quantum confinement* effects appear for silicon films of around 5 nm causing the threshold voltage to increase geometrically with decreasing Si film thickness. This makes the threshold voltage very sensitive to variations in silicon film thickness [ECG+03] which turns in high variability in the memory response. Second, the *parasitic series resistance* increase associated with the use of ultra-thin source and drain regions. A possible solution is achieved by thickening the source and drain regions via selective epitaxial growth (RSD), thus reducing the parasitic resistance but at the cost of increasing the gate to source and drain capacitances [KML05]. Metallic source and drain regions may also be used [CNM+09] for further lowering the series resistance but special care should be taken due to *schottky contacts* formation. Third, there is the need for **ultra-thin BOX** substrates to allow low back-gate threshold voltages and effective dynamic front-gate threshold voltage control by using a **GP** (*Ground-Plane*) [OSH07].

The disadvantage for the GP is the cost of increased source and drain junction capacitances.

Recent progress in the manufacture of SOI substrates leads to **UTBB** (*Ultra-Thin Body and BOX*) devices with uniform thin SOI and thin BOX film structure (t_{BOX} = 25 nm or even 10 nm). This has enabled successful demonstrations of nano scale FD-SOI devices [DBD+09]. In Figure 2.21 the thickness variability in a group of more than 130 wafers is shown. It can be seen how the maximum and minimum thickness across all the wafer vary less than 5 Å from the thickness targeted, ensuring low variability.

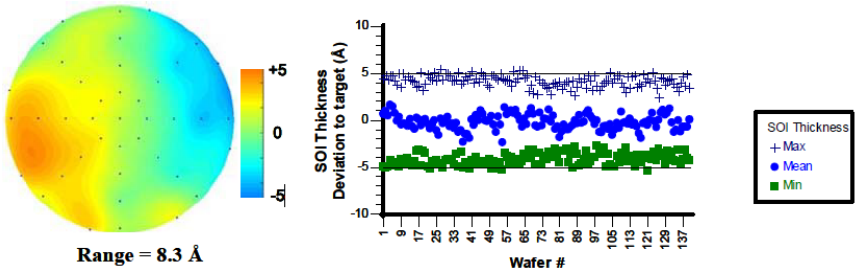


FIGURE 2.21: Experimental data of silicon film thickness variability in the wafer, left, and from wafer to wafer, right. The peak to peak variation is always lower than 1 nm [DBD+09]. Courtesy of Soitec®.

But the main issue for scaling FD-SOI transistors and use them as memory cells is how to deal with an ultra-thin silicon film where the **supercoupling effect** [ECC+07] takes place. This undesired effect **inhibits the formation of an accumulation layer facing the inversion channel in ultrathin SOI**. It appears when the silicon film is thinner than the *critical film thickness*, t^*_{Si}, defined in Equation 2.5 as a 1D model (no lateral influence is taken into account).

$$t^*_{Si} = \frac{k_B T \cdot \epsilon_{Si}}{qC_{BOX}(V_{FB-BG} - V_{BG})} ln\left[\frac{N_A C_{ox} C_{BOX}(V_{FB-BG} - V_{BG})}{q\epsilon_{Si} n_i^2}\right] \; [cm] \tag{2.5}$$

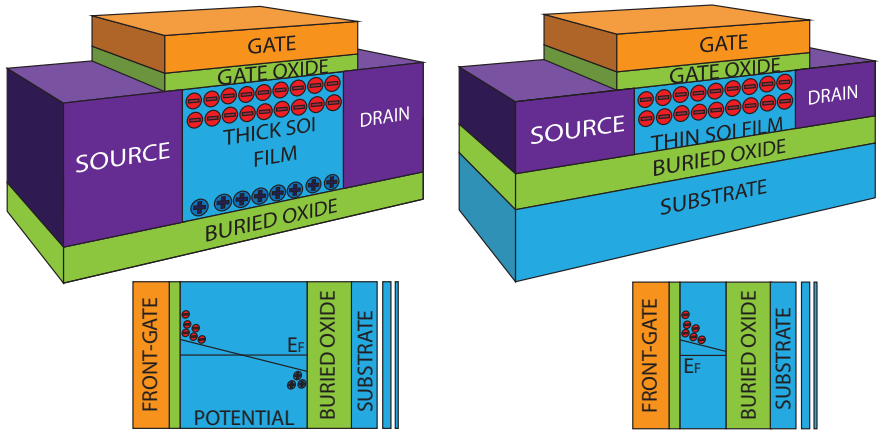


FIGURE 2.22: Body potential comparison between thick and thin SOI film structures. The Supercoupling effect appears for ultra-thin SOI transistors where the potential in the body does not drop enough to allow hole accumulation at the back interface.

The *supercoupling* effect imposes the minimum Si-film thickness in fully depleted SOI devices where the coexistence of a front inversion channel and a back accumulation charge layer can be held simultaneously. In films with sub-critical thickness, $t_{Si} \leq t^*_{Si}$, the potential across the silicon slab does not drop enough to allow large concentrations of electrons and holes at opposite interface, Figure 2.22. The potential appears then to be almost flat, the Si-film behaves as a *rigid quasi-rectangular well*: when the potential at one interface is modified by the dominant gate, the potential of the entire silicon film follows. This implies that the coupling between back and front interfaces is so strong that it becomes **impossible to electrically characterize one channel independently of the opposite by screening the interface effects via accumulation** [CL95].

In order to overcome this intrinsic limitation and maintain the retention and sensing margin performances despite the scaling of the film thickness, several architectures and material have been proposed. The main idea behind

them is the separation of the stored majority carriers and the sensing minority carriers by creating dedicated volumes (potential wells) inside the transistor body. These are the **multi-body cells**.

Figure 2.23 shows two examples of architectures proposed to suppress the supercoupling effect. On the left, the **single-transistor QW** (*quantum well*) 1T-DRAM [EKS08], uses an engineered body integrating within the Si film a thin layer of a material with a lower band gap (i.e., SiGe). This layer serves as storage well for holes. It was theoretically demonstrated that this structure improves the current sensing margin and scalability characteristics. Compared with other FB-DRAM designs, this QW memory has the advantage of storing the holes closer to the front-gate inducing an enhancement in the V_{Th} shift and retention time. As the QW devices are more scalable thanks to the introduction of the extra "storage room", the effect of the volume reduction with the channel length is lessened.

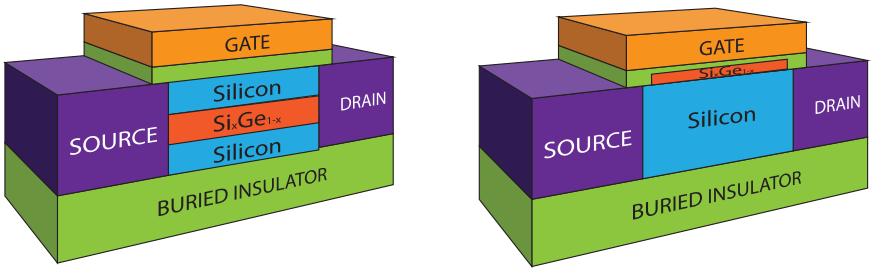


FIGURE 2.23: Examples of multi-body 1T-DRAM cells. On the left, the QW 1T-DRAM where the holes are stored in the potential well created by the Si-Ge layer [EKS08]. On the right, Convex channel 1T-DRAM, the holes are stored in a SiGe layer created into the gate-stack [CSL09].

The performance of this structure can be enhanced by using GaP raised Source/Drain (RSD) regions [PNGS12], which can be either implemented in a planar SOI or FinFET process flow. For the same gate length, the RSD structure has higher volume to store the charge inside the body. Finally, GaP

has a much higher bandgap than Si providing a better hole confinement and hence improving the retention time.

The **convex channel 1T-DRAM** structure (Figure 2.23 on the right), using the bipolar based programming technique, was proposed in [CSL09] to improve the retention time. The holes are stored beneath a raised gate oxide which may be filled by a smaller bandgap material (e.g. SiGe). As the holes stored during the 1-state programming reduce the body/source(drain) potential barrier, they easily diffuse through these junctions filling the SiGe region. The convex channel architecture provides a physical well for more effective storage of holes. Moreover, if a narrower bandgap material is used in the convex channel region, a deeper potential well is formed further improving the sensing margin and retention time.

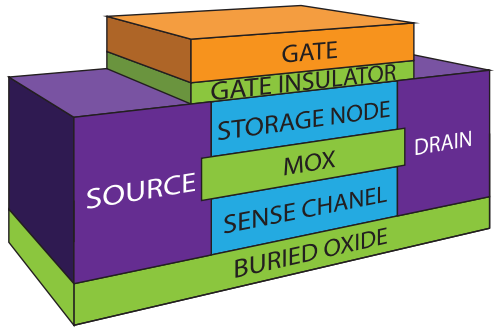


FIGURE 2.24: Structure of the FB memory A-RAM. Notice the innovative multi-body concept achieved by the partition of the Si-film by using an extra oxide layer (MOX).

Another alternative, the **A-RAM** (*Advanced RAM*) was proposed in [RGC10] by physically dividing the body of the transistor into two isolated regions. The body partition is achieved by using an intermediate silicon dioxide layer in the body named **MOX** (*Middle OXide*), Figure 2.24. In order to take advantage of this structure the MOX must present a **dielectric constant smaller than silicon**, using for example SiO_2. When this device is operated

as a memory cell the top semibody is used for majority carrier storage (holes) accommodated in a potential well created by the negative bias of the front-gate, *storage node*. The bottom semibody serves to sense the device state via the minority carrier current, *sense channel*. The low-k MOX constitutes the key advantage of this device: the electrostatic potential difference between the front and back interfaces is enlarged due to a higher electrostatic potential drop through the MOX.

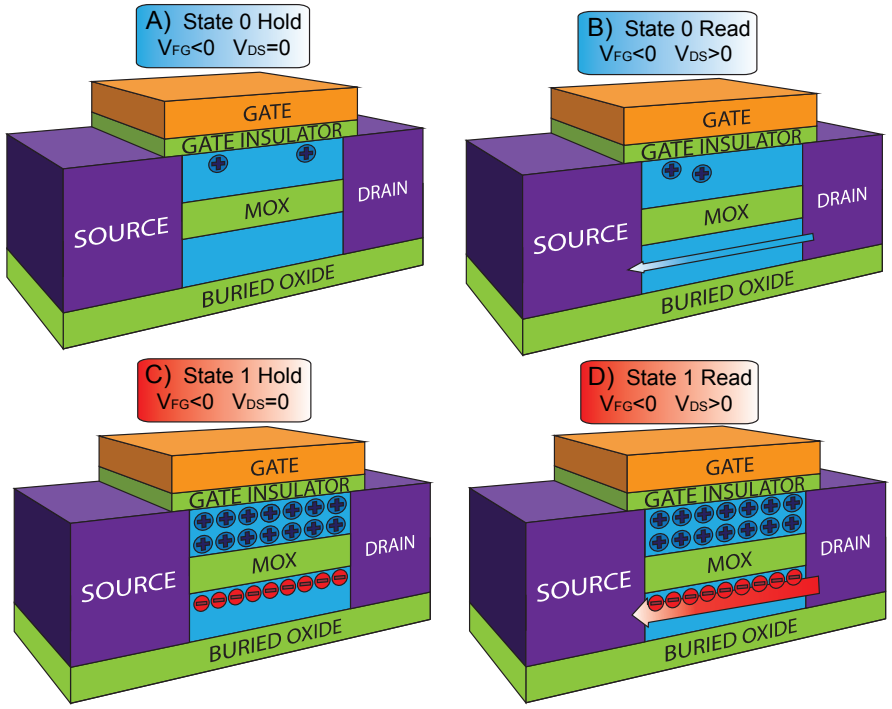


FIGURE 2.25: Structure of the FB-DRAM memory A-RAM under operation. A front negative bias is needed to ensure the hole accumulation in FD-SOI devices. A) No significant hole concentration in the storage node avoids the sense channel to be created, when a drain bias is applied , B) a negligible current is driven through the sense region. C) Charge accumulated in the storage node allows the creation of the channel below the MOX layer. When increasing the drain bias, D) a large current flows across the body in the sense region. Arrows represent the current flow.

The fundamental idea is to accumulate (or not) charge in the storage node (a negative front-gate bias is applied to ensure the carrier retention in a potential well) to modify the current driven through the sense channel. When the '0' state is written after the *erase* operation, no significant amount of carriers are stored so that no channel is created by coupling in the sense layer under the MOX. This state defines the low current level of the memory, Figure 2.25 **(A)**. To *read*, a low bias can be applied to the drain and sense the current, Figure 2.25 **(B)**, which will be almost zero or negligible since no electron channel is formed. The *write* of the high current state on the other hand, is achieved by injecting majority carriers by impact ionization or BtBT (GIDL). Once the charge is injected, it will not scape due to the middle oxide and the front-gate negative bias. The positive charge accumulated will act as a front-gate in a transistor inducing a channel below the MOX, Figure 2.25 **(C)**. Increasing again the drain bias will turn into a much higher level of current driven through the sense channel as shown in Figure 2.25 **(D)**.

But ARAM memory cells also have an important drawback, these cells introduce new fabrication steps to deal with the MOX layer. Nevertheless, it is realistic and feasible. There are several technological possibilities already available to achieve the fabrication of the MOX [RCG11a]:

- **SON technology**: the process starts with a regular SOI wafer, where the ultrathin Si film forms the lower semi-body. A patterned sacrificial SiGe layer (which will be converted in MOX) and the upper semi-body Si film are epitaxially grown. Subsequent SiGe etch leaves a cavity to be refilled with the MOX dielectric [JSP+00].
- **ELO** (*Epitaxial Lateral Overgrowth*): the MOX is formed by local deposition or oxidation on the bottom semi-body. The epitaxial regrowth of the upper semi-body and source/drain regions is enabled by the bottom Si layer which serves as a seed. Since the epitaxial growth proceeds in

vertical and lateral directions, a subsequent thinning of the upper body might be necessary [Neu90].

- **ZMR**: this variant is similar to ELO except that the upper semi-body is deposited on the MOX. The conversion from poly-silicon into crystalline Si is achieved by local melting using lamps or lasers [Cel83]. In both ELO and ZMR approaches, the area of the upper semi-body should be small enough in order to avoid grain boundaries and related issues [CL95]. This condition is easily satisfied by the ARAM cell which is meant to be very small.

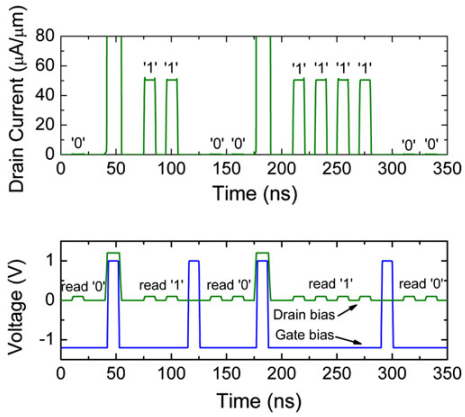


FIGURE 2.26: Simulation waveforms demonstrating A-RAM functionality. Read of the drain current (top). Drain and gate voltage signals during operation (bottom). $t_{ox} = 2$ nm, $t_{Si-total} = 20$ nm, $t_{MOX} = 4$ nm, $L = 100$ nm [RCG11a].

The functionality of A-RAM as memory cell was demonstrated by numerical simulations (Poisson + continuity equations) [RCG11a]. In Figure 2.26, a typical reading/writing sequence is shown. At $t = 0$ s, the cell is in '0' state. The cell state is read by slightly increasing the drain voltage from $V_{DS} = 0$ to 0.1 V.

At $t \simeq 50$ ns, the '1' state is written by impact ionization filling the ultrathin top storage node with excess holes in a few nanoseconds. To do so, a gate voltage pulse is embedded in a drain voltage pulse; this guarantees that the longitudinal electric field remains high when the gate bias returns to its negative retention value: the generations of holes is maintained as long as the electron channel subsists, limiting the electron-hole direct recombination.

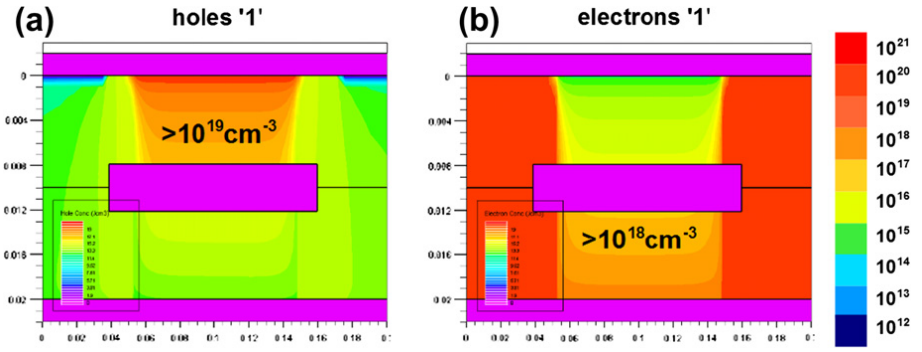


FIGURE 2.27: A-RAM 2D **(a)** Hole and **(b)** electron concentration during state '1'. $t_{ox} = 2$ nm, $t_{Si-total} = 20$ nm, $t_{MOX} = 4$ nm, $L = 100$ nm [RCG11a].

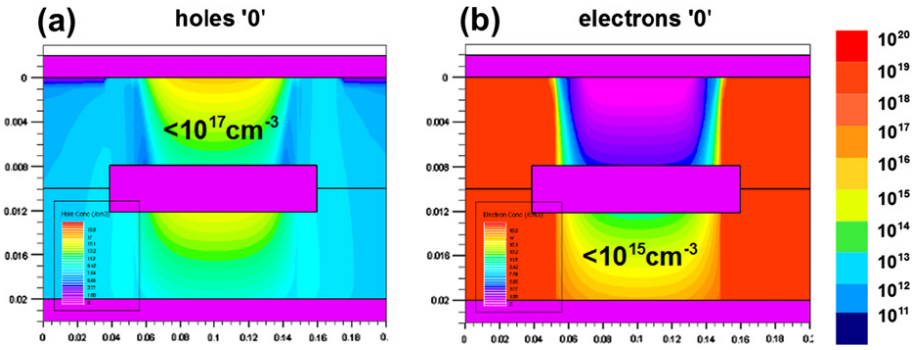


FIGURE 2.28: ARAM 2D **(a)** Hole and **(b)** electron concentration during state '0'. $t_{ox} = 2$ nm, $t_{Si-total} = 20$ nm, $t_{MOX} = 4$ nm, $L = 100$ nm [RCG11a].

The cell state is read at different times by increasing the drain voltage to 0.1 V. The drain current signals in the '1' state are hardly modified. At $t \simeq 125$ ns, the '0' state is written by pulsing the gate voltage from negative to positive value and grounding the drain. The holes are eliminated by the source and drain junctions due to the sudden increase in the body potential; when the gate returns to negative voltage, the top body enters into **deep depletion**. Increasing again the drain voltage to sense the cell state leads to subthreshold currents.

The 2D electron and hole concentrations at $t = 75$ ns (holding '1' state, Figure 2.27) and $t = 130$ ns (holding '0' state, Figure 2.28) reveal the charge distinction between the two states. As observed, the carrier concentration difference between '1' and '0' is in the range of two/ three orders of magnitude.

In Figure 2.29, the electron current density of the cell is shown when the states **(a)** '1' and **(b)** '0' are read. The peak current density for the '1' state is over 100 times larger than for the '0' state. A low/medium value of the drain voltage is mandatory to read the cell state; reading at high drain voltage may cause parasitic impact ionization in the sense channel or GIDL in the drain-to-gate overlap region destroying the information.

So far, some examples of memory cells without an external capacitor have been shown. Each of them may be improved by using some design tricks to enhance its performance: increasing the retention time, the current margin, improving its scalability... In the next section some of these performance boosters are presented.

2.2.3. Improvement Trends on FB-1T-DRAM Cells

Some improvements may be adopted to enhance the memory properties. The main of them are:

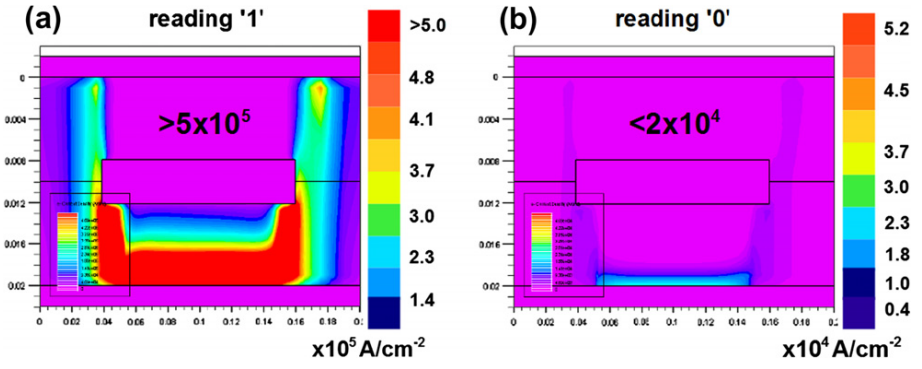


FIGURE 2.29: A-RAM electron current density while reading the **(a)** '1' and **(b)** '0'. $V_{DS} = 0.1$ V, $t_{ox} = 2$ nm, $t_{Si-total} = 20$ nm, $t_{MOX} = 4$ nm, $L = 100$ nm [RCG11a].

Reducing PN Junction Cell Leakage

By reducing the PN junction leakage, the unstable low memory state is maintained for longer time (lower parasitic injection of holes). There are several options such as:

- Non overlapping the gate to source/drain regions [SJL$^+$08].
- Reduce the doping concentration in the body [ECKS08].
- Use thinner silicon films [TLE$^+$08, ES10].
- Use SOI layer to create a trench to enhance the charge accumulation [TLE$^+$08, CLE$^+$10].
- Use silicon with partially insulating layer on SOI [LC11].
- Reducing the electric field at the junctions by reducing V_{GS} or/and increasing t_{ox} [ES10].
- Avoid cell-to-cell leakage by silicide at source an drain regions [HFH$^+$10]

The non-overlap of the source and drain regions with the gate reduces the band-bending in the source and drain edges below the gate oxide. In this way the parasitic band-to-band tunneling injection of carriers is reduced. With lower doping concentration in the body, the junction leakage is also reduced due to lower amount of minority carriers drifting to the source and drain regions from the body and vice versa. This also improves the variability of the threshold voltage due to a decrease in RDF. The third option, thinner Si-films, reduces the PN junction area making smaller the PN junction saturation current (see Equation 2.3). Using side walls, Figure 2.30, also limits the PN junction area and enhance the accumulation of charge in the body.

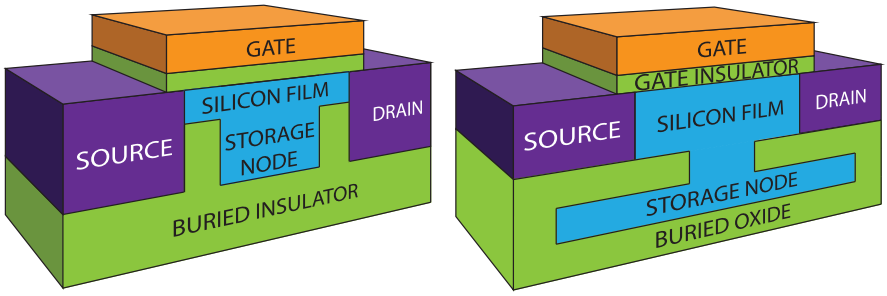


FIGURE 2.30: Scheme of two FB-1T-DRAM transistors with SiO_2 walls [TLE+08] (left) and silicon with partially insulating layer on SOI [LC11] (right) to enhance the charge accumulation in the body.

The use of these methods has also some important drawbacks to mention. For example, non overlapping the gate to source/drain regions reduces drastically the GIDL program mechanism limiting therefore the charging method to impact ionization or gate tunneling. Decreasing the doping concentration further extend the depletion regions near source and drain leading to more sensitivity to SCEs. Thinning the silicon film increases the **SRE** (*Series Resistance Effect*). Using SiO_2 walls consumes the BOX and it is only possible with thick buried oxides and PD-SOI transistors, thus decreasing its scalability and introducing more complexity in manufacturing process.

Increasing Sense Margin

Some of the methods that can be used to enhance the margin between memory states are:

- Use SiGe channel super-lattice [LSJ+11, SBJ+11].
- Combine SiGe with GaP raised source/drain (RSD) [PNGS12].
- Use strain in silicon [KC09]
- Enhance the body coefficient [BA07].

The use of SiGe (*Silicon-Germanium*) channels (as the multi-body cells) creates regions with lower energy band-gap than silicon. These regions have higher valence band edges or equivalently deeper potentials wells where it is easier to store holes enhancing the floating-body effect. Another way of increasing the storage of holes is to employ raised source and drain terminals, which also benefits the series resistance. By doing so, holes are farther from source and drain regions and at the same time the body gets larger allowing more holes to accumulate. Other alternative is to increase the dependence of the threshold voltage with the internal potential in the body. This can be improved increasing the **body coefficient** of the cell given by Equation 2.6 [ECKS08, BA07, HKH02]. The body coefficient of the cell express the sensitivity of the gate threshold voltage, V_{Th}, to changes in the quasi-floating body potential, V_{BS}, thus, to the charge accumulated inside the silicon film. A memory cell with a high body coefficient will require less charge (holes) inside its body to produce a similar shift in the threshold voltage compared to another memory cell with a lower body coefficient. Observing 2.6, it suggests to increase the thickness of the front-gate oxide or to decrease the silicon film thickness to enhance this sensitivity to the charge accumulated. Augmenting the body

coefficient has also an obvious and undesired effect, the cell also becomes more sensitive to undesired body charging/dischargin processes.

$$\frac{dV_{Th}}{dV_{BS}} = \frac{dV_{Th}}{dV_{FG}} \cdot \frac{dV_{FG}}{dQ_{inv}} \cdot \frac{dQ_{inv}}{dV_{BS}} = -\frac{C_{Si}}{C_{ox}} \simeq -3 \cdot \frac{t_{ox}}{t_{Si}} \text{ [-]} \tag{2.6}$$

Others Alternatives

Finally some other improvements are:

- Reduce the buried oxide thickness [Cho11].
- Asymmetrical doping [MVP+09].

Reducing the buried oxide thickness increases the capacitance, thus improving the control of the charge stored in the cell. Finally, by using an asymmetrical implantation (larger doping in the source than in the drain), FB cells based on the parasitic BJT will enhance the emitter efficiency and beta gain factor achieving a better performance while programming and reading.

2.3. Conclusions

In this chapter, the silicon-on-insulator technology has been presented. Thanks to the isolation provided by the use of the buried oxide, SOI allows to accumulate charge in the body of a transistor, this is the so called floating-body effect. Charge accumulation is the key to allow the operation of a single SOI transistor as a FB-DRAM cell. The basic operation details of some of the most important variants and main candidates as FB-DRAM cells have been discussed emphasizing their benefits and drawbacks. How to face silicon film

scaling has proved to be one of the most remarkable disadvantages of these cells due to *supercoupling* effect. Some designs based on multi-body cells were shown presenting some advantages to overcome the supercoupling effect. Among all of them, special attention was paid to the A-RAM.

In the next Chapter 3, a recent and more promising multi-body cell structure is described, the **A2RAM**, main objective of this work.

Part II

Advanced 2 Random Access Memory cell

Chapter 3

Advanced 2 RAM Cell Introduction

In the following chapter a novel FB-DRAM cell is studied in the framework of the present doctoral thesis. The A2RAM original concept is based on the use of a vertical PN junction in the body to facilitate the presence of both type of carriers simultaneously in ultra-thin Si films overcoming the supercoupling effect. Its fabrication process, behavior and principles of operation together with its main properties and advantages will be deeply detailed.

3.1. A2RAM Cell

In FB-1T-DRAMs, the enhancement of an electron channel once the opposite interface is accumulated requires a second gate or a middle oxide like in the previously seen A-RAM. A solution to overcome this issue and simultaneously **suppress the supercoupling effect** consists in the creation of

permanent electron channel within the body of the device [RCG11a]. This can be achieved by implanting or epitaxially growing a highly doped N-type layer in the bottom of the silicon film of a SOI transistor, Figure 3.1. This buried channel (named **N-Bridge**), provides a natural path for electron between source and drain, regardless the use of a back-gate bias, this connection is the unique difference between a typical FD-SOI transistor and this multi-body cell. The population of holes in the fully depleted top P-body controls the N-Bridge through the action of the gate bias [RCG11c, RCG11b]. In this second generation of Advanced RAM only few and simple additional steps are required during fabrication allowing better manufacturing and making it **compatible with a CMOS process**. This device is also fully compatible with **bulk and SOI substrates**. The advantages of using one substrate or the other will be manifested in Chapter 5.

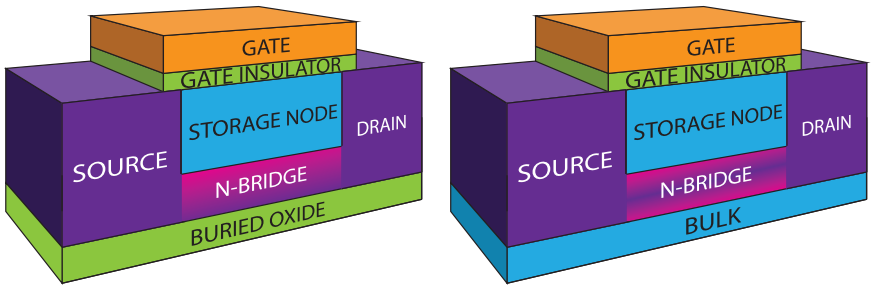


FIGURE 3.1: Structure of the 1T-DRAM memory A2RAM. Instead of using a middle oxide like the A-RAM cell, the separation of carriers in the A2RAM is achieved by using a vertical PN junction.

3.1.1. Fabrication Process

The process behind the fabrication of an A2RAM FB-DRAM cell is explained here: the first four steps are represented in Figure 3.2 and the last four in Figure 3.3.

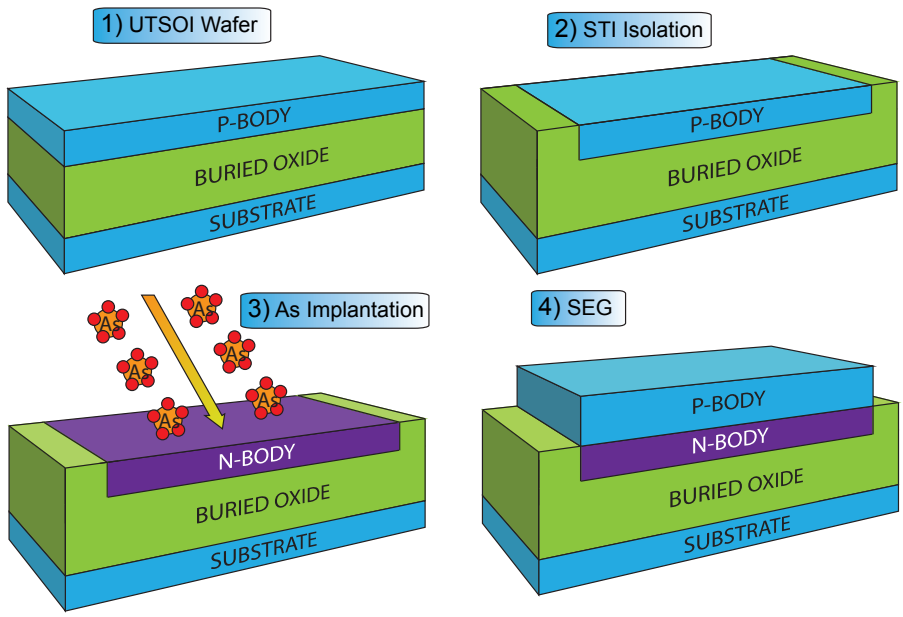


FIGURE 3.2: Step by step fabrication process of an A2RAM Cell on SOI (I).

1. It starts with the unprocessed SOI wafer. Given the advantages of integration obtained using very narrow silicon films layers, an **UTSOI** (*Ultra Thin SOI*) wafer is selected.

2. The first process is to isolate each device laterally. To do so, a shallow trench isolation is carried out.

3. After this, the implantation to create the N-Bridge is performed usually with arsenic ions. The employed energy defines the final profile of implantation.

4. To create the P-type region above the N-Bridge, a **SEG** (*Selective Epitaxial Growth*) is used.

5. Due to thermal load of all processes, including the SEG, the As dopants in the N-Bridge will diffuse to less doped regions, in this case, the new grown P-type layer.

6. The next step is to deposit the multiple layer *high-k* gate oxide. A first layer of silicon dioxide to reduce the number of defects in the interface is often used; the other layers are made of materials with higher permittivity to reduce the gate leakage by tunneling and improve the electrostatic control driven by the gate. Hafnium oxide (HfO_2) is usually employed here.

7. Next a metal gate is created. The material is selected to fit with its metal work-function (Φ_M) the requisites of threshold voltage. Titanium nitrate (TiN) has been lately used.

8. Finally the source and drain regions are created by using an ionic implantation.

These steps represent the fabrication process followed in the SOI samples provided by CEA-LETI (refer to Chapter 4 for a more detailed description of fabrication).

3.1.2. Operation

The operation of this cell is represented in Figure 3.4. **Two different conductivity states are achieved by depleting or not the N-Bridge**. The low current state ('0') takes place when the N-Bridge is depleted and the high current state ('1') when it is not. The simplified sequence of states is shown in Figure 3.4.

The upper P-type body is charged with holes generated either by band-to-band tunneling or by impact ionization. These holes can be retained

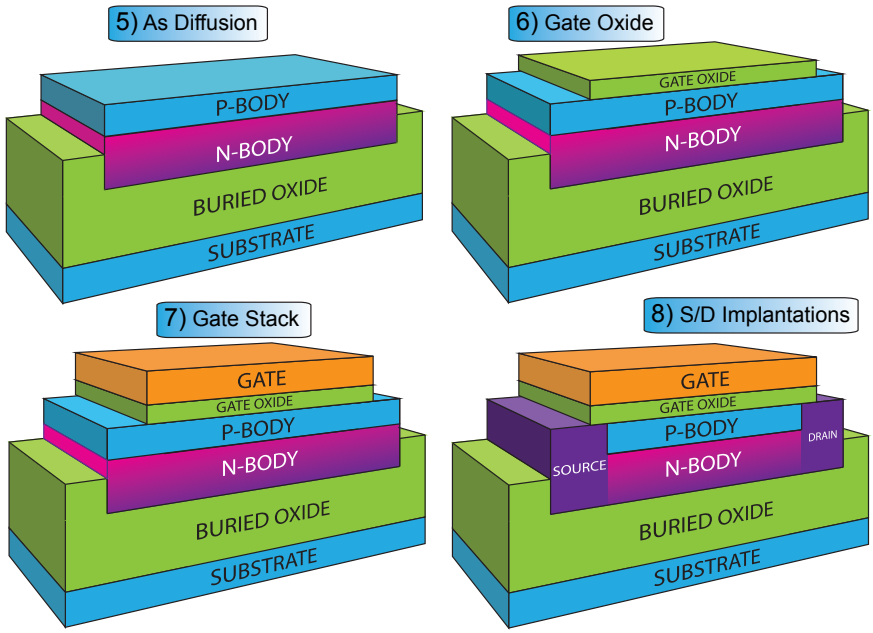


FIGURE 3.3: Step by step fabrication process of an A2RAM Cell on SOI (II).

in the top body thanks to a negative front-gate bias ($V_{FG} < 0$ V), see Figure 3.4 **(A)**. In this situation, the vertical electric field, which is originated due to the negative front-gate bias, is screened by the hole population accumulated in the P-type body so it has a minor effect on the majority carriers accumulation of the N-Bridge. The N-Bridge is partially or not depleted (depending on the population of holes at the P-type body), and a small drain bias leads to a large electron current flowing through the bridge (no current flows through the p-body) when reading the state '1', Figure 3.4 **(B)**. When the top body is discharged of holes (state '0') by capacitive coupling, the front-gate induced electric field is no longer screened by the holes, and the N-Bridge is fully depleted, Figure 3.4 **(C)**. The lack of majority carriers in the N-Bridge causes a very low current if the drain bias is increased due to the high-resistivity of

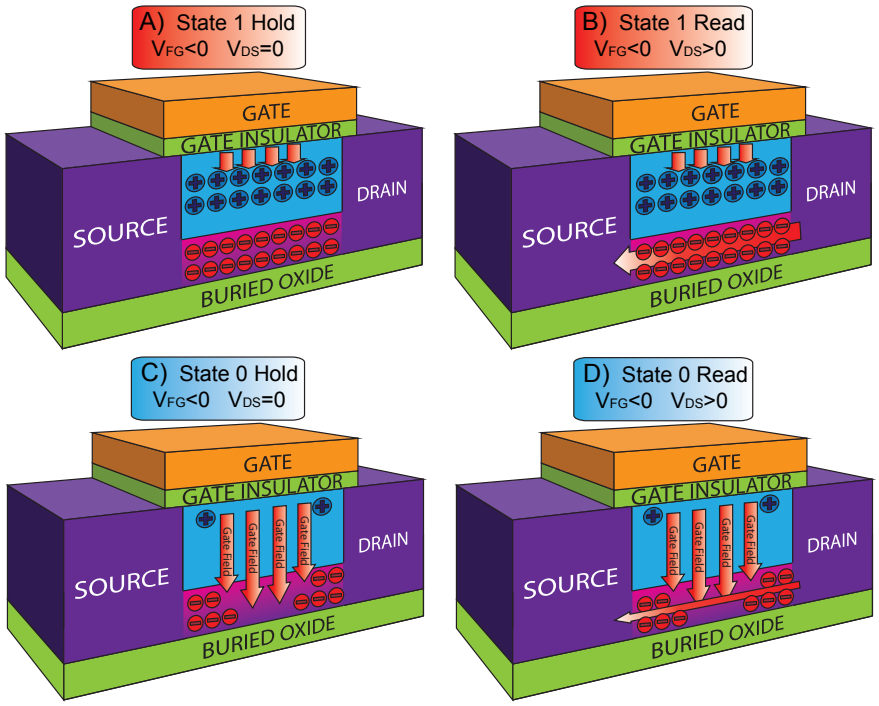


FIGURE 3.4: Schematic of the A2RAM under operation. A front negative bias is needed to ensure the hole accumulation in the storage node. A) No significant hole concentration in the storage node allows the front-gate to deplete the N-Bridge cutting the channel, when a drain bias is applied, B) a negligible current is driven through the N-Bridge since no free carriers are present. C) Charge accumulated in the storage node screens the influence of the front-gate on the N-Bridge and allowing therefore the existence of free majority carriers. When increasing the drain bias, D) a large current flows across the N-Bridge.

the fully depleted N-bridge, Figure 3.4 **(D)**.

The differences with conventional typical FB-1T-DRAMs are threefold [RCG11c].

1. The drain current, which defines the cell state, is due to majority carriers (electrons in the N-Bridge) flowing or not in the volume of the N-Bridge.

2. The *supercoupling* effect is suppressed, the potential drop across the silicon film is obtained through the vertical PN junction (built-in potential) leading to further scaling viability.

3. The use of the BOX insulator layer is not an indispensable requisite, thus these cells may be manufactured also in bulk substrates.

An actual image of the A2RAM memory cell is depicted in Figure 3.5 using a TEM (*Transmission Electron Microscopy*) image. The different regions are illustrated in **(a)** while state '1' and '0' appear in **(b)** and **(c)** respectively.

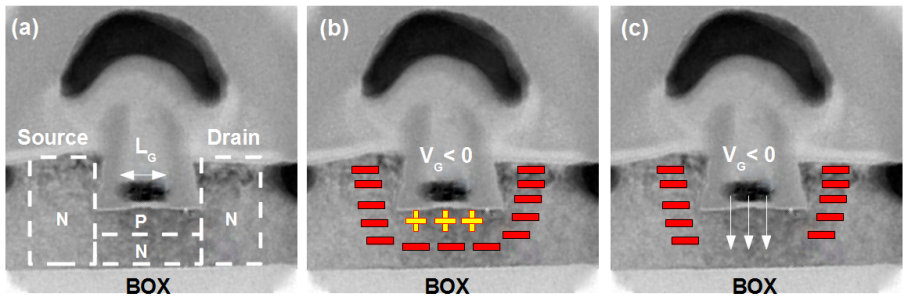


FIGURE 3.5: Actual TEM image of a fabricated A2RAM cell. The substrate can be either insulator or low doped bulk. **(a)** Regions in a A2RAM memory cell. **(b)** The accumulated holes in the top P-body screen the electric field influence from the front-gate; an electron current can flow between source and drain. **(c)** If the P-type body is in deep depletion, the front-gate field is no longer screened fully depleting the N-Bridge from carriers and cutting the drain current.

3.1.3. A2RAM on Bulk Substrates

One of the possibilities that the A2RAM memory cell features is to be fabricated on bulk wafers, as depicted in Figure 3.6.

Since only one additional implantation is required, it makes the fabrication compatible with standard CMOS process (the first four steps are exemplified

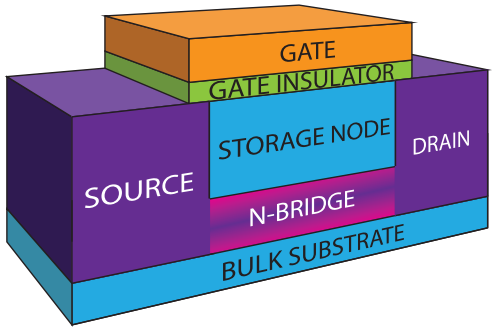


FIGURE 3.6: Structure of the 1T-DRAM memory A2RAM on a bulk wafer.

in Figure 3.7). It fabrication starts with the unprocessed bulk wafer. The **LOCOS** (*LOCal Oxidation of Silicon*) technique is used in these prototypes to isolate devices [AKP+70]. This is achieved by growing a silicon dioxide layer in between of them. After removing the excess of insulator, the definition of the N-Bridge is done by an ionic implantation using arsenic atoms. The implantation energy determines the thickness of the P-type silicon film above the N-Bridge. The implantation is followed by the growing of the front-gate oxide.

The remaining main steps are represented in Figure 3.8. After growing the front-gate insulator, the polycrystalline silicon is deposited and a reactive ion etching process follows to open the source and drain region vias. The aluminium metal gate contact is then sputtered and finally the S/D regions are implanted using phosphorus. Neither the passivation nor the source drain contact deposition have been represented.

Advantages and Disadvantages

The advantages and disadvantages that SOI technology provides have already been discussed in Chapter 2. Regarding the A2RAM, if these cells

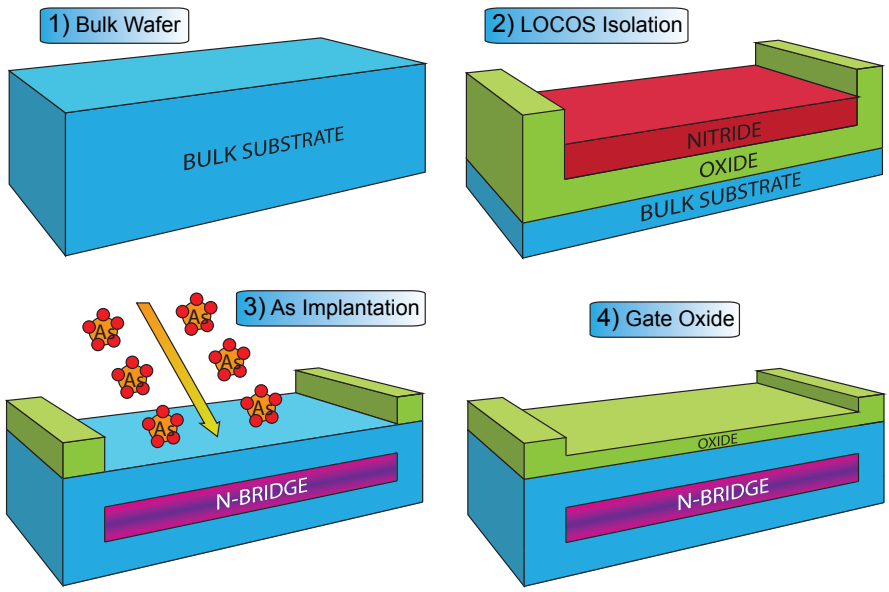


FIGURE 3.7: Step by step fabrication process of an A2RAM Cell on bulk (I).

are manufactured using bulk wafers, they would present further leakage due to the longer area of the PN junction formed by the N-Bridge and substrate, degrading the energy saving. Reduced integration due to extra area employed to isolate devices (devices should be fabricated more separated from each other due to substrate parasitic connection). They would also feature a stronger dependence of SCE limiting the scaling of the channel length. Other drawbacks are for example that the vertical PN doping profile will not be as abrupt as it is in case of an SOI A2RAM cell. The reason is that the buried oxide acts as a natural barrier for dopants avoiding the vertical diffusion of implanted ions. Finally, the films thicknesses, of the N-Bridge and P-type body are better controlled in SOI (thanks to the BOX) than bulk technology leading to more variability on bulk.

On the other hand, the main advantages when using bulk substrates are,

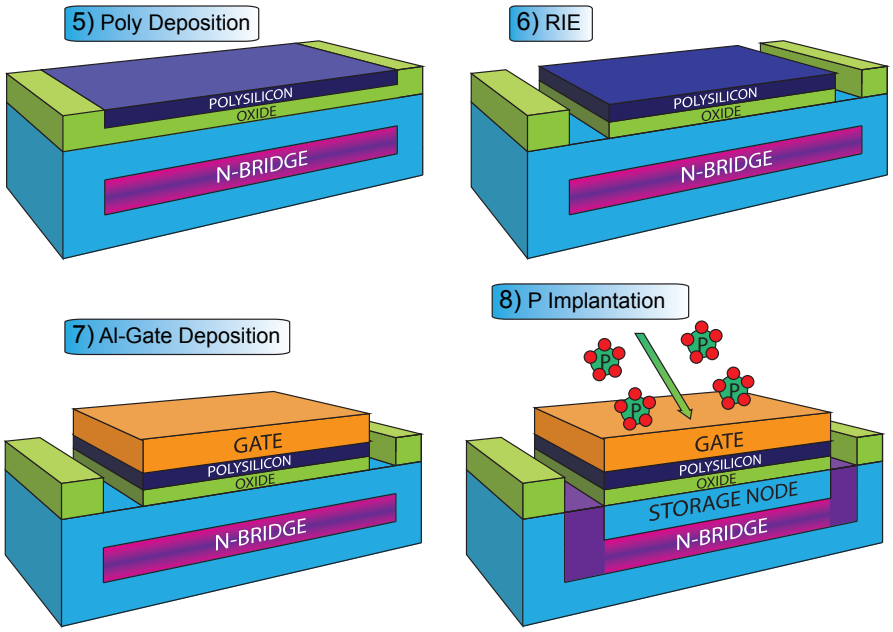


FIGURE 3.8: Step by step fabrication process of an A2RAM Cell on bulk (II).

firstly, the price reduction of the starting wafer and secondly, the possibility of integration with other bulk designs.

3.2. Conclusions

The fundamentals properties of the multi-body Advanced 2 RAM cell have been detailed along the present chapter. It has been explained how it takes care of the limitation that supercoupling effect imposes, separating both types of carriers by using a vertical PN junction. This allows further silicon film thinning and consequently further gate length scaling. The A2RAM cell has been detailed, its structure, peculiarities and its operation were discussed.

Finally the main steps of the fabrication have been enumerated for both cells on SOI and bulk substrates.

In the next Chapter 4, **numerical simulations using Silvaco Atlas® and Athena®** are performed to ensure the feasibility of this memory cell.

Chapter 4

A2RAM Cell Simulations

The rapid developments in semiconductor technology over the past years have led to a dramatic increase in the interest around device modeling and simulation. The need to understand the detailed operation and the optimization of the design of VLSI (Very Large-Scale Integrated) silicon devices and compound semiconductor devices, has pushed device simulation to play a crucial role in modern technology. Today, given the large cost of fabricating a new technology, complete and detailed simulations are always performed before fabrication to ensure that what is going to be manufactured has guaranties to operate as required. In this section, the aim is to simulate the A2RAM prototypes that will be analyzed in following chapters. The result of process and electrical simulations are presented and the detailed operation is demonstrated.

4.1. Silvaco® Software

Silvaco® is a **EDA** (*Electronic Design Automation*) and **TCAD** (*Technology Computer Aided Design*) **process and device simulation**

software. It presents several software tools depending on the aim of the simulation. The main tools used in this work are slightly discussed here.

4.1.1. Athena® Process Simulator

The **Athena®** Two-Dimensional Process Simulation Framework [Sil04a] is a software tool for **modeling semiconductor fabrication processes**. This software provides facilities to perform efficient simulation analysis that substitutes for costly real world experimentation. It combines high temperature process modeling such as impurity diffusion and oxidation, topography and lithography simulations in a single framework. Some of the capabilities Athena® features are:

- CMP: method used for smoothing surfaces with the combination of chemical and mechanical forces.
- Deposition: process that grows, coats, or otherwise transfers a material onto the wafer.
- Diffusion: movement of particles from regions of high concentration to regions of low concentration.
- Epitaxy: deposition of an over-layer on a crystalline substrate, where the over-layer is in registry with the substrate.
- Etch: remove material from the wafer either in bulk or selectively.
- Oxidation: produce a thin layer of oxide (usually silicon dioxide) on the surface of a wafer.

4.1.2. Atlas® Device Simulator

Atlas® is a modular and extensible framework for physically-based one (1D), two (2D) and three-dimensional (3D) **semiconductor device simulation** [Sil04b]. It is implemented using modern software engineering practices that promote reliability, maintainability, and extensibility. It predicts the electrical behavior of specified semiconductor structures and provides insights into the internal physical mechanisms associated with device operation. Some of the analysis Atlas® introduces are:

- DC, AC small-signal, and full time-dependency.
- Drift-diffusion transport models.
- Energy balance and hydrodynamic transport models.
- Fermi-Dirac and Boltzmann statistics.
- Advanced mobility models.
- SRH, radiative, Auger, and surface recombination.
- Impact ionization (local and non-local).
- Band-to-band and Fowler-Nordheim tunneling.
- Quantum transport models.

The following subsections address the main models chosen for the simulations.

Mobility Model

The inversion layer **mobility model from Lombardi** is selected [LMSV88]. This mobility model deals with the **transverse electric**

field dependence (normal E), **doping concentration** dependence and **temperature** dependence. These mobility scattering factors are combined using the *Matthiessen's rule* as Equation 4.1.

$$\mu_T^{-1} = \mu_{AC}^{-1} + \mu_b^{-1} + \mu_{sr}^{-1} \; [cm^2/V \cdot s] \tag{4.1}$$

where μ_T^{-1} is the final mobility, μ_{AC}^{-1} is the surface mobility limited by scattering with acoustic phonons, μ_{sr}^{-1} is the surface roughness factor and μ_b^{-1} is the mobility limited by scattering with optical intervalley phonons.

Recombination Model

Shockley-Read-Hall, **SRH**, is used as recombination model [SR52b, Hal52]. The SRH recombination is modeled using Equation 4.2

$$R_{RSH} = \frac{n \cdot p - n_i^2}{\tau_p \cdot (n + n_i \cdot e^{\frac{E_{trap}}{k \cdot T}}) + \tau_n \cdot (p + n_i \cdot e^{\frac{-E_{trap}}{k \cdot T}})} \; [1/cm^3 \cdot s] \tag{4.2}$$

being E_{trap} the difference between the trap energy level and the intrinsic Fermi level. $\tau_{n,p}$ are the electron and hole lifetime respectively.

Band gap Narrowing Model

In the presence of heavy doping, greater than 10^{18} cm^{-3}, experimental work has shown that the $n_i = p \cdot n$ product in silicon becomes doping dependent [Slo77]. As the doping level increases, a **decrease in the material band gap** separation occurs, where the conduction band is lowered by approximately the same amount as the valence band is raised. These effects may be described by an analytic expression relating the variation in band gap, ΔE_g, to the doping concentration, N, by Equation 4.3 [SdG77].

$$\Delta E_g = a \cdot \left(ln\left(\frac{N}{b}\right) + \left[\left(ln\left(\frac{N}{b}\right)\right)^2 + c \right]^{1/2} \right) \; [eV] \tag{4.3}$$

where a, b and c are constants to fit the model. The variation in band gap is introduced to the other physical models by subtracting the result of the previous equation from the bandgap, E_g.

Band-to-Band Tunneling Model

The tunneling generation rate by BtBT is given by Equation 4.4 [HKK92, Kla91, HKKO89].

$$G_{BtBT} = a \cdot E^b \cdot e^{\frac{-c}{E}} \; [1/cm^3 \cdot s] \tag{4.4}$$

E is the magnitude of the electric field and a, b and c are also user-definable parameters to fit the model.

4.2. CEA-LETI A2RAM Simulation

In this section the A2RAM memory cell on SOI will be simulated trying to take into account the **same fabrication process** that will be used for the actual SOI samples produced by CEA-LETI. After the process simulations, several electrical simulations are performed to verify that the same theoretical operation exposed in Chapter 3 is achieved in the simulated devices.

4.2.1. Preliminary Simulations

Since the A2RAM had been never fabricated so far, **preliminary simulations** were already performed in order to obtain the minimum and maximum values of the N-bridge thickness [RCG11c]. These results were used as a reference to fabricate the devices in CEA-LETI. The values were provided to optimize the A2RAM cell of $L = 80 - 100\,nm$. In particular, a current ratio over 20 was selected by assuming a 10 nm thick top P-body ($t_{Si} = t_{Si-P} + t_{N-Bridge}$). For a given doping, if the bridge is very thin, it is always FD (dotted line in Figure 4.1). On the other hand, a thick bridge is never FD, resulting in a degraded state definition (dashed line in Figure 4.1).

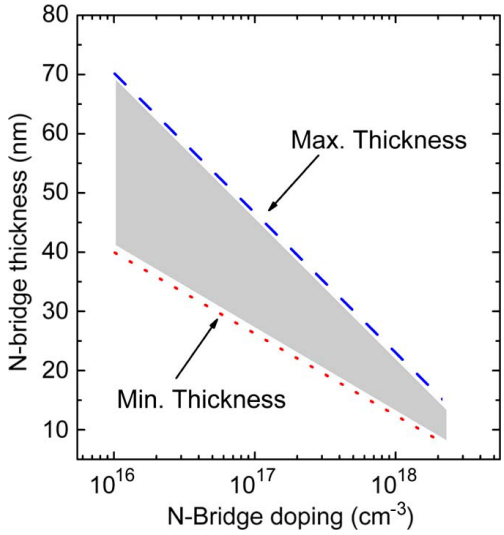


FIGURE 4.1: A2RAM bridge thickness design window as a function of the bridge doping. The top and bottom limits fit a minimum current margin ratio between states of 20 [RCG11c].

It is worth noting that the doping concentration of the N-Bridge (from $N_{N-Bridge} = 10^{16}$ to $2 \cdot 10^{18}\ cm^{-3}$), is lower than those used in state-of-the-art bulk-Si MOSFETs. The RDF are thus not a critical concern for the A2RAM.

4.2.2. Athena® Modeling

Initial wafer

Since this memory cell includes some additional features that traditional transistors does not, it is necessary to model first the fabrication steps before the electrostatic simulations. The Athena® software has been used starting with an unprocessed (100) SOI wafer of 6 nm silicon film, $N_A = 10^{15}\ cm^{-3}$, and a buried oxide thickness of 10 nm. The cross section of this initial wafer is illustrated in Figure 4.2. It must be mentioned that for simplicity only half of the transistor will be fabricated and then a mirror operation will be used to get the complete device.

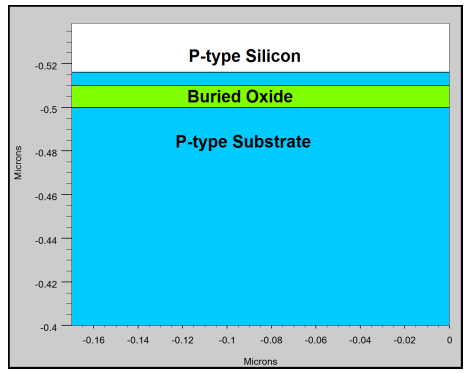
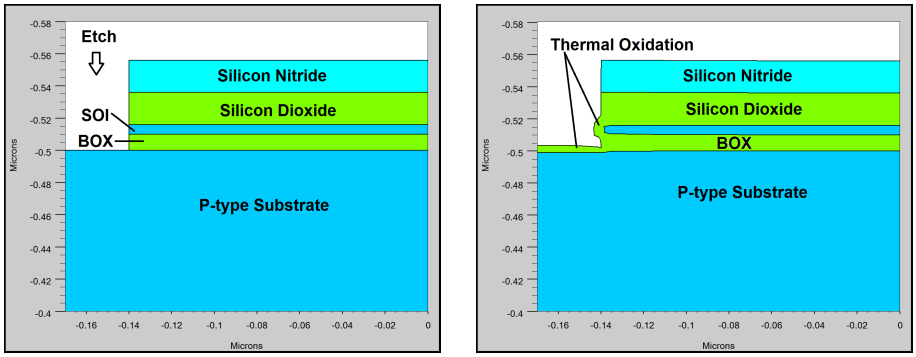


FIGURE 4.2: Initial unprocessed (100) SOI wafer with $N_A = 10^{15}\ cm^{-3}$, $t_{Si} = 6$ nm and $t_{BOX} = 10$ nm.

Lateral Isolation

The first step is to isolate the different devices between them. There are three main techniques, lateral isolation by LOCOS [AKP+70], MESA [FRS66] and the one used in this case, STI [IT84]. A nitride layer is deposited for



(a) Wafer etching (b) Thermal oxidation

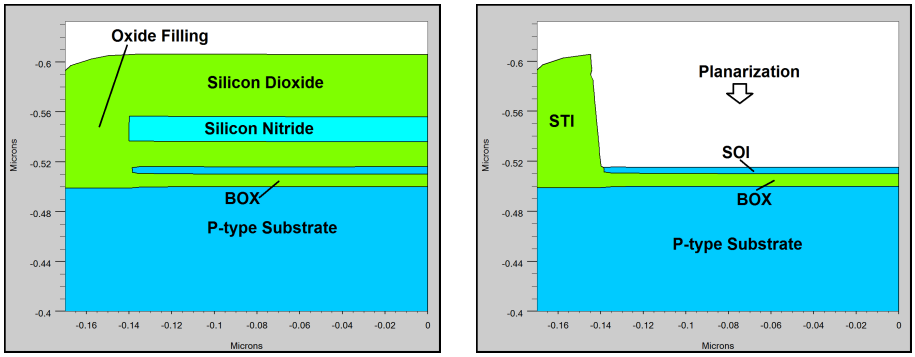
FIGURE 4.3: Shallow trench isolation: **(a)** etching and **(b)** thermal silicon dioxide growth.

selective oxidation in Figure 4.3. In order to avoid the presence of a large amount of defects, it is necessary to use before an initial silicon dioxide film. Once the nitride is on the top, a photolithography step is employed to define the places where the etch will take place, Figure 4.3 **(a)**. After the etch process, a thin thermal oxide is grown and used as a first interface with the silicon, Figure 4.3 **(b)**.

After the thermal oxidation the trench is filled with oxide, Figure 4.4 **(a)**. Next the nitride and excess of silicon dioxide are removed (Figure 4.4 **(b)**) leading to the desired lateral isolation.

N-Bridge creation

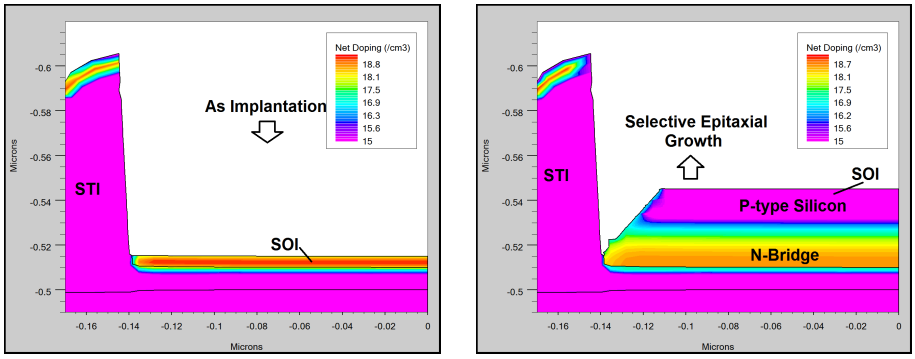
Next, the two steps that differentiate this transistor as an A2RAM cell are carried out. The first one is the arsenic implantation in the channel. A dose of $D_{Im} = 3 \cdot 10^{12}\ cm^{-3}$ atoms of arsenic are implanted with an energy of $E_{Im} = 1\,keV$ and $\theta_{Im} = 7\,^{\circ}$ tilt, Figure 4.5 **(a)**. The same implantation parameters were used in the actual wafer.



(a) Oxide fill (b) Planarization

FIGURE 4.4: Shallow trench isolation: **(a)** oxide filling and **(b)** STI finished after planarization.

After the implantation, a selective 30 nm silicon epitaxial growth is performed. This process defines the final silicon film thickness of the memory cell ($t_{Si} \simeq 36\,nm$). The donor dopants in the channel will start to diffuse due to thermal load because of the epitaxy, Figure 4.5 **(b)**.

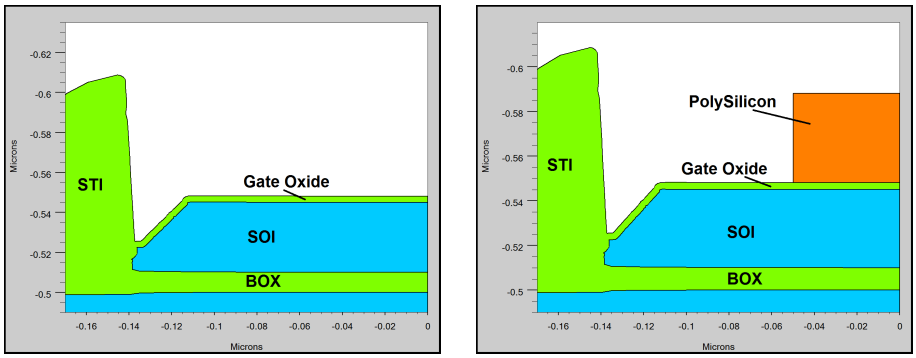


(a) After the N-Bridge arsenic implantation (b) After the selective epitaxial growth

FIGURE 4.5: Net doping concentration (cm^{-3}) after the **(a)** arsenic implantation in the channel to create the N-Bridge and after the **(b)** selective epitaxial growth of 30 nm with the dopant diffusion due to thermal load in epitaxial process. Final $t_{Si} \simeq 36$ nm.

Gate First

Following the N-Bridge formation, the gate of the transistor is fabricated. A dry oxidation is used to obtain a high quality interface. For simplicity, silicon dioxide has been used instead a more complex *high-k* gate stack. The gate oxide thickness in SiO_2 is $t_{ox} = 3.1$ nm, Figure 4.6 **(a)**. After the gate oxide, the gate contact is deposited, in this case polysilicon has been used, represented in Figure 4.6 **(b)**. The simplification of using polysilicon and the equivalent oxide thickness instead the actual metal-*high-k* gate stacks does not make any difference in the electrical simulation. Atlas® performs the simulation in a similar way; it considers the polysilicon as an equipotential material, like a metal with a tunable work-function that will fit the real TiN metal gate.



(a) Dry gate oxidation (b) Poly gate deposition

FIGURE 4.6: **(a)** Dry growth of the SiO_2 front-gate oxide and **(b)** polysilicon gate contact deposition.

Source/Drain definition

Once the gate is created, it is necessary to define the source and drain regions. This is usually performed by an ionic implantation. In this case, since the device is N-type, arsenic atoms are used. The resultant device with the

2D net doping distribution is depicted in Figure 4.7. The source and drain terminals present certain overlap with the gate stack. This will enhance the hole injection during the BtBT based writing process.

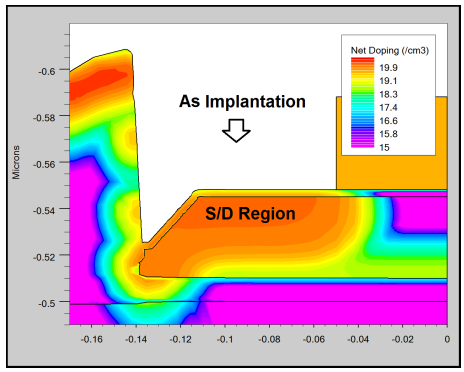


FIGURE 4.7: 2D net doping distribution (cm^{-3}) after the arsenic ionic implantation to create the source and drain regions.

Passivation and Contact Deposition

So far, it only remains to protect the device and create the contacts to access the transistor. The protection of the device is achieved by depositing a thick layer of silicon dioxide over the entire structure. This complete vertical isolation allows to use the top of the structure to create the interconnection metal layers between devices. The A2RAM memory cell, after the passivation, is shown in Figure 4.8.

Finally, an etching process and metal deposition are carried out. The etch is located at the drain and source regions as illustrated in Figure 4.9 **(a)**, the subsequent metal deposition creates the contact. Titanium and aluminium are used to access the implanted regions, Figure 4.9 **(b)**.

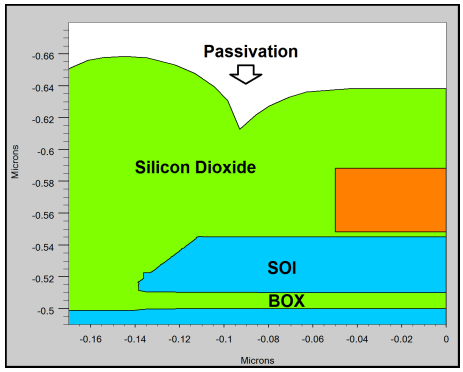
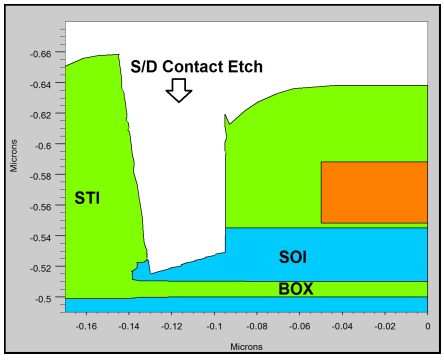
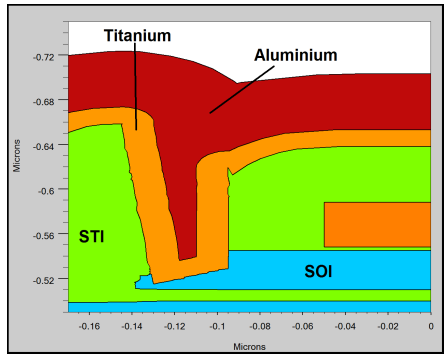


FIGURE 4.8: Silicon dioxide thick layer deposition. Passivation of the surface of the transistor.



(a) S/D metal contact etching

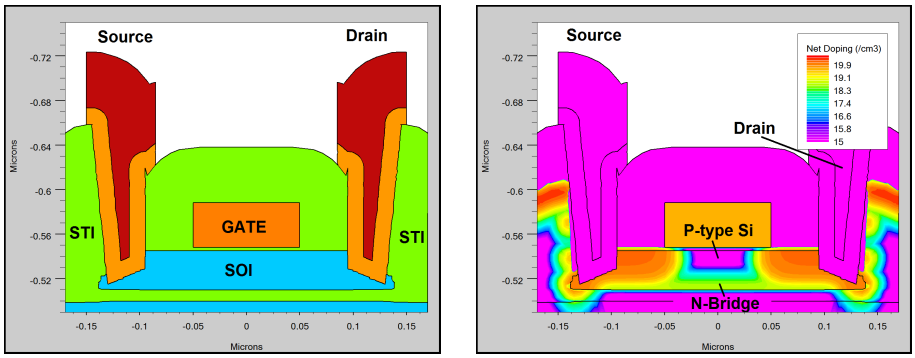


(b) S/D metallization

FIGURE 4.9: **(a)** Silicon dioxide etching to access the source and drain implanted regions. **(b)** Metallization to create the contacts.

Final SOI-A2RAM Cell

In the last steps the metal layers are first etched and then by successive deposition and passivation, connected to create the user end contacts. The final A2RAM cell, once mirrored, is represented in Figure 4.10 **(a)**. The final 2D net doping distribution is illustrated in Figure 4.10 **(b)**. The bottom area of the silicon film presents a large doping concentration. This is the N-Bridge connecting the source and drain regions. The estimated length of the device is around $L = 80\,nm$.

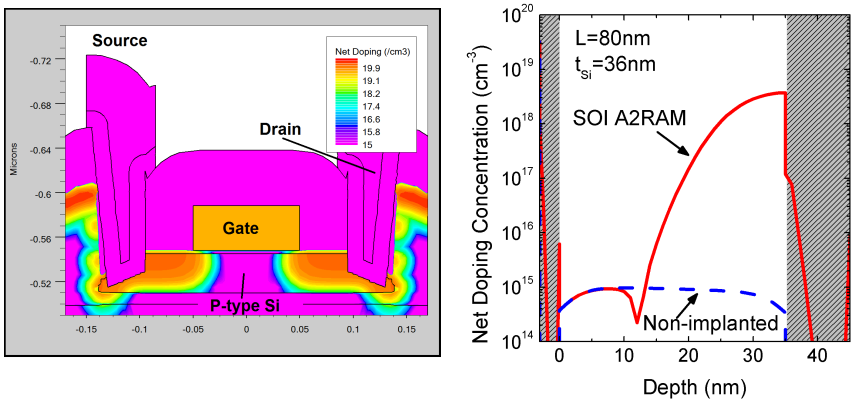


(a) Final A2RAM cell (b) 2D net doping distribution

FIGURE 4.10: **(a)** Final A2RAM cell structure and **(b)** 2D net doping distribution (cm^{-3}). Notice the highly N-type doped bottom region of the Si-film defining the N-Bridge.

The same cell without the arsenic ion implantation has also been simulated (see Figure 4.11 **(a)**). The vertical net doping profiles at mid-channel are represented for both A2RAM cell and non-implanted transistor in Figure 4.11 **(b)**. The effect of the arsenic implantation and thermal diffusion is evidenced in the comparison. The doping profile for the non-implanted transistor shows an almost constant net doping concentration, same as the initial wafer used. In contrast, the A2RAM doping profile presents an increase in the doping concentration as moving close to the buried oxide. This region is the N-Bridge.

A peak over $N_{N-Bridge} = 10^{18}\, cm^{-3}$ is achieved at the back interface $Si - SiO_2$. The obtained A2RAM doping profile is consistent with the preliminary simulations for a $t_{N-Bridge} \simeq 20 - 25\, nm$ (see Figure 4.1).



(a) Non-implanted Cell (b) Si-film net doping profile comparison

FIGURE 4.11: **(a)** Simulated 2D net doping distribution (cm^{-3}) of the non-implanted transistor and **(b)** final vertical net doping concentration profile (from gate to BOX) comparison across the Si-film. Notice the effect of the arsenic implantation to define the N-Bridge.

4.2.3. Operation Principle

Now, the performance of the recently modeled SOI A2RAM cell will be studied. The first step is to check whether it behaves as a transistor or not. A typical front-gate voltage sweep is performed and compared with the same but non-implanted device, Figure 4.12.

On one hand, the non-implanted cell (dashed line) shows the typical transistor drain current curve affected by series resistance effect (mainly due to the thin silicon film of the device and S/D contacts). On the other hand,

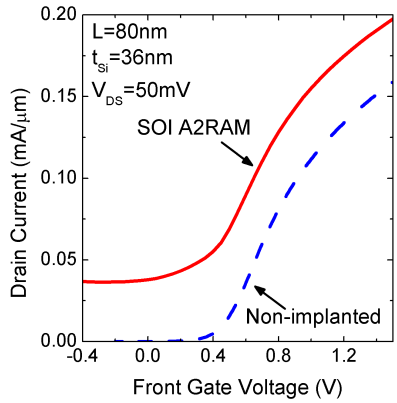


FIGURE 4.12: $I_{DS}(V_{FG})$ comparison between simulated A2RAM cell and non-implanted transistor without As-Implantation (no N-Bridge) using Atlas®. $V_{DS} = 50\,mV$ and $V_{BG} = 0\,V$.

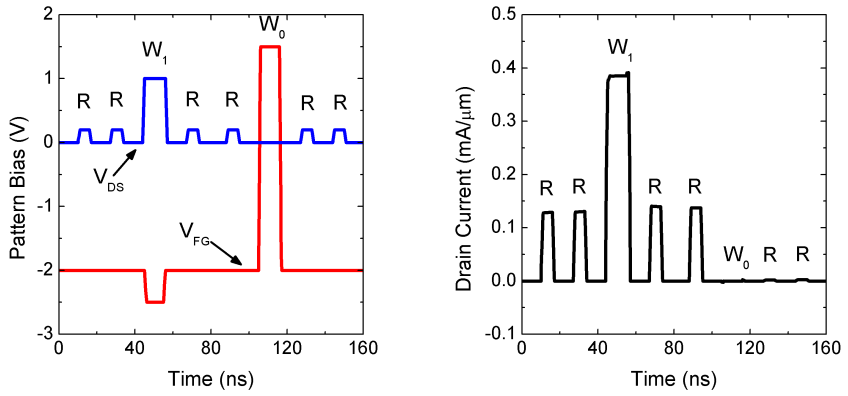
the drain current driven by the A2RAM cell (solid line) is rather the same but with an constant shift. This drain current increase is motivated by the extra current driven through the N-Bridge. The implicit connection acts as a resistance being almost independent of the front-gate voltage applied (from low-negative to positive gate voltages).

Once the device stationary $I_{DS}(V_{FG})$ characteristics has been verified, its capabilities as memory cell will be checked. To do so, a simple transient pattern should be applied. There are four main operations in a memory. They appear summarized in Table 4.1.

The goal of the **Read** (R) process is to measure the drain current to discriminate the state of the cell. The **Hold** (H) operation tries to preserve the stored cell state for as long as possible. Finally, both **Write** operations (W_1 and W_0 which is also called **Erase**) attempt to change or refresh the state of the cell.

Operation	Symbol	Detail
Read State	R	Discriminate whether the state of the cell is high or low
Write High	W_1	Store the high state on the memory cell
Write Low	W_0	Store the low state on the memory cell
Hold State	H	Maintain as long as possible the present cell state

TABLE 4.1: *Most remarkable operations in a A2RAM cell.*



(a) Pattern applied (b) Resulting drain current

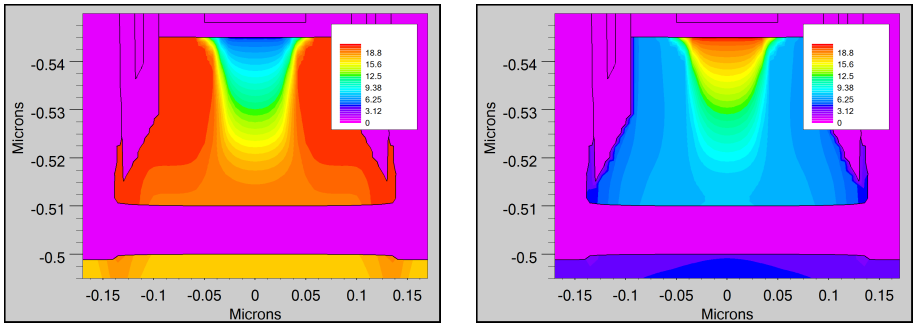
FIGURE 4.13: A2RAM cell operation **(a)** bias pattern and **(b)** drain current readout.

The random pattern applied to the simulated SOI A2RAM cell is represented in Figure 4.13 **(a)**. The complete sequence is as follow: $R \mid R \mid W_1 \mid R \mid R \mid W_0 \mid R \mid R$ where the *hold* operation is the default state; all other operations return to it once ended. The biases used here were optimized to enhance the memory characteristics while using reasonably low voltages to avoid large power consumption and reliability problems.

The response of the cell shows how the drain current levels are modified

attending to the last operation performed, Figure 4.13 **(b)**. The pattern starts with two reads, a low drain bias is used while reading to enhance power saving. The initial sensed current is not negligible, around $I_{DS} = 0.125\, mA/\mu m$. This implies that an important accumulation of holes is present under the front-gate so the N-Bridge is not fully depleted. Immediately after, the cell is written to its high state, W_1. To do so, a large negative drain to front-gate bias is applied to stimulate the injection of holes by band-to-band tunneling (the drain current observed during the W_1 process correspond to the GIDL current but specially drain to source current through the N-Bridge). The two following reads show also the high current level (a bit larger than before the writing, $I_{DS} = 0.140\, mA/\mu m$). Since V_{DS} remains the same, this implies that more holes have been injected. The increase in the hole population further weakens the depletion of the N-type body region. This translates into a higher concentration of electrons in the N-Bridge and to a higher drain current when reading. Lastly, an erase operation (W_0) is carried out followed by two reads. Erasing is achieved by increasing the front-gate voltage while the drain and source contacts are grounded. The rise in V_{FG} increases the body potential, V_{BS}, forward biasing the PN junctions by capacitive coupling (body to source and body to drain). The resultant current removes the holes previously stored below the front-gate. The hole population is then diminished and the front-gate influence over the N-Bridge is no longer screened. The drain current obtained after the erasing is barely visible indicating an almost full depletion of the N-Bridge channel ($I_{DS} = 0.15\, \mu A/\mu m$).

The state of the cell at each memory step is studied via numerical simulations using the simulated A2RAM cell to check the validity of the explanation above. By monitoring some parameters along the silicon body such as the carrier concentration, current density, electric field... it can be observed how the operation follows the theoretical principles already discussed.

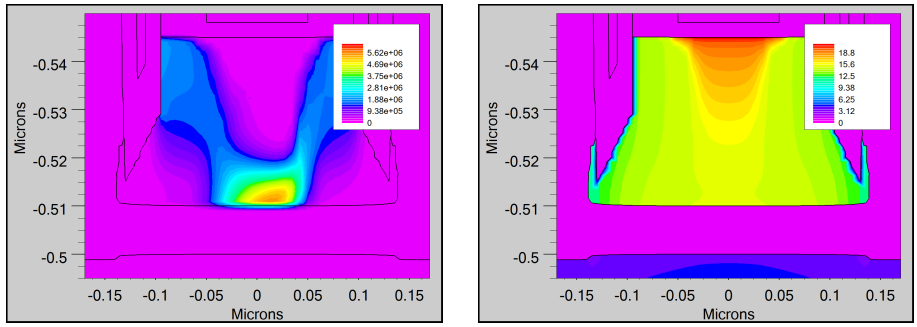


(a) Electron concentration (b) Hole concentration

FIGURE 4.14: Initial steady state of A2RAM cell before the first *read* operation at t=10 ns. **(a)** Electron (cm^{-3}) and **(b)** hole (cm^{-3}) 2D distribution in logarithmic scale. Times are referred to Figure 4.13.

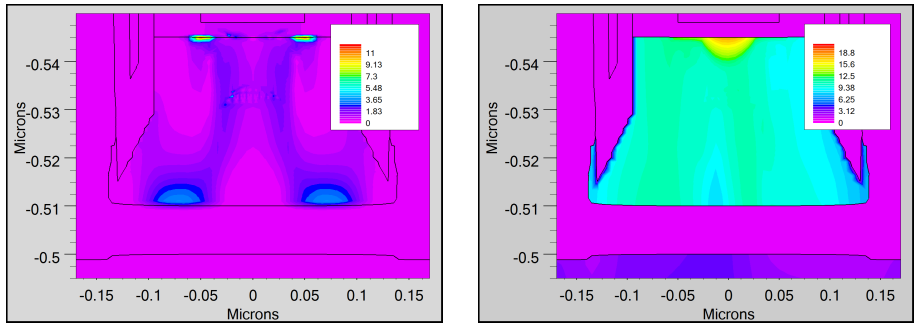
The steady state of the cell before *read* is depicted in Figure 4.14. At t=10 ns a visible accumulation of electrons appears at the bottom of the body in Figure 4.14 **(a)**. At the same time, a high hole concentration is retained below the front-gate oxide due to the negative front-gate bias, Figure 4.14 **(b)**. The positive charge blocks the gate influence avoiding the N-Bridge depletion. It should be noted that in the A2RAM cell, **high hole and electron concentrations are achieved simultaneously**.

The A2RAM cell state during and after the *write* '1' operation appears represented in Figure 4.15. The current during the writing process is illustrated in Figure 4.15 **(a)**. The current density appears as a consequence of the large drain to source bias applied to allow the BtBT at the drain edge. The hole concentration after the *write* '1' is shown in Figure 4.15 **(b)**. The obtained hole population is boosted with respect to the state before programming. Nevertheless, this increase in the positive charge does not translate into a large change in the drain current when reading (around 11%). This means that the N-Bridge is almost not depleted by default, **state '1' is the stable state of the A2RAM cell**.



(a) Total current during *write* '1' (b) Hole concentration after *write* '1'

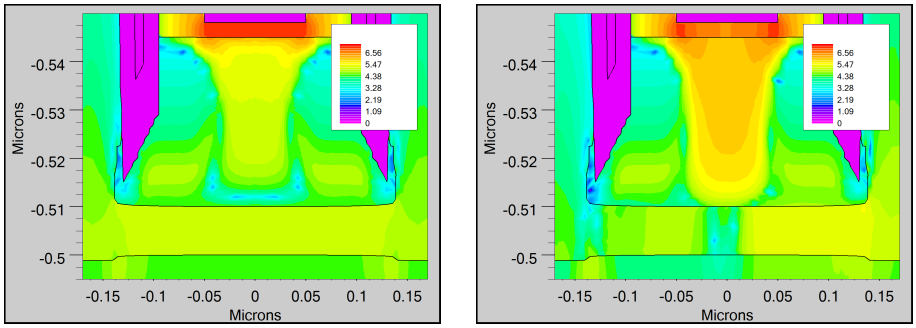
FIGURE 4.15: **(a)** Total current density ($A/cm^2 \cdot \mu m$) during *write* '1' at t=55 ns and **(b)** hole concentration (cm^{-3}) in logarithmic scale after the *write* '1' at t=67 ns. Times are referred to Figure 4.13.



(a) Total current during *write* '0' (b) Holes after *write* '0'

FIGURE 4.16: **(a)** Total current density ($A/cm^2 \cdot \mu m$) during *write* '0' at t=105 ns and **(b)** hole concentration (cm^{-3}) in logarithmic scale after the *erase* at t=133 ns. Times are referred to Figure 4.13.

The state during and after the *erase* operation is also studied. The current density is represented in Figure 4.16 **(a)**. It turns to be negligible since the drain to source voltage is zero. The hole concentration, on the other hand, is drastically reduced from the previous state (Figure 4.16 **(b)**) leading to a lack of free electrons in the N-Bridge due to the non-screened electric field induced by the negatively biased front-gate. This depletion is reflected in the low current sensed when a drain to source bias is applied, see Figure 4.13 **(b)**.

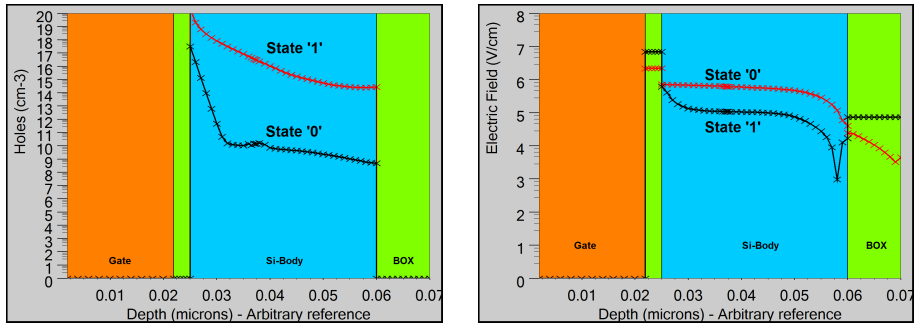


(a) Vertical electric field after *write* '1' (b) Vertical electric field after *write* '0'

FIGURE 4.17: Vertical electric field (V/cm) **(a)** after W_1 process at t=67ns and **(b)** after the erasing, W_0, at t=133 ns. Times are referred to Figure 4.13.

The last simulations illustrate the vertical electric field and carrier concentrations after the *write* and *erase* operations, emphasizing the screening effect of the holes accumulated below the front-gate. The vertical electric field appears represented in Figure 4.17 after the **(a)** W_1 and **(b)** W_0. After the *write* '1', the vertical electric field is mitigated by the positive charge. In case of the *write* '0' (erase), the field is larger and extends deeper into the N-Bridge depleting the implicit source/drain connection from free electrons.

A better insight is obtained when extracting the vertical profiles of the hole concentration and vertical electric field at mid-channel after both memory operations. The role played by the holes is evidenced when observing their



(a) Hole concentration (b) Vertical electric field profiles

FIGURE 4.18: Vertical profile comparison of **(a)** holes concentration (cm^{-3}) and **(b)** electric field (V/cm) in logarithmic scale between both, high at t=67 ns (after W_1), and low, at t=133 ns (after W_0), memory states in the A2RAM cell. Times are referred to Figure 4.13.

population and the associated vertical electric field. The front-gate induced electric field is screened by the positive charge, Figure 4.18. When the hole concentration is large below the front-gate oxide (after *write* '1') in Figure 4.18 **(a)**, the electric field decreases as shown in Figure 4.18 **(b)**.

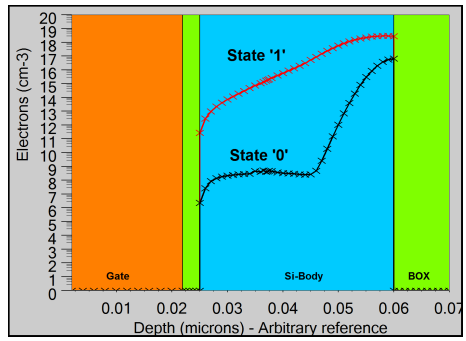


FIGURE 4.19: Vertical profile comparison of the electron concentration (cm^{-3}) in logarithmic scale between the high, at t=67 ns (after W_1), and low, at t=133 ns (after W_0), memory states in the A2RAM cell.

The immediate effect obtained is the **control of the depletion of the N-Bridge by changing the hole population**. The electron concentration along the N-Bridge is extracted after both operations to check its degree of depletion, Figure 4.19.

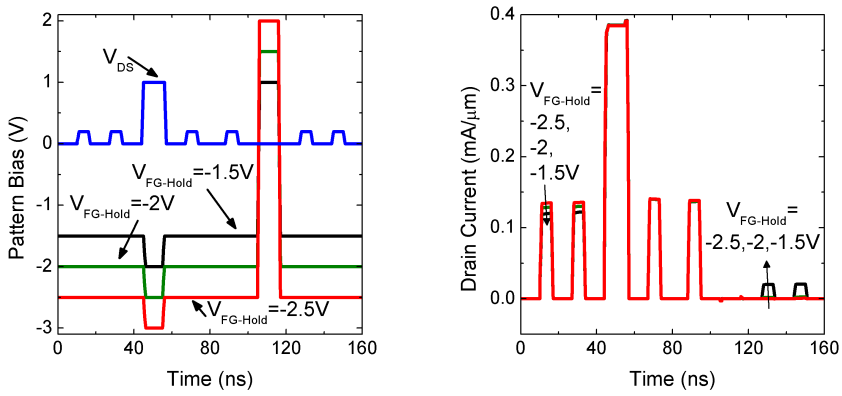
4.2.4. Working Test

So far, the cell behaves as was described in Chapter 3 but some further simulations can be performed to study the dependence of the memory characteristics with the bias or the time.

The drain current of the '1' and '0' states of the cell dependence with the front-gate *hold* and *erase* voltages is depicted in Figure 4.20 **(b)** for several patterns applied (Figure 4.20 **(a)**). Observing the drain current, it does not make sense to use a hold bias lower than $V_{FG} = -2\,V$ or a erasing voltage over $V_{FG} = 1.5\,V$ to enhance the drain current margin between states since no significant change is obtained in the cell current readout. The drain currents for $V_{FG} = -2\,V$ and $V_{FG} = -2.5\,V$ are very similar. The current ratio, ratio between the high and low current levels, can be extracted for $V_{FG} = -2\,V$ using Equation 4.5. Further details about the characterization of the current ratio and current margin will be discussed in Chapter 5.

$$\Delta I_{1/0} = \frac{I_1}{I_0} \simeq 100\ A/A \tag{4.5}$$

The time while the cell data are available for discrimination (retention time) is also strongly influenced by the bias applied. Figure 4.21 shows the evolution of the drain current against the time during a long reading (80 ms) after both a *write* and *erase* operations. The pattern applied to the gate and the drain contacts is represented on top, while the resultant drain current is



(a) Bias patterns applied (b) Driven drain currents

FIGURE 4.20: Front-gate bias dependence on drain current level during hold process. **(a)** Bias pattern applied and **(b)** driven drain current.

depicted at the bottom. The pulse pattern represents the following sequence $W_1 \mid R \mid W_0 \mid R$.

The drain current after the *write* '1' is almost fixed to a constant value, the little drop is coming from the overpopulation of holes after the hole injection. In contrast, the drain current after *erase* (*write* '0') is unstable presenting a prominent rise. This signature indicates how the population of holes behaves with time inside the body of the cell. In the case of the high current level, the population of holes remains quasi-stable. On the other hand, for the '0' state, the drain current increases with time until it reaches the steady current level, around 70 ms after. This happens because the N-Bridge is gradually less depleted. Generated holes are progressively collected below the front oxide by the potential well induced by the negatively biased front-gate. This avoids the full depletion of the N-Bridge and translates into a rise in the drain current. The time it takes for this to happen is strongly related to the thermal

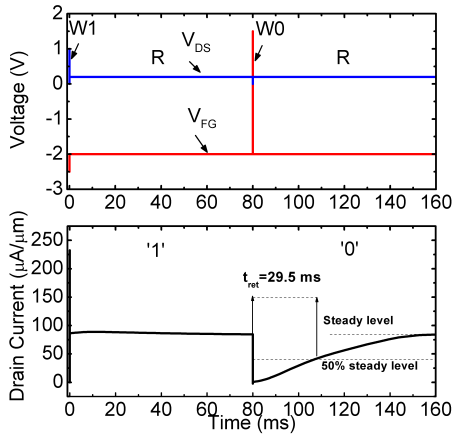


FIGURE 4.21: Simulation of drain current evolution with time. The voltage pattern applied to gate and drain contacts appear on top while the drain current is at the bottom. Notice how the unstable current level is the '0' level. The retention time has been extracted for this scenario.

generation of carriers and hole leakage injection due to undesired GIDL and reverse PN-junction current.

The retention time can be extracted as the time it takes the unstable state (state '0') to arrive to a 50% of the stationary current. Different methods to characterize the retention time will be discussed in Chapter 5. The obtained retention time is given by Equation 4.6.

$$t_{ret} = 29.5\, ms \tag{4.6}$$

4.3. CNM A2RAM Simulation

In this section, TCAD optimization and subsequent simulation of the A2RAM cells fabricated at CNM on SOI and bulk substrates are studied. Firstly, preliminary simulations are carried out to guide the fabrication process. Later, static and dynamic simulations to check the operation as transistor and memory cells are analyzed.

4.3.1. Preliminary Simulations

Some **preliminary simulations** on most critical parameters were again performed. The minimum channel length of $2.5\,\mu m$ was imposed by the technology. The dimensions and main parameters of these simulations appear listed in Table 4.2.

Parameter	Symbol	Value	Units	
P-type Silicon body	t_{Si-P}	50-100	nm	Si
Front Oxide Thickness	t_{ox}	10	nm	SiO_2
N-Bridge Thickness	$t_{N-Bridge}$	Variable	nm	Si
Total Wafer Thickness	t_{Wafer}	1	μm	Si
N-Bridge Doping	$N_{N-Bridge}$	$10^{16} - 5 \cdot 10^{16}$	cm^{-3}	As
Mask Gate Length	L	1	μm	-

TABLE 4.2: *Properties of bulk A2RAM samples during preliminary simulations. Results will be used as reference for manufacturing at CNM (Barcelona).*

To perform the optimization, the response to different writing and reading operations was simulated changing the N-Bridge thickness for several scenarios. The pattern used for these preliminary simulations is depicted in Figure 4.22.

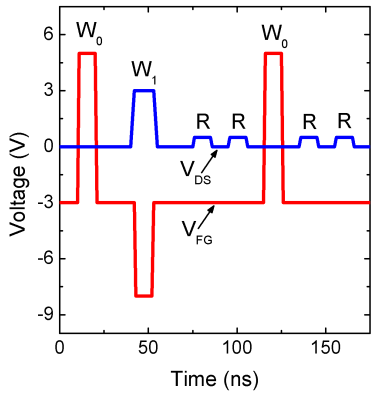
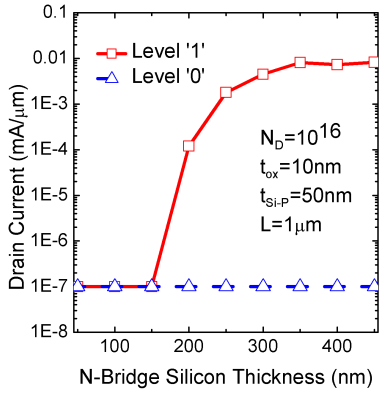


FIGURE 4.22: Bias pattern applied during preliminary simulations of CNM bulk samples. The biases were previously optimized for a $t_{ox} = 10nm$.

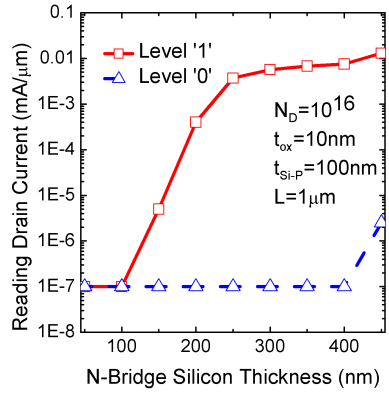
For each scenario a minimum N-Bridge thickness of $t_{N-Bridge} = 50$ nm has been used due to technological limitations and has been gradually increased. The maximum thickness limit was restricted to two cases: that one for which the difference in drain current between levels was insufficient to discriminate them or when it was too thick, $t_{N-Bridge} > 450$ nm. The results are represented in Figure 4.23.

Comparing the results, it can be highlighted how modifying the silicon film thickness and/or the N-Bridge doping yield to a lateral shift of the current levels. Increasing any of them allows the use of thinner N-Bridge layers with similar drain current margins. A balance between the N-bridge and P-type semi-body thicknesses should be found in order to minimize the total Si-film thickness providing the maximum current margin.

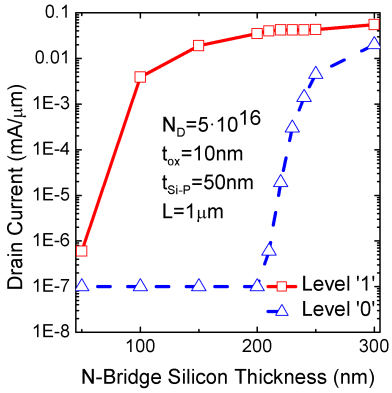
The structure used during these simulations was a simple A2RAM cell with no realistic process simulation (ideal doping concentrations, sharp junctions...). These results served only as a starting point for the engineers at CNM to



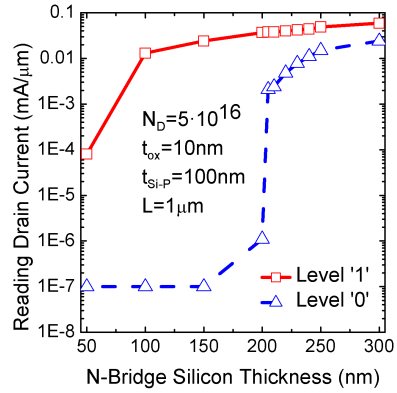
(a) Low-doped and thin cell.



(b) Low-doped and thick cell.



(c) High-doped and thin cell.



(d) High-doped and thick cell.

FIGURE 4.23: SOI A2RAM drain current levels simulated with Silvaco Atlas® for several different cell structures with higher ($N_{N-Bridge} = 5 \cdot 10^{16}\ cm^{-3}$) or lower ($N_{N-Bridge} = 10^{16} cm^{-3}$) doping concentration and thinner ($t_{Si-P} = 50\ nm$) or thicker ($t_{Si-P} = 100\ nm$) P-type silicon over the N-Bridge.

evaluate the feasibility of the project. In the following section, a more realistic A2RAM structure is simulated.

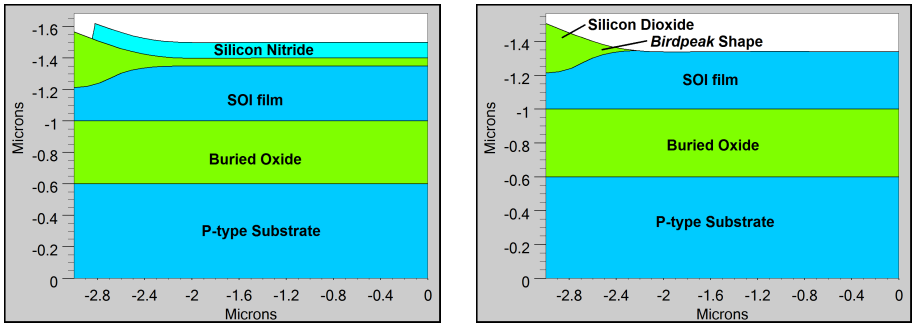
4.3.2. Athena Modeling

Most of the fabrication processes remain virtually the same as for the CEA-LETI SOI case (S/D implantation, passivation, contact creation...). For this reason, only the two main different steps will be shown:

- The lateral isolation technique, LOCOS.
- The N-Bridge creation: arsenic implantation without dopant diffusion by SEG.

Lateral Isolation by LOCOS

STI lateral isolation is the preferred method for the sub-0.5 μm range. In case of the CNM devices, the most traditional **LOCOS** technique [AKP$^+$70] is used instead. The main difference is the area consumption. The first step in LOCOS is to grow a very thin silicon oxide layer. Then a layer of silicon nitride is deposited as an oxide barrier. The pattern transfer to select where LOCOS will take place is performed by photolithography. After applying the mask, the silicon nitride is etched and a thermal oxide is growth (Figure 4.24 **(a)**). Following the wet oxidation process, the excess of nitride is removed leaving only the silicon dioxide underneath, Figure 4.24 **(b)**. This technique is easily recognizable by the *birdpeak* shape that the oxide presents.



(a) Wet oxidation leading to LOCOS (b) LOCOS lateral isolation

FIGURE 4.24: **(a)** LOCOS thermal wet oxidation process to create the lateral isolation and **(b)** final lateral isolation result with the typical *birdpeak* shape. A SOI substrate has been considered.

N-Bridge creation

The second step that differentiates CNM (bulk and SOI) from CEA-LETI SOI samples is the creation of the N-Bridge, the most characteristic region of the A2RAM cell. Instead of using an arsenic implantation and a selective epitaxial growth, in CNM A2RAM cells, the definition of the N-Bridge is achieved by using **only a implantation process**. Figure 4.25 shows the 2D net doping distribution after the arsenic implantation in the CNM SOI wafer. The doping distribution peaks deep inside the silicon film. The depth of this concentration peak can be modulated by changing the implantation parameters, especially the energy used.

Final CNM A2RAM Cell

The resultant A2RAM cells in both types of substrates are represented in Figure 4.26 after all fabrication steps. The devices structure is totally equivalent but the buried oxide. The channel length is around $L = 2.5\ \mu m$

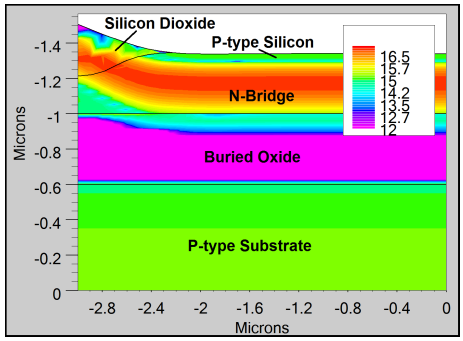
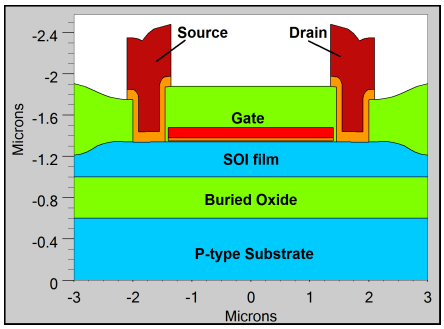
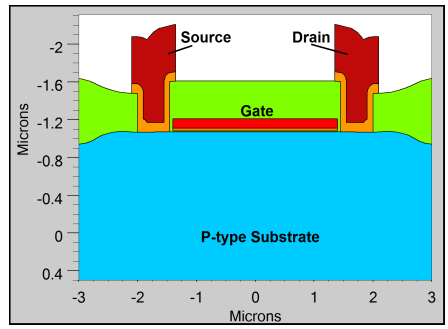


FIGURE 4.25: N-Bridge net doping concentration (cm^{-3})after the arsenic ion implantation in SOI substrate.

and the source and drain implanted regions present certain overlap with the gate contact.



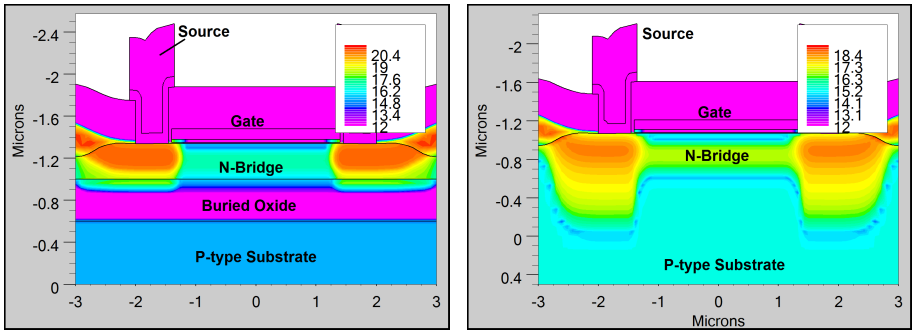
(a) Final CNM A2RAM cell in SOI



(b) Final CNM A2RAM cell in bulk

FIGURE 4.26: Simulated CNM A2RAM cell device fabricated in **(a)** SOI and **(b)** bulk substrates.

The final 2D net doping distributions are depicted in Figure 4.27. In both substrates, the implantation permits the implicit connection between S/D emulating the N-Bridge. A significant difference is observed in the source and drain doping profiles. In bulk wafer the ion implantation is not well controlled and reaches much deeper inside the P-type substrate than for SOI.



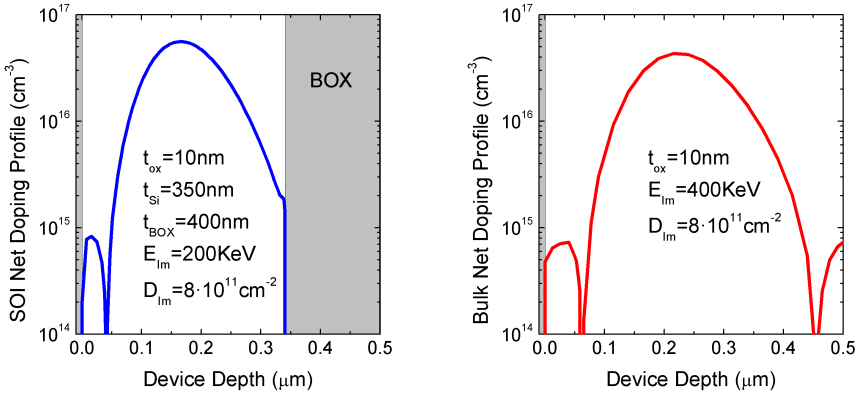
(a) SOI A2RAM net doping (b) Bulk A2RAM net doping

FIGURE 4.27: Simulated CNM A2RAM cell 2D net doping distribution (cm^{-3}) in **(a)** SOI and **(b)** bulk substrates.

The same operation principles from the previous scaled SOI A2RAM apply when moving to larger SOI samples. Modifying the hole accumulation below the front-gate changes the screening level of the electric field induced by the front-gate, modulating the depletion of the N-Bridge. The overall drain current obtained when positively biasing the drain with respect to the source depends on the degree of depletion in the N-Bridge. Figure 4.28 illustrates the final net doping profiles for **(a)** SOI and **(b)** bulk CNM A2RAM cells. The arsenic implantation in the bulk A2RAM cell leads to a peak that is more **widely spread due to the absence of a natural barrier that avoids dopant diffusion**.

4.3.3. Working Test

The comparison between the transfer characteristics, $I_{DS}(V_{FG})$, for A2RAM and non implanted transistors is presented in Figure 4.29 for **(a)** linear and **(b)** logarithmic scale and both types of substrates. An almost constant increase in drain current is found in case of the A2RAM cells as a consequence



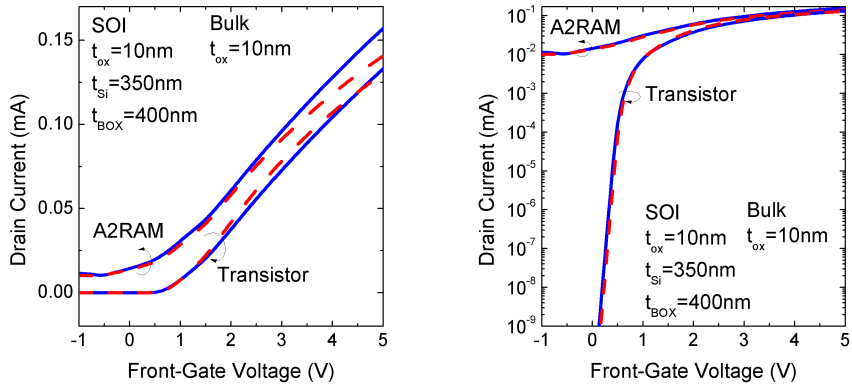
(a) SOI A2RAM doping profile (b) Bulk A2RAM doping profile

FIGURE 4.28: Vertical net doping profiles for A2RAM cells at CNM fabricated in **(a)** SOI and **(b)** bulk.

of the current driven through the N-Bridge. No significant difference is found between A2RAM and SOI for low front-gate voltages. As the gate bias is risen, the drain current in bulk devices present more degradation due to series resistance effect. Although normally SRE is more critical in SOI due to the thinning of the silicon body, in this case the Si-film thickness is thick enough ($t_{Si} = 350\,nm$) so that this contribution can be considered almost negligible. The I_{DS} deterioration can be then attributed to a worse drain and source contacts doping profiles for bulk devices (Figure 4.27). The BOX layer helps stoping the ions implanted leading to a more homogeneous S/D doping regions.

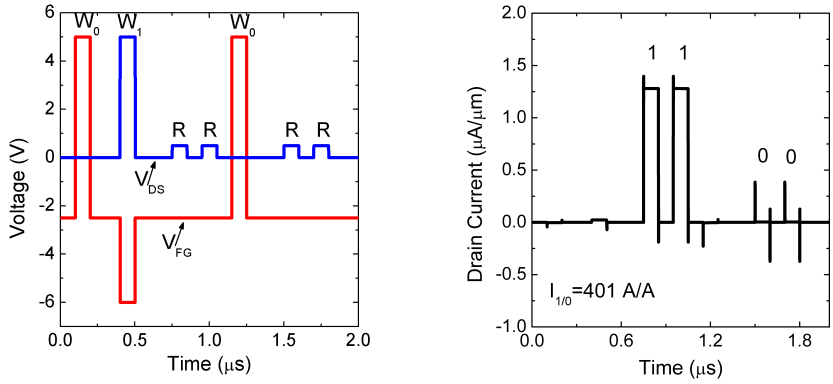
The memory behavior is verified by applying the following sequence: $W_0 \mid W_1 \mid R \mid R \mid W_0 \mid R| \; R$. The bias pattern and the readout current for the SOI CNM simulated sample are depicted in Figure 4.30.

The driven drain current during '1' and '0' memory states are very different. A current margin of more than 400 is extracted confirming the



(a) Linear scale (b) Logarithmic scale

FIGURE 4.29: Drain current comparison for Silvaco Athena® modeled A2RAM cells and transistors (without the As implantation) in bulk (dashed lines) and SOI (solid lines). **(a)** Linear and **(b)** logarithmic scale. $V_{DS} = 0.5\,V$ and $V_S = V_{BG} = 0\,V$.



(a) Bias pattern applied (b) Drain current readout

FIGURE 4.30: Silvaco simulated **(a)** Bias pattern applied to SOI CNM samples and **(b)** drain current readout. $V_S = V_{BG} = 0$ V.

A2RAM memory operation in SOI. A different result is found in case of bulk samples where no significant current margin is obtained (the current ratio arrives only to 1.2), Figure 4.31.

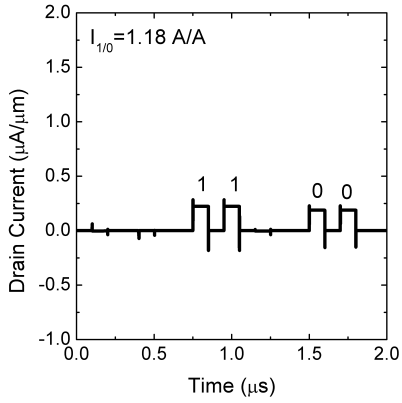


FIGURE 4.31: Silvaco simulated current readout for bulk CNM sample. The bias pattern applied is the same as Figure 4.30 **(a)**.

The reason of this contrast regarding the substrate employed is motivated by the difficulty of fully depleting the N-Bridge in bulk A2RAM cells. It has been shown how the doping profile of bulk A2RAM extends deeper inside the silicon substrate. This suggests the need of a larger negative voltage at the front-gate to effectively cut the bottom electron channel. Nevertheless, a more negative bias at the front involves a higher injection of carriers due to BtBT at the drain edge degrading the retention time.

4.4. Conclusions

In this chapter the fabrication processes of the A2RAM cell in both SOI and bulk substrates have been modeled and electrically simulated using

Silvaco® tools. It has been checked that the simulated A2RAM cells present the same behavior and performance as the theoretical concept, pointed out in Chapter 3. The simulations carried out show that these cells are a promising candidate for floating-body FB-DRAM. This suggests that A2RAM cells are feasible and should be manufactured for further experimental studies.

Actual samples of A2RAM cells are experimentally characterize in the following chapters. In Chapter 5, results from samples coming from CNM are discussed while in Chapter 6 more advanced A2RAM cells from CEA-LETI will be studied.

Chapter 5

A2RAM Cells Fabricated at CNM

This chapter contains the first experimental measurements performed on Advanced 2 RAM cells using a $2.5\mu m$ *CMOS process. The Centro Nacional Microelectrónica, CNM, at Barcelona has been in charge of the fabrication of the SOI and bulk samples used by taking into account the preliminary numerical simulations results obtained in Chapter 4. Firstly, some static properties will be studied and then their properties as a memory will be discussed.*

5.1. Static Characteristics

The basic information regarding the wafer properties and manufactured devices is presented in this section together with the transistors switching operation to check its static characteristics. Several SOI and bulk wafers were fabricated employing different implantation energies and doses but only the

best results are shown in this Chapter. A photography of one of these CNM A2RAM 100 mm wafer is shown in Figure 5.1.

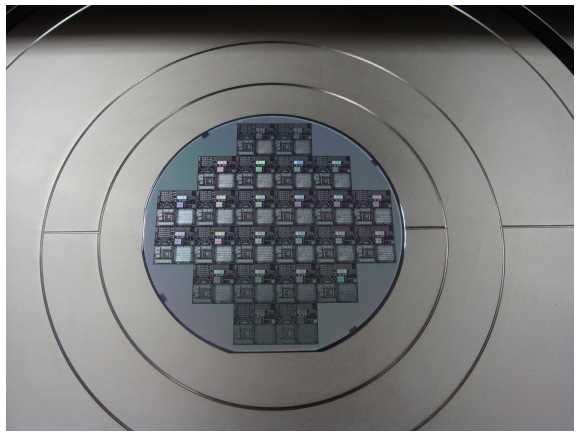


FIGURE 5.1: CNM bulk 100 mm A2RAM wafer.

5.1.1. Device Introduction

The fabrication steps followed for both substrates, bulk and SOI, were the same as those depicted in Chapter 3 for CNM A2RAM cells. In case of bulk, the initial substrate was an unprocessed and non-doped (100) wafer whereas for SOI, the starting substrate was an (100) UNIBOND® wafer, both of them of 100 mm diameter (4 inches). The main properties of both wafers and manufactured devices are summarized in Table 5.1. The thicknesses of the different films in the SOI devices are much thicker than those for state-of-the-art SOI MOSFETs (see typical ET FD-SOI transistors in Appendix B). Indeed, this thinning gives an idea of which has been the scaling trend followed during last years.

The N-Bridge was achieved in both cases by using an arsenic ion implantation with the parameters summarized in Table 5.2.

	Parameter	Symbol	Value	Units	
SOI	Silicon Film Thickness	t_{Si-P}	350	nm	Si
	Buried Oxide Thickness	t_{BOX}	400	nm	SiO_2
Both	Front-Gate Oxide	t_{ox}	10	nm	SiO_2
	Mask Gate Length	L	4	μm	-
	Mask Gate Width	W	30	μm	-

TABLE 5.1: Properties of A2RAM cells fabricated at CNM in 2.5 μm technology.

	Parameter	Representation	Value	Units	
Bulk	Energy	E_{Im}	400	KeV	-
SOI	Energy	E_{Im}	200	KeV	-
Both	Dose	D_{Im}	$8 \cdot 10^{11}$	cm^{-2}	As

TABLE 5.2: Properties of the ionic implantation used to create the N-Bridge for the A2RAM cells from CNM (bulk and SOI).

The final net doping profiles after all thermal load simulated with Athena® were illustrated already in Figure 4.28 **(a)** for SOI and **(b)** bulk. The arsenic implantation defines the buried N-type region more doped than the initial P-type substrate. This is the N-Bridge that connects the source and drain regions and defines the device as an A2RAM cell.

5.1.2. Switching Properties

For static switch operation, the A2RAM cell, as briefly commented in Chapter 4, can be considered as a **transistor with a resistor (N-Bridge) in parallel** between the source and drain regions (see Figure 5.2). Figure

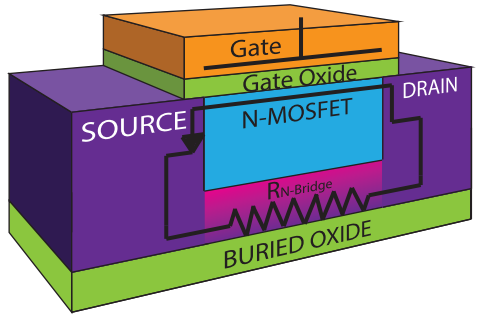
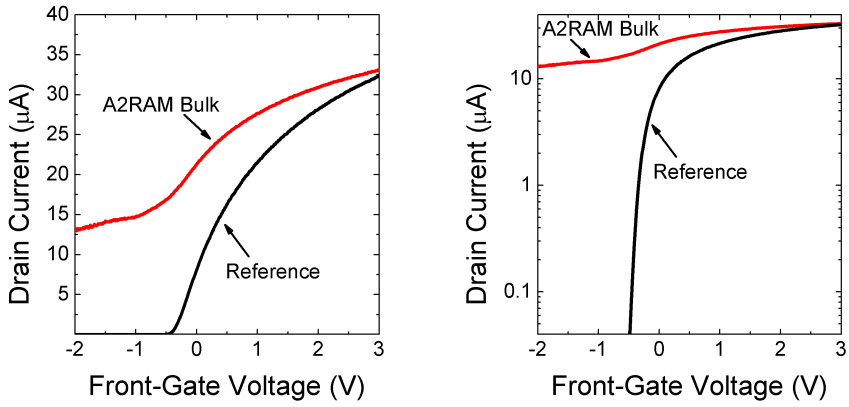


FIGURE 5.2: A2RAM cell showing its equivalent structure with a regular N-MOSFET and a connected resistor, $R_{N-Bridge}$, in parallel between source and drain regions. Although in the picture only the SOI substrate is represented, A2RAM cells on bulk substrates exhibit a similar scheme.

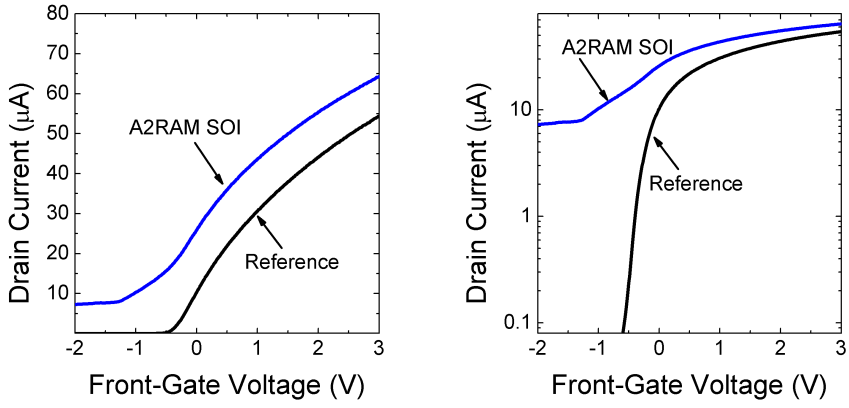
5.3 presents the bulk A2RAM cell drain current compared to a standard N-MOSFET without the steps required to define the N-Bridge in **(a)** linear and **(b)** logarithmic scale. As can be noticed, the current driven by the A2RAM cell is shifted upward with respect to the non-implanted transistor. This current shift appears regardless the front-gate bias applied (even in weak accumulation with the gate voltage lower than the flat band voltage, $V_{FG} < V_{FB-FG}$). This suggests that the device operation can be successfully decomposed into a regular drain current curve of a N-MOSFET transistor and another current term due to a resistor connected in parallel (since the drain current shift is not really constant for all gate voltages applied, the resistor value would neither be perfectly constant).

The same vertical shift is found for SOI A2RAM samples in Figure 5.4. In this case the shift is more constant for all the front-gate bias range considered. This fact reflects a more homogeneous resistance thank to the good controllability of the implantation when defining the N-Bridge. In SOI samples the BOX stops the ions implanted leading to a **more uniform N-Bridge**.



(a) Linear scale (b) Logarithmic scale

FIGURE 5.3: **(a)** Linear and **(b)** logarithmic drain current against the front-gate voltage of implanted bulk A2RAM transistors from CNM and reference transistor. $L = 4\,\mu m$, $W = 30\,\mu m$ and $V_{DS} = 100\,mV$



(a) Linear scale (b) Logarithmic scale

FIGURE 5.4: **(a)** Linear and **(b)** logarithmic drain current against the front gate voltage of implanted SOI A2RAM transistors from CNM and reference transistor. $L = 4\,\mu m$, $W = 30\,\mu m$ and $V_{DS} = 100\,mV$

In both bulk and SOI A2RAM devices, because of the parallel resistance, the switch of the devices is not well defined as inferred from the subthreshold swing depicted in the logarithmic scale plots in Figure 5.3 **(b)** and 5.4 **(b)**. It is important to remark that the same behavior was already demonstrated by simulations in Chapter 4, Figures 4.12 and 4.29.

No further parameters extraction or studies have been performed attending to static measurements with these CNM samples.

5.2. FB-DRAM Operation

In this section the memory capabilities of these A2RAM samples is verified. The hysteresis cycle, current ratio and retention time are extracted and discussed.

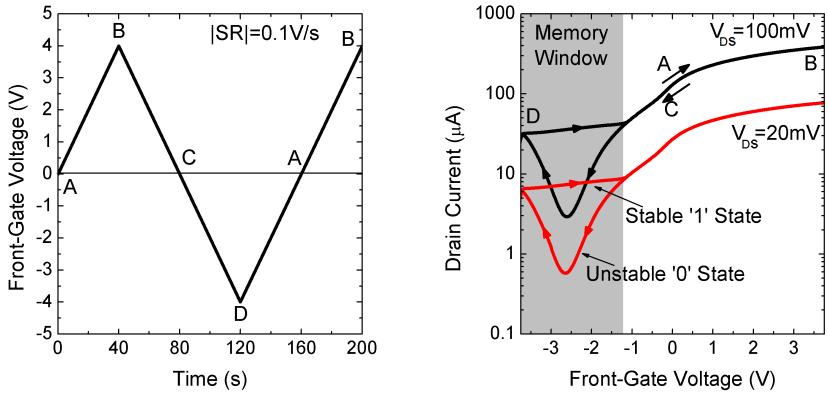
5.2.1. Hysteresis Cycle

The **hysteresis** is the dependence of the current of the device with its past environments. This implies that, in case of the A2RAM cell, it stores some information about its own past (memory effect). Regarding SOI MOSFETs, thanks to the floating-body effect, if a cycle of hysteresis is found, it suggests that the transistor has a chance to work as a DRAM. So, to verify the memory capability of a device, it can be checked the *hysteresis cycle* by applying an adequate bias pattern. The aim is to **check if there exists an operation region in the device where an electrical parameter depends on the bias applied but also on the previous state of the device**.

In case of the A2RAM cells, the parameter scanned for a hysteresis cycle is the drain current as a function of the front-gate voltage. The voltage pattern

applied to the front-gate is depicted in Figure 5.5 **(a)**, where a complete loop ranging from $V_{FG} = 0$ V to $V_{FG} = \pm 4$ V is used with constant **SR** (*Scan Rate* or slope), given by Equation 5.1.

$$SR = \frac{\Delta y}{\Delta x} = \frac{\Delta V_{FG}}{\Delta t} = 0.1\, V/s \tag{5.1}$$



(a) Front-gate bias pattern applied (b) Hysteresis cycles in I_{DS}

FIGURE 5.5: **(a)** Front-gate bias pattern applied to sense the hysteresis cycle with a scan rate of 0.1 V/s. **(b)** Drain current driven as a function of the front-gate bias time-dependent pattern, V_{FG} for several drain voltages applied to the SOI samples. $L = 4\,\mu m$, $W = 30\,\mu m$, $t_{Si} = 350\,nm$, $t_{BOX} = 400\,nm$ and $t_{ox} = 10\,nm$.

From low negative to high positive front-gate biases applied, no significant difference, regardless the sense of sweep or the drain bias considered, is obtained in drain current, Figure 5.5 **(b)**. However, **a clear hysteresis cycle is obtained in the negative front-gate bias region of operation**. The drain current obtained depends on the bias pattern applied as follows:

A→B The front-gate bias is gradually biased to higher voltages from $V_{FG} = 0$ V to $V_{FG} = 4$ V ($SR = +0.1$ V/s). The body potential rises

and the PN junctions formed by body-source and body-drain are forward biased so that **holes are expelled from the top channel**. The sensed current is due to the creation of the front-channel.

B→C The gate bias is then changed from $V_{FG} = 4$ V to $V_{FG} = 0$ V ($SR = -0.1$ V/s). The drain current decreases because the channel moves from strong to weak inversion and finally to cut-off. The potential in the body drops so that PN junctions are no longer forward biased and the **evacuation of positive charge ceases**.

C→D Next, the front-gate voltage goes from $V_{FG} = 0$ V to $V_{FG} = -4$ V ($SR = -0.1$ V/s). Since there are no holes inside the body (they 'all' were expelled) and since no immediate source of holes is available but thermal generation (very slow process), the body enters in the **deep depletion** region of operation. In this mode, an accumulation layer formed by positive charge cannot take place so the influence of the vertical electric field fully depletes the N-Bridge. The current driven by the N-Bridge is then cut-off (largest drop in drain current starting at $V_{FG} = -1.25$ V). At the same time **positive charge is gradually injected by BtBT** as gate bias gets more negative (the positive rise in current starting at $V_{FG} \simeq -2.5$ V). These generated charges are collected below the front-gate oxide restoring the population of majority carriers in the potential well (P-type body) and reducing the level of depletion in the N-Bridge. So, *deep depletion* mode last till a stationary equilibrium state is achieved. This **low current region of operation is the unstable state '0'**.

D→A Finally the gate is biased from $V_{FG} = -4$ V to $V_{FG} = 0$ V ($SR = +0.1$ V/s). The amount of positive charges is already restored implying that the N-Bridge is no longer depleted (holes screen the front-gate induced electric field on the N-Bridge). Therefore, the sensed

drain current follows the typical enhancement in a N-MOS transistor plus the drain current driven by the non-depleted N-Bridge. This **high drain current region is the '1' memory state**.

The window in the hysteresis cycle (difference between the two memory states) strongly depends on how fast the front-gate changes. Given that the state '0' is unstable due to thermal generation of positives charges inside the body, if the scan rate gets faster less holes would be generated at a time. *Deep depletion* regime will then last longer and the difference between states should be thus increased. This is confirmed in Figure 5.6 where the current ratio has been extracted as a function of the scan rate (SR) used. An almost linear rise with increasing scan rate speed is found for the tested SOI device.

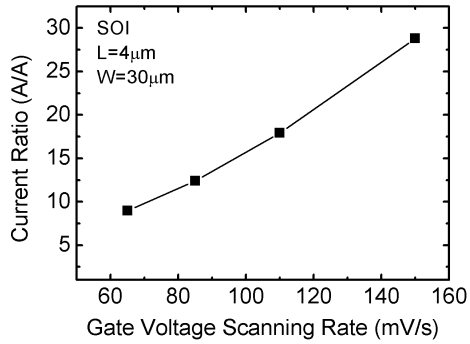


FIGURE 5.6: Current ratio between stable and unstable memory states at $V_{FG} = -2.5$ V for different scanning rates of the front-gate bias for SOI samples. As the front-gate sweep gets faster, the current ratio increases.

The current ratio increases rapidly with faster signals. This anticipates the good performance that is observed when the device is operated at much **higher frequency**.

Once confirmed the viability of the A2RAM samples fabricated at CNM, the current ratio and retention time are characterized.

5.2.2. Current Margin and Current Ratio

The drain **current margin** is defined as the difference in drain current between memory states, Equation 5.2. Since both memory states change with time, the current margin will also depend on the elapsed time.

$$\boxed{\Delta I_{1-0}(t) = I_1(t) - I_0(t)\,[A]} \tag{5.2}$$

An example of a MSD DRAM cell showing the two memory states current (open circles for '0' and squares for '1') and its current margin (open triangles) is represented in figure 5.7. The state '1' and state '0' get closer as time passes, aiming both to the stationary drain current level of the memory cell. This makes sense: for the state '1', the **initial hole overpopulation is lost by recombination and leakage**, this causes the threshold voltage to increase leading to a decrease in the drain current. On the other hand, the state '0' current increases, the thermal generation of carriers starts to re-populate the body with holes reducing the threshold voltage. These parasitic effects make the current margin to decrease with time. This implies that the sensing of the memory cell needs to be performed before this current margin is too small. Doing so, the sense amplifiers would be able to discern the state stored so that the information is not lost.

On the other hand, the **current ratio** is calculated by using Equation 5.3 at a given time t. Its value represent how large the '1' state drain current is

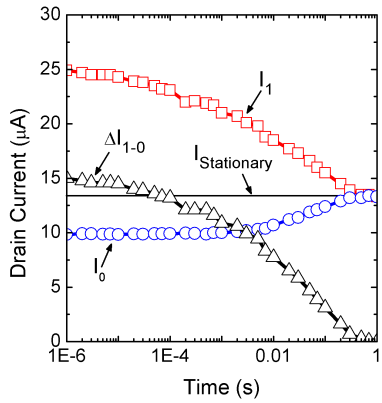


FIGURE 5.7: MSD FB-DRAM cell drain current states and current margin. High current state '1' (squares) and low current state '0' (circles) evolve with time arriving to the stationary current level where they are indistinguishable. The current margin, obtained by subtracting them and illustrated in triangles, also depends on time and approaches zero when both levels of current are similar.

compared to the '0' state.

$$\boxed{\Delta I_{1/0}(t) = \frac{I_1(t)}{I_0(t)}\ [A/A]} \tag{5.3}$$

The current margin gives an absolute value while the current ratio provides a relative value to characterize the cell performance. The use of one or another would depend on the application and context.

In case of the A2RAM, the operation depends on the front-gate bias applied. Whatever is the memory operation considered, *write*, *erase* or *hold*, the front-gate drives the result. In any of the cases but *hold*, the front-gate only aims to control one state, either W_1 by BtBT with large negative bias or W_0 by forward biasing the PN junctions with positive bias. However, in case of *hold*

operation, there exist a tradeoff because this operation must deal with both '1' and '0' states at the same time. If the front-gate *hold* bias is very negative, the injection of holes is more effective and the device will recover faster from *deep depletion* aiming to its equilibrium state. If, on the other hand, *hold* bias is close to zero, the electric field will no longer be able to fully deplete the N-Bridge and the current during state '0' would be not negligible. This strong correlation of cell behavior and front-gate *hold* bias motivates the extraction of the main memory parameters as a function of it.

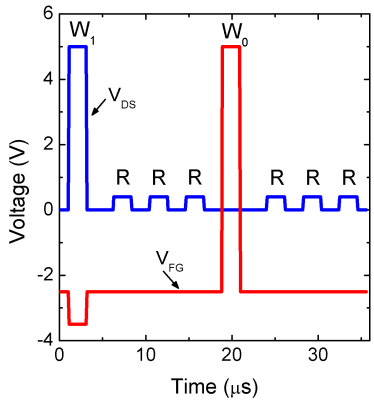
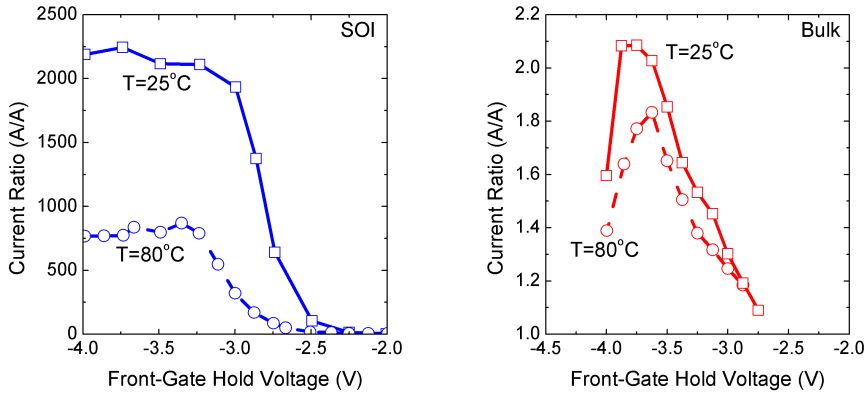


FIGURE 5.8: Bias pattern to extract the current ratio in CNM A2RAM cells. Although a front-gate hold voltage sweep has been performed, in this figure only one holding bias is represented.

The applied bias pattern to characterize the current ratio of the A2RAM cells fabricated at CNM is illustrated in Figure 5.8. Only one of the front-gate *hold* voltages considered is represented. The operation sequence is as follow: $W_1 \mid R \mid R \mid R \mid W_0 \mid R \mid R \mid R$.

The current ratio is depicted for a wide range of hold gate bias in Figure 5.9 **(a)** for the SOI samples and two different temperatures (room temperature and $T = 80$ °C). The current ratio is calculated as the ratio of both memory states



(a) SOI samples (b) Bulk samples

FIGURE 5.9: Current ratio between '1' and '0' states as a function of the front-gate bias during hold operation for **(a)** SOI and **(b)** bulk samples and several temperatures. $V_{DS} = 100\,mV$, $L = 4\,\mu m$, $W = 30\,\mu m$ and $t_{ox} = 10\,nm$.

10 μs after the writing operations. The results show **current ratios over 2000 A/A** for room temperature and hold gate bias below -3 V. For $T = 80$ °C, the current ratio falls to 700 A/A. This drop is related to the higher thermal generation rate with increasing temperatures affecting the state '0'. As the hold bias goes toward zero volts from -3 V, the current ratio rapidly degrades for any temperature as a consequence of the partial depletion of the N-Bridge that increases the drain current during state '0'. For hold front-gate voltages over -2 V the drain current difference vanishes meaning that the N-Bridge is completely not depleted during the low current state.

The bulk case is illustrated in Figure 5.9 **(b)**. The first point to notice is that the current ratio obtained for any given *hold* gate bias is dramatically reduced with respect to the SOI results previously shown. It drops from values over 2000 to hardly surpass a factor 2 at room temperature, showing

similar current in both states. Furthermore, in case of bulk samples, there is no constant current ratio region for very negative front-gate voltages. Once the maximum value is achieved around $V_{FG} = -3.75$ V (depending on the temperature), the current ratio starts to fall again for more negative front-gate voltages.

The difference in current ratios between technologies illustrates the benefits obtained when using the buried oxide in the A2RAM performance. Nevertheless, it should be pointed out that the bulk CNM samples suffered a problem while being fabricated that is responsible for this so degraded performance. Finally, it is worth noting that the current ratios obtained experimentally are in the same order of magnitude to those obtained with simulations in Chapter 4.

5.2.3. Retention Time

The **retention time**, t_{ret}, is probably the most important parameter of any Dynamic RAM cell. In case of a floating-body DRAM, it is strongly linked with the drain current margin (ΔI_{1-0}) and with the current sensitivity of the sense amplifiers ($I_{Sensitivity}$). It is defined as the maximum time the cell maintains its memory state readable counting from the last operation (*write/erase/refresh*). This implies that after the retention time the sensing circuitry is no longer able to discriminate between the two memory current levels (see Equation 5.4).

$$\boxed{\Delta I_{1-0}(t_{ret}) = I_1(t_{ret}) - I_0(t_{ret}) = I_{Sensitivity}\,[A]} \tag{5.4}$$

Figure 5.10 shows the retention time extraction for a given amplifier sensitivity. It can be seen how if the sensitivity is enhanced (the minimum

drain current difference is reduced, $I_{Sensitivity}$ goes downward), the retention time would be increased (t_{ret} goes to the right).

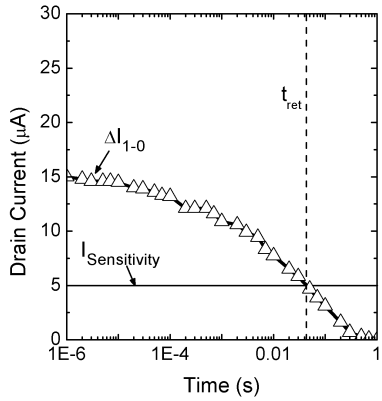


FIGURE 5.10: MSD FB-DRAM cell retention time based on current margin and sense amplifier sensitivity. The current margin, I_{1-0}, and amplifier sensitivity, $I_{Sensitivity}$, define the retention time at the point where they cross.

Other retention time definitions use a relative difference between the high and low current levels. The benefits of these interpretations is that they do not depend on a external circuit so that they are easier to compare. One of them is usually defined as the time the current margin takes to decrease a given percentage of its initial value, $\Delta I_{1-0}(0)$, Equation 5.5.

$$\boxed{\Delta I_{1-0}(t_{ret}) = I_1(t_{ret}) - I_0(t_{ret}) = a \cdot \Delta I_{1-0}(0)\ [A]} \tag{5.5}$$

The retention time extraction based on the percentage current margin decay is illustrated in Figure 5.11 for a value $a = 50\%$.

Finally, the last definition considers the retention time to be the time it takes the most unstable current state to be a given percentage close to the

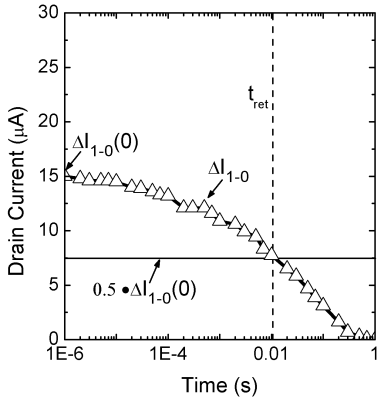


FIGURE 5.11: MSD FB-DRAM cell retention time based on current margin half decay. The time it takes the current margin to fall to a 50 % of its initial value defines the retention time.

stationary current state. It is defined as shown in Equation 5.6 when the unstable state is the '0' and in Equation 5.7 when is the '1'.

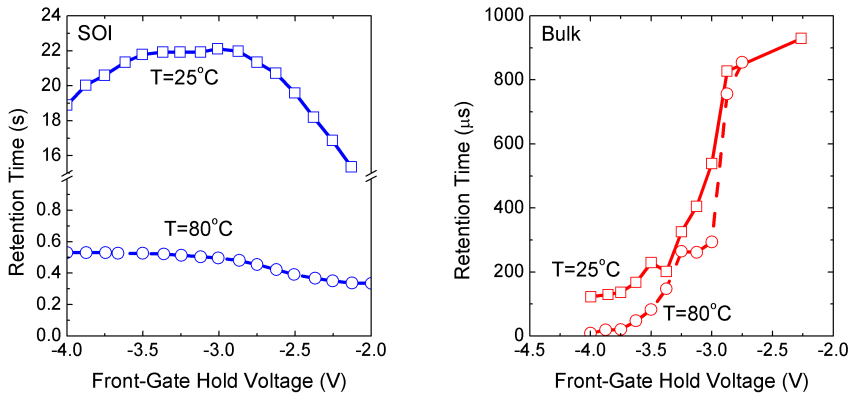
$$\boxed{I_0(t_{ret}) = (1-a) \cdot I_0(t \to \infty)\,[A]} \tag{5.6}$$

$$\boxed{I_1(t_{ret}) = (1+a) \cdot I_1(t \to \infty)\,[A]} \tag{5.7}$$

Now, the constant a expresses the over or under-current percentage (normalized to 1) allowed in the retention time, depending if the most unstable current state is the '0' or '1' respectively.

As happened with the current ratio, the retention time is also extracted as a function of the front-gate bias during *hold* operation. The bias pattern applied consists in two long *read* events after a *write* and *erase* operations (pattern not shown). Figure 5.12 **(a)** exhibits the retention time obtained

in case of the SOI samples for the two temperatures considered before. The retention time definition used is based on Equation 5.6 with $a = 0.5$. In case of the lower temperature ($T = 25$ °C), the retention times achieved **maximum values around 22.5 s** for a front-gate voltage of -3 V, which happily matches also the best case of the best current ratio. If the temperature increases to $T = 80$ °C, the retention time is strongly affected and falls to 0.5 s at the same gate bias (the thermal generation degrades the state '0' faster for high temperatures). If the gate voltage is further reduced (more negative), the retention time slightly drops or is maintained for low and high temperatures respectively. These high retention time values are motivated by the size of the device that allows it to store a high amount of holes and thus to effectively screen the depletion of the N-Bridge.



(a) SOI samples (b) Bulk samples

FIGURE 5.12: Retention time as a function of the *hold* front-gate voltage for **(a)** SOI and **(b)** bulk samples for several temperatures. $V_{DS} = 100$ mV, $L = 4$ μm, $W = 30$ μm and $t_{ox} = 10$ nm.

A strong drop in the retention time is found when moving to bulk A2RAM samples in Figure 5.12 **(b)**. It can be seen how the t_{ret} is reduced to maximum

values around 1 ms (4 orders of magnitude less than SOI) and there is not a significant dependence on temperature. This change is motivated by the lower current margin obtained where the state '0' rapidly arrive to 50 % of the equilibrium current value.

Previous results point out the feasibility of both A2RAM substrates configuration. The SOI samples present extraordinary current ratios and even better retention times. Nevertheless it should be taken into account the size of these devices that makes them more suitable for embedded applications. On the other hand, the bulk substrate samples show a degraded operation suggesting that further optimization in the fabrication process is required to improve their characteristics.

Lastly, it is worth highlighting that **the mechanism that limits the retention time in large SOI devices is the thermal generation** rather than any other method. This is demonstrated by observing the dramatic dependence of the retention time with temperature, Figure 5.12 **(a)**.

5.2.4. Cumulative Statistical Distributions

To conclude, a statistical study is performed to show the retention time cumulative distribution for these samples. These type of representations allow a rapid view of the variability of a given memory cell. A higher slope is desirable since it implies low variability. Almost the same dependence (slope) is found for different temperatures and substrates, Figure 5.13. The SOI A2RAM cells present outstanding retention time characteristics with average t_{ret} well above 10 s and 300 ms for low and high temperature (2 orders of magnitude decay with temperature due to thermal generation). In contrast, the obtained bulk A2RAM average retention time is below 10 ms even for the lowest temperature stating the need of an optimization process for these samples.

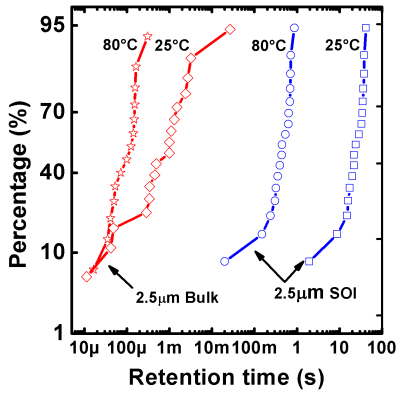


FIGURE 5.13: Cumulative statistical distribution of the retention time for both types of substrates and several temperatures. $V_{DS} = 100$ mV, $L = 4$ μm, $W = 30$ μm and $t_{ox} = 10$ nm.

It is important to notice that the distributions present low variability (almost vertical lines), specially in case of the SOI A2RAM samples. This fact points out an almost **homogeneous retention time** for any cell considered which is extremely important for future DRAM candidates.

5.3. Conclusions

In this chapter, experimental results of A2RAM samples fabricated using 2.5 μm technology are extracted and discussed. Basic static switching properties, the hysteresis cycle, retention time and current ratio parameters are shown for both SOI and bulk substrates. While bulk samples performance is rather poor, SOI samples provide astonishing results as a memory cells. Further optimization process is required for competitive bulk samples.

The large size of the devices studied in this Chapter 5 makes them not suitable for ultimate applications. In the next Chapter 6, **smaller and more advanced samples fabricated at CEA-LETI** will be presented.

Chapter 6

A2RAM Cells Fabricated at CEA-LETI

After studying the large A2RAM samples coming from the CNM, experimental results from more scaled and advanced A2RAM cells fabricated at CEA-LETI are detailed in this chapter. In the first section, the properties and main characteristics of the wafer and the devices will be summarized, the basic parameters like the threshold voltage, mobility... will be also obtained. In the second section, the capabilities as memory cells of these devices will be verified and their main properties like the retention time and current margin will be characterized.

6.1. Implanted SOI-MOSFETs. A2RAM Cells

In this first part of the chapter the A2RAM cells will be treated as a typical switching transistor obtaining all the main parameters that will be compared

with those extracted for state-of-the-art ET FD-SOI MOSFETs in Appendix B. The differences with respect to a regular transistor will be manifested and discussed. A photography of the A2RAM 300 mm wafer is shown in Figure 6.1.

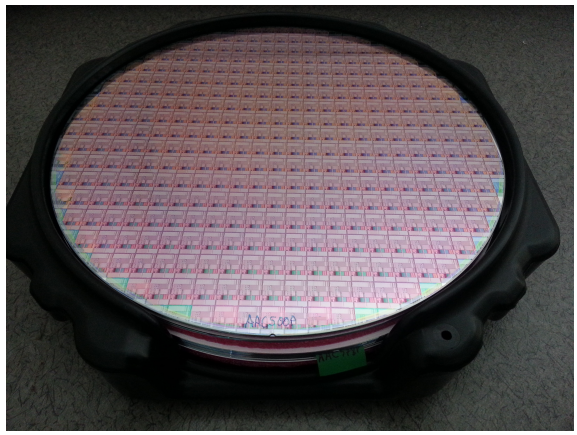


FIGURE 6.1: CEA-LETI 300 mm A2RAM wafer.

6.1.1. Device Introduction

The fabrication of these cells was performed by the *Commissariat l'Énergie Atomique et aux énergies alternatives*, CEA-LETI, in Grenoble, France. The A2RAM, Figure 6.2, main parameters appear listed in Table 6.1. The first A2RAM cells fabricated at CEA-LETI have a thicker silicon film than state-of-the-art SOI MOSFETs (as those characterized in Appendix B). The reason of using an initial thicker Si-film is to demonstrate the A2RAM feasibility before moving to its limits.

The fabrication process is described in Chapter 3. The technological parameters of the ion implantation used to create the N-Bridge are listed in Table 6.2. The angle used in the implantation is necessary to avoid or to

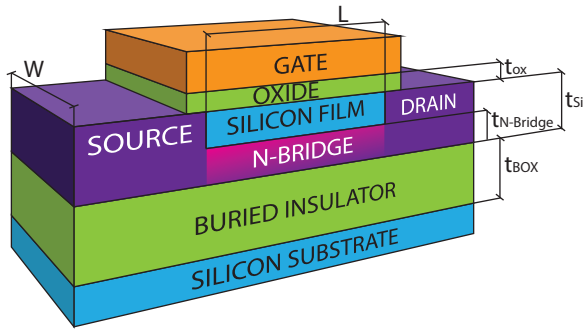


FIGURE 6.2: Diagram of typical A2RAM transistor used as a memory cell.

Parameter	Symbol	Value	Units	
Silicon Film Thickness	t_{Si}	36	nm	Si
N-Bridge Film Thickness	$t_{N-Bridge}$	≈20	nm	-
Equivalent Oxide Thickness	EOT	3.1	nm	HfO_2
Buried Oxide Thickness	t_{BOX}	10	nm	SiO_2
Mask Gate Length	L	30-10.000	nm	-
Mask Gate Width	W	80-10.000	nm	-

TABLE 6.1: *Properties of the CEA-LETI A2RAM memory cells.*

favor the *ion channeling* (implanted ions reach deeper in the sample due to the existence of privileged paths in the lattice). The applied energy and dose were selected to fit the requirements for the N-Bridge.

Parameter	Representation	Value	Units	
Implantation Energy	E_{Im}	1	KeV	-
Dose	D_{Im}	$3 \cdot 10^{12}$	cm^{-2}	As
Angle	θ_{Im}	7	°	-

TABLE 6.2: Properties of the ion implantation used to create the N-Bridge for the A2RAM cells.

The final net doping profile of the A2RAM memory cell obtained from Athena® process simulator is represented as a function of the depth of the device in Figure 6.3; an identical wafer without the implantation has been considered for comparison. Both body doping concentrations are constant and equal on the top of the silicon film due to the initial uniform concentration of the P-type wafer. A gaussian doping concentration profile is found at the bottom of the implanted cell. This is motivated by the arsenic implantation and its posterior diffusion during the selective epitaxial growth. The result is a vertical P^-N^+ junction. Note that **the retrograde doping profile has been successfully achieved in a 36 nm thick Si-film**.

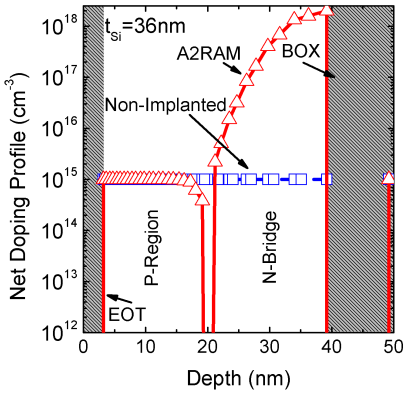
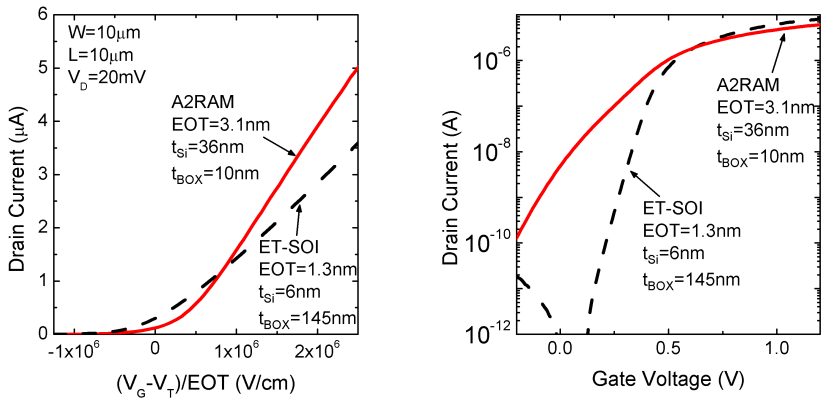


FIGURE 6.3: Net doping profile of the A2RAM cell (triangles) obtained from Athena® process simulation. For comparison, a non-implanted cell is also represented (squares). The ion implantation leads to a vertical P^-N^+ junction inside the body of the A2RAM cell.

Now the electrical behavior as a transistor will be checked and compared with the ET FD-SOI samples (Appendix A). In each case, the technique employed will be mentioned and the main differences will be highlighted.

6.1.2. Drain Current

Figure 6.4 **(a)** illustrates the drain current comparison between A2RAM cells and ET FD-SOI MOSFETs against the overdrive voltage (applied gate voltage over the threshold voltage $V_{FG} - V_{Th}$) normalized by the front-gate oxide thickness. This representation provides a fairer comparison since neither the front-gate oxide nor the threshold voltage are the same in both types of devices. The result shows a **larger drain current in implanted A2RAM devices**, mainly motivated by the implicit connection due to the N-Bridge between source and drain regions. Unfortunately, this connection also implies higher drain current in the subthreshold regime, as shown in Figure 6.4 **(b)** where the drain current is represented in logarithmic scale.



(a) Linear scale

(b) Logarithmic scale

FIGURE 6.4: **(a)** Linear drain current as a function of the overdrive voltage normalized by EOT and **(b)** logarithmic drain current against the front-gate voltage of A2RAM transistors compared to ET FD-SOI devices. $L = 10\,\mu m$, $W = 10\,\mu m$ and $V_{DS} = 20\,mV$.

The last point that can be noticed is the different slope during the strong inversion regime (Figure 6.4 **(a)**). The reason is related to different effective

electron mobility values as will be discussed later.

6.1.3. Subthreshold Swing

The subthreshold swing is obtained against the mask gate length and compared in Figure 6.5 (the extraction method is discussed in Appendix A). In case of the ET MOSFETs, the subthreshold swing is much lower than for the A2RAM cells. The extracted slope values are close to the ideal $\simeq 60\, mV/dec$ at room temperature. These values differ significantly from those obtained in case of the A2RAM cells, always over 120 mV/dec and up to 350 % larger. The A2RAM subthreshold slope values fit better with those obtained for PD-SOI devices [Col04]. The **worse subthreshold swing in A2RAM cells** leads to a higher power consumption compared to non implanted transistors in OFF state. The influence of the N-Bridge in this parameter is very remarkable. For a typical transistor the change on drain current in the subthreshold regime is mandatory for the fast switching of the current. In the case of A2RAM, this change is less abrupt (larger swing values) because of the N-Bridge parallel resistor that always drives current if a drain bias is applied.

The presence of the As-implantation in A2RAM samples implies the difficulty to turn off the current driven due to the higher electron concentration in the body which also motivates a lower threshold voltage since it is easier to create the inversion channel. A2RAM off-state current leakage is prohibitive for present CMOS applications.

Finally, an increase in the subthreshold swing is observed when reducing the gate length of the transistors whether the device is implanted or not. This can attributed to a larger influence of the SCE's that provokes the loss of electrostatic control by the front-gate on the channel.

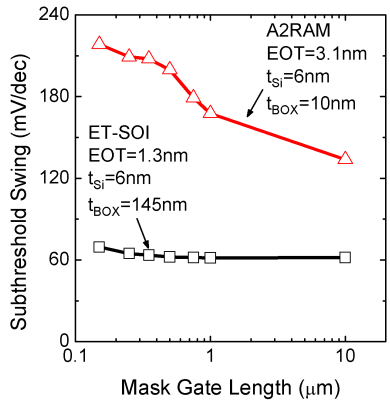


FIGURE 6.5: Subthreshold swing comparison between CEA-LETI A2RAM cells and FD-SOI transistors with ultra thin silicon film. $W = 10\,\mu m$.

6.1.4. Drain Induced Barrier Lowering

The drain induced barrier lowering has been extracted against the gate length (DIBL extraction is detailed in Appendix A). **Huge A2RAM DIBL values** are obtained. Up to 750 % over those obtained for the extremely thin silicon film transistors, Figure 6.6. The significant dependence against the gate length is clearly due to a lower influence of the gate on the channel onset when decreasing the distance between source and drain. These large DIBL values appear due to the thicker front-gate oxide in A2RAM cells, which implies a worse electrostatic control by the gate; also due to the thicker silicon film thickness but especially, due to the implicit connection of the source and drain through the N-Bridge. As gate length is reduced, DIBL increases due to a greater influence of the drain terminal on the potential barrier.

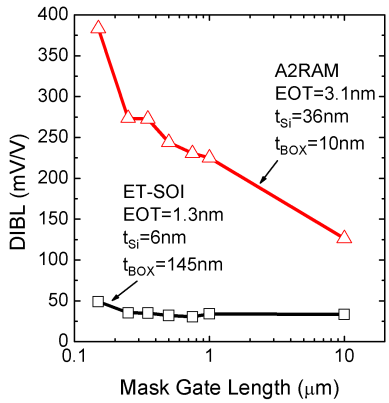


FIGURE 6.6: Drain induced barrier lowering comparison between CEA-LETI A2RAM cells and ET FD-SOI MOSFETs. $W = 10\,\mu m$.

6.1.5. Oxide Thickness

The front-gate oxide thickness study has first been performed through the electrostatic gate coupling method (discussed in Appendix B), in particular, the front-gate threshold voltage has been monitored for several back-gate biases. The resultant coupling curve is represented in Figure 6.7.

Given the high concentration of electrons in the N-Bridge, the front-gate threshold voltage is saturated already for an applied back-gate voltage of zero volts. In this case, the electrons screen the influence of the back bias on the front-gate and therefore for zero and higher positives biases the V_{Th-FG} remains constant implying no dependence with V_{BG} (**electron accumulation** in the N-Bridge). As the back bias moves towards negative values from zero volts, the electron concentration in bottom of the body starts to decrease (**N-Bridge depletion**) and the back-gate bias starts to influence the front threshold voltage (it does not remain constant anymore). This situation is hold

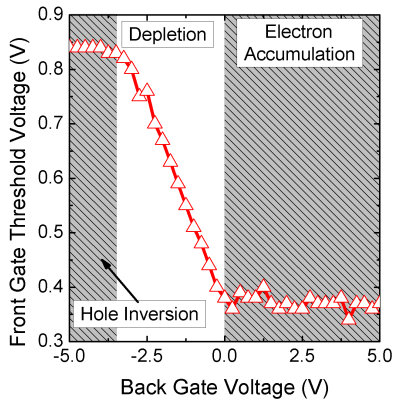


FIGURE 6.7: Front-gate threshold voltage dependence with the back-gate bias. Notice the unusual behavior of carrier gathering due to the N-Bridge in P-type body.

until the back-gate bias is negatively enough to collect a large concentration of holes at the back-interface, (**N-Bridge inversion with holes**). The hole populated back-channel screens again the influence of the back-voltage on V_{Th-FG} and leads to another flat region around $V_{BG} \simeq -3\,V$.

It is possible to relate the slope of the front-gate threshold voltage coupling in the depleted region (from $V_{BG} \simeq -3\,V$ to $V_{BG} \simeq 0\,V$), with the front-gate oxide thickness through Equation 6.1.

$$EOT = t_{ox} = -\frac{C_{Si} \cdot C_{BOX}}{m \cdot \epsilon_{ox} \cdot (C_{BOX} + C_{Si} + C_{it-BG})} = 3.18\,nm \tag{6.1}$$

where $D_{it-BG} \simeq 0\,cm^{-2} \cdot eV^{-1}$ has been considered. The extracted thickness is very close to the value calculated through **CET** (*Capacitance Equivalent Thickness*, see Appendix A) using the front-gate to channel capacitance in

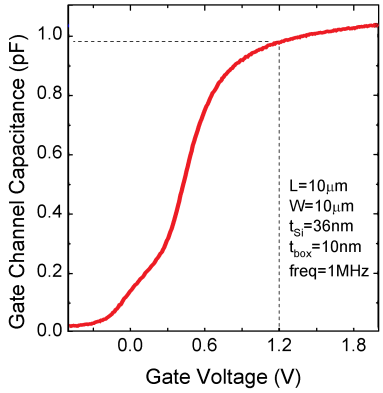


FIGURE 6.8: Front-gate to channel capacitance measurements to extract the equivalent oxide thickness.

Figure 6.8 (Equation 6.2).

$$CET = \frac{L \cdot W \cdot \epsilon_{ox}}{C_{GC}(V_{FG} = 1.2V)} \simeq 3.3\, nm \tag{6.2}$$

Both front-gate oxide thickness values match quite well the expected t_{ox} of 3.1 nm obtained from ellipsometry measurement [CSN+00] at the fabrication facility. Furthermore, the thickness obtained from the capacitance measurements of 3.3 nm is even better if the *dark space region* or *quantum depletion* is taken into account. This quantum effect appears as a **consequence of the vanishing probability of finding electrons at the** $Si - SiO_2$ **interface**. Consequently, the inversion-electron distribution shows a barycenter at a certain distance from the interface in contrast with the classical case that shows a maximum at the interface [HG05]. This yields to an increases in the effective thickness of the front-gate oxide because the charge is spaced from the interface. The effective thickness is then the insulator thickness

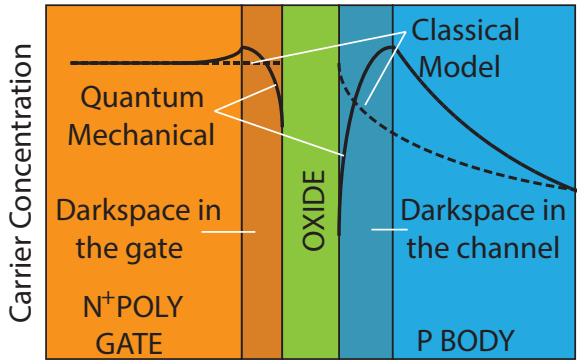


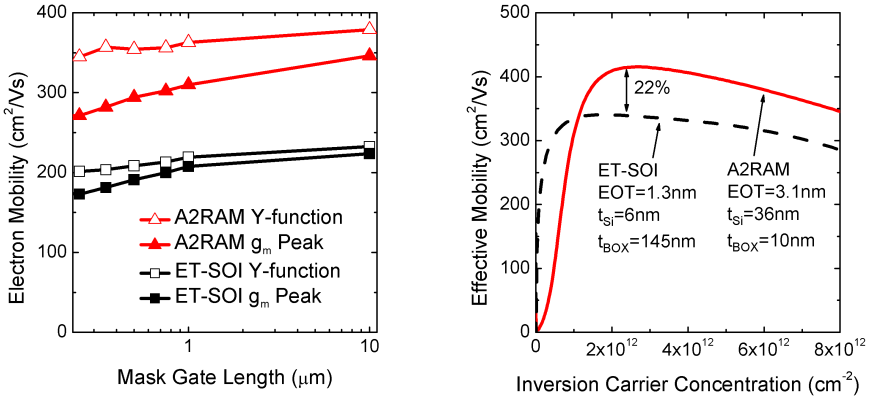
FIGURE 6.9: Dark space or quantum depletion representation in a N-MOSFET device. Notice the difference in electron profile distribution with the classical approximation in contrast to the quantum mechanical model [HG05].

plus the separation of the charge from the interface (Figure 6.9). This extra separation is very dependent of the gate bias and the body doping concentration and is usually taken as 9-12 Å for electrons and 15-18 Å for holes. Taking into account the dielectric constant difference between Si and SiO_2, the equivalent oxide thickness increase is 3 Å for electrons and 5 Å for holes [HG05]. So, the final results should be much closer to the expected value of 3.1 nm. The *dark space region* at the gate side will strongly depend of the material, being more important in poly-Si gates than metal gates such as TiN (the one used in the devices considered).

6.1.6. Mobility

The carrier mobility is extracted and compared to study the changes among the different devices. Mobility from Y-function (open symbols) [Ghi88] and transconductance peak (plain symbols) [Vas] have been extracted (see Appendix A) and compared in Figure 6.10 **(a)**. A carrier mobility degradation

appears when decreasing the channel length. This carrier mobility degradation can be attributed to several factors: **remote Coulomb scattering, interface states charges, ballisticity or process-induced defects near drain and source** [CRF+06, PNFBV+09]. Comparing both set of devices, it can be noticed how the A2RAM samples (triangles) present larger electron mobility values that ET-SOI (squares). There is also a difference in mobility values depending on the extraction technique employed. This **mismatch is originated by the series resistance effect**; while Y-function takes the first order SRE into account, the transconductance peak method does not, leading then to an underestimation of the mobility.



(a) Against the mask gate length

(b) Against the inversion carrier concentration

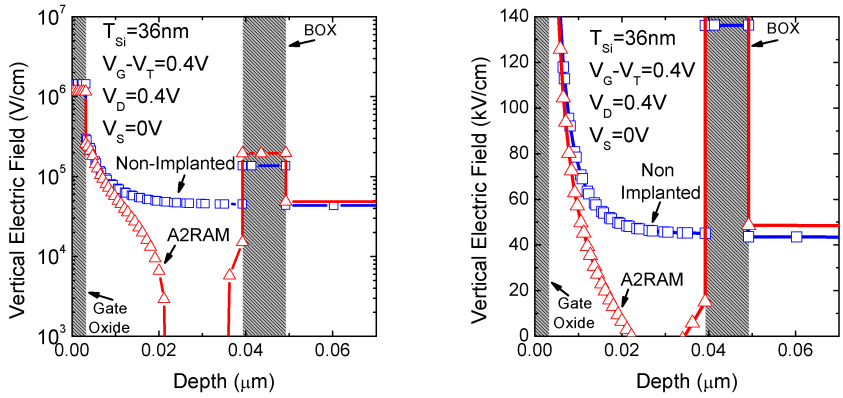
FIGURE 6.10: Mobility comparison between CEA-LETI A2RAM and ET FD-SOI transistors against **(a)** mask gate length ($W = 10$ μm) and **(b)** the inversion carrier concentration ($W = 10$ μm and $L = 10$ μm).

Figure 6.10 **(b)** illustrates the effective mobility against the inversion carrier concentration. The inversion charge has been extracted through capacitance measurements using the Split-C(V) technique [Sch06a] (see Appendix A). These results corroborate the carrier mobility difference between

A2RAM and ET-SOI devices previously found in Figure 6.10 **(a)**. A maximum electron mobility difference of 22% at an inversion charge close to $N_i = 2 \cdot 10^{12}\, cm^{-2}$ is calculated between A2RAM cells and the reference transistors.

There are several reasons for this remarkable difference in the mobility. On one hand, at low inversion charge, the A2RAM devices show **larger scattering by Coulomb centers** due to their large impurity concentration after the arsenic implantation to define the N-Bridge. This larger scattering for A2RAM cells leads to an initial smaller electron mobility (solid line compared to dashed line in Figure Figure 6.10 **(b)**). On the other hand, when the front-channel is strongly inverted, for inversion carrier concentrations over $N_i \simeq 10^{12}\ cm^{-2}$, the effective mobility of the A2RAM surpasses the mobility of ET-SOI transistors. This was intuited when observing the different slopes in Figure 6.4 **(a)** at large overdrive voltages. This enhanced in the mobility at strong inversion has been attributed to a **reduction in the effective electric field**. The vertical electric field profile within the body was simulated with Silvaco Atlas® for an arsenic implanted (A2RAM) and non implanted device (Figures 6.11).

The doping profiles for both devices were already shown in Figure 6.3. Results show a decrease of up to ten times in the vertical electric field in arsenic implanted transistors (A2RAM cells, triangles). This vertical field reduction motivates at the same time a reduction in the effective electric field (see Appendix C for more details about the effective field) that yields to an increase in carrier mobility as predicted by the *Universal Mobility Curve* [TTIT94a, TTIT94b]. These results present an important, and unexpected, enhance in electron mobility for implanted transistors. The doping concentration in the N-Bridge (large electron concentration) is able to reduce the vertical electric field. So, this back-channel implantation may be used for other devices to improve their performance. Nevertheless it only would be



(a) Logarithmic scale (b) Linear zoom

FIGURE 6.11: Atlas® simulated vertical electric field comparison between A2RAM and same but non-implanted wafer against wafer depth for **(a)** logarithmic scale. A linear zoom is represented in **(b)**.

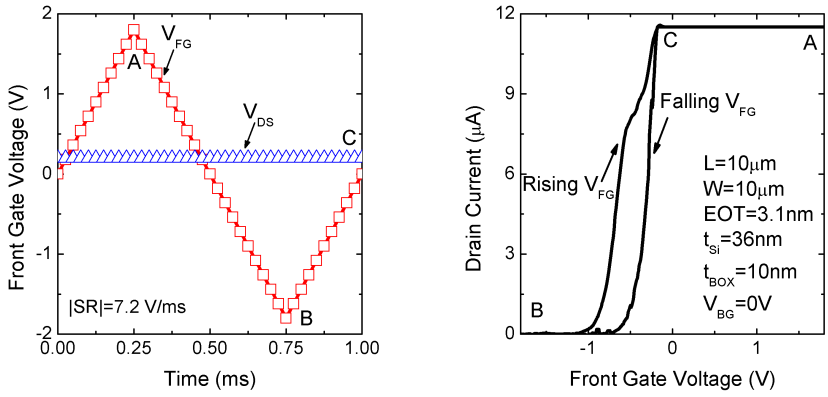
practical if both source and drain regions are not connected (the implantation does not cover all the silicon body). Otherwise, the static characteristics will be degraded as happens for the A2RAM cells.

6.2. A2RAM Capabilities as Memory

So far, typical characteristics of A2RAM cells operated as transistors have been discussed. In the rest of the chapter, the memory performance will be studied. To do so, the hysteresis cycle, the current ratio and the retention time will be investigated.

6.2.1. Hysteresis Cycle

The applied bias pattern to demonstrate the hysteresis cycle of the A2RAM cells is shown in Figure 6.12 **(a)**. The front-gate voltage is swept from $V_{FG} = +1.8$ V to $V_{FG} = -1.8$ V and the same way back while the drain bias is maintained constant at $V_{DS} = 0.2$ V. The A2RAM cell response is captured and illustrated in Figure 6.12 **(b)**.



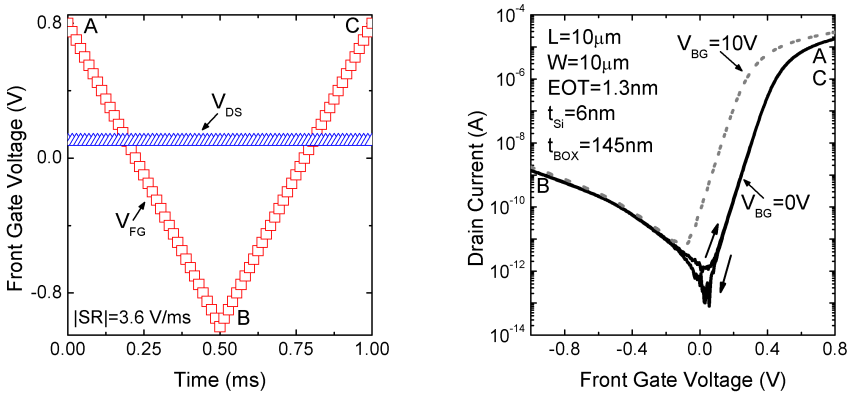
(a) Hysteresis bias pattern

(b) Drain current readout

FIGURE 6.12: **(a)** Pattern applied with $|SR| = 7.2\ V/ms$ and **(b)** drain current readout demonstrating the hysteresis of A2RAM cells with $V_{BG} = 0$ V.

Starting from point **A** and moving toward point **B**, the top interface goes rapidly from strong inversion to deep depletion. In the negative front-gate region, the top channel tends to be accumulated, but since there is no immediate source to provide holes (thermal generation takes a while), the top channel-interface remains depleted. Given that there is no significant charge concentration at the top, the electric field induced by the front-gate is not screened and fully depletes the N-Bridge of electrons. The result is that the drain current drops rapidly. If the front-gate bias is reduced enough, there

will be an important hole injection due to band to band tunneling process (GIDL). Injected holes will be collected in the potential well created at the top side of the silicon film screening the front-gate electric field. As more and more holes are collected the N-Bridge exits depletion and the drain current increases, **B** to **C**. This hysteresis result has been obtained with a grounded back-gate. This demonstrates that **it is not necessary to apply a back-gate bias to achieve the memory operation**.



(a) Logarithmic scale (b) Linear zoom

FIGURE 6.13: **(a)** Pattern applied and **(b)** drain current readout to check the hysteresis of ET FD-SOI transistors with and without a back-gate bias.

The same test can be carried out also for the extremely thin MOSFETs to check if they present a hysteresis cycle as well (memory effect). The pattern applied is represented in Figure 6.13 **(a)**. The driven drain current for two different back-gate biases is plotted in 6.13 **(b)**. A **very small hysteresis cycle** (in the range of pA) is obtained in the case of $V_{BG} = 0$ V (solid line). This hysteresis cycle is not enough to used these devices as a memory based on modulating the body majority carriers and MOSFET reading but, this does not imply that some other memory operation could be achieved with them. If

the hysteresis cycle is then tried to be enhanced by back-gate biasing, with a $V_{BG} = 10$ V (dashed line), it is not only not enhanced but it **totally vanishes due to the supercoupling effect** [ECC+07] (the silicon film thickness is only 6 nm).

Finally, it can be concluded that the characteristics presented by the ET FD-SOI transistors are specially interesting for their use as switching for *more Moore* applications but, they do not provide sufficiently good performance to be treated as floating-body DRAM cells. On the other hand, the arsenic implanted devices, A2RAM samples, exhibits poor characteristics as typical transistors but are in fact **suitable for the study as DRAM cells** applications due to their hysteresis cycle.

6.2.2. Pulsed Pattern Response

The first target for these A2RAM samples (once the memory operation was verified) was to investigate the optimal bias pattern applicable in order to obtain the best memory performance. To do so, many different voltage conditions were applied until the largest drain current margin between high and low current states was obtained. The pattern applied is based on pulses of 1 μs long. The final bias conditions are summarized in Table 6.3.

Operation	V_{FG} (V)	V_{DS} (V)
Read	-1.2	0.2
Write '1'	-1.7	0.85
Write '0'	0.85	0
Hold	-1.2	0

TABLE 6.3: Optimized bias pattern used for the A2RAM memory cells. The substrate bias is maintained grounded, $V_{BG} = 0\,V$.

To perform a *read* operation, only the drain side needs to be pulsed. This allows lower complexity while performing the reading and, at the same time, the front-gate voltage remains the same as for hold operation. In contrast, for the *hold* operation, the drain terminal is grounded meaning low power consumption because no current flows. The purpose of the *write* '1' operation is to strongly bend the energy bands in the drain so that BtBT can take place to inject holes. To obtain this large electric field required, high drain biases and very negative front-gate voltages are applied. This operation is probably the most critical in terms of power consumption of the memory cell. The high drain bias may lead to large drain currents and power dissipated. Finally, the *write* '0' operation, is achieved by positively pulsing the front-gate to evacuate holes by forward biasing the lateral PN junctions with the source and drain, both grounded. The bias pattern applied is represented in Figure 6.14.

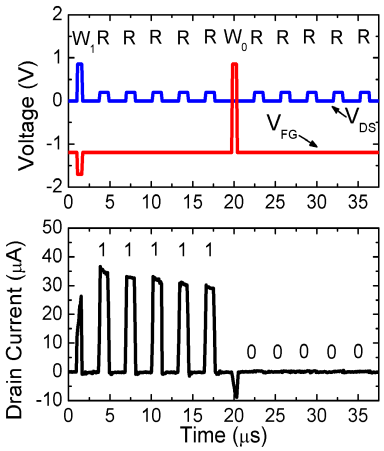


FIGURE 6.14: Top: Final bias pattern obtained after optimization for $L = 80$ nm and $W = 10$ μm. $V_S = V_{BG} = 0$ V. Bottom: drain current readout demonstrating large high current for the '1' state and negligible current for '0' state.

As expected, the **drain current obtained after writing '1' is much**

larger than after writing '0', which can be considered negligible. This result demonstrates the feasibility of scaled A2RAM cells on SOI. Although it can be used to further improve the drain current margin, no back-gate bias has been applied during the previous bias pattern.

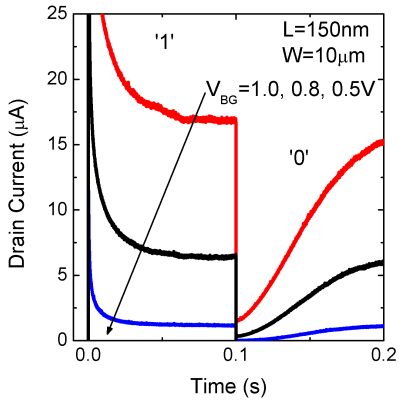


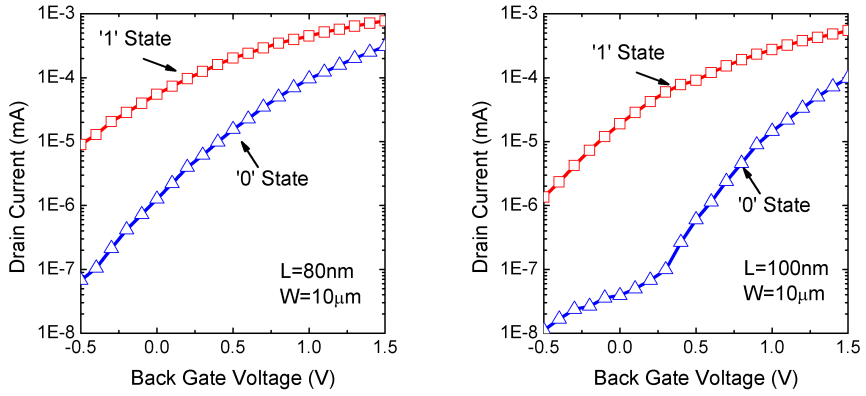
FIGURE 6.15: Drain current levels evolution with time for several back-gate biases applied. $L = 150$ nm and $W = 10$ μm.

An example of positive back-biasing boost is illustrated in Figure 6.15 for a device of $L = 150\,nm$. The applied positive back-gate bias enhances the electron accumulation at the bottom of the silicon film. This makes more difficult for the front-gate to fully deplete the N-Bridge increasing the driven current when reading. The overshoot in the high current level is due to an overpopulation of holes. The excess of holes recombine gradually with time aiming to the stationary current level of the memory cell. The 'lost' of the unstable low current level is mainly due to parasitic injection of holes by GIDL into the body of the cell and thermal generation. These holes start to screen the front-gate influence over the bottom of the silicon film preventing the depletion of the N-Bridge so that the current starts to increase as time passes.

In the next sections, the extraction of the drain current margin level and retention time will be carried out.

6.2.3. Current Level Margin

The current sense margin is strongly related to the back-gate bias and also to the size of the device. Therefore, the drain current has been extracted 10^{-4} s after the last programming event against the back-gate bias for **(a)** $L = 80$ nm and **(b)** $L = 100$ nm, Figure 6.16.



(a) $L = 80nm$ (b) $L = 100nm$

FIGURE 6.16: Drain current for different memory states extracted 10^{-4} s after last memory operation against back-gate bias for **(a)** $L = 80$ nm and **(b)** $L = 100$ nm. $W = 10$ μm.

The drain current ratio can be extracted using Equation 6.3. Figure 6.17 **(a)** shows the current ratio obtained for several devices featuring different channel lengths. The maximum values, for each gate length, are represented in Figure 6.17 **(b)** together with the back-gate bias used in each case. The highest current ratio case is found for $L = 150$ nm with a **maximum current**

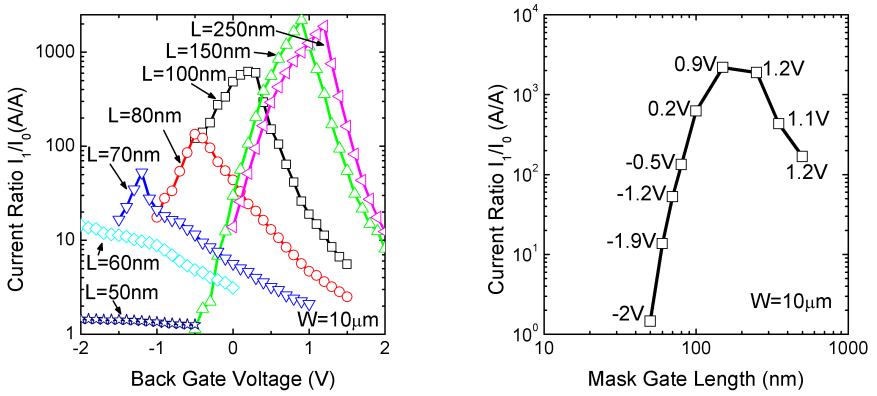
ratio of around 2.200. It decays rapidly for shorter or larger gate lengths; however it remains large enough for level discrimination. Being more specific, a ratio of over one hundred is achieved for devices with length in the range of 80 nm $< L <$ 500 nm.

There exists a remarkable dependence of the current ratio with the back-gate bias and length considered. This dependence reflects the strong impact that SCE play in this cell due to the implicit connection between source and drain. The enhancement in current margin by opposite-gate biasing moves from positive to negative voltages, depending on the channel length. For long channel MOSFETs ($L >$ 100 nm), a V_{BG} around 1.2 V is required to enhance the electron population at the N-Bridge. However, in more scaled A2RAM cells ($L <$ 100 nm), a negative back-gate bias is required to compensate the implicit enhancement in the N-Bridge electron concentration due to SCE. The negative back voltage compensates the increasing potential due to the source and drain-body depletion region influence and fringing field effect. For $V_{BG} = 0$ V, the best current ratio is found for $L = 100$ nm which precisely was the channel length for which the fabrication process was optimized.

$$I_{1/0}(10^{-4}s) = \frac{I_1(10^{-4}s)}{I_0(10^{-4}s)}\,[A/A] \tag{6.3}$$

Finally, a cumulative statistical study is performed for the drain current margin for over 300 transistors fabricated on the same wafer. For each transistor the same pattern was applied. It consists in a simple sequence: $W_1\,|\,R\,|\,W_0\,|\,R$ (not shown). The drain current margin was sensed again 10^{-4} s after each programming operation.

Results are illustrated in Figure 6.18, with **(a)** being the high and low drain current levels, and **(b)** the calculated current ratio. In this plot each point represents the percentage of cells, y-axis, that have a drain current level

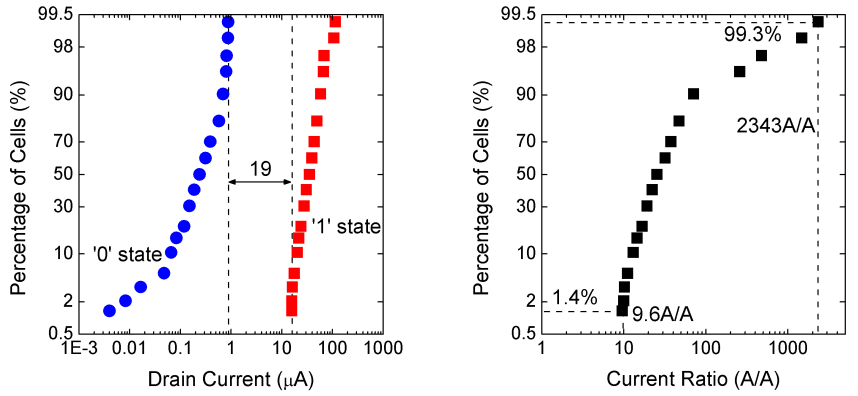


(a) Several Gate lengths (b) Current ratio peak

FIGURE 6.17: **(a)** Drain current ratio between memory states for several gate lengths and **(b)** drain current ratio peak against the device mask gate length with the back-voltage used. The ratios are measured 10^{-4} s after the writing. $W = 10$ μm.

or ratio (attending to **(a)** or **(b)**) equal or lower than their x-axis value. For example, the lowest point in the drain current ratio cumulative representation has a pair values of $x = 9.6$ A/A and $y = 1.4$ % of cells, this means that only 1.4 % of total cells measured have a maximum drain current ratio of 9.6 A/A, or equivalently, the others 98.6 % of cells have more than 9.6 A/A. The maximum at the right side has, on the other hand, a current ratio of $x = 2343.1$ A/A at a percentage of $y = 99.31$ % meaning that 99.3 % of the cells have less than a current ratio of 2343 or the rest of cells, 0.7 %, have more than a ratio of 2343 A/A between states.

The variability of the high current level is quite small, the points are almost aligned in a vertical line meaning an almost constant drain current. It does not happen the same for the low current level (and consequently for the current ratio). In the case of the low current state, there are some cells that



(a) Cumulative drain current levels (b) Cumulative drain current ratio

FIGURE 6.18: Cumulative statistical study for over 300 devices for **(a)** drain current levels and **(b)** drain current ratio. $L = 80$ nm, $W = 10$ μm, $V_{BG} = 0$ V and $T = 25\,^{\circ}$C.

presents much lower current than others. This is not bad as long as the worst current level during the '0' state is low enough. Lastly, **no crossing between the '0' and the '1' states distributions** is found. This implies that the **state discrimination can be carried out with no major problems**.

6.2.4. Retention Time

For the following calculations and parameter extraction, the back-gate voltage will be tied to ground. The reason behind not applying any substrate bias is because, in contrast to many of the floating-body DRAM cells that has been already proposed, the A2RAM can operate properly without it, exhibiting good performance and lower biasing scheme complexity.

The different definitions of retention time were already discussed in Chapter 5. In this case, it is defined as the minimum time taken by the

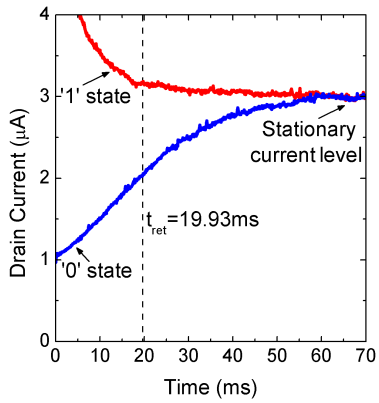


FIGURE 6.19: Example of calculated retention time for an A2RAM memory cell. The retention time is defined as the time it takes the state zero to achieve a 50 % of the current in stationary state. $L = 80$ nm, $W = 10$ μm and $V_{BG} = 0$ V.

unstable '0' state to achieve half of the stationary drain current value ($a = 0.5$ in Equation 5.6). An experimental example is represented in Figure 6.19. The '1' state current level presents a large current overshoot due to the initial overpopulation of holes inside the body. However, this fact does not affect the definition of the retention time since it is referred to the stationary cell current ($I_1(t \to \infty) = I_0(t \to \infty)$). A value close to $t_{ret} = 20$ ms is extracted for $L = 80\,nm$. This value is in the same order of magnitude as the simulations carried out for the CEA-LETI A2RAM cells in Chapter 4.

The retention time depends on how efficient is the A2RAM cell on storing holes under the front oxide, avoiding their regeneration and depleting the N-Bridge. The control of these operations is driven by the front-gate bias during the *hold* operation. The retention time is represented as a function of the *hold* front-gate voltage in Figure 6.20. A strong relationship between the cell retention time and the applied *hold* bias is manifested.

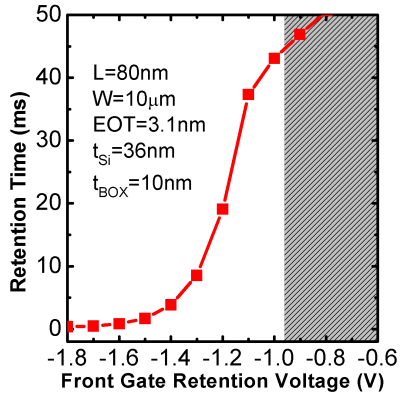


FIGURE 6.20: Retention time obtained as a function of the front-gate voltage applied to retain holes. In shaded area the front-gate bias considered is not enough to fully deplete the N-Bridge so the current for '0' state increases leading to a poor drain current ratio. $L = 80$ nm, $W = 10$ μm and $V_{BG} = 0$ V.

On one hand, if the *hold* V_{FG} is too negative, the retention time is almost zero. This is motivated by a parasitic charge injection of holes inside the body. Although, a high hole injection rate is indeed beneficial in case of the '1' state, it will also make the body to recover rapidly the stationary hole population during the '0' state. Therefore, it reduces the time it takes for the low level to achieve the 50 % of the stationary current. On the other hand, if the front-gate is not enough negatively biased, the current sense margin between high and low memory levels will decrease since the N-Bridge will be no longer fully depleted after *write* '0'. This will make the low current level to be non-negligible (shadowed region), thus increasing dramatically the power consumption of the cell. **A tradeoff results between power consumption and A2RAM retention time**.

A cumulative statistical study is carried out in Figure 6.21. Over 300

transistors ($L = 80$ nm and $W = 10$ μm) were measured and processed to extract their retention time. Retention time results are compared with other proposed floating-body DRAM candidates.

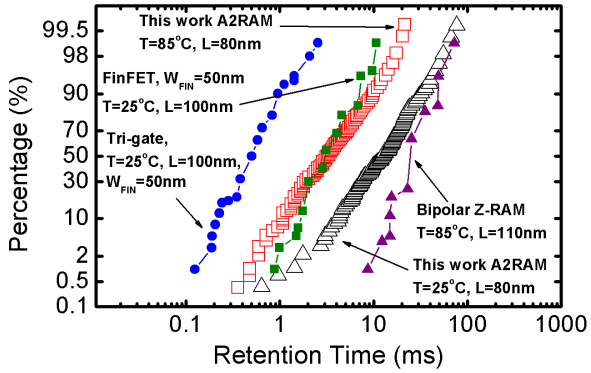


FIGURE 6.21: Cumulative retention time for A2RAM at different temperatures compared with other FB-DRAM candidates. $L = 80$ nm, $W = 10$ μm and $V_{BG} = 0$ V.

The variability of the retention time is monitored through the cumulative A2RAM retention time plot for two different temperatures: at room temperature, $T_R = 25$ °C (open triangles), and at high temperature, $T = 85$ °C (open squares) [BFX+05]. Several retention time results from other FB-DRAM alternatives has been also represented to compare. A memory cell based on Tri-gate structures at room temperature (plain circles) [BFX+05], another memory based on Fin-FETs also at room temperature (plain squares) and finally, the bipolar Z-RAM candidate at high temperature, $T = 85$ °C (plain triangles) [ONC+07].

The variability presented by the A2RAM cells does not change significantly when varying the temperature. They have almost the same slope with a slightly higher deviation that other single transistor schemes. It should

be noted that no special junction engineering process was followed during the fabrication of these A2RAM cells to enhance their properties as memory. However, the retention times measured for high temperature are better in this planar structure than other more complex 3D architectures designs such as Fin-FETs or Tri-gate at lower temperature. The improvement provided by the bipolar operated Z-RAM at high temperature is around one order of magnitude higher but, in contrast, the Z-RAM uses larger devices with thicker films and also larger biases [ONC+07]. This means larger power consumption and also reliability and disturbance concerns.

So far, it is worth noting that **the measured A2RAM cells have not been specifically optimized for memory applications**. Their design has followed typical FD-SOI transistor design flow. No special junction engineering nor any device optimization mentioned in Chapter 2 has been considered to enhance the memory performance. Even with that, **the studied A2RAM cells present almost the best results in the comparison** made (Figure 6.21). Moreover they are the **shortest cells in the previous comparison and can be further scaled** by N-Bridge doping and body thinning optimization together with bias adjustments.

6.2.5. Disturbance Test

One of the last studies that is examined in this work is the **immunity to disturbances in the connection lines**. Until now, all the test performed have considered the A2RAM cell as an independent and isolated device but, in practice, this is not true. Memories are made with millions of interconnected cells to form a 2D matrix. This way, accessing a given cell is much more efficient since there is a dramatic reduction of connection lines but, in this scenario, the operation of one memory cell may affect an adjacent cell. The most critical

situation is the disturbance to one cell that is storing a '0' (unstable current level

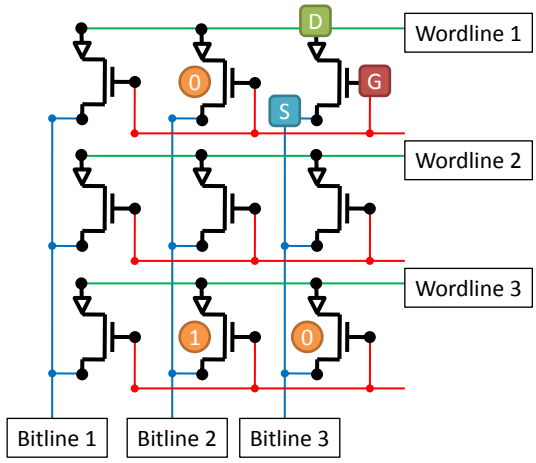


FIGURE 6.22: Simplistic A2RAM memory cell array scheme with only 3 words (rows) with 3 bits each (columns) to study the disturbance phenomenon. During *read* operation the drain is considered to be at the selector (triangle) side.

A generic and simplistic array composed of A2RAM cells is shown in Figure 6.22. This memory matrix is formed by only 3 words (rows) of 3 bits each (columns). The information (stored memory level) of three different cells is also depicted. For each scenario, the disturbed cell will be represented with a lightning symbol while the cell being addressed will appear with the background highlighted. Each A2RAM cell has been represented with an additional element at the drain side (the small triangle). This device, called **selector**, **avoids undesired current path between cells** that could lead to a malfunction of the memory array. An example of an undesired current path is represented in Figure 6.23 where the drive current is drawn (dashed line and arrows) for both a case with and without selectors. In the first case (at the left), using the selectors allow the first word ('1' and '0') to be successfully read. On the other hand, when the selector is not present in the memory matrix (at the right), the

driven current cannot be rightly controlled leading to an undesired contribution from one column cell on another cell. This yields to a wrong current readout

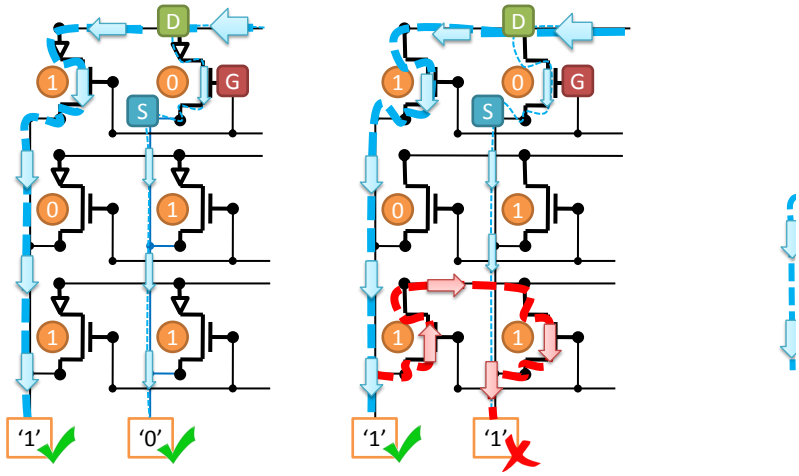


FIGURE 6.23: Schematic view of the need of selectors to avoid undesired current paths between A2RAM cells. On the left, the cell array with selectors that prevent the current flow in the wrong sense and, on the right, the cell array without selectors showing a forbidden current path for proper operation.

It is important to mention that thanks to the **symmetric structure** of the A2RAM cell, **the role played by the drain and source sides can be interchanged**. This way, the read operation (as appeared in Figure 6.23) considers the drain to be in the same terminal as the selector to allow the state discrimination based on current flow. On the other hand, for writing operation, the drain is considered to be at the opposite terminal (see Figure 6.24). This interchanged role permits the proper work of the cell and further improves the performance. **The power consumption during the *write* '1' would be lowered thanks to the use of the selector**. Since during writing, the drain terminal is not the same as the terminal where the selector is connected, the

selector will not allow any drain to source current flow. So, the worst operation, in terms of power consumption (W_1), would turn to be negligible. Nevertheless, it should be noted that adding the selector component may require the tuning of the bias levels for the different events and may also affect the fabrication process.

Dra

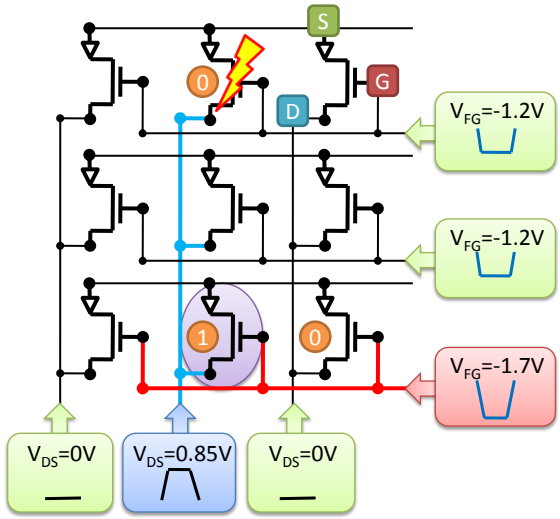


FIGURE 6.24: Drain disturbance to a cell storing '0' (lightning symbol) when writing '1' to another cell in the same bit line (highlighted cell in the same column). During *write* '1' or '0' operations the drain is considered to be at the opposite side of the selector.

It will be checked whether the state stored in the disturbed cell (lightning symbol) is modified when changing the drain bias to *write* a '1' state in a different cell that shares the same bit line (column). To do so, all four bias operations will be verified (same biases as Table 6.3 are considered). Since the first assumption is that there is a '0' stored, it is straightforward that in this case only the *write* '1' event or *read* operation may affect this cell. All others

operation have $V_{DS} = 0$ V. The *read* operation with $V_{DS} = 0.2$ V does not affect since it is addressed at the selector terminal of the chosen word (it does not affect other A2RAM cells in the same bit line then) but the *write* '1' is carried out at the opposite terminal so that it could disturb the cell as shown in Figure 6.24.

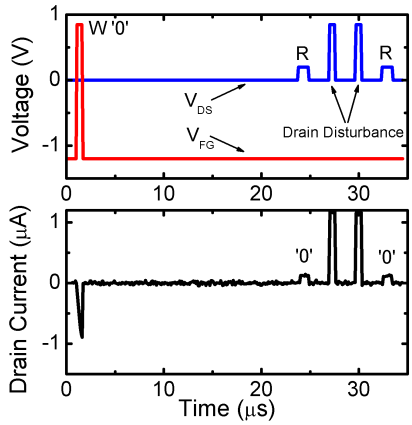


FIGURE 6.25: Disturbance test at the drain side. At the top, bias pattern applied to the drain and gate terminals. At the bottom, the drain current readout as a result of the pattern applied. It can be noticed how the reads before and after the disturbances are the same demonstrating the immunity to drain disturbances. The two consecutive peaks of drain current due to the drain disturbance would not appear if the selector is used.

To verify if the '0' state stored in the lightning cell is degraded, a specific pattern is generated and applied. Both the pattern and drain current response of the disturbed cell are shown in Figure 6.25. Two consecutive drain pulses of the same amplitude are applied to emulate the *write* '1' operation to another cell in the same bit line, $V_{DS} = 0.85$ V (Figure 6.25). This means that only the drain of the disturbed cell is affected, not the gate. A pre-*read* and post-*read* operations are performed to check if there is any significant drain current change in the disturbed cell state.

The readout current, Figure 6.25, shows two peaks due to the drain disturbance but the effect on the stored level is negligible since the current for the pre and post-*read* present the same level. Furthermore, the use of the selector avoids these two peaks to appear (as explained before). This demonstrates the **A2RAM cell immunity to drain disturbances** if using this matrix structure.

Gat

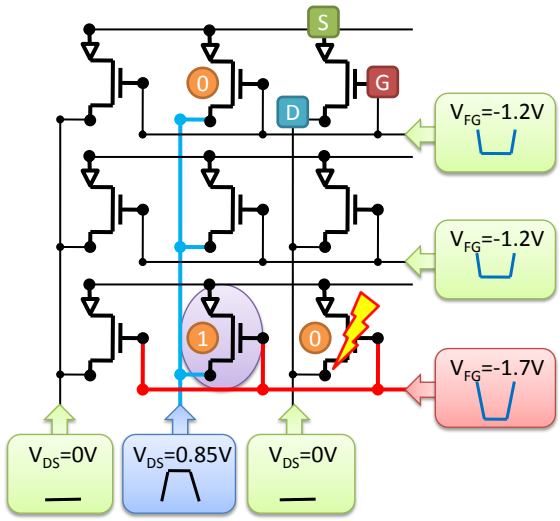


FIGURE 6.26: Gate disturbance to a cell storing '0' (lightning symbol) when writing '1' to another cell in the same word (row). During *write* '1' or '0' operations the drain is considered to be at the opposite side of the selector.

Now the gate line disturbance is studied, it is again considered that the line disturbance affects a cell storing a '0' state. The *read* and *hold* states do not imply a disturbance risk since the gate bias does not change. The *write* '0' operation will be beneficial since it will refresh the '0' state. Thus, the only

operation that could disturb the cell is the *write* '1' process. The disturbance scheme in the considered array looks like Figure 6.26.

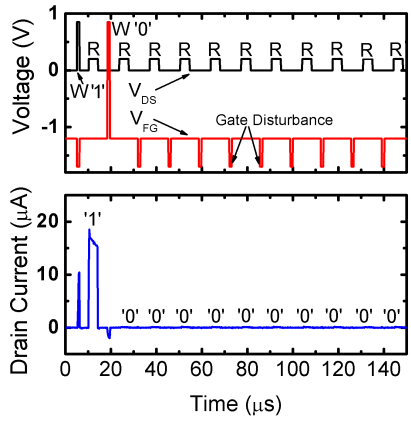


FIGURE 6.27: Disturbance test at the gate side. At the top, bias pattern applied to the drain and gate terminals. At the bottom, the drain current obtained as a result of the pattern applied. It can be noticed how the reads before and after the disturbances are the same demonstrating the immunity to gate disturbances.

As done before, another specific pattern is applied to test the reference cell as it would be in an actual memory matrix. Both the pattern and the drain current readout are illustrated in Figure 6.27. In this case, the disturbance appears at the gate side with nine consecutive peaks at $V_{FG} = -1.7$ V. A pre and post-*read* are performed after every disturbance to check variations in the current levels.

In this case, the drain current does not show the disturbance peaks since the drain terminal remains grounded. In contrast, during each *read* operation, the drain current is constants meaning that the **gate disturbance is not affecting the A2RAM** in the actual configuration. It has been tested that

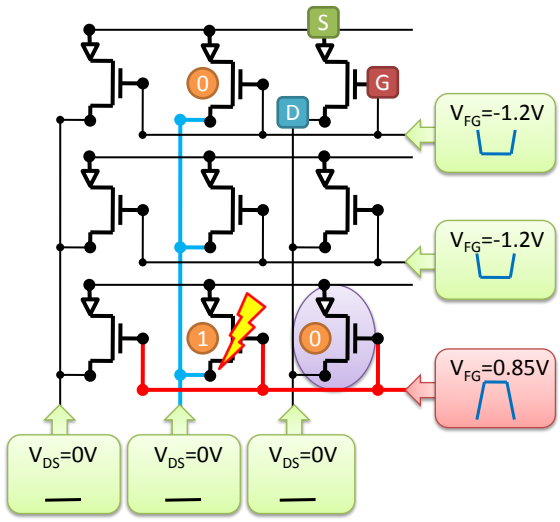


FIGURE 6.28: Gate disturbance to a cell storing '1' (lightning symbol) when writing '0' to another cell in the same word (row).

when using this matrix the '0' state in A2RAM cells is immune to drain or gate disturbances from operations in other memory cells.

In the case of a cell storing the '1' state, there is only one operation that could affect the cell in the proposed matrix, the *write* '0' at the gate terminal, Figure 6.28. But, since to perform the *write* '0' in a cell, the whole word is erased and after that, the cells containing '1's are *overwritten*, there is no possible disturbance for the stored '1'.

It can be concluded that the A2RAM cell is immune to drain or gate disturbances either the cell is storing a '1' or '0' if using the memory matrix proposed.

6.2.6. Power Issues

This section will be focused on analyzing the power consumption of the A2RAM cell. Performing a detailed analysis and comparison with commercial synchronous DRAM cells is extremely difficult due to the complexity of the signals involved and amount of different modules, see Figure 6.29. A detailed analysis will be therefore out of scope (there are some rigorous approaches though, [Mic07, Vog10]). Nevertheless, it is possible to **study the A2RAM power consumption as an isolated cell** and mention its advantages over traditional 1T+1C DRAM memories or other FB-DRAM cells.

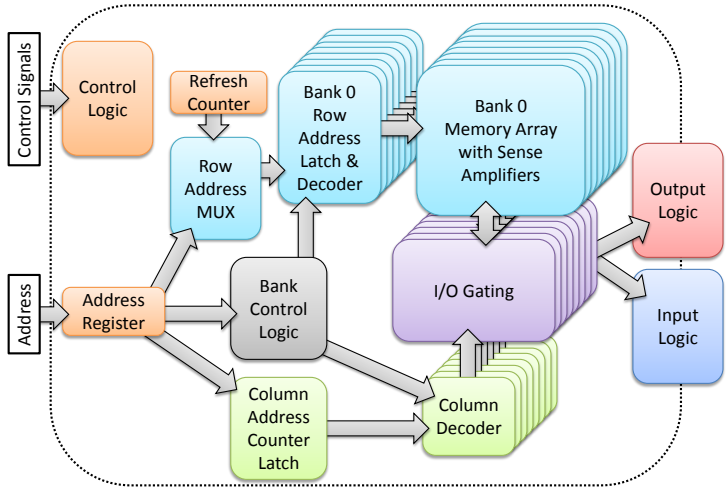


FIGURE 6.29: DDR SDRAM basic structure. Notice the complexity regarding the number of modules involved.

Attending to power saving operation differences, the most significant are that A2RAM, as almost any other floating-body DRAM cell, has not the need of being refreshed after a read operation. It also requires lower drain operating voltage which is the one main bias for power consumption ($V_{DS-max} = 0.85\,V$ instead the minimum used by DDR4 around $V_{DS-max} = 1.2\,V$). On the other

hand, it will probably require to be refreshed more often due to its lower retention characteristics and it also involve the use of larger gate voltages.

An approximation of the power consumption for each memory operation can be obtained averaging from the previous results (Figure 6.14). Table 6.4 summarizes the power consumption for all the operations.

CEA-LETI A2RAM			
Parameter	I_{DS} ($\mu A/\mu m$)	V_{DS} (V)	Power ($\mu W/\mu m$)
Writing 1	1.743	0.85	1.482
Reading 1	3.103	0.2	0.621
Writing 0	0.604	0	0
Reading 0	0.136	0.2	0.027
Holding	0.024	0	0

TABLE 6.4: CEA-LETI A2RAM averaged power consumption per micrometer width. $L = 80$ nm and $W = 10$ μm.

Of course, all these values are related to an array of only one cell without considering gate leakage or other memory cells leakage. With this assumption in mind, it can be seen that the power consumption is almost entirely related to two operations, *write* '1' and *read* '1'. In the first case, the energy is used in generating the intense vertical electric field that bends the energy bands while tunneling takes place. The second operation, *read* '1', uses the power to drive the high current level through the N-Bridge. All other operations are typically low power processes since whether the drain bias used is grounded or the driven current is very small.

Regarding the use of this cell in an actual memory matrix, as the selector element is required for proper memory operation, the power consumption will be reduced during the *write* '1' operation (the current across the device would be negligible since the selector will be biased in reverse mode).

We can compare the A2RAM power results with another astonishing advanced novel memory, the Z2FET DRAM (see Chapter 2) in Table 6.5. All values have been scaled to a constant gate width of 1 μm.

	Z2FET DRAM		
Parameter	I_{DS} ($\mu A/\mu m$)	V_{DS} (V)	Power ($\mu W/\mu m$)
Writing 1	260	-1.25	325
Reading 1	260	-1.25	325
Writing 0	5	0	0
Reading 0	5	-1.25	6.25
Holding	5	0	0

TABLE 6.5: Averaged experimental power consumption for the Z2FET DRAM [Wan12]. The Z2FET cell features $t_{ox} = 6\,nm$, $t_{Si} = 20\,nm$, $t_{BOX} = 145\,nm$ and $L_{Total} = 600\,nm$.

The power consumed by the Z2FET is distributed in the same way as for the A2RAM. There are two high-power operations, the *write* and *read* '1' events. However, results in Table 6.5 show a dramatic difference. The Z2FET [Wan12] presents a remarkable increment in the power dissipated compared with the A2RAM. Nevertheless, the driven current by the Z2FET is also larger. If the selector is present in the cell, it is expected to reduce, even more, the power consumption of the A2RAM cell. Attending only to the power waste, the A2RAM cell should be considered at first, but always, as long as the output sense amplifiers of the matrix are able to discern their lower current levels (the A2RAM current can also be augmented by increasing the drain bias while reading).

6.3. Conclusions

This chapter has presented the static and dynamic behavior of scaled arsenic implanted transistor emulating the A2RAM cells in SOI. A poor operation as a switching device has been found due to the arsenic implantation that connects the drain and source regions. This implantation on the other hand, allows A2RAM cells to present a hysteresis cycle based on the floating-body effect. Further studies, regarding its properties as a memory, postulate A2RAM as a promising FB-DRAM alternative for the future.

In the next final Chapter 7 the **final conclusions** of this report are presented.

Chapter 7

Conclusions and Future Steps

This final chapter stands for giving the main ideas extracted from this work, from the theoretical to the experimental achievements. As a result, the strengths of the A2RAM are highlighted showing the promising capabilities introduced by these novel memory cells.

7.1. Theoretical Framework

The study was set out to **explore the concept of the advanced 2 RAM cells** enclosed into the potential alternative that FB-DRAM are shown to be versus the 1T+1C DRAM. A theoretical framework has been given around the semiconductor memory history and the revolutionary technology that may lead to a steep change in the dynamic RAM cells, Silicon on Insulator. This technology plays a key role in the floating-body concept since it is the essential

pillar on which almost any single transistor memory cell lies. The advantages provided by SOI (discussed in Chapter 2) are achieved by using a buried oxide layer. This buried insulator prevents the evacuation of the charge through the substrate, thus allowing the floating-body effect to appear.

The most representatives floating-body memory candidates have been shown together with their operation, benefits, drawbacks... until reaching the Advanced RAM and its boosted sister, the advanced 2 RAM. In contrast to many designs, these two memories benefit from the multi-body cell concept. Multi-body architecture makes the Advanced and Advanced 2 RAM not to work as a traditional floating-body memory. Their operation resides on capacitive coupling to modulate the creation or depletion of a minority (A-RAM) or majority carrier (A2RAM) region between source and drain terminals, thus changing the current sensed when reading. While it is true that they also need to allow the coexistence of both kind of carriers inside the cell body, for the A-RAM, this is achieved by using an extra buried oxide layer called middle oxide, MOX, and in case of the A2RAM, a vertical PN junction inside the body is used. The specific fabrication process for the A2RAM has shown to be almost identical to a typical CMOS process with an additional implantation step together with a selective epitaxial growth in ultrathin SOI.

The established objectives sought to answer these questions:

1. Can the Advanced 2 RAM memory cell theoretical concept be fabricated?
2. Does its performance allow this type of cell to be competitive?
3. Does this novel floating-body DRAM have any real contribution or innovation to the technological framework regarding dynamic memories today?

7.2. Empirical Findings

The main empirical findings are chapter specific and were summarized within the respective empirical sections:

- Chapter 4, A2RAM cell Simulation of manufacturing and operation using Silvaco Athena® and Atlas® respectively.
- Chapter 5, A2RAM memory demonstration on SOI and bulk substrates using 2.5 μm technology.
- Chapter 6, A2RAM samples on 22 nm node technology fabricated at CEA-Leti.

This section will summarize the empirical findings along this report to answer the previous questions.

1. Can the Advanced 2 RAM memory cell theoretical concept be fabricated?

   a) In Chapters 3 and 4 all the processing steps required to achieve the N-Bridge inside a bulk or SOI transistor are detailed. In Chapter 5 the viability of fabricating A2RAM samples is demonstrated on either bulk or SOI substrates. In case of bulk, a 2.5 μm CMOS process is used at Centro Nacional de Microelectrónica in Barcelona. By performing an hysteresis study on the cells, their behavior as a memory was verified. Further research is carried out to benchmark these samples.

   b) On the other hand, in Chapter 6 the feasibility of Advanced 2 RAM cells on sub 100 nm is evidenced thanks to CEA-LETI Grenoble. A deep study not only as a memory cell, but also as a transistor, is carried out to check their strengths and weaknesses compared to

ET-SOI transistors studied in Appendix B. It is shown how they behaves closer to PD-SOI MOSFETs rather than ET-SOI due to their explicit connection between source and drain, but also, how they present remarkable properties as innovative single transistor dynamic memory.

It is therefore demonstrated that A2RAM manufacturing and memory behavior is a fact that has become true surpassing the concept scope. The *best* and the *averaged* results achieved are summarized in Table 7.1 and 7.2 respectively.

A2RAM [L/W]	Current Ratio 25 °C	Retention Time 25 °C	Retention Time 80 °C
Bulk (CNM) [$4\mu m/30\mu m$]	2.1	30 ms	300 μs
SOI (CNM) [$4\mu m/30\mu m$]	2300	25 s	1 s
SOI (CEA-LETI) [$80nm/10\mu m$]	2200	80 ms	20 ms

TABLE 7.1: A2RAM cell best results achieved for different technologies and substrates studied in this work.

A2RAM [L/W]	Current Ratio 25 °C	Retention Time 25 °C	Retention Time 80 °C
Bulk (CNM) [$4\mu m/30\mu m$]	1.6	1 ms	200 μs
SOI (CNM) [$4\mu m/30\mu m$]	1500	20 s	500 ms
SOI (CEA-LETI) [$80nm/10\mu m$]	30	15 ms	4 ms

TABLE 7.2: A2RAM cell averaged results achieved for different technologies and substrates studied in this work.

2. Does its performance allow this type of cell to be competitive?

   a) When comparing the bulk A2RAM, the performance is poorer than the presented by other FB-DRAM alternatives. Despite this degraded behavior, they still exhibit memory effect.

b) The SOI samples provided by CNM demonstrate the feasibility of defining the N-Bridge by using only an arsenic implantation. They exhibit impressive properties as memory but their size makes them to be considered just as a proof of concept, rather than being really functional for a real application.

c) CEA-LETI memory cells are the most promising samples tested since they join very promising memory properties together with good scalability. The experimental results obtained give these single transistor memories current margins ratios over 2200 and retention times around 80 ms on their best and 15 ms averaging at room temperature, 300 k.

It is shown how the A2RAM follows the theoretical behavior anticipated by the good results extracted from simulations. It is important to notice that further improvements could be achieved by optimizing the hole retention and the injection by *junction engineering*.

3. Does this novel FB-DRAM have any real contribution or innovation to the technological framework regarding dynamic memories today?

   a) There are very few reports about 1T-DRAM memories on bulk [RVM+04]. This gives an idea of one of the advantages the A2RAM cell provides. A2RAM cells are not restricted to SOI substrates, although they benefits from the strengths of this technology.

   b) Scaling on SOI technology is thickness related: to decrease the gate length it is necessary to use thinner silicon and buried oxide films. Due to supercoupling effect [ECC+07], the minimum silicon film thickness that can be used is limited to allow the required coexistence of electrons and holes in the body of the cell at the same time. The use of the vertical PN junction in A2RAM allows to obtain a very steep vertical change in the body potential. The

potential drop is achieved by junction itself rather than by biasing. This relaxes the drawback and allows farther t_{Si} scaling.

It has been argued why the A2RAM cell presents some clear advantages over most of other FB-DRAM candidates. These crucial points make the Advanced 2 RAM memory to be considered as one of the most promising choices to continue the research on.

7.3. Beyond A2RAM

Although this work presents a detailed scope of floating-body DRAM cells, especially focused on A2RAM, it is important to remark that there are some points that have not been covered and could lead to some extended studies. Some of the uncovered aspects are:

- Further A2RAM structure optimization and reliability test.
- Memory cell array design and simulation.
- Cell array manufacture and benchmark.
- A2RAM concept on 3D structures (FinFETs, tri-gate...).

The structure optimization aims to enhance the performance of the cell basically by *junction engineering*. Although some characteristics have been already investigated, as the effect of overlapping of drain and source regions by the gate [RCG11c], this point also involves changing the doping level concentration and/or doping profiles, employing new features as SiGe wells to help accumulating the positive charge, use strain, modifying the N-bridge thickness... with each of these improvements related to the gate length considered ([SJL+08, ECKS08, TLE+08, CLE+10, LC11, MCJ+05,

ES10, HFH$^+$10]). Looking forward commercial implementations, a reliability study would be required.

The second uncovered aspect is the complete circuit design and following simulation of a full memory cell array composed by A2RAM cells, including the selectors, output amplifiers to sense the cell state, all signaling modules to drive for example the row (RAS) and column strobes (CAS) and any other basic module. This step does not aim to design a large cell array but instead a fully operational memory to prove by simulations its feasibility. Once the complete array has been simulated and its basic operation verified, it should be sent to be manufactured and then experimentally characterized its performance.

Finally, the A2RAM concept is easily applicable to other more complex structures such as: FinFETs, tri-gate [GRC12]... This technological change should improve the characteristics that planar A2RAM cells present thanks to the better electrostatic control that the multi-gate structures provide.

7.4. Final Conclusions

Along this report it has been presented an introduction around the semiconductor memory paradigm today, focusing on a real and potential alternative to continue with the incessant scaling around dynamic memories. This candidate, the A2RAM, solves some of the problems than other FB single transistor alternatives do not, like far silicon film thickness scaling or substrate independency, while keeping, at the same time, very good performance attending to drain current margin and retention time. The Advanced 2 RAM memory cell should be therefore taken into account as a real option to replace 1T+1C dynamic memories in a non very long term, especially for embedded applications.

Part III

Appendices

Appendix A

Electrical Characterization of FD-SOI Transistors

A.1. General Characterization Techniques

In this Appendix some techniques and methods to experimentally evaluate some parameters such as the threshold voltage, carrier mobility and equivalent oxide thickness are presented [Rod08].

A.1.1. Threshold Voltage

The **threshold voltage** is probably the most significant parameter regarding the technology used. Over time this parameter has been decreasing gradually reaching values around 0.4 V in state-of-the-art N-MOSFETs [RAN+11]. For bulk and PD-SOI transistors, the threshold voltage is essentially fixed for a given temperature, substrate bias, drain bias and gate

length (DIBL). On the contrary, **for FD-SOI transistors the threshold voltage of one gate is strongly related to the opposite gate bias applied due to inter-gate coupling** and it should be therefore extracted as a function of it, $V_{Th-FG}(V_{BG})$ and $V_{Th-BG}(V_{FG})$ for the front and back-gates respectively [LF83].

The threshold voltage is usually **defined as the gate voltage for which the surface potential at mid-channel equals** $\Phi_S = 2 \cdot \Phi_F$, or equivalently the gate voltage for which the minority carriers reach at the silicon-insulator interface, the same concentration as majority carriers (some modifications have been proposed on this definition for short-channel devices, where an empirical term is added to the conventional expression [TM11, OCRSL98]). The most widely used methods to extract the threshold voltage, but not the only ones, are described in the following subsections [OCSL$^+$02].

Drain Current Extrapolation

The **drain current extrapolation** defines the threshold voltage as the x-axis point, gate voltage, crossed by the tangent line of the drain current at its inflection point [CL95]. The drain current inflection point occurs by definition at the same gate voltage as the maximum of the transconductance, hence once the inflection point is known, only remains to calculate the tangent of the drain current at that point. A schematic representation of this process is sketched in Figure A.1.

The accuracy of the method may be increased if evaluated several times for different drain to source biases in the linear region, V_{DS} in the range of 10 mV and 50 mV.

Although this method was widely used in bulk devices, as device size has shrunk, **the *series resistance* and *mobility degradation* have become**

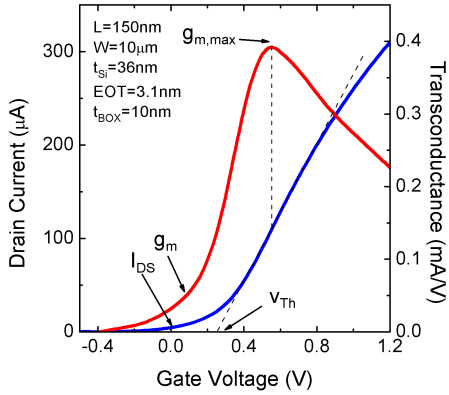


FIGURE A.1: Threshold voltage extracted using the drain current extrapolation technique. Intersection of the drain current tangent line evaluated at its inflection point with the x-axis.

major issues reducing the accuracy of the technique; these two effects bend the drain current curve for high gate voltages so that it does not present anymore a linear behavior, reducing the effectiveness of the linear extrapolation.

This extraction technique presents another important drawback: it **fails in devices with more than one channel inverted at the same time**. In these cases, the threshold voltage for a given channel, for example front-channel, V_{Th-FG}, is not well defined because there may be current flow driven by the back-channel, even when the front-gate voltage is below its threshold, $V_{FG} < V_{Th-FG}$.

Constant Drain Current

The **constant drain current** extraction technique [LOF82] evaluates the threshold voltage as the gate to source voltage value, V_{GS}, corresponding to a given constant drain current, I_{DS}. A typical value for this constant drain

current is $I_{DS} = I_0 = 0.1\mu A$ for a device with 1 μm width and 1 μm long at a constant drain bias of $V_{DS} = 50\, mV$ [TST+99]. Since in most cases the size of the device under study will not fit these values, the reference current should be then scaled using Equation A.1.

$$I_{ref} = \frac{W}{L} \cdot I_0 = \frac{W}{L} \cdot 0.1\ \mu A \tag{A.1}$$

An example of this technique is shown in Figure A.2. The measured device features $W = 10\ \mu$m and $L = 0.15\ \mu$m so the resultant scaled drain current is given by Equation A.2. The threshold voltage is extracted as Equation A.3.

$$I_{ref} = \frac{W}{L} \cdot I_0 = \frac{10\ \mu m}{0.15\ \mu m} \cdot 0.1\ \mu A = 6.67\ \mu A \tag{A.2}$$

$$\boxed{V_{Th} = V_{GS}(I_{ref}) = V_{GS}(6.67\ \mu A)} \tag{A.3}$$

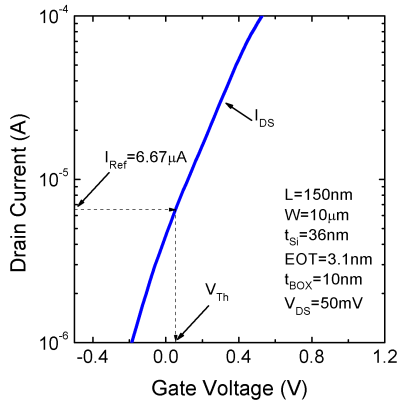


FIGURE A.2: Threshold voltage extracted using the constant drain current technique.

This method presents two important advantages: **it does not use any approximation**, which makes it very favorable to study very little fluctuations on the threshold voltage more accurately and, in addition, **the threshold voltage can be extracted very fast** since this method does not require any special processing.

In spite of its simplicity, this method has the severe disadvantage of being **totally dependent on the chosen value of the drain current level** I_0. An unappropriate choice of I_0 would result in a wrong threshold voltage determination. Furthermore, for FD-SOI transistors, it may provide **wrong results if more than one channel is inverted**; the current sensed is a contribution of the front and back-channels, so the current reference level I_0 is wrong if more than one channel drives current.

Drain Current Second Derivative

The **second derivative maximum** of the drain current or, equivalently, the inflection point of the transconductance, is achieved at a gate voltage for which the surface potential is very close to twice the fermi potential, $2 \cdot \Phi_F$ [OCRSL98, WWKB87, TFLTVDW91].

Its origin can be understood by analyzing the ideal case of a MOSFET modeled with a simple level 1 SPICE model, where $I_{DS} = 0$ for $V_{GS} < V_{Th}$ and I_{DS} is proportional to the gate voltage applied for values over the threshold voltage, $V_{GS} > V_{Th}$. Using the previous simplified assumption, $\partial I_{DS}/\partial V_{GS}$ becomes a step function, which is zero for $V_{GS} < V_{Th}$ and has a positive constant value for $V_{GS} > V_{Th}$. Therefore, the second derivative, $\partial^2 I_{DS}/\partial V_{GS}^2$, will tend to infinity at the voltage where the step takes place, $V_{GS} = V_{Th}$.

For a real device the second derivative would not become infinite, but would instead exhibit a maximum at the threshold voltage,

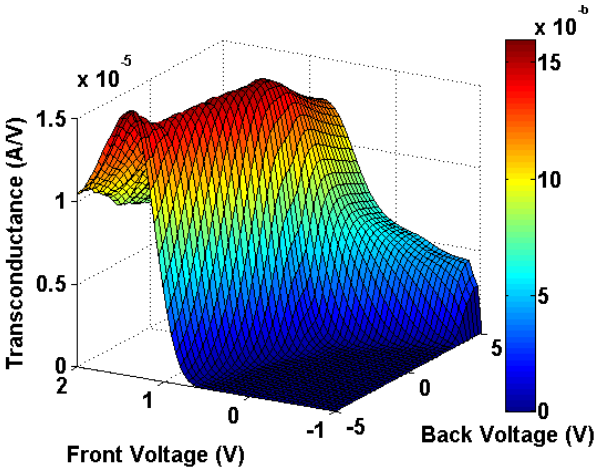


FIGURE A.3: Transconductance as a function of front and back-gate bias, $g_m(V_{FG}, V_{BG})$ [Rod08]. It can be appreciated the distorted flat regions due to back-channel inversion at high V_{BG} voltages. $V_{DS} = 50\,mV$, $L = 80$ nm, $W = 100$ nm, $t_{Si} = 26$ nm, $t_{ox} = 4$ nm, $t_{BOX} = 25$ nm and $N_A = 2 \cdot 10^{17}\ cm^{-3}$.

$max(\partial^2 I_D / \partial V_{GS}^2) \rightarrow V_{Th}$. This technique has been validated through numeric calculations of the derivative of inversion charge as a function of the surface potential for various back-gate voltages and technological options [ICR93].

In the case of bulk devices the accuracy of using this technique improves when moving to high body doping concentrations and ultra-thin front-gate oxides. On the other hand, **for FD-SOI MOSFETs it may lead to errors if the back-channel is inverted** since the transconductance would be modified by the inter-gate coupling. In Figure A.3 it is shown how transconductance presents flat regions which means not only one but two different inflection points in $\partial g_m / \partial V_{FG}$ when $V_{BG} > V_{Th-BG}$.

The extraction method is illustrated in Figure A.4. Triangles are used to represent the case when $V_{BG} = 0$ V. In that case, the back-channel is not inverted and the transconductance (plain triangles) only has one inflection

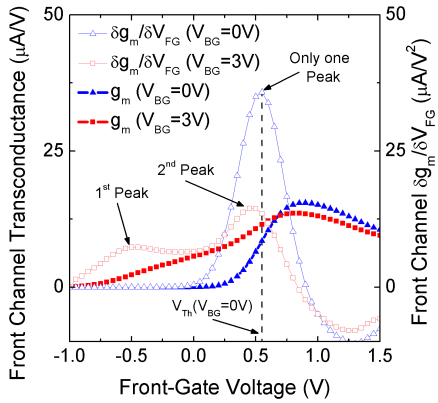


FIGURE A.4: Threshold voltage extracted using the drain current second derivative technique [Rod08]. Notice the multiple peaks problem when inverting the back-gate, $V_{BG} > V_{Th-BG}$. $V_{DS} = 50$ mV, $L = 80$ nm, $W = 100$ nm, $t_{Si} = 26$ nm, $t_{ox} = 4$ nm, $t_{BOX} = 25$ nm and $N_A = 2 \cdot 10^{17}\ cm^{-3}$.

point, thus only one peak in the second derivative is found (open triangles). However, when the back-channel contribution is no longer negligible ($V_{BG} = 3V > V_{Th-BG}$), the transconductance (plain squares) presents two inflection points leading to two different peaks in the second derivative (open squares); each one of the inflection points corresponding to a different channel activation.

This technique is one of the best option to extract the threshold voltage in devices featuring more than one active channel. Nevertheless, **the careful discrimination of the right second derivative peak is essential** to achieve an accurate value of threshold voltage.

A.1.2. Subthreshold Swing

An ideal transistor presents a zero delay switch located at the threshold voltage, from zero current, below threshold, and allowing an infinite current, over threshold. Unfortunately, real devices present a degraded switch operation (see Figure 2.13). The **subthreshold slope is the parameter that defines how fast a transistor switches from state OFF to state ON**. It is measured in the subthreshold region of the device, $V_{GS} < V_{Th}$, and it is usually employed its reciprocal value, the **subthreshold swing** expressed in mV/decade. This parameter indicates how much gate voltage shift is required to obtain a change of a decade, a factor 10, on the subthreshold current. A low subthreshold swing (high subthreshold slope) means that the device tends to a perfect sharp switch (0 mV/dec).

For FD-SOI transistors, the subthreshold swing (referred to the drain current driven by the front-gate) can be calculated using Equation A.4 [Cri05].

$$SS = ln(10) \cdot \frac{k_B \cdot T}{q} \cdot (1 + \frac{C_{it-FG}}{C_{ox}} + \alpha_{FG} \cdot \frac{C_{Si}}{C_{ox}}) \, [mV/dec] \tag{A.4}$$

where the front-interface coupling coefficient, α_{FG}, is given by Equation A.5.

$$\alpha_{FG} = \frac{C_{BOX} + C_{it-BG}}{C_{Si} + C_{BOX} + C_{it-BG}} < 1 \, [-] \tag{A.5}$$

This expression accounts for the influence of back interface traps and buried-oxide thickness on the front-channel current. The remaining capacitances are defined per unit of area as appear in Table A.1.

In ultrathin Si-film devices with good quality film-BOX interface ($D_{it-BG} < 10^{11} \, cm^{-2} \cdot eV^{-1}$), the last term in Equation A.4 can be neglected given that $t_{ox} << t_{BOX}$ and $t_{Si} << t_{BOX}$, Equation A.6. If the front-interface

Symbol	Parameter	Equation
$C_{it-FG/BG}$	Interface D_{it} capacitance	$C_{it-FG/BG} = q \cdot D_{it-FG/BG}\ [F]$
$C_{ox/BOX}$	Oxide capacitance	$C_{ox/BOX} = \epsilon_{ox/BOX}/t_{ox/BOX}\ [F]$
C_{Si}	Silicon film capacitance	$C_{Si} = \epsilon_{Si}/t_{Si}\ [F]$

TABLE A.1: Capacitances in SOI transistors.

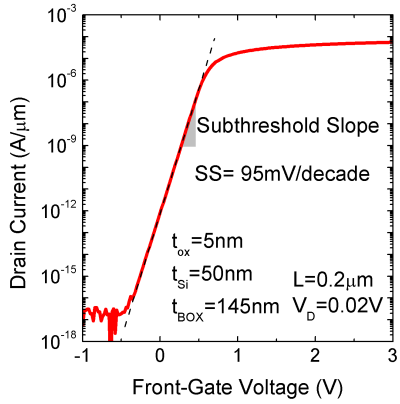


FIGURE A.5: Simulated subthreshold slope extraction by obtaining the drain current slope in the subthreshold region. The subthreshold swing is its reciprocal value.

is also high quality ($D_{it-FG} < 10^{12}\ cm^{-2} \cdot eV^{-1}$), the ratio C_{it-FG}/C_{ox} is negligible as well. In this ideal case, the subthreshold slope becomes close to the theoretical limit, Equation A.7 [CL95].

$$\alpha_{FG} \cdot \frac{C_{Si}}{C_{ox}} = \frac{C_{BOX} + \cancel{C_{it-BG}}}{C_{Si} + \cancel{C_{BOX}} + \cancel{C_{it-BG}}} \cdot \frac{C_{Si}}{C_{ox}} \simeq \frac{t_{ox}}{t_{BOX}} << 1\ [-] \tag{A.6}$$

$$SS_{min}(T) = ln(10) \cdot \frac{k_B \cdot T}{q}\ [mV/dec] \rightarrow \boxed{SS_{min}(300\ k) \simeq 60\ mV/dec} \tag{A.7}$$

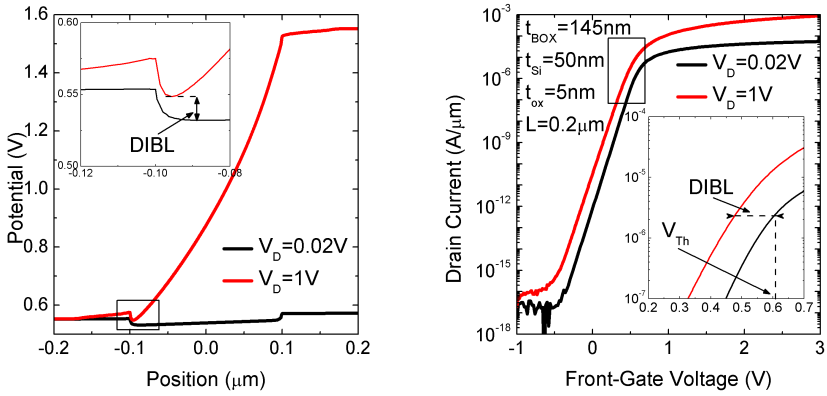
The characterization of the subthreshold swing is straightforward: the drain current curve is plotted in logarithmic scale as a function of the gate voltage applied. The resultant curve will present a straight line in the subthreshold region from which the subthreshold slope should be calculated, Figure A.5. To obtain the subthreshold swing (**SS**), the reciprocal of the subthreshold slope should be obtained (Equation A.8).

$$SS = \frac{1}{Subthreshold\ Slope} \rightarrow \boxed{SS = \frac{\partial V_{GS}}{\partial(log_{10}\ I_{DS})}\ [mV/dec]} \tag{A.8}$$

A.1.3. Drain Induced Barrier Lowering

The change of the threshold voltage with the drain to source biasing, or **DIBL**, shows how strong is the influence of drain voltage over the channel barrier that avoid carriers to flow during subthreshold operation. As drain to source voltage increases, the potential across the channel is pushed up by the drain region reducing the intrinsic built-in barrier due to the NPN junction (source-body-drain). This barrier reduction allows carriers to flow from the source to the drain at lower gate voltages (lower threshold voltages). This effect increases with reduced gate length since the S/D depleted regions influence extend further over the channel, and with increasing oxide layers due to fringing fields [ERFC07]. DIBL is thus defined as appears in Equation A.9.

$$\boxed{DIBL = \frac{\partial V_{Th}}{\partial V_{DS}}\ [V/V]} \tag{A.9}$$



(a) Potential profiles (b) Effect on drain current

FIGURE A.6: Simulated front-gate DIBL **(a)** effect on potential profiles lowering the built-in barrier for electrons (NMOS) and **(b)** drain current. $V_{BG} = 0$ V, $L = 0.2$ μm, $t_{Si} = 50$ nm, $t_{ox} = 5$ nm and $t_{BOX} = 145$ nm.

This short-channel effect should be extracted, using the previous equation: the gate voltage shift for a constant drain current in the subthreshold regime. In particular, once obtained the threshold voltage in the linear region (low drain bias), it should be checked the gate voltage for which the same drain current is flowing for a different and larger drain bias. Then, the ratio between the increase in both, gate voltage and drain bias, is performed. DIBL results in a linear decrease with drain bias of the threshold voltage [Sch06a] following Equation A.10, where λ (DIBL) is found to depend on channel length and less on temperature.

$$V_{Th}(V_{DS1}) = V_{Th}(V_{DS2}) - \lambda(T)(V_{DS1} - V_{DS2}) = V_{Th}(V_{DS2}) - \lambda(T)\ \Delta V_{DS}\ [V] \tag{A.10}$$

In Figure A.6 **(a)** it is illustrated how the drain voltage affects the potential profiles across the device reducing the potential barrier and in **(b)** how this

translates into a significant change into the drain current.

A.1.4. Carrier Mobility

The current driven by a MOSFET transistor in the active region ($V_{GS} > V_{Th}$) is proportional to the **carrier mobility**. Basically, the speed of a device is related to its driven current (together with some other parameters as the parasitic capacitances) and hence to its mobility, thus increasing this parameter is one of the mechanisms for enhancing its performance. Some of the strategies that have been used to do so are: the change of the crystallographic orientation of the lattice to enhance [SUKS06] or privilege the conduction of a type of carrier [DGR09]; substrate strain in Si induced using Ge [NWP$^+$93, WHG92]; the reduction of the body doping concentration to decrease the Coulomb scattering [YXD$^+$06]...

The most common techniques for extracting the carrier mobility are summarized here [Sch06a, Vas].

Bulk Mobility by Hall technique

Hall techniques are usually employed for **carriers concentration characterization**, **bulk mobility extraction** and **resistance measurements** [Lin52]. The basic setup of this technique is represented in Figure A.7. The conventional theory is developed considering a rectangular device with its length larger than its width, $L > W$. The **Hall effect** is a well known phenomenon that occurs when carriers move in the presence of a magnetic field perpendicular to the transport plane. Even if carriers are deflected by the *Lorentz force*, there cannot be any current in the transversal direction (y-axis) in stationary state. Indeed, the Lorentz force is balanced,

on the average, by an electric field, from now on, **Hall field** in the transversal direction.

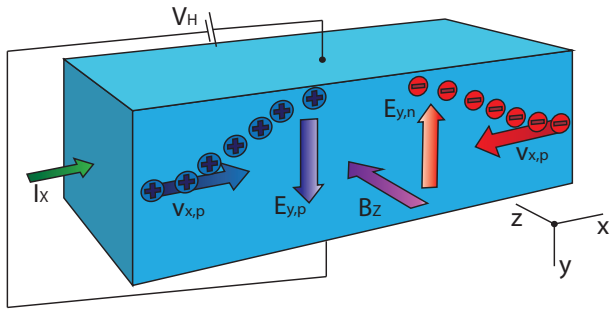


FIGURE A.7: Typical setup of a magnetoresistance measurement.

A piece of semiconductor device with length L, in the x-axis, width W, in y-axis and thickness t in the z-axis is considered, Figure A.7. A voltage difference is applied along the x-axis (not represented) leading to a current $\overrightarrow{I_x}$ directed to +x. The resultant Lorentz force motivated by the magnetic field oriented in the $+z$ direction, $\overrightarrow{B_z}$, is for electrons $\overrightarrow{F_{y,n}} = -q \cdot (-\overrightarrow{v_x} \times \overrightarrow{B_z})$ and for holes $\overrightarrow{F_{y,p}} = +q \cdot (+\overrightarrow{v_x} \times \overrightarrow{B_z})$ (the direction of the Lorentz force is finally independent of the carrier since the charge sign is compensated with the carrier's sense of motion). This force causes that carriers move and collect on the top of the device $(-y)$. With the charged carriers motion, two electric fields are generated aiming in opposite directions: $\overrightarrow{E_{y,n}}$ due to electrons and pointing to $-y$ and $\overrightarrow{E_{y,p}}$ due to holes and pointing to $+y$. Given that the vertical motion does not cause any current in stationary state, the electric field induced through the y-axis compensates the Lorentz Force leading to Equation A.11.

$$\overrightarrow{F_{y,n}} = (-q) \cdot \overrightarrow{E_{y,n}} + (-q) \cdot \left[-\overrightarrow{v_{x,n}} \times \overrightarrow{B_z} \right] = 0\,[N] \rightarrow \overrightarrow{E_{y,n}} = \overrightarrow{v_{x,n}} \cdot \overrightarrow{B_z}\,[V/cm] \tag{A.11}$$

It is possible then to relate the current due to one type of carrier, electrons for example, with the electric field they induced, Equations A.12 and A.13.

$$\overrightarrow{I_{x,n}} = -q \cdot n \cdot \overrightarrow{v_{x,n}} \cdot t \cdot W \; [A] \rightarrow \overrightarrow{v_{x,n}} = \frac{-\overrightarrow{I_{x,n}}}{q \cdot n \cdot t \cdot W} \; [cm/s] \tag{A.12}$$

$$\overrightarrow{E_{y,n}} = \frac{-\overrightarrow{I_{x,n}} \cdot \overrightarrow{B_z}}{q \cdot n \cdot t \cdot W} = \frac{+R_{H,n} \cdot \overrightarrow{I_{x,n}} \cdot \overrightarrow{B_z}}{t \cdot W} \; [V/cm] \tag{A.13}$$

where the Hall coefficient, R_H, is defined in Equation A.14.

$$R_{H,n} = \frac{-1}{q \cdot n} \; [cm^3/C] \tag{A.14}$$

The electric field in the y-axis can be expressed as $\overrightarrow{E_y} = V_H/W$, being V_H the Hall voltage. By substituting the electric field results Equations A.15 and A.16.

$$\frac{V_H}{W} = \frac{+R_{H,n} \cdot \overrightarrow{I_{x,n}} \cdot \overrightarrow{B_z}}{t \cdot W} \; [V/cm] \tag{A.15}$$

$$R_{H,n} = \frac{-1}{q \cdot n} = \frac{V_{H,n} \cdot t}{\overrightarrow{I_{x,n}} \cdot \overrightarrow{B_z}} \; [cm^3/C] \tag{A.16}$$

In the case of holes an analogous analysis leads to Equation A.17.

$$R_{H,p} = \frac{+1}{q \cdot p} = \frac{V_{H,p} \cdot t}{\overrightarrow{I_{x,p}} \cdot \overrightarrow{B_Z}} \; [cm^3/C] \tag{A.17}$$

And lastly, using the Hall coefficient, the Hall mobility can be extracted through Equations A.18 and A.19.

$$\boxed{\mu_{H,n} = \mu_{H,n}(-q \cdot n)\frac{-1}{q \cdot n} = -\sigma_n \cdot R_{H,n} = \frac{-\sigma_n \cdot V_{H,n} \cdot t}{\overrightarrow{I_{x,n}} \cdot \overrightarrow{B_z}} \, [cm^2/V \cdot s]} \tag{A.18}$$

$$\boxed{\mu_{H,p} = \mu_{H,p}(+q \cdot p)\frac{+1}{q \cdot p} = +\sigma_p \cdot R_{H,p} = \frac{+\sigma_p \cdot V_{H,p} \cdot t}{\overrightarrow{I_{x,p}} \cdot \overrightarrow{B_z}} \, [cm^2/V \cdot s]} \tag{A.19}$$

where the Hall voltage, V_H, thickness, t, current, $\overrightarrow{I_x}$, and magnetic field, $\overrightarrow{B_z}$ can be measured directly, and the conductivities $\sigma_{n,p}$ are whether known or can be obtained through resistance measurements.

Effective Mobility by Split-C(V)

The **effective mobility**, μ_{eff}, is deduced from the drain conductance in the linear region (it can be assumed that $V_{DS} << 1$ V and thus $V_{DS}^2 \simeq 0 \; V^2$) according to Equation A.20.

$$\boxed{g_d = \frac{\partial I_{DS}}{\partial V_{DS}} \, [A/V] \rightarrow \mu_{eff} = \frac{L}{W} \cdot \frac{I_{DS}}{Q_i \cdot V_{DS}} = \frac{L}{W} \cdot \frac{g_d}{Q_i} \, [cm^2/V \cdot s]} \tag{A.20}$$

where L and W are the gate length and width of the device, g_d is the drain conductance at constant gate to source voltage, I_{DS} is the drain current, V_{DS} is the drain to source bias and Q_i is the channel inversion charge in strong inversion. The inversion charge can be approximated as $C_{ox} \cdot (V_{GS} - V_{Th})$ [TM11]. Nevertheless, this approach has some deficiencies. The first is that the channel charge density is not exactly given by the previous expression. Second,

the threshold voltage is not necessarily well known and lastly, the capacitance C_{ox} is actually influenced by quantum effects like the *dark space region*.

Better results are obtained with a direct measurement of the inversion charge from capacitance measurements. The mobile channel charge density can be determined from the gate to channel capacitance per unit of area, C_{GC}, according to Equation A.21.

$$Q_i = \int_{-\infty}^{V_{GS}} C_{GC}(V_{GS})\,\mathrm{d}V_{GS}\ [C] \tag{A.21}$$

The integral's lower limit can be replaced by a front-gate voltage for which the device is on strong accumulation, V_{GS}^{acc}, (the front-gate voltage is much lower than the flatband voltage for a NMOS transistor, $V_{GS}^{acc} << V_{GS-FB}$) making $C_{GC} \simeq 0$ F because in strong accumulation the inversion channel has not been formed yet so the capacitance approaches zero (disregarding the overlap capacitances between gate and source or drain). The final expression for the inversion charge appears in Equation A.22.

$$Q_i = \int_{V_{GS}^{acc}}^{V_{GS}} C_{GC}(V_{GS})\,\mathrm{d}V_{GS}\ [C] \tag{A.22}$$

One common way to obtain the required capacitance measurement is to use the Split-C(V) technique. The **Split-C(V)** technique was first developed to measure the **trap density in the interface** and the **substrate doping** [Koo73]. Later, it was adapted to measure the **effective mobility** [SEM82]. This technique receives its name because it allows (on bulk devices) to extract separately the inversion charge (minority carriers such as electrons in a NMOS) or the depletion charge (Q_d, related to the majority carrier in the substrate) depending on the bias configuration. In SOI devices the buried oxide avoids the

extraction of the depletion charge. The Split-C(V) setup is shown in Figure A.8 where both drain and source regions are short-circuited while a bias (AC+DC) is applied to the front-gate with respect to the S/D regions. The opposite gate may be polarized as well with a constant DC voltage.

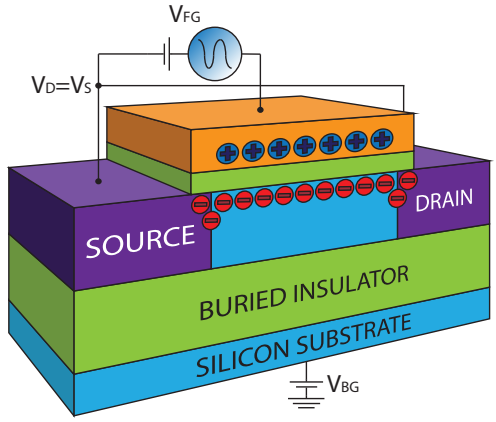


FIGURE A.8: Front-gate Split-C(V) mobility extraction technique scheme. The reference of the front-gate bias applied are the source and drain regions in order to collect the body minority carrier from them.

In order to measure the capacitance, the AC signal is mandatory. The capacitance should be measured at a sufficiently high frequency for interface traps to be unable to follow the AC signal, typically 100 kHz to 1 MHz. For low frequencies, the interface traps contribute with a capacitive component [Sch06a]. As the DC gate voltage is increased, more and more minority carriers are accumulated under the front-oxide increasing the capacitance measured. Most of these carriers come from the S/D grounded regions, forced by the $V_{G-S/D}$ voltage, instead of having to wait until they are thermally generated, which would limit the maximum frequency allowed. This modification turns to be especially important in case of SOI devices since it takes much more time to generate carriers than bulk MOSFETs because the volume of the silicon body is smaller.

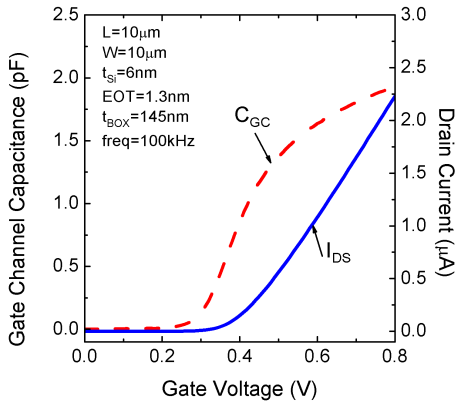


FIGURE A.9: Examples of drain current and gate to channel capacitance curves to extract the mobility using the Split-C(V) technique.

The effective channel mobility, μ_{eff}, is then extracted from a combination of the gate to channel capacitance (dashed line in Figure A.9) obtained through Split-C(V) and from the drain current measurements (solid line in Figure A.9).

For SOI, the Split-C(V) technique can also be used to extract the effective back-channel mobility with only interchanging the roles of the front and back-gates in the setup depicted in Figure A.8.

The previous analysis has assumed μ_{eff} to be invariant with the gate length but there are some studies and methods for taking it into account [RAEG04].

Finally, the **low-field mobility**, μ_0, can be extracted from the effective mobility, μ_{eff}, as its maximum, as appear illustrated in Figure A.10.

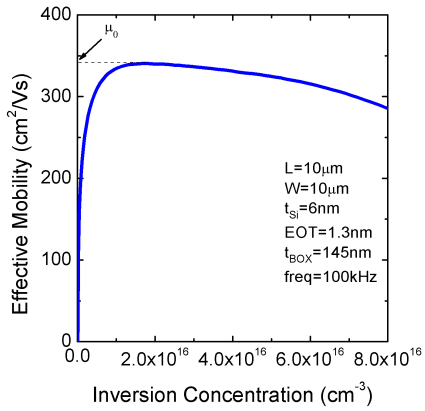


FIGURE A.10: Effective mobility plotted against the inversion carrier concentration. Extraction of the low field mobility as the maximum of the effective mobility.

Field-Effect Mobility by the Transconductance Peak

While the effective mobility is derived from the drain conductance, the **field-effect mobility** is calculated from the transconductance peak in the linear region of operation. It can be obtained starting from the drain current expression, Equation A.23, and doing then the first derivative, where it has been assumed again that the device operates in its linear region, $V_{DS}^2 \simeq 0\ V^2$. The final expression for the transconductance appears in Equation A.24.

$$I_{DS} = \frac{W}{L} \cdot C_{ox} \cdot \mu_{eff} \cdot \left((V_{GS} - V_{Th}) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right) \ [A] \tag{A.23}$$

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{W}{L} \cdot C_{ox} \cdot \mu_{eff} \cdot V_{DS} \ [A/V] \tag{A.24}$$

When this expression is solved for the mobility term, it is usually known as *field-effect* mobility, Equation A.25.

$$\boxed{\mu_{FE} = \frac{L}{W} \cdot \frac{g_{m,max}}{C_{ox} \cdot V_{DS}} \, [cm^2/V \cdot s]} \tag{A.25}$$

where $g_{m,max}$ makes reference to the peak value of the first derivative of the drain current against gate voltage that is illustrated in Figure A.1.

The experimentally measured field-effect mobility is normally lower than the previous effective mobility. The discrepancy obtained, even for the same device and bias conditions, is associated with the neglect of the electric-field dependence (more precisely, the neglect of the gate voltage dependence) in the derivation of the μ_{FE} expression [Vas]. Both terms can be related by Equation A.26.

$$\mu_{FE} = \mu_{eff} + (V_{GS} - V_{Th}) \cdot \frac{\partial \mu_{eff}}{\partial V_{GS}} \, [cm^2/V \cdot s] \tag{A.26}$$

Since the effective mobility decreases with gate voltage, $\partial \mu_{eff}/\partial V_{GS} < 0$ (except for very low gate voltages, where it actually increases due to decreased importance of Coulomb scattering), $\mu_{FE} < \mu_{eff}$. Therefore, if μ_{FE} is used for device modeling, the currents and device switching speeds are going to be underestimated. For recent technologies this method is not advisable.

A.1.5. Y-function

The **Y-function** [Ghi88] is a method for the extraction of MOSFET parameters based on the **combined exploitation of the** $I_{DS}(V_{GS})$ **and** $g_m(V_{GS})$ **characteristics**. Using both curves it is possible to avoid the effects of mobility degradation with gate voltage on the determination both of the threshold voltage and of the low field mobility. The parameter extraction is

performed within the strong inversion regime of the MOSFET linear region (the squared drain voltage term is neglected) [Sze81, MK86]. The drain current expression considering the attenuation factor term appears in Equation A.27.

$$I_{DS} = \frac{W}{L} \cdot C_{ox} \cdot \frac{\mu_0}{[1 + \theta \cdot (V_{GS} - V_{Th})]} \cdot (V_{GS} - V_{Th}) \cdot V_{DS} \, [A] \tag{A.27}$$

where W and L are the effective channel width and length, C_{ox} is the gate oxide capacitance per unit of area, μ_0 is the low field mobility, θ is the mobility reduction coefficient, V_{Th} is the threshold voltage and V_{GS} and V_{DS}, are the gate and drain to source voltages respectively.

The transconductance g_m of the MOSFET is obtained with the derivative of the Equation A.27 leading to Equation A.28. Both, drain current and transconductance can be observed for a given device in Figure A.11.

$$g_m = \frac{W}{L} \cdot C_{ox} \cdot \frac{\mu_0}{[1 + \theta \cdot (V_{GS} - V_{Th})]^2} \cdot V_{DS} \, [A/V] \tag{A.28}$$

The basic idea of this technique consists in constructing a new function, through a proper combination of the previous drain current and transconductance expressions, which eliminates the influence of the mobility attenuation with gate voltage. This can be achieved by dividing the drain current expression by the square root of the transconductance as Equation A.29

$$\boxed{Y = \frac{I_{DS}}{\sqrt{g_m}} = \sqrt{\frac{W}{L} \cdot C_{ox} \cdot \mu_0 \cdot V_{DS}} \cdot (V_{GS} - V_{Th}) \, [A \cdot V]} \tag{A.29}$$

Since all parameters are constant, in strong inversion the Y-function should be linear in gate voltage. The intercept with the x-axis (V_{GS}) gives the

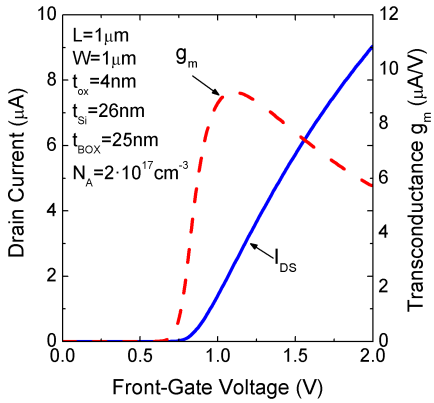


FIGURE A.11: Experimentally obtained curves of drain current and transconductance for a given FD-SOI MOSFET. For high gate voltages the drain current presents a lower slope due to series resistance effects and mobility attenuation factor. This degradation complicates the extraction of some electrical parameters.

threshold voltage, Equation A.30. Assuming that L, W and C_{ox} are known, the slope, m, provides the low effective mobility, Equation A.31. The resultant Y-function curve is illustrated in Figure A.12.

$$\boxed{V_{Th} = V_{GS}(Y = 0)\,[V]} \tag{A.30}$$

$$\boxed{\mu_0 = \frac{m^2 \cdot L}{W \cdot C_{ox} \cdot V_{DS}}\,[cm^2/V \cdot s]} \tag{A.31}$$

A.1.6. Oxide Thickness

Front-gate oxide thickness is one of the most sensitive parameters in MOSFETs. Although the oxide thickness is one of the best controlled physics

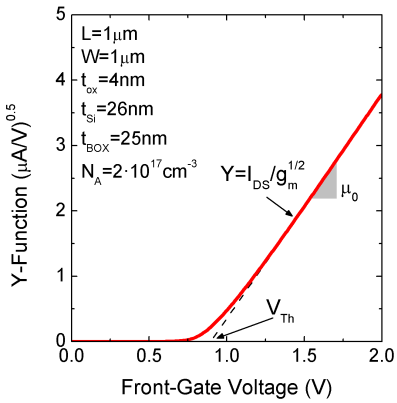


FIGURE A.12: Threshold voltage and low field mobility extraction using the Y-function. Notice the linearity in strong inversion whereas the drain current was degraded in Figure A.11.

parameters during transistor fabrication, it is necessary to obtain accurate measurements of it, which are typically indirects. In this section the t_{ox} will be studied through two techniques: the **inter-gate coupling** presented in FD-SOI MOSFETs and by capacitance measurements.

Inter-Gate coupling

For FD-SOI transistors, the **inter-gate coupling makes the threshold voltage of one gate to be strongly linked to the bias applied on the opposite gate (or substrate)**. Both parameters are related by the *Lim-Fossum model*, Equation A.32 [LF83].

$$V_{Th-FG}^{dep} = V_{Th-FG}^{acc} - \frac{C_{Si} \cdot C_{BOX}}{C_{ox} \cdot (C_{BOX} + C_{Si} + C_{it-BG})} \cdot (V_{BG} - V_{BG}^{acc}) \, [V] \tag{A.32}$$

where the back and front-gate may be interchanged depending on the gate under study. This coupling effect serves to study the dependence of $V_{Th}(V_{BG})$ (or $V_{Th}(V_{FG})$) but also to relate its slope with the front-gate oxide thickness though its capacitance, C_{ox}. So, knowing the slope, m, the thickness of the oxide can be calculated using Equation A.33.

$$m = \frac{-C_{Si}C_{BOX}}{C_{ox}(C_{BOX} + C_{Si} + C_{it-BG})} \rightarrow \boxed{t_{ox} = \frac{-C_{Si}C_{BOX}}{m\epsilon_{ox}(C_{BOX} + C_{Si} + C_{it-BG})}\,[cm]} \tag{A.33}$$

In Figure A.13 some examples of this dependence for the front-gate threshold voltage against the back-gate bias are illustrated. For thick silicon films (circles and squares) the supercoupling effect [ECC+07] does not take place. The Si-film is thick enough to allow the coexistence of both types of carriers when inverting one interface while accumulating the opposite at the same time. The supercoupling effect can be easily checked by verifying if the device presents or not flat threshold voltage regions. These flat regions indicate that the front-gate threshold voltage remains fixed not depending on the opposite gate bias. This coupling suppression appears as a consequence of the collected carriers; the electric field from the back-gate is screened avoiding it to influence the front-gate. If the silicon film gets very thin (triangles) the threshold voltage does not present any flat region. This suggest that it is not possible to have both types of carriers at the same time in the body; supercoupling effect is then taking place.

Capacitance Equivalent Thickness

Capacitance Equivalent Thickness technique, is based on the direct gate to channel capacitance measurements as a function of the front-gate bias applied, $C_{GC}(V_{FG})$. It is usually chosen $V_{FG} = 1.2$ V since it is the typical power supply voltage on CMOS at this moment. From the area of the transistor

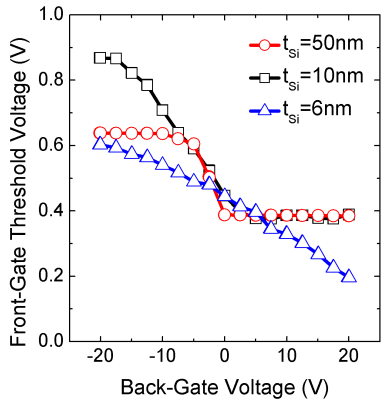


FIGURE A.13: Threshold voltage as a function of the back-gate bias for different silicon film thickness devices. When the silicon film is thin enough, the curve does not present any flat region meaning supercoupling effect is taking place.

(W and L) and the capacitance at a specific bias point, the front gate oxide thickness can be extracted using Equation A.34.

$$C_{GC}(V_G = 1.2V) = \frac{\epsilon_{ox} \cdot A}{t_{ox}} \, [F] \rightarrow \boxed{t_{ox} = \frac{\epsilon_{ox} \cdot A}{C_{GC}(V_G = 1.2V)} \, [cm]} \tag{A.34}$$

Given that the permittivity of the silicon dioxide has been used, the obtained thickness is actually the *equivalent oxide thickness*. In general, the thickness conversion from other dielectric material X to EOT can be done through Equation A.35 for planar structures.

$$C_{SiO_2} = \frac{A \cdot \epsilon_{SiO_2}}{t_{SiO_2}} = \frac{A \cdot \epsilon_X}{t_X} = C_X \, [F] \rightarrow \boxed{EOT = t_{SiO_2} = \frac{\epsilon_{SiO_2} \cdot t_X}{\epsilon_X} \, [cm]} \tag{A.35}$$

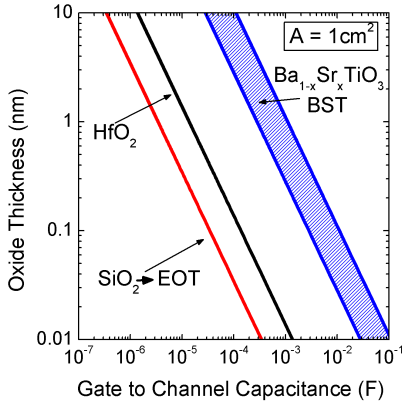
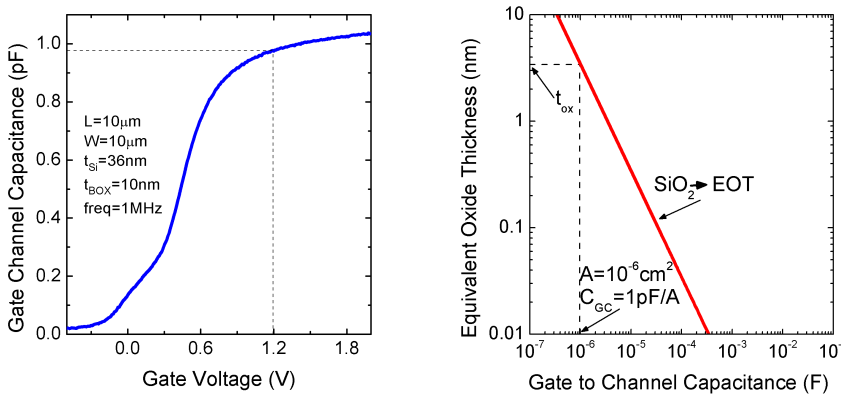


FIGURE A.14: Dielectric thickness against gate to channel capacitance normalized to $A = 1\ cm^2$ for silicon oxide, SiO_2, hafnium oxide, HfO_2, and barium strontium titanate $Ba_{1-x}Sr_xTiO_3$ whose thickness varies depending on the barium to strontium ratio.

The resultant thicknesses can be represented against the gate to channel capacitance for different materials as shown in Figure A.14. It is important to point out that in order to use this representation, the gate to channel capacitance used should be re-scaled depending on the area of the device by Equation A.36.

$$C_{GC-Graph} = \frac{C_{GC-Measured}(V_{FG} = 1.2V)}{A_{cm^2}}\ [F/cm^2] \tag{A.36}$$

An experimental example of this method is illustrated in Figure A.15. At $V_{FG} = 1.2\,V$ the capacitance measured is around $1\,pF$ for an area of $A = 100\,\mu m^2$ (Figure A.15 **(a)**). After converting the area in squares cm ($A_{cm^2} = 10^{-6} cm^2$) and calculating the graph capacitance (Equation A.37), the insulator



(a) Capacitance extraction (b) Oxide thickness extraction

FIGURE A.15: **(a)** Gate to channel capacitance extraction, at $V_{FG} = 1.2$ V the capacitance is 1pF for an area $A_{cm^2} = 10^{-6} cm^2$. **(b)** The gate oxide thickness result for SiO_2 where the area should be scaled to cm^2: $A = 100\ \mu m^2 = 10^{-6}\ cm^2$.

thickness can be extracted from Figure A.15 **(b)**.

$$C_{GC-Graph} = \frac{C_{GC-Measured}(V_{FG} = 1.2V)}{A_{cm^2}} = \frac{1\,pF}{10^{-6}\,cm^2} \simeq 1\,\mu F/cm^2 \tag{A.37}$$

The final thickness of the front-oxide is for SiO_2 material, $EOT = 3.36\,nm$.

Appendix B

ET FD-SOI Transistors

B.1. Electrical Characterization of Extremely-Thin SOI MOSFETs

The characterization of FD-SOI transistors with Extremely-Thin Si-film allows the study of ultimate devices. They provide a good reference for benchmarking the static results obtained for the A2RAM cells in Chapter 6 (all characterization techniques applied here are discussed in Appendix A). This way, the weaknesses and strengths of the memory cells as typical transistors will be highlighted. The MOSFETs devices measured present the characteristics listed in Table B.1. All ET FD-SOI devices were fabricated at CEA-LETI Grenoble in 22 nm node process using 300 mm SOI UNIBOND® (100) wafers (see Figure B.1).

The study of these devices [RAN+11], whose structure appears depicted in Figure B.2, was performed as a function of the wafer temperature with

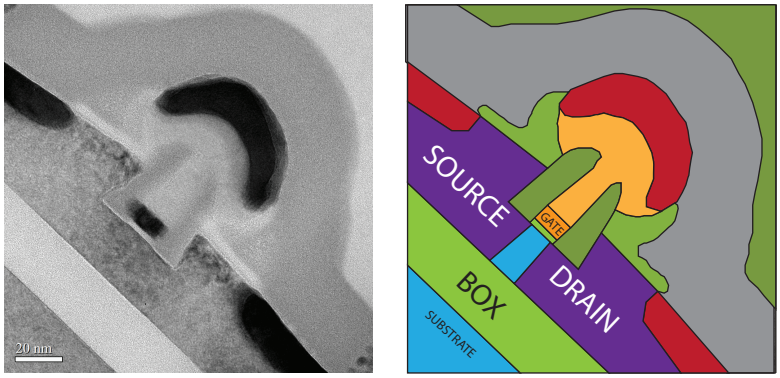


FIGURE B.1: Transmission Electron Microscope image from 30nm FD-SOI transistor fabricated at CEA-LETI Grenoble.

Parameter	Symbol	Value	Units	
Silicon Film Thickness	t_{Si}	6	nm	Si
Equivalent Oxide Thickness	EOT	1.3	nm	HfO_2
Buried Oxide Thickness	t_{BOX}	145	nm	SiO_2
Mask Gate Length	L	30-10.000	nm	-
Gate Width	W	80-10.000	nm	-

TABLE B.1: Physical characteristics of ET FD-SOI MOSFETs that will be used for benchmarking.

variations between -50 °C and 250 °C. In particular, the following parameters were extracted:

- Threshold Voltage (V_{Th}).
- Subthreshold Swing (SS).
- Drain induced barrier lowering ($DIBL$).
- Equivalent front-gate oxide thickness (EOT).

- Mobility (μ).

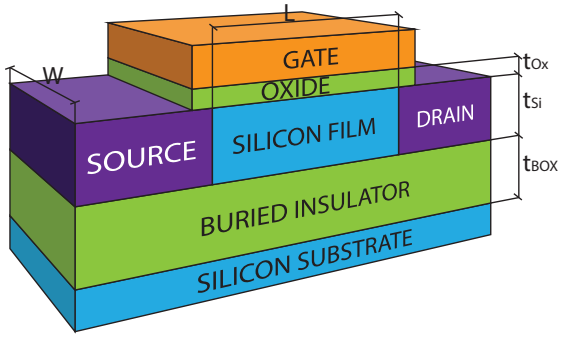


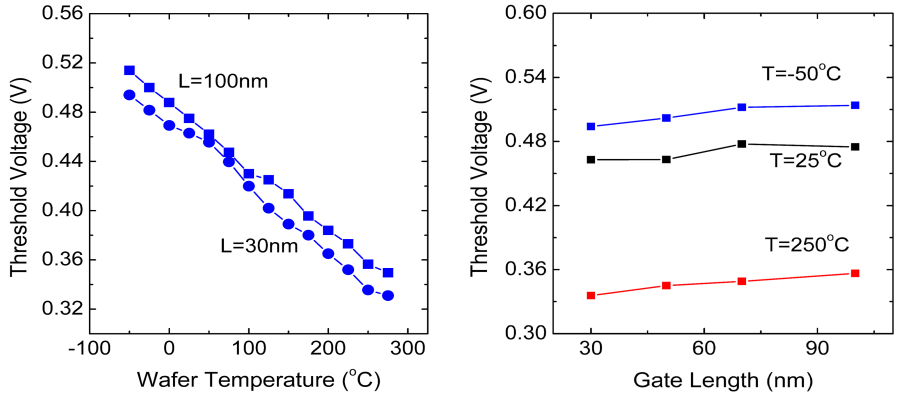
FIGURE B.2: Diagram of typical ET FD-SOI MOSFET structure used for benchmark the static characteristics of the A2RAM cells.

B.1.1. Threshold Voltage

To extract the threshold voltage the **Y-function** technique [Ghi88] was used (see Appendix A). The reason of choosing this method is the large *series resistance* that these transistors feature due to the ultra-thin silicon film and the non-doped body [And12, MWK$^+$09]. Y-function corrects the first order terms of series resistance improving the accuracy of the extracted values. The threshold voltage as a function of the wafer temperature, $V_{Th}(T)$, is shown in Figure B.3 **(a)** for two transistors with different gate length, 30 and 100 nm. The temperature dependence is almost the same for both channel length: the threshold voltage decreases when increasing the temperature with a slope around $\partial V_{Th}/\partial T \simeq$ -0.6 mV/°C. The variation with temperature is motivated by the **dependence of the Fermi potential level with temperature through the thermal voltage** ($\phi_T = k_B \cdot T/q$).

On the other hand, the variation of threshold voltage with the gate length is illustrated in Figure B.3 **(b)** for three distinct temperatures. Regardless the

temperature applied, V_{Th} is almost constant with the gate length. However, a slight decrease is observed when shrinking the channel length caused by the SCEs (threshold voltage *roll-off*).



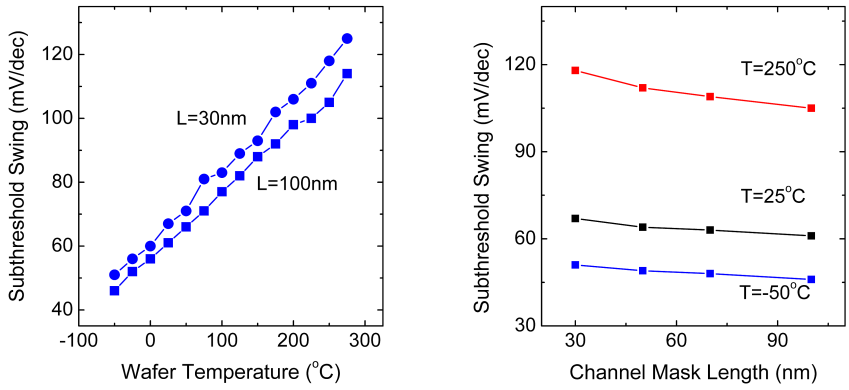
(a) Against temperature (b) Against gate length

FIGURE B.3: Threshold Voltage dependence with **(a)** temperature and **(b)** gate length. $W = 80$ nm, $t_{Si} = 6$ nm, $EOT = 1.3$ nm and $t_{BOX} = 145$ nm.

B.1.2. Subthreshold Swing

The obtained subthreshold swing values against temperature appear in Figure B.4 **(a)** for gate length. Independently of the length, a constant increase in the subthreshold swing with temperature is obtained. The slope is around $\partial SS/\partial T \simeq 0.25\,(mV/dec\cdot^{\circ}C)$ which is very close to the ideal slope dependence, Equation A.6. The ideal temperature dependence is given by Equation B.1.

$$\frac{\partial SS}{\partial T} = ln(10)\cdot\frac{k_B}{q} \simeq 0.2\,(mV/dec\cdot^{\circ}C) \tag{B.1}$$



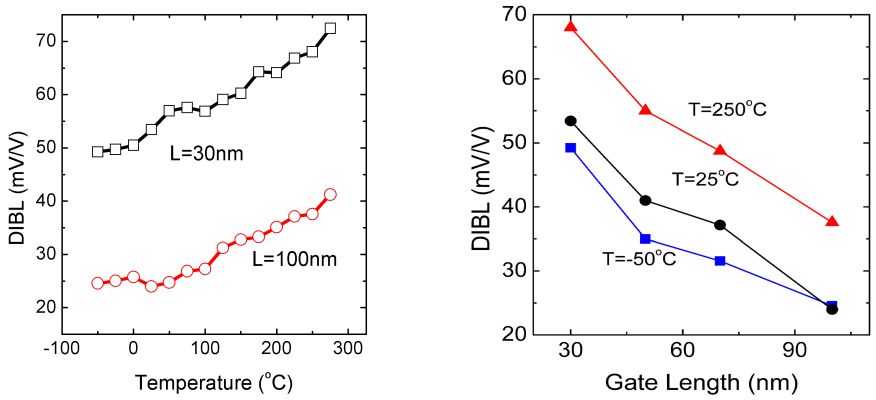
(a) Against temperature (b) Against gate length

FIGURE B.4: Subthreshold Slope dependence with **(a)** temperature and **(b)** gate length. $W = 80$ nm, $t_{Si} = 6$ nm, $EOT = 1.3$ nm and $t_{BOX} = 145$ nm.

According to Figure B.4 **(b)**, the SS is almost independent of the transistor gate length. At room temperature, the values measured are very close to the minimum SS of $60\,mV/dec$ (Equation A.7) demonstrating the benefits and goodness of FD-SOI technology. As gate length is reduced, the subthreshold swing value slightly increases up to 12 % of its minimum value at $L = 100\,nm$. This rise is related to the lateral influence caused by source and drain depletion regions.

B.1.3. Drain Induced Barrier Lowering

The Drain Induced Barrier Lowering has been studied as a function of the temperature (Figure B.5 **(a)**) and gate length (Figure B.5 **(b)**). For these ET FD-SOI transistors, with such a thin silicon film, the sensitivity of the threshold voltage with the bias applied to the drain region is extremely low. Even for the worst high temperature case, $T = 250\,°C$ and for the



(a) Against temperature (b) Against gate length

FIGURE B.5: Drain induced barrier lowering dependence with **(a)** temperature and **(b)** gate length for ET FD-SOI MOSFET. $W = 80$ nm, $t_{Si} = 6$ nm, $EOT = 1.3$ nm and $t_{BOX} = 145$ nm.

shortest device, 30 nm, the DIBL is below 70 mV/V. λ Equation A.10) is nearly temperature insensitive [BG01]. It increases around 20 mV/V for a temperature rise of $T = 300$ °C. The increase in DIBL when reducing the channel length is motivated by the higher influence the source and, especially, drain regions have on the channel creation. As the length of the gate is reduced it becomes more difficult for the gate to electrostatically drive the channel.

B.1.4. Oxide Thickness

In this section the front-gate **oxide thickness** is studied by the electrostatic inter-gate coupling [LF83], Figure B.6. It is easy to relate the slope of the front-gate threshold voltage coupling with back-gate bias to the EOT using Equation B.2. Since the buried oxide is quite thick, $T_{BOX} = 145$ nm, it is necessary to sweep from large negative up to large positive back-gate voltages.

In this case, the sweep has been performed in the range of $V_{BG} = -25$ V to $V_{BG} = 20$ V with a bias step of 1 V.

$$EOT = t_{SiO_2} = -\frac{C_{Si} \cdot C_{BOX}}{m \cdot \epsilon_{SiO_2} \cdot (C_{BOX} + C_{Si} + C_{it-BG})} = 1.25\, nm \tag{B.2}$$

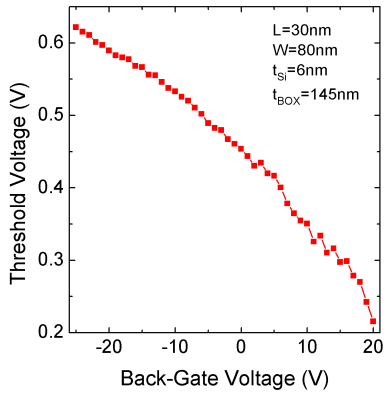


FIGURE B.6: Threshold voltage dependence with back gate bias. Supercoupling effect is taking place since no flat region is observed for negative back-gate biases. $L = 30$ nm, $W = 80$ nm, $t_{Si} = 6$ nm and $t_{BOX} = 145$ nm

where it has been assumed that the interface state density is negligible ($D_{it-BG} = 0\ cm^{-2}eV^{-1}$). No significant difference, lower than 1 %, is found when changing this value to a more realistic like $D_{it-BG} = 10^{11}\ cm^{-2}eV^{-1}$. The obtained final EOT is 1.25 nm, which fits very well with the value provided by CEA-LETI of 1.3 nm from spectroscopic ellipsometry measurements [CSN+00].

Another interesting point is that the coupling curve does not arrive to any flat region for negative V_{BG}. There is no point where the front-gate threshold voltage is insensitive to changes in the back bias and takes a constant value.

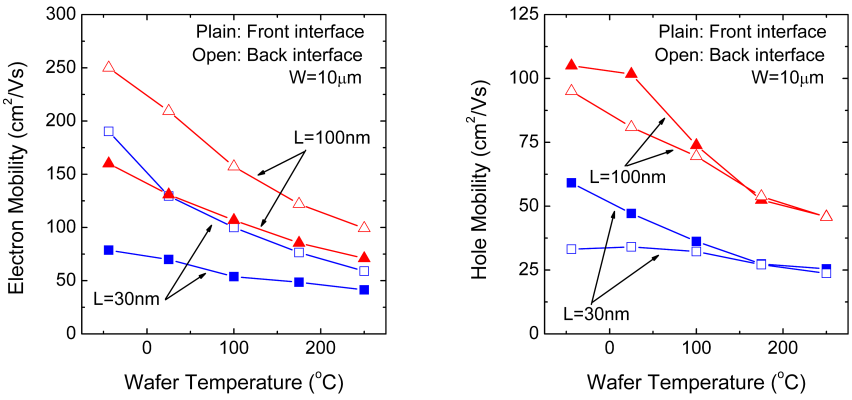
This means that these devices suffer from supercoupling effect [ECC+07]. Their silicon film thickness is only 6 nm so no accumulation of holes at the back interface is possible once the front interface is inverted with electrons.

B.1.5. Mobility

The **carrier mobility** for these ET FD-SOI transistors was extracted for the front, Silicon *high-k*, and the back, Silicon SiO_2, channels. The Y-function technique was employed taking into account N but also P-MOSFETs. The mobility for electrons is represented against the wafer temperature in Figure B.7 **(a)** for a gate length of 30 nm (squares) and 100 nm (triangles). Regardless the channel-length considered, the back-interface mobility (open symbols) appears to be much larger than the obtained for the front interface (plain symbols). This difference is due to a larger carrier scattering because of the **remote coulomb scattering due to the *high-k* stack** used in the front interface. The maximum mobility value is always achieved for the minimum temperature, $T = -50°\text{C}$. The phonon scattering has less impact on mobility at lower temperatures. In any case, the back-channel mobility is almost twice the front one. This difference is attenuated when increasing the temperature of the wafer. For $L = 30$ nm the back-channel mobility decays to less than 40 % of its maximum when $T = 250°\text{C}$. Although it is specially remarkable for the back interface and short transistors, this behavior is repeated also for longer devices, $L = 100$ nm, and the front interface.

Assuming that the **phonon scattering is the main responsible for the mobility decrease with temperature** [CHD+97], the temperature coefficient, k, can be extracted by using Equation B.3.

$$\mu \simeq \left(\frac{T}{T_0}\right)^{-k} \; [cm^2/V \cdot s] \tag{B.3}$$



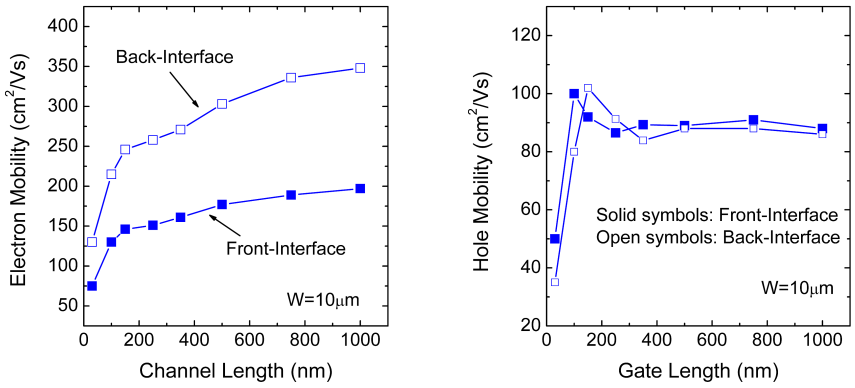
(a) Electrons (b) Holes

FIGURE B.7: Front and back-channels mobility dependence with wafer temperature for several gate lengths for **(a)** electrons and **(b)** holes. $W = 10\ \mu$m, $t_{Si} = 6$ nm, $EOT = 1.3$ nm and $t_{BOX} = 145$ nm.

where k takes distinct values for the front and back interfaces. For $L = 30$ nm and the front Silicon-*high-k* interface $k_{FG} = 0.79$, and in the back Silicon-SiO_2 interface $k_{BG} = 1.39$. These values demonstrate that the SiO_2 **back interface is more affected by phonon scattering**.

Regarding the hole mobility, Figure B.7 **(b)**, now surprisingly, is the front interface which presents the better mobility results. At low temperatures the difference is maximum but as temperature increases, the difference between channel mobilities is drastically reduced until both curves merge together no matter the chosen gate length.

The dependence of electron mobility with the gate length is represented in Figure B.8 **(a)**. As gate length is shrunk the electron mobility dramatically decreases. This effect has been attributed to the **presence of *neutral effect* and additional *coulomb scattering* from source and drain regions** [PNFBV$^+$09]. On the other hand, hole mobility is almost constant for devices



(a) Electrons (b) Holes

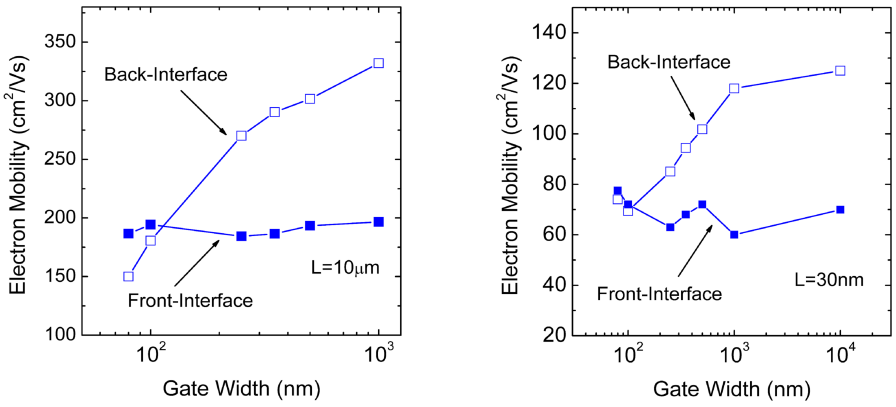
FIGURE B.8: Mobility dependence with gate length for front and back-interfaces for **(a)** electrons and **(b)** holes. $W = 10\ \mu$m, $t_{Si} = 6$ nm, $EOT = 1.3$ nm and $t_{BOX} = 145$ nm.

featuring channel length over 100 nm, Figure B.8 **(b)**. However, for shorter transistors, $L < 100\,nm$, the hole mobility also drops. In contrast to electron mobility, for holes, the mobility is again similar in both channels.

An important mobility size effect is manifested when reducing the device width in Figure B.9. The back-channel mobility rapidly degrades when reducing the gate width. This undesired effect is related to the employed lateral isolation technique, STI. To understand how the STI degrades the mobility, it is necessary first to study how the device is processed, Figure B.10. Its main steps are listed here:

0. The start process begins with a wafer on which a thin silicon dioxide, SiO_2, has been grown to deposit the nitride, Si_3N_4.

1. The first step is to etch a trench from the top to the buried oxide.



(a) Long channel (b) Short channel

FIGURE B.9: Electron mobility dependence with gate width for front and back-interfaces for **(a)** $L = 10\ \mu$ m and **(b)** $L = 30$ nm. $t_{Si} = 6$ nm, $EOT = 1.3$ nm and $t_{BOX} = 145$ nm.

2. After that, a very thin and good quality silicon dioxide is grown thermally on the sides that are now exposed of silicon.

3. The trench is filled with SiO_2 by **CVD** (*Chemical Vapor Deposition*).

4. Finally, the excess of nitride is removed by chemical mechanical polishing.

STI isolation technique induces compressive uniaxial strain into the silicon film layer (the crystallographic orientation of devices considered was (100)) affecting the lattice structure [BKC+10]. The initial and ideal lattice symmetry is destroyed by strain so that the electrical behavior is modified through the change in the band structure. This stress depends on the crystallographic orientation of the channel and on the type of carrier. The change in the lattice translates into different carrier effective masses leading to different mobility results. In case of electrons, the **compressive strain induced by STI turns to be detrimental as it reduces the electron**

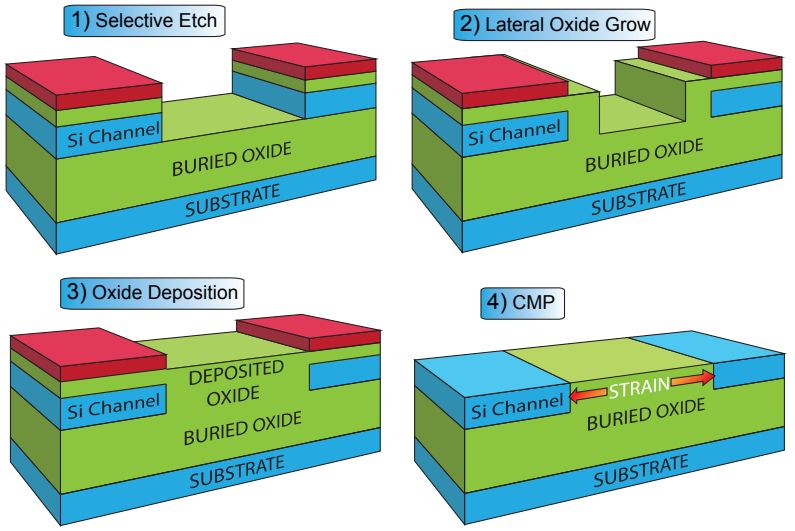


FIGURE B.10: Main steps to isolate devices using STI technique

mobility [SLR+99, OWI+00], Figure B.9. Since the front-channel mobility is mostly limited by remote Coulomb scattering from the high-k stack, it does not vary that much with the gate width. As a consequence, the back-channel mobility can become lower than the front for very short MOSFETs (Figure B.9 **(a)**). The situation can however be improved by recessing the STI which relieves the compressive stress in the channel [KST07] or using tensile strain induced by heteroepitaxial strain [ACB+05]. Unlike for electrons, different results are found for holes. No degradation is observed when reducing the gate width (the **compressive strain seems to be beneficial for holes**, as suggested by Figure B.8 **(b)** [DGR09, SOM+03, TAA+04]).

Appendix C

Multi-Branch Mobility Representation and Analysis

C.1. Introduction

Carrier mobility is one of the most important parameters in semiconductor based devices. It is often used to benchmark the experimental data for demonstrating the benefits of new technologies as could be, silicon-germanium channels, source and drain metallic regions or strained channel. Sometimes it is difficult to extract mobility in MOSFETs. Firstly, because it is necessary to used indirect measurements since no direct technique can be applied but, specially, because this parameter depends on several factors as type of carrier, doping concentration, temperature, interface quality (charges and surface roughness)...

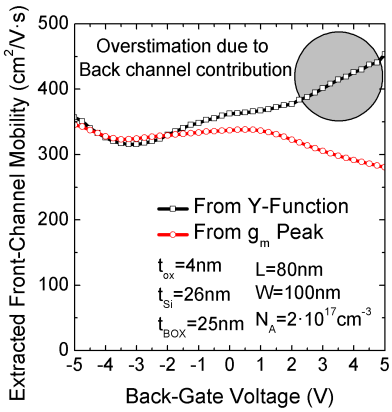
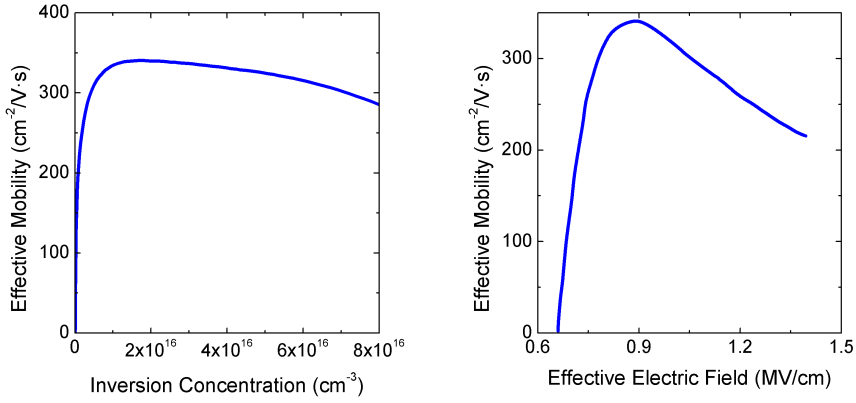


FIGURE C.1: Front-channel electron mobility as a function of the back-gate voltage extracted with two different characterization techniques. Mobility is overestimated when the back-channel is inverted since that moment the overall mobility is the contribution of front and back-channel. $V_{BG} = 3\,V$.

In bulk MOSFETs, mobility results reflect the properties of the channel below the front-gate oxide, as a result, the physical interpretation is simple. In this case, several techniques can be used to extract mobility (some explained in Appendix A). On the other hand, for SOI MOSFETs, the extraction is much more complicated. Now, two different channels may be present, the same front-channel as before and the one created when using the buried oxide as the back-gate oxide. **In SOI, mobility has multiple channel contributions** that are hard to discriminate. Furthermore, the **standards techniques are not always suitable for SOI devices**. This turns to be especially true when a back-gate bias is applied (Figure C.1) or when the silicon film is very thin leading to *supercoupling* effect [ECC+07].

When applying a back-gate bias the back-channel is enhanced. If any technique is used to obtain the front-interface mobility, it is possible than **not only the front-channel but also the back-channel are contributing to**

the mobility. The mobility extraction is hence distorted.



(a) Against inversion charge (b) Against E_{eff} approximation

FIGURE C.2: Typical SOI representations of mobility against **(a)** inversion charge and **(b)** the approximation of effective electric field.

Common studies on SOI typically show effective mobility against inversion charge, Figure C.2 **(a)**, or against a debatable effective electric field approximation, Figure C.2 **(b)** [EMC$^+$01]. However, these representations do not provide enough information to fully understand the contribution of each channel to the characterized mobility. **Multi-Branch representation permits the separation and therefore accurate interpretation of how each channel is contributing to total effective mobility**.

C.2. Split-C(V) Mobility Results

The Multi-Branch technique [NRO$^+$12] is based on **mobility results extracted using the Split-C(V) technique** (detailed in Appendix A). In this case, it has been used to characterize the electron and hole mobility in two

different devices. Both kind of devices are presented in Figure C.3 with their main parameters summarized in Table C.1.

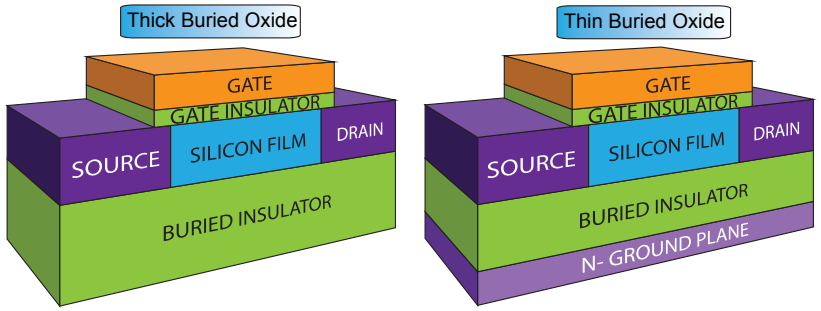
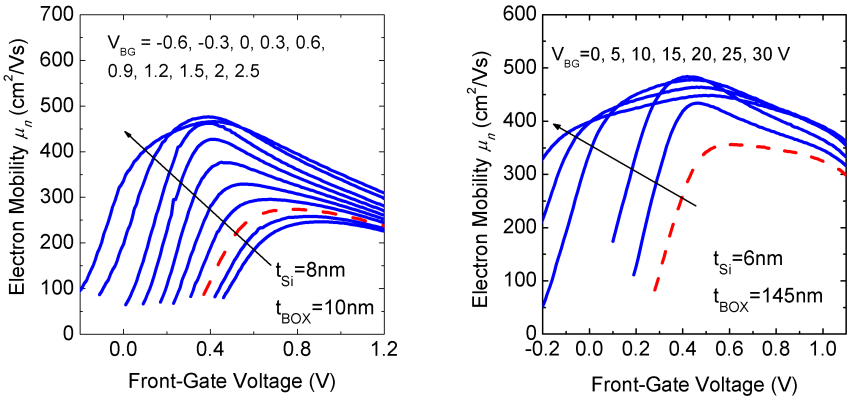


FIGURE C.3: Devices selected for testing the Multi-Branch mobility representation, their main difference is the thickness of the buried oxide. At the left, device A with $t_{BOX} = 145$ nm and at the right, device B with $t_{BOX} = 10$ nm.

Parameter	Device A	Device B	Units
Silicon Film Thickness	6	8	nm
Equivalent Oxide Thickness	1.3	1.3	nm
Buried Oxide Thickness	145	10	nm
Mask Gate Length	10	10	μm
Mask Gate Width	10	10	μm
Ground Plane	Not present	N-Type	-

TABLE C.1: Parameter of the two different badges of samples used for Multi-Branch mobility representation.

Figure C.4 **(a)** shown how electron mobility changes for thin buried oxide transistors when varying the back-gate bias applied. The curve for $V_{BG} = 0$ V is represented in dashed line and the arrow aims to increasing back-gate voltages. In the case of thick buried oxide devices the results is very similar: a **remarkable increase in the mobility is obtained as the back-bias is risen**.

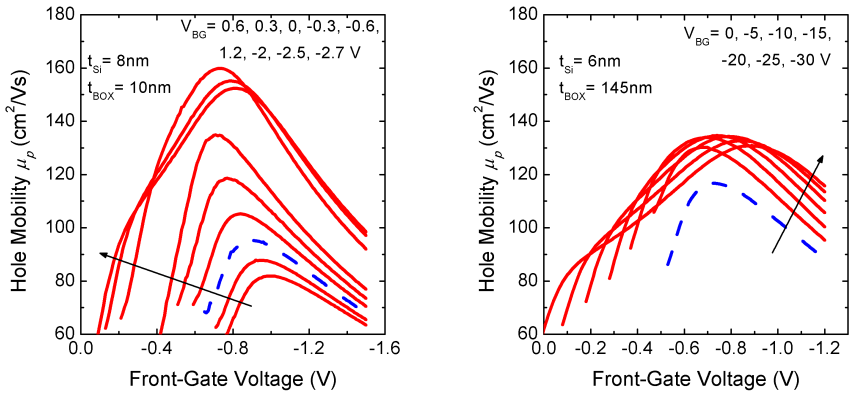


(a) Thin buried oxide (b) Thick buried oxide

FIGURE C.4: Electron mobility enhancement by back-gate biasing for **(a)** thin and **(b)** thick BOX devices. Arrows aim to higher back-gate voltages, in dashed the curve for $V_{BG} = 0$ V.

The same behavior, but for decreasing back-gate voltages, is observed for holes in Figure C.5 where the dashed curve is again the one corresponding to zero back-gate voltage and the arrows aim in this case to decreasing V_{BG}. Results show again an increase in mobility by only applying a voltage to the back-gate. This means that **biasing the back-gate is a performance booster for this ultra thin silicon film devices**. The reason is that these devices, N-type or P-type, benefit from **volume conduction regime: carriers are shift to the center of the silicon film where they suffer less scattering due to the interfaces**. This turns to be more important when using a *high-k* stack that normally degrades more the mobility. These results agree with previous studies [OBFBC12, RCG07, KSU09].

The mobility gain has been defined as the mobility increase with respect to the case of the back-gate grounded, Equation C.1. μ_{max} is the maximum mobility for a given back-gate voltage and μ_0 the maximum mobility when the



(a) Thin buried oxide (b) Thick buried oxide

FIGURE C.5: Hole mobility enhancement by back-gate biasing for **(a)** thin and **(b)** thick BOX transistors. Arrows aim to lower back-gate voltages, the curve for $V_{BG} = 0$ V is dashed.

back-gate voltage is zero volts. Mobility gain is represented as a function of the back-gate voltage normalized by the buried oxide thickness (to compare between different carriers and different BOX thickness layers) in Figure C.6.

$$\mu_{Gain} = \frac{(\mu_{max} - \mu_0)}{\mu_0} \cdot 100\ [\%] \tag{C.1}$$

A **maximum enhancement for thin BOX devices of around 70 %**, no matter the type of carrier, is found in the comparison. This mobility enhancement is reduced below **40 % when moving to thick buried oxides**. Multi-Branch mobility representation will be used later to explain this large difference obtained for different thicknesses of buried oxides.

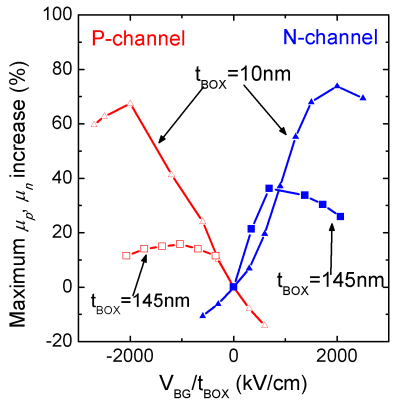


FIGURE C.6: Mobility gain by back-gate biasing comparison between holes and electrons for thin and thick BOX.

C.3. Multi-Branch Mobility Representation

The Multi-Branch representation is a novel way to represent the mobility against the most accurate expression of effective electric field. **Multi-Branch representation combines experimental mobility results with effective electric field simulations obtained with a calibrated Poisson-Schroedinger solver** at the same time. The integral definition of the effective electric field appear in Equation C.2.

$$E_{eff} = \frac{\int |\overrightarrow{E_z}| \cdot p_z \, dz}{\int p_z \, dz} \, [V/cm] \tag{C.2}$$

Given that the evaluation of the this integral implies to know $\overrightarrow{E_z}$, the vertical electric field inside the device, and p_z, the vertical inversion charge profile, it is usually taken an approximation like Equation C.3 for SOI,

[SSCAeb].

$$E_{eff} = \frac{1}{\epsilon_{Si}} \cdot (\eta \cdot Q_i + Q_d) + E_{back} \, [V/cm] \tag{C.3}$$

Where E_{back} is the electric field at the back surface and η is a constant that represents the weighting of the inversion charge and the depletion charge. η value depends on the crystal orientation [SC79]. It is normally assumed to be $\eta = 0.5$ for electrons on silicon (100) [TTIT94b, AG87], and $\eta = 0.33$ for holes on silicon (100) [SKU07], there is some debate around though.

The problem is that **the approximation is not accurate when applying a back-gate bias** to the transistor as shown in Figure C.7. It can be seen how the approximation (dashed line), does not follow properly the values provided by the integral and more accurate definition (solid line). The approximation is monotonically increasing since it is proportional to the inversion charge. The integral, on the other hand, presents at first for low front-gate voltages, a decrease behavior.

This decrease in effective electric field is motivated by the absolute value of the vertical electric field in the integral definition. The electric field evolution with increasing front-gate voltages for a back-gate bias of zero volts is shown in Figure C.8 **(a)**. In this case, as the voltage applied to the front-gate increases, the vertical electric field also increases monotonically. In Figure C.8 **(b)** on the other hand, with $V_{BG} \neq 0 \; V$, although the vertical electric field is still always increasing, it starts from negative values, so, its absolute value shows initially a drop until the vertical electric field goes beyond zero toward positive values, $\overrightarrow{E_z} > 0 \, V/cm$, and start increasing again.

Hence using the integral definition becomes a major issue when applying back biasing schemes. The problem is the evaluation of this integral. To do so, it is necessary to know the transverse electric field across the device and also

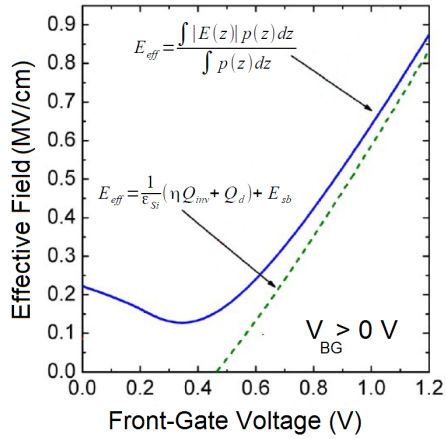
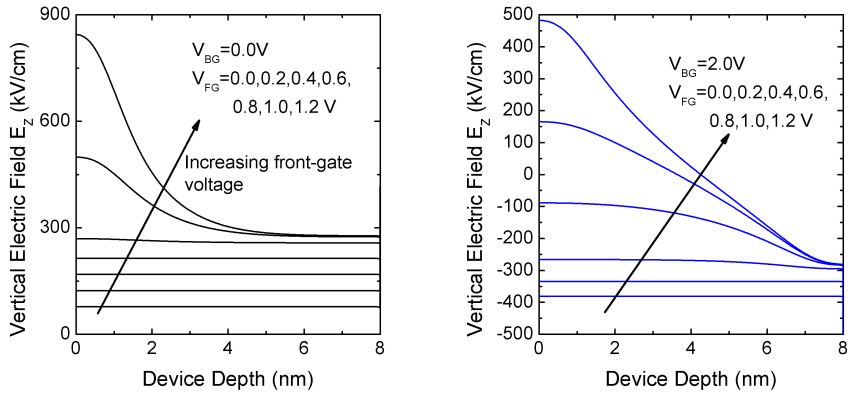


FIGURE C.7: Effective electric field comparison between formula and approximation when a back-gate bias is applied. Notice how the approximation (dashed line) fails to follow the integral values (solid line) [CRG10].

the profile of inversion charge. These quantities are impossible to measure experimentally and are only available performing numerical simulations by using TCAD software. **The Poisson-Schroedinger solver is used to calculate the profile distribution of inversion charge and the vertical electric field across the device, allowing the final evaluation of the effective electric field by its integral definition**.

For optimal results and, in order to reduce the errors, the solver will be calibrated with the help of the experimental measurements previously performed to extract the mobility by Split-C(V). The inversion charge will be fitted tuning the metal work-function, Φ_M, and the body doping concentration of the devices, $N_{A,D}$. In Figure C.9 an example of this fitting is presented. For best adjustment in the whole back-gate range, two opposite extreme values of back-gate voltage are fitted. It can be seen the almost **perfect matching**



(a) No back-gate applied $V_{BG} = 0$ V (b) Back-gate applied $V_{BG} \neq 0$ V

FIGURE C.8: Vertical electric field inside the device ($t_{Si} = 8$ nm and $t_{BOX} = 10$ nm) for **(a)** $V_{BG} = 0$ V and **(b)** $V_{BG} \neq 0$ V. Arrows aims to increasing front-gate voltages. Notice how although both are always increasing with front-gate voltage, however the absolute value in the case of $V_{BG} \neq 0$ V will make it to be decreasing at first.

between simulations (solid line) **and experimental points** (open squares symbols).

Finally, the methodology to elaborate the Multi-Branch mobility plot can be summarized in three steps:

1. The **effective mobility is experimentally determined** by the front-gate split-C(V) method, leading to a $\mu_{eff}(V_{FG})$ plot for each back-gate value (Figures C.4 and C.5).

2. A self-consistent **Poisson-Schroedinger solver is used to determine the profiles of** $\overrightarrow{E_z}$ (Figure C.8) **and** p_z (not illustrated) in Equation C.2 to perform the final calculation of E_{eff}. The solver is calibrated to reproduce the $Q_i(V_{FG})$ (Figure C.9) curves obtained from the front-gate

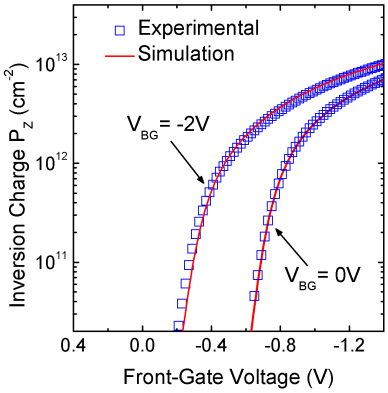


FIGURE C.9: Experimental inversion charge extracted using Split-C(V) (open squares symbols) and simulated (solid lines). This fitting was performed to calibrate the Poisson-Schroedinger solver.

split-C(V) measurements by tuning the metal work-function and doping concentration.

3. Once the $\mu_{eff}(V_{FG})$ and $E_{eff}(V_{FG})$ are determined in the first and second steps, they can be combined using the front-gate voltage to complete the actual Multi-Branch mobility representation by plotting $\mu_{eff}(E_{eff})$.

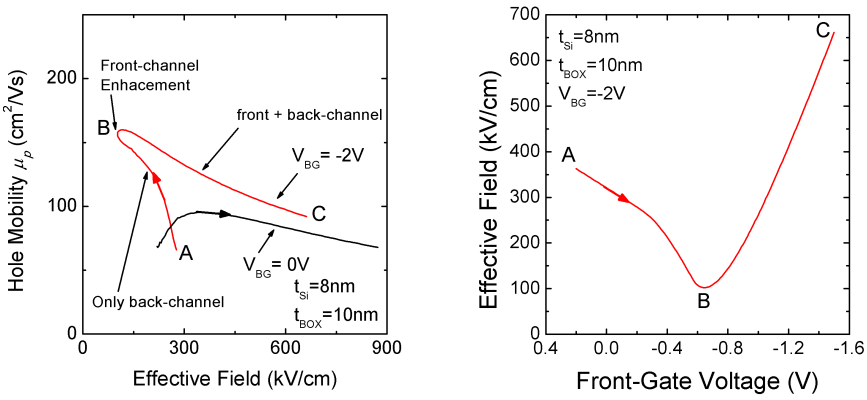
C.4. Experimental Application

The complete Multi-Branch curves for the previous devices at different bias conditions are presented here.

C.4.1. Multi-Branch examples

The Multi-Branch plot for holes in thin buried oxides films is represented in Figure C.10 **(a)** when $V_{BG} = 0$ V and $V_{BG} = -2$ V. To facilitate the understanding, the effective electric field against the front-gate voltage for $V_{BG} = -2$ V is also represented in Figure C.10 **(b)**. In this example, the case with $V_{BG} = 0\,V$ presents the **typical effective mobility curve reflecting the scattering from Coulomb centers, phonons and surface roughness**, very similar to the behavior previously seen in the **UMC** (*Universal Mobility Curve*) [TTIT94a, TTIT94b]. However, the non-zero back-gate voltage ($V_{BG} = -2V$) curve shows a much more interesting behavior. A result to remark is that **two distinct mobility values can be obtained for a given effective field**. This is due to **different carriers concentration profiles inside the device**. Multi-Branch name is originated due to the presence of these two regions clearly differentiated: one with only the back-channel activated and another with the front and back-channels enhanced simultaneously. In this scenario, when moving from point **A** to point **B**, this is the back-branch, the front-gate voltage is reduced (PMOS moving towards inversion) so the back-gate threshold voltage is also reduced by inter-gate coupling. The back-channel is then more enhanced and leads to an increase in mobility. In point **B**, the front-interface gets also enriched with holes so, from now on, both interfaces contribute to the effective mobility. Decreasing more the front-gate bias, going from point **B** to point **C**, back+front branch, makes the mobility to decay due to an increase in the effective electric field as observed in Figure C.10 **(b)**. The last thing to point out is that the back+front branch presents higher mobility values than the back branch, this will not be the case for NMOS.

A **similar behavior is found for electrons** in thin BOX devices, Figure C.11. Firstly, the $V_{BG} = 0$ V curve shows the typical UMC behavior as before. When biasing the back-gate, $V_{BG} = 2$ V curve, in point **A**, only

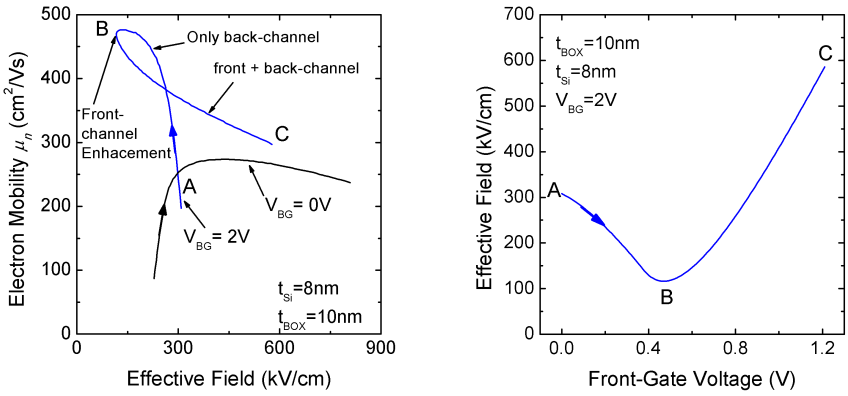


(a) Multi-Branch (b) Effective electric field

FIGURE C.10: **(a)** Multi-Branch representation and **(b)** effective electric field for holes in devices with thin buried oxide.

the back-channel is enriched so the mobility is only due to back-interface. As front-gate voltage is increased (enhancing the electron concentration of the NMOS), from **A** to **B**, the front surface potential increases making the channel to move towards strong inversion and increasing the mobility. In point **B** the front-channel starts to contribute also in the mobility and increasing more the front bias reduce the mobility because of the rapid rise of the effective electric field. It is very interesting to notice that **in contrast to what happened to holes, the electron mobility for the back branch is larger than the back+front branch in narrow buried oxides**. This different mobility contribution of the front branch attending to the type of carrier is related to the concentration profiles along the Si-film as will be detailed later. The same result is obtained for thick BOX transistors.

PMOS devices with thick buried oxide are represented in Figure C.12. The back interface is strongly inverted in point **A**. As the front-gate bias is decreased moving to **B**, the absolute value of the vertical electric field decreases (although

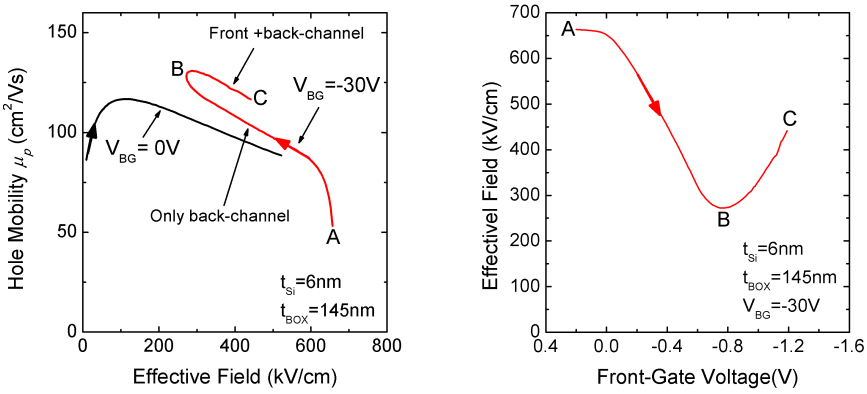


(a) Multi-Branch (b) Effective electric field

FIGURE C.11: **(a)** Multi-Branch representation and **(b)** effective electric field for electrons in devices with thin buried oxide.

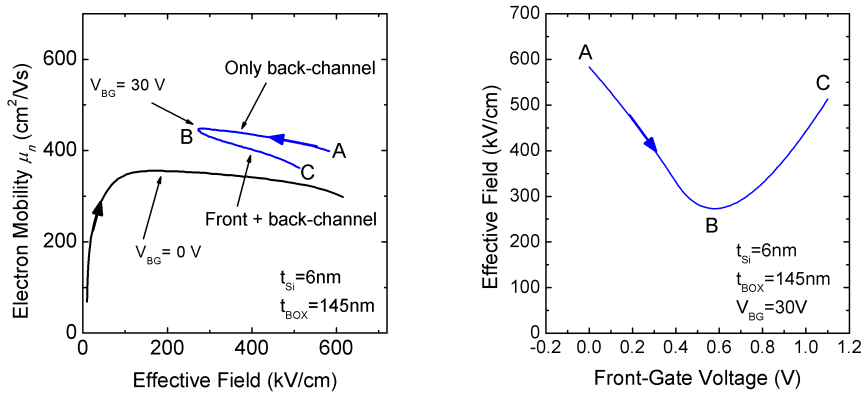
the vertical electric field is increasing as explained before). This translates into a reduction in the effective field and finally, into an increase in the mobility. Once beyond point **B**, holes starts to be collected also in the front interface leading to the enhance of the front-channel. From this point and up to point **C**, the mobility decreases due to the rise of the effective electric field motivated by the increase of the vertical $\overrightarrow{E}$ (in point **B** the vertical $\overrightarrow{E}$ now goes over zero and the absolute value starts to rise). As mentioned before, thick BOX PMOS transistors feature a higher mobility for the back+front branch than for only the back branch.

Lastly, the case of NMOS with thin buried oxide is analyzed in Figure C.13. The behavior is quite similar to those previously analyzed. From point **A** to **B** the front-gate voltage is increased reducing the effective electric field. This leads to an increase in the mobility. At point **B** the front-channel is also enhanced and E_{eff} starts to increase so the mobility drops.



(a) Multi-Branch (b) Effective electric field

FIGURE C.12: **(a)** Multi-Branch representation and **(b)** effective electric field for holes in devices with thick buried oxide.

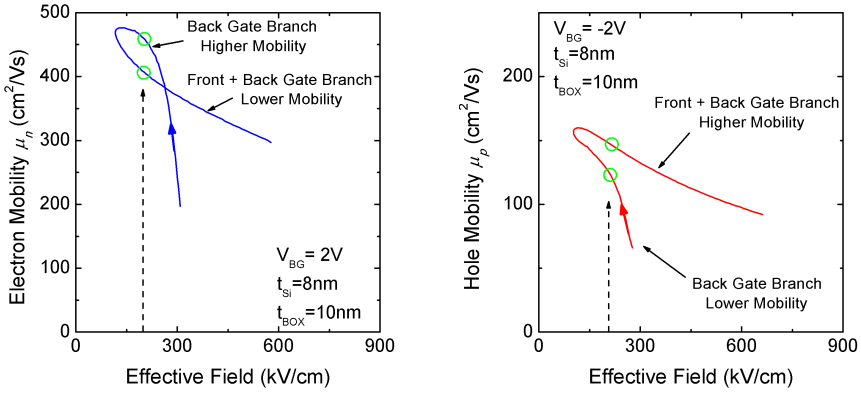


(a) Multi-Branch (b) Effective electric field

FIGURE C.13: **(a)** Multi-Branch representation and **(b)** effective electric field for electrons in devices with thick buried oxide.

C.4.2. Mobility Carrier Dependence

It was demonstrated that **the contribution of the front interface was beneficial for holes but detrimental for electrons** (Figure C.14). To explain this dependence of carrier mobility once the front interface is enhanced, the carriers concentration profiles are studied at a constant and equal effective electric field of 200 kV/cm (circles) for the thin BOX samples.

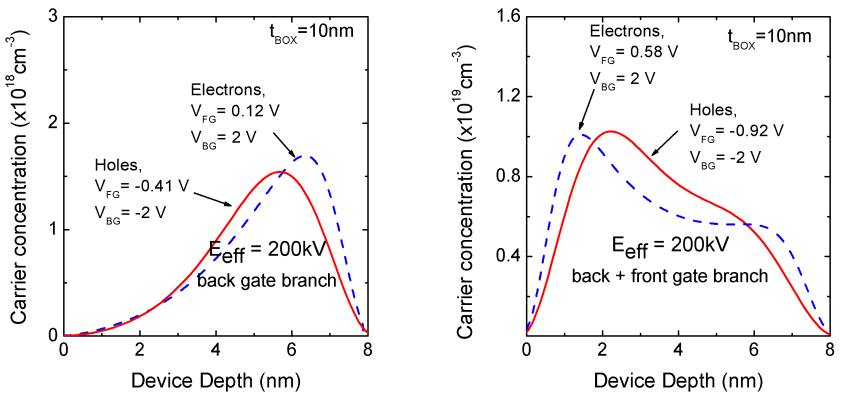


(a) Detrimental for electron (b) Beneficial for holes

FIGURE C.14: Difference between the effect of the front interface regarding the type of carrier, **(a)** electrons and **(b)** holes. The effect appears to be beneficial for holes and detrimental for electrons when comparing with their back branch. The thin BOX samples have been considered.

The resultant carrier profiles distribution are represented against the depth of the device (vertical position in the silicon film) in Figure C.15. The back branch in **(a)**, shows that both profiles are spread to the back interface (the unique interface inverted at that point). The difference distribution between them can be attributed to the distinct effective masses of carriers ($m^*_{e,l} \simeq 0.98 \cdot m_0$ for the longitudinal effective electron mass and $m^*_{h,lh} \simeq 0.16 \cdot m_0$ for the effective light hole mass). Once the front-channel is

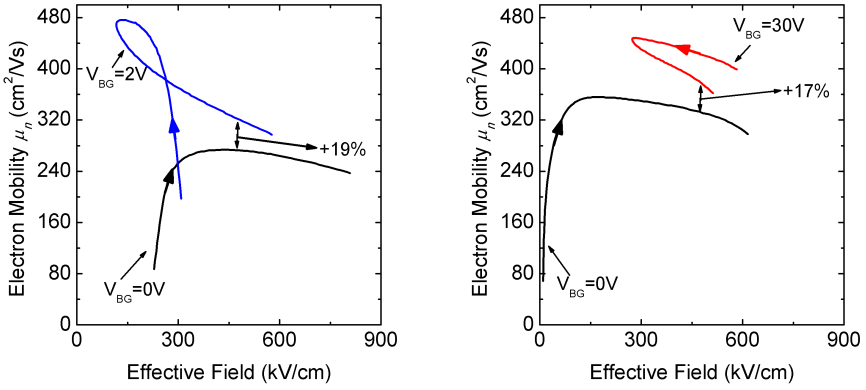
also enriched, the back+front branch in **(b)** shows how the profiles for electrons and holes are now more spread to the center of the Si-film. This effect is called *volume conduction regime*. It implies that the conduction along the dispositive is not the typical surface conduction seen in a bulk transistor with a charge sheet layer beside the interface. In this case the carriers flow in the middle of the silicon film. The channel now cannot be considered as a charge sheet anymore, and instead of that, the carriers go through a piece of the silicon volume separated from both oxides. This conduction spaced from the interfaces reduces the mobility degradation due to interface scattering (mainly surface roughness). Nevertheless, the scattering mechanism associated with the front *high-k* interface is still the most limiting factor. The profiles also show that this volume conduction is specially remarkable in the case of holes because they present larger carrier concentrations in the center of the device. This is the reason why holes benefit more from the inversion of both interfaces at the same time.



(a) Carriers profile for back branch (b) Carriers profile for front+back branch

FIGURE C.15: Carrier profile concentration attending to the branch for a constant effective electric field (200 kV/cm), **(a)** back branch and **(b)** front+back branch. $t_{ox} = 1.3$ nm, $t_{Si} = 8$ nm and $t_{BOX} = 10$ nm.

C.4.3. Multi-Branch Mobility Enhancement



(a) Thin buried oxide

(b) Thick buried oxide

FIGURE C.16: Mobility enhancement by back-gate biasing for Multi-Branch representation. The difference between **(a)** thin and **(b)** thick buried oxide devices is not so remarkable as seen when comparing against V_{BG}/t_{BOX}.

In Figure C.6 was presented a large difference in mobility gain between thin and thick BOX transistors when a applying a back-gate voltage. A comparison of mobility using the Multi-Branch representation is now represented in Figure C.16. The case for electrons is shown in Figure C.16 **(a)** for thin BOX devices and **(b)** for the thick BOX case. If the previous gain comparison is now made against a constant effective electric field of 450 kV/cm (instead of using a constant bias over BOX thickness), the difference drastically decreases and is not so remarkable as before. For thin BOX transistors, **(a)**, the difference is only 19 % and for thick devices, the difference arrives now only to **(b)** 17 %. The conclusion is that the comparison using a constant V_{BG}/t_{BOX} is quite unfair since it does not take into account the physics inside the device (carrier concentration profiles). It only considers the external bias applied and the device film structure.

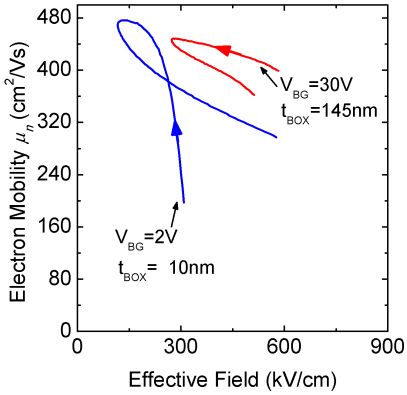


FIGURE C.17: Left-shift to lower effective electric field for thin devices which motivates higher mobility due to lower scattering by surface roughness.

It is also worth noting that there is a shift to lower effective electric fields in the case of thin BOX devices, Figure C.17, so **the large mobility in narrow buried oxide devices may be attributed to lower E_{eff} rather than any other technological factor** [TTIT94a, TTIT94b].

C.4.4. Drawbacks and Advantages

The main disadvantage that this technique presents is that it is not only based on direct measurements but it needs to go through experiments and also simulations. This implies more steps and time spent to complete it. Nevertheless, it has been demonstrated that the Multi-branch plots turn to be an interesting tool to take into account, showing much more information, and more accurately, than other approximations that has been used over last years. Some of the benefits that Multi-branch representations show are [FRO+13]:

- The mobility is obtained experimentally, no simulations are used to extract any mobility value.
- The representation is against the integral definition of the effective electric field and not against a debatable approximation [CRG10].
- It allows to separate the contributions of the mobility for the front and back interfaces for a better understanding.
- It can be used with the front or back-gate Split-C(V).

C.5. Conclusions

In this appendix, the Multi-Branch technique has been presented and discussed. Both NMOS and PMOS have been considered in different film structure devices, featuring thin and thick buried oxides. The results obtained show a better understanding of the behavior inside the transistors allowing a proper discrimination of interface contributions on mobility. The increase in mobility by back-gate biasing schemes is again demonstrated showing, better mobility values in case of thin silicon film devices due to lower effective electric fields and better results for holes than electrons due to distinct effective masses.

Appendix D

Characterization Facilities

D.1. Instruments and Equipments

In this section the most important instruments and equipments that have been used in the nano-electronic laboratory (Figure D.1) are briefly explained and discussed.

D.1.1. Semi-Automatic Probe System

The Semi-Automatic probe system used in all measurements was the *Suss Microtec PA300 PS-MA*, Figure D.2 [Cas12]. It permits the measurements for fine-pitch probing of pads down to $30\mu m \times 30\mu m$. The semi-automatic probe system employs the *ProbeShield* technology, enabling accurate low-noise measurements of atto amps and femto farads. It is prepared to make studies against the temperature in a range from -60 °C to $+300$ °C. Finally, it enables the automatic measurements of a specified pattern along all the wafer. To do

FIGURE D.1: Photography of the nano-electronic laboratory in Granada.

so, a previous calibration (to take into account non-idealities in the surface of the wafer measuring its deviation) and adjustment is required (the final contact is performed manually).

D.1.2. Semiconductor Analyzer

The semi-automatic wafer prober does not perform any measurements itself, it only helps contacting down to device level for other equipment. The main instrument used for measuring is the *Agilent B1500* semiconductor analyzer [Agi12a, Agi12b]. This analyzer is oriented to the characterization of semiconductor based devices. The B1500 semiconductor analyzer can be fully customized adding or removing different plug-in modules to fit the requirement of the user or application. Its rear view, composed by different modules as a rack, is represented in Figure D.3. Each module has specific characteristics oriented for particular applications: power units (HP-SMU and MP-SMU),

FIGURE D.2: Semi-Automatic probe system by Suss Microtec. This equipment provides a perfect environment for accurate current and capacitance low-noise measurements.

frequency unit for capacitance measurements (MF-CMU), high resolution voltage/current measurements unit (HR-SMU), high voltage (HV-SPGU) and an arbitrary waveform generator (WGFMU). Most of these units are **SMUs** (*Source Monitor Units*) that are able to generate and measure synchronously currents and voltages at the same time. This equipment also provides already defined software measurement setups for many of the most usual configurations: IV and CV curves, CMOS devices, solar cells, power devices...

D.1.2.1. Arbitrary Waveform Generator

The **WGFMU** (*Waveform Generator Fast Measurement Unit*) is the arbitrary waveform generator in the B1500. This module is named B1530 [Agi12d, Agi12c]. The WGFMU module offers the combination of arbitrary linear waveform generation with synchronized fast current or voltage measurement for up to two channels, which enables high-speed IV

FIGURE D.3: Front and rear view of the Agilent B1500 Semiconductor Analyzer. This instrument is the equipment in charge of performing most of the measurements. Notice in the rear view the different plug-in modules installed.

characterization. It allows to generate not only DC, but also various types of AC waveforms (such as pulses, staircase sweeps and staircase pulsed sweeps) with 10 ns programmable resolution. The connector panel of this module is depicted in Figure D.4.

FIGURE D.4: Agilent B1530 Waveform Generator. This module driven by the B1500 semiconductor analyzer allows it to perform arbitrary pattern measurements.

To facilitate the measurement setup, **RSUs** (*Remote-Sense Switch Unit*) are used together with the B1530. They permit the connection of the probes to a SMU (HR,HP,MP...) or the WGFMU without changing any cable. The internal switch diagram is shown in Figure D.5.

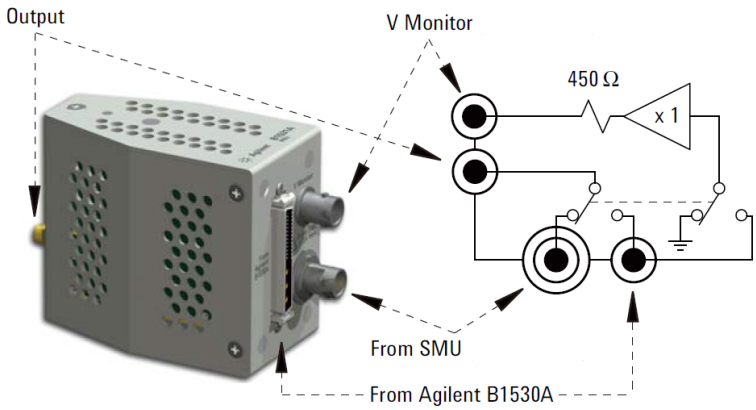


FIGURE D.5: The Remote-Sense Switch Unit (RSU) and its internal scheme that allows to act as SMU or WGFMU without changing any cable.

Given the nature of the transistor and its usual operation as memory, based on specific programming operations (Read/Write/Erase/Hold), it results very convenient to apply a custom bias pattern. To do so, the WGFMU is used to create a specific memory programming sequence. The patterns generated are usually applied to the front-gate and to the drain.

D.1.2.2. Needle Setup

For a proper DC measurement setup (Figure D.6), it is necessary to connect not only the WGFMU using the RSU to the probes but also some of the probes between them using a short-open cable, see Figure D.7. The short-open cables interconnect on one side, yellow, the shield and the signal line while on the other side, black, there is no signal pin. They are used to drive the drain current return path and share the ground connection between source and well terminals and the shielding protection.

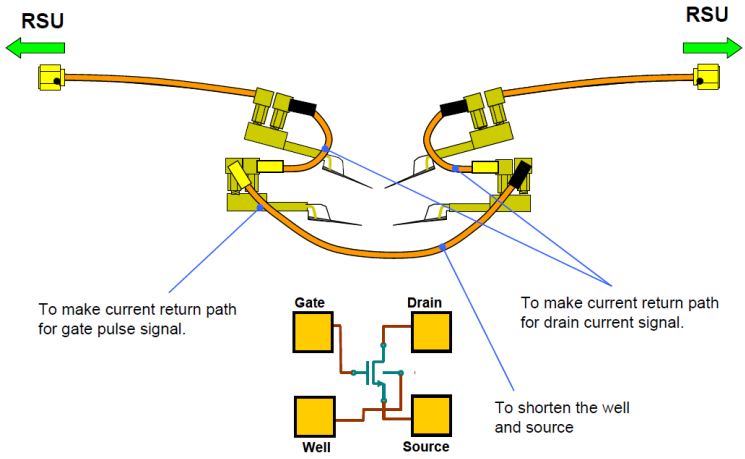


FIGURE D.6: DC probes measurement setup for WGFMU. Only the front-gate and drain pads receive an arbitrary pattern signal from the WGFMU.

If the shielding conductors of test cables are not interconnected properly at the ends of the cables, accurate loop current does not flow through the cables and, as a result, the measurement range will be limited, or in some cases, measurements cannot be made [Agi09].

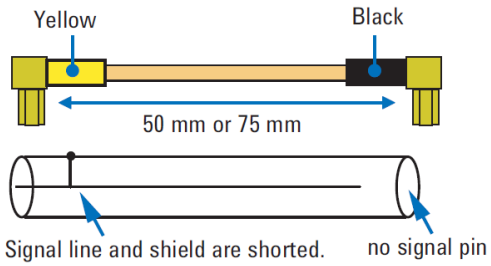


FIGURE D.7: Short-Open cable and its internal connection diagram. This cable allows to drive the drain current return path, yellow side, and share the ground connection between source and well (substrate) in the black side.

Short Summaries

English

In the present work it has been summarized the actual state of semiconductor based dynamic memories, focusing in one of the alternatives to complement or replace (depending on the application) the typical 1T+1C DRAM, the FB-DRAM cells. Some of the most important candidates of FB-DRAM have been detailed to give a consistent point of view when presenting the A2RAM, main objective of this work. This novel and advanced floating-body DRAM cell has been extensively studied, firstly, by TCAD simulations, from its fabrication to its electrostatic behavior, and then experimentally characterized at wafer level in different substrate configurations, bulk and SOI.

Some of the most powerful and widely used methods and characterization techniques have been presented and exemplified with a set of state-of-the-art ET FD-SOI transistors fabricated at CEA-LETI Grenoble. The obtained results have been used to benchmark the A2RAM in order to give an idea of how the extra steps of fabrication of these memory cells, influence its operation as a typical transistor. The degradation of some parameters when the device is operated as an usual transistor is set aside by the extraordinary properties

as memory. It has been shown how its memory concept of operation fits the electrical simulations and finally the experimental results extracted. These results give an idea of the excellent potential the A2RAM cell present, providing solids arguments to consider this cell as a real candidate for future DRAMs, specially for embedded applications.

Español

En el presente trabajo se ha resumido el estado actual de las memorias dinámicas basadas en semiconductores. Se ha prestado especial atención a una de las alternativas para complementar o reemplazar (dependiendo de la aplicacin) a la celda DRAM compuesta por un transistor y un condensador, las memorias FB-DRAM. Algunas de las candidatas más importantes han sido detalladas con objeto de dar un punto de vista consistente al presentar la A2RAM, objetivo principal de este trabajo. Esta novedosa celda de memoria basada en el efecto de cuerpo flotante ha sido extensivamente estudiada, primero, mediante simulaciones por ordenador, desde el proceso de fabricación hasta su comportamiento electrostático, y después con medidas experimentales a nivel de dispositivo en diferentes substratos, bulk y SOI.

Algunos de los métodos y técnicas de caracterización más avanzados y ampliamente utilizados hoy día han sido expuestos y posteriormente empleados con éxito en dispositivos de última generación fabricados en el CEA-LETI en Grenoble. Los resultados obtenidos han servido como marco de referencia a la hora de caracterizar la celda A2RAM y comprobar como los pasos extra de fabricación requeridos para obtener este tipo de memoria, influyen negativamente en su comportamiento como transistor. No obstante, esta degradación en su rendimiento como conmutador queda eclipsada por las extraordinarias propiedades como memoria dinámica. Se ha mostrado como el concepto de funcionamiento de la A2RAM concuerda, primero con el concepto teórico, después con las simulaciones llevadas a cabo y finalmente también con los resultados experimentales extraídos. Resultados que permiten hacerse una idea del excelente potencial que esta celda de memoria presenta, aportando argumentos sólidos para considerarla como una candidata firme como memoria RAM dinámica, especialmente para aplicaciones embebidas.

List Of Publications

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developments of A2RAM memory cells on SOI and bulk substrates", submitted to *IEEE Transactions on Electron Devices*.

Conference Contributions

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