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3D-TCAD benchmark of two-gate dual-doped Reconfigurable FETs on FDSOI28 technology☆

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ABSTRACT

Through 3D-TCAD simulations this work aims to demonstrate the benefits of Reconfigurable FETs based on dual doping with respect to the Schottky junctions counterparts using the 28 nm FDSOI platform. These devices feature both N and P dopant species at source and drain to allow for electron and hole symmetrical currents instead of using mid-gap metallic regions. Quasi-static results reveals much larger currents thanks to the enhanced carrier injection with analogous capacitances, leading to faster logic circuits in mixed-mode simulations. Dynamic results also show lower energy-delay products making these devices more efficient and appealing to implement reprogrammable logic.

1. Introduction

The transition to future fabrication nodes is based on the use of pricey technologies such as high-NA (Numerical Aperture) EUV (Extreme UltraViolet) [1,2] or MP (Multi-Patterning) [3,4] lithographies, 3D packaging [5,6], and innovative signal routing schemes [7–9] among other solutions. Together with the semiconductor Integrated Circuit (IC) shortage, all these additional steps and complex processes elevate the fabrication costs, hence saving wafer area to limit the IC value is more important than ever. To do so, the traditional approach has been the device downscaling [10]. However, there is also another solution based on reducing the number of devices within the IC. The former is the dominant path but the latter is gaining momentum as reprogrammable circuits are being investigated. Its fundamental principle is to improve the circuit footprint efficiency. This can be done by either reducing the number of devices for a given functionality or taking advantage of the reconfigurability to build different non-essential functions with a single circuit. This would avoid the need to fabricate two circuits reducing the required design surface. Depending on the application, the circuit would adapt its logic according to the current needs. Any of these solutions can be achieved using Reconfigurable Field-Effect Transistors (FETs), i.e., devices that can operate as N- or P-FETs depending upon the biasing conditions [11]. A full review of these devices can be found in [12]. From the beginning, these devices have been investigated using Schottky barriers (SB) at source and drain (S/D) to allow for the bipolar behaviour. Nevertheless, a new approach has been recently launched based on typical CMOS-like source/drain doping rather than on silicidation [13]. These unique devices, known as Dual Doped (DD) RFETs, aim to solve most of the challenges that SB-RFETs present [14], with especial attention to the reduced output current. This work benchmarks this innovative perspective for a two top-gates architecture [15] on 28 nm FDSOI technology. The second Section of the manuscript explains the basics of these devices highlighting the differences with traditional SB-RFETs. Section three presents the models and parameters accounted for during the numerical simulations. The next two Sections, 4 and 5, analyse the static and dynamic operations, respectively, comparing the results with reference SB-RFETs and regular MOSFETs. Finally, some aspects about the feasibility of these devices and the main conclusions are drawn.

2. Fundamental structure & operation

Conventional MOSFETs feature two different flavours according to the S/D dopant species used during the fabrication process. If the dopant is Boron, the device is P-type (Fig. 1a) and the current consists of holes flowing, whilst if the dopant is Phosphorus or Arsenic, the FET is N-type (Fig. 1b) and the charge carriers are electrons. Regardless of the MOSFET polarity, only majority carrier at S/D can flow across the channel and contribute to the current. The carrier injection in MOSFETs

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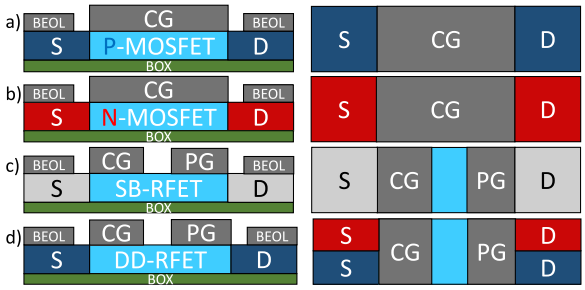

Fig. 1. Front (left) and top (right, no BEOLs represented) views of (a) P- and (b) N-type MOSFETs, (c) Schottky Barrier (SB) and (d) Dual doped (DD) Reconfigurable FETs. RFETs feature two top gates, the typical control gate (CG) and the polarity gate (PG) to select the device polarity. DD-RFETs share their lateral S/D terminals between the N and P doping.

is not restricted as long as the S/D lateral terminals feature a very high doping concentration. This makes the energy barrier of the Schottky contact, that appears between the junction formed by the metallic BEOL contact and the S/D semiconductor, extremely thin, Fig. 2a, b, ensuring an unimpeded injection of carriers through field-emission and behaving as an ohmic contact [16]. On the other hand, reconfigurable FETs must be able to behave as N- or P-type FETs depending on the biasing conditions, i.e., they must drive both electrons and holes in the same device although not at the same time. To achieve this, the lateral S/D terminals are typically transformed into metallic regions through a silicidation process, Fig. 1c. In these devices, the carrier injection takes place between the junction formed by the metallic S/D and the body but, in contrast with typical MOSFETs, the body doping is limited making the Schottky barrier very thick, Fig. 2c, and degrading the field-effect injection efficiency. Instead of field-emission, carriers need now to surmount the energy barrier and be injected through thermionic-field emission. Unless the S/D workfunction is close to the conduction (valence) band as in SB-MOSFETs [17], electrons (holes) will be mostly blocked degrading the output current. Since one of the RFET's goals is to yield symmetric N/P currents and this is achieved by setting the S/D workfunction close to the mid energy band-gap, the workfunction tuning is not possible and the driven current is dramatically hindered.

Dual Doped RFETs (Fig. 1d) use a mix of the previous two concepts: The structure resembles that of an RFET device but the injection mechanism is analogous to the one commented for MOSFETs, allowing for larger injection efficiencies, and thus, improved current flows. To do so, instead of using metallic S/D, the lateral terminals present both donor and acceptor doping profiles as a parallel combination of a N- and P-type transistors. Such device would feature a large ambipolar issue as any gate bias, positive or negative, will drive current with a mediocre OFF level. In order to improve the switching sharpness, one or more additional gates, known as Polarity Gates (PG), are included in the device. Their role is to supress the ambipolar current and select the desired polarity, i.e. the dominant carrier, of the RFET. Meanwhile, the remaining gate, named Control Gate (CG), is in charge of controlling the turning ON and OFF of the device as in a regular MOSFET.

Although RFETs have been studied in different configurations with one or more PGs [11,18] and in distinct technologies (planar SOI [19], trigate SOI [20] or nanowires [11] for example), in this work only the double gate (one CG and one PG) is considered on a planar FDSOI platform [15].

3. Simulation setup

All devices were built using Synopsys TCAD tool [21] to conduct the numerical simulations. Due to the dual doping profile at S/D in DD-RFETs, devices had to be designed in 3D (Fig. 1d). Main accounted models and parameters were: Poisson, electron/hole continuity equations and quantum confinement correction through density

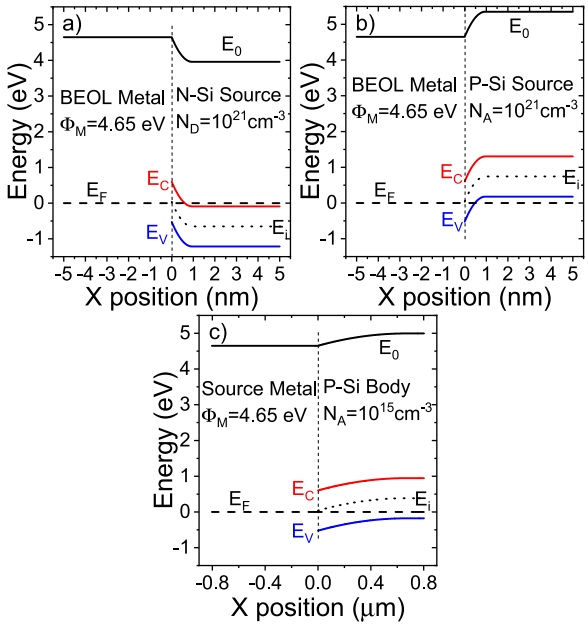

Fig. 2. Simplified energy band diagram for different metal–semiconductor Schottky junctions. Midgap BEOL metal in contact with a highly (a) N- and (b) P-doped Silicon source regions as found in MOSFETs and DD-RFET (field-emission injection). Thin energy barriers allow contacts to behave as ohmic. (c) Midgap source metal in contact with a low-doped Silicon body as in SB-RFET (thermionic emission). The thick barrier prevents any field-emission, restricting the carrier injection. The reference energy coincides with the metal Fermi level.

gradient [22,23]. Simulations were set at room temperature (300 K). Mobility was established based on experimental FDSOI28 results [24] for a given source–drain ($L_{S/D}$) distance (at 145 nm: μ_n = 246 cm^2/Vs and μ_p = 68 cm^2/Vs). All devices feature control and polarity gates with 4.7 eV metal workfunction and P-type polysilicon doping. Their length is fixed to 28 nm for RFETs (CG and PG) and to $L_{S/D}$ for MOSFETs. The RFETs control and polarity gate pitch is set to 120 nm to comply with the technology restrictions. The available FDSOI back-gate was achieved thanks to a highly-doped N-type ground-plane. The buried-oxide is 25 nm thick with a 7 nm SOI film and 1.5 nm as top insulator EOT. In case of Schottky barrier RFETs, the lateral terminals are metallic regions with a workfunction of 4.65 eV emulating Ni silicides. This workfunction, close to mid bandgap, allows to achieve symmetrical output currents for N and P devices. The tunnelling masses are fixed to optimistic values, with $m_n^* = 0.16$ m$_0$ and $m_p^* = 0.19$ m$_0$ (lighter than in previous works [14]). More conservative (heavier) masses would reinforce the message of the manuscript as the SB-RFETs would feature even lower currents and performance in this work. Regular MOSFETs and DD-RFETs have source and drain terminals with concentrations of 10^{21} cm^{-3} instead. These profiles extend along the whole width, W = 200 nm by default, but for dual-doped RFETs where both the N and P doping profile are present at the same time (with W_N and $W - W_N$ widths, respectively). Analogous results can be expected for different geometries. However, smaller devices would face additional fabrication challenges to accommodate either the doping profiles in narrow devices or the two gates in shorter RFETs.

4. Quasi-static operation

Static $I_D(V_{CG})$ curves are illustrated in Fig. 3 for both the N and P branches. The width (dual doped) and workfunctions (Schottky barrier) were selected to provide symmetrical current curves in case of reconfigurable FETs (commented later). The first important aspect to notice is that DD-RFETs in Fig. 3a exhibit the expected transistor shape curve for both polarities validating the structure as a

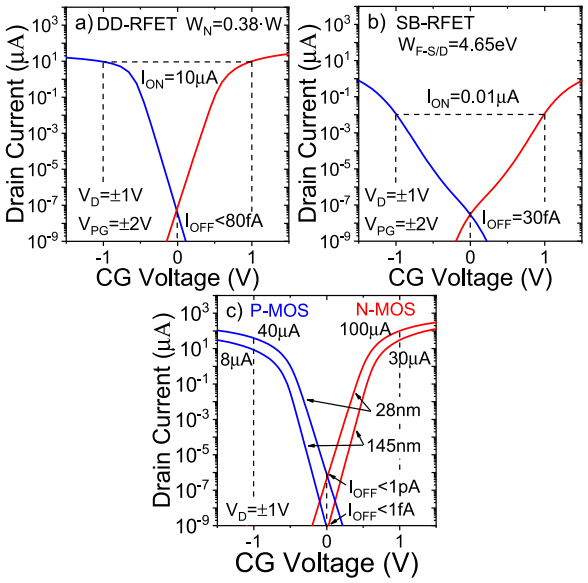

Fig. 3. $I_D(V_{CG})$ comparison for (a) Dual-Doped RFETs, (b) Schottky–Barrier RFETs at $L_{S/D}$ = 145 nm and (c) regular MOSFETs with 28 nm and 145 nm gate length. $V_{BG} = V_S = 0$ V and $W = 200$ nm.

reprogrammable device. The second key point is that they present a much larger current flow than SB-RFETs, Fig. 3b, with up to three orders of magnitude difference at identical biasing conditions which is in line with previous studies [13]. The DD-RFET current resembles more to traditional MOS devices, Fig. 3c, in terms of subthreshold swing with steeper activations, much closer to the ideal 60 mV/dec than SB-RFETs (around 75 mV/dec rather than 210 mV/dec), but with a slightly deteriorated current density for same lengths due to the degraded channel electrostatic control of the ungated region and limited effective width. Besides, it is worth noting that MOSFETs can still be further downscaled improving, even more, the current and enhancing as well the integration density to levels that DD-RFETs cannot reach.

The RFETs comparison concerning the ON (I_D at V_{CG} = 1 V) and OFF (I_D at V_{CG} = 0 V) currents is represented in Fig. 4 as a function of the polarity gate voltage V_{PG}. As RFETs are not expected to change their polarity as often as they switch ON and OFF, if the technology withstands larger electric fields, the V_{PG} can be increased to boost the device performance without having to drive and charge the associated PG capacitance. Note in the figure that a minimum polarity voltage of around ±1 V is required to obtain different ON/OFF current levels. This requisite arises as a consequence of the ambipolar current that steadily rises the OFF current, rendering the device unusable, rather than to a loss of electrostatic control below the polarity gate itself. Once this condition is satisfied, the main difference is again the strong current gap between the two types of reprogrammable transistors. Large V_{PG} voltages seem to be more beneficial for the DD-RFET with no visible trace of saturation, in contrast with what is observed for Schottky RFETs.

The back-gate (ground plane) impact on the device, a typical FDSOI boosting strategy, is studied in Fig. 5. The idea is to use positive (negative) back-gate voltages to allow for larger N (P) currents due to the back-channel activation or the volume inversion regime [25], depending on the applied biases and SOI thickness. This characteristics comes at the expense of a larger OFF current degrading the power saving. Fig. 5a shows that back-gate biasing can improve the driven ON currents by one order of magnitude in case of DD-RFET. However, it is not as effective for Schottky RFETs, Fig. 5b, which suggest that the current flow is saturated due to the carrier injection mechanism.

The ON drain current is now monitored in Fig. 6 with respect to the parameters defining the N/P flavour current symmetry: the N-type

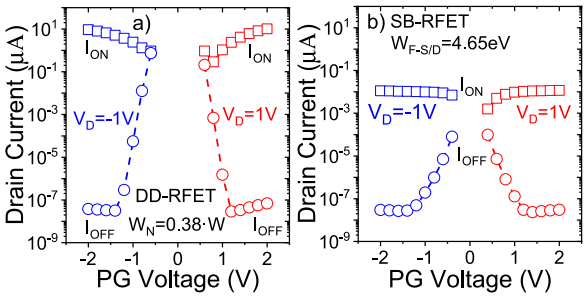

Fig. 4. ON and OFF currents for (a) DD-RFETs and (b) SB-RFETs as a function of the polarity gate voltage (V_{PG}). $I_{ON} = I_D(V_{CG} = \pm 1$ V). $I_{OFF} = I_D(V_{CG} = 0$ V). $V_{BG} = V_S = 0$ V and $W = 200$ nm.

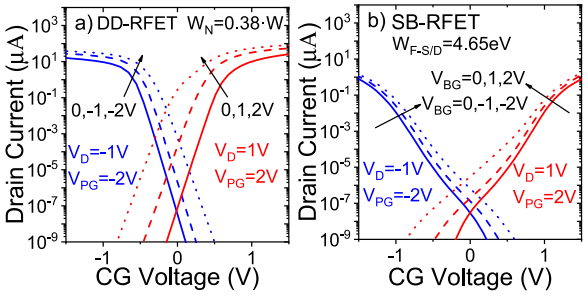

Fig. 5. $I_D(V_{CG})$ comparison at distinct ground-plane voltages (V_{BG}) for (a) DD- and (b) SB-RFETS. $V_S = 0$ V and $W = 200$ nm.

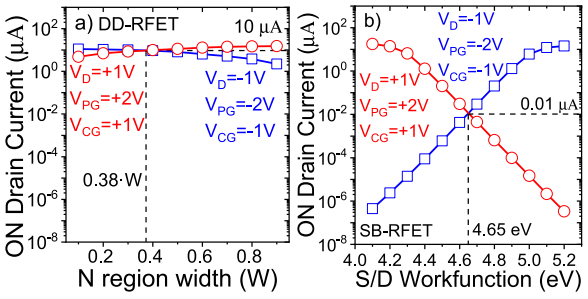

Fig. 6. ON current levels as a function of the (a) N-type doping region width for DD-RFETs and (b) the S/D metal workfunction for SB-RFETs. $V_{BG} = V_S = 0$ V and $W = 200$ nm.

doping width, W_N (equivalently the P-type doping as $W_P = W - W_N$), in case of DD-RFETs; and the S/D metal workfunction, $\Phi_{S/D}$, for SB-RFETs. Results demonstrate that the ON current is much less sensitive, limited slope, to the width definition than to the lateral terminals workfunction. It can be seen that a sufficiently low (or high) workfunction in SB-RFETs yields analogous, or even larger, N (P) current levels than DD-RFETs. The problem is that the device operation is unbalanced and the current symmetry is completely lost jeopardizing the interest for reprogrammable logic. Fig. 6 also highlights the impact that variability might have while seeking the current symmetry: it is harder to achieve it in SB-RFETs if the process, i.e. the workfunction alignment, is not perfectly controlled.

Finally, the control gate capacitance is extracted from quasi-static simulations for the two reprogrammable devices, Fig. 7. Both RFETs exhibit the typical inversion–depletion–accumulation regimes, expected from devices with electron and holes reservoirs like gated PIN diodes [26,27]. The maximum capacitance is essentially the same as both devices share the same structure. The small misalignment may come from deviations in the DD-RFET Gaussian doping profile and the SB-RFET metallic region extensions within the device under the control

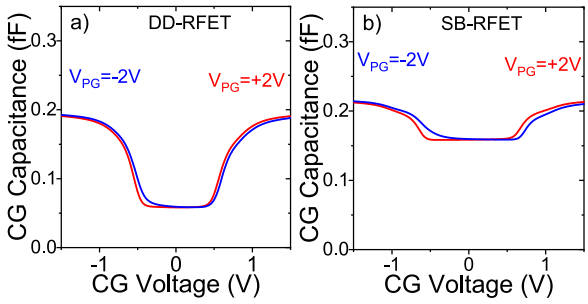

Fig. 7. Static control gate (CG) capacitances for (a) DD- and (b) SB-RFETs. $V_{BG} = V_D = V_S = 0$ V and $W = 200$ nm.

and polarity gates. Concerning the depletion minima difference around zero gate voltage, it reflects the carrier population difference when no control gate voltage is present. Note that the polarity gate voltage is not zero and allows for carrier injection from the drain lateral terminal towards the body.

5. Dynamic operation: Mixed-mode simulations

The dynamic results are extracted in this section using mixed-mode simulations [21] to build simple CMOS logic inverters. A capacitor of only 0.3fF is accounted at the output to model the wiring capacitances. This is a rather optimistic scenario as this capacitance is not enough to model any fan-in capacitance from a following stage in any logic circuit. The selected operation frequency is fixed to 50 Mhz and different supply voltages are accounted, from $V_{DD} = 0.5$ V to $V_{DD} = 2.0$ V. Fig. 8a shows the dynamic transient operation for two of these supply voltages, 1.2 V and 2.0 V. The inverter output voltages for all previous devices are shown separately in Fig. 8b–d. Observe that, at $V_{DD} = 2.0$ V, all devices present the expected switching operation inversely following the input. Only the SB-RFET struggles a bit to follow in time the input signal. As the supply voltage is lowered, all delays increase but this is not really noticeable for MOSFETs nor for DD-RFETs. In contrast, SB-RFETs do not have enough time to reach the maximum (1.2 V in this case) and minimum (0 V) limits and barely operates as a logic inverter. The reason of this malfunction is the very limited output current that SB-RFETs drive due to the poor carrier injection mechanism as a result of the mid-gap S/D workfunction.

From the previous inverter transient responses, the propagation delay can be evaluated as the time shift between the input and output at 50% of the supply voltage V_{DD}. This is performed for both the rising τ_r and falling τ_f edges and then averaged. The delay is represented in Fig. 9a. It is straightforward to relate the average propagation delay with the output current. FDSOI devices present the lowest delay as their output current exceeds the current of any RFET. Concerning RFETs, Dual doped have a much lower delay than Schottky ones thanks to their enhanced carrier injection mechanism. In all cases, as the supply voltage rises, the current increases and the delay is reduced as expected.

The propagation can be also related to the total inverter load capacitance C_L through the following expression [28]:

$$\tau_p = \frac{\tau_r + \tau_f}{2} = \log(2) \cdot R_L \cdot C_L \tag{1}$$

where R_L stands for the equivalent load resistance. This parameter is approximated with the channel resistance using the Ohm's law ($R_L \simeq V_{DS}/I_{DS}$ with the current extracted from Fig. 3 at $V_{CG} = 1.2$ V). The obtained capacitances are summarized in Table 1.

Note the similar capacitances between both RFETs as their structure coincides and that their load capacitance is approximately half the MOSFETs one due to the shorter gates on top of the SOI layer. The extracted value is in the same order of magnitude of the results from

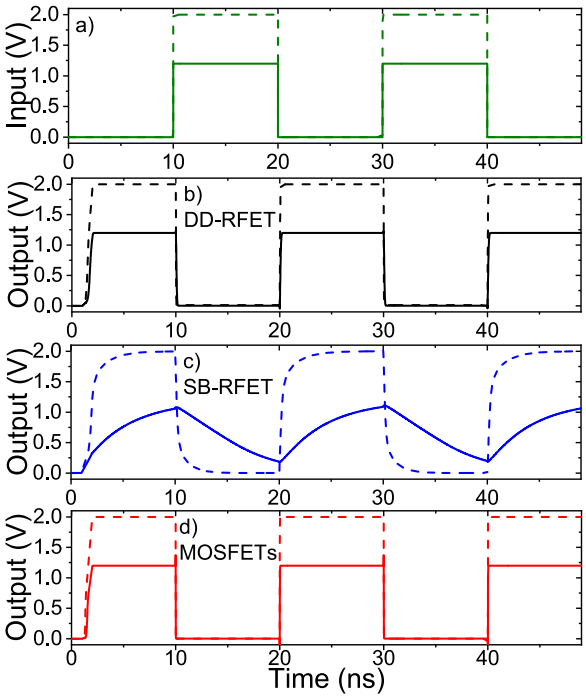

Fig. 8. Transient mixed-mode simulation examples of inverters for $V_{DD} = 1.2$ V and $V_{DD} = 2.0$ V at 50 MHz. (a) Input voltage. Output voltage results for (b) DD-RFET, (c) SB-RFET and (d) MOSFETs ($L_G = 145$ nm). An output capacitance of 0.3 fF is considered to model some wiring capacitances. In case of RFETs the pull-up top device is biased with $V_{PG} = 0$ whilst the pull-down bottom device uses $V_{PG} = V_{DD}$ V. $L_{S/D} = 145$ nm, $V_{BG} = V_S = 0$ V and $W = 200$ nm.

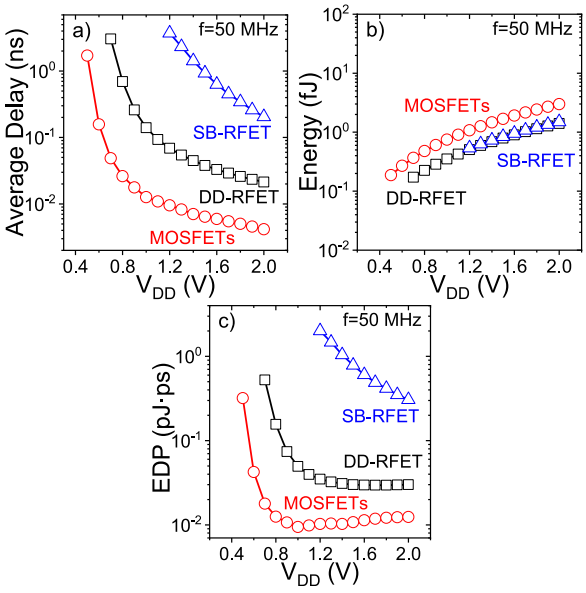

Fig. 9. (a) Average propagation delay (τ_p), (b) Energy (E) and (c) Energy-Delay product (EDP) comparison as a function of the supply voltage at 50 Mhz. $L_{S/D} = 145$ nm, $V_{BG} = V_S = 0$ V and $W = 200$ nm.

Fig. 7, once the output parasitic capacitance of 0.3 fF is accounted. Also C_L is in range with similar values from previous works [14]. The average dynamic energy per switch, E, can be then obtained using Eq. (2) [28] and represented as a function of the power supply, Fig. 9b.

$$E = V_{DD}^2 \cdot C_L \tag{2}$$

Table 1
Equivalent capacitances approximated using Eq. (1).

Device	Load capacitance
DD-RFETs	0.352 fF
SB-RFETs	0.374 fF
MOSFETs	0.747 fF

Very similar energies are extracted for RFETs as a result of having comparable output load capacitances. On the other hand, MOSFETs presents slightly larger energys per transition due to the larger capacitance. Note that this would be solved by simply downscaling the MOSFET towards their natural 28 nm gate length. It can be noted as well that the energy can be made arbitrarily low by reducing the supply voltage. From this perspective, the optimum voltage to run the circuit would be the lowest possible that still ensures functionality although this comes at the expense of the delay, Fig. 9a. The energy-delay product (EDP) is a more relevant metric as it takes into account both parameters simultaneously. It can be calculated using Eq. (3) [28].

$$EDP = \tau_p \cdot E = \tau_p \cdot V_{DD}^2 \cdot C_L \tag{3}$$

The representation of the EDP against the supply voltage provides the optimum spot (from a delay-energy point of view) to run the circuit. This spot coincides with the voltage at which the curve presents its minimum, Fig. 9c. On the one hand, the long MOSFET device would work better at around $V_{DD} = 1$ V, while the DD-RFET would at least require 1.5 V that is where the curve reaches the minimum and flattens. From a designer point of view, when the EDP is constant, the selection of the supply voltage would be based on deciding whether it is more critical to have a lower delay (should use larger V_{DD}) or reduce the power consumption (lower V_{DD}). On the other hand, the SB-RFETs do not even show the minimum in the considered range (it would be outside the considered V_{DD} window, above 2.0 V). This comparison demonstrates again the much better characteristics, now in dynamic operation, that DD-RFET features compared with traditional SB-RFETs.

6. Reconfigurable FET challenges

In this section, some aspects about the fabrication and device feasibility will be commented. The main benefit of SB-RFETs is the doping-free design that reduces the expected RDF (*Random-Dopant Fluctuations*) compared to DD-RFETs. However, they present numerous challenges and disadvantages with respect to DD-RFETs regarding their manufacturing. The first obstacle is the precise control of the silicidation, not only to obtain a very accurate workfunction and achieve the N/P current symmetry (for which they have to overcome the Fermi-level pinning issues), but for the lateral extension control into the RFET channel. In contrast, Dual Doped RFETs are defined based on traditional lithography doping masks which are far better controlled (thanks to the experience with MOSFETs), inducing much lower variability and, furthermore, making them compatible with the CMOS process flow. This last perk enables the easier co-integration with other logic circuits. Another advantage of DD-RFETs is that the N/P current balance can be adapted much more easily through mask sets width tuning, enabling for example high-performance and low-power consumption logic within the same design.

In the case of DD-RFET, besides the RDF problem, there is also an important aspects to consider: The achievement of shallow N/P junction profiles at the S/D lateral terminals. The definition of very close distinct carriers reservoirs might not be possible. As a solution, DD-RFET have demonstrated to still being operative when both profiles at S/D are separated without losing performance [13] at the expense of their footprint.

7. Conclusions

Reconfigurable FETs provide an interesting framework to develop future custom in-situ adaptable logic. Nevertheless, the usual RFET based on Schottky barriers is way too far from regular MOSFETs in terms of size, performance and CMOS compatibility. In this work, another RFET solution is proposed that significantly reduces the gap regarding the performance and CMOS compatibility by simply using a dual doping approach at source and drain terminals. 3D simulations demonstrate that this solution is able to operate at lower voltages, drives up to 1000 times more current (even accounting for optimistic SB tunnelling masses) outperforming SB-RFETs, and allows for an optimistic path for on the fly circuit reprogrammability logic.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: The authors report financial support was provided by Spain Ministry of Science and Innovation. The authors have patent Dispositivo FET reconfigurable con dopado dual pending to P202030318.

Data availability

Data will be made available on request.

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