

This Bachelor Thesis is intended to reflect the complex process behind the

Development Process of a product, from the academic perspective. With the purpose of designing an economical receiver for DATV, the system is analyzed

and designed according to the requirements given, following a market-oriented philosophy. As part of the system, a mixer design is proposed. The whole Project is approached as a multidisplinary problem which culminates with a functional BACHELOR THESIS

DATV Receiver System Design and Development



prototype of the System.

José Carlos Martínez Durillo is a telecommunication engineer from Bailén, Spain. He earned his bachelor's degree in 2017 at University of Granada. He started working with GranaSAT Team in 2016, involved in an ADSB Reception System. With this challenging Bachelor Thesis complements his education in others specialities and finalizes his B.E.



Andrés María Roldán Aranda is the academic head of the present project, and the student's tutor. He is professor in the Departament of Electronics and Computers Technologies

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José Carlos Martínez Durillo





### UNIVERSITY OF GRANADA

Bachelor of Telecommunication Technologies Engineering

**Bachelor Thesis** 

### DATV Receiver System Design and Development

José Carlos Martínez Durillo 2016/2017

Tutor: Andrés María Roldán Aranda



#### BACHELOR OF TELECOMMUNICATION TECHNOLOGIES ENGINEERING

#### **Bachelor** Thesis

# "DATV Receiver System Design and Development"

ACADEMIC COURSE: 2016/2017

José Carlos Martínez Durillo



BACHELOR OF TELECOMMUNICATION TECHNOLOGIES ENGINEERING

# $"DATV \ Receiver \ System \ Design \ and \\ Development"$

AUTHOR:

José Carlos Martínez Durillo

SUPERVISED BY:

Andrés María Roldán Aranda

DEPARTMENT:

**Electronics and Computers Technologies** 

D. Andrés María Roldán Aranda, Profesor del departamento de Electrónica y Tecnología de los Computadores de la Universidad de Granada, como director del Trabajo Fin de Grado de D. José Carlos Martínez Durillo,

Informa:

Que el presente trabajo, titulado:

#### "DATV Receiver System Design and Development"

ha sido realizado y redactado por el mencionado alumno bajo mi dirección, y con esta fecha autorizo a su presentación.

Granada, a 12 de Septiembre de 2017

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Autrestolda

Fdo. José Carlos Martínez Durillo

Fdo. Andrés María Roldán Aranda

### Diseño y desarrollo de un sistema receptor para DATV José Carlos Martínez Durillo

#### PALABRAS CLAVE:

ADS<sup>®</sup>, Altium Designer<sup>®</sup> 16, Antena, CST<sup>®</sup>, DATV, EDA, Electrónica, Microstrip Technology, Diseño de PCB, MATLAB<sup>®</sup>, Mezclador, S-Band.

#### **RESUMEN:**

El objetivo principal del presente Proyecto es desarrollar un producto en forma de sistema completo de recepción de la señal de DATV, transmitida desde la ISS. Para ello se estudiará el radioenlace de forma integral, desde el sistema de transmisión hasta la Ground Station. Desde el primer momento, este Proyecto persigue una metodología orientada a producto y a mercado. Toda decisión concerniente al desarrollo será tomada no sólo en base a criterios técnicos y de ingeniería, sino también atendiendo al coste. Todo ello emerge a partir de los requisitos funcionales que se desprenderían de un hipótetico cliente. De ellos derivan los requisitos técnicos necesarios para cumplir con los primeros. El siguiente paso será un proceso de análisis y estudio del sistema, durante el cual se aprovechará para introducir conceptos teóricos claves para el posterior diseño. En el proceso de diseño ha sido usual la realización de comparativas entre las diferentes opciones del mercado, de manera fidedigna a como se haría en un proyecto profesional real.

Este Proyecto se presenta como Trabajo Fin de Grado de la titulación de Grado en Ingeniería de Tecnologías de Telecomunicación de la Universidad de Granada. A pesar de que durante la titulación se realiza una diferenciación en especialidades, se ha tratado de enfocar el proyecto de forma multidisciplinar, acercando al alumno a las especialidades no cursadas.

Con el fin de preservar el carácter académico del Proyecto, durante el mismo se ha hecho uso intensivo de herramientas no utilizadas durante la titulación, pero de importancia capital en la industria. Del mismo modo, también se han analizado y aplicado técnicas avanzadas de prototipado de PCB, como el fresado de sustratos de doble cara mediante control numérico, comparándose el resultado obtenido con el que se puede obtener mediante un proceso atacado químico.

El resultado de todo lo expuesto culmina con la obtención de un sistema completo, que cumple con los requisitos funcionales y necesidades indicadas en la primera fase y con el cual se cierra la etapa universitaria de Grado.

### DATV Receiver System Design and Development José Carlos Martínez Durillo

#### **KEYWORDS**:

ADS<sup>®</sup>, Altium Designer<sup>®</sup> 16, Antenna, CST<sup>®</sup>, DATV, EDA, Electronics, Microstrip Technology, PCB Design, MATLAB<sup>®</sup>, Radio-link, Mixer, S-Band.

#### **ABSTRACT:**

The main purpose of this Project is developing a product consisting of a complete reception system for DATV signal transmitted from the ISS. To accomplish it, the radio-link will be studied in a comprehensive way, from the transmission system to the Ground Station.

Since the first moment, this Project pursuits a product&market-oriented philosophy. Every decision concerning the development will be taken not only according to technical and engineering criteria, but also pricing and market. The whole emerges from the Functional Requirements which would be given by an hypothetical client. Technical requirements needed are derived from the previous. Then, it will be started an analysis process of the system, in which theoretical concepts, key for the later design, will be included. At the design process, comparatives among the possibilities of the market are often included, as it would be made in a real professional project.

This Project is presented as Bachelor Thesis within the Bachelor of Telecommunications Technologies Engineering of the University of Granada. Despite the specialities differentiation made during the degree, this Project has been focused from a multidisciplinary perspective, getting the student closer to the specialities not taken.

Trying to preserve the academic character of the Project, an extensive use of unused tools during the degree, but crucial at industry, has been made. In the same way, advanced prototyping techniques have been analyzed and used, such as milling substrate using Computer Numeric Control. Then, the result is compared with the one obtained through series manufacturing process.

The result of the exposed culminates obtaining a complete system, which complies with the Functional Requirements and needs indicated at the beginning, and which supposes the finalization of the Degree.

When people ask you '-What do you do?' Answer '-Whatever it takes'

### Agradecimientos:

Durante el desarrollo de este Proyecto, me ha sido necesario interactuar con una ingente cantidad de personas. Con un número muy reducido de ellas lo he hecho en persona, mientras que una mayoría estaban entre las páginas de libros, manuales y sitios web.

Mientras que estas últimas han obtenido su reconocimiento a través de sendas referencias, las primeras merecen un reconocimiento especial que tengo el placer de brindarles en estas líneas. El primero de ellos ha de ir destinado a mi familia, mis padres, José y Amparo, y mi hermano Francisco Javier. Desde siempre, su apoyo incondicional en todos los aspectos ha resultado de importancia capital para que toda empresa acometida llegara a buen puerto. El apoyo mostrado durante el periodo de desarrollo de este Proyecto no ha sido sino una muestra más del mismo.

Sería injusto no acordarme de mis compañeros de fatigas técnicas. Pocas, pero auténticas amistadas se forjaron al inicio esta carrera de fondo, habiendo perdurado en el tiempo, como sin duda lo harán para siempre, junto a las que ya existían. A los compañeros y amigos de laboratorio, por hacer más amena la tarea diaria, especialmente a Pablo, siempre dispuesto a ayudar en cuanto pueda.

Desde la perspectiva técnica, este Trabajo Fin de Grado no habría visto la luz sin la colaboración y supervisión de mi tutor, Andrés Roldán Aranda. Su encomiable afán de mejora, capacidad de trabajo y conocimiento obligan a responder con un nivel de trabajo de la misma magnitud. La búsqueda de la excelencia es la única manera de poder, algún día, soñar con alcanzarla.

Y, por último, no en orden de relevancia, sino con espacio propio, a Natalia, por aparecer al principio de esta aventura y permanecer aquí mientras escribo estas líneas, soportando cada tarde mis frustraciones técnicas y ofreciéndome un apoyo incondicional que facilita cualquier tarea. Su esfuerzo y dedicación personal son el espejo en el que mirarme cuando las fuerzas flaquean.

Cada uno de los mencionados son partícipes de este Trabajo. A todos ellos, y a los que no pudieron verlo, muchas gracias.

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During the realization of this Project, I had the need to interact with an enormous amount of people. With a reduced number of whom I did it personally, whereas the majority of them were in pages of books, manuals and websites.

While the latter have been recognized through references, the first ones deserve special recognition, which I have the pleasure to afford them in these lines. The first of them must be for my family, my parents, José and Amparo, and my brother Francisco Javier. Ever since I can remember, its unconditional support in every aspect has been of primary importance so every of my undertaking come to fruition. The support provided during this Project has been only a proof more.

It would be unfair forget my comrades in arms. Not many, but authentic friendships forged at the beginning of this stage, which have persisted through time, as they undoubtedly will do forever, along with the already existent ones.

From a technical perspective, this Bachelor Thesis would not have been released without the collaboration and supervision of my tutor, Andrés Roldán Aranda. His praiseworthy desire to improve and vast knowledge obliged me to answer with a level of work of the same magnitude. Pursuiting for excellence is the only way to be able to, someday, dream with reaching it.

And finally, not in relevance order, but with own space, thanks to Natalia, for appearing at the start of this adventure and staying here while I am writing these lines, tolerating each afternoon my technical frustrations and providing me with an unconditional support which eases every task. Her effort and personal dedication are the mirror to look at when I am losing strength.

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## GLOSSARY

- 1 dB Compression Point Most nonlinear devices, such as mixers or amplifiers, tend to become lossier with increasing input power. At a certain power level, the gain response of the device will become reduced by 1 dB; that point is known as 1 dB compression point and it is expressed as a function of input or output power depending on the device.
- Altium Designer<sup>®</sup> 16 EDA software used to design PCB from schematics. It allows 3D Design, as well as electronics simulation.
- **Axial Ratio** Ratio of the orthogonal components of an E-field. For circularly polarized antennas, ideal value is 0 dB. In case of linear polarization, it tends to infinite.
- **Baseband** Signal whose spectral magnitude is non-zero only in the nearby of the origin of frequencies and negligible elsewhere.
- **Bias-Tee** Three-Port Network widely used to set the DC bias point in electronics devices, such as mixers or amplifiers.
- Border Outline In a PCB, said of the boundary or extents of the board.
- **Broadside** Regarding radiation pattern, an antenna is said to be working at broadside direction when the maximum radiation direction is transversal to the axis.
- Cubesat Miniaturized satellite normally for space research, with dimensions of  $1 \,\mathrm{dm^3}$  and mass lower than 1.33 kg per unit.

- - **DATV** Also known as Digital Amateur TeleVision, it allows transmitting video signals with less bandwidth in comparison with others transmission schemes. It applies DVB-S system, which is widely used in Europe.
  - **Differential Impedance** Said of the ratio derived from the change in voltage between two ports and the change in current.
  - **Directivity** Regarding antenna parameters, it measures the power density radiated in the direction of the strongest emission, when compared with the power density radiated by an ideal Isotropic radiator radiating the same power.
  - **Dispersive** Regarding a material, and normally referred to frequency, it implies variations of its behaviour along with frequency.
  - **Dropout Voltage** Regarding voltage regulators, minimum voltage drop required across the regulator to maintain output voltage.
  - Effective Area Ratio between received power and incident power density at the receiving antenna.
  - **Far Field** Regarding Antenna Propagation, region of the electromagnetic field which occurs at enough distance from the antenna and in where the radiation pattern does not change with distance.
  - Faraday Rotation In satellite radio-links, phenomena due to Earth's Magnetic Field which implies a certain rotation when a linear polarized signal goes through ionosphere. Negligible above 10 GHz.
  - **GranaSAT** GranaSAT is an academic project from the University of Granada consisting in designing and developing a picosatellite (Cubesat). Coordinated by the Professor Andrés María Roldán Aranda, GranaSAT is a multidisciplinary project with students from different degrees, where they can acquire and enlarge the knowledge necessary to face an actual aerospace project.
  - Ground Station Facilities in which instruments and devices necessary to establish a radio link communication are normally located. Also used to control and monitor antenna system.
  - Ground Bouncing Phenomena which occurs when there is an inductance from the ground pin on an Integrated Circuit to a common ground for the system. IC switching provokes the current to flow through this inductance and makes the ground reference of the IC become higher than the global ground reference.
  - Guided transmission medium Said of the transmission medium in which waves are guided along a solid medium, unlike to unguided mediums. Transmission lines are an example of these.

- **Insertion Losses** Loss of signal power as a consequence of going into a transmission line or optical fiber. Usually measured in dB.
- **Isotropic** Regarding antennas, it is an ideal type of those which radiate< the same intensity of radiation in all directions. It is not physically feasible.
- **Keysight Genesys RF<sup>®</sup>** RF and microwave EDA software for circuit synthesis and simulation, from filters to transmission lines or PLL.
- **Microstrip Technology** Planar transmission line in which a conductor of width W is printed on a thin, grounded dielectric substrate of thickness d and Relative Permittivity  $\epsilon_r$ .
- MPEG-4/H.264 Video compression standard format, one of the most used for recording and distribution of video content. It is actually composed of a group of standards, with different profiles.
- **Noise Floor** Measure of the signal created from the sum of all undesired signals and noise sources within a measurement system.
- **PLF** Polarization Losses Factor. They occur when receiving and transmitting antennas are not equally polarized, or their polarizations are not of high quality. Depending on the type of mismatching, the amount of losses will vary.
- Quasi-TEM Mode Normally referenced when using Microstrip Technology, name given to the phenomena which occurs in that technology, where two different mediums (substrate and air), coexist. It differs from the TEM, among others things, in the propagation constant, which depends on Relative Permittivity.
- **Radio-Link Budget** In a **RF** design, accounting of the gains and losses which occur through the system, i.e., transmitter, medium and receiver.
- **Reflection Losses** They occur on a medium when part of the energy is reflected back to the emitter. It may happen in different mediums, e.g., a transmission line.
- **Relative Permittivity** Regarding a material, said of its permittivity expressed as a ratio relative to permittivity of vacuum.
- **S-Band** Official designation given by the IEEE to a part of the microwave band of electromagnetic spectrum. It covers the range from 2 GHz to 4 GHz. It is widely used by radars, satellite radio-links and also for the ISM band.
- **Selectivity** Measure of the performance of a receiver to receive only the radio signal for which it has been tuned, rejecting others signals nearby in frequency.
- SolidWorks<sup>®</sup> CAD Software from Dessault Systèmes for 3D Mechanical Design.

per second.

- **Symbol Rate** Also known as baud rate, it refers to the number of symbols or waveform changes per time unit, across a transmission medium. It is measured in baud or symbols
  - **Varactor** Also known as **varicap**, it is a type of variable diode, depending on capacitance. It is usually used as voltage-controlled capacitor.

# ACRONYMS

**ADC** Analog to Digital Converter.

 $\mathbf{ADS}^{\textcircled{B}}$  Advanced Design System.

 $\label{eq:added} \textbf{ADSB} \ \ \mbox{Automatic Dependent Surveillance} - \ \mbox{Broadcast}.$ 

AGC Automatic Gain Control.

**AMSAT** AMateur SATélite.

 ${\bf ARISS}\,$  Amateur Radio on the International Space Station.

**BOM** Bill of materials.

 $\mathbf{CST}^{\circledast}$  Computer Simulation Technology.

**DVB-S** Digital Video Broadcasting by Satellite.

**EDA** Electronic Desing Automation.

**EIRP** Equivalent Isotropic Radiated Power.

 ${\bf EMC}\,$  ElectroMagnetic Compatibility.

 ${\bf FEC}\,$  Forward Error Correction.

**FR4** Fire Retardant 4.

GPIB General Purpose Interface Bus. I2C Inter-Integrated Circuit. **IEEE** Institute of Electrical and Electronics Engineers. **ISM** Industrial, Scientific and Medical (Radio-bands). **ISS** International Space Station. LDO Low Drop-Out. **LED** Light-Emitting Diode. LHCP Left-Handed Circular Polarization. LNA Low-Noise Amplifier. LNB Low-Noise Blocker. LNC Low-Noise Converter. LO Local Oscilator. MATLAB<sup>®</sup> MATrix LABoratory. **MPEG** Moving Picture Experts Group. **NIM** Network Interface Module. **PCB** Printed Circuit Board. **PCI** Peripheral Component Interconnect. pHEMT pseudomorphic High Electron Mobility Transistor. **PLL** Phase-Locked loop. **QPSK** Quadrature Phase-Shit Keying. **RF** Radio Frequency. **RHCP** Right-Handed Circular Polarization. **SMA** SubMiniature version A. **SMD** Surface Mount Devices. **SMT** Surface Mount Technology.

- ${\bf THT}\,$  Through-Hole Technology.
- **URE** Unión de Radioaficionados Españoles.
- ${\bf USB}\,$  Universal Serial Bus.
- $\mathbf{VCO}$  Voltage-Controlled Oscilator.
- $\mathbf{VNA}\xspace$  Vector Network Analyzer.
- ${\bf VSWR}\,$  Voltage Standing Wave Ratio.

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# CHAPTER

# INTRODUCTION

This Bachelor Thesis is presented as a compilation of the knowledge acquired throughout the years of the degree and specially, during the Project period. It aims to reflect the engineering process behind the design, development and prototyping stage of a product. Particularly, the main purpose of the project is developing a receiver to receive DATV signal from the ISS.

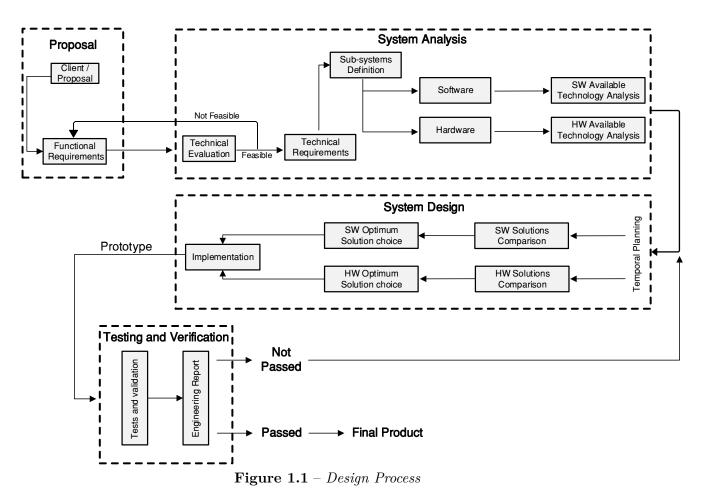
The final result is expected to be a fully-integrated design with capability to be directly connected to a PC, as well as a signal conditioning block, if necessary. In order to achieve said objective, the system will be studied from different points of view, from the existent radio - link in which the transmission is made, to the needs that the electronics have to comply, or the software necessary to process the signal. When finished, the system will allow to receive everywhere, with a portable device, DATV signal, showing not only the video but also technical information about the signal received.

In brief, the conjunction of both fields of knowledge, electronics and communications technology will allow to develop a potentially marketable product, which solves the problem of adequately receiving this satellite signal.

As it can be deduced from the previous lines, a market-oriented philosophy will be followed in this project, seeking to integrate different technologies by applying an iterative process of designing and improving of the product.

The Product Development Process composed different stages: is of Technical Definition, System Analysis, System Design, Requirements

Verification and Testing. The diagram of the figure 1.1 shows how that process flows since the initial step, which using a Market analogy could be the client proposal, until obtaining the final product. This process follows the planning proposed as a consequence of the Analysis, which can be seen at figure 1.3. Once Verification and Testing stage has been adequately passed, should the product comply with functional and economics requirements, the product and therefore the Project will be finished.



This Bachelor Thesis fits within GranaSAT Project, a multidisciplinary project which gathers people from a variety of fields who are committed to acquire new knowledge related to Electronics and Aerospace Engineering. It is coordinated by the professor Andrés María Roldán Aranda and although it was conceived to build a Cubesat, today its goals goes far beyond, and every type of devices and projects are developed.

José Carlos Martínez Durillo



Figure 1.2 – GranaSAT Logo

# 1.1 Prior art. ARISS Program: Problem Statement

The ARISS Project is an initiative of AMSAT along with amateur radio organizations. It mainly consists in providing live communication between ISS and schools, in order to get student closer to the job performed by astronauts, using the experience as a first approach to aerospace world. It allows students to learn about life on board the ISS and explore Earth from space through scientific activities, in a innovative and interactive way, by exploring amateur radio world. ARISS Project was created and is managed by an international working group, including several countries in Europe as well as Japan, Russia, Canada, and the USA. Since it is international in scope, the team coordinates locally with their respective space agency. In addition, it provides a contingency communications system for NASA and the ISS crew.

Scheduled ARISS contacts with the ISS are conducted either by direct contact, or by telebridge contact. Because the ARISS Project program supports the testing and installation of amateur radio stations aboard the ISS, astronauts have the equipment available to also make unscheduled ham radio contacts with radio amateurs all around the world on a one-to-one basis during their personal time.

The reasoning behind the conception of this Bachelor Thesis is the difficulty, and price, that contacting with the ISS implies for an educational institution as schools. It does exist in the market a number of radio systems of different manufacturers, such as RF HAMDESIGN [30] which allow the communication, but at a high price and including only Receiving Antenna System. Therefore, it is also needed an amplification stage, as well as a receiver. In conjunction, the total amount needed to establish the radio-link is unaffordable for the majority of the schools, which makes them miss this invaluable opportunity.

This Project will seek to develop a fully-integrated receiver with a low-cost oriented philosophy; when finished, it is expected to have a functional prototype available. As it will be analyzed later, there are really few integrated receivers in the market like the one to be designed, and the existent one uses outmoded technology and is expensive.

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# 1.2 Motivation

In my case, there was an special motivation when started this Final Project. My desire of going a step beyond the formal education I had received, as well as making something different to what I was used to, made me choose a Bachelor Thesis not related with my speciality, Telematics Systems. It forced me to change my way of working and learning a vast amount of new concepts and techniques to be able to effectively develop a product, knowledge which will undoubtedly be useful for my future career.

Performing this Bachelor Thesis has made me realize the significant knowledge left to learn when finishing the degree, in my case, in the field of Electronics and Communications Systems. By developing the mentioned system, I have found myself obliged to deal with real issues far from programming, including study of the market, comparison, generation of multiple versions, as well as performing real testing and measuring at laboratory. In sum, all of that makes it possible to offer a solution to a particular problem as in this case.

The product or group of products which emerge from this Bachelor Thesis are the result of a painstaking process of engineering and study and comparison of the technology used to solve the problem. In addition, the possibility to provide schools the opportunity to effectively perform a contact with the ISS and getting them closer to the aerospace and scientific field has been a strong incentive.

# **1.3** Project Goals and Objectives

The main objectives of this Bachelor Thesis are the following:

- Studying and analyzing the needs of a complete signal receiving system over satellite.
- Deducing the main and secondary requirements of the system as well as the subsystems by which it is formed, studying its viability, providing improvement and better possibilities.
- Performing an analysis of the existent technologies in the market which may be used to solve the problem, reasonably choosing the best one for each case.
- Designing and manufacturing a prototype of the receiver, in PCB format.
- Applying an adequate test bench to the prototype, in order to determine the grade of success of the design and functionality of the product.
- Acquiring electronics design knowledge, getting the student closer to a real problem.
- Demonstrate the knowledge acquired during the Degree, not only at the speciality coursed by the student, but also from a general point of view, inside of the Telecommunications Engineering.
- Successfully overcome the subject of the Bachelor Thesis.

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# 1.4 Project Structure

This Project is divided in 5 chapters and an addendum which try to describe not only this project, but also each one of the parts of the design and development process of a product, in a logical and chronological way.

These chapters are:

- **Chapter one**. This chapter, which is intended to serve as introduction and shows the objectives and the reasons for its realisation.
- Chapter two. Requirements of the desired system are exposed from a functional an economic point of view. They must be understood as the requirements of the *client* which have to be correctly interpreted to obtain the **technical requirements** that will lead to the design constraints and needs. On the other hand, a brief search-on-the-market is performed to be able to give a price estimation to the client.
- Chapter three. It deals with analysis and development issues for the first time. It starts analyzing the functional requirements given, from which a very first system block diagram can be obtained. After that, each one of those blocks are subsequently analyzed, deriving in the technical requirements of the system, and how they could be met. In addition, given the vast amount of different concepts which this project will involve, this chapter will be also used to briefly introduce and clarify the most important ones to be able to follow the design process. At the end of this chapter, different technological solutions will have been explored and from that analysis it will surge a Project Timing reflected in a Gantt Chart.
- **Chapter four**. The fourth chapter deals with **system design**. It translates the technological solutions analyzed in the previous chapter to actual devices which are able to execute the tasks required. Usually, different possibilities will be studied and compared, resulting in the optimum choice according to both, engineering and economic factors.
- **Chapter five**. Finally, chapter five includes the main conclusions extracted from the Project, as well as some future lines of work which have naturally emerged during the developing process.
- In addition, an addendum, in which the budget and associated cost of these Project are detailed, is included.

		ember		ober		mber				uary	Feb	ruary	Ma	rch	A	pril	M	ay	Ju	ine	Jı	ıly		just	Septe	ember
	1 <sup>st</sup>	2 <sup>nd</sup>																								
Project Start																										
Documentation Analysis																										
Feasibility Evaluation																										
System Analysis																										
Functional Requirements Definition																										
Technical Requirements Definition																										
Software Subsystem Evaluation																										
Transmission System Evaluation																										
Radio-Link Evaluation and Budget																										
Receiving Antenna Evaluation																										
RF Conditioning Evaluation																										
Signal Reception Evaluation																										
Transmission to PC Evaluation																										
Supply System Evaluation																										
System Design																										
Receiving Antenna Analysis																										
Receiving Antenna Simulation and Measurement																										
PCB Components Analysis & Comparison																										
PCB Design																										
PCB Prototype Manufacturing																										
RF Conditioning Stage Components Comparison																										
MatLab Library Development and Commercial Mixer Analysis																										
Mixer Design																										
Documentation																										
Diagrams and Documentation Compilation																										
Project Narrative Edition																										
Defense Preparation																										

## DATV Receiver System Design and Development

Figure 1.3 – Gantt Chart of the Project

# CHAPTER

2

# SYSTEM REQUIREMENTS DEFINITION

As a first step in every design, it can be defined a set of system requirements, from which the technical requirements of the system will be extracted. In addition, economic requirements will be estimated.

# 2.1 Functional Requirements Definition

Functional requirements reflect what the system is expected to do and how. They are usually given from the client's point of view, so they do not have to be neither excessively technical nor accurate. At the end of the development process, the product is expected to comply with this requirements. According to its importance in the system performance, they can be divided in **Primary** and **Secondary**.

# 2.1.1 Primary

- The system must be able to receive the DATV Downlink signal from the ISS, by using a PCB format device.
- The system must allow connecting to an antenna which permits the reception.
- The system must allow feeding up to the antenna, in case it is necessary DC current

at any point of the system.

• The system must have the possibility of being supplied directly from electrical grid.

# 2.1.2 Secondary

- The system is expected to have an USB interface which allows direct connectivity with a PC, being portable as opposed to the existent PCI solutions.
- The system must be compatible with the existent software solutions.
- The system should include some software solution which allow to watch the video received through the signal. This software will show all the technical information possible about the signal.
- The system should be the smallest size possible.
- The system should consume the smallest amount of power possible.

# 2.2 Economics Requirements Definition

Regarding the economics requirements, this project follows a cost-oriented philosophy, constantly seeking for costs reduction, in order to develop a competitive marketable product. As a consequence, for each functional block of the system, different alternatives will be analyzed, finally choosing the one with the best value for money.

The main product, the PCB receiver, according to the previous analysis, is expected to have a production cost inferior to  $60 \in$ .

# CHAPTER

# 3

# SYSTEM ANALYSIS

In this third chapter, the system will be analyzed progressively reducing the abstraction level. Firstly, technical requirements of the system will be defined, based on the functional requirements given in the previous chapter.

Once technical requirements are specified, analysis will start at the top abstraction level with a Block Diagram showing the structure of the system. Several Blocks, representing Subsystems, will be established in that Diagram, which will be individually analyzed afterwards, in frequency of work decreasing order. Right after that, different technologies will be studied and compared, to develop an optimum solution for each one of the Subsystems. Different devices may be added throughout the analysis when necessary for the functioning of the system. Analysis stage finishes with the comparison of the possible solutions in the System Design, in Chapter 4, following the planning which also emerges from the Analysis.

As it was said before, the first step consists in performing an study of the functional requirements exposed in Chapter 2, in order to define the technical requirements of the system. In this project, the Subsystems can be arranged into two groups: Software and Hardware.

# 3.1 System Technical Requirements

By analyzing the functional requirements given, it can be determined that the main function the product has to be able to perform is **receiving DATV** signal in a portable

way. As a consequence, it must have connectivity possibilities, reduced size and low consumption.

In order to meet those requirements, the system will be composed of the subsystems shown in the figure 3.1.

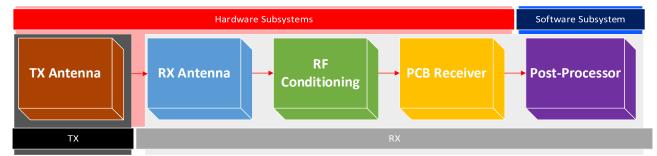


Figure 3.1 – High Level System Block Diagram

From the figure 3.1 it can be seen that the system is susceptible to be clearly separated into the groups commented before:

# • Software Subsystems

Once the signal has been received and adequately treated, it is transmitted to the PC so it can be watched from there. In order to accomplish that, it is necessary the Software Subsystem.

-Post-Processor: It will be the final block of the system. It is in charge of processing the signal received, interpreting and showing it in a functional user interface. It must be compatible with the existent software and in order to be used by the majority of the users it must be run under Microsoft Windows<sup>®</sup>. It also has to be compatible with the hardware used in the system, so the greater hardware compatibility is desired. Free Software would be advisable too.

# • Hardware Subsystems

**-TX Antenna:** In this case, it is the S-Band Transmission System of the ISS. Knowing the transmission system used is crucial in order to design the reception system; for that reason, it will be previously analyzed and taken into account in the design of the whole system.

**-RX Antenna:** Receiving Antenna is the first block of the RX System. Several options, from handmade to commercialized, will be studied in the System Analysis seeking for the optimum one to be finally implemented in the System Design.

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-RF Conditioning: When designing hardware for satellite communications, it is common the need of an stage which prepares and adapts the signal for the following stage. Depending on the system, this stage will have different components or even devices; its need and characteristics will be analyzed.

**-PCB Receiver:** This is the main purpose of this Project. Contrary to the majority of the existent solutions, it is sought a portable solution in PCB Format. PCB Design is a high-complexity matter which will require of deep analysis and multiple iterations until the optimum design is determined.

In this chapter, the system is going to be analyzed following those divisions.

#### 3.1.1 Software Subsystem

Given that the final aim of this Project is getting the video signal from the ISS in a PC, an adequate software solution will be necessary in that end. According to the functional requirements given, this software must be able not only to handle the signal received, but also to show every technical information possible about it, constellation, SNR, power received, etc.

#### 3.1.1.1 Post-Processor

One of the most acclaimed software for this purpose in recent times is **Minitioune**. Minitioune was developed by Jean Pierre F6DZP, primarily to be used with PCI Card Solutions. Several versions later, the possibility of a portable hardware arises and with it, did Minitioune. Every information needed can be found at Viva DATV, the French website in which Jean Pierre states the news regarding his software.

Minitioune constrains the hardware used to receive, to be able to communicate with it adequately. Particularly, it expects to find an USB Interface, as well as specific chips to perform the demodulation in the tuner. These constraints, along with the checking process, will be detailed in Chapter 4. In addition, Microsoft Windows<sup>®</sup> is needed to execute Minitioune.

Figure 3.2 shows the interface of the software, when hardware has not been configured yet. It can be seen that Minitioune exhibits, apart from a video section, several blocks to show received frequency, decodification codecs, AGC, which allows to set the gain of the tuner, and even another to Record the video received. In sum, this software complies with every requirement needed for the system so, from now on, the analysis and design of the system will be undertaken considering the use of this software.

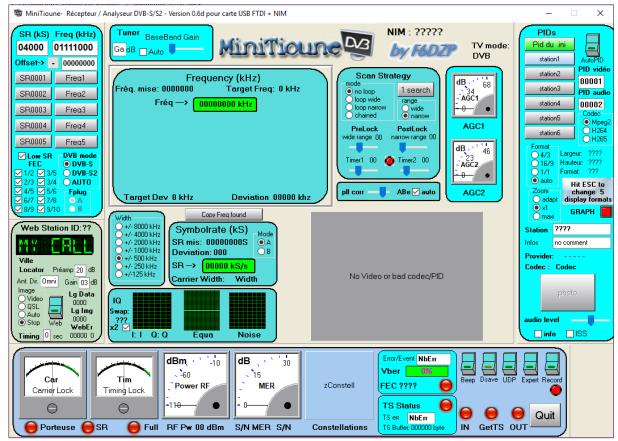


Figure 3.2 – Minitioune v0.6 Interface

# 3.1.2 Hardware

In this section, blocks concerning the hardware part of the System are going to be analyzed. In this case, there will be different possibilities for each one of the subsystems, in contrast to section 3.1.1. Technological solutions will be exposed as a previous step to the design.

# 3.1.2.1 TX Antenna

To determine the characteristics and choice of the receiving antenna, it is indispensable to previously know the characteristics of the transmission side, in the ISS. Antennas can be characterized according to multiple parameters, which can be mainly classified into two subgroups: transmission and reception parameters. In this section, a couple of basic transmission concepts will be presented.

### 3.1.2.1.1 Transmission Parameters

Although this Project deals with reception side of the communication, as it has been commented before, knowing transmission parameters is crucial to adequately choose the reception parameters which the receiving antenna must have, as some of them are highly correlated. Particularly, two of the most important ones for the issue at hand are briefly exposed below.

### • Polarization. Faraday Rotation.

Regarding Antennas Polarization, it is defined as the polarization of the wave radiated by the antenna, normally in its direction of maximum gain. Given that the polarization of a radiated wave is said to be the property which describes the time-varying direction and relative magnitude of the electric-field, it can be understood as the curve traced by the end point of the vector representing the instantaneous electric field. An example of that can be seen in figure 3.3.

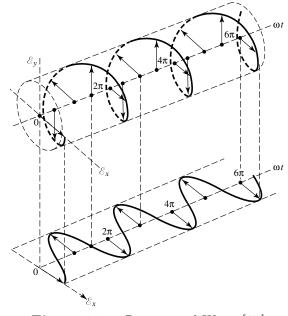


Figure 3.3 – Rotation of Wave [37]

Depending on the figure the electric field vector traces in space, polarization can be classified as *linear*, *circular* or *elliptical*, the first two being special cases of the latter. When dealing with circular or elliptical polarization, it can be distinguished between right-hand polarization, RHCP, and left-hand polarization, LHCP, depending on the rotation of the electric field vector. Graphical comparison of them can be seen at figure 3.4.

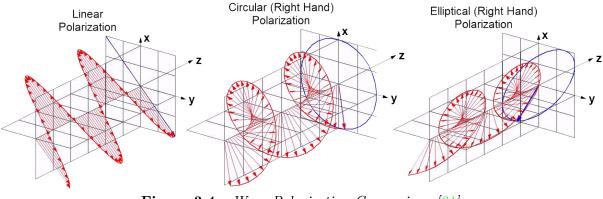


Figure 3.4 – Wave Polarization Comparison [34]

When designing radio-link for satellite communications, polarization choice is a major matter. As a rule of thumb, linear polarization is inadvisable when frequency of work is below 10 GHz, being necessary the use of circular or elliptical polarization. Without going into detail, this is due to a curious phenomena which occurs as a result of Earth's magnetic field which implies a certain rotation when the signal goes through ionosphere, known as Faraday Rotation. The following figure can be illustrative:

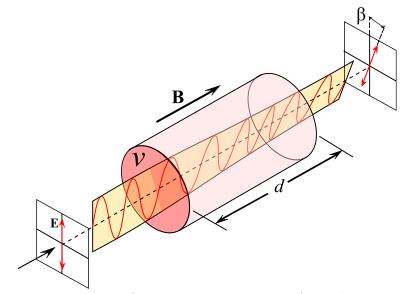


Figure 3.5 – Rotation of Wave as a consequence of Faraday Rotation [16]

This rotation affects to linearly polarized waves below 10 GHz. Above that frequency, Faraday Rotation becomes absolutely negligible (less than 1° of rotation). As it will be seen later, polarization and its associated issues will have to be taken into account in System Design.

#### • Radiation Pattern

According to [37] Radiation Pattern of an antenna is defined as a mathematical function or a graphical representation of the radiation properties of the antenna as a function of space coordinates. It is commonly determined in the far-field region and reflects the spatial distribution of radiated energy along a surface of constant radius. It is usually plotted on a logarithmic scale, normally in decibels (dB). Some of the parts of a radiation pattern are referred to as *lobes*, defining them as portions of the radiation pattern bounded by regions of relatively weak radiation intensity. Significant lobes along with relevant beamwidth are represented in a three-dimensional polar pattern in figure 3.6. Some of them are worth to be defined.

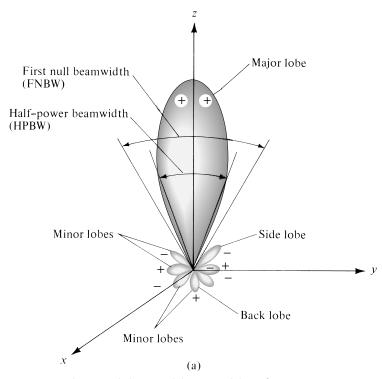


Figure 3.6 – Radiation lobes and beamwidths of an antenna pattern [37]

- Major lobe. Maximum radiation area.

- Minor lobes. Lobes adjacent to the major, with minor amplitude. They are normally undesired and for satellite communication, its magnitude is regulated by UIT Regulation 580 (1 to 5) [60] and UIT Regulation 465 [61].

- Side lobes. The major of the minor lobes.

- Back lobe. Lobe in the opposite direction to the major.

- First Null Beamwidth (FNWB). Angular distance between the directions of the space where the radiation pattern is minimum.

- Half-power Beamwidth (HPWB). Angular direction in which the radiation pattern equals to half of the maximum, (-3 dB).

# 3.1.2.1.2 Analysis

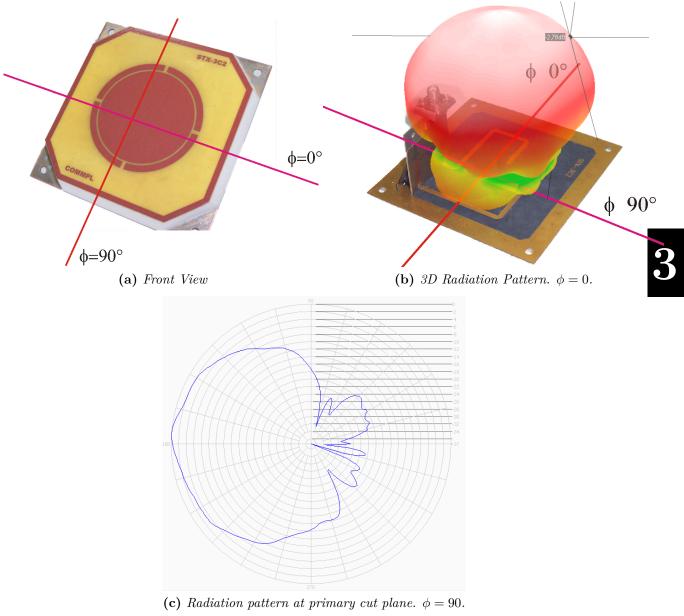
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According to [6], the transmission is operated with the following characteristics:

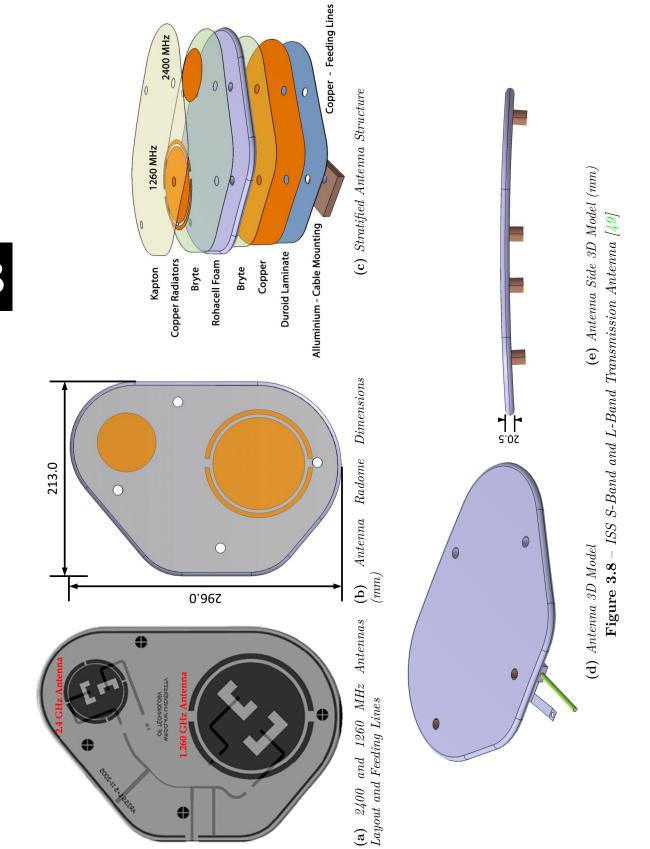
- Transmission frequency may vary between 2369 MHz, 2395 MHz, 2422 MHz and 2437 MHz [15] so, from now on, 2400 MHz will be considered as frequency of work.
- Transmission system is composed of patch antennas, RHCP Polarized. Circular polarization is likely to have been chosen because of being less prone to meteorological attenuation at this frequency and also to prevent the signal from suffering Faraday Rotation.
- EIRP will be 10 W.
- QPSK with FEC 1/2 and a Symbol Rate of 1.3 Ms/s or 2.3 Ms/s will be used as modulation scheme.

The Project which was in charge of designing and developing the 2.4 GHz Antenna for ISS included a 1260 MHz Antenna too. As a consequence, they were developed and encapsulated in the same structure. Both were designed as *patch* antennas with the weight reduction as one of the main requirements of the design, finally resulting in a total weight of 0.525 kg. Printed circuits were manufactured using Rogers RT 5870 laminate, with 0.79 mm of thickness. Descriptive 3D models, dimensions and antenna structure can be found in figure 3.8.

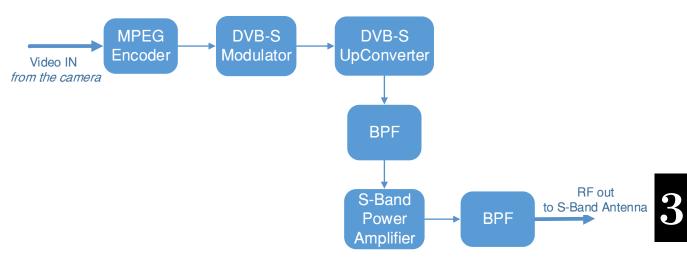
Regarding the feeding cable, 50  $\Omega$  <u>MA/Com NRFC-50-COAX-3</u> was chosen, with inner and outer conductors of silver coated copper, presenting an attenuation of 27.23 dB Max./100 m at 1000 MHz. Once its design was finished, it was manufactured and measured. Measurements yield to qualify circular polarization of the antenna of high quality, with Axial Ratio values between 0 and 2 dB up to wide elevation angles within the beam. The measured antenna gain was 8 dBi (at Broadside direction). Figure 3.7a shows the front view of the final antenna design whereas figure 3.7b shows the 3D radiation pattern for 2.4 GHz antenna when  $\phi = 0$ . On the other hand, 3.7c shows the diagram pattern at primary cut plane, with  $\phi = 90$ .



**Figure 3.7** – 2400 MHZ Antenna [49]



Regarding the transmitter itself, it can be represented with the block diagram of the figure 3.9.



**Figure 3.9** – *Transmission System Block Diagram* 

In brief, the Video IN side will be fed by a Camera, the signal of which will be encapsulated into a MPEG Stream to be transmitted after being modulated to the S-Band using QPSK modulation scheme. Another important piece of information to design the radio-link is the distance between the transmitter, in the ISS, and the Ground Station, on the Earth, which will be calculated from the vertical distance between the transmitter and the surface of the Earth, 400 km.

#### 3.1.2.2 Radio-Link Budget: Friis Equation [42]

First step when designing radio-link is the calculation of its budget, that is, the expected power received. That calculation may be approximated with the following reasoning: let us assume two antennas in free space, being both far enough from each other to consider that they only interact by their Far Fields. Assuming that both antennas are Isotropic, the energy supplied to the antenna will be spread out in a sphere shape, with centre on the radiating antenna. Regarding the received power by the other antenna, placed at a distance r from the transmitting antenna, it will be equally spread across a sphere of radius r when reaching the antenna. Taking into account the area of the sphere and the transmitted power,  $P_{\rm t}$ , it can be written:

$$\phi = \frac{P_{\rm t}}{4\pi r^2} \tag{3.1.1}$$

Equation 3.1.1 is known as *power flux density*. Assuming the receiving antenna is pointing to the maximum gain direction, noting the transmission antenna gain as  $G_{t}$ , it yields to:

$$\phi_{\rm r} = \frac{P_{\rm t}}{4\pi r^2} G_{\rm t} \tag{3.1.2}$$

At the moment, it has been calculated the power density at the receiving antenna, however, not all the power is effectively received, it depends on the antenna aperture; noting it as  $A_{\rm r}$ , the power received is then:

$$P_{\rm r} = \frac{P_{\rm t}}{4\pi r^2} G_{\rm t} A_{\rm r} \tag{3.1.3}$$

On the other hand, Antenna Gain and Effective Aperture are related by:

$$A_{\rm r} = \frac{\lambda^2}{4\pi}G\tag{3.1.4}$$

And finally, substituting equation 3.1.4 into equation 3.1.3, it yields to:

$$P_{\rm r} = P_{\rm t} G_{\rm t} G_{\rm r} \left(\frac{\lambda}{4\pi r}\right)^2 \tag{3.1.5}$$

Expression 3.1.5 is known as **Friis Equation**. Given the extended use of logarithmic units in radio-link design, it is common to rewrite it as:

$$P_{\rm r_{dBm}} = P_{\rm t_{dBm}} + G_{\rm t_{dB}} + G_{\rm r_{dB}} + 20\log\left(\frac{\lambda}{4\pi r}\right)$$
(3.1.6)

Where f is in Hertz and  $\lambda$  and r are in meters. The factor  $20\log(\frac{\lambda}{4\pi r})$  is known as propagation losses which have to be considered regardless of antennas or transmission systems used, as they are independent of them. It is trivial to see that the Friis Equation presented, 3.1.5, is only valid in an absolutely ideal scenario. However, it can be made more realistic by adding factors just as it has been shown in the demonstration. Particularly, *Reflection Losses, Polarization Losses Factor,* PLF, and Meteorological Losses Factor,  $\gamma_r(\frac{dB}{km})$ , will be added. Therefore, Friis Equation 3.1.5, again in decibels, becomes:

$$P_{\rm r} = P_{\rm t} + G_{\rm t} + G_{\rm r} + 10\log(1 - |\Gamma_{\rm r}|^2) + 10\log(1 - |\Gamma_{\rm t}|^2) + PLF - \gamma_{\rm r}d + 20\log\left(\frac{\lambda}{4\pi r}\right)$$
(3.1.7)

Once the Friis Equation has been fully demonstrated, it is going to be particularized for the Radio-Link Budget needed.

From the transmission system information given in 3.1.2.1, the power is given as EIRP,

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and equals to 10 W, so the product corresponding to  $P_tG_t$  can be replaced by  $10\log(EIRP)$ ; in addition, knowing the work frequency and the distance, 400 km, propagation losses factor is entirely known. As a first reasonable approximation, let us assume that transmission system is matched, and receiver system will be too, implying no Reflection Losses, and therefore  $\Gamma_t = \Gamma_r = 0$ . If the receiver system uses RHCP antenna, there will have no polarization losses and PLF=0. Substituting all those variables in equation 3.1.7 it yields to:

$$P_r = -112.087 \text{ dBm} + G_r - \gamma_r d \tag{3.1.8}$$

Now, Friis Equation for the radio - link is function of receiver antenna gain and rain fading. Regarding the latter, it is estimated by using ITU-T coefficients [59]. Particularly, that factor is given by the following expression:

$$\gamma_{\rm R} d = k R^{\alpha} d \tag{3.1.9}$$

Where d is the effective distance of the radio-link and k and  $\alpha$  coefficients varies depending on frequency and vertical or horizontal polarization and, as said before, are tabulated in [59] the following values are obtained for 2.5 GHz:

Coefficients/Polarization	k	α			
Vertical	0.0001464	1.0085			
Horizontal	0.0001321	1.1209			

Table 3.1 – Coefficients for rain attenuation at 2.5 GHz

Coefficients at 2.4 GHz could be interpolated, however, the difference is so small that it is not worth it. However, equation 3.1.9 cannot be directly used because neither vertical nor horizontal linear polarization will be used, but circular. For that reason, k and  $\alpha$  coefficients have to be recalculated, using the following expressions:

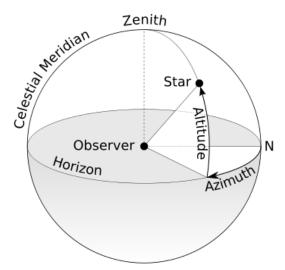
$$k = \frac{k_{\rm H} + k_{\rm V} + (k_{\rm H} - k_{\rm V})\cos^2\theta\cos^2\tau}{2}$$
(3.1.10)

$$\alpha = \frac{k_{\rm H}\alpha_{\rm H} + k_{\rm V}\alpha_{\rm V} + (k_{\rm H}\alpha_{\rm H} - k_{\rm V}\alpha_{\rm V})(\cos^2\theta)(\cos\tau)}{2k}$$
(3.1.11)

Where in addition to the coefficients commented before, there are two angles of interest:

•  $\theta$ : Elevation Angle. Each pass of the ISS will be made with a different elevation angle. Those angles can be tracked for Granada from [17]. It is also known as altitude.

21



**Figure 3.10** – Elevation Angle and another notable angles representation [35]

•  $\tau$ : Polarization Angle. In the case of circular polarization as the one considered, it equals to  $45^{\circ}$ .

Once the coefficients have been recalculated, the only variable left is R, the rainfall rate in mm/h. According to the information given by [1], Granada rainfall rate is quite low, being classified as an arid area, which probably means that there will not be significant signal losses due to rain. As a reference, 3 mm/h will be considered, which is classified as 'moderate rainfall'; of course, higher rainfall rate could circumstantially occur, implying higher attenuation, however the reference taken is reasonable for the major part of the time. Differences in k and  $\alpha$  with  $\theta$  have been proved to be negligible, therefore equation 3.1.9 becomes:

$$\gamma_{\rm R}d = 0.1392 \cdot 35^{1.0618}d = 6.07d \tag{3.1.12}$$

Now, rain-caused attenuation is just a function of effective distance, in kilometers. As it can be appreciated in figure 3.12, effective distance, d, between Ground Station and the ISS will also vary with  $\theta$ , given that 400 km is the vertical distance above the sea level.

Calculating the effective distance as a function of  $\theta$  is a matter of basic trigonometry. Particularly, it is calculated for the data range between 10 and 90 degrees. Considering resulting distances and equation 3.1.12, attenuation due to rain can be calculated as a function of elevation angle. Figure 3.11 shows the results.

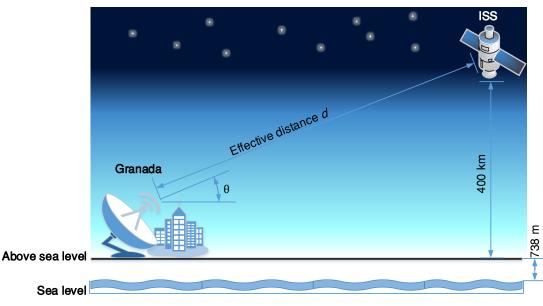


Figure 3.12 – Radio-Link Schematic Representation

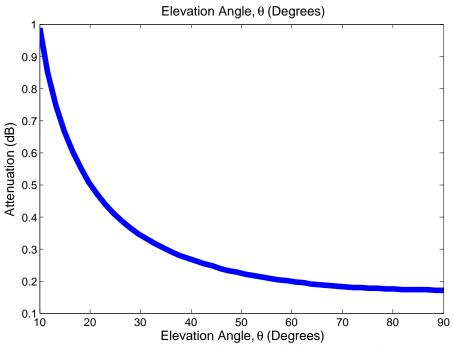


Figure 3.11 – Rain losses with elevation angle

It can be appreciated that attenuation is not significant for almost any elevation angle, when assuming the rainfall rate indicated; only if elevation angle  $\theta$  equals to 10° the attenuation rises to 1 dB. In sum, attenuation due to rain in this area can be neglected for the radio-link.

3

Taking it into account, equation 3.1.8 yields to:

$$P_r = -112.087 \text{ dBm} + G_r \tag{3.1.13}$$

Therefore, received power expression is now only function of receiving antenna gain. Once again, it is necessary to remark the approximated character of these calculations, nevertheless, they suppose a vital step previous to the receiver design, as it will be seen later.

# 3.1.2.3 RX Antenna

When an antenna receives an incident wave, part of its total power is transferred to the receiver. Then, the antenna is said to be in reception mode. Reception System Side must be designed in accordance with the information provided in 3.1.2.1, given that this side allows a great number of degrees of freedom, unlike the transmission side, which is fixed. In the same way, data provided by Radio-Link Budget in section 3.1.2.2 must also be taken into account. Previously, it is worth to make clear some basic concepts regarding reception antennas parameters.

### 3.1.2.3.1 Reception Parameters

As mentioned in section 3.1.2.1, and in spite of being related, reception and transmission antenna parameters can de defined separately. Two of the most important reception parameter, also for the System in hand, are the following.

# • Adaptation

Adaptation parameter is a capital one not only in Antenna Field but also in almost every Electronics or Radio-frequency design. When working in reception mode, antenna is connected either to a transmission line or directly to a receiver. In order to get **maximum power transfer**, antenna impedance,  $Z_a = R_a + jX_a$  and load impedance  $Z_L = R_L + jX_L$ must be complex conjugate,  $Z_L = Z_a^*$ . When this occurs, delivered power corresponds to:

$$P_{\rm L_{max}} = \frac{|V_{\rm ca}|^2}{4R_{\rm a}} \tag{3.1.14}$$

When there is no adaptation, assuming no source load, delivered power decreases with a factor  $\Gamma$  according to the following expression:

$$P_{\rm L} = P_{\rm L_{max}} (1 - |\Gamma|^2) \tag{3.1.15}$$

Where  $\Gamma$  is the reflection coefficient at the load and is given by equation 3.1.16.

$$\Gamma = \frac{Z_{\rm L} - Z_0}{Z_{\rm L} + Z_0} \tag{3.1.16}$$

Where  $Z_{\rm L}$  is the antenna impedance and  $Z_0$  is the characteristic impedance of the transmission line or input impedance of the receiver attached.

### • <u>Effective Area</u>

When an incident wave reaches an antenna, the effective power it takes from the wave depends on its Effective Area; it is defined as the relation between the power the antenna delivers to its load, (assuming perfect matching and lossless environment), and power density of the incident wave.

$$A_{\rm ef} = \frac{P_{\rm L}}{\wp} \tag{3.1.17}$$

Equation 3.1.17 represents the portion of the wavefront the antenna has to capture and transmit to the load. It immediately implies dependency with load impedance, adaptation and wave polarization. If equation 3.1.14 is substituted into equation 3.1.17 and taking into account that  $\wp = |E|^2/\eta$  it yields to:

$$A_{\rm ef} = \frac{|V_{\rm ca}|^2}{4R_{\rm a}\wp} = \frac{|V_{\rm ca}|^2\eta}{4R_{\rm a}|E|^2}$$
(3.1.18)

In addition, maximum Effective Area of an antenna can be related with its Directivity D, with:

$$A_{\rm ef_{max}} = D \frac{\lambda^2}{4\pi} \tag{3.1.19}$$

Once again, these concepts will gain importance in both, analysis and design stage of the System.

## 3.1.2.3.2 Analysis

Now, some preliminary constraints can be extracted from the transmission system:

- RX Antenna must be tuned at 2.4 GHz, with 100 MHz bandwidth, in order to be able to receive among the different transmission frequencies.
- RX Antenna must be RHCP Polarized, in consonance with the transmission system. If circular polarization mismatching occurs, there would not be signal reception.

- RX Antenna should be very directive. It implies having a narrow HPBW, so the signal of interest is maximized while weakening the rest of the spectrum.
- Taking into account expression 3.1.13, RX Antenna should be high-gain, in order to increase signal power, which will reach Ground Station with very low amplitude.

Considering those guidelines, RX could be helicoidal or parabolic, in order to get highgain, and being preferably circularly polarized. Linear Polarization is inadvisable not only to avoid Faraday Rotation commented before, but also because it would imply 3 dB attenuation because of polarization mismatch.

# 3.1.2.4 RF Conditioning

Keeping in mind equation 3.1.13, and considering that the receiver implemented in the following block will exhibit a certain sensitivity, it is likely to be needed an stage to adapt the signal and provide it with the characteristics expected by the rest of the System.

When sending signals using antennas and specially when dealing with radio - link over satellite, at the receiver the signal normally needs an strong **amplification** stage because of the attenuation suffered, as seen in section 3.1.2.2; again, the reason why this amplification is needed is meeting the minimum sensitivity required by the rest of the circuitry in order to adequately function. In the same way, a **mixing** stage, which *down-converts* the signal to an **intermediate-frequency**, lower, is also necessary. Despite the transmission of the signal over the air being made at higher frequencies, because it allows to minimize antennas size, the benefits of reducing the signal frequency when reaching the receiver are countless:

- The higher the signal frequency, the higher circuitry complexity, and poor performance.
- Passive components such as capacitors or inductors multiply their parasitics components, making their behavior unpredictable.
- Active devices such as transistors exhibit lower gain than at lower frequencies.
- Attenuation over Guided transmission mediums (e.g, coaxial cable) increases noticeably with frequency.
- It allows working with a fixed frequency at the receiver regardless of little changes at the transmission frequency.
- It allows keeping a constant bandwidth.
- It increases Selectivity dramatically.
- Reducing costs.

Therefore, *RF* Conditioning block can be mainly subdivided in the following blocks.

#### 3.1.2.4.1 Pre-Amplification Stage

Right after being received by the antenna, at the RF Front-end, the signal is weak and its pass through a Guided transmission medium without an amplification will bring signal below *Noise Floor*, reducing the signal to just noise. To avoid it, a pre-amplification stage as close as possible from the antenna is needed. Particularly, it usually consists of a **Low Noise Amplifier**, or LNA, which is intended to increase the power of the signal without significantly degrading its SNR.

The main part of a LNA is the **amplifier**. When dealing with <u>microwave</u> amplifiers as the ones used in a typical LNA, some vital concepts must be remarked as part of the previous analysis. The reader is aware of the complexity and extension of the concepts explained below, so this does not expect to be neither a complete nor a detailed definition but only a brief introduction for the concepts and techniques which will appear through this analysis and later design. Detailed and more accurate explanations as well as S-Parameters definition can be found in [43] and [53].

## -Stability

The stability of an amplifier, or its resistance to oscillate, is a crucial consideration in amplifier design and use. In a two-port network, oscillations are possible when either the input or output port presents a negative resistance; it occurs when  $|\Gamma_{IN}|>1$  or  $|\Gamma_{OUT}|>1$ . Figure 3.13 will result clarifying for this brief definition.

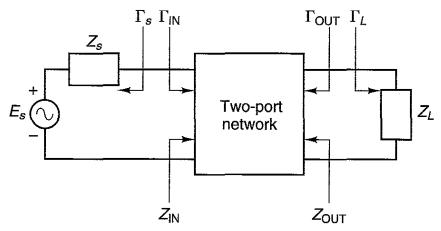


Figure 3.13 – Stability of two-port networks [43]

The two-port network of the figure 3.13 is said to be **unconditionally stable** at a given frequency if and only if the real parts of  $Z_{\rm IN}$  and  $Z_{\rm OUT}$  are greater than zero for every passive load and source impedances. Other way, it is said to be **potentially unstable**. In terms of reflection coefficients, they must be minor than one at both sides of the two-port network.

Although relatively complex calculations can be performed in order to determine the regions of the Smith's Chart where the amplifier is conditionally stable, for the sake of simplicity it will be exposed only the test for unconditional stability; it is known as  $K - \Delta$  test and is based on the **Rollet's condition**, defined as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1$$
(3.1.20)

Where  $|\Delta|$  is given by:

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{3.1.21}$$

Equations 3.1.20 and 3.1.21 must be simultaneously satisfied. When choosing the amplifier of an LNA, it must be ensured that it complies with this condition, for the source and load impedances.

#### -Power-Gain Circles

With regards to *gain* concept, it coincides with the habitual used in electronics. However, again, due to the frequency range, it is necessary to differentiate a couple of concepts which will be necessary to know in order to select an amplifier for the LNA design. These are:

- MAG: Maximum Available Gain, is only defined when K is greater than one, that is, the device is unconditionally stable. It corresponds to the maximum gain the device is able to offer, at all cases.
- MSG: Maximum Stable Gain, it is defined as the maximum gain possible when the device is potentially unstable.

## -1 dB Compression Point

To quantify the linear operating range of the amplifier, (and mixers) we define the 1 dB Compression Point as the power level for which the output power has decreased by 1 dB from the ideal linear characteristic. For amplifiers  $P_{1dB}$  is usually specified as an output power, while for mixers  $P_{1dB}$  is usually specified in terms of input power. Figure 3.14 illustrates this concept.

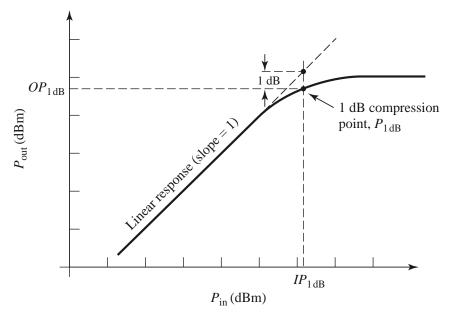
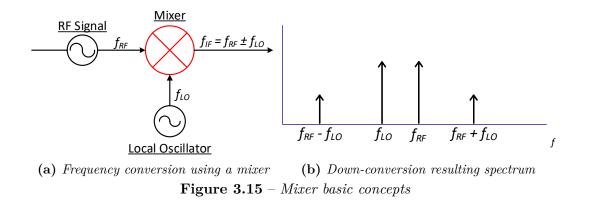


Figure 3.14 – Definition of the 1 dB compression point for a non-linear amplifier [53]

# 3.1.2.4.2 Mixer

As said before, when reaching the receiver, mixing is an habitual and beneficial operation. Just as mentioned in the previous sub-block, Mixers form a huge matter by themselves, not affordable from these lines. For that reason, only the concept of  $\underline{\text{mixing}}$  will be briefly introduced.

A mixer is a three-port device that uses a non-linear or time-varying element to achieve frequency conversion. Operation of practical RF and microwave mixers is usually based on the non-linearity provided by either a diode or a transistor which can generate a wide variety of harmonics and other products of input frequencies, so filtering must be used to select the desired frequency components. Frequency conversion using a mixer and down-conversion resulting spectrum (ideal) are shown in figure 3.15.



Mixer acts as a frequency multiplier resulting in an output which consists in the sum and differences of the input signal frequencies.

$$f_{\rm IF} = f_{\rm LO} \pm f_{\rm RF} \tag{3.1.22}$$

Note that the above explanation only considers the sum and difference outputs as generated by multiplication of the input signals, whereas in a realistic mixer many more products will be generated due to the more complicated non-linear behavior of the diode or transistor. These products are usually undesirable and are removed by filtering, as will be verified in simulation in chapter 4.

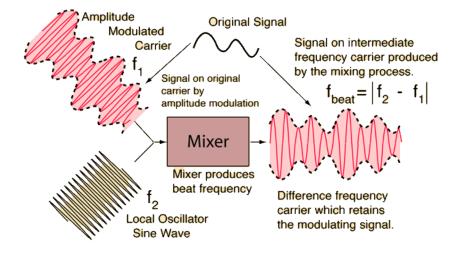


Figure 3.16 – Mixing operation [54]

# 3.1.2.5 PCB Receiver

After reaching the antenna, or going through RF Conditioning Block if necessary, the signal reaches the *PCB Receiver*. PCB Receiver analysis and design is highly related with the functional requirements stated at 2.1. Particularly, the requirements to be met with this block are the following:

- The system must allow connecting to an antenna which permits the reception.
- The system must allow feeding up to the antenna, in case it is necessary DC current at any point.
- The system is expected to have an USB interface which allows direct connectivity with

a PC, being portable as opposed to the PCI solutions.

- The system must be compatible with the existent software solutions.
- The system should consume the smallest amount of power possible.
- The system must have the possibility of being supplied directly from electric network.

To clearly differentiate how they are going to be met, the PCB Receiver block can be at the same time divided in 3 sub-blocks.

# 3.1.2.5.1 Signal Reception

To receive the signal after *RX Antenna* Block, or *RF Conditioning* if needed, PCB Receiver must have a NIM, or *tuner*. In essence, the Tuner receives an RF Signal and, after down-converting to Baseband, demodulates it, getting MPEG-4/H.264 video stream. There are plenty of options in the market for this band of frequency; however, the election is constraint by the chips accepted for the software subsystem, as analyzed in subsection 3.1.1. Particularly, Minitioune constraints the selection regarding the Zero-IF and demodulator chips, accepting the following models:

- Zero-IF: STB6100, STV6110, STV6111.
- Demodulator: STV0903, STV0913.

Everyone belongs to the widely known semiconductor trademark ST. In order to keep with the analysis, the functioning of these chips will be briefly introduced.

# <u>- Zero-IF</u>

Zero-IF or homodyne receiver, is the chip in charge of demodulating the incoming signal to Baseband, by using synchronous detection driven by a local oscillator. The standard block diagram of the chips accepted is the one in figure 3.17.

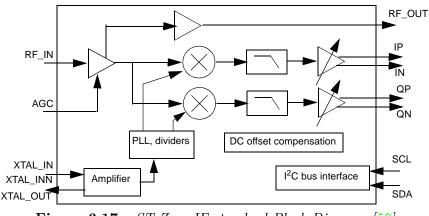


Figure 3.17 – ST Zero-IF standard Block Diagram [57]

On the RF input, there is a LNA as well as an Automatic Gain Control, a closed - loop feedback to provide a controlled signal amplitude at the output, regardless of The signal reaches the mixers, which are connected to an variations at the input. integrated PLL; this PLL contains an on-chip VCO which provides LO signals to the mixer. VCO output frequency is controlled via I2C, using the software MiniTioune. A **phase-frequency detector** is used to compare input frequency with the frequency of the LO generated, by dividing the crystal oscillator reference frequency, which does not suffer from the thermal drift. This produces a correction voltage which varies the LO frequency if needed, keeping it *locked* with the input signal. One of the major drawbacks of a direct-conversion receiver as the analyzed, is that signal leakage can occur; particularly, LO energy may leak trough the mixer stage to the antenna input and be reflected back into the mixer stage. The overall effect of it, is that the LO energy self-mixes and generate a DC offset signal, which may be large enough to overload the Baseband amplifiers, overlapping desired signal; for this reason, after mixing stage, a **DC offset compensation** block is implemented. Finally, the signal is converted into its equivalent Baseband signal in 8PSK/QPSK, with in-phase and quadrature component signals. As for the chips allowed, the input frequency range goes from 950 MHz to 2150 MHz; it means that it will be necessary, as anticipated in section 3.1.2.4.2, a mixing stage to down-convert from 2400 MHz to that range.

#### - Demodulator

After the Zero-IF, the signal attacks the demodulator. It processes the two quadrature outputs from the direct-conversion receiver, being sent to a Dual 10-bit ADC. The DC offset, amplitude mismatch and quadrature error are corrected and the AGC signal level to the tuner is calculated. The carrier frequency offset is corrected. After going through FEC block, the data is taken to the transport stream interface. Figure 3.18 shows the typical application diagram with two of the chips allowed.

Once the data has been encapsulated into an MPEG-4/H.264 stream, it has to be sent to the PC, which will be made with the next sub-block.

Regarding the meeting of the functional requirements achieved with tuners, they all allow, obviously, **connection to an antenna** and **feeding up the antenna**. Although it was not a functional requirement *per se*, they convert the signal coming from the antenna to a digital stream to be transmitted to the PC which is, indeed, the final aim.

#### 3.1.2.5.2 Transmission to PC

As said before, the main goal of the system is transmitting the video signal to a PC. Once the signal has been correctly demodulated with the NIM, it has to be brought to a PC. Taking into account it is the *de facto* standard for easy quick connectivity, USB connection is another functional requirement. The equivalent technical requirement to comply it, is having an USB Microcontroller. An USB Microcontroller implements the USB Protocol

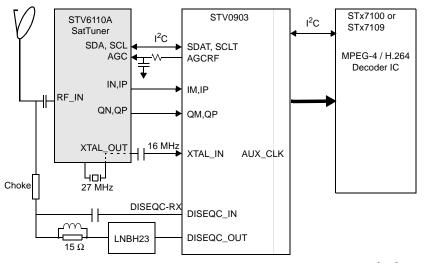


Figure 3.18 – Typical Application Block Diagram [56]

Stack and is in charge of making the PC recognize the USB Driver, at the time that converts the data received in a parallel bus into an USB signal. It allows rapid USB integration, being useful for prototyping. Contrary to the tuner chips, there are no, *a priori*, constraints on USB Microcontroller selection.

Selected USB Microcontroller must be able to receive I2C instructions, as it will be the interpreter between PC and Tuner, which, as seen in previous sub-block, will receive LO Frequency by this via. In addition, lower consumption would be recommendable. At least USB 2.0 Version will be compulsory, in order to achieve enough Speed Transfer. Existence of dedicated software to program the chip will also be taken into account.

Depending on availability and price, integrated board will be considered to accomplish this task.

#### 3.1.2.5.3 Supply System

Although Supply System and Power Budget will be consequently analyzed and designed according to the rest of components selected in chapter 4, as it has been previously made, some basic concepts are introduced as part of the System Analysis.

Given the variety of components existent nowadays in every design, it is unlikely that they share the same voltage supply. In these cases, **voltage regulators** are needed, to step up, down or invert the main voltage supply to the different voltage lines needed. When choosing a regulator there are mainly two possibilities: switching and linear. They will be briefly introduced.

#### - Linear Regulator

Linear Regulators behave as a variable resistor, which is continuously adjusting a voltage divider network, maintaining a constant voltage output. The difference between the input and output voltage is burnt up as heat. Obviously, these facts make these devices highly inefficient, normally wasting more power stepping down the voltage than the finally delivered to the load. In addition, given that output voltage must always be lower than input, linear regulator can only function in step-down mode. The minimum difference between input and output voltage in order for the regulator to correctly function is known as Dropout Voltage. LDO Voltage Regulators are an special range of them which deals with minimizing that voltage. Figure 3.19 shows a simplified schematic of a typical linear regulator.

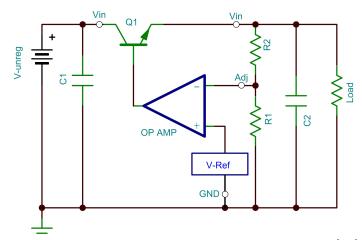


Figure 3.19 – Linear Regulator Basic Schematic [58]

Despite the disadvantages commented, its use is simple and they are cheaper than switching regulators, which makes them very popular. Figure 3.20 shows the classical Linear Regulator LM7805.



Figure 3.20 – LM7805 in Through-Hole Package.

#### - Switching Regulator

Contrary to linear, switching regulators alternate the state of its/their transistor/s between on and off (cut and saturation). That switching is controlled by what is known as Duty Cycle and allows that almost no power is dissipated as in linear regulators, which make these much more efficient. In addition, since the efficiency is not so dependent on input voltage, it can be used with higher voltage sources to deliver more power to the load. Apart from that, they allow not only stepping-down voltage, but also stepping-up or inverting. The major drawback of switching regulators, besides of its superior complexity and price, is the production of noise and radio-frequency interference at the output. Basic schematic of a step-down (Buck) switching regulator is shown in figure **3.21**.

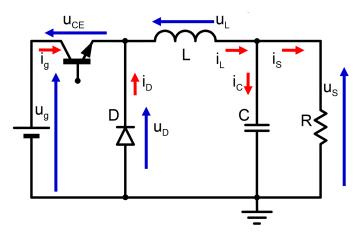


Figure 3.21 – Switching Buck Regulator Basic Schematic [55]

The main differences between both are summarized in table 3.2.

#### 3.1.2.5.4 Discrete Components

Apart from the different devices which compose the system, such as tuner or regulators, discrete components are needed to assure the correct functioning of the rest. Within the possibilities, the most advanced is SMT technology, so discrete components will be implemented using this package, when possible.

SMT Technology optimizes space when compared with THT Technology, however the latter one may be needed when high temperatures are reached. Particularly, in this Project, SMT 0805 will be used, this is, 8 mils length and 5 mils width. Figure 3.22 shows some of the discrete SMD components used.

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SMD

0805

(a)

Resistor



 $\dot{E} lectrolytic$ 

Capacitor



SMD

0805



(**d**) *SMD* 0805 *LED* 

Figure 3.22 – Discrete Components Used Examples

(c)

Capacitor

	Linear	Switching		
Function	Buck function (only steps down)	Boost (steps up), buck, inverts		
Efficiency	Low, except if difference between input and output voltage is small	High, except for very low load currents		
Complexity	Low	Medium - High		
Size	Generally small except if includes large heatsinking	Usually larger than linear		
Cost	Low	Medium - High		
Noise	Low	Medium - High, due to switching rate		

Table 3.2 - Linear Regulators and Switching Regulators Comparison

### CHAPTER

4

## SYSTEM DESIGN

In this chapter, each one of the blocks and sub-blocks analyzed in Chapter 3 will be designed and implemented. In the design, every constraint or requirement extracted in former chapters (regarding RX Antenna, RF Conditioning Block, Supply System, Signal Reception and Transmission to PC) will be taken into account, as well as the ones which will appear. In the same way, the software solution used will be configured and the process to allow the reception will be exposed.

Given that the software configuration varies depending on the hardware design, the first section deals with this block of the system, receiving antenna choice, the selection of every technology needed, component choices, and finally their integration in a PCB. Schematics and 3D Models will be added as part of the design, as well as the manufacturing section. With regards to RF Conditioning Block, Mixer schematics and simulation using ADS<sup>®</sup> will be added too.

#### 4.1 Hardware

#### 4.1.1 RX Antenna

Reception System Side must be designed in accordance with the information provided in 3.1.2.1, given that this side allows a great number of degrees of freedom, unlike the transmission side, which is fixed. In the same way, the data provided by Radio-Link Budget in section 3.1.2.2 must be also taken into account. Particularly, some preliminary constraints can be extracted from the transmission system:

- RX Antenna must be tuned at 2.4 GHz, with 100 MHz bandwidth.
- RX Antenna must be RHCP Polarized.
- Taking into account expression 3.1.13, RX Antenna should be high-gain, in order to make possible the radio-link.

Considering those guidelines, RX could be helicoidal or parabolic, in order to get highgain, and being preferably circularly polarized. Linear Polarization is inadvisable not only to avoid Faraday Rotation commented before, but also because it would imply 3 dB attenuation because polarization mismatch. Three possibilities will be considered: two antennas available off-the-shelf and another commercialized one.

#### 4.1.1.1 Helix Antenna

The first off-the-shelf option is a 3 turns helicoidal antenna designed as part of a final master thesis [40]. It was first modelled with SolidWorks<sup>®</sup> with the dimensions shown in figure 4.1.

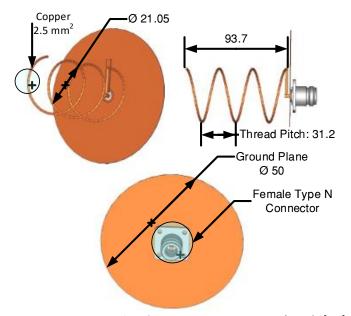


Figure 4.1 – Helix Antenna Dimensions (mm) [40].

Figure 4.2 shows the antenna after building.



Figure 4.2 – Helix Antenna Built [40].

Once modelled it is exported to  $CST^{\otimes}$  and simulated, getting the results shown in figures 4.3 and 4.4.

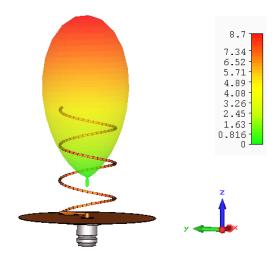


Figure 4.3 – Helix Antenna Simulation Results. 3D Radiation Pattern.

According to the results obtained, the antenna is correctly tuned at 2.4 GHz and exhibits a directive radiation pattern, with 8.7 dB gain. A priori, it looks not sufficiently directive. Materials needed for its building have a cost of about 20  $\in$ .

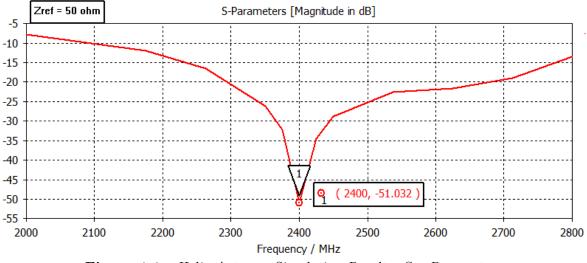


Figure 4.4 – Helix Antenna Simulation Results. S<sub>11</sub> Parameter.

#### 4.1.1.2 Long Helix Antenna

Another antenna available in stock is a long helix like the one in figure 4.5.



**Figure 4.5** – *WiMo Helix 13-40* 

It is sold by WiMo [36], and according to the manufacturer, it shows the characteristics exposed in table 4.1.

Although the first intention was experimentally measuring it, its dimensions makes it difficult as a consequence of the distance needed to start its Far Field. This can be easily proved [37]. When the maximum overall dimension of the antenna is large in comparison with the wavelength (in this case, it is 10 times larger) the Far Field region is commonly taken to exist at distances greater than the one given by:

$$d_f = \frac{2D^2}{\lambda} \tag{4.1.1}$$

Being D the largest dimension of the antenna and  $\lambda$ , the wavelength. Applying equation

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Parameter	Value
Frequency (MHz)	2300-2450
Gain (dB)	16
Turns	40
SWR	1.5
Max Power (W)	500
Connector	Ν
Length (m)	1.25
Material	AlMgSi 0.5

 Table 4.1 – WiMo Helix 13-40 Specifications

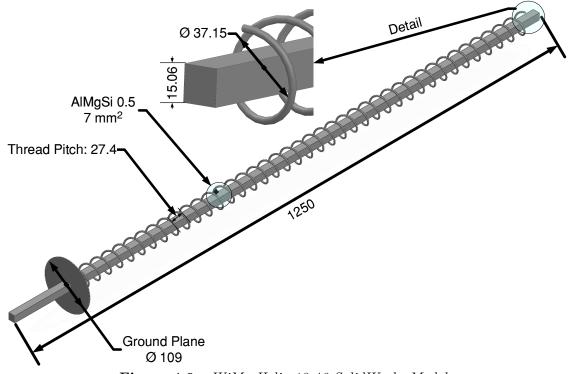


Figure 4.6 – WiMo Helix 13-40 SolidWorks Model

4.1.1 yields to a Far Field distance of **25 m.** Given that the necessary distance cannot be reached, so the measurement is correctly performed, it is decided to evaluate its behavior in a simulation environment. In order to do this, the antenna is first modelled with SolidWorks<sup>®</sup> and then simulated with CST<sup>®</sup>. 3D Model is shown in figure 4.6.

The model is imported into  $CST^{\otimes}$  and simulated, getting the results shown in figure 4.7 and 4.8.

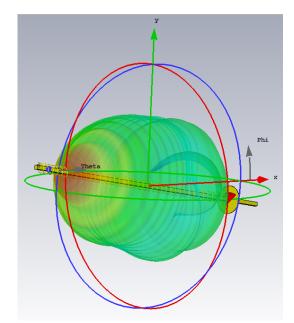


Figure 4.7 – WiMo Helix 13-40 Simulation Results. 3D Radiation Pattern.

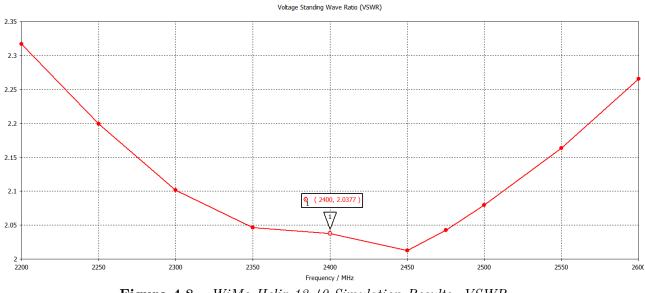


Figure 4.8 – WiMo Helix 13-40 Simulation Results. VSWR

Simulations results show 15 dB gain and VSWR of 2.04 at 2.4 GHz. Given that those results are quite similar to the ones provided by the manufacturer, table 4.1, the specifications are accepted as valid. WiMo Helix 13-40 has a cost of  $122 \in$ .

#### 4.1.1.3 Commercialized Helix Antenna with Parabolic Dish

Finally, it will be analyzed a commercialized Helix Antenna with an associated Parabolic Dish, which will allow to substantially increase antenna gain. Regarding the supplier [30], RF HAM DESIGN is a specialized trademark in satellite communications. Unfortunately, the lack of technical information about the system in their website impedes to perform any kind of simulation; however, multiple users have rated their designs to work successfully for ISS Communications, which supposes a positive feedback for the present design. The Helix Dish Feed offered by RF HAM Design for the band needed to make this radio-link possible is LHCP Polarized and is tuned in the range 2.4 - 2.5 GHz, return losses greater than 28 dB and VSWR equals to the unit at the frequency of work. LHCP Polarization is needed at the dish feed, due to the inversion that dish produces in the original polarization, RHCP. Its costs is  $121 \in$ .

As for the Parabolic Dish, it is common to use 1.2 diameter version, with F/D equals to 0.45, exhibiting 26 dBd at 2.4 GHz and 8.1 degrees for -3 dB angle. The cost of the Parabolic Dish is  $265 \in$ , so the total price rises to  $386 \in$ .



Figure 4.9 – RF HAM Design 1.2 m Parabolic Dish

To conclude, it must be remarked an important antenna parameter which has not been taken into account during analysis: **antenna temperature**. Every object with a physical temperature above absolute zero (0 K = -273°C) radiates energy. The noise power at the terminals of a receiving antenna is associated to a certain antenna noise temperature,  $T_a$ . Depending on antenna ohmic losses, noise power will entirely come from external sources or not. Unfortunately, there is no information available from the supplier about this parameter for the exposed antennas. For this reason, figure 4.10 is included, providing a general reference for antenna temperature as a function of frequency.

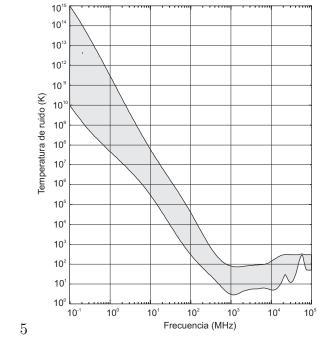


Figure 4.10 – Antenna Temperature as a function of frequency [39]

Thus, according to 4.10, antenna temperature for 2.4 GHz is in the range 7.5 K - 90 K. The following table summarizes the different possibilities shown:

Antenna	Gain	VSWR	Lenght/Diameter (m)	Weight (kg)
Helix Antenna	$8.7 \mathrm{~dB}$	1.01	0.094	0.350
Long Helix Antenna	16  dB	1.5	1.25	1.1
Helix Antenna + Parabolic Dish	25.5  dBd	1.01	1.2	6

 Table 4.2 – RX Antenna Analyzed Possibilities

Prices differ significantly between the three options exposed. In order to decide the optimum antenna for this Project, and given that gain is one of the vital parameters to take into account, (the amplification already accomplished with the antenna will allow reducing the amplification needed in the RF Conditioning Block, and therefore its price), equation 3.1.13 is computed for the three values of gain, resulting in the received powers shown in table 4.3.

Antenna	Received Power (dBm)	Price $(\in)$	
Helix Antenna	-103.39	20	
Long Helix Antenna	-96.09	122	
Helix Antenna + Parabolic Dish	-86.59	386	

 Table 4.3 – Received power depending on RX Antenna, according to Friis Equation 3.1.13

The final choice must depend on receiver specifications, particularly on its sensitivity. For instance, short helix antenna is not likely to be directive enough; such a lower gain will require large and expensive amplification on the following sub-block of the system and therefore can be discarded. Regarding the couple of antennas left, taking into account that Long Helix Antenna is already in stock and that although the parabolic system offers 10 dB gain more, it is 216.4 % more expensive, **the Long Helix Antenna is chosen to be the receiving antenna**.

#### 4.1.2 PCB Receiver

In order to later design the block corresponding to *RF Conditioning*, it is necessary to firstly design the PCB Receiver block, which will allow knowing its input signal requirements, so in the previous block of the system the signal can be adequately treated to acquire those characteristics. Before designing the receiver, one of the PCI solutions is shown. As studied before, the software used constraints the hardware which can be used; regarding PCI cards, one of the accepted ones is TechnoTrend S2-3200, from German Manufacturer TechnoTrend, [32].



Figure 4.11 – TechnoTrend S2-3200 [33]

This PCI card exhibits the specifications shown in table 4.4. It is a plug & play device which, however, lacks of portability, one of the main objectives of this Project. Its cost is  $40 \in$ .

Parameter	
Input Frequency Range (MHz)	950 - 2150
RF Input Level (dBm)	-65 to -25 dBm
Channel Bit Rate (Mbps)	Up to $90$
Input Connector	F-Type

 Table 4.4 – TechnoTrend S2-3200 Main Specifications

With the aim of portability, PCB Design is undertaken. It is made using Altium Designer<sup>®</sup> 16, an EDA tool in which the design is firstly made on schematics that are later converted into *footprints* to perform the design. As a first step, the sub-blocks belonging to the PCB Receiver analyzed in 3 are listed again, so actual components using the technologies needed are compared, in order to select the optimum one.

#### 4.1.2.1 Signal Reception

As analyzed, some NIM is necessary at the receiver. Considering the constraint given by the chips analyzed in that section, it is made a research of tuners which implements one of the accepted chips. Among the selection found, the ones that have been proved to adequately receive this signal by users of Viva DATV are chosen. These are:

- Eardatek EDS-4B47FF2B+
- Sharp BS2F7VZ0169
- Samsung DNBU10711IST

There is no information available for neither Eardatek nor Samsung. However there is for the Sharp, and considering that they all use the same demodulator chip, STV0903, it can be assumed that its behavior is going to be comparable. The main technical information is:

- Receiving Frequency Range (MHz): 950 2150.
- Input Signal Level Range (dBm): -65.
- Input Impedance ( $\Omega$ ): 75.
- Channel Symbol Rate (Ms/s): Up to 45.
- RF Output Gain: -5 to +5 dB.
- Supply: 3.3 V for demodulator, 1 V for zero-IF.

Their price fluctuates, however it is often about  $20 \notin$  or less. Given that the three share technical characteristics, design election has depended on availability, as they are usually hard to find. Regarding the meeting of the functional requirements achieved with them, they all allow, obviously, **connecting to an antenna**, with F-Type connector, and **feeding up the antenna**. Although it was not a functional requirement *per se*, they convert the signal coming from the antenna to a digital stream to be transmitted to the PC which is, indeed, the final aim. **The chosen NIM is Sharp BS2F7VZ0169**, with a cost of 14  $\notin$ .

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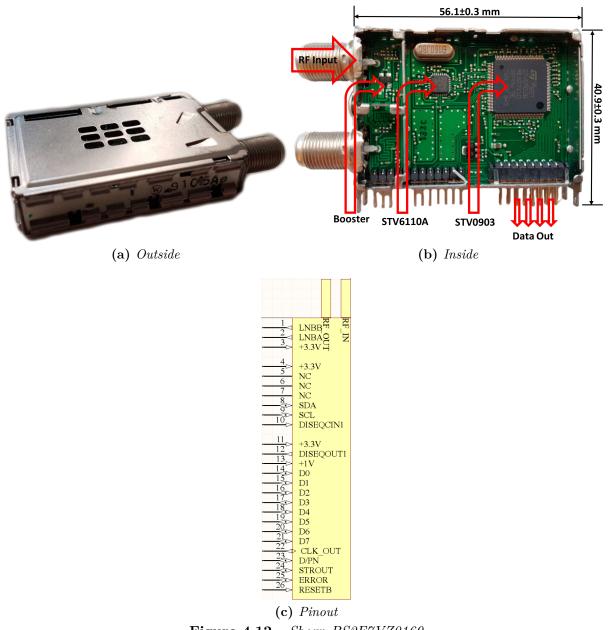


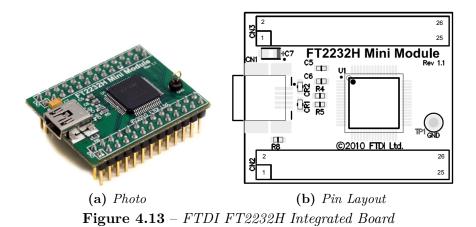
Figure 4.12 – Sharp BS2F7VZ0169

Figure 4.12 shows it, as well as its internal circuitry.

Figure 4.12b shows that Sharp BS2F7VZ0169 is composed of some of the chips allowed, particularly, STV6110A y STV0903.

#### 4.1.2.2 Transmission to PC

Section 3.1.2.5.2 served as introduction to the USB technology which will be used to perform the transmission to a PC, by making use of an USB Microcontroller. When dealing with this kind of microcontroller, there are two distinguished trademarks: FTDI and Cypress. They both offer the possibility to buy either just the controller or an integrated PCB with the microcontroller on-board, allowing a direct connection. Two of the most popular solutions of each one is analyzed. First, regarding FTDI, FT2232H chip is proposed; this chip is easy to program using the official programmer supplied by FTDI, *FTProg.* One of the integrated board with this chip is the genuine one provided by FTDI:



Its cost is 27  $\in$ . It is equipped with a Mini-B USB Connector and needs 5 V supply. Another possibility is using one of the low cost unofficial integrated board; for instance:



Figure 4.14 – Unofficial FTDI FT2232H Integrated Board

It is bigger than the official one and, although both are based on FTDI FT2232H chip, (so the datasheet of the chip is valid for both), there are no information on the pin-out of this one, it would have to be manually made. On the other hand, it costs only  $13 \in$ . Both

options are compatible with USB 2.0 Version so they are valid and satisfy the requirements regarding the connectivity and compatibility with software solutions.

With regards to Cypress, CY7C68013 chip is another possibility. Again, genuine  $plug \ \mathcal{E} play$  boards are available, for example, the one shown in figure 4.15.



Figure 4.15 – Cypress CY7C68013 Integrated Board

It is supplied with 5 V too, Mini USB Connector 2.0 Compatible, and, of course, allows being programmed using official software, *PSoC Programmer*. Its cost is  $15 \in$  and, although it is cheaper than the genuine FTDI integrated module of figure 4.13 it is really hard to find, and its freight cost makes it an inadvisable option.

Among both FTDI options, given that the unofficial is half of the price of the genuine one, and it has been reported to function correctly with the software solution used, **unofficial FTDI FT2233H module is chosen**, see figure 4.14.

Simplified Schematic Functioning of FT2232H in the System can be seen in figure 4.16.

As mentioned, there is no information on this module pinout, so it is obtained by inspection. It is concluded that there is only a nomenclature change in the buses, with respect to the used in the chip for the same function.

#### 4.1.2.3 Supply System

With regards to the supply system, according to the blocks studied before, they are needed 3 different voltage lines: 1 V, 3.3 V and 5 V. In order to have a wider range, it is decided to have a main voltage supply of 12 V; they will be successively regulated to the voltages needed. In addition, 12 V will be the voltage feeding up RF Conditioning block, if needed.

Considering the differences between linear and switching regulators analyzed in 4, given

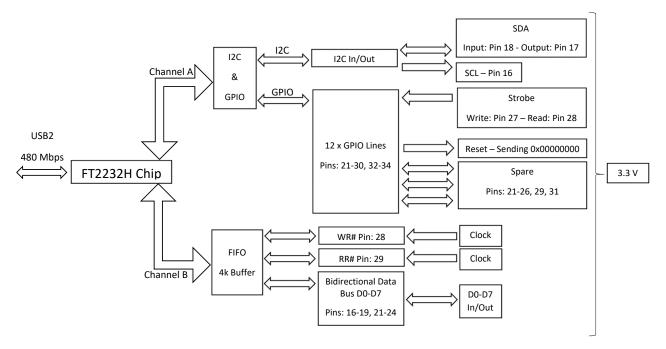


Figure 4.16 – FTDI Simplified Schematic Functioning in the System

that the first step-down stage is the one with the larger step, it is decided to use switching regulator to ensure the highest possible efficiency. After it, several LDO voltage regulator will be used to achieve the voltage needed. If possible, regulators *off-the-shelf* will be used, depending on stock. Firstly, it will be necessary to accurately knowing the consumption of the main components. Once it is known, each consumption will be associated to a voltage line; all these data will allow to determine the peak of current that every single regulator will suffer, and its efficiency. The following table shows the different voltage lines and the components which are connected to them, as well as the current consumption for each one, for the **typical** case:

Voltage Line (V)	Component	Current Consumption (mA)
1 V	NIM	400
$3.3 \mathrm{V}$	NIM	485
$5 \mathrm{V}$	FTDI	300

 Table 4.5 – Voltage Lines with connected components and associated typical current consumption

Once consumptions are known, the supply design can be performed; it will be made in reverse order, from the lowest to the highest voltage, in order to comply with the different Dropout Voltage.

#### • 3.3 V -> 1 V

The last stage is stepping down from 3.3 V to 1 V; 1 V line will feed the tuner, so it will have high consumption. One regulator in stock which might be valid is Texas Instruments LP3879. It allows 1 V fixed output, with 800 mA maximum current and 1.5 V of Dropout Voltage. Therefore, it is a valid option, given that it allows the desired output, and Dropout Voltage is respected, being input voltage 0.8 V superior to it. Current flow and efficiency will be adequately analyzed in *Power Budget*. Its cost is  $1.72 \in$ .



Figure 4.17 – Texas Instruments LP3879-1.0

• 5 V -> 3.3 V

Previous stepping-down stage is from 5 V to 3.3 V. Again, this line of voltage will be used for the NIM. As shown in table 4.5 it is expected to have a moderate current consumption. ON Semiconductor NCP1117DT33G is proposed; it allows 3.3 V fixed output, with 1 A current and 1 V Dropout Voltage. Again, Dropout Voltage is respected, and current allowed is enough. Its cost is 0.376  $\in$ .





Figure 4.18 – ON Semiconductor NCP1117DT33G

• 7.5 V -> 5 V

This is the first stage after the switching regulator, whose output has been chosen to be 7.5 V, so Dropout Voltage of this LDO Voltage Regulator is respected. ON Semiconductor MC7805BD2TR4 is proposed, allowing 5 V output, with 1 A and 2 V Dropout Voltage. As in the previous cases, everything looks, a priori, correct. Its cost is  $0.586 \in$ .



Figure 4.19 – ON Semiconductor MC7805BD2TR4

#### • 12 V -> 7.5 V

The very first regulation stage will be composed, as said before, of a switching regulator. LM2596 Module Board has been chosen because of its versatility and ease of use. It is a high-efficiency adjustable buck switching regulator, allowing up to 3 A output and up to 40 V input voltage; of course, it is more than enough in the matter at hand. Its cost is  $2 \in$ .



Figure 4.20 – LM2596 Module Board

In order to check the regulation chain proposed, power budget for the typical and maximum current consumption will be analyzed. Taking into account 4.5 the power budget diagram of the figure 4.21 can be designed.

In 4.21 the different voltage lines have been considered, as well as the typical current consumptions. From that data, power needed has been estimated for every regulator, and also their efficiencies. The table below the diagram shows the calculations considering the number of elements per PCB and the maximum current allowed by each regulator, as commented before. It must be noticed the generally low efficiencies of the LDO, while the switching regulator exhibits 80 % of efficiency. In conclusion, the supply system proposed comply with the power requirements needed for the typical current consumption.

In the same way, the process can be made for the **maximum** current consumption. The main difference come from the NIM, which according to its datasheet, may increase the current consumption if the Symbol Rate reaches the maximum allowed (45 Ms/s). Table 4.5 would change to:

Voltage Line (V)	Component	Current Consumption (mA)
1 V	NIM	2200
3.3 V	NIM	485
$5 \mathrm{V}$	FTDI	300

As before, power budget diagram is included in figure 4.22.

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										∧ <b>1</b> +		[	4		$P_{1}=1 V \times 0.4 A = 0.4 W$	
	ч	30%	61%	74%	80%	12	3.625	0.30	12 V/1 A	1	Ş	LP3879MR	3.3 V → 1 V (3.3 V-1 V)x400 mA = 0.920 W η=30 %	P <sub>2</sub> =0.92W	2 W	
	P <sub>in</sub> (W)	1.32	2.15	2.9	3.625	V <sub>source</sub> (V)	Power Total (W)	Current Needed (A)	Source Specs 1	17-336 HHE33 HHE33		NCP1117DT33G	$\begin{array}{c} 5 \ V \rightarrow 3.3 \ V \\ (5 \ V-3.3 \ V) X485 \ mA \\ = 0.83 \ W \\ \eta=61 \ \% \end{array} \right. \  \  1.32 \ W$	P <sub>4</sub> =0.83 W	$P_{3} = P_{1} + P_{2} = 1.32 \text{ W}$ I=0.4  A	Figure 4.21 – Power Budget Diagram. Typical Consumption Case.
	(A) I <sub>out</sub> (A)	0.4	0.4	0.43	0.387					+5 <	•	NCP	(5 V-3.1 (5 V-3.1 =	P4-	P <sub>5</sub> = P <sub>3</sub> + P <sub>4</sub> = 2.15 W I=0.43 A	gram. Typical
Typical Consumption Budget	Pout (W) Iout_Max (A)	0.4 1.2	1.32 1	2.15 1	2.9 3					•	an Kan	MC7805BD2TR4	7.5 V $\rightarrow$ 5 V (7.5 V-5 V)x300 mA = 0.75 W $\eta$ =74 %	P <sub>6</sub> =0.75 W	P <sub>5</sub>	er Budget Diag
pical Con	V <sub>in</sub> (V)	3.3	5	7.5	12					5 <		2	<u> </u>		= 2.9 W A	– Powe
Τy	Number/PCB	1	1	1	1	lators				+7.5 +7.5		596	- 7.5 V 0 %	25 W	P <sub>7</sub> = P <sub>5</sub> + P <sub>6</sub> = 2.9 W I=0.39 A	Figure 4.21
	Component	LP3879MR (3,3 V→1 V)	NCP1117DT33G (5 V→3,3 V)	MC7805BD2TR4 (7,5 V→5 V)	LM2596 (12 V→7,5 V)	*Quiescent Current is neglected in LDO Regulators				+12 V		LM2596	$P_{9}=P_{7}/\eta \approx 3.6 \text{ W}$ $\eta = 80 \%$	P <sub>8</sub> =0.725 W		

											:	+ > •				$P_{1}=1 V \times 2.2 A = 2.2 W$	
	L	30%	80%	92%	85%		12	10.4	0.87	12 V/1 A		Ć	LP3879MR	3.3 V → 1 V (3.3 V-1 V)x22 A = 5.06 W η=30 %	P <sub>2</sub> =5.06 W	26 W	e.
	P <sub>in</sub> (W)	7.26	8.09	8.84	10.4		V <sub>source</sub> (V)	Power Total (W)	Current Needed (A)	Source Specs	11-336	Rie33 +3.3 V	NCP1117DT33G	5 V → 3.3 V (5 V-3.3 V)x485 mA = 0.83 W η=90 %	P4=0.83 W	P <sub>3</sub> = P <sub>1</sub> + P <sub>2</sub> = 7.26 W I=2.2 A	Figure 4.22 – Power Budget Diagram. Maximum Consumption Case.
udget	Iout_Max (A) Iout (A)	1 2.2	1 2.2	1 1.618	3 1.179					output		+5 <		M 60.8	P4-	$P_5 = P_3 + P_4 = 8.09 W$ I=1.618 A	agram. Maximum
Maximum Consumption Budget	V <sub>in</sub> (V) P <sub>Out</sub> (W) I <sub>0</sub>	3.3 2.2	5 7.26	7.5 8.09	12 8.84				s would make nec	se the maximum o		J.	MC7805BD2TR4	7.5 $V \rightarrow 5 V$ (7.5 V-5 V)x300 mA = 0.75 W $\eta=74 \%$	P <sub>6</sub> =0.75 W	84 W	ower Budget Di
Maxim	Number/PCB V	1	1	1	1	lators			tion requirements	system, to increas		A 5.74	596	7.5 V )% 8:84 W	M	P <sub>7</sub> = P <sub>5</sub> + P <sub>6</sub> = 8.84 W I=1.179 A	gure 4.22 – $P$
	Component	LP3879MR (3,3 V→1 V)	NCP1117DT33G (5 V→3,3 V)	MC7805BD2TR4 (7,5 V→5 V)	LM2596 (12 V→7,5 V)	*Ouiescent Current is neglected in I DO Regulators			Meeting the maximum consumption requirements would make necessary	a change in the LDO Regulators system, to increase the maximum output current		+12V	LM2596	$P_{9}=P_{7}/\eta \approx 10.4 \text{ W}$ $J_{2} V \Rightarrow 7.5 \text{ V}$ $\eta = 80 \%$	P <sub>8</sub> =1.56 W		Fi

José Carlos Martínez Durillo

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In the table included in figure 4.21 can be seen 3 red cells. They indicate that the maximum current allowed by the regulator has been exceeded. Particularly, the whole LDO Regulator section is saturated when considering maximum consumption case. To support this case, the LDO Regulators should be changed for others which allow larger output current, probably being necessary Through-Hole cases with larger heatsink; in fact, LDO Regulators are not likely to be able support those consumptions rates, at least with a merely decent efficiency. However, considering that ISS TX System transmits using a Symbol Rate of 1.3 Ms/s or 2.3 Ms/s and the Symbol Rate necessary for the NIM to reach the maximum current consumption studied below is 45 Ms/s, the system will never have to support that current, and complying with the typical case is enough. In addition, once again, users of the NIM proposed claim its correct functioning with standard supply. For these reasons, the supply system proposed is accepted as valid. In addition to this voltage regulation chain, capacitors at supply stage are vital for correct functioning. Particularly, on the one hand, LDO regulators as the ones exposed require relatively large capacitors placed at the input and output, to assure stability; this is specially important if they are located at some distance of the power source. These capacitances will enhance the output transient response as well. In these case, 22 µF ceramic capacitor will be used, as recommended in the datasheets. On the other hand, when designing ground return, from any supplied pin, **bypass** capacitors must be used as follows:

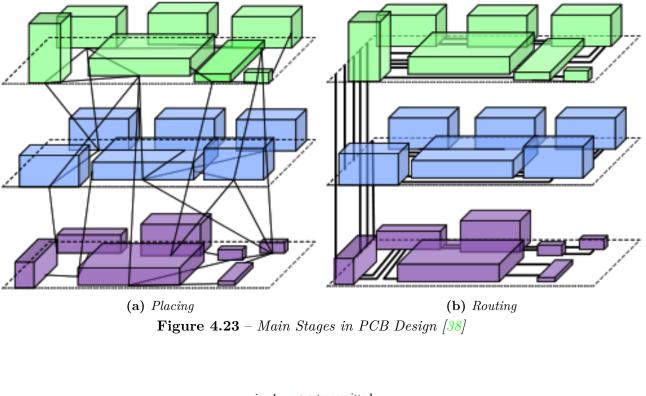
- 100 nF ceramic capacitor will decouple system supply from noise.
- $10\,\mu\text{F}$  electrolytic capacitor in parallel to the previous one, with lower frequency of resonance, will allow keeping stable supply voltage when consumption peaks occur.

In all cases, capacitors must be placed as close as possible to the device involved, to reduce parasitic inductance.

Once the components have been chosen, and the supply system has been validated, it is designed the PCB. As commented before, in the first place, schematic system is designed, which provides a solution for the simple interconnection of the components needed, from the NIM to the FTDI or the different regulators which form the supply system. In sum, these schematics represent by themselves the meeting of the technical requirements.

Once completed, PCB Design is composed of different stages which can be fundamentally arranged into two: *placing* and *routing*.

*Placing* process consists in optimally collocating, onto the PCB surface, the components which are part of the design. This process must optimize not only the surface used, (to save money), but also allowing an adequate routing in matters of EMC, keep traces short, and the rest of *good practices* when designing PCB. Regarding *routing* process, it starts after finishing placing, and it supposes making the connections between the different components; it is a crucial step which can determine the functionality of the system, with countless factors to take into account. Unpredictable behaviors, radiating areas, impedance mismatching or noise generation can occur as a result of deficient traces; prevent designs from those undesired effect is known as keeping **signal integrity** and figure 4.24 illustrates it.



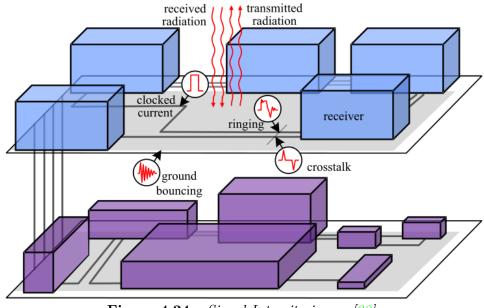
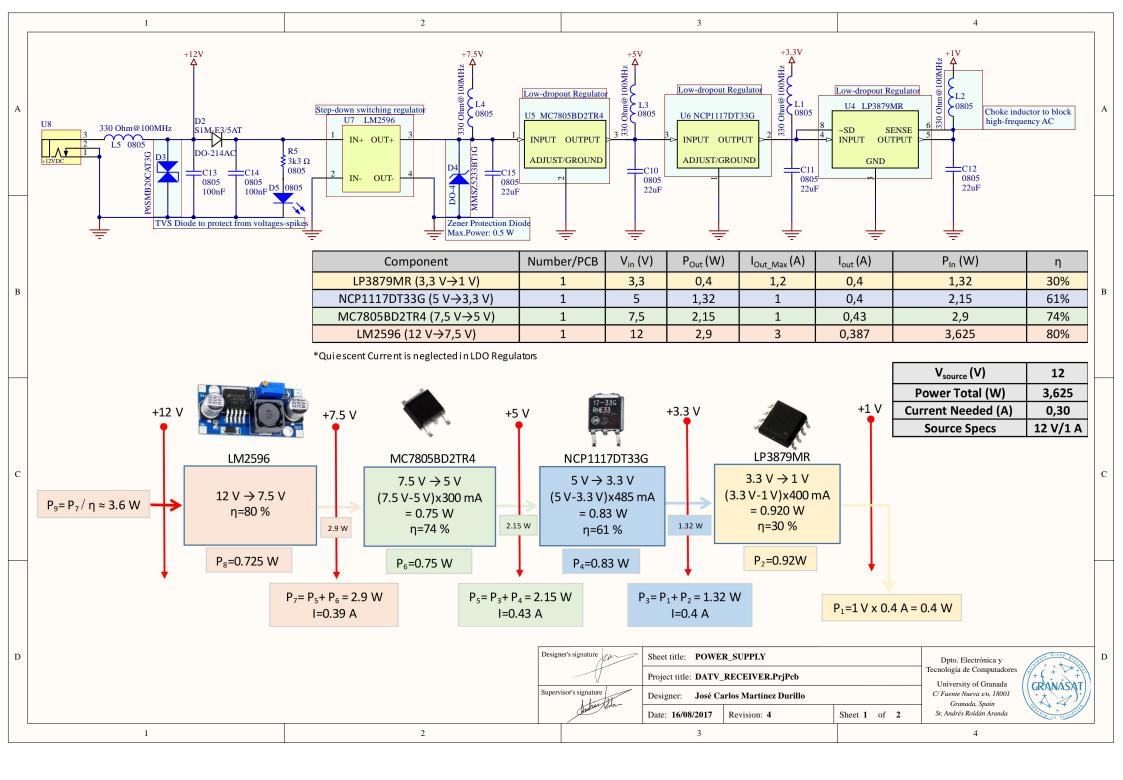


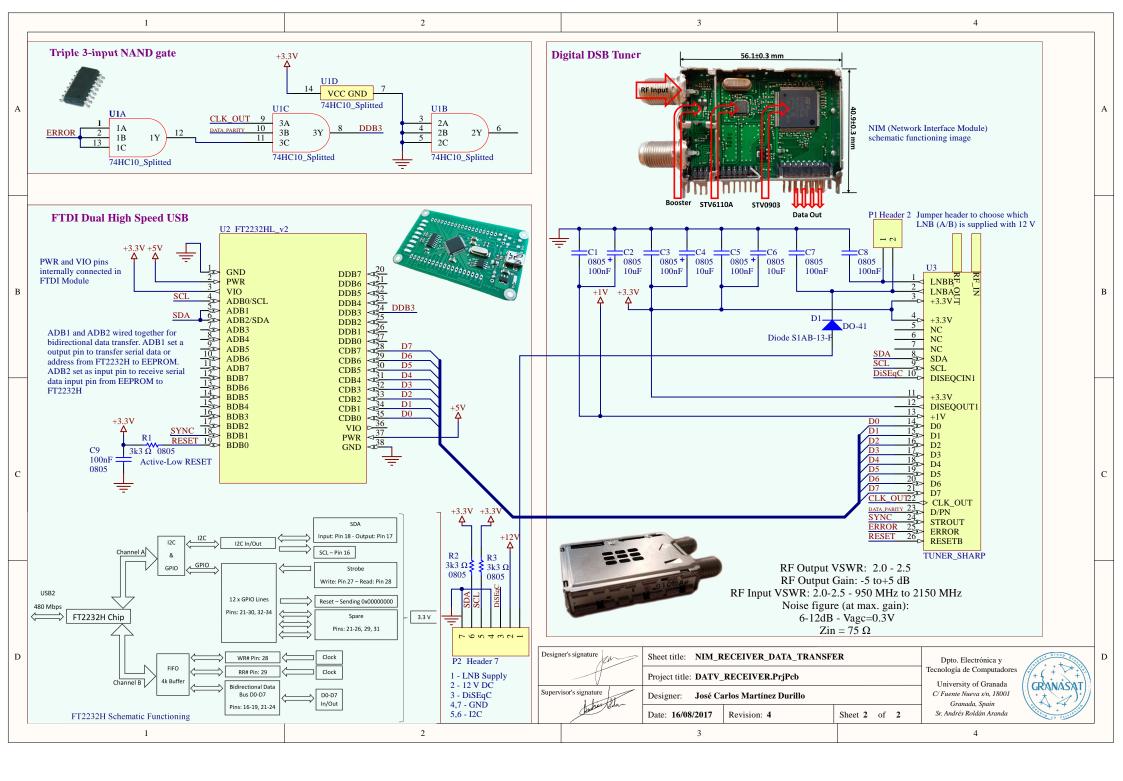
Figure 4.24 – Signal Integrity issues [38]

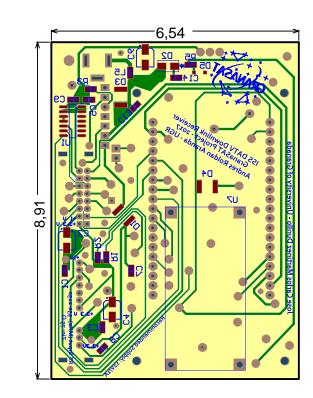
Every design must comply with some *Design Rules* due to manufacturing constraints. They vary depending on how the PCB is manufactured, for instance, a common technique for prototyping is **milling**. For this project, an automatic CNC Machine, LPKF ProtoMat S62 [51], will be used for the first prototype. Their constraints are stronger than the ones found when using chemical etching, and are mainly related with the following concepts:

- **Traces**: Traces should be the minor length possible, maximizing width to avoid resistive behaviors, especially in supply traces, to allow the current needed for the system to go through them.
- **Clearance**: It is defined as the separation between two elements of the design: traces, drills, components, etc. In case of using milling techniques, this comes from the minor milling cutter diameter. In the machine available, it corresponds to 8 mils or more. In case of chemical etching, this separation is even less.
- **Drills**: Any hole which goes through the laminate is known as drill. Again, possible diameters depend on the available milling cutters, which in the machine at hand are 0.6, 0.7, 0.8, 0.9, 1.1, 1.3 y 1.5 mm.
- Annular Ring: It is the area which surrounds a drill when it needs to be soldered. The only constraint regarding them is that they should be large enough to allow soldering.

In addition, given that serigraph tools are not available, desired text must be directly drilled onto the laminate. Considering these limitations, the PCB is designed and improved following an iterative process which consists of **6 versions**. The following pages show the result.







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## **BOTTOM LAYER**

2

# **DATV PCB Receiver**

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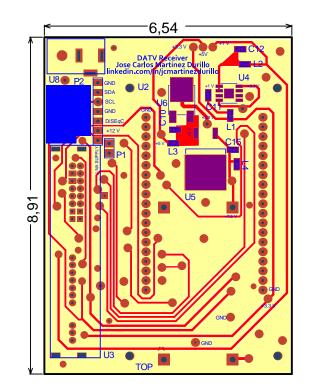
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This PCB acts as intermediary between RF Front-End of the System and a PC.

NIM should be connected to a mixer with IF between 950-2150 MHz, (F-Connector IN). Pre-amplification is expected to be needed.

Recommended Supply: 12 v/1A

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		Designer:	José Carlos Martínez Durillo		GranaSAT	
		Supervisor:	Andrés Roldán Aranda		Date: 09.08.2017 Revision: 6 Sheet 1 of 1	
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## **TOP LAYER**

# **DATV PCB Receiver**

This PCB acts as intermediary between RF Front-End of the System and a PC.

NIM should be connected to a mixer with IF between 950-2150 MHz, (F-Connector IN). Pre-amplification is expected to be needed.

Recommended Supply: 12 v/1A

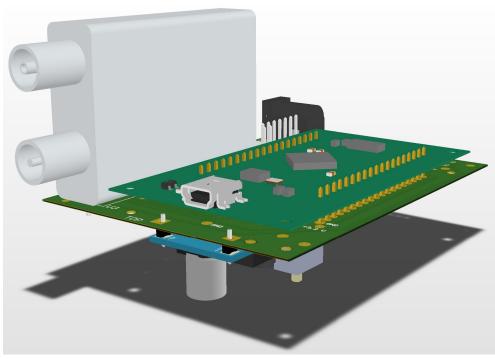
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	Designer: José Carlos Martínez Durillo	Granada, Spann GranaSAT	
	Supervisor: Andrés Roldán Aranda	Date: 09.08.2017 Revision: 6 Sheet 1 of 1	
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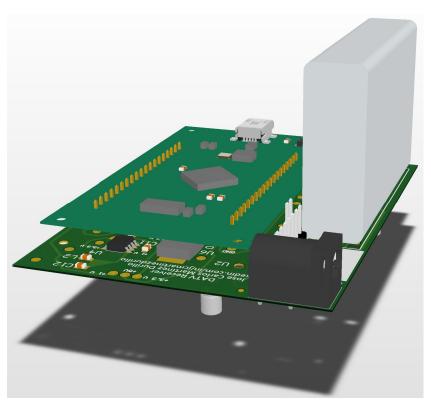
Some aspects which deserve to be remarked regarding the design are:

- Both Top Layer and Bottom Layer are shown. Top layer tracks are depicted in red, whereas ground layer tracks are shown in green. In the same way, silkscreen and text layers are shown, which allows seeing components footprints.
- Supply System has been implemented as studied in 4.1.2.3. LM2596 Module steps down from 12 V from 7.5 V, voltage which is then successively stepped-down to the voltage needed in every line, using LDO Regulators.
- As mentioned, decoupling capacitors have been placed as close as possible to the IC, to prevent inductive behaviors.
- Size of traces involved in Supply System have been maximized to avoid resistive behaviors, trying to keep 25 or 30 mils width in them. In addition, small area **power planes** have been used around supply when possible. It helps to stabilize voltage and allows greater current to go through the conductor.
- Several headers which allow feeding up the antenna, as well as choosing which LNB is supplied, have been included.
- Ground Planes in Top Layer and Bottom Layer (in yellow) have been used. Using ground planes instead of traces allows lower impedances, functioning as current return path and voltage reference. It also minimizes capacitive coupling and Ground Bouncing. In addition, ground vias have been added along the whole PCB, connecting both ground planes and allowing a bigger and stable reference to ground. It also prevents PCB to present large isolated areas which could radiate energy as an antenna would do.
- As studied in Chapter 3, SMD package has been chosen for every possible component. Therefore, there are only three Through-Hole devices, excluding headers. This fact supposes an easier fabrication.
- Test Points for voltage checking have been included. They will be useful during soldering to check the correct functioning of the supply system.
- Mechanical Holes are included, coinciding with the FTDI ones. They provide mechanical strength and allow using screws in a hypothetical package.

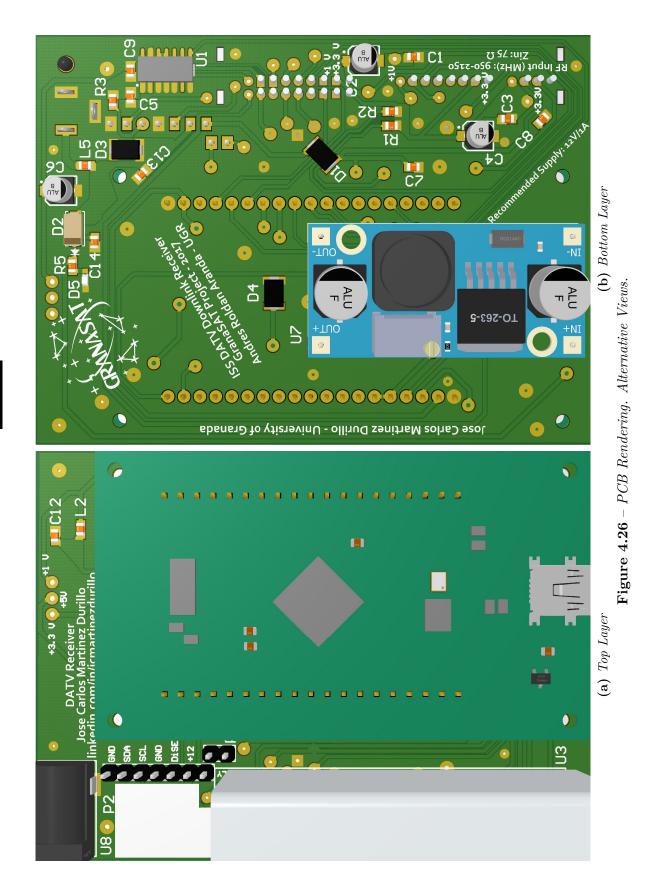
In the same way, during PCB design, 3D models of each one of the components are included and considerated. It allows having a very realistic approximation of the final result. Besides, it permits detecting mechanical issues, due to collisions between components because of their heights or any other characteristic. Figure 4.25a shows 3D final rendering, whereas figure 4.26a and 4.26b shows details and different views. Finally, the result is depicted with a video, 4.1 (double click when viewing with Adobe Reader).



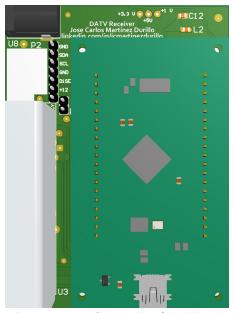
(a) Front.



(b) Rear. Figure 4.25 – PCB Final Version



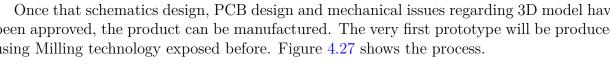


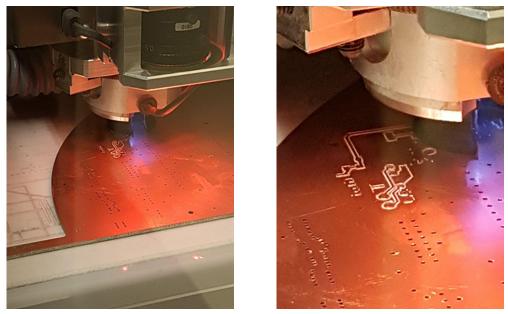


Video 4.1 – PCB Video (double click)

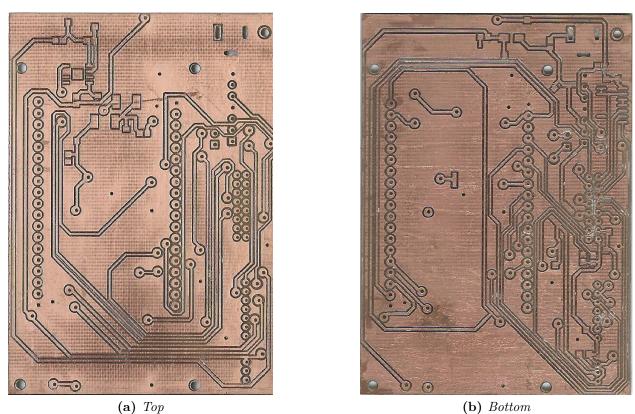
#### 4.1.2.4Manufacturing

Once that schematics design, PCB design and mechanical issues regarding 3D model have been approved, the product can be manufactured. The very first prototype will be produced using Milling technology exposed before. Figure 4.27 shows the process.





(a) (b) Figure 4.27 – Manufacturing process using LPKF ProtoMat S62



The result is shown in figure 4.28.

Figure 4.28 – Manufactured PCB using milling technology

As mentioned before, this technology does not allow neither serigraph nor surface finish, as it would be obtained through chemical etching; however it is absolutely right as a prototype. For the same reason, it is needed to varnish the PCB with a mixture of colophony and acetone. This varnish prevents PCB from oxidation, as well as easing soldering. After it, tracks connectivity is checked; although it seems to not to exist any effective shortcircuit, some tracks do not exhibit the clearance expected and they suppose potential shortcircuits. After studying the board, it is attributed to the bits condition. However, the main components are soldered and the functioning is correct.

After checking the prototype, because of designer will, the PCB is sent to be manufactured to a professional PCB manufacturer. Given the differences between both manufacturing process, the constraints regarding clearance, drilling diameters and so forth change; nevertheless, the new constraints are soft than the milling ones, so there no is actual need to change the design. However, drill diameters is reduced, and the width of some tracks is changed in order to avoid the problems exhibited by the prototype.

Once the PCB has been optimized for the manufacturing process it is ordered, resulting

in the product shown in figure 4.29. Differences between milling prototype and this one are easily noticeable, vias are already metallized, solder mask has been applied (responsible for the characteristic green colour), and text are silk-screened. Apart from the aesthetic aspect, the manufacturing process followed to produce the PCB eases soldering substantially. Again, connectivity is verified, and the components are soldered. Final product is shown in figure 4.29.

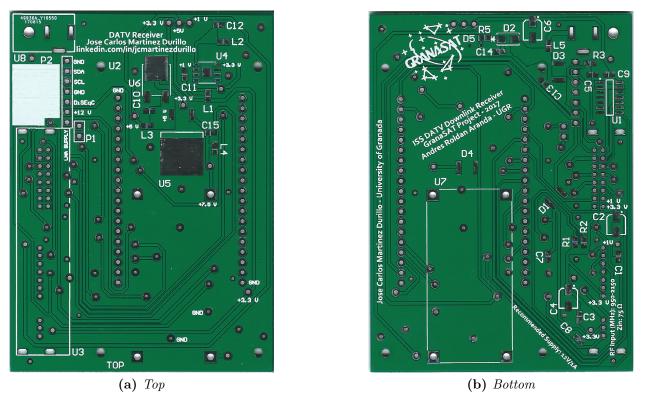


Figure 4.29 – Manufactured PCB using chemical etching

#### 4.1.3 RF Conditioning

Once that *PCB Receiver* block has been designed, it can be studied if it is necessary an *RF Conditioning* block. Keeping in mind equation 3.1.13 and considering that the chosen NIM exhibits a sensitivity of -65 dBm it is clear that a Pre-Amplification Stage is needed to reach that power. In addition, input frequency range of the proposed NIM do not include the frequency of work, (2400 MHz), so a mixing stage will be also needed. It can be concluded that it is definitely needed an *RF Conditioning Block* which adequately adapts the signal for the tuner. Again, this block can be subdivided in the blocks said before.

# 4.1.3.1 Pre-Amplification Stage

Right after reaching the receiving antenna, the signal is extremely weak and needs to be quickly amplified before going trough the rest of the system. This is the purpose of the **pre-amplification stage**. It is normally implemented as an LNA. In this kind of devices, it is vital, apart from exhibiting high gain, not to significantly degrade the signal to noise ratio, (what is known as having a low **noise figure**), given that the overall noise figure of the system is usually dominated by the first stage of the receiver's Front-end. Some commercial LNA are compared.

The first commercialized LNA proposed is **KUHNE LNC 23 TM** [18], shown in figure 4.30.



Figure 4.30 – KUHNE LNC 23 TM

This device acts not only as amplifier, but also as mixer, so it is what is called LNC. Therefore, this device could be also valid for the next section, 4.1.3.2 about mixing. Its main specifications are shown in table 4.7.

Parameter	
Input Frequency Range (MHz)	2320 -2450
Intermediate Frequency Range (MHz)	1404 - 1534
Noise Figure @ 18°(dB)	0.7
Gain $@25^{\circ}(dB)$	40
Input connector/Impedance $(\Omega)$	N-female, 50
Output connector/Impedance $(\Omega)$	F-female, 75
Supply Voltage (VDC)	9-18 V

 Table 4.7 – KUHNE LNC 23 TM Specifications

This LNC exhibits high gain and extremely low noise figure, even output connector is matched to the usual input impedance of tuners (75  $\Omega$ ). It is a built-in, really functional solution. It has, however, a high price: 216  $\in$ .

Another possibility is Pasternack PE15A1010. The main difference between this one and Kuhne's is the bandwidth; while the latter is a narrow-band amplifier (in this sense, it is designed from the mixer perspective), the Pasternack one works in the band of 2-6 GHz, exhibiting 40 dB gain in the whole range, and noise figure below 1 dB. Its performance can be undoubtedly be qualified as exceptional. It is achieved through the use of advanced GaAs pHEMT. Detailed specifications are shown in table 4.8.



Figure 4.31 – Pasternack PE15A1010

2000 - 6000
0.9
40
SMA, 50
SMA, 50
+14
12

 Table 4.8 – Pasternack PE15A1010 Specifications [27]

Given the greater bandwidth, besides its outstanding specifications, its price is significantly higher than Khune's, 770  $\in$ .

The choice is significantly influenced by the mixer selected: middle-gain LNA will require higher conversion gain in the mixer, and viceversa, high-gain LNA will require lower conversion gain in the mixer. Of course, antenna gain must also be taken into account. It must be remarked again the aim of the amplification: **reaching the** 

minimum sensitivity of the NIM. At this point, and given that KUHNE LNC 23 TM complies with the frequency translation needed for the NIM, it is possible to show the first blocks diagram of the system; particularly, the *one* shown presents devices which have been already analyzed and which correspond to the global solution recommended by ARISS organization to receive DATV signal. In addition, RF power balance has been included in the diagram, from the estimated received power to the NIM; although it exposes the ideal case, with perfect matching conditions at all points and negligible cable and Insertion Losses, it allows showing how the power goes increasingly high as passes through the system, surpassing the required sensitivity. On the other hand, the cost of this solution (687  $\in$ , assuming availability of a PC at least) makes it unaffordable for the majority of the schools, as explained in Chapter 1.

Obviously, none of the options above look valid for the design of this cost-oriented system, specially the Pasternack one. Therefore, it is decided to opt for a low-cost LNA which assures low **noise figure**, and moderate gain. By using reduced length cable between RX Antenna and LNA, the power reduction of the signal would be small enough to be compensated at the amplification stage of the **mixer**. On the other hand, as mentioned before, given that the LNA will be part of the **RF Front-End** it is important to exhibit a low noise figure, as the first stage dominates the noise figure of the whole system. One of the best options in the market for this low-cost sector is [20]. It is an economical preamplifier in the frequency range of 28-2500 MHz which exhibits a gain 11 dB @ 2.4 GHz. It is based on Mini-Circuits PSA4-5043+ [26]. Further specifications are shown in table 4.9

Parameter	
Input Frequency Range (MHz)	28 - 2500
Noise Figure (dB)	1
Gain $@$ 2.4 GHz (dB)	11
Input connector/Impedance ( $\Omega$ )	SMA, 50
Output connector/Impedance ( $\Omega$ )	SMA, 50
Output at 1 dB Compression Point (dBm)	+21
Supply Voltage (VDC)	6 - 9

 Table 4.9 - LNA4ALL Specifications



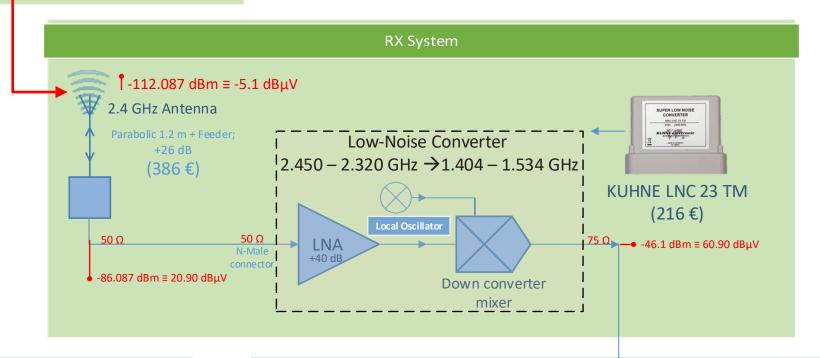
Figure 4.32 – LNA4ALL

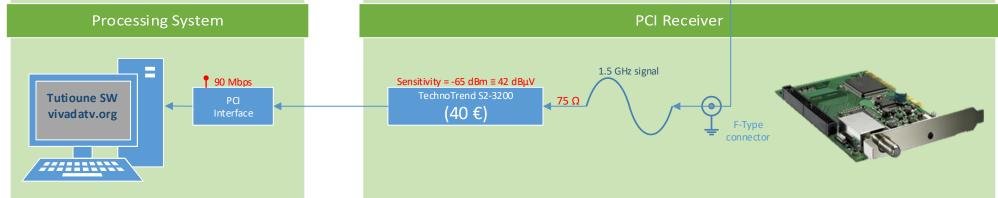
# TX System

TX data Freq=2.395 GHz DVB-S like signal Symbol rates: 1.3 Ms/s, 2.0 Ms/s FEC : ½ Video PID = 256 Audio PID = 257 RF radiated power : 10 W EIRP Patch Antennas RHCP Polarized

This project aims to develop a fully-integrated system to receive the DATV Signal from the ISS Downlink. More expensive systems than the one developed have been proposed before. Particularly, herein is shown the one recommended by the ARISS organization.







## DATV Receiver for ISS Downlink

Given that noise figure is also acceptable, 1 dB at frequency of work, and its price is  $20 \in$ , it is selected to be the LNA at the RF Front-End.

### 4.1.3.2 Mixer

As studied in Chapter 3, mixers are common devices when dealing with satellite down-links. Its design is not trivial at all, given the number of factors to take into account. This section will be approached following the same methodology applied before, commercialized options will be analyzed first; if feasible, a proper design will be suggested. It must be reminded that the first option has been proposed in the previous section, KUHNE LNC 23 TM, given its double functionality.

### 4.1.3.2.1 DG0VE KON13-900 Analisys and Measurement Setting-up

As preceding step to design a new mixer, a process of **reverse engineering** will be applied to a commercialized mixer. Particularly, the analyzed one is manufactured by the German DG0VE [11], model KON13-900. Technical information available is composed of the schematics and layout; the latter is shown in figure 4.33 whereas the datasheet is included here. Several blocks have been included as part of the reverse engineering process, to make clear the structure followed in that design.

Parameter	
Input Frequency Range (MHz)	2320 -2450
Intermediate Frequency Range (MHz)	1420 - 1550
Noise Figure @ 18°(dB)	1.9
Gain $@25^{\circ}(dB)$	58
Input connector/Impedance ( $\Omega$ )	N-female, 50
Output connector/Impedance ( $\Omega$ )	F-female, 75
Supply Voltage (VDC)	12-18 V

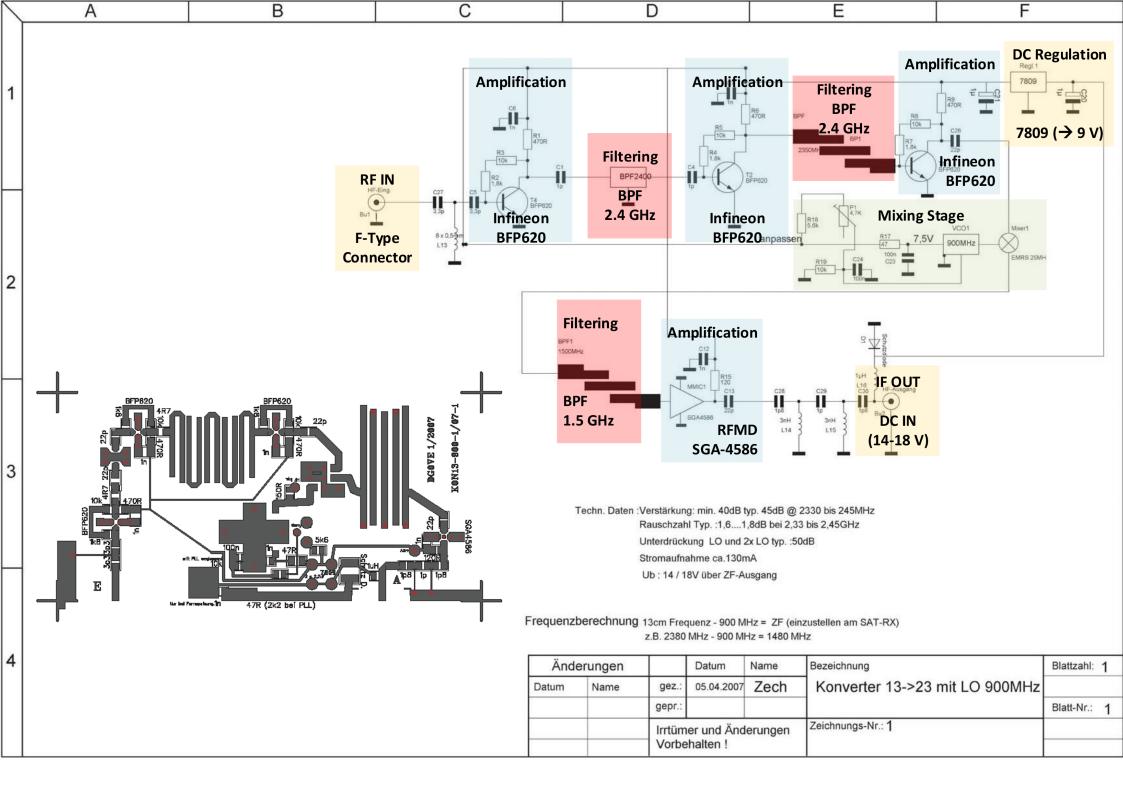
The main specifications of this mixer are presented in table 4.10.

 Table 4.10 - DG0VE KON13-900

It can be seen that, theoretically, DG0VE KON13-900 exhibits higher gain, but also higher noise figure with respect to Khune LNC 23 TM. It is designed using Microstrip Technology and its cost is 90  $\in$ , significantly lower.

Before studying DG0VE KON13-900 in detail, it is measured using a VNA. Figure 4.34 shows the setting-up necessary to perform the measurement.

Given that the mixer is not under an operation environment, it is necessary to assembly



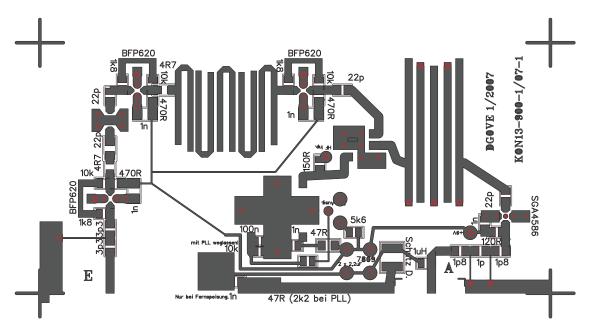


Figure 4.33 – DG0VE KON13-900 Layout



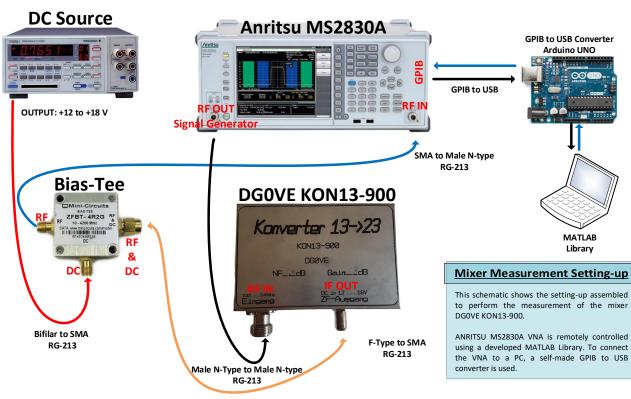


Figure 4.34 – Measurement setting-up needed

an scenario which allows reproducing the actual situation, i.e., an RF signal is needed as input, and DC Signal is needed to supply the mixer. For those reasons, a Bias-Tee, as the one shown in figure 4.34 is needed. A Bias-Tee is a three-port network widely used to set the DC bias point in electronics devices. It allows passing DC signal without disturbing RF signal. On the other hand, the VNA used is able to generate a signal at a desired frequency, with a certain power. Figure 4.34 also shows the different cables used for the setting-up, including end-connectors and type (USB, coaxial...). Coaxial wire used is Flexible RG58, with 50  $\Omega$ impedance. As every coaxial, their losses increase with frequency; therefore, it is necessary to *calibrate* the cable, i.e., knowing its behavior in frequency. To perform that calibration,  $S_{12}$ parameter is measured in a 2 m piece of the cable used, using Agilent E5071C. It is analyzed in the expected range of functioning, from 100 MHz to 3 GHz; the results are shown in figure 4.35.

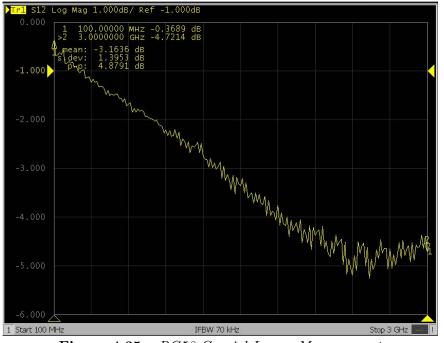


Figure 4.35 – RG58 Coaxial Losses Measurement

As anticipated, losses increase with frequency. At 100 MHz, 0.37 dB of losses are measured, whereas 4.72 dB are measured at 3 GHz. Although they are relatively higher, considering Insertion Losses of the connectors, (approximately 1 dB each) they can considered acceptable for this wire. Consequently, it will be used to measure the mixer.

## 4.1.3.2.2 Anritsu MS2830A MatLab Library Development and Measurement

The only factor left is a way to efficiently control the Anritsu MS2830A VNA and also to receive data from it. It is achieved by using a GPIB to USB converter; because of the

extremely high cost of these, a self-made one is used, based in an Arduino UNO. Regarding the software used to control the VNA, a MATLAB<sup>®</sup> library is developed. Previously, some **Software Requirements** can be stated:

- Capability to establish an effective Serial Communication between a PC and the Anritsu MS2830A, making use of the GPIB to USB Converter.
- Capability to choose the instrument of the Anritsu MS2830 to be controlled, Spectrum Analyzer, Signal Analyzer or Signal Generator.
- Capability to set the main parameters necessary to use the VNA, such as frequency, span or markers.
- Capability to transfer a certain trace to a PC, using the GPIB to USB Converter.
- Capability to automatically search and indicate with markers the main peaks of the measurement is also desirable.

The first step to remotely control Electronics Instrumentation using a GPIB interface and MATLAB<sup>®</sup> is establishing a *serial* communication. It sets *data rate*, *parity*, termination character and timeout of the communication, as well as other parameters. The piece of code in charge of these function is shown below.

# Serial Communication Establishment Code

```
switch command
 1
 ^{2}_{3}
                           %Case 'open'. Sets the information needed for the GPIB
%Comunication. Initially, no need to change for this instrument.
 \frac{4}{5}
                                     case 'oper
                                             serialPort = instrument.serialPort;
serialObject = serial(serialPort, 'baud', 115200,'StopBits',1,'DataBits', 8,
'Parity', 'none', 'InputBufferSize',100000,'OutputBufferSize',1000); %
set(serialObject,'Terminator','LF');
set(serialObject, 'Timeout',900);
fopen(serialObject);
nerres(0,5);
 \frac{6}{7}
8
9
10
                                             pause(0.5);
fwrite(serialObject,uint8(sprintf('++addr %d\r\n',instrument.addrGPIB)));
fwrite(serialObject,uint8(sprintf('*CLS\r\n')));
pause(0.5);
\frac{11}{12}
13 \\ 14
15 \\ 16
                           %%Case
                                           'close '. Close GPIB Comunication.
17
                                    case
                                             fclose(serialObject);
delete(instrfind);
18
19
```

Usually, when communicating with electronics instruments, these expect to receive pre-defined commands which correspond to a function allowed by their systems. These commands are often listed in the device's documentation, in the case of Anritsu MS2830A, it is available in their website [4].

Once established the link between MATLAB<sup>®</sup> and the VNA, it is necessary to study the functions required and search for the appropriate commands. In the case in hand, there will be necessary to control functions of both *Signal Generator*, and *Spectrum Analyzer*. For example, figure 4.36 shows the expected command to set the frequency of the Spectrum Analyzer.

Chapter 2 SCPI Device Message Details		
[:SENSe]:FREQue Start Frequency	ncy:STARt <freq></freq>	
Function	This command sets t	the start frequency.
Command	[:SENSe]:FREQuer	ncy:STARt <freq></freq>
Parameter	<freq> Range [MS269xA] [MS2830A]</freq>	Start frequency -100 MHz to 6.0499997 GHz (MS2690A) -100 MHz to 13.5999997 GHz (MS2691A) -100 MHz to 26.5999997 GHz (MS2692A) -100 MHz to 3.6999997 GHz (Option 040) -100 MHz to 6.0999997 GHz (Option 041)

Figure 4.36 – Example of Anritsu MS2830A command from datasheet [4]

Following that methodology, it is coded and documented a MATLAB<sup>®</sup> function to control the instruments of the VNA needed. It is available to be downloaded at [41]. Particularly, the following functionalities are programmed (some pieces of code are included as reference):

• Set Signal Generator, Spectrum Analyzer or Signal Generator as used Instrument.

# Spectrum Analyzer Selection Code

1	778 Spectrum Analyzer Setting up:
2	
3	spectrum.center=1679630; %Center Frequency
4	spectrum.units=signal.units;%Frequency units
5	spectrum.start=810.000; %Start Frequency
6	spectrum.stop=2549.260; %Stop Frequency
$\overline{7}$	spectrum.reflevel=10; %Reference Level
8	spectrum.powerUnits='DBM'; %Power units for Reference Level
9	<pre>spectrum.points=101; %Points number for the displayed trace. OPTIONS:</pre>
	11, 21, 41, 51, 101, 201, 251, 401, 501, 1001, 2001, 5001, 10001
10	
11	%Now the function "Anritsu_MS2830A_V01" is used, to send the spectryum analyzer
	configuration to the case "set_SpectrumAnalyzer"
12	Anritsu_MS2830A_V01(instrument,'set_SpectrumAnalyzer',spectrum);

- **Peak Search**, which allows performing an automatic search of the signal received in the Spectrum Analzyer.
- Trace Query, to request the VNA to send the trace on screen to the PC, via GPIB.
- Marker Settings, to remotely control the characteristics of a particular marker, such as width, center peak and others.

# Automatic Main Peak Detection and Centering Code

```
Case 'center_peak'. Sets the spectrum analyzer so the main peak \% is played. It is calculated through a for loop with 3
%Case
 %%iterations
 %(PAGES REFERENCE TO SPECTRUM ANALIZER REMOTE MANUAL:)
 %INST SPECT - Sets the instrument which is goint to receive the string
 %CALC:MARK:AOFF - P16
%CALC:MARK:ACT - P115
                             P160
%CALC:MARK:ACT - P115
%CALC:MARK:RES PEAK - P147
%CALC:MARK:MAX - P171
%CALC:PMAR:Y? - P158
%CALC:MARK:X - P121
%CALC:MARK:WIDT? - P140
%\r\n - Compound string is send after them.
 case 'center peak'
       clc
       for i = 1:3
       pause(1);
fwrite(se
pause(1);
                   serialObject , uint8(sprintf('INST SPECT; CALC:MARK:AOFF\r\n')));
       fwrite(serialObject,uint8(sprintf('INST_SPECT; CALC:MARK:ACT_ON; CALC:MARK:
RES_PEAK; CALC:MARK:MAX\r\n')); %; CALC:PMAR:Y?
        pause(1);
                     ,
serialObject,uint8(sprintf('INST_SIGANA; SYST:COMM:GPIB:SELF:DEL_LF
       \r\n'));
fwrite(serialObject,uint8(sprintf('INST SPECT; CALC:MARK:X?\r\n')));
fcenter=fscanf(serialObject);
       function (control of solution);
pause(1);
fcenter=str2double(fcenter)
fwrite(serialObject,uint8(sprintf('INST SPECT; CALC:MARK:WIDT?\r\n')));
        pause(1);
       marker_span=fscanf(serialObject);
        \underline{\text{pause}}(1);
        marker_span=str2double(marker_span)
        f0=fcenter-marker span
        fl=fcenter
        f2=fcenter+marker span
       First Center Finance: span
fwrite (srialObject, uint8(sprintf('INST SPECT; FREQ:START %.0f HZ; FREQ:
CENT %.0f HZ; FREQ:STOP %.0f HZ\r\n',f0,f1,f2)));
       pause(1.5);
        end
```

- Initial setting-up of the instruments, frequency range, power reference level, number of peaks, trace desired, number of points for the trace and others.
- Finally, a **main script** is developed to allow setting the functions mentioned before easily.

Because of the nature of the interface used for the communication, it must be remarked the need of waiting some time after each instruction is sent; other way, interface will saturate and communication will be lost. This is the reason why the *pause* instruction is often included. All the Software Requirements given have been met.

After the assembly of the setting-up shown in figure 4.34, and the connection with MATLAB<sup>®</sup>, the measurement of the mixer is performed using the library exposed before. Firstly, the generator is set to produce a 2.4 GHz signal, with a power -42 dBm, which is a reasonable power for the actual signal received at the mixer, as seen in previous sections. The output obtained is shown in figure 4.37.

78

2 3 4

 $5 \\ 6 \\ 7 \\ 8 \\ 9$ 

18 19

 $\frac{20}{21}$ 

 $\frac{22}{23}$ 

 $\frac{24}{25}$ 

26 27

28

30

36

37

38

39

40

41 42

43

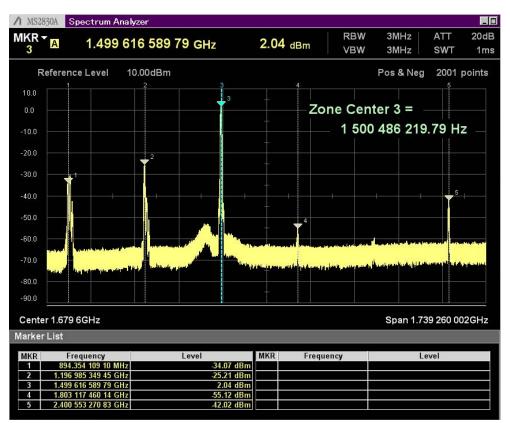


Figure 4.37 – DG0VE KON13-900 Output with 2.4 GHz @ -42 dBm signal input.

The markers allows detecting easily the output peaks produced by the mixer. They are summarized in table 4.11.

MKR Number	Frequency (GHz)	Power Level (dBm)
1	0.894	-34.07
2	1.196	-25.21
3	1.5	2.04
4	1.803	-55.12
5	2.4	-42.02

 Table 4.11 – Markers shown in figure 4.37

Then, at the output of the mixer, the largest peak corresponds to the expected IF frequency, at 1.5 GHz, with 2.04 dBm. However the presence of the rest of the peaks correspond to **intermodulation products**, are undesired and known as **spurious**; they must be studied in order to determine its possible influence in the system. On the one hand, peaks at 0.894 GHz (LO signal) and 2.4 GHz (RF Signal) are not a problem because they are not included in the NIM bandwidth, as analyzed in 4.1.2.1. Regarding the 1.8

GHz harmonic,  $(2 \cdot \text{LO signal})$  it falls within NIM bandwidth, however its power is close to the sensitivity limit, -55 dBm. Even so, it must be considered. Finally the only undesired peak left is the one at 1.2 GHz, with -25 dBm. Therefore the side bands of the desired frequency should be removed, normally with filtering.

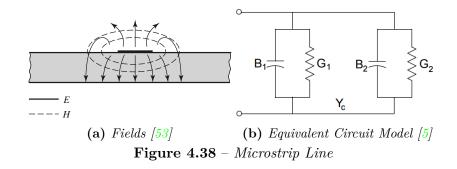
To complete the measurement, 1 dB Compression Point is studied, concept which was introduced in 3.1.2.4.1. As studied, in case of mixers, it is usually given as a function of input power. For DG0VE KON13-900, this point is reached with an input power of -35 dBm.

#### 4.1.3.2.3 Mixer Design

Once DG0VE KON13-900 has been analyzed, an alternative design is proposed as part of the System. Previously, the substrate to be used will be theoretically and experimentally analyzed. Then, the first version of the mixer will be designed using ADS<sup>®</sup> schematics. Firstly, different component alternatives will be analyzed for each one of the blocks appreciated in the studied mixer. When the BOM is completed, the schematic will be composed and simulated. Finally, if simulation succeeds, a layout will be proposed.

# 4.1.3.2.3.1 Substrate Analysis

The first step in microwave design implying Microstrip Technology as the one in hand is conveniently analyze the available substrate to manufacture the design. In this case it is an standard glass fiber, FR4 substrate whose datasheet is not available. When designing Microstrip Technology, one of the most important parameters of the design is substrate Relative Permittivity. Microstrip lines, (whose equivalent circuit model is shown in figure 4.38b), function in Quasi-TEM Mode, because two different mediums coexist: the substrate itself and the air. Although the majority of the fields stays at the substrate, some of them fall in the air, as shown in figure 4.38a.



Because the fields do not keep totally confined in the substrate, Relative Permittivity given by the manufacturer of the substrate is not completely valid, as it does not represent the actual situation. It makes necessary to define a new parameter which allows taking that fact into account, increasing accuracy of the design. This parameter is called **Effective Permittivity** and it can be calculated with the expression shown below.

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12\frac{H}{W}}}$$
(4.1.2)

Therefore, effective permittivity depends on both, Relative Permittivity and physical dimensions of a certain Microstrip Technology line. In the case of FR4 substrate, Relative Permittivity is usually in the range of 4. However, instead of using the equation shown above, effective permittivity will be **experimentally** measured. To do this, VNA Agilent E5071C and a piece of the available substrate will be used. The foundations behind the following measurement is approximating a piece of laminate to a rectangular *open-sided* **waveguide**, measuring the effective permittivity by analyzing the reflections produced when a signal goes through the substrate [12]. FR4 available is a two faces substrate, with 35 µm of copper and 1.575 mm of thickness. As reference, figure 4.39 shows technical specifications of an standard BUNGARD FR4 substrate, (not the one available).

Technical data StandardOriginal Bungard presensitized base material FR4 with UV blocker IPC 4101APropertyTest method IPC-TM-650 or as notedSpecificationUnitsTypical ValueGlass Transition Temperature (Tg) by DSC, spec. Minimum2.4.25110-150°C150Decomposition Temperature (Td)ASTM D3850-°C320CTE, Z-Axis CTE, X-Y-Axispre TG2.4.24ABUSppm"C15CTE, X-Y-Axispre TG2.4.24-ppm"C15CTE, X-Y-Axispre TG2.4.24ABUSppm"C15CTE, X-Y-Axispre TG2.4.24-ppm"C15CTE, X-Y-Axispost TG2.4.24-ppm"C15Thermal Conductivity-ASTM D59304.8Thermal Stress 10s @ 288'C spec maximumetched2.4.13.1Pass visualRating RatingPassSpec maximumB. @ 100 MHz2.5.5.54.6C. @ 1 GHz2.5.5.50.015Spec maximumB. @ 100 MHz2.5.5.50.015Spec maximumB. @ 100 MHz2.5.5.50.015Spec maximumB. @ 100 MHz2.5.5.50.015Spec maximumB. @ 100 MHz2.5.5.50.015Spec maximumA. @ 1 MHz2.5.5.50.015Spec maximumA. @ 1 GHz2.5.5.50						
IPC-TM-660 or as noted       Glass Transition Temperature (Tg) by DSC, spec. Minimum       Decomposition Temperature (Td)     ASTM D3850     -     "C     320       CTE, Z-Axis     pre TG     24.24     ABUS     ppm"C     15       CTE, Z-Axis     post TG     24.24     ABUS     ppm"C     15       CTE, X, Y-Axis     post TG     24.24     ABUS     ppm"C     15       CTE, X, Y-Axis     post TG     24.24     -     ppm"C     15       CTE, X, Y-Axis     post TG     24.24     -     WMK     0.36       Thermal Stress 10s @ 288°C     unetched/     24.13.1     Pass visual     Rating     Pass       Permittivity,     A. @ 1 MHz     2.5.5.3     5.4     -     4.8       spec minimum     B. @ 100 MHz     2.5.5.5     -     -     0.015       Loss tangent,     A. @ 1 MHz     2.5.5.5     -     -     0.015       Spec maximum     B. @ 100 MHz     2.5.5.5     -     -     0.015       Spec minimum     A. @ 1 MHz     2.5.5.5     -     -     0.015       Spec minimum     A. @ 1 MHz     2.5.5.5     -     -     0.015       Spec minimum     A. @ 1 MHz     2.5.6.6     40     KV				nsitized base mater	ial FR4 with UV	/ blocker
by DSC, spec. Minimum         ASTM D3850         -         °C         320           Decomposition Temperature (Td)         ASTM D3850         -         °C         320           CTE, Z-Axis         port TG         2.4.24         AABUS         ppm/°C         250           CTE, X-, Y-Axis         post TG         2.4.24         -         ppm/°C         15           CTE, X-, Y-Axis         post TG         2.4.24         -         ppm/°C         17           Thermal Conductivity         ASTM D38930         -         WmK         0.36           Thermal Stress 10s @ 288°C         unetched/         2.4.13.1         Pass visual         Rating         Pass           spec maximum         B. @ 100 MHz         2.5.5.3         5.4         -         4.6           C. @ 1 GHz         2.5.5.5         -         -         4.6         -           Loss tangent, spec maximum         B. @ 100 MHz         2.5.5.9         -         -         0.015           Volume Resistivity         After moisture resistance         2.5.17.1         10°         MOhm cm         7.0x10°           Surface Resistivity         After moisture resistance         2.5.17.1         10°         MOhm d0h         0.016           Surfac	Property			Specification	Units	Typical Value
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		3)	2.4.25	110-150	°C	150
CTE         Z-Axis         post TG         2.4.24         AABUS         ppm/°C         250           CTE         X-, Y-Axis         post TG         2.4.24         -         ppm/°C         15           CTE, X., Y-Axis         post TG         2.4.24         -         ppm/°C         17           Thermal Conductivity         ASTM D5930         -         W/mK         0.36           Thermal Stress 10s @ 288°C         unetched/         2.4.13.1         Pass visual         Rating         Pass           Spec minimum         etched         2.4.3.1         Pass visual         Rating         Pass           Spec maximum         B. @ 100 MHz         2.5.5.9         -         -         4.6           C. @ 1 GHz         2.5.5.9         -         -         0.015           Spec maximum         B. @ 100 MHz         2.5.5.9         -         -         0.015           Volume Resistivity         After moisture resistance         2.5.17.1         10°         MOhm cm         7.0x10°           Surface Resistivity         After moisture resistance         2.5.17.1         10°         MOhm cm         7.0x10°           Surface Resistivity         After moisture resistance         2.5.17.1         10°         MOhm cm	Decomposition Temperature (Td)		ASTM D3850	-	°C	320
Thermal Stress 10s @ 288°C spec minimumunetched/ etched2.4.13.1 2.4.13.1Pass visual Pass visualRating 	CTE, Z-Axis CTE, X-, Y-Axis	post TG pre TG	2.4.24 2.4.24	-	ppm/°C ppm/°C	250 15
spec minimumetched2.4.13.1Pass visualRatingPassPermittivity, spec maximumA. @ 1 MHz2.5.35.4-4.6Spec maximumB. @ 100 MHz2.5.5.94.6C. @ 1 GHz2.5.5.94.5Loss tangent, spec maximumB. @ 100 MHz2.5.5.9-0.015Spec maximumB. @ 100 MHz2.5.5.9-0.015Volume Resistivity spec minimumAt elevated temperature2.5.17.110°MOhm cm4.0x10°Surface Resistivity spec minimumAt elevated temperature2.5.17.110°MOhm cm7.0x10°Surface Resistivity spec minimumAt elevated temperature2.5.17.110°MOhm cm7.0x10°Surface Resistivity spec minimumAt elevated temperature2.5.17.110°MOhm3.0x10°Dielectric Breakdown, spec minimumspec minimum2.5.640kV60Comparative Tracking IndexCTI / ASTM D3638UL-746A-Volts205 (CL=3)Peel stenght spec. minimumAfter thermal stress2.4.8105N/mm145Spec. minimum2.4.8105N/mm14535Spec. minimumSpec maximum2.6.2.10.80%0.20UL ApprovalLengthwise2.4.4415G.Pa442Flexural strength, minimumlengthwise2.4.4345G.Pa435Moisture absorbtion UL Approvalspec ma	Thermal Conductivity		ASTM D5930	-	W/mK	0.36
spec maximum         B. @ 100 MHz         2.5.5.9         -         -         4.6           Loss tangent, spec maximum         A. @ 1 MHz         2.5.5.3         0.035         -         0.015           spec maximum         B. @ 100 MHz         2.5.5.3         0.035         -         0.015           spec maximum         C. @ 1 GHz         2.5.5.3         -         -         0.015           Volume Resistivity         After moisture resistance         2.5.17.1         10 <sup>6</sup> MOhm cm         4.0x10 <sup>8</sup> Spec minimum         At elevated temperature         2.5.17.1         10 <sup>4</sup> MOhm cm         3.0x10 <sup>6</sup> Surface Resistivity         After moisture resistance         2.5.17.1         10 <sup>4</sup> MOhm cm         3.0x10 <sup>6</sup> Spec minimum         At elevated temperature         2.5.17.1         10 <sup>4</sup> MOhm cm         3.0x10 <sup>6</sup> Spec minimum         At elevated temperature         2.5.17.1         10 <sup>4</sup> MOhm cm         3.0x10 <sup>6</sup> Comparative Tracking Index         Spec minimum         2.5.6         40         KV         60           Comparative Tracking Index         CTI / ASTM D3638         UL-746A         -         Volts         205 (CL=3)           Peel st						
spec maximum         B. @ 100 MHz         2.5.5.9         -         0.015           Volume Resistivity         After moisture resistance         2.5.17.1         10 <sup>6</sup> MOhm cm         4.0x10 <sup>6</sup> spec minimum         At elevated temperature         2.5.17.1         10 <sup>3</sup> MOhm cm         7.0x10 <sup>7</sup> Surface Resistivity         After moisture resistance         2.5.17.1         10 <sup>3</sup> MOhm cm         7.0x10 <sup>7</sup> Surface Resistivity         After moisture resistance         2.5.17.1         10 <sup>3</sup> MOhm cm         7.0x10 <sup>7</sup> Surface Resistivity         After moisture resistance         2.5.17.1         10 <sup>4</sup> MOhm cm         7.0x10 <sup>7</sup> Dielectric Breakdown,         spec minimum         2.5.6         40         kV         60           Arc Resistance,         spec minimum         2.5.17         10 <sup>3</sup> MOhm cm         7.0x10 <sup>9</sup> Comparative Tracking Index         CTI / ASTM D3638         UL-746A         -         Volts         205 (CL=3)           Peel strenght         After thermal stress         2.4.8         105         N/mm         145           spec. minimum         At 125 °C         2.4.8         105         N/mm         145           Spec		B. @ 100 MHz	2.5.5.9	-	-	4.6
spec minimum         At elevated temperature         2.5.17.1         10 <sup>-3</sup> MOhm cm         7.0x10 <sup>7</sup> Surface Resistivity         After moisture resistance         2.5.17.1         10 <sup>-4</sup> MOhm dm         3.0x10 <sup>6</sup> Surface Resistivity         After moisture resistance         2.5.17.1         10 <sup>-4</sup> MOhm dm         3.0x10 <sup>6</sup> Dielectric Breakdown,         spec minimum         2.5.6         40         kV         60           Arc Resistance,         spec minimum         2.5.1         60         Seconds         105           Comparative Tracking Index         CTI / ASTM D3638         UL-746A         -         Volts         205 (CL=3)           Peel strenght         After thermal stress         2.4.8         105         N/mm         145           spec. minimum         cross solutions         2.4.8         105         N/mm         145           Flexural strength,         lengthwise         2.4.4         415         G.Pa         442           minimum         crosswise         2.4.4         345         G.Pa         435           Moisture absorbtion         spec maximum         2.6.2.1         0.80         %         0.20           UL Approval         E45456		B. @ 100 MHz	2.5.5.9	-		0.015
spec minimum         At elevated temperature         2.5.17.1         10 <sup>-3</sup> MOhm         6.0x10 <sup>-6</sup> Dielectric Breakdown,         spec minimum         2.5.6         40         KV         60           Arc Resistance,         spec minimum         2.5.6         40         KV         60           Comparative Tracking Index         CTI / ASTM D3638         UL-746A         -         Volts         205 (CL=3)           Peel strenght         After thermal stress         2.4.8         105         N/mm         145           spec. minimum         At 125 °C         2.4.8         105         N/mm         145           Spec. minimum         Alt er process solutions         2.4.8         105         N/mm         145           Flexural strength, minimum         lengthwise         2.4.4         415         G.Pa         442           Moisture absorbtion         spec maximum         2.6.2.1         0.80         %         0.20           UL Approval         E         45456         E         F         F         V-0           Thickness tolerance dielectric         spec minimum         UL-94         V-1         Rating         V-0           Thickness tolerance coper         L         Gass II						
Arc Resistance,         spec minimum         2.5.1         60         Seconds         105           Comparative Tracking Index         CTI / ASTM D3638         UL-746A         -         Volts         205 (CL=3)           Peel strenght         After thermal stress         2.4.8         105         N/mm         145           spec. minimum         At125 *C         2.4.8         105         N/mm         145           Flexural strength,         lengthwise         2.4.4         105         N/mm         145           Flexural strength,         lengthwise         2.4.4         345         G.Pa         442           minimum         crosswise         2.4.4         345         G.Pa         442           Moisture absorbtion         spec maximum         2.6.2.1         0.80         %         0.20           UL Approval         E         E45456         E         E         E         Flammability, 35 */- 0.08           Thickness tolerance dielectric         spec minimum         UL-94         V-1         Rating         V-0           Thickness tolerance copper         E         Gass II         E         35 */- 5         5						
Comparative Tracking Index         CTI / ASTM D3638         UL-746A         -         Volts         205 (CL=3)           Peel strenght spec. minimum         After thermal stress         2.4.8         105         N/mm         145           After process solutions         2.4.8         105         N/mm         145           After process solutions         2.4.8         105         N/mm         145           Flexural strength, minimum         lengthwise         2.4.4         315         G.Pa         442           Moisture absorbtion         spec maximum         2.6.2.1         0.80         %         0.20           UL Approval         E45456         E         E         E         E         F           Flammability,         spec minimum         UL-94         V-1         Rating         V-0           Thickness tolerance copper         E         Class II          35 +/- 5	Dielectric Breakdown,	spec minimum	2.5.6	40	kV	60
Peel strenght spec. minimum         After thermal stress At 125 °C         2.4.8         105         N/mm         145           Flexural strength, minimum         lengthwise         2.4.8         105         N/mm         145           Flexural strength, minimum         lengthwise         2.4.8         105         N/mm         145           Kore the process solutions         2.4.8         105         N/mm         145           Motisture absorbtion         spec maximum         2.6.2.1         0.80         %         0.20           UL Approval         E 45456         E         E         E         E           Flammability, Thickness tolerance dielectric         spec minimum         UL-94         V-1         Rating         V-0           Thickness tolerance copper         E         Class II         µm         3.5 ±/-5         3.5 ±/-5	Arc Resistance,	spec minimum	2.5.1	60	Seconds	105
spec. minimum         At 125 °C         2.4.8         105         N/mm         145           After process solutions         2.4.8         105         N/mm         145           Flexural strength, minimum         lengthwise         2.4.4         415         G.Pa         435           Moisture absorbtion         spec maximum         2.6.2.1         0.80         %         0.20           UL Approval         E         4556         F         F         F         Thickness tolerance dielectric         V-0           Thickness tolerance copper         Class II         V-1         Rating         V-0	Comparative Tracking Index	CTI / ASTM D3638	UL-746A	-	Volts	205 (CL=3)
minimum         crosswise         2.4.4         345         G. Pa         435           Moisture absorbtion         spec maximum         2.6.2.1         0.80         %         0.20           UL Approval         E         4556		At 125 °C	2.4.8	105	N/mm	145
UL Approval     E 45456       Flammability,     spec minimum     UL-94     V-1     Rating     V-0       Thickness tolerance dielectric     Class II     mm     1.55 +/- 0.08       Thickness tolerance copper     μm     35 +/- 5						
Flammability,         spec minimum         UL-94         V-1         Rating         V-0           Thickness tolerance dielectric         Class II         mm         1.55 +/- 0.08           Thickness tolerance copper         μm         35 +/- 5		spec maximum		0.80	%	0.20
$ \begin{array}{ccc} Thickness tolerance dielectric & Class II & mm & 1.55 +/- 0.08 \\ Thickness tolerance copper & & \mu m & 35 +/- 5 \end{array} $		spec minimum	UL-94	V-1	Rating	V-0
	Thickness tolerance dielectric	- F		·	mm	1.55 +/- 0.08
		th		< 3	%	< 3

Figure 4.39 – Standard FR4 Datasheet [7]

Regarding the assembly necessary to perform the measure, it consists in soldering a single SMA connector to a corner of the piece of laminate, as shown in figure 4.40.

a corner **Figure 4.40** – Effective Permittivity Measurement Assembly [12]

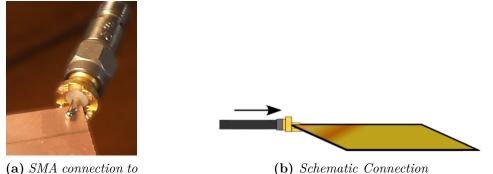
Because FR4 is a Dispersive substrate, Relative Permittivity will vary with frequency. Therefore, and taking into account the waveguide approximation applied, a piece of substrate long and narrow will allow identifying the modes of the 'waveguide' easily; for this reason, a piece of 248x35.60 mm is cut. Firstly, theoretical resonance frequencies for a rectangular waveguide are calculated using 4.1.3.

$$f = \frac{c}{2\pi\sqrt{\mu\epsilon}}\sqrt{\left(\frac{\pi p}{L}\right)^2 + \left(\frac{\pi q}{W}\right)^2} \tag{4.1.3}$$

Where p and q correspond to the different propagation modes of the waveguide and L and W to the *Length* and *Width*, respectively. It is obvious that, previously, a certain Relative Permittivity must be assumed as correct in order to use equation 4.1.3; in this case, a value of 4 will be taken. Substituting every variable, for different p modes, it yields to the frequencies in table 4.12.

Before measuring, it is necessary to calibrate the VNA Agilent E5071C. It is made using the corresponding **calibration kit**, which includes terminations for *short*, *open* and *load*.

Figure 4.41 – Agilent E5071C Calibration Kit [2]



Once calibrated, resonance frequencies along with the theoretical bandwidth calculated are measured, getting the ones shown in table 4.13. Figures 4.42 and 4.43 show two of the resonances.

_P:	ropagation Mode	Frequency (MHz)
р	q	-
1	0	263.64
2	0	527.28
3	0	790.92
4	0	1055
5	0	1318
6	0	1582
$\overline{7}$	0	1845
8	0	2109

<b>Fable 4.12</b> –	Theoretical	resonance	frequencies	
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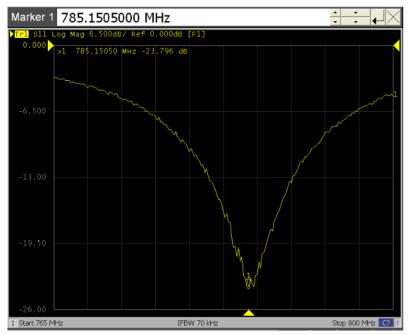


Figure 4.42 – Resonance at 785.15 MHz

r

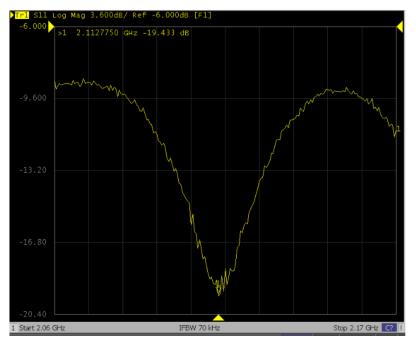


Figure 4.43 – Resonance at 2111.21 MHz

Pro	pagation Mode	Frequency (MHz)
р	q	-
1	0	260
2	0	524.19
3	0	787.5
4	0	1049.76
5	0	1311.06
6	0	1572.88
7	0	1836.19
8	0	2111.21

 Table 4.13 – Resonance Frequencies Measured

In addition, depending on the **quality factor** of the resonance, some losses may occur. To take them into account, the correction factor developed by Howell [46] and Wang [62], can be applied. It is shown in equation 4.1.4.

$$f_{adj} = \frac{f_{\text{Measured}}}{1 - \frac{1}{2Q}} \tag{4.1.4}$$

A reasonable value for FR4 quality factor is 50. Applying equation 4.1.4 to frequencies

Pro	pagation Mode	Frequency (MHz)
р	q	_
1	0	262.63
2	0	529.49
3	0	795.46
4	0	1060
5	0	1324
6	0	1589
7	0	1855
8	0	2133

in table 4.13, frequencies in table 4.14 are obtained:

 Table 4.14 - Corrected Resonance Frequencies

Correction factor increases frequency about a 1 %. It is negligible for Q>100.

To determine the effective permittivity, manipulating equation 4.1.3 and simplifying constants, it yields to equation 4.1.5.

$$\epsilon = \left(\frac{14990}{f}\right)^2 \left(\left(\frac{p}{L}\right)^2 + \left(\frac{q}{W}\right)^2\right) \tag{4.1.5}$$

Expression in which f must be taken in MHz and L and W in cm. Applying it to the frequencies in table 4.14, it yields to **effective permittivity** values of table 4.15.

 Table 4.15 – Calculated Effective Permittivities

The mean of the calculated values is **3.963**, with an standard deviation of 0.032. Finally, in order to determine the accuracy of the technique applied, theoretical frequencies are calculated again using **3.963** as permittivity, showing a relative error of 0.227 % with respect

to the experimental frequencies obtained. Therefore, the technique is assumed valid, and 3.963 will be taken as **effective permittivity** for the design.

Another important phenomena to take into account when designing at microwave frequencies is the **Skin Effect**. It is produced because of the tendency of alternating current to distribute along the conductor so its density is greater closer to the conductor surface, and lower at the inner. As a consequence, effective section of the conductor decreases and therefore, the current in the center of the conductor does too, as shown in figure 4.44. The section of the conductor in which the current tends to concentrate is known as *skin effect depth* and it is defined as the distance where the signal has decayed in a factor  $\frac{1}{e}$ .

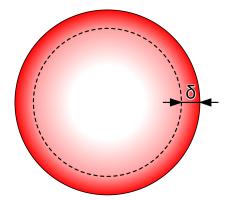


Figure 4.44 – Skin Effect at a circular conductor [35]

However, the situation must be analyzed for a Microstrip Technology line onto a substrate. The equivalent figure is shown in 4.45.

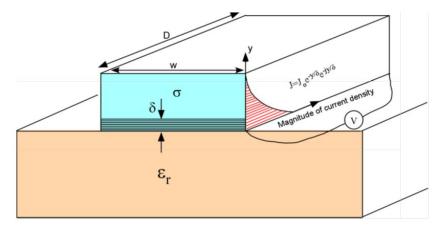


Figure 4.45 – Skin Effect at a microstrip line [31]

In a Microstrip Technology line, current tends to concentrate close to the substrate plane. For both cases, skin effect depth is given by expression 4.1.6.

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \sqrt{\sqrt{1 + (\rho\omega\epsilon)^2 + \rho\omega\epsilon}}$$
(4.1.6)

Skin effect increases along with frequency. If equation 4.1.6 is computed for a range and frequency and plotted, the graphic of figure 4.46 is obtained. In the matter in hand, 2.4 GHz is considered as frequency of work, so it has been indicated that frequency with a vertical yellow line. For that frequency, skin effect depth equals to  $1.33 \,\mu\text{m}$ 

It can be demonstrated that 98 % of the current will flow in a thin layer whose thickness corresponds approximately to 4 times skin effect depth, i.e.,  $5.32 \,\mu$ m in this case. Given that the analyzed substrate disposes of  $35 \,\mu$ m of copper, the current will flow, because of Skin Effect, in a layer which corresponds to a  $15.2 \,\%$  of the amount of the conductor, as shown in 4.1.7.

$$\frac{\text{Usable Conductor}}{\text{Available Conductor}} = \frac{5.32\,\mu\text{m}}{35\,\mu\text{m}} = 15.2\% \tag{4.1.7}$$

Therefore, **Skin Effect** is responsible for wasting almost 85 % of the conductor. Consequently, it must be remarked the capital importance that this phenomena has in every design implying printed technology, from a sufficiently high frequency.

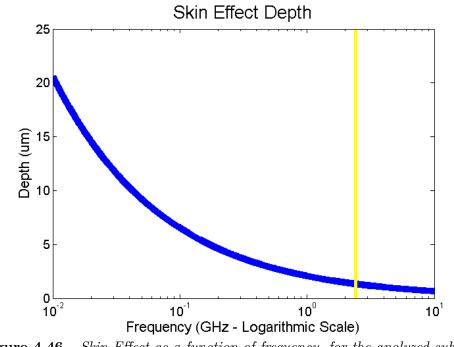


Figure 4.46 – Skin Effect as a function of frequency, for the analyzed substrate

### 4.1.3.2.3.2 ADS Design

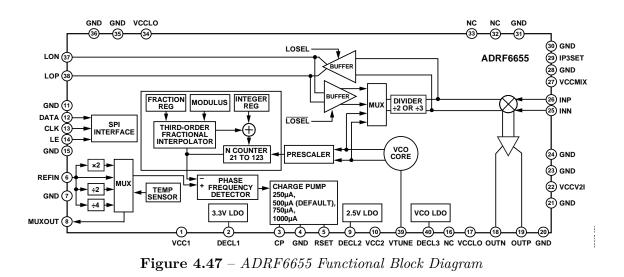
After adequately characterizing the substrate used, the next step is starting the design of the mixer. As mentioned, it will be made following the blocks structure seen in the analyzed mixer, 4.1.3.2.1. There are mainly four elements to distinguish: VCO, Mixer, Amplifiers, Supply and Filtering. Firstly, VCO and Mixer will be chosen, so Intermediate Frequency is defined.

• VCO

A VCO is, in short, an electronic device used to provide an output signal whose frequency depends on a tuning voltage. In this case, it will be used, along with a mixer, to down-convert the input signal from the 4.1.3.1 stage to an **Intermediate Frequency**. Different commercialized alternatives are considered, shown in the section 'VCO' of the table of the following page; all of them have been chosen to be in the band 0.5-1.2 GHz, at least. The main initial constraint is that the chosen one is needed to be a built-in VCO, without any need of adding external resonators, quartz crystal, Varactor or any other component. The reason for this condition is that a fully integrated VCO is less likely to suffer thermal drift than the others; on the other, those are cheaper.

Regarding the options shown, it is appreciable that it does exist large prices difference between the ones shown; this variation depends mostly on a number of factors: tuning sensitivity, bandwidth, output power and also the need for external circuitry. For example, **Pasternack PE1V11017** [28], exhibits low phase noise and a huge tuning sensitivity, as well as great output power; however, its high price makes it prohibitive for the design. With regards to the **Maxim Integrated MAX2620** [22], although it is an economical option, it requires adding external Varactor and resonator, so it is discarded. Another possibility is **Analog Devices ADRF6655** [3]. It is an extremely interesting option because its versatility: it includes not only an VCO but only a **mixer** and a PLL; it means that its choice would make unnecessary the selection of a mixer. Its complexity is obviously greater than the others, as appreciable at figure 4.47.

Model <u>Minicircuits PGA-103+</u>	RF Freq (GHz) 0.1 - 2.5	Mixers LO Freq (GHz) 1.050 - 2.3	IF Freq (GHz) LF - 2.2	Max RF Power (dBm) 20	Max LO Power (dBm) (1)
Macom MAMX-009239-001500	0.01 -2.5 Input P1dB (dBm)	0.01 -2.6 Price (€)	0.01 -2.7	13	17
	12 13	18 6.1			
Notes:	1) Mixer with integrate	1) Mixer with integrated VCO. Ouput power of the VCO internally controlled	he VCO internally cont	trolled	
Model	Ered range (GH2)	Tuning Voltage (VDC)	Supply Voltage (V)	Outhout Dower (dBm)	Drica (£)
Pasternack PE1V11017	0.8 - 1.2	0-20	Juppiy Voliage (V) 14-16	+10 to +16	86.4
Maxim Integrated MAX2620	0.01 - 1.05	0.5-30	2.7-5.25	8-	3.77
Crystek CVCO55BE-0510-0770	0.550 - 0.770	1.0-8.0	6	+2 to +11	24.4
Analog Devices ADRF6655 (1)	1.050 - 2.3	2 - 2.3	4.75 - 5.25	-7 (2)	18
Crystek CVCO55BE-0510-0900	0.510 - 0.900	0.5-10	12	+6 to +13	21.66
Notes:	1) Integrated VCO in Mixer ADRF6655 2) Output Power when LO = 1.050 GHz	ixer ADRF6655 LO = 1.050 GHz			
	Figure 4	Figure 4.48 – VCO and Mixer Comparative	ixer Comparative	0	



It has, however, a *disadvantage*. Input and output impedances of the mixer ports are not **50**  $\Omega$ , but a Differential Impedance of **50**  $\Omega$  input and also differential **200**  $\Omega$  at the output. Of course, it would imply the need of a matching network, which for the output would be like the one shown in figure 4.50.

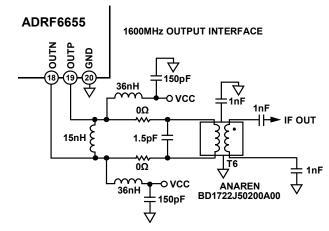


Figure 4.49 – Output Matching Network required for ADRF6655

It implies a greater number of components, which from a production point of view, requires a higher number of components and references in *stock*. On the other hand, the complexity of the circuitry increases significantly. For all these reasons, it does not seem an optimum solution, although it must not be completely discarded. There are two options left, from the same company, **Cristek** [8] [9]. Unlike the latter, they are only VCO and exhibit similar characteristics. They are both completely built-in and have an acceptable tuning sensitivity. Because of availability reasons, **Crystek CVCO55BE-0510-0900** [9], with a price of 21.66 €, is chosen as VCO. Therefore, 900 MHz will be the LO frequency.

## • Mixer

With regard to **mixer**, as mentioned before, **Analog Devices ADRF6655** is valid as mixer too, nevertheless, given the selection of the VCO already made and the considerations made about this device, it is discarded. The reference table mentioned before shows the other possibility, Macom MAMX-009239-001500 [21].

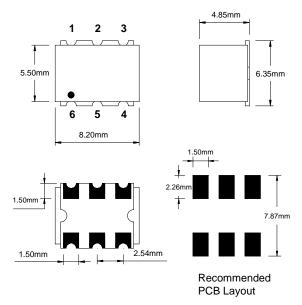


Figure 4.50 – Macom MAMX-009239-001500

It is a cheaper mixer, internally matched to 50  $\Omega$  input and output impedances, and although it supposes 7.5 dB of conversion losses, it is chosen as mixer for the system.

### • Amplifier

As seen in the analysis of the DG0VE KON13-900, see section 4.1.3.2.1, amplifiers are a vital part of a mixer, because of the weakness of the signal received. As before, different commercialized possibilities are shown in the following page, from **Mini-Circuits**, one of the most reliable and widely used trademarks for this devices; datasheets can be found at [24], [25], [26] and [23]. Figures of merit have been included at both frequencies of work, RF Frequency (2.4 GHz) and IF Frequency (1.5 GHz, given that 900 MHz has been chosen as the LO frequency).

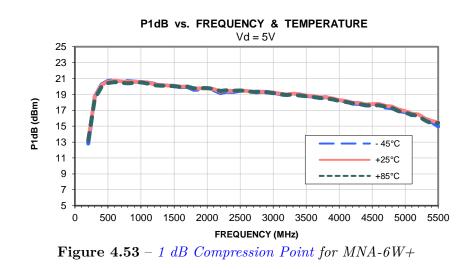


	Price (€)	2.84	1.64	2.19	2.25		Noise Figure (dB)	1	1.1	0.89	2.78		Noise Figure (dB)	0.87	0.85	0.82	2.59	odel
	Supply (V)	5.00 (3)	3,00	5.00 (3)	5.00		IP3 output (dBm)	22.57	30.95	35.95	30.47		IP3 output (dBm)	43.32	30.05	35.1	31.81	test conditions in this m with 40 mA. <i>tive</i>
Amplifiers	Freg range (GHz)	0.05-4	0.05-7	0.05-4	0.5-5.5		P1dB(dBm)	47.36	18.9@60mA (2)	22.05	19.44	_	P1dB(dBm)	22.19	18.5@60mA(2)	21.5	20.08	Power is specified as a requirement under test d with 60 mA current limit. Also available with d with 5 V suppy. 3 V supply also possible <b>Figure 4.52</b> – <i>Amplifiers Comparative</i>
	RF Input Power		I	-25 dBm (1)	-25 dBm (1)	RF @2.4 GHz Measurements	Gain (dB)	9.68	12	11.85	23.82	IF @1.5 GHz Measurements	Gain (dB)	13.21	15.75	14.45	25.38	<ol> <li>RF Input Power is specified as a requirement under test conditions in this model</li> <li>Measured with 60 mA current limit. Also available with 40 mA.</li> <li>Measured with 5 V suppy. 3 V supply also possible</li> <li>Figure 4.52 - Amplifiers Comparative</li> </ol>
	Model	Minicircuits PGA-103+	Minicircuits PMA-5451+	Minicircuits PSA4-5043+	Minicircuits MNA-6W+		Model	Minicircuits PGA-103+	Minicircuits PMA-5451+	Minicircuits PSA4-5043+	Minicircuits MNA-6W+		Model	Minicircuits PGA-103+	Minicircuits PMA-5451+	Minicircuits PSA4-5043+	Minicircuits MNA-6W+	Notes: Temperature = +25º at all cases

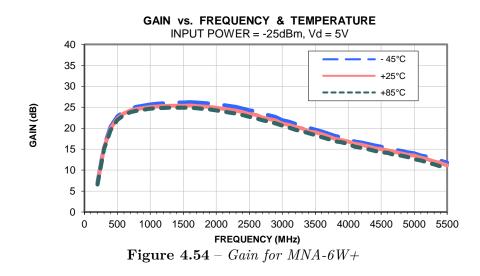
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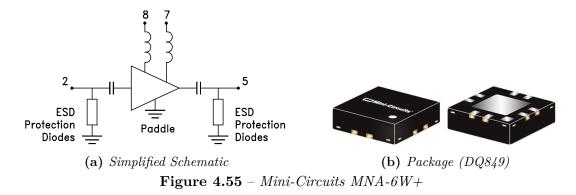
Regarding Input Frequency Range, every amplifier shown is valid, reaching up to 7 GHz in some cases. Price is quite similar in all of them too. 1 dB Compression Point is neither a problem because in all cases is far from the expected output power. In addition, every one is internally matched to 50  $\Omega$  so there is no need for external matching network.



Gain, however, is a crucial issue; depending on the gain of the chosen amplifier, there will be needed two or three amplification stages. Amplification is specially needed at the input of the amplifier, when in spite of the amplification given by the LNA, the signal has been deteriorated because of the cable distance between the antenna and the receiver. Therefore, the only amplifier from the exposed which guarantees enough signal amplification is MNA-6W+ [23], with 23.82 dB at the Input Frequency, and 25.38 dB at IF, almost doubling the rest in some cases.



It exhibits also higher noise figure than the others, but it is worth it. Mini-Circuits MNA-6W+ is also a completely integrated amplifier, with DC Block and bias circuits incorporated, as well as the already mentioned internal 50  $\Omega$  matching network. Simplified schematic and case is shown in figure 4.55.



# • Supply

Given that **active** elements have already been chosen, supply system for the mixer can be designed.

It must be remembered that input voltage comes from the PCB Receiver, which feeds up the antenna (and therefore the mixer and LNA) with +12 VDC. On the one hand the chosen VCO requires +12 VDC of supply, so it can be directly fed; in addition, according to the datasheet, it will need about 9.5 V for tuning voltage. On the other hand, amplifiers require +5 VDC supply. Linear regulators will be used; as considered in the design of the PCB, taking into account the large step between input and output voltage, it is recommended, to increase efficiency, stepping-down in two stages. For the sake of simplicity, it will be made with two classics regulators, **7809** and **7805**, in their **throgh-hole** packages, to prevent the system from dissipating excessive heat. With them, every voltage line needed for supply is achieved, and a simple **voltage divider using a variable resistor** is implemented to achieve the tuning voltage for VCO.



Figure 4.56 – 7809 Through-Hole Regulator

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# • Filtering

For filtering stages, Microstrip Technology will be useful again. Microstrip Filters will be designed using Keysight Genesys RF<sup>®</sup> software. Unlike others design software like Altium Designer<sup>®</sup> 16, Keysight Genesys RF<sup>®</sup> does not need a previous schematic, but it can be designed from given parameters. It makes this software a powerful and versatile tool.

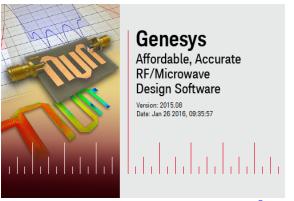


Figure 4.57 – Keysight Genesys RF<sup>®</sup>

At this point it must be pointed out, as made before in this Project, the fact that Microstrip Filter Design, (even Filter Design, generally), is a huge topic which cannot be afforded in depth in this Bachelor Thesis, because of simple length reasons; therefore, aspects like advanced details of the different topologies mentioned here, some shapes or others will not be analyzed here.

Given the inexperience of the author in Microstrip Technology filter design and with the purpose of adequately knowing the technology before starting the proper design for this Project, some testing design are performed. Particularly, and because of the previously developed ADSB system within GranaSAT Project, (which resulted in a paper publication at URE, see [48]), it is designed a 1090 MHz bandpass Hairpin Filter, to be used along with the system. Figure 4.58a shows an example of a Hairpin topology, while figure 4.58b shows an ideal bandpass filter as reference.

Of course, frequency response of figure 4.58b is not physically feasible. Therefore, a set of parameters will be given to Keysight Genesys  $RF^{\textcircled{m}}$  in order to determine the best topology and response of the proposed filter. These parameters are the ones shown in table 4.16 for the 1090 MHz Bandpass Hairpin Filter. Before designing the desired filter, a new **substrate** has been added, corresponding with the one available and analyzed at 4.1.3.2.3.1.

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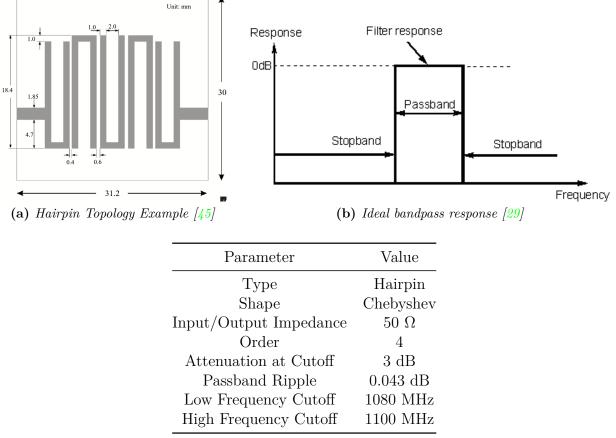


 Table 4.16 – 1090 MHz Bandpass Hairpin Filter Design Parameters

As mentioned, instead of generating an structure from schematics as others, Keysight Genesys RF<sup>®</sup> will generate from the parameters above an schematic and the corresponding layout. Figures 4.58, 4.59 and 4.62 show them.

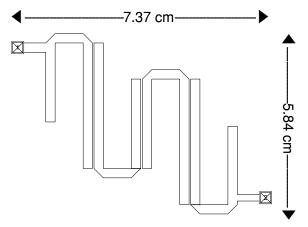


Figure 4.58 – 1090 MHz Bandpass Hairpin Filter Layout

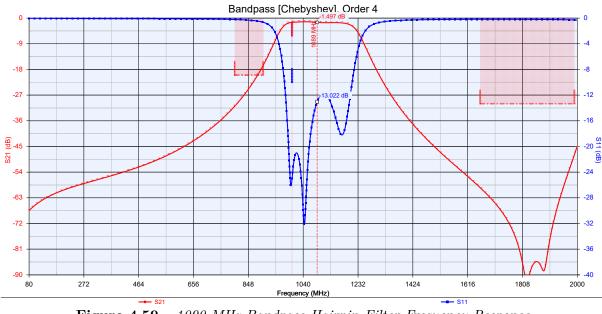


Figure 4.59 – 1090 MHz Bandpass Hairpin Filter Frequency Response

It can be seen how the simulated response of the filter is adequate, the passband is at the expected range and  $S_{21}$  parameter is minor than 1.5 dB at the bandpass so the filter design is accepted. It is manufactured using **LPKF ProtoMat S62**, introduced to manufacture the PCB receiver. The result is shown in figure 4.60.

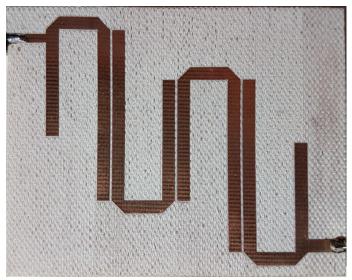
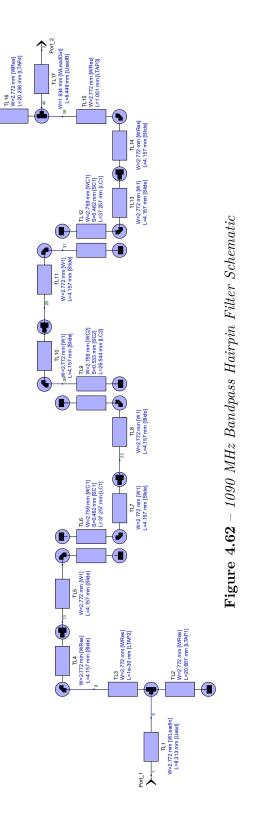


Figure 4.60 – 1090 MHz Bandpass Hairpin Filter. Milling manufactured.

Once manufactured, two SMA connectors are soldered to their ports and  $S_{11}$  parameter is measured using Agilent E5071C. The measurement is shown in figure 4.61.



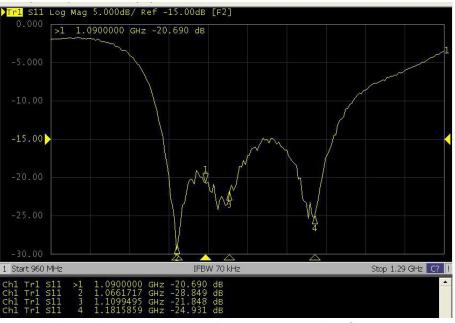
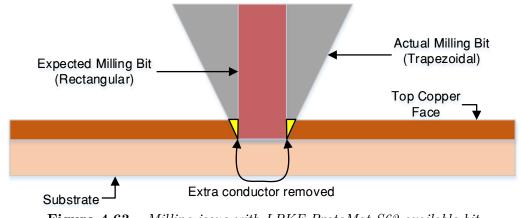


Figure 4.61 – 1090 MHz Bandpass Hairpin Filter  $S_{11}$  parameter

Measurements shows that  $S_{11}$  parameter is -20.69 dB at 1090 MHz, which is an acceptable result. However, even although the measured response is similar to the simulated one, some variations are appreciable regarding high and low cutoff frequencies and bandwidths. For this reason, the design is revised and some test are performed with another manufactured filters. It is concluded that although the design is correct, the manufacturing process is not; LPKF ProtoMat S62 drills using a trapezoidal bit, while the design expects a perfectly rectangular one. This is a crucial matter taking into account, as it will be seen later, the importance of the width and shape in a Microstrip Technology line. This issue is reflected (in an exaggerated manner) in figure 4.63.



Therefore, LPKF ProtoMat S62, with the available bit, is an unreliable manufacturing technique for designs implying Microstrip Technology.

However, given that designs have been proved to be correct, mixer filtering stage will be designed according to the technique exposed before. Particularly, two different **bandpass** filters will be designed according to the frequencies in the mixer, i.e., 2.4 GHz and 1.5 GHz; obviously, the first one will be implemented before the mixer, and the second one will be implemented after down-converting the signal.

In the first place, 2.4 GHz filter will be designed. In this case, **Edge-Coupled** Topology, with Chebyshev shape, will be used as first iteration. As before, main parameters design are shown in table 4.17.

Parameter	Value
Type	Edge-Coupled
Shape	Chebyshev
Input/Output Impedance	$50 \ \Omega$
Order	6
Attenuation at Cutoff	3  dB
Passband Ripple	$0.023 \mathrm{~dB}$
Low Frequency Cutoff	$2350 \mathrm{~MHz}$
High Frequency Cutoff	$2450~\mathrm{MHz}$

 Table 4.17 – 2.4 GHz Bandpass Edge-Coupled Filter Design Parameters

In this case, for the sake of experimentation, the topology has been changed, and a wider bandwidth has been set. Testing stage explained before clearly reflected that setting unrealistic values, for this substrate, (excessively narrow bandwidth, or unachievable attenuations in a real filter) often yields to faulty designs, with countless losses. Therefore, moderated values are set for the first iteration. As before, schematic, layout and frequency response are shown in figures 4.64, 4.65 and 4.68.

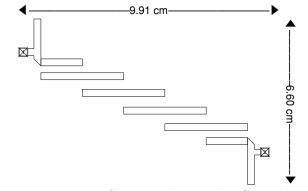


Figure 4.64 – 2.4 GHz Bandpass Edge-Coupled Layout

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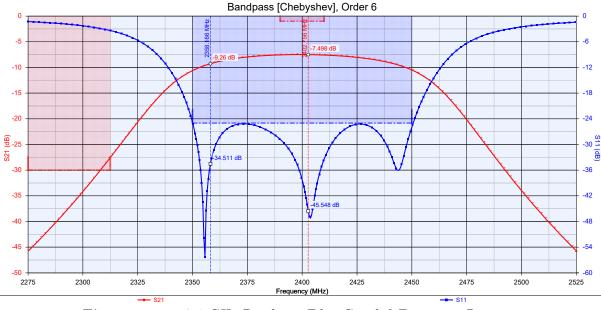


Figure 4.65 – 2.4 GHz Bandpass Edge-Coupled Frequency Response

There are two main problems with the design obtained with this topology. The first of them is **size**; unlike testing performed before, size is an important issue at this design, because the larger the filter, the larger the surface needed for the substrate, and as commented in preceding lines, **higher** price. For instance, these edge-coupled filter needs  $65.42 \text{ cm}^2$  of surface, which is a noteworthy size, taking into account that at least 2 of them will be needed. In addition, Insertion Losses are also noticeable, with almost 7.5 dB at the bandpass; even although the frequency range at the bandpass is correct, these are a really significant amount of losses.

For these reason, another design iteration is performed, seeking for better performance and layout. In this case, **Hairpin** topology is used again. Design parameters are listed in table 4.18, whereas figures 4.66, 4.67 and 4.69 show the results.

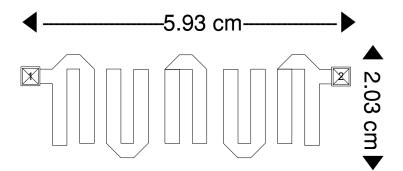
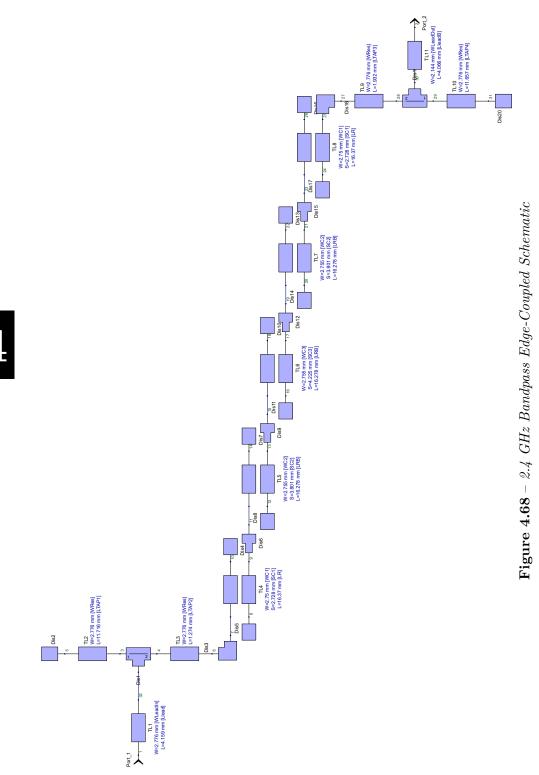


Figure 4.66 – 2.4 GHz Bandpass Hairpin Layout



Chapter 4. System Design

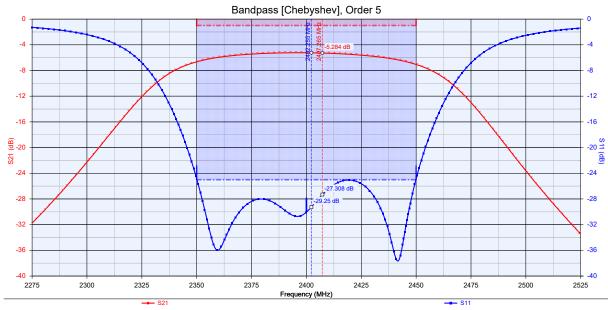
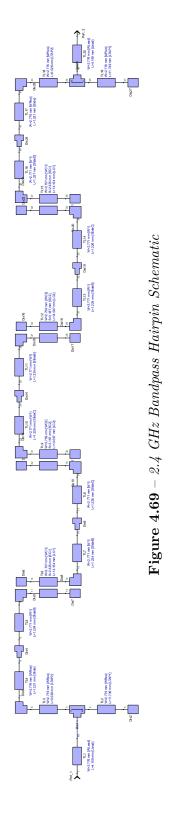


Figure 4.67 – 2.4 GHz Bandpass Hairpin Frequency Response

Parameter	Value
Туре	Hairpin
Shape	Chebyshev
Input/Output Impedance	$50 \ \Omega$
Order	5
Attenuation at Cutoff	5  dB
Passband Ripple	$0.023~\mathrm{dB}$
Low Frequency Cutoff	$2350 \mathrm{~MHz}$
High Frequency Cutoff	$2450 \mathrm{~MHz}$

 Table 4.18 – 2.4 GHz Bandpass Hairpin Filter Design Parameters

In this case, layout size has decreased considerable, needing a surface  $12.04 \text{ cm}^2$  for the filter. However, Insertion Losses are still relatively high, with 5.28 dB of attenuation at bandpass. By comparison with the DG0VE KON13-900 analyzed at 4.37, it is obvious that the attenuation suffered by the designed filters, as well as the size, are higher than the ones experimented by the commercialized mixer. After several test with others topologies and shapes (as **Bessel**), it is concluded that it is due to the **substrate** used. Effectively, and as many authors have stated in previous literature, FR4 is not an optimum substrate for RF and Microwave Design, because of its losses; in addition, it has been also checked that a higher Relative Permittivity allows getting smaller size filters so it is reasonably to think that the substrate used in DG0VE KON13-900 mixer has a higher one, probably not being FR4.





Therefore, if size reduction is sought, another approach to design the mixer is using high Relative Permittivity substrates, (up to 90), or designing using advanced techniques such as dual-mode resonators filters, multilayer filters or slow-wave resonator filters (see [45]), which are beyond the scope of this Bachelor Thesis. It is proposed as a future line of work.

Despite the problems arisen during the previous design, it is decided to continue with the design using the available substrate, compensating the losses suffered with the different amplification stages and leaving size reduction for subsequent versions of the prototype. Therefore, in view of the improvement experimented with Hairpin topology at the 2.4 GHz Filter, it is selected for this filtering stage. Two of them will be implemented at the mixer, after the corresponding amplification stage.

As mentioned, the next filtering stage will be implemented after the mixer, so it will be composed of a bandpass filter at 1.5 GHz (IF). Given the previous results, it seems clear that the topology and shape which fit better with the substrate used is Hairpin & Chebyshev, respectively. Consequently, this filter will be designed using that scheme too. As usual, Table 4.19 shows design parameters, and figures 4.70, 4.71 and 4.72 the generated design.

Parameter	Value
Туре	Hairpin
Shape	Chebyshev
Input/Output Impedance	$50 \ \Omega$
Order	5
Attenuation at Cutoff	5  dB
Passband Ripple	$0.043~\mathrm{dB}$
Low Frequency Cutoff	$1450 \mathrm{~MHz}$
High Frequency Cutoff	$1550 \mathrm{~MHz}$

 Table 4.19 – 1.5 GHz Bandpass Hairpin Filter Design Parameters

It is appreciable that design parameters are almost equal to the used for the 2.4 GHz filter, except for frequency range, obviously. Regarding the issues already analyzed, in the 1.5 GHz Hairpin Filter, Insertion Losses are slightly lower, 4.58 dB (which was expected, because the frequency is also lower). As for size, this filter requires  $22.42 \,\mathrm{cm}^2$  of surface, more than the 2.4 GHz one. Assuming those facts as inevitable the filter behaves correctly with regard to low and high frequency cutoff and  $S_{11}$  parameter reaches -25.93 dB at central frequency, so it is chosen for this filtering stage.

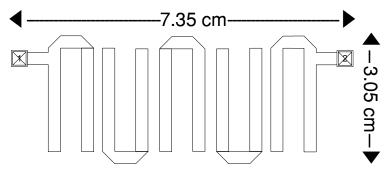


Figure 4.70 – 1.5 GHz Bandpass Hairpin Layout

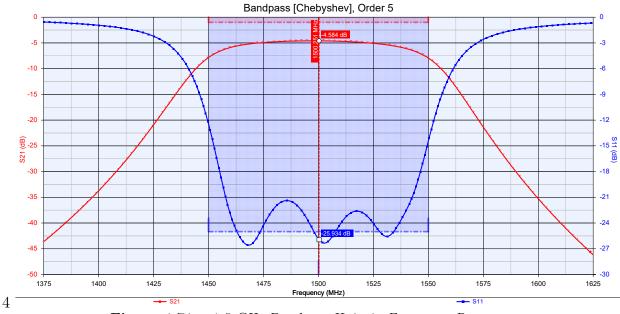
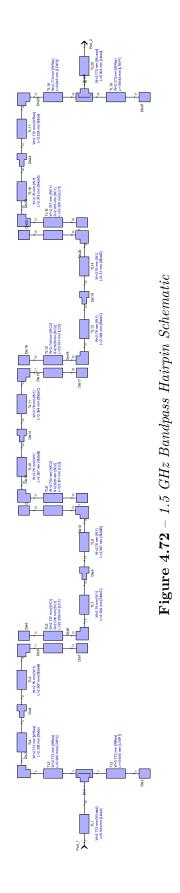


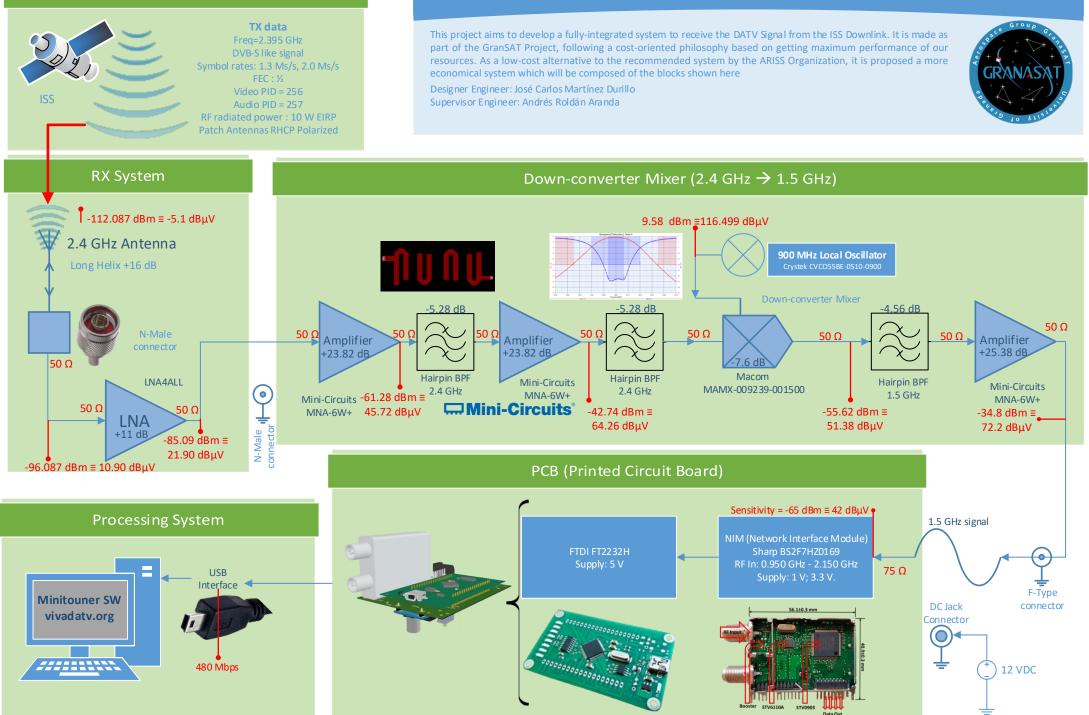
Figure 4.71 – 1.5 GHz Bandpass Hairpin Frequency Response

This completes the design regarding the functional components and stages of the mixer. Therefore, a new **block diagram**, equivalent to the one shown in figure 4.1.3.1 can be composed. The final composition of the system is shown here. It shows again a power balance for the whole system, from the receiving antenna to the PC. Insertion Losses at filters, conversion losses and of course gains have been taken into account, showing how the power varies through the system, finally reaching the tuner with an expected power of -34.8 dBm, far from the sensitivity limit (-65 dBm). Although it must be reminded again the approximate character of these power calculations, it provides a valuable analysis of the feasibility of the design. For instance, wire losses, measured in 4.35, have not been considered, as well as Insertion Losses of the connectors, or little mismatches occurring at the system, (for example, between the mixer output and the tuner), so actual power would be lower. Nevertheless, considering the available margin existent until the sensitivity limit



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## TX System



### DATV Receiver for ISS Downlink

of the tuner, the design is **accepted**.

At this point, the mixer can be implemented using  $ADS^{\textcircled{B}}$ .

ADS<sup>®</sup> is a powerful tool widely used for RF, microwave and high speed electronics design. It is based in the philosophy Schematic Design  $\rightarrow$  Simulation  $\rightarrow$  Layout. Then, this will be the procedure followed.



Figure 4.73 – ADS Design Typical Procedure

Besides the devices which compose the mixer, it is formed by **transmission lines** in Microstrip Technology. Given the frequency of work (Microwave range), Reflection Losses are a capital issue to prevent the system not only from losses but also from damages to the different components. Reflection Losses are avoided by matching impedances between the different components and the transmission lines. Impedance in Microstrip Technology lines depends mostly of their widths, and it varies with frequency. Therefore, the first step will be calculating the width corresponding to the different frequencies of work involved in the system.

Microstrip Technology width calculation can be performed through experimental expressions developed throughout the second half of XXth century. Numerous authors have developed different equations of diverse complexity and accuracy, see Wheeler [63], Owens [52], Kobayashi [50] or Hammerstad [44]. Nowadays, it does exists various software which makes it possible to automatically calculate the width for an impedance given. For that reason, expressions corresponding to the authors cited will not be directly applied here. Using those software solutions is preferable not only because of ease and speediness but also because they are programmed to use complex expressions instead of the simplified ones, which increases accuracy. To assure accuracy, the width will be calculated using two different software: on the one hand **Saturn PCB Design** and secondly directly with the tool incorporated in ADS<sup>®</sup>.

Saturn PCB Design is a really versatile tool which offers a complete set of possibilities for PCB Design. Each one of these possibilities is available choosing one of the tabs in its main interface. For conductor impedance, 'Conductor Impedance' tab must be selected. In this software, instead of indicating the desired impedance to obtain an adequate width, impedance is calculated depending on the width set, as well as the substrate parameters and frequency of work. Figure 4.74 shows the calculation using Saturn PCB Design software for the trace width corresponding to the 2.4 GHz area.

	stalk Calculator	Wavelength Calcula		Ohm's Law	Reactance
ia Properties Conductor Properties Bandwidth	& Max Conductor				
Conductor Spacing Conductor Impedance	Conversion Data	Planar Inductors	Plane Calculator	Thermal F	using Current
Conductor Impedance Conductor Width (W) 133 mils A Conductor Height (H) 62 mils Frequency (MHz) 2400 Note: This calculator uses a complex formula, not the formula. Results track the Sonnet 3D solver.	e simplified	С	Options Base Copper Weight 0.25oz 0.5oz 1oz 2.5oz 2.5oz 4oz 5oz Plating Thickness Bare PCB 0.5oz 1.5oz 2.5oz 2.5oz 2.5oz 2.5oz 2.5oz 2.5oz 2.5oz 2.5oz 2.5oz 2.5oz 2.5oz 2.5oz 2.5oz 2.5oz 2.5oz 2.5oz 2.5oz	Units Imperial Metric Substrate Material See Custom Er 3,963 Temp Rise 20 Temp in (9)	Tg (°C)       130       (°C)
J←w→ ↓	Lo <b>7.4448</b> Co <b>2.9692</b> Tpd		<ul> <li>3oz</li> <li>Passive Circuits</li> <li>Microstrip</li> <li>Microstrip Embed</li> <li>Stripline</li> <li>Stripline Asym</li> <li>Dual Stripline</li> <li>Coplanar Wave</li> <li>Information</li> <li>Total Copper Thickness</li> <li>2.10 mis</li> </ul>	Ambient T 22 Temp in (°) Print Via Thermal N/A	(*) (*) (*) (*) (*) (*) (*) (*) (*) (*)
SATURN	Follow Us		Conductor Temperature Temp in (°C) = N/A Temp in (°F) = N/A	Via Count: 1 N/A Via Voltage N/A	Ŧ

Figure 4.74 – Trace Width Calculated using Saturn PCB Design

Black Box (D) shows the impedance calculated according to the rest of parameters, as well as inductance of the trace, among other data. Red Box (A) is used to iterate with the different widths; it is changed until obtain the 50  $\Omega$  desired in (D). Finally Blue Box (B) and Green Box (C) are used to set the parameters regarding the substrate used, the technology (Microstrip Technology) and the frequency of work. According to Saturn PCB Tool, to obtain 50  $\Omega$  impedance with this substrate, at 2.4 GHz, the width must be 133 mils.

The second option to calculate the width is an integrated tool in ADS<sup>®</sup>, called LineCalc. It allows using the same procedure applied with Saturn or the inverse, directly setting the desired impedance. Figure 4.75 shows the result.

LineCalc/unti Simulation								- 0
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mponent								
pe MLIN	▼ ID M	LIN: TL2		•				
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Er	3.963	N/A	~			N/A	~	
Mur	1.000	N/A	~			N/A	<b>v</b>	
Cond	1.0E+50	N/A	~	Synthesize	Analy			Calculated Results
Hu	3.9e+034	mil	•			▼		K_Eff = 2.805
т	35.000	mil	•	Electrical				A_DB = 0.227
TopD	0.015	NI/A	. Y	ZO	50.000	Ohm	-	SkinDepth = 0.000
Component Par	ameters			E_Eff	230.000	deg	-	
Freq	2.400	GHz	•			N/A	~	
Wall1	1.0E+30	mil	•			N/A	v	
Wall2	1.0E+30	mil	-			N/A	$\nabla$	

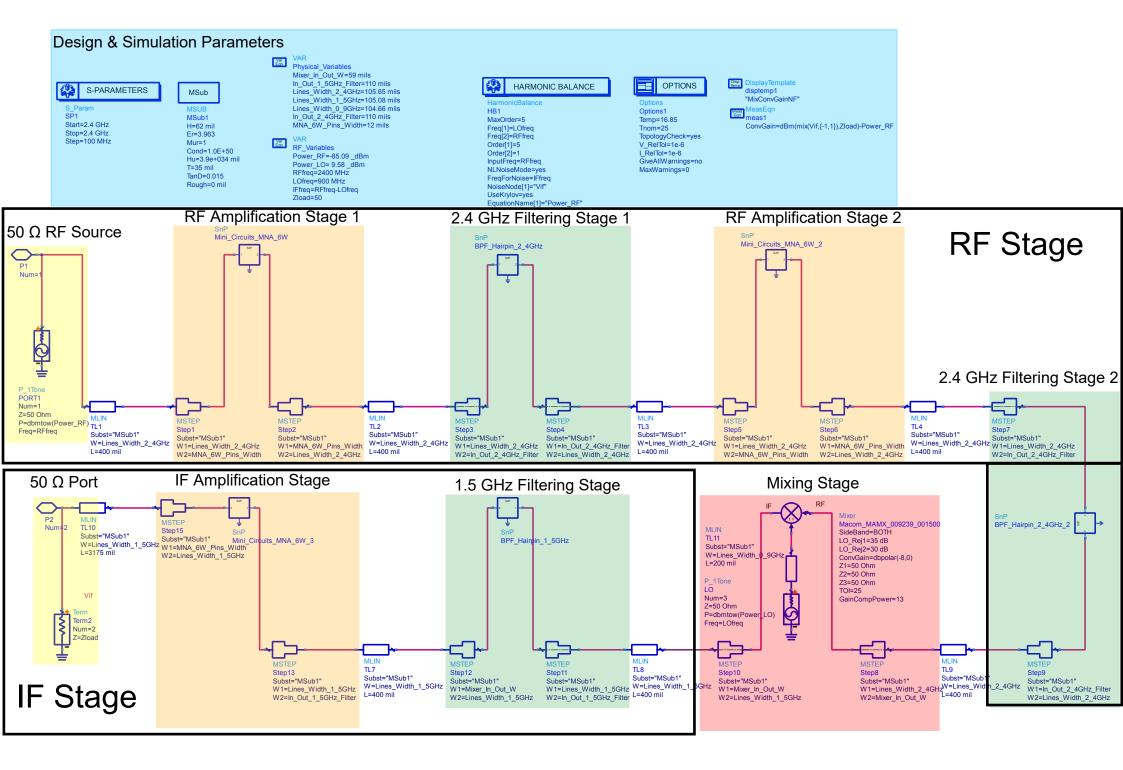
Figure 4.75 – Trace Width Calculated using LineCalc from ADS®

The functioning is very similar to Saturn. After indicating substrate characteristics and frequency of work, in this case, *Synthesize* option is used, **obtaining 106.46 mils as width 50**  $\Omega$  **at 2.4 GHz**. Although it may look like a large difference (27.35 mils) compared to the result given by Saturn, 26.54 mils equals to 0.67 mm, which is an acceptable of accuracy for the majority of manufacturing processes. This is undoubtedly because they use different expressions to calculate the width, among the numerous available, as stated before. For the sake of simplicity, given that  $ADS^{\oplus}$  is the software used for the design, its result will be taken.

The same process is followed to calculate the width at 1.5 GHz, (Intermediate Frequency), obtaining **105.08 mils**. It is a tiny difference  $(35.5 \,\mu\text{m})$  with respect to the 2.4 GHz width, definitely negligible. The only width left to calculate is the one corresponding to the 900 MHz line (from the VCO to the mixer). The calculation process yields to a width of **104.7 mils**, whose difference with respect to the first is negligible again.

Once every Microstrip Technology line width is calculated, it can be assembled the schematic of the mixer. It is included, along with some blocks to illustrate the different parts which compose it.

The schematic is built following the same structure analyzed in the block diagram, and it is also similar to the one analyzed in DG0VE KON13-900. Each part corresponding to RF and



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IF have been marked, as well as each one of the different stages. The initial and the last stage are 50  $\Omega$  terminations, with the first one functioning also as RF Source, generating a signal of frequency and power indicated in the parameters. In addition, several **amplification stages** have been included, corresponding to the amplifier selected in 4.1.3.2.3.2, MNA-6W+. In order to perform the simulation, an *N-Port S parameters* block has been used for every amplifier, loading the S-Parameter file provided by Mini-Circuits for this device. Regarding filtering stages, a similar procedure has been followed, the same block is used to model the filter using S-Parameters obtained from Keysight Genesys RF<sup>®</sup>, for both 1.5 GHz and 2.4 GHz. Mixer and VCO have been modelled with generic libraries from ADS<sup>®</sup>, which have been characterized with the information provided by the manufacturer. Finally, Microstrip Technology lines have been used to connect every stage, with the corresponding width, indicated in the Parameters section. Also, **MSTEP** blocks have been used to model the effects of stepping to a narrow or wider widths, (which occurs, for instance, when attacking the terminals of some devices). The schematic is shown, as usual, in vector format, which allows the reader to analyze it closer for further details.

## 4.1.3.2.3.3 ADS Simulation

With the schematic composed and analyzed, the next step is performing an appropriate simulation which allows to confirm the functioning of the system. Mainly, two types of simulation will be executed: isolated ones, to assure the correct behavior of each one of the blocks, and a global **Harmonic Balance** Simulation, to check the global functioning of the mixer, by studying the harmonics present at the output.

Previously, simulation parameters have been set, apart from the ones corresponding to the substrate used. Generally speaking, simulation parameters are used to fix frequencies of work (RF and LO) and their corresponding powers, and to set significant parameters for **Harmonic Balance** Simulation. Firstly, isolated simulations will be performed, and the process will conclude with the mixer simulation.

## • Isolated Simulations

## Amplifier: MNA-6W+

To simulate the amplifier used, it is isolated and connected to 50  $\Omega$  terminations, just as would be in the complete design. Given that it is internally matched to that impedance, there must no be significant reflections. The simulation performed shows its behavior as a two-ports network, by the analysis of its S-Parameters. The results are shown in 4.76

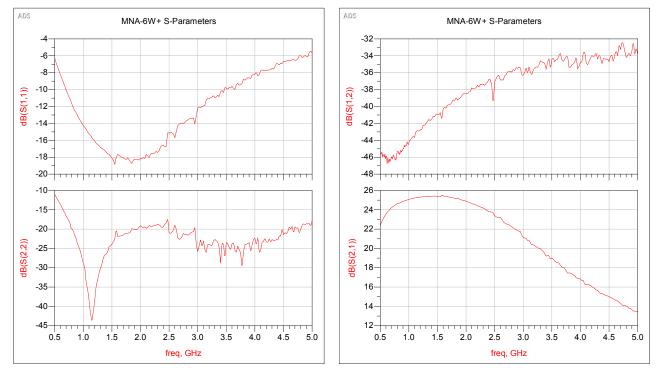


Figure 4.76 – MNA-6W+ S-Parameters

Every plot is in dB, in the range of frequency given by Mini-Circuits. Particularly, at the frequencies of interest, simulations yield the results shown in table 4.20.

Parameter	$1.5~\mathrm{GHz}$	$2.4~\mathrm{GHz}$
$S_{11}$	-18.09 dB	-16.59 dB
$S_{22}$	-23.86  dB	-19.4  dB
$S_{12}$	$-40.89~\mathrm{dB}$	$-36.78 \mathrm{~dB}$
$S_{21}$	$25.38~\mathrm{dB}$	$23.82~\mathrm{dB}$
O C Damar	motore at the	fragmonica

 Table 4.20 – S-Parameters at the frequencies of interest

 $S_{11}$  and  $S_{22}$  plots confirm the impedance matching mentioned, reaching values below - 10 dB practically in the whole range, and near -20 dB at the frequencies of interest. On the other hand, gain ( $S_{21}$ ) reaches the expected value too, with about 24 dB at both frequencies. Final, MNA-6W+ exhibits excellent **reverse isolation**, ( $S_{12}$ ), with -40.89 dB and -36.78 dB, respectively.

In conclusion, when isolated the amplifier behaves as expected at the frequencies of interest and it can be included in the global simulation.

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#### Filtering Stage: 2.4 GHz

In this case, the 2.4 GHz filter corresponding to the two first filtering stages is isolated and simulated. Given that input and output impedances of the filter have been designed for 50  $\Omega$ , once again, terminations for that impedance are connected to the filter, as shown in figure 4.77.

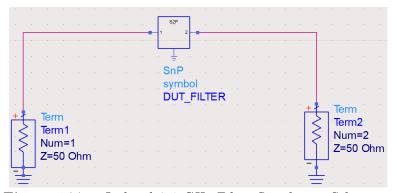


Figure 4.77 – Isolated 2.4 GHz Filter Simulation Schematic

After simulation, results of figure 4.78 are obtained.

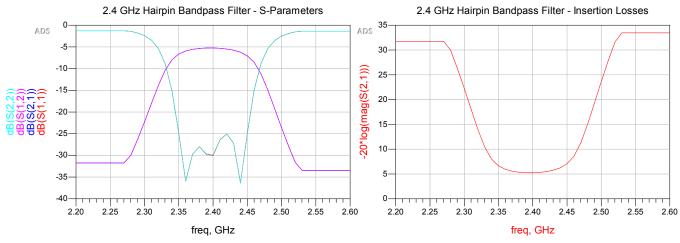


Figure 4.78 – 2.4 GHz Hairpin Bandpass Filter Simulation

The first plot, on the left side, shows S-Parameters Simulation. As expected, they are in accordance with the one obtained in Keysight Genesys  $RF^{\oplus}$ , exhibiting an adequate behavior at the bandpass, (considering the issues mentioned), covering the whole range of the TX signal. Notice that  $S_{11} = S_{22}$  and  $S_{12} = S_{21}$  because the filter is a linear passive network and it also symmetric.

The plot on the right side shows Insertion Losses, which are about 5 dB as analyzed

during filter design.

Therefore, the **2.4 Bandpass filter** behaves as expected in isolation and **it can be** included in the global simulation.

## Filtering Stage: 1.5 GHz

The same process is repeated for the filter at 1.5 GHz. The results are exposed in figure 4.79.

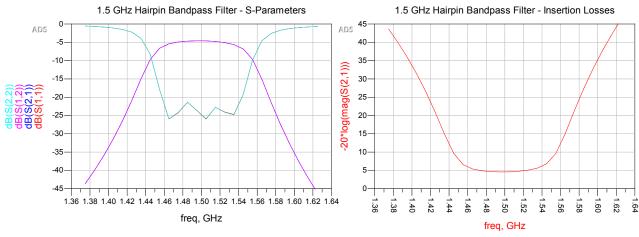


Figure 4.79 – 1.5 GHz Hairpin Bandpass Filter Simulation

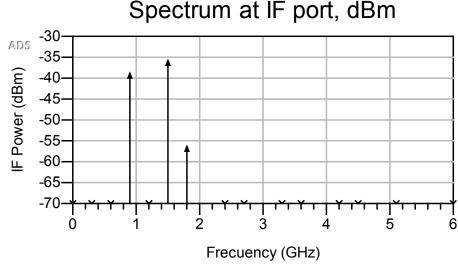
First plot confirms the result obtained when designed, and the behavior of a linear passive symmetrical network is appreciated once more. On the other hand, Insertion Losses are calculated at the second plot, reaching a minor value at the bandpass in this case, as expected.

As a consequence, the **1.5 GHz filter is considered valid** to be included at the global simulation.

## • Harmonic Balance Simulation

After simulate amplification and filtering stages of the design, the whole simulation of the system can be performed. It also implies simulating the stages left, Mixer and VCO which, because of their character, are simulated as part of the **Harmonic Balance**.

Harmonic Balance Simulation is performed to calculate the response of nonlinear circuits, such as a mixer. In this case, it is used to analyze the harmonics of the signal at the output of the mixer, which ideally will be composed only of the desired **Intermediate Frequency** at 1.5 GHz and with a power superior to -65 dBm, which was the sensitivity of the NIM. From the noise contribution of each one of the components, the **noise figure** is also estimated



from the simulation. Figure 4.80 shows the spectrum at the output port.

Figure 4.80 – Spectrum at the Output Port of the mixer

It can be seen how three harmonics reach the output of the mixer with a non negligible power, summarized in table 4.21.

Harmonic Frequency (MHz)	Power (dBm)
900	-38.72
1500	-35.67
1800	-56.22

Table 4.21 – Harmonics present at the Output Port

Given that the output port is the final step before reaching the NIM, they must be analyzed from its point of view. Obviously, there are one desired harmonic at **1.5 GHz** (IF), and two undesired. The first one, at 900 MHz, comes from the LO Frequency and it is out from the input frequency range of the tuner, so it is not a problem. The second undesired harmonic is at 1.8 GHz (2·LO) with a power of -56.22 dBm. It is within NIM bandwidth, but considering the losses not taken into account mentioned before (wire, connectors, etc.) it is likely to be at the sensitivity limit in real functioning (-65 dBm). Finally, the desired harmonic is also within sensitivity range, (with a power of -35.67 dBm), which was the initial aim, so the design has proved to be correct under **Harmonic Balance** simulation conditions. Particularly, a **conversion gain** of 49.42 dB has been estimated.

Regarding **Noise figure**, simulation yields a value of 3 dB. The main sources of noise are shown at table 4.22.

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Noise Contributor	Noise Voltage Contribution (nV)
RF Amplification Stage 1	135.1
RF Amplification Stage 2	16.01
2.4 GHz Filtering Stage 1	13.14
<b>Table 4.22</b> – $M$	ain Noise Contributions

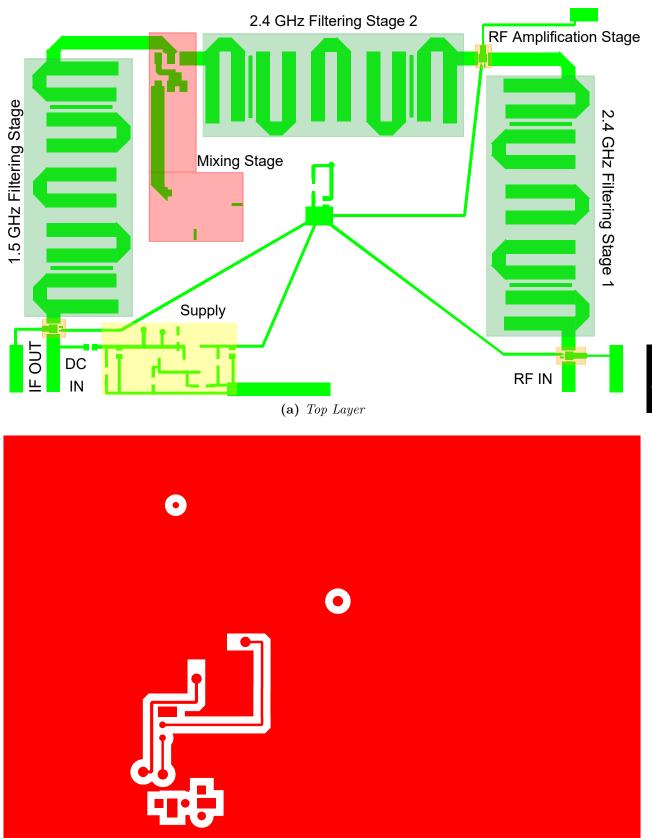
It is noticeable how the main noise contributor is, by far, the first Amplification Stage. It is, however, an already pointed fact: in the same way that the LNA is obliged to have a low noise figure because it is the first stage of the system and it dominates the overall noise figure of the whole system, the first stage of the mixer is also the main contributor to the noise figure of the device. Comparing with the analyzed mixer, see 4.10, noise figure is 1 dB higher whereas Gain is 9 dB lower. They are acceptable results taking into account that most part of the design has been made with *off-the-shelf* components and economical and not recommended for microwave design substrate, FR4.

With this finishes the simulation process, the only step left is designing the layout.

## 4.1.3.2.3.4 ADS Layout

At this point, the only remaining procedure of the design process shown in 4.73 is the layout. Although the concept is the same applied at 4.1.2, i.e., establishing the physical connections between the components of the device, the way to do it changes completely, again because of the frequency of work. The design of the layout is performed using the Momentum, a powerful tool included in ADS<sup>®</sup> for this purpose. Besides of the components analyzed in section 4.1.3.2.3, the layout is composed of some passive ones such as capacitors or resistors when necessary.

Figure 4.81 shows Top and Bottom Layers of the proposed layout, respectively. Besides, figure 4.83 shows the composition of both layers, illustrating the final result. In figure 4.81a, it has been added several blocks as in schematic design, to show the connection between both. Every stage has been marked except for amplification stage, which has been indicated just once, on the upper-right corner. RF Input is on the right side, followed by the first RF Amplification Stage and also the first Filtering Stage, at 2.4 GHz. After that, another block composed RF Amplification Stage + Filtering Stage at 2.4 GHz. Then, the signal attacks the Mixing Stage, composed of the VCO and the Mixer. The signal is down-converted and the IF signal goes through the last Filtering + Amplification Stage, before reaching the output of the mixer. Active devices are also supplied from the IF OUT port, which is at the same time, the DC IN port. The signal flow is exactly the same as the exposed at schematic design.



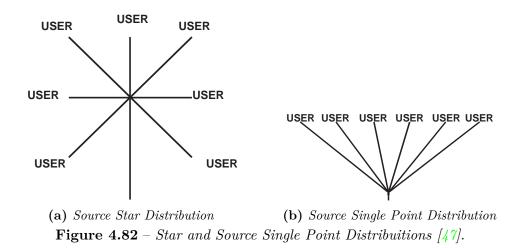
(b) Bottom Layer Figure 4.81 – Proposed Layout

DATV Receiver System Design and Development

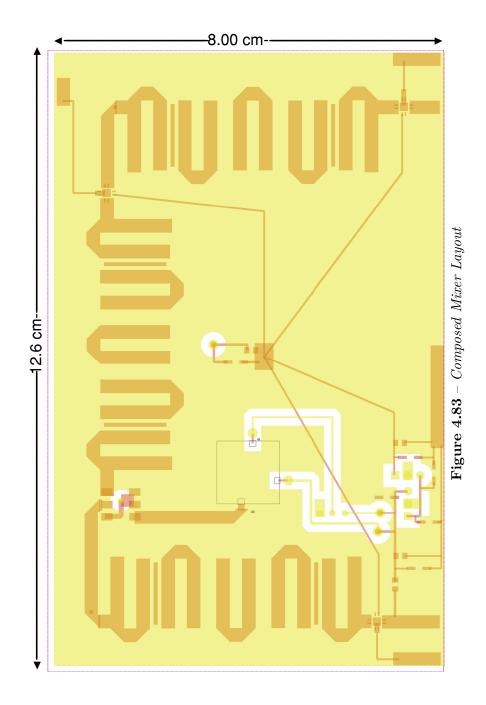
4

Some aspects regarding the layout deserve to be mentioned:

- The mixer is expected to have a metallic package as DG0VE KON13-900 does, see figure 4.34; it is used as ground along with the Ground Plane at the bottom layer. For this reason, prudential distance has been respected between the different traces and the Border Outline. Because of the behavior of the fields in a line designed using Microstrip Technology, see figure 4.38a, the presence of a metallic material near enough the line can provoke undesired Reflection Losses and unpredictable behaviors. Respecting that distance allows the fields to fall onto the substrate, as desired.
- Star Distribution has been used for routing supply traces. In this distribution, every supply trace references to the same point, located centrally and using same length traces, approximately, reducing noise. In addition, small area power plane has been used at the center, along with 100 nF decoupling capacitor and also a electrolytic capacitor to prevent the supply voltage from becoming unstable.



- Long narrow traces are used to design supply nets, providing them with a significant inductance, easing the flow of the DC and blocking high-frequency noise.
- Large Ground Plane is used at the Bottom Layer, minimizing the inductance. Only the VCO supply and voltage tuning are routed through Bottom layer.
- **RF** Areas are isolated when possible, keeping a prudential distance from supply traces and also avoiding traces below them.
- Small Area Ground Planes are used at some points of the design, to avoid using vias which increase parasitic inductance. They are soldered to the metallic package, which at the same time is soldered to the Ground Plane of the Bottom Layer. In conjunction, a large low impedance Ground Plane is accomplished.
- A variable resistor is implemented, which allows tuning the VCO and changing the LO frequency.



## DATV Receiver System Design and Development

The main drawback of the design, as mentioned in 4.1.3.2.3.2, is size. Large filtering stages increase the total size of the mixer significantly. Different techniques to solve this problem have been also mentioned in 4.1.3.2.3.2.

This concludes the mixer design. The next step would be getting it manufactured and measuring it as made with DG0VE KON13-900 in section 4.37.

## 4.2 Software

In this section, the software setting-up previously needed will be explained. As exposed in 3.1.1, **Minitioune** software, developed by Jean Pierre F6DZP at Viva DATV will be used.

The major part of the process is oriented to install the drivers necessary for the PC to adequately recognize the FTDI and to program it. The first step is installing the drivers provided by FTDI, see [10]. It is a standard installation process, which finalizes with the notification shown in 4.84 indicating that the drivers have been correctly installed.

Asistente para la instalación de controladores de dispositivos

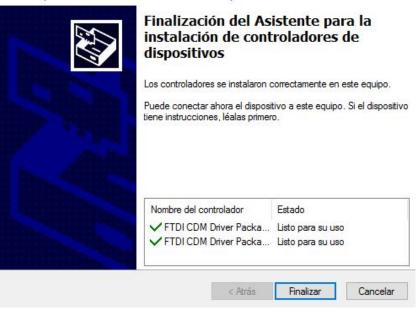


Figure 4.84 – Drivers OK notification

Once the drivers are installed, it is necessary the utility to program the chip, FT Prog, see [13]. Again it is installed following an usual process. After installing, the FTDI must be connected to the PC, (high quality USB cable is recommended), and the program will show something similar to figure 4.85.

File devices help ] 😂 🛃   🖻 +   🔎 🥖   🏧		
Device Tree	Property	Value
	Chip Type: Vendor ID: Product ID: Product Desc: Serial Number: Manufacturer Desc: Location ID: EEPROM Type:	'FT2232H' 0x0403 0x6010 'FT2232H MiniModule' FTWTCQER 'FTDI' 0x 0x131 93C56 EEPROM
	Property FTDI Device	
		device, the treeview gives a EEPROM contents. Expand for more
Device Output Device: 0 [Loc ID:0x1151]	representation of the	device, the treeview gives a EEPROM contents. Expand for more

Figure 4.85 – FT Prog before Programming

In order to facilitate the programming, Jean Pierre, software author, provides with a template which includes the parameters needed. It is also available at Viva DATV. It is an **xml** file which, once downloaded is loaded into FT Prog by clicking at the **Device**  $\rightarrow$  **Apply template**  $\rightarrow$  **From file**. After applying the template, an 'Operation Successful' message will be shown and now FT Prog will look like figure 4.86

This finalizes the process of FTDI drivers installation and programming.

At this point it is necessary to install certain software to allow Minitioune to work correctly. The first one is called **GraphStudioNext** and it is available at [14]. It is used to allow Minitioune to read the graphs files which show the structure of the decoded data. It is also needed to install another software later. Installation is a routine process again.

Second software is **LAVFilters**, available at [19] and it allows decoding the received stream. Finally, a particular filter is needed, which is downloaded together with Minitioune and is called **usrc.ax**. To install it, GraphStudioNext is opened and from **Graph** Menu, *Insert Filter* is selected, and file usrc.ax is chosen. The process will be finished by clicking

EEPROM V FLASH ROM		
FILE DEVICES HELP		
🗋 🚰 🛃 i 🖻 📲 🔎 🖉 i 🏧		(
Device Tree	Property	Value
Device: 0 [Loc ID:0x131]     Device: 0 [Loc ID:0x131]     Device Descriptor     USB Device Descriptor     USB Config Descriptor     USB String Descriptor     Device: 0 USB String     Device: 0 USB String Descriptor     Device: 0 USB String D	Chip Type: Vendor ID: Product ID: Product Desc: Serial Number: Manufacturer Desc: Location ID: EEPROM Type:	'FT2232H' 0x0403 0x6010 'USB <-> NIM tuner' DA1EEOOA 'FTDI' 0x131 93C66 EEPROM
Port B → Hardware → UART → 245FIFO → CPUFIFO → OPTO → Driver → IO Pins		ice, the treeview gives a representatio . Expand for more detail.
→ Hardware → UART → 245FIFO → CPUFIFO → OPTO → Driver → IO Pins	FTDI Device The connected FTDI devi	. Expand for more detail.
Device Output $ \begin{array}{c} \hline \\ \hline $	FTDI Device The connected FTDI devi of the EEPROM contents	. Expand for more detail.
Device Output Device: 0 [Loc ID:0x131] Word MSB	FTDI Device           The connected FTDI devior           of the EEPROM contents           008 3333 0A9A           000 0000 0000           00 0000 0000           00 0000 0000           00 0000 0000	. Expand for more detail.

Figure 4.86 – FT Prog after Programming

## on **Register**.

After rebooting, the software needed for the functioning of the system will be ready to be used.

José Carlos Martínez Durillo

# CHAPTER

# - 5

# CONCLUSIONS AND FUTURE LINES

Through this document it has been shown the analysis, design and development of a system to receive DATV signal. Although it was not an actual order from an enterprise, one of the purposes of this Bachelor Thesis was treating it from a commercial approach. It has allowed the student to get closer to its professional activity, by following standard development & design procedures, and handling specialized widely used software, not only from the engineering field, but also tools for document preparation and markup language, such as LATEX.

From the student's perspective, the realization of this Bachelor Thesis has supposed a true challenge. A vast amount of problems to solve have arisen whose resolution sometimes required of applying the knowledge acquired throughout the degree. Often, however a completely new scenario for the student emerged and it required to initiate an analysis and study stage to be able to solve the problem. Actually, another purpose of this Bachelor Thesis was facing a multidisciplinary problem which allow applying abilities and gain knowledge of every Telecommunications branch, specially Electronics and Communications.

At the same time, a product-oriented philosophy has been followed. From the initial *costumer* requirements, an engineering process was applied: analysis of the requirements, evaluation of the system, system design, budget estimation, etc. In essence, an optimum solution from every point of view of a Product Development Process has been sought.

Nevertheless, some improvements and or future lines of work have naturally arisen during the development of this Project, for instance:

- Changing the PCB Design, (see 4.1.2) in order to use a NIM whose bandwidth includes the 2.4 GHz band, so no **mixing stage** is required.
- With the goal of making the System completely portable, a **battery-based** supply could be studied. It should include an analysis of the charging process as well as the current which is able to provide in a certain moment, given the possibility of high consumption of the system.
- Regarding the mixer, studying the field of **filter miniaturization** with techniques such as compact open-loop, multilayer filters or hairpin resonators, in order to reduce the overall device size. Also, analyzing high Relative Permittivity substrates and their influence in the mixer size and behavio r.
- Design the structure of the mixer using **Grounded Coplanar Waveguide** Technology instead of Microstrip Technology. It allows more controlled impedance and it is a technology with a great future potential, given the growth of high frequency designs.
- Studying adequate prototyping techniques to manufacture the mixer, such as Laser Engraving.
- Design an adequate parabolic **dish** for the helix antenna proposed in 4.1.1.1 seeking to obtain a similar performance to the commercialized one proposed.
- From a commercialization perspective, the design of an adequate **package** is an essential issue for both PCB receiver and mixer.

As final conclusion, it must be remarked the huge knowledge, abilities and techniques that the student considers to have acquired through the completion of this Project, by spending countless hours of desk and laboratory.

Of course, this Project does not finalizes here. As in every development process, once the product is ready to be brought to market, it does start the *Under Operation* stage, in which feedback from clients will be crucial to fix possible problems and to improve the product in future versions.

The future is exciting.



José Carlos Martínez Durillo

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## APPENDIX

А

# PROJECT BUDGET

## A.1 Hardware Cost

In this section, project cost regarding hardware sections will be detailed. Each one of the different hardware stages is differentiated. Human resources will be detailed at the end.

## A.1.1 Receiving Antenna Cost

According to the System Design, 4, the Long Helix Antenna is chosen to be the receiving antenna of the system. It has a cost of  $122 \in$ . Tasks related with measurement and characterization of the different antennas analyzed are considered indirect costs and are detailed in table 5.9.

## A.1.2 LNA Cost

Regarding LNA choice, a low-cost one is selected, with a cost of  $20 \in \mathbb{C}$ .

### A.1.3 Mixer Cost

Mixer budget has higher complexity because of the greater number of components. They are shown, along with their cost, in table 5.8. Indirect costs are also computed in table 5.7. On the other hand, a summarized table showing the total cost of the mixer can be found in

Item	$\begin{array}{c} \text{Cost} \\ (\textbf{\textit{\in}}) \ (\text{-IVA}) \end{array}$	$\begin{array}{c} \text{Cost} \\ (\textbf{\textit{\in}}) \ (+\text{IVA}) \end{array}$
Components	42.19	51.047
Indirect Cost	335	405.34
Human Resources	41.32	50
LPKF ProtoMat S62 Renting	4.13	5
TOTAL	422.64 €	511.4 €

A.1; human resources and renting of the milling tool attributable to mixer design are not actually part of its manufacturing so they are not computed separately.

Table A.1 – $Mixe$	r Development Cost
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## A.1.4 PCB Receiver Cost

Regarding the PCB Receiver, its cost can also be divided in various items: manufacturing and human resources cost and component cost. Table A.2 shows the first, whereas 5.6 details the second and A.3 the total cost of the PCB Receiver.

Item	Cost (€) (-IVA)	$\begin{array}{c} \text{Cost} \\ (\textbf{\textit{\in}}) \ (+\text{IVA}) \end{array}$
Human Resources	41.32	50
LPKF ProtoMat S62 Renting	4.13	5
Definitive Prototype	18.18	22
TOTAL	44.45 €	55 €

Table A.2 – PCB Receiver Manufacturing and Human Resources Cost

Item	Cost (€) (-IVA)	$\begin{array}{c} \text{Cost} \\ (\text{€)} \ (\text{+IVA}) \end{array}$
Components	54.31	65.72
Human Resources	41.32	50
LPKF ProtoMat S62 Renting	4.13	5
TOTAL	99.73 €	120.72 €

 Table A.3 – PCB Receiver Total Cost

## A.2 Software Cost

Software	License Owner	Cost (€)
Altium Designer 16	UGR	Free
Solidworks 2015	UGR	Free
Keysight Genesys RF	Author	Demo
Keysight ADS	UGR	Free
$\operatorname{CST}$	Author	Demo
MatLab 2014	UGR	Free
TeXnicCenter	Author	Free
Miktex	Author	Free
SumatraPDF	Author	Free
	TOTAL	0€

This Project has required the use of different software. The price of the different suites used is detailed in table A.4

Table A.4 - Software Cost

## A.3 Human Resources Cost

Apart from the human resources derived of manufacturing process as the ones detailed in A.1 and A.2, this Project has required hiring two people. The first one is a **junior engineer**,  $(10 \notin /h)$ , hired as a part-time worker during twelve months. Secondly, as Project Supervisor a **senior engineer** is hired,  $(50 \notin /h)$ , computing 5 hours per week. Then, Human Resources amounts to **25440**  $\epsilon$ , as detailed in table A.5.

Post	Ti	ime (Hours)	Cost $(\in)$
Junior Engineer		1344	13440
Senior Engineer		240	12000
		TOTAL	<b>25440 €</b>
	<b>TT</b>	D	<i>a</i> .

Table A.5 - Human Resources Cost

	(Used)	(€) (-IVA)	Cust/u. (€) (+IVA)	) ( $(\in)$ (-IVA)	$(\in) (+IVA)$	Appl. Cost $(\in)$ (-IVA)	$(\varepsilon) (+IVA)$	erence
Diode S1AB-13-F	3(1)	0.2	0.24	9.3	11.25	5.58	6.75	es I
Diode S1ME3/5AT	3(1)	0.18	0.22	0.54	0.66	0.18	0.22	
TVS Diode P6SMB20CAT3	3(1)	0.33	0.4	0.99	1.20	0.33	0.4	
Diode MMSZ5233BT1	3(1)	0.11	0.13	0.33	0.39	0.11	0.13	
Ferrite Bead	10(5)	0.16	0.19	1.60	1.90	0.8	0.95	
Capacitors	25(15)	0.160	0.194	4	4.85	2.4	2.91	
Resistors	15(4)	0.017	0.020	0.26	0.3	0.068	0.08	
Nexperia 74HC10	3(1)	0.442	0.54	1.33	1.62	0.442	0.54	
FTDI FT2232HL Module	2(1)	13	15.73	26	31.46	13	15.73	
Sharp BS2F7HZ0169	2(1)	14	16.94	28	33.88	14	33.88	
LP3879MR-1.0	3(1)	1.72	2.08	5.16	6.24	1.72	2.08	
MC7805BD2TR4	3(1)	0.586	0.71	1.76	2.13	0.586	0.71	
NCP1117DT33G	3(1)	0.376	0.46	1.13	1.38	0.376	0.46	
LM2596 Module	2(1)	2	2.42	4	4.84	2	2.42	
Barrel Jack Connector	3(1)	1	1.21	3	3.63	1	1.21	
FR4 Laminate	× 1	8.26	10	8.26	10	8.26	10	
					TOTAL	54.31	65.72 €	
		Table 5.6 –	PCB Receiver (	PCB Receiver Components Costs				I
Element	% Dedica	% Dedicated Used	Dedication (months)	Depreciation Period (months)		$\begin{array}{c c} Cost & Appl \\ (\epsilon) (-IVA) & (\epsilon) (\end{array}$	Appl. CostAppl.( $\boldsymbol{\epsilon}$ ) (-IVA)( $\boldsymbol{\epsilon}$ ) (+	Appl. Cost $(\in) (+IVA)$
Agilent E5071C Renting Amritan MS2830A Renting	1(	100	0.21	60 60	27(	27000 9. 27000 1	94.5 1 164 1	114.35 198 44
SIIIIII I IOOOZAI	) T	2	11.0	0	LOT	ۍ ۱	£ 4	405.34 €

Item	Units (Used) (	Cost∕u. (€) (-IVA)	$\begin{array}{c} \operatorname{Cost/u.} \\ (\pounds) \ (+\mathrm{IVA}) \end{array}$	Cost (€) (-IVA)	$\underbrace{\operatorname{Cost}}_{(\in) \ (+\mathrm{IVA})}$	Appl. Cost (€) (-IVA)	Appl. Cost $(\in) (+IVA)$
Mini-Circuits MNA-6W+	5(3)	1.86	2.25	9.3	11.25	5.58	6.75
Macom MAMX-009239-001500		5.04	6.1	10.08	12.2	5.04	6.1
Crystek CVCO55BE-0510-0900	2(1)	17.90	21.66	35.80	43.32	17.90	21.66
L7809CV Through-Hole	4(1)	0.55	0.66	2.18	2.64	0.55	0.66
L7805CV Through-Hole	4(1)	0.42	0.51	1.69	2.04	0.42	0.51
Capacitors	15(6)	0.160	0.194	2.41	2.91	0.96	1.164
Resistors	15(2)	0.017	0.020	0.26	0.3	0.034	0.040
FR4 Laminate	, I	8.26	10	8.26	10	8.26	10
Male N-Type Connector	2(1)	1.19	1.44	2.38	2.88	1.19	1.44
Female F-Type Surface Connector		2.27	2.75	4.54	5.50	2.27	2.75
1					TOTAL	42.19 €	51.047 €
	% Dedicated Used	Dec (m		Depreciation Period (months)	(A)	ost A)	Appl. Cost (€) (+IVA)
Agilent E5071C Renting	100	0.25	C	60	27000 <b>TOTAL</b>	112.5 <b>112.5 €</b>	136.13 <b>136.13 €</b>
	Table	5.9 -	RX Antenna Indirect Costs	Costs			References