UNIVERSIDAD DE GRANADA

FACULTAD DE CIENCIAS

Departamento de Electrónica y Tecnología de Computadores

Advanced modeling of nanoscale multigate transistors for circuit simulation

Tesis Doctoral

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Granada 2012

Editor: Editorial de la Universidad de Granada
Autor: María Balaguer Jiménez
D.L.: GR 356-2013
ISBN: 978-84-9028-343-1

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Acknowledgements

I would like to use these lines to thank all the people who, in one way or another, have contributed to this research work. First and foremost I would like to thank my supervisor D. Juan Bautista Roldán for putting at my disposal all necessary means for this work to be done. Thank you for your invaluable help to fit the different modeling activities carried out during these years, for your advice and support. Without your encouragement and advices this work would not have been possible.

To my co-tutor during the initial research stage at the University of Granada, D. Francisco Gámiz Pérez for his help and support. I would also like to appreciate his work as head of the research group in nanoelectronics (TIC-216) which has made possible the development of this work.

I would also like to thank to Professor Benjamín Íñiguez and the members of the Departament d'Enginyeria Electrònica, Elèctrica I Automàtica at the Universitat Rovira i Virgili for their attentions during my stay at their department and the opportunity to participate in their research group. I would also like to give my sincere gratitude for having put at my disposal the resources needed to develop part of the work that constitutes this thesis.

To Fran, Luca, Noel and Isabel for the productive scientific discussions. Thank you or the ambiance created at our shared office.

To Andrés Godoy, and also Fran, Luca Isabel, Carlos and Curro for their contribution to this work in terms of the simulations provided for the models we present.

To Carlos Sampedro for having reviewed this thesis and contributed with his time to improve it.

To Encarni for her friendship, help and support during these years.

I would give special thanks to the rest of the members of the research group of nanoelectronics and the members of the Departamento de Electrónica y Tecnología de Computadores at the University of Granada.

To my family, thank you for your love, encouragement, and support.

PREFACE

In the past decades the semiconductor industry has dedicated great efforts to advance in the continuous reduction of electron device dimensions. Today, scaling also remains as one of the most important challenges from the technology viewpoint. The channel length of Field Effect Transistors (FETs) has passed from micrometers to tens of nanometers following the prediction of the well-known Moore's law, and this tendency goes on now, i.e. More Moore trend. The reduction of transistor dimensions is essential to increase the performance while the active area of integrated circuits is reduced. However, scaling has drawbacks that have to be solved for each technology node. Among them, it can be highlighted the increase of short channel, parasitic, reliability and variability effects.

To overcome the problems shown up in relation to scaling, new transistor architectures have to be investigated. One of the most widespread solutions available is the use of multi-gate transistors (MuGFETs) like Trigates, FinFETs or surrounding gate transistors (SGTs). Additionaly to the differences on the architecture, these devices can incorporate new materials for the channel like strained silicon and III-V substrates to enhance the low-field mobility. The materials that are being used for the transistor gate (metal gates) and insulators (high-κ dielectrics) offer great possibilities for nodes below 22nm. But the dimensions reduction does not only affect to the design of the device itself, the dramatic increase of the number of transistors on an integrated circuit introduces new issues to be solved like the concentration of dissipated power in relatively small hot spots within the chip, the influence of variability on important parameters (e.g. the threshold voltage) or reliability issues. The main implication is the increasing of the complexity of circuit architectures due to the applied techniques used to overcome these issues at both circuit and chip level. For this reason circuit simulators are essential in order to speed up the design process reducing cost. However it is necessary to develop accurate enough models to take into account the problems arising from ultimate scaling scenarios. In this context, with the introduction of the multi-gate devices and the difficulties of their inherent two-dimensional geometry, compact modeling has become an essential and encouraging activity. Despite there is a great number of research groups dedicated to this task, a lot of work remains to be done due to the wide variety of multi-gate transistor architectures and materials that can be found in the current fabrication landscape.

Dealing with MuGFETs devices implies developing new modeling techniques. It is very important to take into account quantum mechanical effects as well as the bidimensional features of the geometry, and also the particularities of the charge transport mechanisms, which are highly influenced by the high level of quantum confinement. In order to correctly reproduce the device behavior, all these features must be accurately integrated in compact models that can be implemented in circuit simulators. It is interesting to highlight at this point that when design houses choose a new technology; their decision is influenced by the availability of appropriate models that correctly work in design arena.

In this research work, some of the most important effects that show up in multi-gate devices are analyzed. Double gate MOSFETs (DGMOSFETs), surrounding gate transistors (SGTs) as well as Schottky barrier (SB MOSFETs) have been studied. Quantum effects have been analyzed in depth, and taken into account for DGMOSFETs and SGTs of different geometries both in mobility and inversion charge models. The most important feature of the models developed in this thesis lays on the simplicity of the mathematical equations used. In this respect, we have always focused on the development of models that could be easily implemented in circuit simulators.

This work is structured in five chapters. The first one includes an introduction of the current technological trends of the microelectronic industry; in particular, the lines followed for new FET devices development. An important part of this chapter is dedicated to SOI technology and multi-gate transistors, where issues arising from deep scaling are widely explained. The final section is dedicated to compact modeling, where current modeling techniques are analyzed and the future needs identified.

In the second chapter, the simulation tools used to develop the models presented in the following sections are described. The main characteristics of DGMOSFET and SGT simulators, developed by the Nanoelectronics group at the University of Granada, are described. One section of this chapter is devoted to ATLAS (from Silvaco) which has been used for the study of SB DGMOSFETs presented in chapter 4.

The third chapter is devoted to DGMOFET modeling. The influence of quantum mechanical effects on the inversion charge and the need to account for them in models has been deeply

studied. Another important part is dedicated to the characterization and modeling of the influence on the inversion charge of substrate crystallographic orientation in DGMOSFETs. Different models have been developed to take into account the effects previously explained. Finally, a current model including short channel, velocity overshoot, saturation velocity and quantum effects has been introduced merging some of the aforementioned models.

In chapter four the study and modeling of SB DGMOSFETs (devices with metallic source and drain contacts) is discussed. An advanced model for the current has been developed that correctly reproduces the main characteristics of SB DGMOSFETs charge transport, such us ambipolarity, tunneling at the source and drain contacts, gate induced drain leakage, etc. The model takes into account the most important transport mechanisms in these devices including all of them in a coherent, explicit and analytic model that can be easily used in circuit simulators.

The final chapter is dedicated to SGTs. A new model for the inversion charge has been developed taking into account quantum effects. The influence of these effects was studied in depth in a similar way as it was done for DGMOSFETs. Finally, the low-field mobility was characterized and modeled.

Most of the results included in this work have been published in different international journals (see chapter 8). Another part has been submitted for publication, including interesting results which are pending of publication in the short run (study of quantum effects on the inversion charge and mobility in SGTs, the final version of the current model for DGMOSFETs…). Some issues studied in this work will be enhanced in the future since they deal with hot topics. For example, different types of SB MOSFET will be analyzed and modeled, the models presented for the inversion charge and mobility will be adapted for different device architectures such us Trigates and FinFETs (see figure 6 in chapter 3), or parasitic current components in the latter devices will be studied and modeled.

General Objectives

The work presented in this thesis is devoted to the development of multi-gate MOSFET compact models. As it will be explained in depth in the manuscript, compact models are essential in the integrated circuit design landscape since the correctness of these designs depends absolutely on the accuracy of the device models and parameters of the technology used. It is well known that the current trend, in what transistors is concerned, is to reduce device dimensions. The continuous scaling described by Moore's law leads to the appearance of new physical effects that have to be incorporated in compact models. Consequently, the development of 22 nm technology node and beyond will demand new models including the latest characteristics linked to the novel geometries and fabrication trends. Among them, quantum mechanical effects, channel strain, velocity overshoot, short channel effects, parasitic currents, etc., must be taken into account. In this context, we have gone through an in-depth study of the major physical effects in multi-gate devices (in particular double-gate DGMOSFETs and surrounding gate transistors (SGTs), some of the structures proposed to substitute conventional bulk devices for the 22nm node and beyond) for compact modeling development purposes.

These compact models are based on explicit and relatively simple analytic expressions for the calculation of the charge and the current in the transistor. They can be easily introduced in circuit simulators. In this way, the main features of the transistor behavior can be reproduced.

Specific objectives

As already stated above, we have developed advanced models for three different kinds of transistors: DGMOSFETs, SB DGMOSFETs and SGTs. A dedicated chapter has been devoted for each device. In this respect, the specific objectives are briefly described as follows:

Despite DGMOSFETs have been widely studied and a great variety of models exist, we have stepped forward in the modeling state-of-the-art by introducing effects not included so far in a rigorous manner.

- In DGMOSFETs the role of the different channel crystallographic orientations has been taken into consideration to analyze the influence of quantum effects on the inversion charge.
- The development of a full inversion charge model accounting for n-type and p-type devices was undergone, the crystallographic orientation of the channel, the geometry of the devices and the operation regimen features were included.
- A complete characterization of the mobility in SG and DGMOSFETs has also been performed, where the role of Coulomb and surface-roughness scattering has been studied by means of Monte Carlo simulations. A model to account for the influence of the quality of the different semiconductor-insulator interfaces has been developed.
-Finally, a drain current model was developed integrating the models developed previously. It was to be based on the inversion charge of the device which was taken as state variable. Quantum effects, short channel effects, saturation velocity and velocity overshoot effects were considered.

SB DGMOSFETs were also studied. Metal contacts are used for drain and source in these novel devices in order to reduce the series resistance which is becoming one of the limiting factors in the scaling process. From the modeling (also from the fabrication) point of view these devices have a long way to go. There are very few models available and most of them are based on complicated numerical schemes where the tunneling currents are solved iteratively. For this reason we have considered the development of an explicit model for these transistors based on analytical expressions for circuit simulation purposes. The following goals have been completed.

- The drain current model previously developed was enhanced to account for the tunneling mechanisms needed to characterize the Schottky barriers that constitute the source and drain contacts.
- A Gate induced drain leakage scheme was added to the general model to account for the high currents observed for negative voltages.
- An ambipolar behavior was necessary to accurately describe the drain current curves. With all these physical mechanisms implemented the simulated curves were accurately reproduced for a wide variety of technological characteristics and operation regimes.

The third group of models developed is connected with SGTs. This type of multi-gate devices has the greatest potential to reduce short channel effects. These devices are much less studied than DGMOSFETs.

- In this case, we have also dealt with the analysis of quantum effects and their influence on the inversion charge. Different structures and sizes were considered.
- The low-field mobility was to be studied and modeled.
- An inversion charge model was developed to account for quantum effects considering different geometries and technological characteristics.
- We have also dealt with different types of insulators, materials with high permittivity to reduce parasitic tunneling currents. A model was also presented dependant on the insulator permittivity and other physical features.

Objetivos Generales

El trabajo presentado en esta tesis está dedicado al desarrollo de modelos compactos de MOSFETs multi-puerta. Como se explicará con detalle a lo largo de esta tesis, los modelos compactos son esenciales en el campo del diseño de circuitos ya que la precisión de estos diseños depende absolutamente de la bondad del modelo del dispositivo y de los parámetros de la tecnología empleada. El continuo escalado descrito por la ley de Moore lleva consigo la aparición de nuevos efectos físicos que han de ser incorporados a los modelos compactos. De esta manera, en los años venideros, para el nodo de tecnología de 22 nm y menores, serán imprescindibles nuevos modelos que incluyan las últimas características asociadas a nuevas geometrías y tendencias de fabricación. Entre ellas se encuentran los efectos mecánicos cuánticos, sustrato tenso, saturación de la velocidad, efectos de canal corto, corrientes parásitas, etc. En este contexto hemos estudiado los pricipales efectos físicos presentes en dispositivos multi-puerta desde el punto de vista del desarrollo de modelos compactos. En particular hemos estudiado los transistores MOSFET de doble puerta y los transistores SGT que son algunas de las estructuras propuestas para sustitutir a los transistores de sustrato tradicionales para el nodo de 22nm y menores.

Los modelos compactos desarrollados en este trabajo se basan en expresiones analíticas relativamente simples que permiten calcular la carga del transistor, la movilidad de bajo campo y la corriente. Estas expresiones pueden introducirse fácilmente en simuladores de circuitos y de esta manera se pueden reproducir la mayor parte de las características del comportamiento del transistor.

Objetivos específicos

Como hemos indicado anteriormente, se han desarrollado modelos compactos avanzados para tres tipos de dispositivos, los transistores MOSFETs de doble puerta (DGMOSFETs), los transistores SB MOSFETs y los SGTs. Los modelos desarrollados se han distribuido en tres capítulos que corresponden a cada tipo de dispositivo. Los objetivos específicos se detallan a continuación:

A pesar de que los transistores MOSFETs de doble puerta se han estudiado ampliamente y existen una gran variedad de modelos, en este trabajo hemos ido un paso más allá al introducir efectos no considerados hasta ahora en los modelos existentes.

- En el caso de los transistores MOSFETs de doble puerta el papel jugado por las diferentes orientaciones cristalográficas ha de ser tenido en cuenta para analizar la influencia de los efectos cuánticos en la carga en inversión.
- Se ha desarrollado un modelo completo para transistores tipo n y p, teniendo en cuenta la orientación cristalográfica del canal, la geometría de los dispositivos y las características de los distintos regímenes de operación.
- Se ha llevado a cabo una caracterización completa de la movilidad en transitores de puerta simple y doble a través de simulaciones de Monte Carlo con las que se ha estudiado el papel del scatering culombiano y por rugosidad superficial. Se ha desarrollado un modelo que tiene en cuenta la calidad de los distintos interfaces semiconductor-aislante.
- Finalmente se ha desarrollado un modelo de corriente que integra los modelos descritos previamente. Este modelo está basado en la carga en inversión del dispositivo. Para el que se han cosiderado efectos cuánticos y saturación de la velocidad.

Los transistores SBMOSFET también se han estudiado en esta tesis. En estos dispositivos novedosos se usa metal para los contactos de fuente y drenador para reducir de esta manera la resistencia serie que se está convirtiendo en uno de los factores restrictivos en el proceso de escalado en los transistores tradicionales. Desde el punto de vista del modelado (y también de la fabricación) estos dispositivos tienen un gran futuro. Hay muy pocos modelos disponibles y la mayoría de ellos están basados en esquemas numéricos complicados en los que las corrientes de túnel se resuelven de manera iterativa. Por esta razón hemos considerado el desarrollo de un modelo explícito para estos transistores basado en expresiones analíticas que puedan usarse en simuladores de circuitos. Los siguientes objetivos se han alcanzado:

- Se ha complementado un modelo de corriente previamente desarrollado para tener en cuenta los mecanismos de túnel necesarios para caracterizar las barreras Schottky que forman los contactos de fuente y drenador.
- Se ha añadido al modelo de corriente general un modelo de gate induced drain leakage (GIDL) para tener en cuenta las grandes corrientes observadas para voltajes negativos.
- El desarrollo de un modelo ambipolar es necesario para describir adecuadamente las corrientes de drenador. Con todos estos mecanismos físicos implementados las curvas

simuladas se han reproducido correctamente para una gran variedad de características tecnológicas y regímenes de operación.

El tercer grupo de modelos está relacionado con los transistores SGTs. Este tipo de dispositivos multi-puerta tiene un gran potencial para reducir los efectos de canal corto. Estos dispositivos han sido mucho menos estudiados que los transistores de doble puerta.

- En este caso hemos incluido el análisis de efectos cuánticos y su influencia en la carga en inversión. Hemos considerado diferentes estructuras y tamaños.
- Hemos desarrollado un modelo de carga en inversión para tener en cuenta los efectos cuánticos considerando diferentes geometrías y características tecnológicas.
- Se han considerado diferentes tipos de aislantes, matriales con alta permitividad para reducir corrientes de túnel parásitas. Hemos presentado un modelo dependiente de la permitividad del aislante y de otras características físicas.

Resumen

En las últimas décadas la industria de los semiconductores ha dedicado gran parte de sus esfuerzos a reducir las dimensiones de los dispositivos electrónicos, siendo el escalado uno de los desafíos más importantes desde el punto de vista de la tecnología. La longitud del canal de los transistores de efecto campo (FET) ha pasado de varios micrómetros a decenas de nanómetros siguiendo la predicción de la conocida ley de Moore y esta tendencia continua. La reducción de las dimensiones del transistor es esencial para incrementar las prestaciones a la vez que el área activa de los circuitos integrados se reduce. Sin embargo, el escalado tiene una serie de desventajas que tienen que resolverse para cada nodo de tecnología. Entre estas hay que señalar el incremento de una serie de efectos como los de canal corto, los parásitos, de fiabilidad y de variabilidad.

Para solucionar los problemas relacionados con el escalado de las dimensiones de los dispositivos se han investigado nuevas arquitecturas. Una de las soluciones más extendida es el uso de transistors multi-puerta (MuGFETs) como los trigate, FinFETs o los SGTs junto con la incorporación de nuevos materiales para el canal como silicio tenso y sustratos III-V para aumentar la movilidad de bajo campo. Además se están usando nuevos materiales para la puerta del transistor y para el aislante de la puerta que pueden aportar soluciones para nodos por debajo de los 22 nm. También hay que tener en cuenta que la reducción en las dimensiones no sólo afecta al diseño del dispositivo. Con el gran aumento del número de transistores presentes en un circuito integrado, aparecen nuevos aspectos a tener en cuenta como la concentración de la potencia disipada en regiones pequeñas del chip o la variabilidad en parámetros importantes (tensión umbral) o temas de fiabilidad. Todos estos factores llevan a un aumento de la complejidad de las arquitecturas de los circuitos. Por esta razón los simuladores de circuitos son esenciales para acelerar el proceso de diseño reduciendo costes. Sin embargo es necesario desarrollar modelos lo suficientement buenos que tengan en cuenta todos los problemas que aparecen a medida que se escalan las dimensiones de los dispositivos. Por esta razón, con la introducción de dispositivos multi-puerta, las actividades de modelado compacto han tomado un papel relevante. A pesar de que hay muchos grupos de investigación dedicados a estas tareas, queda mucho trabajo por realizar debido a la gran variedad de arquitectura de dispositivos y de materiales que se están empleando actualmente para la fabricación de dispositivos.

El hecho de tratar con dispositivos multi-puerta, implica desarrollar nuevas técnicas de modelado. Es fundamental tener en cuenta tanto efectos mecánico-cuánticos como efectos bidimensionales debidos a la geometría, así como las particularidades de los mecanismos de transporte, que están fuertemente influenciados por el alto nivel de confinamiento cuántico. Para reproducir correctamente el comportamiento del dispositivo todos estos efectos tienen que integrarse de manera adecuada en modelos compactos que puedan ser implementados en simuladores de circuitos. Es interesante señalar en este punto que cuando se decide escoger una nueva tecnología, la decisión está influenciada por la disponibilidad de modelos que funcionen correctamente.

En este trabajo de investigación se han analizado algunos de los efectos más importantes que aparecen en dispositivos multi-puerta. Entre estos, el trabajo se ha centrado en transistores de doble puerta (DGMOSFETs), transistores surrounding gate (SGTs) y transistores Schottky barrier (SB MOSFETs). Los efectos cuánticos se han analizado en profundidad y se han incorporado en modelos de carga en inversión y de movilidad para DGMOSFETs y SGTs de diferentes geometrías. La característica más importante de los modelos desarrollados en esta tesis radica en la simplicidad de las ecuaciones matemáticas empleadas. El objetivo principal para el desarrollo de estos modelos ha sido su fácil implementación en simuladores de circuitos.

La mayor parte de los resultados presentados han sido publicados en diferentes revistas internacionales del JCR.

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List of Abbreviations/symbols

AC	Alternating Current
BOX	Buried Oxide
BISM	Berkeley Short-channel IGFET Model
DIBL	Drain Induced Barrier Lowering
CMOS	Complementary Metal Oxide Semiconductor
CS	Coulomb Scattering
DEG	Dimensional Electron Gas
DELTA MOSFET	Depleted Lean-channel Transistor
DGMOSFET	Double Gate MOSFET
DT-MOS	Dynamic-Threshold MOS
ECE	Electrical Confinement Effects
EOT	Equivalent Oxide Thickness
FD	Fully Depleted
GCA	Gradual Channel Approximation
GCE	Geometrical Confinement Effects
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
MuGFET	Multi-gate Field Effects Transistors
MIGS	Metal Induced Gap States
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MR	Matthiessen's Rule
NMOS	n-type MOSFET
PD	Partially Depleted
PMOS	p-type MOSFET
PS	Phonon scattering
QME	Quantum Mechanical Effects
SBMOSFET	Schottky Barrier Metal Oxide Semiconductor Field Effect Transistor
SCE	Short Channel Effects
SG	Single Gate
SGT	Surrounding Gate Transistor
SIMOX	Separation by IMplanted OXygen
SOI	Silicon On Insulator
SRS	Surface Roughness Scattering
UTB	Ultra Thin Body
VI	Volume Inversion
V_T	Threshold Voltage
WKB	Wentzel–Kramers–Brillouin

1. Multi-gate devices. Moore's law

1.1. Moore's law. CMOS fabrication state-of-the-art

The reduction of MOSFET transistors dimensions has been one of the most important technological challenges over the past decades. MOSFET channel lengths have been reduced from several micrometers to tens of nanometers, and despite the time-to-time claims that assure that this tendency is going to reach an end, the trend goes on now [Colinge-2008, ITRS-2011, Nazarov-2011, Bohr-2011]. There are several reasons that motivate the development of smaller transistors. The main one is connected with integration purposes, i. e., the aim to have as many devices as possible fabricated in a given chip area. This challenge implies a reduction in the device cost due to the fact that the total semiconductor wafer production cost increases much lower than the number of devices integrated per chip. During the last 30 years, the number of transistors per chip has been doubled each year and a half or two years approximately, as was predicted by Moore's law [Moore-1965], which was first stated in 1965. This trend has been obeyed by the semiconductor industry for more than four decades. Transistors scaling allows improved density (reduction in the cost per function) and also performance (speed and memory capacity), being the latter another important reason to go on scaling. However, different problems have shown up in this scaling process, related to the semiconductor device fabrication and devices operation [Borkar-1999, Taur-1998, Colinge-1997, ITRS-2011, Colinge-2010, Bohr-2011, Navarov-2011]. Some of them are listed in the paragraphs below.

1.- Higher subthreshold conduction: In order to maintain transistor characteristics, when MOSFET geometries shrink, the gate and threshold voltage must be reduced and as consequence the transistor cannot be switched from complete off to complete on states. This is partly due to the increase of subthreshold leakage current (including diffusion conduction, gate-oxide leakage and reverse-biased junction leakage, to name a few of the most important leakage mechanisms) which is clearly linked to scaling [Nikolic-2008, ITRS-2011, Nazarov-2011]. The power supply was kept at 5V since the 2 μm technology dated from 1980, to the 0.5 μm technology prevailing in the 90s. However, continuous scaling dramatically increases the electric fields inside the device towards inacceptable values to control transistors reliability, leading to investigate new strategies to diminish the power supply. In addition to the reduction of the power supply, the threshold voltage (V_T) became lower in order to keep the adequate current levels. Nevertheless, this strategy led to an increase of transistors leakage

current and therefore an increase in the IC standby power. Despite this component to the total power was traditionally not taken into account, nowadays cannot be ignored and the leakage power (also known as standby power) represent a non-negligible component of the overall power consumption.

1.1.- Increased gate-insulator leakage: When the transistor dimensions are shrunk, the gate oxide thickness has also to be reduced in order to keep the value of the channel conductivity (increase of the inversion charge by increasing oxide capacitance), and consequently, rise the performance when the transistor is on. However, for oxide thicknesses around 1.2 nm, important quantum mechanical effects (QMEs) appear and phenomena such as electron tunneling take place between the gate and channel. Power dissipation in digital circuits has, in general, four components: active, leakage, short circuit and biasing [Nikolic-2008]. The parasitic current due to gate insulator tunneling contributes therefore to the static (standby) power consumption increase by raising the leakage associated power [Nikolic-2008, Lo-1997]. The gate current component (tunneling current through gate dielectric with reduced thickness) is essential in nanometer devices, and its continuous increase has kept the gate dielectric thickness (T_{ox}) almost constant since the 90 nm node. In order to solve this problem, insulators with dielectric constants higher than silicon dioxide (known as high-κ dielectrics), such as group IVb metal silicates (e.g. hafnium and zirconium silicates and oxides) are being used to reduce gate leakage in the 45 and 32 nanometer technology nodes and beyond [Intel-2007, IBM-2007, Bohr-2011]. The use of these insulators implies the possibility of fabricating thicker insulator layers maintaining high insulator capacitances.

1.2.- Increased junction leakage: Scaling has also complicated junction design, leading to different technological changes in the last years such us shallower junctions, "halo" doping, pocket implants, etc. All attempts aimed at reducing short channel and related effects like drain-induced barrier lowering (DIBL) or threshold voltage roll-off. Heavier doping levels in the substrate were also needed and implying thinner depletion layers and more recombination centers that resulted in increased leakage currents and higher Coulomb scattering mechanisms (which means lower channel mobilities) [Takagi-1994, Gámiz-2002, Gámiz-2003a]. Higher channel doping also induces doping fluctuation, and therefore threshold voltage variation in nanoscale transistors [Bukhori-2010, Kovac-2008, Millar-2008, Craig-2008, Tanaka-2000, Asenov-1998].

2.- Heat production: The continuously-increasing density of MOSFETs included in integrated circuits is related to the problem of localized hot spots due to power dissipation that can cause circuit operation deficiencies. Circuits operate slower at high temperatures, and have reduced reliability levels that lead to shorter lifetimes. During the last ten years, microprocessors dissipated power has increased by a 2.5 factor in every generation. In high-performance applications, the dissipated power can be limited by high cost IC cooling solutions. In IC refrigerated air-cooling systems, the limit for the dissipated power is in the range of 100-150 W. However, in mobile applications, this limit is about 2W for IC with plastic packaging [Nikolic-2008]. Heat sinks and other cooling methods are now required for many integrated circuits including microprocessors, where heating problems are among the most serious issues dealt by designers. In addition, device compact modeling and circuit design at temperatures higher than 300 K is absolutely necessary to estimate the impact of heat production on integrated circuit prototypes. This is a difficult task due to the complexity of current state-of-the-art devices and circuits.

3.- Drain and source series resistance: The intrinsic MOSFET is in series with two parasitic resistances associated with the drain and source contacts (among other extrinsic elements). When the transistor is subjected to severe scaling processes, these series resistances are no longer negligible (the extrinsic capacitances are also important) and their effect has to be taken into account [Nazarov-2011].

4.- Lower transconductance (velocity saturation): When MOSFET geometry is reduced, electric fields in the channel increase, and the dopant impurity levels have to be increased to control short channel effects (SCE), which leads to a reduction in the carrier mobility (due to the enhanced Coulomb scattering), and hence in transconductance [Gámiz-2002, Gámiz-2003a, Gámiz-2003b]. If channel lengths are reduced without a proportional reduction in drain voltage, raising consequently the electric field in the channel, the result is the saturation of the carrier velocity in the channel and the limitation of the current and the transconductance values.

5.- Process variations: With MOSFETS becoming smaller, chip manufacturing is getting more complicated. During chip manufacturing, random process variations affect all transistor

dimensions: length, width, junction depths, oxide thickness, etc. These variations from their nominal values become the characteristics of the fabricated transistors less certain, more statistical, greatly affecting the chip performance [Bernstein-2006, Nazarov-2011, Millar-2008, Craig-2008, Colinge-2008].

Due to all these drawbacks, the technological problems that have to be solved to keep on scaling increase in each generation node. In this context, the International Technology Roadmap for Semiconductors (ITRS) was created. The pace of the MOSFET development is described by the ITRS roadmap [ITRS-2011]. It is foreseen that by the end of the next decade it will be necessary to increase the capabilities of the CMOS process, as shown in figure 1, where the predictions made by the ITRS are depicted. The capability of the CMOS process can be improved by introducing new devices that will overcome the difficulties found in conventional bulk technologies. However, it is believed that most of these new devices will not have all the properties of current CMOS devices, and therefore, it is anticipated that heterogeneous integration either at the chip level or at the package level will shape these new capabilities around a CMOS core [Bohr-2011].

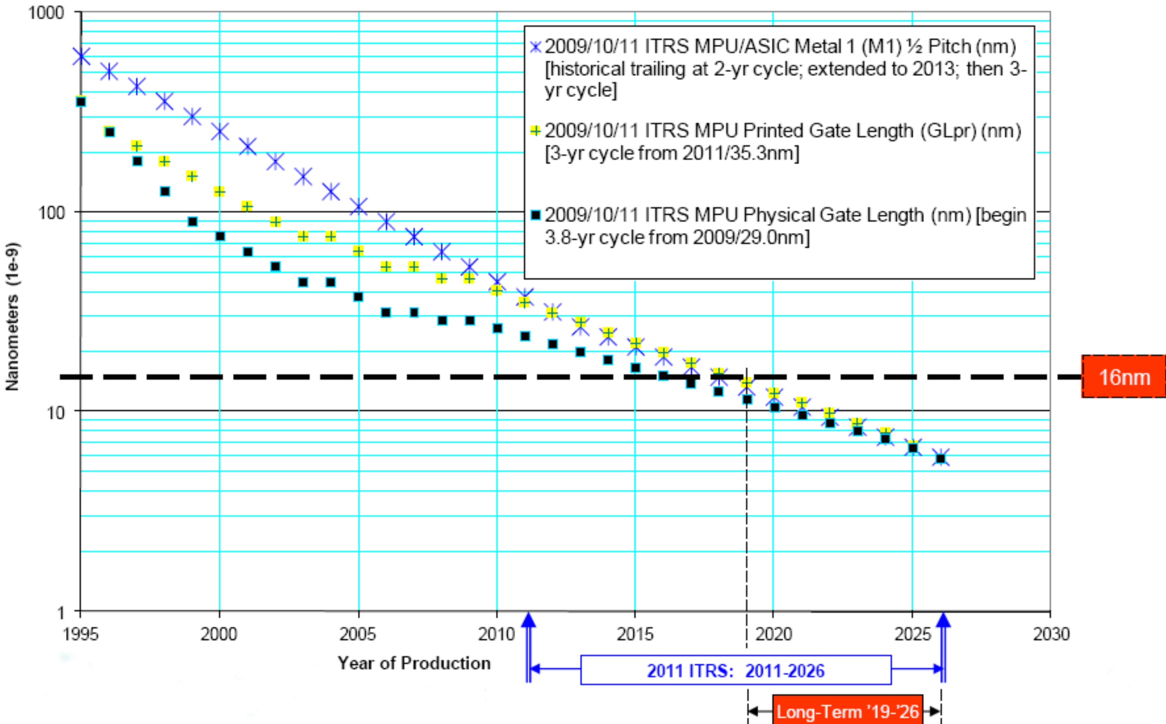


Figure 1. MPU/high-performance ASIC Half Pitch and Gate Length Trends [ITRS-2011].

Several challenges related to SCE have been identified for the implementation of the forthcoming $L_g \leq 22$ nm technology. The limitations imposed by SCEs in the technology

scaling process have made the designers to use high doping substrates, but because of this low-field mobility is reduced due to an increase in the Coulomb scattering. An alternative to the use of high doping is becoming very seriously considered with the evolution of SOI technology and the introduction of multiple-gate transistors (Double-Gate Transistors (DGMOSFETs), FinFETs, Trigate MOSFETs, PIGATEs, Gate-All-Around MOSFETs…). Device fabrication with two or more gates allows a greater control of the channel charge, and consequently, a reduction of the SCEs (higher subthreshold slopes) and also a reduction of parasitic capacitances. In addition, SOI technology allows the possibility of using undoped channels, which improves low field mobility, reduces parasitic currents between channel and drain/source contacts and lightens variability problems due to random fluctuations in the dopant distribution [Craig-2008, Kovac-2008]. In accordance with this, the use of drain and source contacts with different geometries (including metallic source/drain contact) also contributes to lighten SCE.

Two important manifestation of SCE are the DIBL (Drain-Induced-Barrier-Lowering) and threshold voltage roll-off. Based on SCE analysis, a parameter can be defined which can be used to calculate the minimum gate length that can be used for different technologies. This parameter, known as natural length, is derived from a solution of Poisson's equation. It basically represents the length of the region in the channel that can be controlled by the drain. As a rule of thumb, a device is free of SCE if the effective gate length of a MOSFET is larger than 5 to 10 times the natural length [Colinge-2004].

In line with the restriction imposed by scaling in bulk devices, where high doping levels are mandatory to control SCE, new techniques to improve the low field mobility, seriously damaged by Coulomb scattering, are necessary. One of them is based on the use of strained substrates (both with biaxial strain and uniaxial strain) to modify the band structure [Shimizu-2007, Tagaki-2008, Reggiani-2007]. Another technique proposes the use of crystallographic orientations different to the conventional one to improve low field mobility both in NMOS and PMOS transistors. In particular, the (110) crystallographic orientation enhances the mobility in PMOS by a factor of 2-4 compared to the conventional orientation (100). In that respect, the use of hybrid orientations to fabricate CMOS gates for IC future generation might be considered. Finally, a last trend is focused on the use of substrates made of Ge and III-V materials (GaAs, InSb, InGaAs, etc.), which present higher mobilities as silicon. The improvement of the technique needed to fabricate these devices opens a wide range of possibilities in relation to the scaling trends that should be explore for future IC generations [Cantley-2007, Passlack-2008, ITRS-2011].

As it has been addressed before, high-κ insulators allow the improvement of the on-current without degrading the off-leakage current due to gate insulator tunneling [Chau-2004, Manoj-2007, Darbandy-2011]. By using high-κ oxides (electrically equivalent in terms of insulator capacitance to SiO_2) leakage may be reduced by over 5 orders of magnitude. The equivalent oxide thickness (EOT) of a high-κ gate dielectric can be defined as the SiO_2 thickness necessary to achieve the same gate capacitance as with the high-κ material. When planar devices such as bulk or single-gate SOI MOSFETs are considered, the EOT can be calculated using [Huff-2005]:

$$EOT = T_{high-k} \frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}} \tag{1}$$

where ε and T are the permittivity and thickness of each material respectively. Due to the high permittivity material, the gate coupling capacitance is increased (higher inversion charges can be achieved).

When poly gates are used, the depletion layer formed between the poly and the gate dielectric generates an additional capacitance in series which degrades the device behavior. The solution to this issue is the use of metal gates, which prevent depletion layer formation (high-κ insulator and metal gates were introduced in the technology of the 45nm node at INTEL [Bohr-2011]).

For the sub-22 nm nodes, the difficulties are specially focused on the following trends: implementation of advanced non-classical CMOS structures to control short channel effects; drain engineering to reduce the series resistance; study of the quasi-ballistic transport characteristics; non-classical CMOS channel materials for enhancing transport characteristics; etc., as can be seen in figure 2. New material investigation (e.g., high-permittivity gate dielectrics, embedded structures to induce channel strain, and metal-gate electrodes) make predicting trends uncertain for transistor mismatch and for 1/f noise.

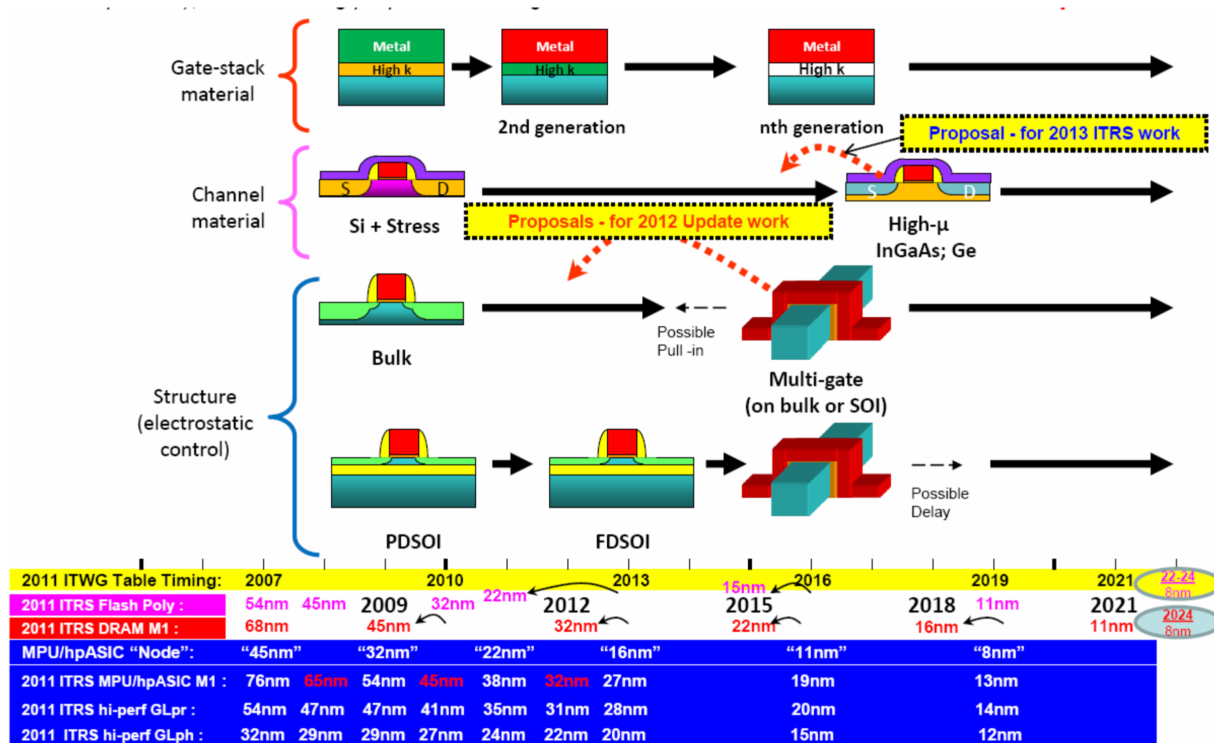


Figure 2. Graphical Trends ("Equivalent Scaling" roadmap for logic (MPU and high performance ASIC) [ITRS-2011].

In addition, an important factor to keep in mind is that the conventional scaling trend for the devices, i.e., scaling by simply reducing device size, will no longer be valid for the future generation devices where quantum mechanical effects play an extraordinarily important role (this means charge confinement, as well as phonon confinement [Donetti-2006a], influencing the low field mobility and the way heat spreads out in the devices [Pop-2004], [Goodson-1994], different tunneling processes, etc.). Therefore, as stated by the ITRS there are many issues that will have to be addressed to extend Moore's law.

From the above explanation the first conclusion that can be drawn is the following: although the complexity of the fabrication processes not always increase, the geometrical structures that are coming (and will come out) from the fabrication lines are much more intricate than their conventional bulk counterpart. Therefore, the modeling of the physical mechanisms involved in charge distribution and transport become more challenging as well. Both in high-performance applications, where the increase of the operation temperature is critical, and in mobile (low power) applications, where the use of batteries made power consumption a critical issue, the availability of accurate compact models is essential for a reliable circuit design. These models, which have to be incorporated in circuit simulators, must correctly

reproduce the electrical characteristics and also incorporate thermal effects. Moreover, the consideration of some of the technologies reported before, such as the SOI one, as mainframe is being delayed by the microelectronics community due to the lack of reliable compact models at the disposal of circuits' developers. This thesis is devoted to the development of models for advanced devices (seriously considered as alternative to conventional bulk transistors for the future [Nazarov-2011, Colinge-2004, Colinge-2008, Cristoloveanu-2004, ITRS-2011]). The urgent need for good compact models to deal with the new physical effects that show up as the scaling process goes on can be seen in the current increasing number of modeling papers published monthly in the most important refereed journals devoted to electron devices. In this context, this work deals with few of the important issues that represent the hot topic for the compact modeling community, such us the analysis and modeling of quantum effects, low-field mobility, short channel effects, drain current, etc., in multi-gate transistors, as well as the modeling of devices with source and drain based on Schottky barrier contacts.

1.2. Silicon-on-Insulator technology

We have described in depth the challenges related to transistor scaling in the previous section. In this respect, different technologies are under scrutiny to overcome the issues raised by scaling, being silicon-on-insulator (SOI) technology an important candidate [Colinge-2008, Nazarov-2010, Flandre-2001, Bohr-2011]. SOI technology advantages over conventional bulk-silicon have been demonstrated in terms of performance and reliability [Allibert-2001, Mohd-2011, Brown-2010]. Among them, the following can be counted: higher speed, lower power dissipation, high radiation tolerance, lower parasitic capacitances, lower SCE, high subthreshold swing, less variability...

SOI circuits consist of single devices fabricated in silicon islands dielectrically isolated from each other and from the underlying substrate [Cristoloveanu-2001], as can be seen in figure 3. The Buried Oxide (BOX) located under the silicon layer is in charge of isolating active devices from the parasitical effects linked to the substrate. The source and drain regions extend down to the BOX, therefore leakage currents and junction capacitances are minimized. Regarding reliability, SOI devices are also more robust to transient radiation effects than their bulk counterparts.

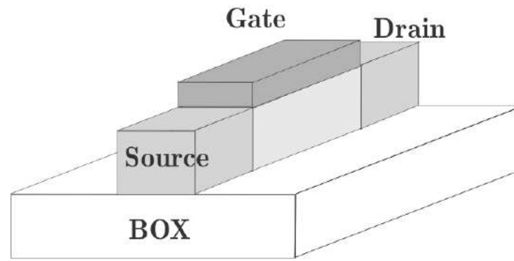


Figure 3. SOI transistor [Sampedro-2006].

Two types of categories can be distinguished in SOI MOSFETs: partially depleted (PD) and fully depleted (FD), depending on the extent of the depletion layer. On the one hand, in PD MOSFETs, the silicon film thickness is larger than the depletion regions formed at the back and front oxide-semiconductor interfaces. This implies that there is no interaction between the two layers (they are uncoupled) and there is a neutral part of silicon, the body. These types of SOI transistors behave in a way very similar to bulk transistor, but if the body is left electrically floating parasitic effects can appear (see figure 4). One of these effects is the kink effect or floating body effect [Cristoloveanu-2001], which is due to majority carriers generated by impact ionization, which are collected in the body and increase the body potential (lower threshold voltage). In weak inversion and for high drain bias, a positive feedback is responsible for negative resistance regions, hysteresis in $\log(I_d(V_g))$ curves, and eventually latch. The floating effect may also cause drain current overshoot or undershoot.

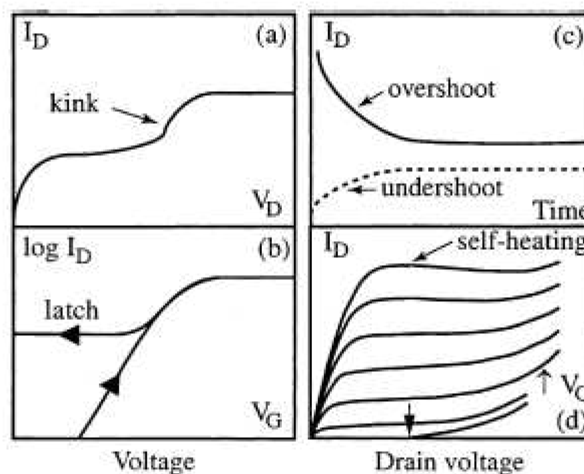


Figure 4. Parasitic effects in partially depleted SOI MOSFETs: (a) Kink curve in $I_d(V_d)$ curves, (b) latch in $I_d(V_g)$ curves, (c) drain current overshoot and undershoot, (d) premature breakdown and self-heating [Cristoloveanu-2001].

On the other hand, in FD MOSFETs, the whole substrate layer is depleted, and therefore the extent of the depletion layer does not change with the gate voltage. In these devices a strong

coupling appears between the two oxide-semiconductor interfaces, which usually lead to a drain current enhancement. With the evolution of SOI technologies FD SOI MOSFETs with nanometric channels, high-κ gate insulator, low doping and mid-gap metal gates are being studied. New architectures for this technology such as dynamic-threshold (DT-MOS), or ground-plane SOI MOSFETs have also been under investigation [Allibert-2001, Ming-2005, Soleimani-2009, Saremi-2010]. Advanced SOI MOSFETs (single or multiple gate MOSFETs) are very promising structures for the downscaling of MOSFETs below the 22 nm technological node. Thin film fully depleted SOI MOSFETs offer important advantages over partially depleted SOI MOSFETs: lower body factor, better subthreshold slope, reduced SCE, higher saturation current and smaller mobility degradation.

In summary, SOI CMOS technology presents important advantages over bulk CMOS: a simpler technology with no wells or trenches, better dielectric isolation in both vertical and horizontal directions, no latch-up, better radiation tolerance, reduced sub-threshold swing which allows lower voltage operation, low parasitic capacitances: drain/source junctions and interconnects.

In the 90s the predominant SOI technology was SIMOX [Cristoloveanu-2001], but this technology, despite is still in use, has several disadvantages like the use of non standard equipment and the need of $T > 1300°C$ annealing which could be a limitation for 300 mm wafer size [Auberton-1996]. Recently, the Smart Cut® Technology, which makes use of both implantation of light ions and wafer bonding to define and transfer ultra-thin single-crystal layers from one substrate to another, has been introduced. This technology incorporates some advantages like a wide range of possible thicknesses of the Si layer on top of the BOX, an extremely high quality in terms of uniformity, bonding interfaces and control of thickness variability, and it is based on standard semiconductor-industry tools, therefore the wafers can be scaled to multiple diameters [SOITEC]. Thinning the buried oxide layer (Ultrathin BOX, UTBOX) has been found very efficient to reduce SCE and DIBL, and therefore, limits the silicon film thickness reduction, which is good for the access resistance of FD SOI devices [Faynot-2011]. This reduction can also be achieved successfully from the technology point of view. Most of today's industry-leading SOI wafers oriented to be used for chip manufacturing are made using Smart Cut® technology.

1.3. Multi-gate devices. Scaling

Despite the advantages of SOI over bulk technology, SCE are also present in ultrathin-film SOI technology [Eminente-2004, Colinge-2008]. Therefore, the semiconductor community needs to look for alternative technologies in order to maintain the device shrinking trend that has fueled the electronics industry in the last forty years. When the device gate length is reduced, the capacitive coupling between the drain and the channel is increased. As we highlighted in the previous section, a leakage current flows in ultrashort device even if no gate voltage is applied, and consequently deteriorates the standby power consumption.

In order to tackle this problem, novel devices using more than one gate are introduced (Multi-Gate MOSFETs) (see figures 5, 6 and 7 for SOI MuGFETs), which can control the channel from several sides (due to the use of several gates) and therefore reduce SCE.

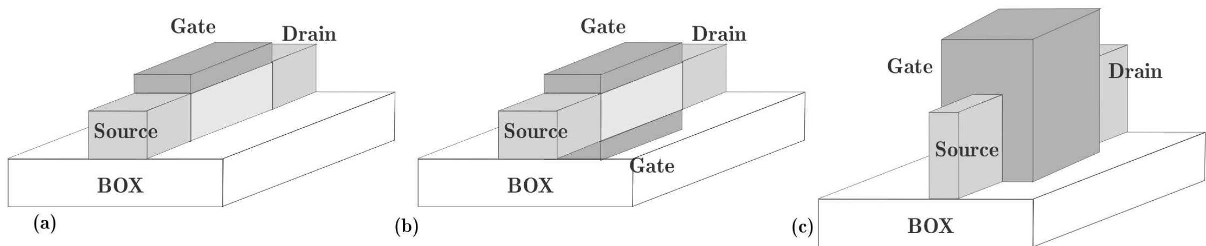


Figure 5. (a) Single gate, (b) Double gate, (c) FinFET, [Sampedro-2006].

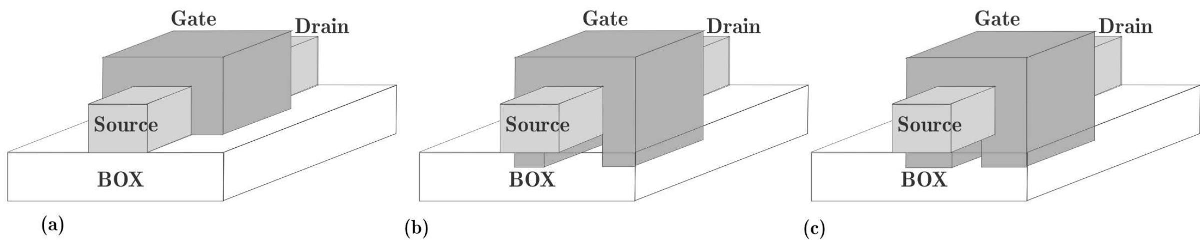


Figure 6. (a) Trigate, (b) pi-gate, (c) Ω-gate, [Sampedro-2006].

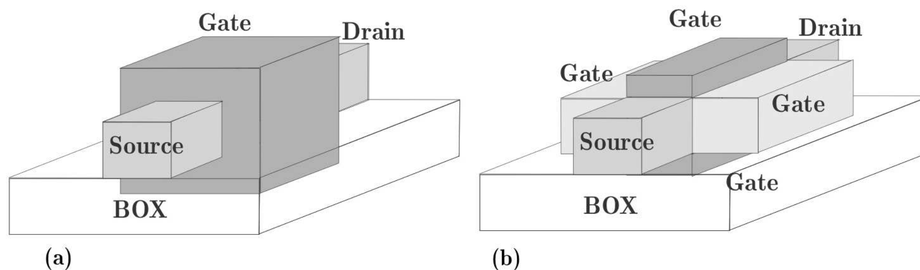


Figure 7. (a) Gate all around, (b) G4 FET [Sampedro-2006].

The potential of these devices is great, that is why there is a strong commitment in the microelectronic community in terms of research and development in connection with them. The control over SCE permit the reduction of channel doping, this fact obviously implies lower Coulomb scattering and higher low-field mobility. Undoped multi-gate devices can be both fully inverted or accumulated (even, the inversion layer can be located in the middle of the silicon layer, which is known as volume inversion [Balestra-1987], as will be explained below in this section). It is also interesting to highlight that in multi-gate devices the total current compared to the SG devices increases due to the higher number of gates [Colinge-2004, Nazarov-2011, Colinge-2008, Enz-2006, Arora-2007, Amara-2009]

Several devices of the so-called multi-gate MOSFETs (in its SOI version, since several of them can be also fabricated on bulk wafers) are sketched in figures 5, 6 and 7. One of the first that was successfully fabricated was the double-gate MOSFET (DGMOSFET) (also denominated the DELTA MOSFET Depleted Lean-channel TrAnsistor), where the silicon film was vertical [Colinge-2004]. After this first transistor, several implementations of the DGMOSFET [Colinge-1990] appeared like the FinFET, the MFXMOS, the triangular-wire SOI MOSFET and the Δ-channel SOI MOSFET.

One of the most interesting effects that show up in DGMOSFETs is called volume inversion (VI). This effect, which also takes place in other multi-gate devices, was first characterized by Balestra and co-workers [Balestra-1987]. It is produced when the silicon film thickness in DGMOSFETs is reduced. If the whole silicon film is depleted an important coupling appears between the two potential wells formed at the semiconductor-oxide interfaces; in this case, the inversion layer is not formed near the two interfaces but in the middle of the silicon layer. If that happens, the device is said to operate in VI. This operation regime presents several advantages such as the enhancement of the number of minority carriers and the increase in low-field carrier mobility due to the reduction of Coulomb (due mainly to insulator interface charges) and surface-roughness scattering mechanisms, which leads, consequently, to an increase in the drain current and transconductance. The low frequency noise is also reduced as well as hot-carrier effects.

Another step in the MuGFET development was introduced by means of the triple-gate MOSFET, which consist on a thin-film narrow silicon island with a gate on three of its sides. Some examples of this device are the PI- and the DELTA MOSFET [Colinge-2004], [Sampedro-2006] (see figures 5 and 6). INTEL 22 nm technology which has been got ready in 2012 in several of its fabrication plants is based on Trigate MOSFETs [Bohr-2011]. Another

promising MuGFET is the surrounding gate transistor (SGT), which consists on a semiconductor core with cylindrical or square shape completely surrounded by an insulator and a gate. This latter device allows potentially high packing densities and presents the highest invulnerability to SCEs. Unfortunately, SGT devices present drawbacks that have to be solved in relation to their fabrication process. The fabrication of these devices is not easily transferable to the already existing and widely used CMOS or even SOI CMOS manufacturing. For this reason, further investigation has to be carried out. The current focus is on devices such as FinFETs, Pi-gate MOSFET or Ω-MOSFET [Park-2001, Colinge-2008, Colinge-2006, Nazarov-2011]. These devices are based on triple-gate MOSFET geometry, their main differences are linked to the way the gate electrode is fabricated and extends inside the buried oxide (see figure 6). In this respect, the gate extension in the buried oxide behaves emulating a back gate because it shields the back of the channel region from the electric field lines from the drain; as a result, the DIBL and the subthreshold characteristics are comparable to those of a SGTs. That is why these devices can be viewed as an alternative to the SGT since they can be manufactured with the conventional CMOS technology. For these devices the natural length can be reduced by decreasing the gate oxide thickness, the silicon thickness, and by using a high-κ gate dielectric instead of SiO_2. An analysis of the scaling perspectives for the next few years based on this parameter shows that SGTs and TRIGATE MOSFETs seem to be the ideal candidates for nodes below 22 nm.

The thickness and/or width of the silicon layer in MuGFETs are reaching values in the nanometer range. Under these conditions, electrons in the channel form either a two-dimensional electron gas (2DEG) if we consider quantum confinement in one dimension (such us in DGMOSFETs) or a one dimensional electron gas (1DEG) in the case of two dimensional quantum confinement (found in triple- or quadruple-gate MOSFETs, in the latter case the devices are also denominated quantum nanowires). This confinement is at the origin of "volume inversion" effects, and yields an increase of threshold voltage when the width/thickness of the device is reduced [Omura-1993] [Poiroux-2005, Colinge-2008, Amara-2009]. We will develop this analysis in the third and fifth chapters of this work.

Finally, to summarize the role of MuGFETs in the scaling scenario we include the figure below. These MOSFETs are the preferred structures for the 22-8 nm window. In this shorter case, other authors add that MuGFET devices will be transformed and adapted making use of Schottky-barrier drain and source contacts (SB MOSFETs, to be analyzed and modeled in chapter 4) and different flavors of tunnel structures, deriving in tunnelFETs intensively under study currently (subthreshold slopes steeper than 60mV/decade are supposedly promised in

tunnelFETs that will enable lower threshold voltages and lower active powers). Nanowires, nanoribbons and graphene transistors might also be key players in the beyond CMOS scenario, although the basic geometry of MuGFET devices will probably remain.

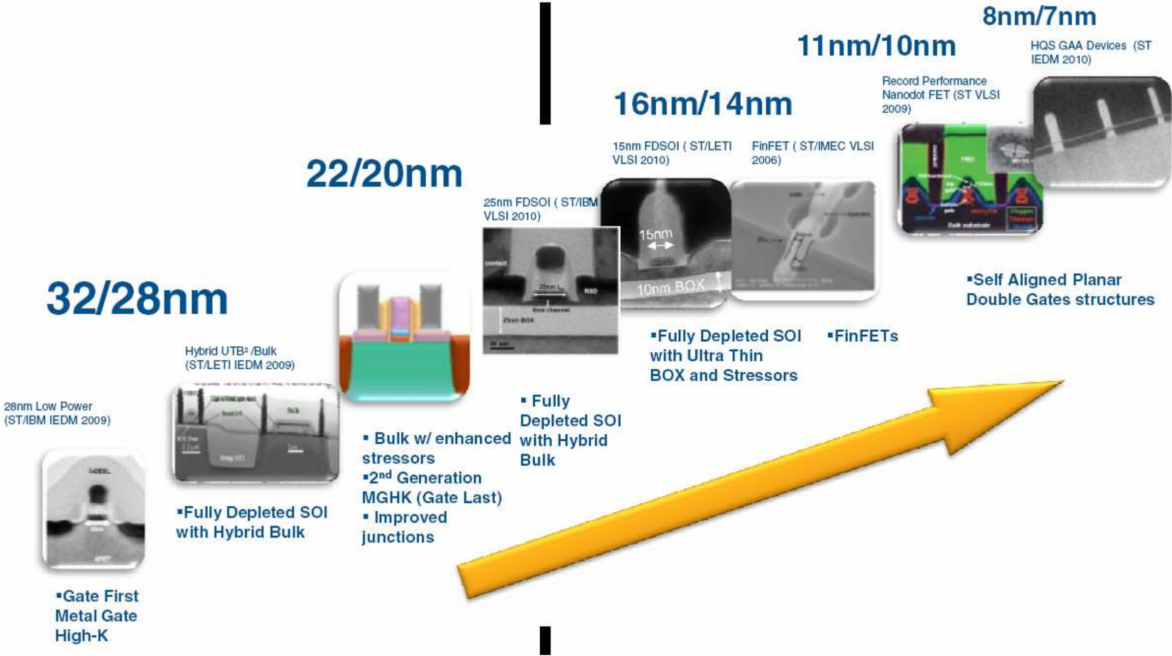


Figure 8. MOSFET architecture evolution [Skotnicki-2011].

1.4. Compact modeling. Current models in use and future needs

A compact model is a mathematical description of an electrical component as used by circuit designers and technologists to mimic the electrical device behavior in a technology. Accurate and physics-based compact models are useful for the design and development of MOSFETs for digital and analog circuits. The model, representing the expected physical mechanisms through mathematical equations, is expected to be able to reproduce the device characteristics for different device dimensions, range of temperature, process variations, etc. Additionally, the description must keep valid under a variety of operating conditions. The model parameters are the interface between the design community, the model users, and the device manufacturers [Bhattacharyya-2009]. Compact models are needed to numerically compute the component or device characteristics (currents, charges and noise as a function of the terminal

voltages) accurate and fast enough to simulate complete electrical circuits [Woltjer-2007, Gildenblat-2010, Galup-2007].

The accuracy of compact models is an essential issue for IC designers to simulate complex circuits before they become fabricated. In fact, this is a key issue to most Fab-less companies devoted to IC design, since among the features they analyze, when they choose between the different technologies in the market.

The evolution of MOSFET compact models is shown in figure 9, where the year of introduction of the different models is presented. The first MOSFET compact models were develop in the early 70's, but the real evolution and proliferation took place at the end of the 80's, and has been maintained up to now. One of the most important family models that can be found in the figure 9 is the BSIM model family (University of Berkeley), which has been widely used for the simulation of planar bulk MOSFET. Berkeley's compact models belong to the threshold voltage based models [Bhattacharyya-2009] and they describe the MOSFET behavior in weak and strong inversion demarcated by threshold voltage. BSIM1 [BSIM] represents a second generation approach which involves device dimensions in the model equations and parameters, but introduced many fitting parameters. BSIM3 [BSIM] represents a third generation approach where both computational robustness and physical basis are the main features. Despite the continuously increasing number of model parameters is turning out to be a major concern for this approach, they are still considered as a standard.

Another important family is the EKV charge-based models [Enz-2006]. These models fall into the charge based model category where the drain current is formulated in terms of the inversion charge density at the source and drain ends of the channel [Bhattacharyya-2009]. This approach has been very effective where low-power analog design is involved. It is physics-based, with a minimum requirement of empirical fitting, and has a relatively easy parameter extraction procedure [EKV]. EKV models have now evolved into a full featured scalable compact model that includes all the major effects needed to describe the nanometric technologies [Enz-2008, Bremer-2010] (a merge of these two models (EKV+BSIM) has been announced in the last MOS-AK meeting held in Helsinki, September 2011. The BSIM6, featuring the most challenging features of each model will be launch soon, as it was announced by Chemming Hu and Christian Enz).

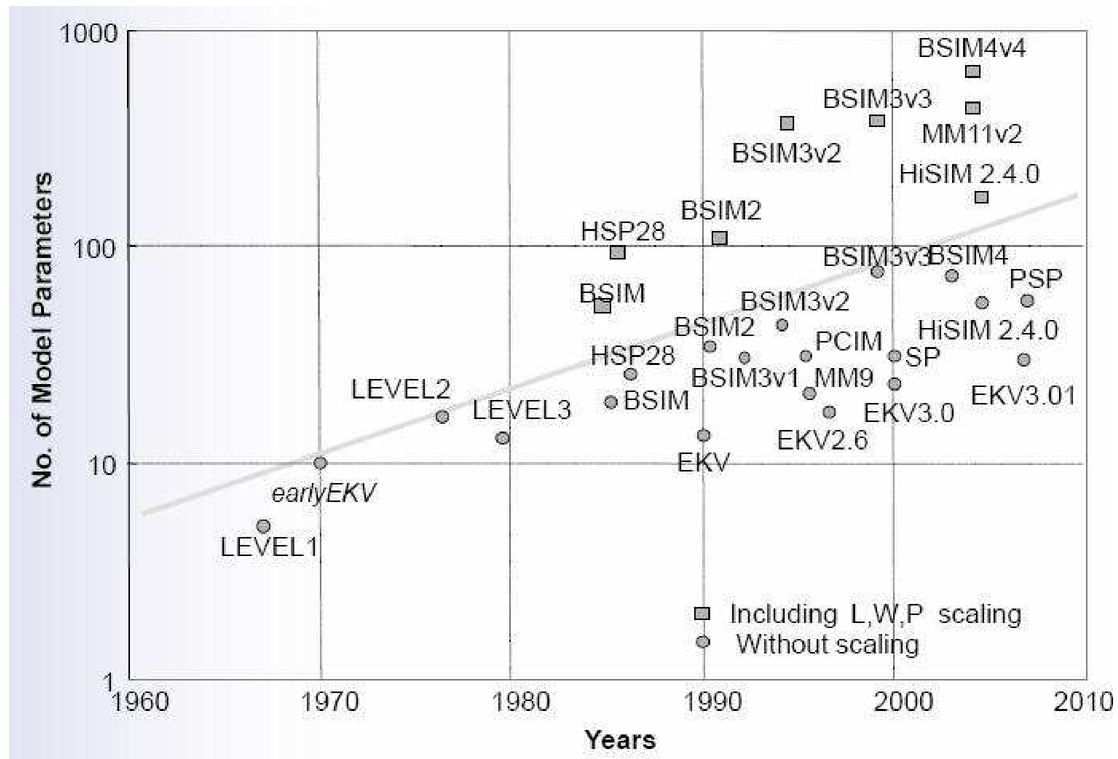


Figure 9. MOSFET model evolution. [W. Grabinski, Training Courses on Compact Modeling, Tarragona 2010].

One of the approaches to develop MOSFET compact models is the so-called gradual channel approximation [Woltjer-2007, Tsividis-1999]. This approach consists on separating the 2D MOSFET Poisson equation into two 1D equations [Sah-1991]. The 1D solution perpendicular to the channel is known as the "input voltage equation" and it relates the gate voltage to the potential at the insulator interface by an electrostatic solution of Poisson's equation. The 1D solution parallel to the channel is known as "output current equation" and relates the source-drain current to the input voltage equation and the source and drain voltages. This approach assumes a drift-diffusion transport mechanism and is only valid when the potential along the channel varies gradually. Another approach for MOSFET compact models is the charge sheet approximation, which assumes that the electric potential does not change along the channel thickness (the inversion layer thickness). For MOSFET devices, there are three kinds of models: threshold-voltage-based, inversion-charge-based and surface-potential based models [Woltjer-2007]. For the first kind, the surface potential is approximated by a simple function of the gate voltage which is constant above the threshold voltage and linear for the gate voltage below threshold. These models are becoming in disuse because of the discontinuities produced when the different regions of operation are swept by the transistor in a simulation

process. The second type of models is based on equations that relate the current and the different charges found in the device. Finally the third kind of models solves the surface potential at both ends of the channel, and the currents and its derivatives are calculated as a function of this surface potential. These two latter models gained importance in the nineties and were found to be especially adequate for MuGFET modeling.
For MuGFETs, the principles of modeling will change as compared to the traditional SG MOSFETs, firstly because they will have to introduce the volume inversion effect, secondly, contrary to bulk MOSFETs, depletion charges in multiple-gate devices are negligible because the silicon film is undoped (or lightly doped) in most cases. Thus, only the mobile charge term needs to be included in Poisson's equation. Therefore, the exact analytic solutions for the 1D Poisson's and current continuity equations based on the gradual channel approximation (GCA), which assumes that the quasi-Fermi potential stays constant along the direction perpendicular to the channel, can be derived without the need of the charge-sheet approximation. Most models presented so far are for undoped devices with a long enough channels to assume that the transport is due to the drift-diffusion transport mechanism [Iñiguez-2006, Taur-2004, Ortiz-Conde-2005, Jiménez-2004], although correction mechanisms to account for velocity saturation, SCEs, DIBL… are also included in a second stage. Ballistic or quasi-ballistic effects are gaining importance among the effects to consider in the current compact modeling activity due to the very short channel lengths of current and surely future nodes. In this context, the transport characteristics of the carriers injected from the source and drain will depend on the potential barrier at each contact and the back-scattering matrix will have to be determined in each case [Toriumi-1988, Natori-1994, Ren-2000, Chang-2000, Ge-2001, Lundstrom-2002, Ren-2001, Rhew-2002].

For future devices, the availability of accurate compact models will be critical prior to introduce them as mainstream technology. Circuit designers require, in addition to DC models, a complete small-signal model with analytical or semi-analytical expressions of current, total charges, transconductance and conductance, transcapacitaces, and noise. In MuGFETs there is still a long way to go in this subject.
In the context we have described along this introductory chapter, we present this coherent set of results that constitute a step forward in different areas of MuGFET modeling.

2. Simulators description

2.1. Introduction

Simulators are becoming essential tools for most sciences and engineering studies nowadays. This also happens in the electronics industry, where its use is widely extended. We can simulate to predict the behavior of semiconductor devices. The results can be analyzed to improve the device performance by changing both the technological structure and the bias. Simulators also help us to clarify the dependencies and limiting physical mechanisms in the device/circuit capacity (e.g. effects of noise, limits on frequency/gain, trap effects, effects of geometry…). The characterization of charge carriers transport properties (mobility, diffusion coefficients…) can be performed in a particular material at different conditions of temperature, quantization, strain, crystallographic orientation, and many others features.

Device simulators are also known to be essential tools for compact modeling purposes. Firstly, simulators allow the extraction of internal variables that can not be obtained in any other way, such us the electric field and potential within the device; some of these variables are the building blocks (state variables) needed to develop a compact model (as explained in the previous chapter). Secondly, device simulators can be of great help to complement the experimental data obtained in the laboratory to deal with parameter extraction algorithms that are essential to accurately characterize a given technology.

In this section we describe the simulators used to obtain the data we have employed to develop some of the models presented here. Different kinds of software tools have been used. On the one hand, the data for p-type and n-type DGMOSFETs and SGTs have been obtained by means of simulators developed in our research group (the Nanoelectronics Research Group at the University of Granada). Details of these tools will be given in sections 2.3 and 2.4. On the other hand, to obtain the data for SB (Schottky Barrier) MOSFETs presented in chapter 4, the commercial ATLAS TCAD simulator has been used. The simulated structure and the procedure followed using ATLAS is described in section 2.2.

2.2. Commercial device simulators: ATLAS from Silvaco

ATLAS is a general purpose device simulator that enables electronics engineers to analyze the electrical, optical, and thermal behavior of semiconductor devices in a 2D or 3D numerical scheme [ATLAS-2010]. It is commercialized as a part of a simulation suite from Silvaco ranging from fabrication process to circuit analysis tools. In this respect, the simulations performed with this suite can be employed in most of I+D stages of an integrated circuit creation, from the process engineering first steps to the device characterization for circuit design purposes.

In the following paragraphs we include a short description of the different programs included in the Silvaco suite [ATLAS-2010]:

ATHENA is a tool for modeling semiconductor fabrication processes. High temperature process modeling such as impurity diffusion and oxidation can be described as well as lithography simulation in a single framework.

DevEdit is a device structure editor. It can be used to generate a new mesh on an existing structure, modify a device or create a device from scratch. These devices can then be used by 2-D and 3-D simulators. DevEdit can be used through a Graphical User Interface (GUI) or as an independent tool.

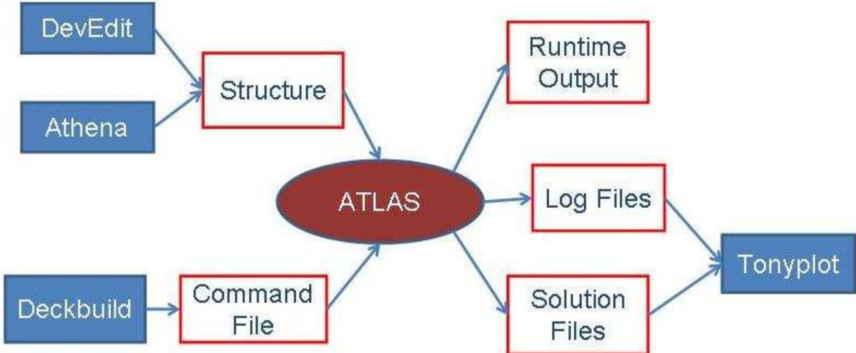
DeckBuild is an interactive, graphic runtime environment for developing process and device simulation input decks. It consists of a window for input deck creation and editing, a window for simulator output and control, and a set of popups for each simulator that provide full language and run-time support.

Tony plot is a tool designed to visualize 2D and 3D structures produced by the suite simulators.

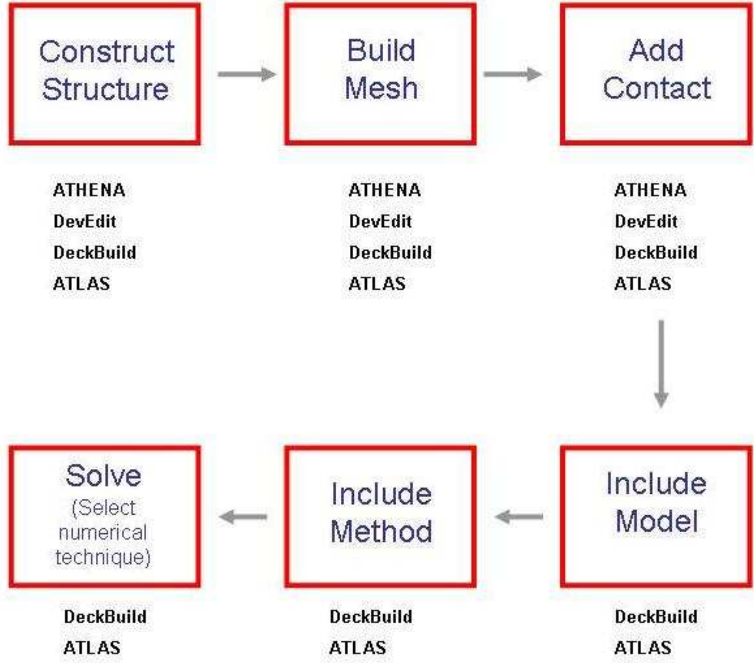
ATLAS is a device simulator that offers the possibility to use a wide variety of materials such as silicon, metals, different alloys (III-V, II-VI, IV-IV) or polymer/organic based structures, as well as parameters to change, for instance: temperature, pressure... It has a wide range of built-in physical models that account for mobility, recombination, impact ionization, traps, quantum behavior, hot-carrier injection, tunneling, thermal, stress, anisotropic, optical generation, phase change, ferro-electric, radiation and degradation effects. Different analysis studies can be performed (DC, AC, noise and transient analysis). Two types of input files can be used: structure files or command files, which can be obtained by using the different programs included in the suite (figure 10a). The output files obtained are also depicted in this

figure. We have used this simulator mainly to study the devices presented in chapter four, Schottky Barrier DGMOSFETs. The device description has been carried out by employing Deckbuild.

In figure 10 b), the steps that we have followed to generate a command file that completely describes the SB DGMOSFET devices studied (chapter 4) are depicted. Under each box we have specified the different programs that can be used to perform the task.



a)



b)

Figure 10. ATLAS device simulation flow [ATLAS-2010].

We have proceeded in the following way: firstly, the device structure was created by using predefined statements to indicate the number of regions in which the device is divided (source, drain, body, insulator...), the doping profile in each region, the electrodes and the material they are made of, etc. The basic structure used for the SB DGMOSFET studied in this work is shown in figure 11. Secondly, the mesh was defined. For the SB DGMOSFET as the drain and source regions are not defined by means of heavily-doped semiconductor regions that differ from the body area, but by means of metallic contacts, it is critical to define a fine enough mesh, especially underneath the source and drain contacts. The use of a coherent mesh avoids convergence problems when simulating the device. To make sure the source and drain contacts behave as Schottky contacts instead of as ohmic ones, suitable work functions were defined for the source and drain electrodes.

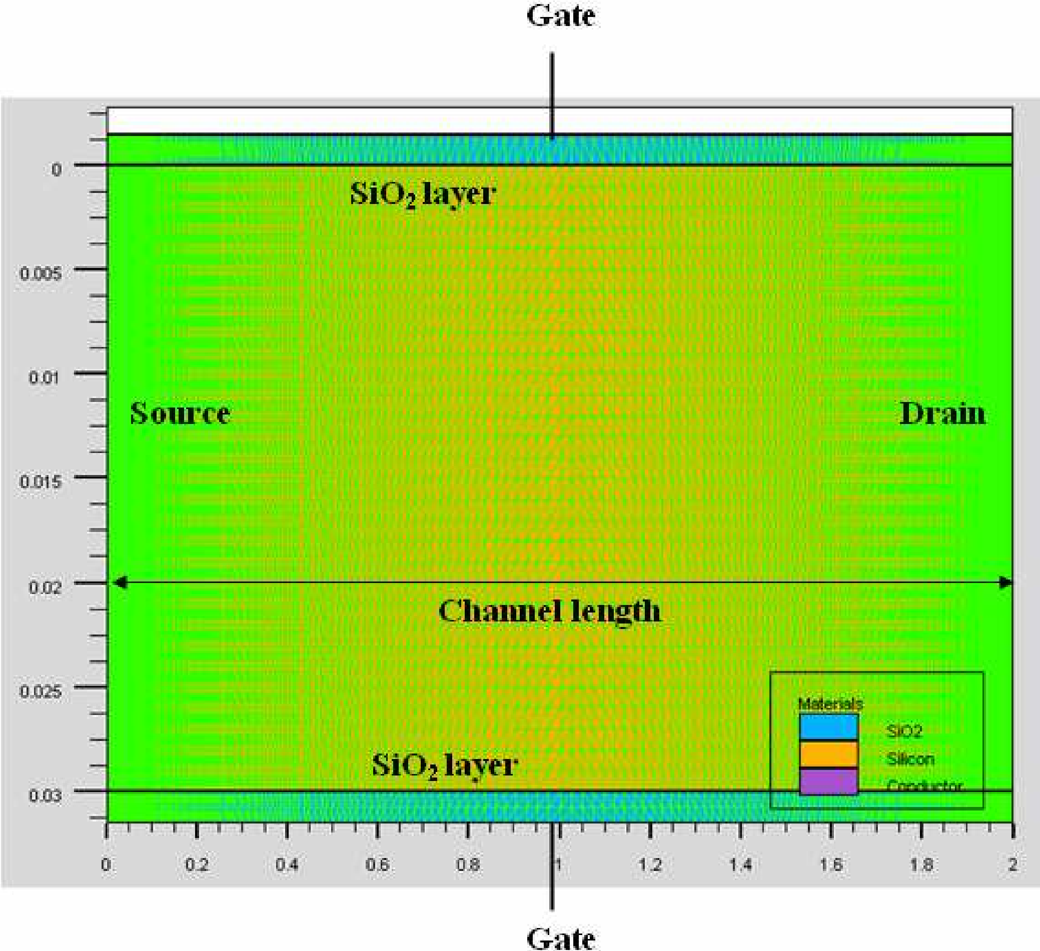


Figure 11. SB MOSFET structure simulated with ATLAS. The main device areas and the triangular mesh used in the simulation can be clearly seen.

Finally, the physical models for the different materials and the type of simulation along with the numerical method chosen for the set of partial differential equations involved in the device description (drift-diffusion, hydrodynamic, inclusion of quantum effects, etc.) are chosen. The SB DGMOSFET structure studied has been simulated considering both types of carriers: electrons and holes (as it will be shown in chapter four, the ambipolarity of these devices is very strong and it has to be taken into consideration to accurately model its transport characteristics [Balaguer-2011]). The universal Schottky tunneling and the band-to-band tunneling mechanisms were also included to account for the main charge conduction contributions found in these kind of structures.

2.3. DGMOSFET Simulator

In this section the DGMOSFET simulators are presented. As an introduction to the following sections, we have included a schematic representation of the simulated DGMOSFET structure. In figure 12 the different regions that conforms the DGMOSFET are indicated as well as the most characteristics geometrical parameters which are referred when dealing with these devices and that will be used in the following sections when describing the different DGMOSFET simulators.

As indicated in figure 12, T_{ox} is the gate oxide thickness, T_{Si} is the silicon thickness and L is the channel length.

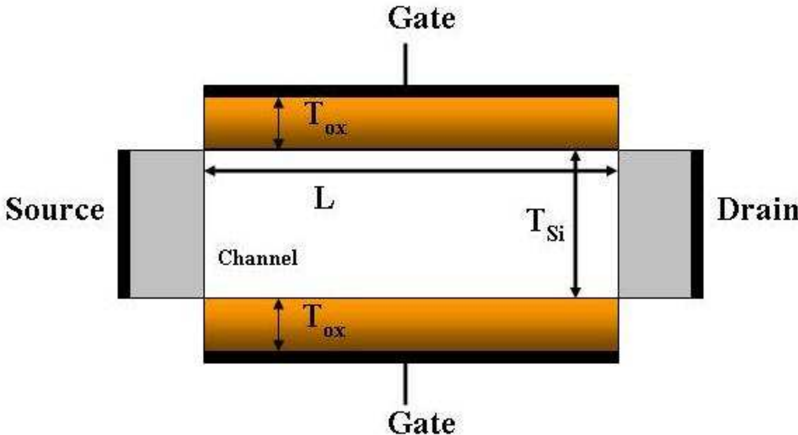


Figure 12. Cross-section of the DGMOSFET simulated structure.

2.3.1. N-type devices

2.3.1.1. One dimensional self-consistent solution of Poisson and Schrödinger equations for electrons

To simulate the DGMOSFET structures studied in chapter 3, whose geometrical features are described in the previous figure, accounting for different crystallographic orientations a simulator developed in our research group has been used. The simulator provides the electron distribution, the electric potential, the distribution of energy levels for each conduction band valley, among other magnitudes. To do so, this tool self-consistently solves the Poisson and Schrödinger equations in n-type DGMOSFET [Gámiz-2004, Rodríguez-2007]. The solver makes use of a non-uniform adaptive mesh and an iterative-Newton numerical scheme, and uses a non-parabolic band model. In figure 13, it can be seen the simulated charge distribution for an undoped n-type DGMOSFET for two different substrate orientations.

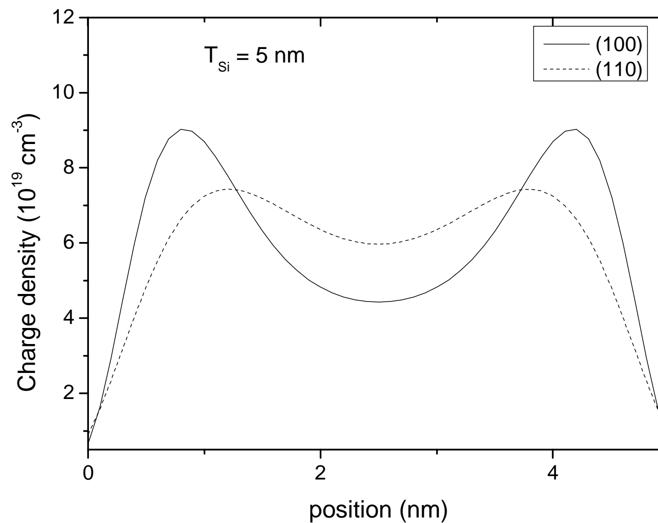


Figure 13. Charge distribution for an undoped n-type DGMOSFET grown on (100) and (110) substrates with V_G = 2.0 V, T_{ox}=1.5 nm.

Poisson and Schrödinger equations are also solved inside the dielectric layer in order to take into account the wavefunction penetration effect, i.e., the nonzero value of the electron probability density inside the insulator. The penetration of the wavefunctions inside the oxide has an important effect on the centroid calculation, as reported in [Mudanai-2001].

We have applied the procedure described in [Rahman-2005] to calculate the effective masses in our system assuming parabolic bands. Then, we empirically add a correction factor α following Kane's model and the procedure explained above. The nonparabolicity factor has

been considered to be the same regardless of the crystallographic orientation ($\alpha = 0.5$ eV^{-1}) in the present work [Fischetti-1993].

2.3.1.2. Low-field electron mobility calculation by the Monte Carlo method

The Monte Carlo simulator used to obtain the mobility curves introduced in section 3.6 takes into account the electron distribution and wave functions obtained in the silicon inversion layer by self-consistently solving the Poisson and Schrödinger equations as reported above; more details are given in [Gámiz-2002, Gámiz-1998a]. The crystallographic orientation considered for all the devices studied in section 3.7 was the conventional Si (100). In these conditions, by considering quantum effects, the degeneracy of the six equivalent minima of the silicon conduction band breaks and the electrons are distributed into two sets of subbands. Once these two equations are solved the wave-functions are used to calculate the scattering probabilities needed in the low-field mobility calculation by means of the Monte Carlo method. The electron effective masses were assumed to be those obtained for the silicon bulk: $m_t = 0.19m_0$, $m_l = 0.916m_0$, with m_0 being the free-electron mass.
For the phonon scattering, acoustic deformation potential scattering and intervalley phonon events were considered. The coupling constants for the intervalley phonons were the same as in bulk silicon inversion layers [Gámiz-1998a], whereas for acoustic phonon scattering, the coupling constant was increased with respect to bulk silicon in order to reproduce the effect of confinement and quantization of acoustic phonons due to the reduced dimensions of the silicon slab [Donetti-2006a, Donetti-2006b]. Surface-roughness scattering was also considered making use of the model introduced in [Gámiz-1999a], where different delta parameter (Δ) values representing the abrupt variations of the oxide-semiconductor surface were considered.

Coulomb scattering is produced by charged centers that disturb the potential V_0 which is obtained assuming a continuous density of charges in the self-consistent solution of Poisson and Schrödinger equations [Gámiz-1994, Gámiz-2002]. These charges may be ionized impurities, trapped charges inside the dielectrics or charges at the interfaces between the silicon layer and the insulators (the case considered in this study). Let $\rho_{ext}(\vec{r}, z)$ be the

external charge density that causes this perturbation to the potential (the resultant scattering mechanism is just the Coulomb scattering).

In order to calculate the Coulomb perturbation potential ($V(\vec{r},z)$), the following Poisson equation must be solved [Ando-1992]:

$$\nabla\left[\varepsilon(z)\nabla V(\vec{r},z)\right]=2\varepsilon_{sc}\sum_{i}S_i g_i(z)\int V(\vec{r},z_1)g_i(z_1)dz_1-\rho_{ext}(\vec{r},z), \quad (2)$$

Where $\vec{r}$ represents the spatial component parallel to the interfaces and z is the coordinate perpendicular to them. ε(z) is the position dependent permittivity overall and ε_{SC} is the permittivity of the semiconductor, g_i (z) is the square of the electron envelope function in the ith sub-band and S_i is the screening parameter [Gámiz-1994]. The first term on the right-hand side of equation (2) is the charge induced in the inversion layer by the external charges. This term contributes to reduce the influence of the external charges given by $\rho_{ext}(\vec{r},z)$ (that is, mobile carriers partially screen the charged centers responsible for the Coulomb scattering). In order to eliminate the parallel spatial coordinate $\vec{r}$, equation 2 is multiplied by $e^{-j\vec{Q}\cdot\vec{r}}$ and integrated over $\vec{r}$. The following equation for the Fourier transform of the electrostatic potential perturbation, $V(\vec{Q},z)$ is then obtained [Gámiz-1994, Gámiz-2002]:

$$\left[\frac{\partial}{\partial z}\varepsilon(z)\frac{\partial}{\partial z}-\varepsilon(z)Q^2\right]V(\vec{Q},z)-2\varepsilon_{sc}\sum_{i}S_i g_i(z)\int V(\vec{Q},z_1)g_i(z_1)dz_1=-\rho_{ext}(\vec{Q},z), \quad (3)$$

where Q is the module of $\vec{Q}$. The resolution of equation 3 provides the Coulomb perturbation potential and is carefully detailed in [Gámiz-1994, Jiménez-Molinos-2008] for several structures. Finally, it is interesting to highlight that among other features, this model accounts for the distribution of electrons in the inversion layer, the geometrical distribution of external charged centers, the screening of charged centers by mobile carriers, the charged center correlation and image charges.

2.3.2. P-type devices

2.3.2.1. One dimensional self-consistent solution of Poisson and Schrödinger equations for holes

To study the p-type DGMOSFETs presented in chapter 3.4, a fully self-consistent solver for the six-band k·p Schrödinger and Poisson equations to compute the valence-band structure with arbitrary substrate orientation has been used [Donetti-2010, Donetti-2009, Donetti-2008]. This simulation tool allows us to compute the electrostatic potential, charge distribution and subband energy dispersion relation for hole inversion layers.

The 6-bands k·p Hamiltonian is discretized along the confinement direction with the appropriate rotation on the k space if the substrate orientation is different from (001). The discretized Hamiltonian depends on the wave-vector component perpendicular to confinement direction. Its eigenvalues allow us to obtain the energy levels and dispersion relationships of the hole subbands, while the eigenvectors are the corresponding six-component wavefunctions.

The Poisson equation (using the same grid in the confinement direction) is then solved taking as input the charge distribution computed with the k·p solver. This procedure is repeated until self-consistence is reached. The calculation of carrier concentration is performed by momentum-space integration by summing over the triangles defined by the aforementioned mesh; inside each of them the energy of hole subbands is linearly interpolated [Donetti-2009].

2.4. SGT (Surrounding Gate Transistor) simulator

This section is devoted to the description of the SGT simulator used to obtain the simulation data shown in chapter 5. We have already seen in chapter 1 that SGT behaviour, when the device dimensions are reduced, differs from DGMOSFETs. In particular, in SGTs the electrons form a one dimensional electron gas (1DEG). The electrons are free to move in the x direction only, while they are confined in the y and z directions (these structures also known as quantum nanowires [Nazarov-2011]). This high degree of confinement results in the formation of energy subbands and charge distributions in the silicon core that can be significantly different from what is predicted by classical theory (also different of what is found in devices with one dimensional quantum effects). The confinement of the electrons also causes different behavior in what mobility and threshold voltage concerns. The simulator described in the following section takes into account these particularities for SGT devices.

2.4.1. Two dimensional self-consistent solution of Poisson and Schrödinger equations

The SGT structure presented in chapter 5 was simulated by means of a simulator developed within our research group [Godoy-2006]. It calculates the charge distribution in a structure with a gate that surrounds a cylindrical silicon channel where conduction takes place (see figure 14).

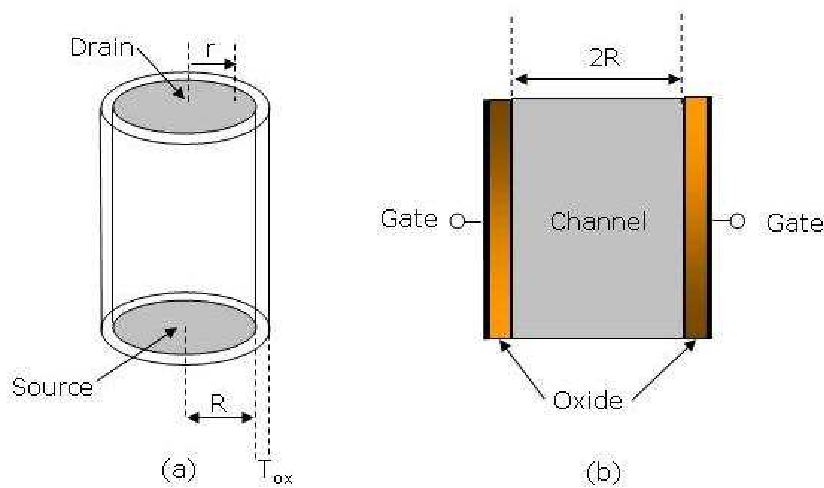


Figure 14. (a) Simulated structure of the cylindrical surrounding gate transistor, (b) Cross-section of a SGT.

In order to obtain accurate simulation data, the simulator self-consistently solves the two-dimensional Poisson and Schrödinger equations. To reach a fast convergence, the equations have been solved using the predictor-corrector scheme proposed by Trellakis et al. [Trellakis-1997] which has been proved reliable and robust in different structures [Godoy-2006], as far as enough number of eigenvalues and eigenfunctions are included in the quantum electron density calculation. Both, electrons and holes are included in the Poisson equation although only electrons are treated from a quantum point of view.

The energy valley degeneration of the silicon conduction band has been taken into account. This algorithm provides accurate results for the simulation of different semiconductor structures where the carriers are confined in two dimensions [Trellakis-1997, Godoy-2006,

Godoy-2007a]. The main requirement is that the number of energy levels and wave functions employed in the calculation is high enough to capture all the occupied levels.

The geometry of the SGT confines the electrons in the plane perpendicular to the transport direction, this means that we are dealing with a one-dimensional electron gas. The quantum electron density is therefore obtained by evaluating the following expression [Trellakis-1997]:

$$\rho(r) = \frac{q}{\pi}\left(\frac{2mk_BT}{\hbar^2}\right)^{\frac{1}{2}} \sum_n \psi_n^2(r) \Im_{-\frac{1}{2}}\left(\frac{E_F - E_n}{k_BT}\right) \quad \frac{\mathrm{C}}{\mathrm{cm}^3} \tag{4}$$

Where q is the electron charge, E_F is the Fermi level, ψ_n is the wave function belonging to energy level E_n, $\Im_{-1/2}$ the complete Fermi-Dirac integral of order $-1/2$ and the remaining symbols have their usual meaning. The simulator uses finite elements for the discretization of the equations and then offers the possibility of analyzing different geometries and materials.

2.4.2. Low-field mobility calculation in SGT devices

For mobility calculations, the starting point is the output of the self-consistently solver for the two-dimensional Schrödinger and Poisson equations in the transversal cross-section of the SGT described above. This approximation is accurate enough for electrons in SGT devices[1] of the size simulated in this work [Bescond-2007, Wang-2005]. The mobility is calculated using the Kubo-Greenwood formula [Kubo-1957]. Only phonons and surface-roughness are considered as scattering processes. To calculate the surface-roughness limited mobility a model similar to the one described in [Jin-2007b] has been used, although the possibility of considering anisotropy for the confinement effective mass has been included.

In our case, the fluctuations of the potential energy have not been considered. Besides, it was assumed that the power spectrum of the interface random roughness followed an exponential model characterized by the parameters Δ and L_{sr} [Goodnick-1985]. Both intervalley and acoustic are included following the expressions presented in [Kotlyar-2004].

[1] Also described as quantum nanowires.

3. Double Gate MOSFETs advanced modeling

3.1. Introduction

This chapter is devoted to the DGMOSFET advanced modeling. As reported in the first chapter, these devices, among other multi-gate ones, are currently considered as important candidates to substitute conventional bulk transistors as the mainstream technology in the future. In particular, in these multi-gate transistors geometrical quantum effects due to the confinement of the inversion charge within the silicon channel are very important. They are indeed a major feature to take into account in the modeling and characterization of these devices; therefore, we have started this chapter with the inclusion of an in-depth study, from the modeling point of view, of quantum mechanical effects (QMEs) in low-doped DGMOSFETs for different substrate crystallographic orientations [Balaguer-2011b]. The influence of these QMEs in the inversion charge calculation for devices with different oxide and silicon layer thicknesses has been analyzed for all the interesting operation regimes in order to determine when quantum effects have to be taken into consideration or be neglected, depending on the transistors dimensions, in particular on T_{Si} and T_{ox}. This study is presented in section 3.2.

Section 3.3 is devoted to the description and characterization of the threshold voltage and the electric potential in DGMOSFETs, and the importance of accounting for QMEs effects when calculating these parameters. The inclusion of QMEs, by solving analytically the Schrödinger equation, even when simplifying assumptions are considered, usually makes the new models useless from the circuit simulation viewpoint, since the calculations needed in the study and design of circuits with a high number of components become too time-consuming. Therefore, semiempirical approaches have been considered the appropriate strategy to deal with the inclusion of QMEs in device models. In this context, we have developed sections 3.4 and 3.5 where the inversion charge of these devices is accurately modeled [Balaguer-2012]. To do so, we have considered as starting point the classical analytical, explicit and continuous inversion charge model for undoped symmetrical DGMOSFETs developed in [Moldovan-2007a]. This model that constitutes the basis for the development of this chapter is based on a unified charge control model derived from Poisson's equation and is valid from below to well above threshold with a smooth transition between the different regimes.

The DGMOSFET model previously referenced has been enhanced in order to incorporate QMEs by introducing a modified inversion charge centroid [Balaguer-2012, López-Villanueva-1997] where the role of crystallographic orientations is taken into account. Firstly, the inversion charge centroid for different crystallographic orientations has been developed and secondly, it has been used to calculate the inversion charge including quantum effects also accounting for the different crystallographic orientations of the substrate. This model has been obtained for n-type and p-type devices, and the modeled results have been compared to the simulated data obtained with the software tools described in section 2.3. The role of high-κ dielectric has also been analyzed.

The next part of this chapter is devoted to the characterization of the low-field mobility both in SGMOSFETs and DGMOSFETs, and the analysis of useful rules for mobility model development. Mobility models are essential to deal with drain current model activities. In fact, this latter issue is the subject of the last section of this chapter, where we have introduced a DGMOSFET current model enhancing a previous one (see reference [Lime-2008]). This new DGMOSFET current model takes into account velocity overshoot, QMEs, velocity saturation and short channel effects. This model has been validated by using additional simulation data (obtained with a Multi-Subband Ensemble Monte Carlo DGMOSFET simulator [Sampedro-2011]) as will be explained in section 3.7.

3.2. Quantum mechanical effects

In this section, we will demonstrate that in the subthreshold operation regime, electrical confinement effects (ECEs) can be neglected, since only geometrical confinement effects (GCEs) are important, although they could also be neglected for silicon layers thicker than 20 nm. ECEs are only important above threshold; however, in general, for oxide layers thicker than 2 nm they can be neglected [Balaguer-2011b].

As it has been explained in chapter 1, QMEs make the charge distribution reach its maximum out of the oxide semiconductor interface but inside the silicon film, whereas it virtually vanishes right at the interface [Stern-1972]. The reduction of the silicon layer thickness (T_{Si}) in DGMOSFETs produces (in addition to the electrical confinement effects also present on bulk devices) a high degree of structural or geometrical confinement effects that, for certain silicon layer thicknesses and gate voltages, lead to a high concentration of carriers at the center of the silicon layer (volume inversion operation [Balestra-1987]). The inversion charge

quantization obviously depends on the crystal orientation; in n-type devices this dependence is linked to the orientation of the six silicon ellipsoidal valleys with respect to the confinement direction (this dependence was modeled in n-type bulk MOSFETs for three common substrate orientations [Rodríguez-2007]). As it was made clear in the first chapter of this work, crystallographic orientations different from the conventional (100) one are becoming of interest both because in p-type MOSFETs the low-field mobility is 2.5 times higher on (110) substrates than on conventional (100) substrates [Yang-2003] and because in devices like FinFETs different surface orientations are easily achieved by rotating the fin without having to use non-standard wafer substrates.

In this context, a characterization of QMEs considering different substrate orientations from a compact modeling viewpoint is necessary. The answer to this issue will provide a guide to make clear the need to include QMEs in the inversion charge calculation of DGMOSFETs. In this respect, QMEs increase the complexity of the analytical expressions; therefore, it is crucial to determine what the limits are where QMEs can be neglected, and the error in calculating the inversion charge doing so.

Two groups of simulations were performed to study also the influence of the most significant crystallographic orientations (the substrate orientations chosen were (100) and (110)). The substrate was left undoped and a midgap metal was chosen for both gates. The simulation data were obtained by self-consistently solving the Poisson and Schrödinger equations (the simulator has been described in chapter 2).

Our analysis was based on the calculation of the Q factor, defined as follows:

$$Q = \frac{Q_{Iclassical} - Q_{Iquantum}}{Q_{Iclassical}} \quad (5)$$

where $Q_{Iclassical}$ represents the inversion charge obtained by solving just Poisson equation, and $Q_{Iquantum}$ stands for the inversion charge calculated by self-consistently solving Poisson and Schrödinger equations. We will show that the Q factor successfully determines reasonably well the relative influence of QMEs [Balaguer-2011b, Roldán-2008a].

The Q factor has been plotted in figure 15 for symmetrical DGMOSFETs with different silicon layer thicknesses, for T_{ox} = 1 nm and T_{ox} = 2 nm at room temperature.

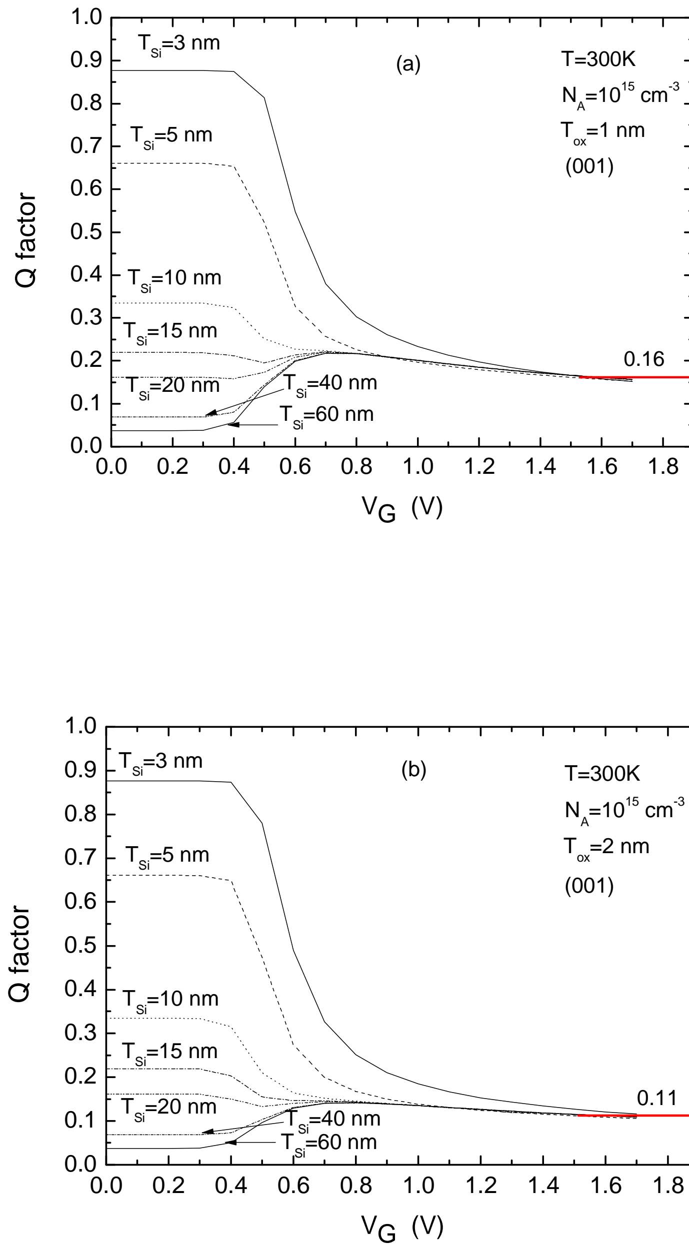
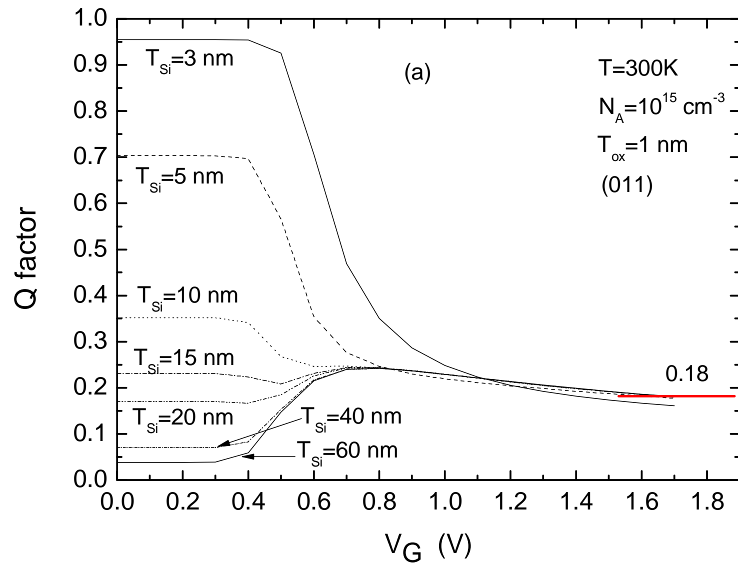


Figure 15. Q factor versus gate voltage for undoped DGMOSFETs grown on (001) silicon at room temperature. (a) T_{ox}=1 nm, (b) T_{ox}=2 nm.

In figure 16, similar calculations are shown for devices grown on (110) Si substrates.



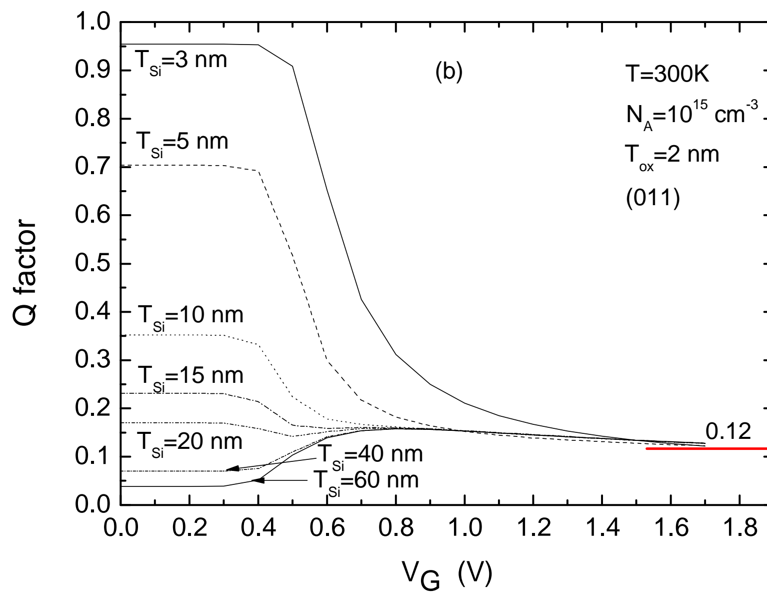


Figure 16. Q factor versus gate voltage for undoped DGMOSFETs grown on (011) silicon at room temperature. (a) T_{ox}=1 nm, (b) T_{ox}=2 nm.

In the previous figures the influence of QMEs on the inversion charge determination is clearly seen:

On the one hand, for $V_G < 0.4$ V, the Q factor shows a constant behavior whose value depends just on T_{Si}; for this gate voltage range GCEs are the most important ones. Obviously, the Q factor rises as T_{Si} is reduced since geometrical confinement increases. For the lowest value considered (T_{Si} =3 nm) the Q factor is close to 0.9 (even higher for (011) substrates), which means that the inversion charge including QMEs is roughly 10% of the classical one.
For T_{Si} =3 nm the device operates in the volume inversion regime [Balestra-1987] for all the gate voltages considered (see also figure 17b).

On the other hand, for $V_G > 0.8$V, ECEs are dominant since the structure enters the strong inversion operation region. We have highlighted (see the horizontal red lines) that in figures 15 and 16 the Q factor curves merge at high gate voltages. This is the expected behavior, and in this operation regime the T_{Si} value is irrelevant (the reader should observe that the thinner T_{Si} the higher V_G needed to reach the value marked with the red line because of higher GCEs influence). In strong inversion, QMEs are very similar to those observed in bulk MOSFETs. Summarizing, from these figures the following facts can be highlighted:

i) At high gate voltages, no matter the T_{Si} value, QMEs (mainly ECEs) should always be considered from the modeling viewpoint (this affirmation works for the T_{ox} values considered in figures 15a and 16a, results for thicker T_{ox} are given latter to clarify this issue) [Balaguer-2011b].

ii) Nevertheless, at low gate voltages, we have to take into account also the T_{Si} values: for the thicker T_{Si} values, QMEs (mainly GCEs) could be neglected (for $T_{Si} > 40$ nm we get $Q < 0.1$, which means that $Q_{Iclassical}$ needs a correction lower than 10% in comparison to $Q_{Iquantum}$, for T_{Si} = 20 nm we get $Q \approx 0.15$, which is also reasonable). For $T_{Si} < 20$ nm the inclusion of QMEs in the inversion charge and drain current models (corresponding to the subthreshold operation regime) is essential [Balaguer-2011b].

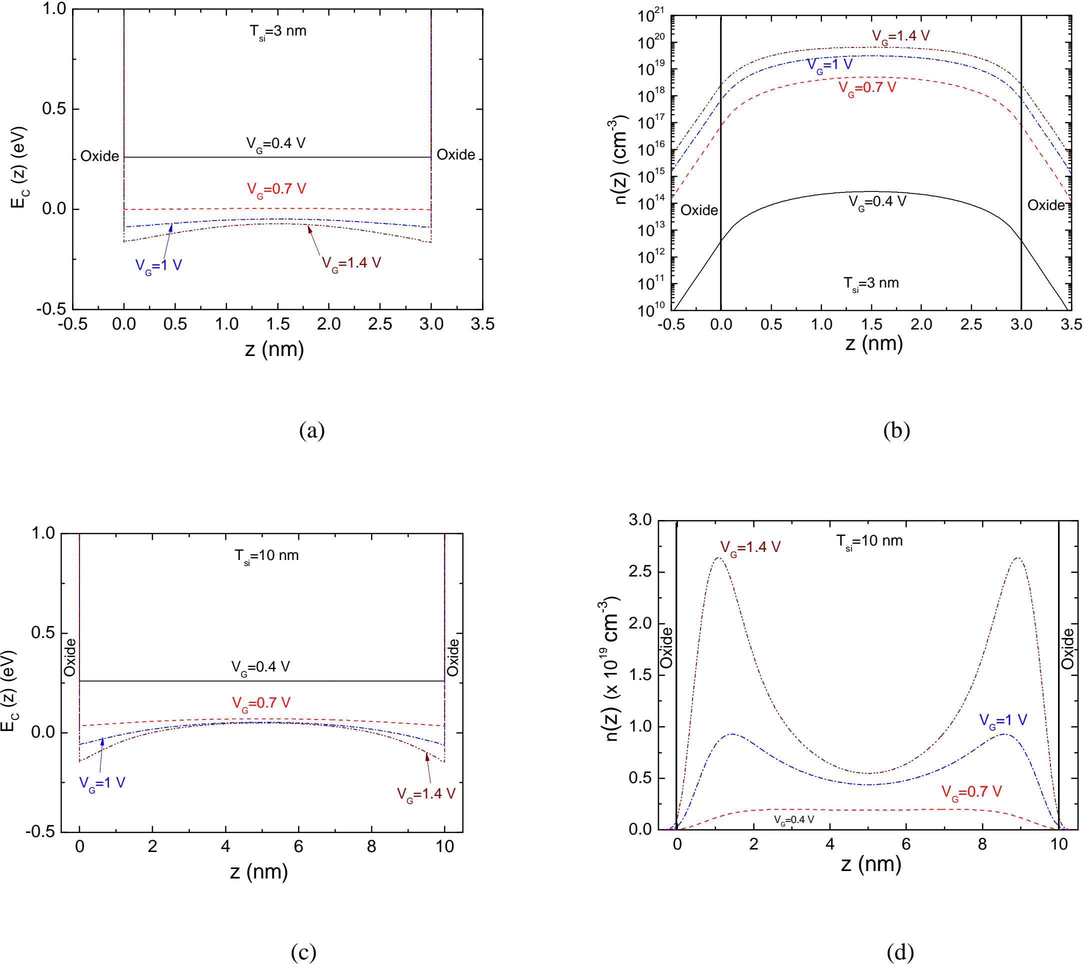


Figure 17. Conduction band edge (a), (c) and electron density (b), (d) as a function of the position along the *z*-axis (perpendicular to the silicon-oxide interface) for an undoped DGMOSFETs grown on a (001) substrate for different gate voltages (T_{ox}=2 nm). (a, b) T_{Si}=3 nm, (c, d) T_{Si}=10 nm.

Most of the facts highlighted above can be understood by means of figure 17. At low gate voltages the quantum well formed by the oxides and the silicon layer is flat (no ECEs), the device operates in volume inversion. This regime is conserved for T_{Si} = 3 nm (figure 17b) because of the strong influence of GCEs, this fact is reflected by the low depth of the potential well at the oxide interface for high gate voltages; for thicker silicon layers (figure 17c) this potential well is deeper.

GCEs - GEOMETRICAL CONFINEMENT EFFECTS

To analyze the influence of GCEs and ECEs separately in the operation of the DGMOSFETs we have plotted $Q(T_{Si}) - Q(T_{Si} = 60\text{ nm})$ in figures 18 and 19 (see in figure 15 that $Q \approx 0$ for T_{Si} = 60 nm at low gate voltages, which implies negligible GCE). For devices with wide T_{Si}

only ECEs are important, i.e., there is no coupling between the two channels. In this consideration, figures 18 and 19 show the isolated influence of GCEs.

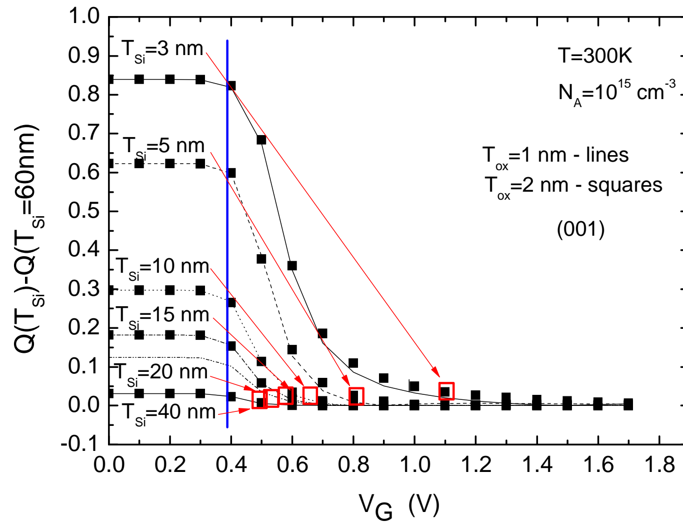


Figure 18. Q factor isolating GCEs versus gate voltage for undoped DGMOSFETs grown on (001) for different T_{Si} at room temperature. T_{ox}=1 nm (lines) and T_{ox}=2 nm (symbols)

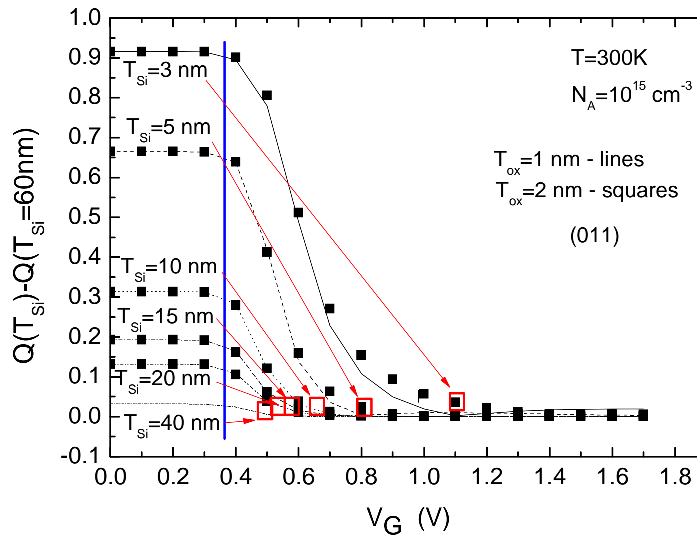


Figure 19. Q factor isolating GCEs versus gate voltage for undoped DGMOSFETs grown on (011) substrates for different T_{Si} at room temperature. T_{ox}=1 nm (lines) and T_{ox}=2 nm (symbols).

GCEs are not dependant on T_{ox} (see the symbols (T_{ox} = 2 nm) plotted almost over the lines (T_{ox} =1 nm) in figures 18 and 19), as it should be since they depend just on T_{Si}. However, ECEs do depend on T_{ox} (see figure 15 and also figures 21-22 below). For T_{ox} =1 nm, $Q \approx 0.16$ at high gate voltages; for T_{ox} = 2 nm, $Q \approx 0.13$. In this respect, the influence of ECEs (which could be characterized by the comparison of T_{ox} with the inversion charge centroid [López-

Villanueva-2000, Rodríguez-2007, Roldán-2008b]) is obviously higher for T_{ox} =1 nm [Balaguer-2011b]. The beginning of the gate voltage interval where the transition from GCEs to ECEs takes place is marked by the blue vertical line, at this point the Q factor starts to drop off till GCEs become negligible with respect to ECEs (this last case is characterized by $Q(T_{Si}) - Q(T_{Si} = 60\text{ nm}) \approx 0$). The gate voltage range where both effects are influential (transition from subthreshold to strong inversion) is highlighted by the vertical blue line and the hollow red squares in figures 18 and 19 for each T_{Si}. In this transition region the threshold voltage (V_T) is found; however, its exact value depends on particular definitions and extraction procedures [Flandre-2010].

The usual consideration given to QMEs from model developers so far has been conditioned to the value of T_{Si} [Taur-2001], this is reasonable since the electron population is confined in the silicon layer. Accordingly, QMEs have been neglected for T_{Si} higher than a certain limit value. However, as shown before, this is not a simple issue since apart from GCEs we have to account for ECEs. Several modeling strategies to deal with QMEs have been published in the last years [Kang-2008, López-Villanueva-1997, Roldán-2008b]. As can be seen in figure 15 and 16, the Q factor depends on V_G and T_{Si}, and therefore physically based models dependent on these parameters are needed. However, for low gate voltages (in the subthreshold operation region) the Q factor is constant and it depends just on T_{Si}. We have plotted this constant Q factor value versus T_{Si} in figure 20.

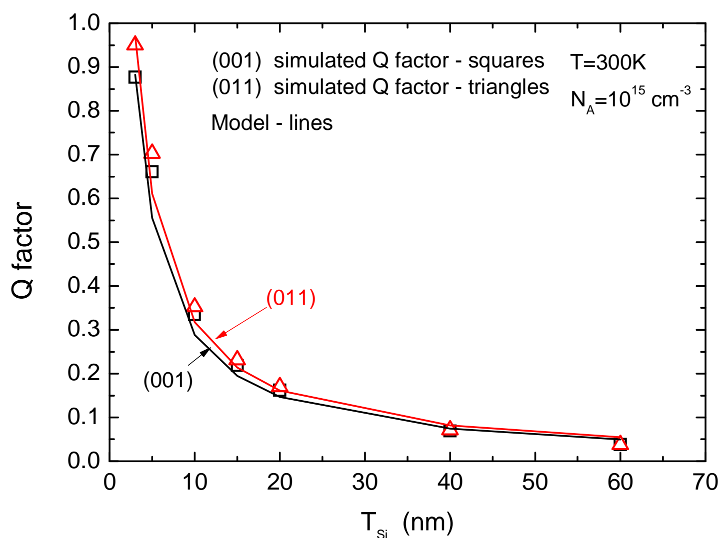


Figure 20. Q factor in the subthreshold operation region versus the silicon layer thickness for undoped DGMOSFETs grown on (001) and (011) substrates. The a parameters chosen in equation 6 was a = 3 nm for (001) substrates and a = 3.3 nm for (011), b was 0.4 nm in both cases.

The curve shown in figure 20 can be fitted with a simple function (equation 6).

$$Q(T_{Si}, a) \approx \frac{a}{T_{Si} + b} \tag{6}$$

Making use of this easy model the inversion charge including QMEs can be obtained from the classical value in the subthreshold operation regime [Balaguer-2011b]. The increasing number of low power applications (most operating in the subthreshold region [Vaddi-2009]) in SOI devices makes this result interesting since it greatly simplifies the inclusion of QMEs on the inversion charge calculation in the compact modeling context.

As highlighted before, a complex model can deal with all the operation regimes and device dimensions in what is related to the inclusion of QMEs. Nevertheless, due to the burden of complicated algebraic expressions in circuit simulators, simple calculation schemes are welcome to avoid convergence problems usually linked to the frequent iterative algorithms needed to obtain the potential and charges included in drain current calculations.

ECEs - ELECTRIC CONFINEMENT EFFECTS

It is also interesting plotting the Q factor for different oxide thicknesses in order to analyze the role that ECEs play on the inversion charge calculation.

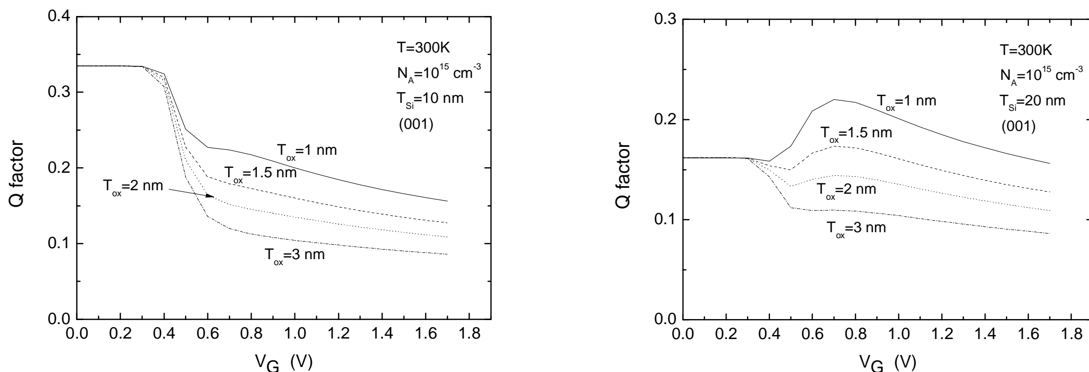


Figure 21. Q factor versus gate voltage for different oxide thicknesses. The devices simulated were undoped DGMOSFETs grown on (001) substrates at room temperature (T_{Si} =10nm, T_{Si} =20nm).

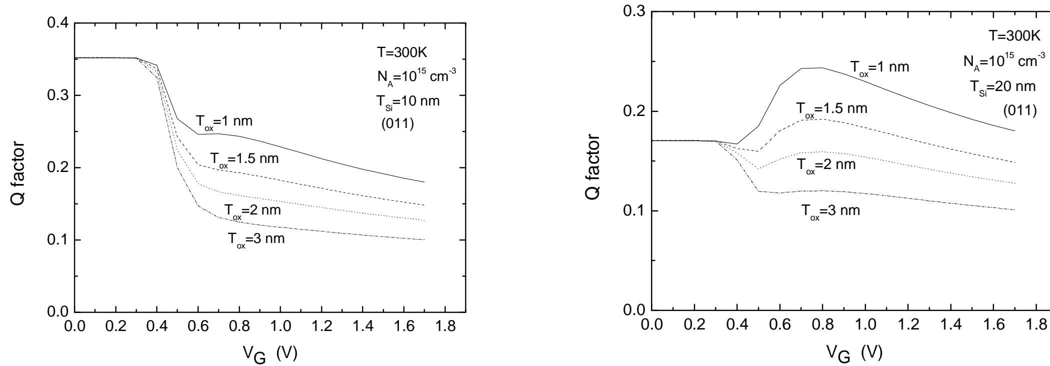


Figure 22. Q factor versus gate voltage for different oxide thicknesses. The devices simulated were undoped DGMOSFETs grown on (011) substrates at room temperature (T_{Si}=10nm, T_{Si}=20nm).

As can be seen, in the strong inversion regime, were ECEs are more significant as highlighted before, the Q factor remains almost constant for the thicker T_{ox} values. However, for thin oxides this "plateau" is not achieved. For $T_{ox} \geq$ 2nm ECEs could be neglected ($Q \leq 0.15$ above threshold). Nevertheless, for thin oxides ECEs can not be neglected. Taking into consideration the current high-performance mainstream technology for SiO_2 insulator thicknesses, the inclusion of the T_{ox} values above 1.5 nm in the previous analysis might seem useless. However, other technologies (e.g. memory and analog electronics applications) with thicker oxides are in use currently for which these results are relevant. In figures 21 and 22, for the T_{Si} = 20 nm case (low GCEs), at the onset of inversion and due to the rise of ECEs, a growth of QMEs is seen (the highest peak obtained in this case is obviously for T_{ox} = 1nm).
We have plotted the data of figures 21 and 22 versus T_{ox} at high gate voltages (figure 23). At these high voltages (V_G = 1.2V and V_G = 1.5V) GCEs are negligible (see that data for T_{Si} =10nm and T_{Si} = 20nm coincide).

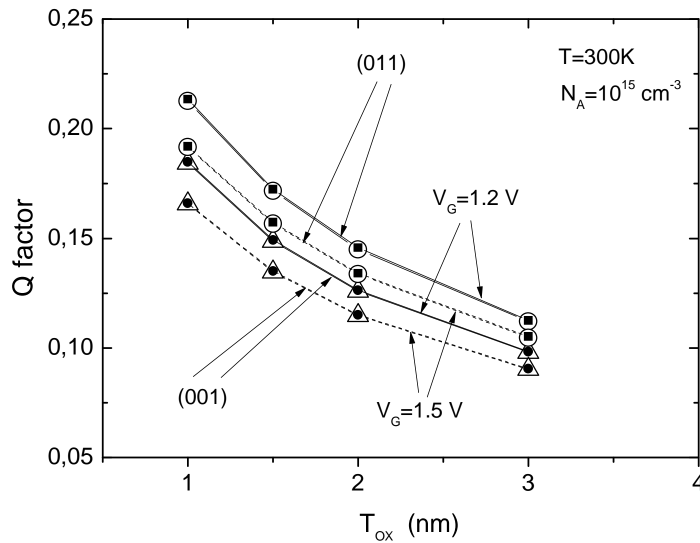


Figure 23. Q factor versus oxide thickness for undoped DGMOSFETs grown on (001) and (011) substrates at room temperature. Two different gate voltages have been used V_G=1.2V and V_G=1.5V. T_{Si}=10nm (solid circles for (001), solid squares for (011)), T_{Si}=20nm (hollow triangles for (001), hollow circles for (011))

As reported before and more clearly seen here, in general, for $T_{ox} \geq 2$ nm QMEs are low. It can be also noticed that there is no dependence on the T_{Si} value (as expected from figures 15 and 16). A wider perspective of this analysis (to explore further the T_{Si} dependence) can be drawn from figure 24 where Q factor contour plots considering all the device dimensions studied here are summarized for V_G=1V.

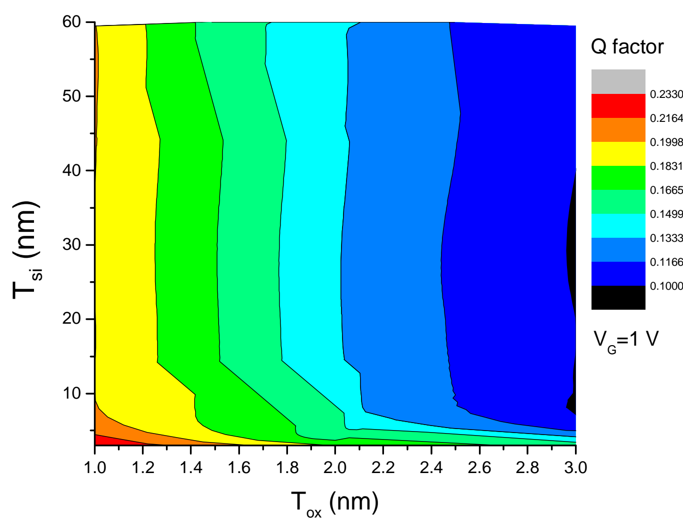


Figure 24. Q factor contour plots versus silicon layer and oxide thickness for undoped DGMOSFETs grown on (001) substrates at room temperature in the strong inversion regime.

The blue and black areas correspond to Q factor values below 0.15 (that could reasonably be considered the area were QMEs are negligible). T_{ox} = 1.8-2 nm represents approximately the boundary value, in addition with $T_{Si} \geq 5$ nm. For $T_{Si} < 5$ nm the influence of GCEs can reach the strong inversion region making the Q factor grow [Balaguer-2011b].

Summarizing the main results presented in this section, QMEs can be neglected in the subthreshold operation region (in this case QMEs are mainly due to GCEs and electrical confinement effects can be neglected) for $T_{Si} > 20$ nm. In this operation region the Q factor shows a constant value dependent on T_{Si} (and independent on V_G) that can be easily modeled by means of a simple model that calculates the quantum inversion charge using the classical charge as starting point. In the strong inversion operation region QMEs can be neglected for $T_{ox} > 1.8$-2 nm if $T_{Si} > 5$ nm. In the operation region between subthreshold and strong inversion (sometimes named moderate inversion) QMEs show a complex behavior due to the contribution of GCEs and ECEs simultaneously.

3.3. Threshold voltage and electric potential

According to the classical theory, when the silicon thickness is reduced, the threshold voltage decreases in a fully depleted SOI MOSFET assuming a constant doping concentration. This is due to the reduction of depletion charge qN_AT_{Si} (assuming an N-type device) when the film thickness is made thinner [Colinge-2008]. When the film thickness is below 10 nm, however, the depletion charge is very small and it can usually be neglected. In this case, nonclassical contributions to threshold voltage have to be taken into account. The concentration of inversion carriers needs to be higher than predicted by the classical theory in order to reach the threshold (consequently, the potential in the silicon film is higher that the classical one) due to the appearance of subbands in the conduction band, which causes an increase in the minimum energy in the conduction band when the silicon thickness is decreased (this effect can explain the increase of the threshold voltage that has been observed experimentally and modeled in nanometric transistors [Trivedi-2005, Lui-2004, Uchida-2000]).
Making use of the simulation data presented in the previous section, we have extracted the threshold voltage (V_T) with two different techniques. On the one hand, we have selected the gate voltage needed to obtain an inversion charge equal to $Q_{IT} = C_{ox}V_{th}$ (where V_{th}=kT/q, k is Boltzmann's constant, T stands for the temperature and q for the electron charge) [Autran-

2005], on the other hand we have extracted the gate voltage at which the $\frac{\partial^2 Q_{Iquantum}}{\partial V_G^2}$ reaches a maximum [Flandre-2010] (the results are shown in Table 1).

T_{Si} (nm)	**(001)**		**(011)**	
	V_T (V) [Autran-2005]	**V_T (V)** [Flandre-2010]	**V_T (V)** [Autran-2005]	**V_T (V)** [Flandre-2010]
3	0.56	0.55	0.57	0.56
5	0.52	0.5	0.525	0.5
10	0.49	0.48	0.49	0.48
15	0.48	0.47	0.48	0.47
20	0.47	0.46	0.47	0.46
40	0.46	0.45	0.46	0.45
60	0.46	0.45	0.46	0.45

Table 1. Threshold voltage for undoped DGMOSFETs grown on different substrates with several silicon layer thicknesses at room temperature.

It can be seen that for (011) substrates V_T is slightly higher for the thinnest T_{Si}, as expected since energy levels for this substrate orientation are higher than in (100) because of lower effective masses in the confinement direction. The V_T values are connected with the curves shown in figures 18 and 19. Higher V_T values are obtained when higher GCEs are present (see that the curves for the lower T_{Si} are shifted to the right, for higher V_G values).

The approach we have followed in this work in order to develop compact models is focused on charge control schemes. As explained in the first chapter, in addition to the use of the inversion charge as state variable, there is an alternative approach that is focused on the use of the electric potential. In surface potential based models the drain current is expressed in terms of surface potential at the source and drain ends of the channel. Some examples of models based on this scheme can be found in [Taur-2001, Taur-2004, Sahoo-2010, Bhattacharyya-2009]. As can be seen in [Ortiz-Conde-2007], both approaches are valid and coherent

equivalent descriptions can be obtained independently of the state variable (inversion charge or surface potential) chosen as basic building block for the model.

Surface potential models were associated traditionally with elevated computational requirements but this problem has been overcome by analytical or numerical algorithms developed in models like PSP [PSP] and HiSIM [HiSIM]. One of the features to highlight in surface potential models [Bhattacharyya-2009] is the fact that their do not adopt a regional modeling approach. They consider drift-diffusion current transport which provides a single expression for the current in all the operation regimes. Despite the models developed in this work are not potential-based, we have described the electric potential behavior within the silicon channel of these devices, and the influence of QMEs on it to shed light in the analysis of DGMOSFETs and for the sake of completeness. In this case, basing the study on the electric potential behavior (although, taking into account our choosing of a charge control model) we will not analyze the electric potential in the (profound) way we have undergone for the inversion charge.

Taking as a starting point the simulation data shown in the section above, we have studied the electric potential. We have compared the classical and quantum potential at the oxide surface and at the channel central position for n-type and p-type DGMOSFETs (see figure 25).

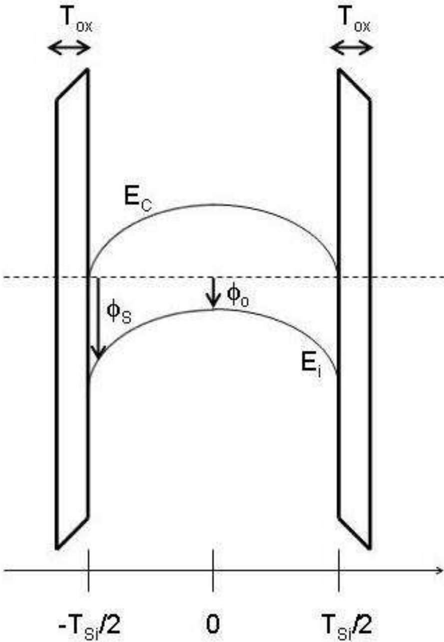


Figure 25. Central and surface electric potential in DGMOSFETs.

The results are plotted in the following figures:

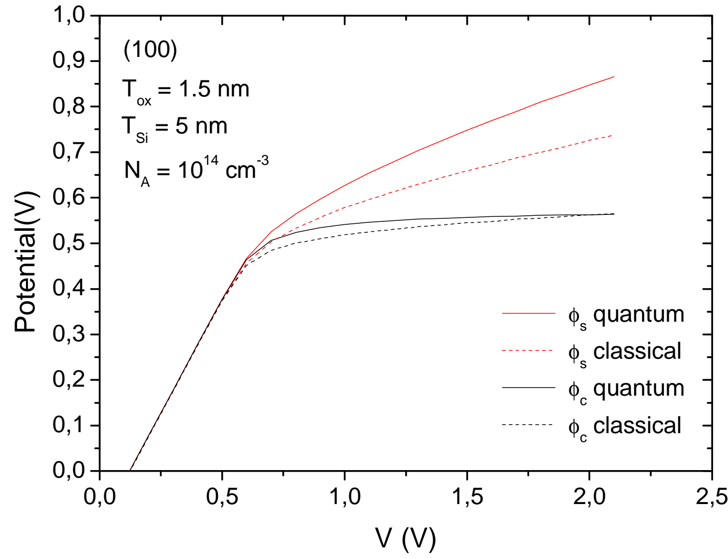


Figure 26. N-type DGMOSFET classical and quantum potentials at the central part of the silicon layer and at the oxide interface.

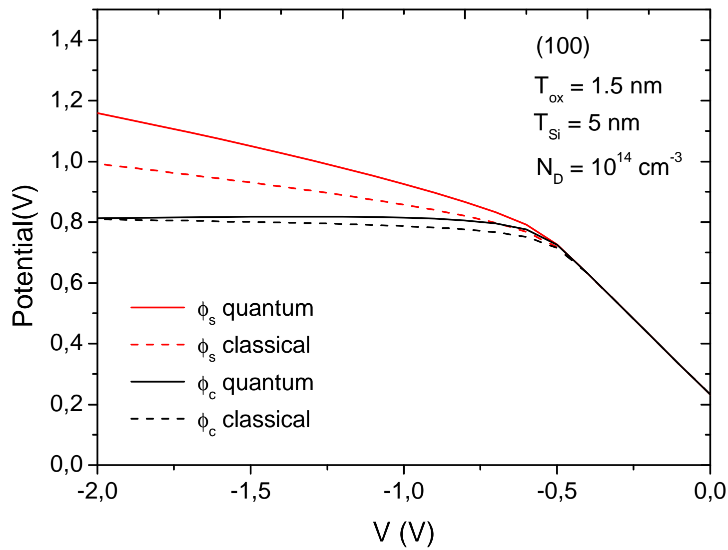


Figure 27. P-type DGMOSFET classical and quantum potential comparison. The values are given at the silicon layer center and at the oxide interface.

For both types of transistors, the potential behavior is quite the same. The central potential is similar to the surface potential in the subthreshold region, no matter if QMEs are included or not, but a difference is observed in the flat part of the curve (corresponding to the strong inversion operation regime). For the surface potential, the differences observed between the

classical and quantum curves are higher than in the central potential case since in strong inversion, the charge located close to the oxide interface screens further gate voltage increases, in this respect the electric potential at the centre of the silicon layer remains constant. The surface potential in strong inversion is higher if QMEs are taken into account, i.e. a higher potential is required to achieve the same amount of inversion charge.
The behavior observed in the figures above remarks the great influence of QMEs also in the electric potential of the devices under study, and the necessity to include them in the calculations when transistor dimensions are reduced (some authors have dealt with this issue recently [Chaves-2010]).

In order to study the surface orientation effects on the electric potential, we have compared the central and surface potentials for n-type and p-type DGMOSFET considering different substrate orientations. The results are shown in the following figures.

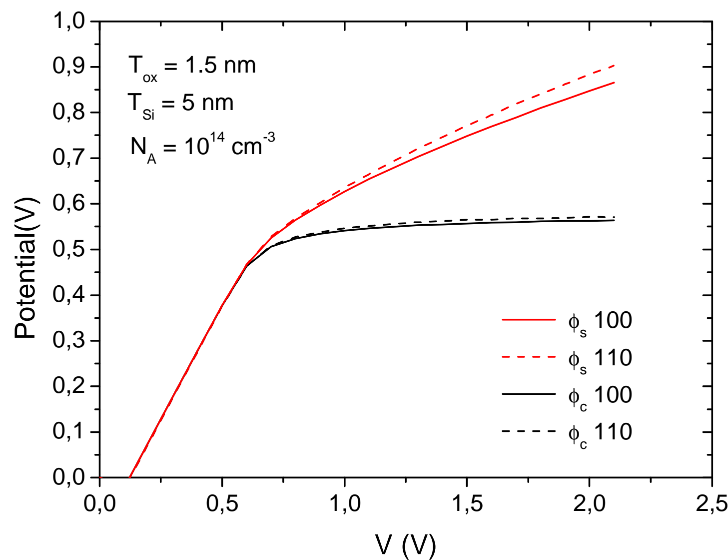


Figure 28. N-type DGMOSFETs (T_{Si} = 5 nm) central and surface potential comparison for (100) and (110) substrate orientations.

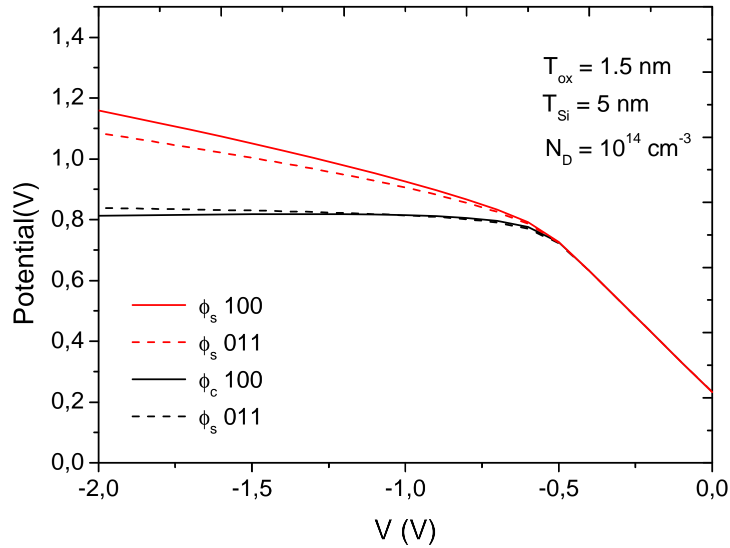


Figure 29. P-type DGMOSFETs (T_{Si} = 5 nm) central and surface potential comparison for (100) and (011) substrate orientations.

In the figures above, significative differences in the surface potential for both types of transistors are obtained for different substrate orientations. It can be concluded, that QMEs and substrate crystallographic orientation effects can not be ignored when modeling the new nanometric DGMOSFET structures. In the following section, as a natural continuation of the systematic study we have already presented, we deal with the study and modeling of DGMOSFETs inversion charge (this magnitude will be the basis of the further drain current model that we will develop in the last section of this chapter).

3.4. Inversion charge centroid for different crystallographic orientations and device geometries

This section is devoted to the study of the influence of the different substrate crystallographic orientations on the spatial distribution of inversion charge in DGMOSFETs. In order to describe the distribution of inversion charge in the silicon layer one of the most interesting parameters that can be used is the inversion layer centroid [López-Villanueva-2000, Rodríguez-2007, Roldán-2008b, Balaguer-2012]. This parameter has been employed to quantify and model the influence of QMEs on the inversion charge of MOSFETs [López-Villanueva-1997] as well as in the gate-to-channel capacitance. As is well known, the accurate calculation of these two magnitudes is essential to develop good compact models.

We have already highlighted that under a quantum mechanical description the charge distribution does not reach its maximum at the oxide-semiconductor interface, but inside the silicon film [Stern-1967, Stern-1972]. While in n-type devices QMEs are linked to the orientation of the six silicon ellipsoidal valleys with respect to the confinement direction, in p-type transistors the strong anisotropy of the valence band makes the differences found for the substrate orientations considered even higher. These differences are plotted for n-type DGMOSFETs in figure 30 showing important dependence on the substrate orientation. Similar results were obtained for p-type DGMOSFETs [Donetti-2010].

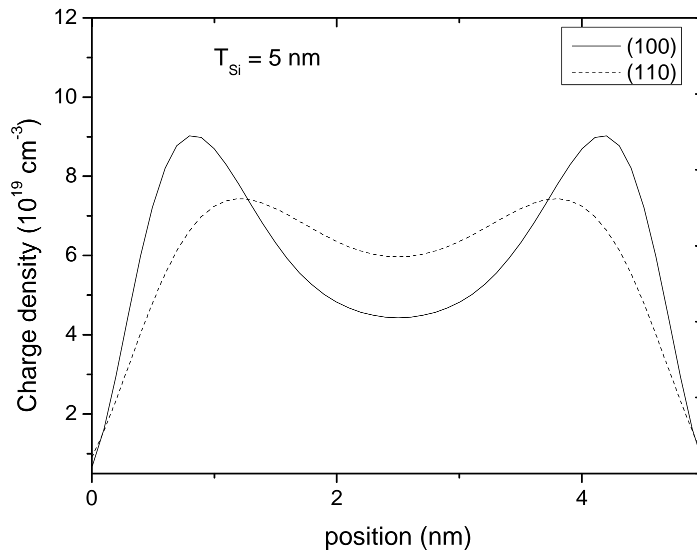


Figure 30. Charge distribution for an undoped n-type DGMOSFET grown on (100) and (110) substrates with V_G = 2.0 V, T_{ox}=1.5 nm.

It obvious that accounting for substrate orientation is necessary not only to calculate the amount of charge but also its distribution. These results gain momentum in a technological context where hybrid substrates and different substrate orientations (that easily come up in devices such as Trigate MOSFETs or FinFETs) are being seriously considered [ITRS-2011]. The analysis and modeling of the inversion charge distribution will be the first step of a more general inversion charge model for n-type and p-type DGMOSFETs, accounting for different substrates orientations, which is of great interest for the microelectronics community [Balaguer-2012].

For the inversion charge centroid model we considered and enhanced a previous DGMOSFET model (and adapted it also for p-type devices) in order to account for the different substrate

orientations. Different silicon layer and dielectric thicknesses were analyzed. As will be shown, the model fits simulation data both in the subthreshold and above threshold operation regions. Firstly we will present the development and results achieved for n-type DGMOSFETs. The starting point equation [López-Villanueva-2000] to model the inversion charge centroid of a DGMOSFET grown on a (100) substrate was the following (this will also be the starting point for p-type DGMOSFETs).

$$\frac{1}{z_I} = \frac{1}{a + bT_{Si}} + \frac{1}{z_{I0}} \left(\frac{N_I}{N_{I0}} \right)^n \tag{7}$$

where a, b, z_{I0}, N_{I0} and n are fitting parameters, and z_I stands for the position of the inversion charge centroid calculated from the insulator-semiconductor interface as follows (n(z) stands for the inversion charge density):

$$z_I = \frac{\int_0^{T_{Si}/2} zn(z)dz}{\int_0^{T_{Si}/2} n(z)dz} \tag{8}$$

The inversion charge centroid (z_I) was calculated, following equation 8, for different symmetric DGMOSFETs with silicon layer thicknesses ranging from T_{Si} = 5 nm to T_{Si} = 20 nm. For each silicon layer thickness, three simulations were performed to study the influence of the different crystallographic orientations (the substrate orientations chosen were (100), (110) and (111)). The gate insulator considered was SiO_2 with two different thicknesses: T_{ox} = 1.5 nm and T_{ox} = 3 nm, the substrate was left undoped and a midgap metal was chosen for both gates.

The centroid data obtained showed very similar values for the (110) and (111) substrate orientations (figure 31), where the inversion charge centroid simulation data are depicted for the three common surface orientations (100), (110) and (111) [Balaguer-2012]. Note that smaller centroid values are obtained for the (100) orientation; this behavior was already observed in bulk devices as reported in [Rodríguez-2007].

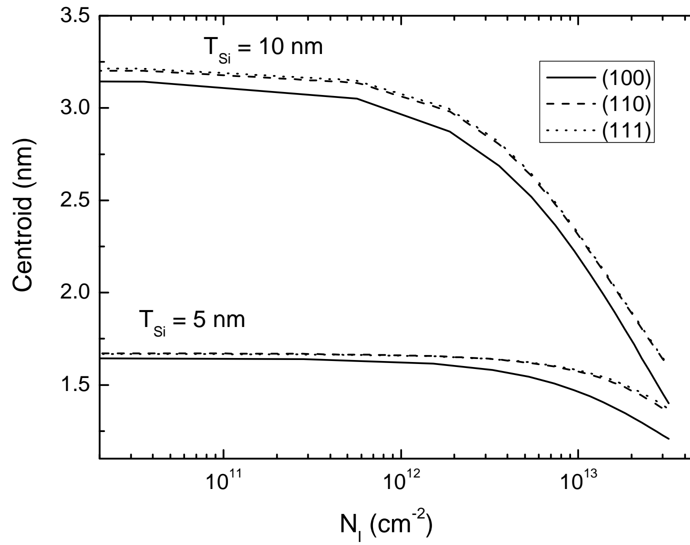


Figure 31. Inversion charge centroid versus the inversion electron concentration in a n-type DGMOSFET structure for the three most common silicon crystallographic orientations (T_{ox}=1.5nm). The data plotted here have been obtained by applying equation 8 to simulations.

The centroid values for the (100) substrate orientation were, in general, lower due to a higher perpendicular (to the oxide-semiconductor interface) effective mass ($m_z=m_l$) for the Schrödinger equation calculation; however, the different subband distributions obtained in DGMOSFETs in comparison to bulk devices might change this behavior for certain silicon layer thicknesses and gate voltage values. In all these cases, equation 7 was modified to fit the simulation data for the considered substrate orientations and silicon thicknesses. The analytical expression used here to model the centroid is the following:

$$\frac{1}{z_I} = \frac{1}{a + bT_{Si} + cT_{Si}^2} + \frac{1}{z_{I0}}\left(\frac{N_I}{N_{I0}}\right)^n \tag{9}$$

Where the N_{I0} = 7 10^{12} cm^{-2} in all cases, and a, b, c, n, z_{I0} values can be found at table 2 at the end of this section (n and z_{I0} depend on T_{Si}, the rest of parameters are constants) [Balaguer-2011c].

Figure 32 shows the inversion charge centroid values obtained for DGMOSFETs grown on (100) substrates for different silicon layer thicknesses.

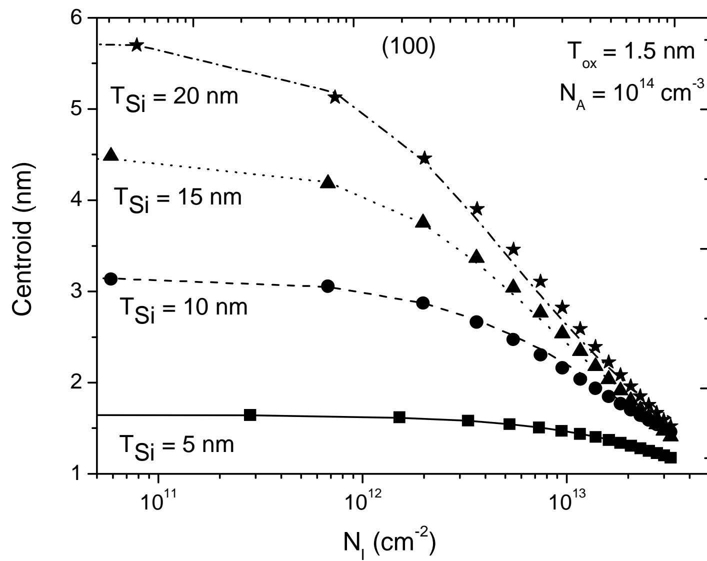


Figure 32. Inversion charge centroid versus inversion charge for an undoped DGMOSFET grown on a (100) substrate, for different silicon layer thicknesses. Simulation results are plotted in lines and modeled data (calculated by using equation 9) in symbols. T_{ox}=1.5 nm (squares – T_{Si}=5 nm, circles – T_{Si}=10 nm, triangles – T_{Si}=15 nm and stars – T_{Si}=20 nm).

In figure 33, the inversion charge centroid data are plotted for DGMOSFETs grown on (110) substrates, similar values are obtained for (111) substrates.

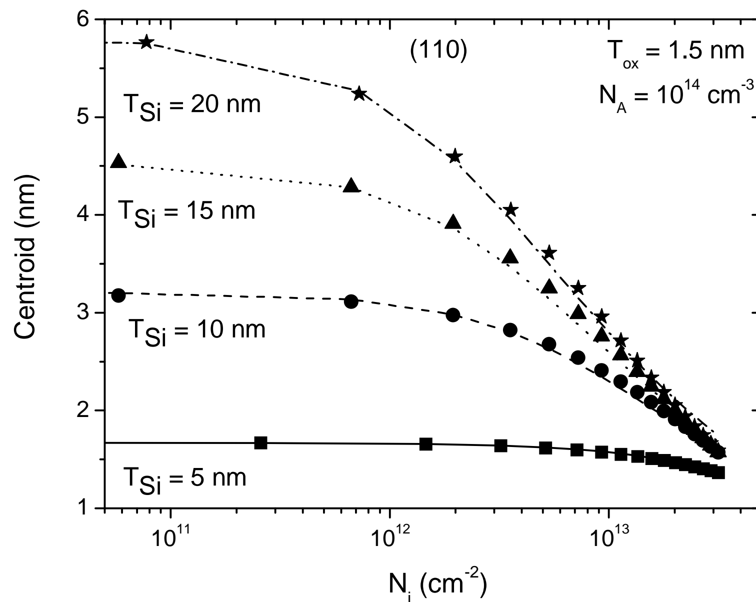


Figure 33. Inversion charge centroid versus inversion charge for an undoped DGMOSFET grown on a (110) substrate, for different silicon layer thicknesses. Simulation results are plotted in lines and modeled data (calculated by using equation 9) in symbols. T_{ox}=1.5 nm (squares – T_{Si}=5 nm, circles – T_{Si}=10 nm, triangles – T_{Si}=15 nm and stars – T_{Si}=20 nm).

The fitting parameters employed to fit simulation data for (110) and (111) silicon substrate orientations are also given in a table at the end of the section. A good fit is observed in all cases. It can be also seen that the centroid for the thinnest silicon inversion layer (T_{Si} = 5 nm) is almost constant for the range of inversion charges considered. In this case, the role played by the structural confinement is much stronger than in thicker silicon inversion layers and the volume inversion regime [Balaguer-2011b, Balaguer-2011c, Celler-2003, Colinge-2004] is observed for almost all the gate voltages used in our study.

In the next part of this section, the inversion charge centroid taking into account different substrate orientation for p-type devices is developed following the same procedure as detailed previously for n-type transistors. To obtain an analytical expression for the hole inversion charge centroid, we used also equation 9. Although it was developed for n-type devices, the model also works to fit the p-type DGMOSFETs simulation data, being the only difference between them the parameters used for the fitting.
The hole inversion charge centroid (z_I) from simulation data was calculated using equation 8 for different devices with silicon layer thicknesses ranging from T_{Si} = 5 nm to T_{Si} = 20 nm. For each silicon layer thickness, three simulations were performed to study the influence of the different crystallographic orientations. The gate insulator considered was SiO_2 (T_{ox} = 1.5 nm), the substrate was left undoped and a midgap metal was also chosen for both gates. The hole inversion charge centroid has been plotted in figure 34 for the three surface orientations under study and for three different silicon layer thicknesses versus inversion charge. As can be seen, the centroid of charge for holes varies substantially as the substrate orientation is changed. This behavior differs from the one observed for electrons, due to the great differences between the conduction and valence bands.

As far as electrons are concerned, smaller values of the inversion charge centroid are obtained for the (100) orientation since, in this orientation, a higher perpendicular effective mass is obtained. Mobility shows also a dependence on different effects as volume inversion, population redistribution among different valleys and phonon scattering form factor, and all these effects are modified when the substrate orientation changes (hole inversion layers have not been as studied as in electron ones due of the strong anisotropy and non-parabolicity of valence band dispersion).

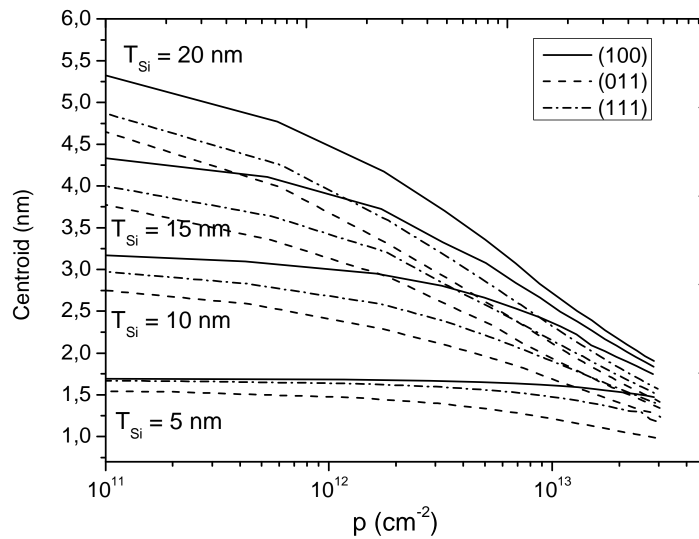


Figure 34. Inversion charge centroid versus the inversion electron concentration in a p-type DGMOSFET structure for the three most common silicon crystallographic orientations (Tox = 1.5 nm). The great anisotropy of the valence band makes the centroid curves separate for the different crystallographic orientations considered, mostly at high inversion charge concentrations.

It can be seen that lower centroid values are achieved for the (110) substrates due to a higher effective mass in the confinement direction of the device. This can be observed in [Donetti-2010], where the valence band of the devices under study is accurately described. This behavior is also different when compared to the n-type devices case, where the lowest centroid values were found for (100) orientation (see Ref. Rodríguez-2007 for results corresponding to the conventional bulk transistor case).

As in the case of electrons (through equation 9), to accurately reproduce simulation data some fitting parameters are made dependant on the silicon layer thickness. The parameters used are given in the table included at the end of this section. Figure 35 shows the hole inversion charge centroid values obtained for DGMOSFETs grown on (100) substrates with different silicon layer thicknesses.

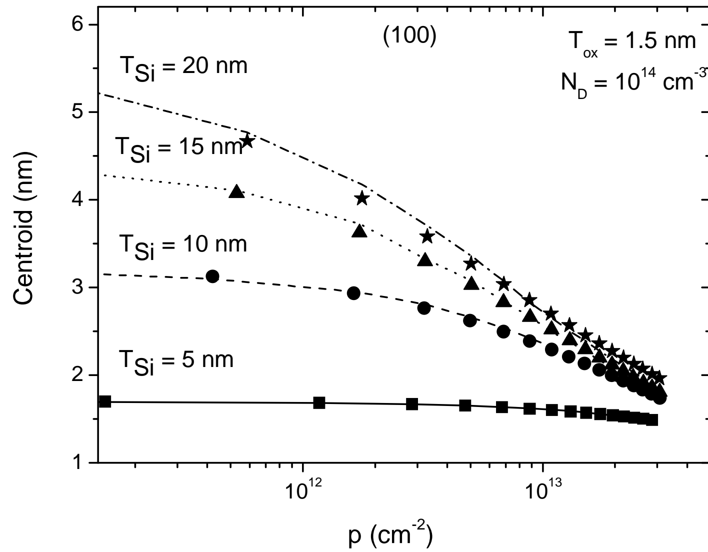


Figure 35. Inversion charge centroid versus inversion charge for an undoped DGMOSFET grown on a (100) substrate, for different silicon layer thicknesses. Simulation results are plotted in lines and modeled data (calculated by using equation 9) in symbols. T_{ox} = 1.5 nm (squares – T_{Si} = 5 nm, circles – T_{Si} =10 nm, triangles – T_{Si}=15 nm and stars – T_{Si}=20 nm).

In figure 36 and figure 37, the hole inversion charge centroid data for the other two substrate orientations are given:

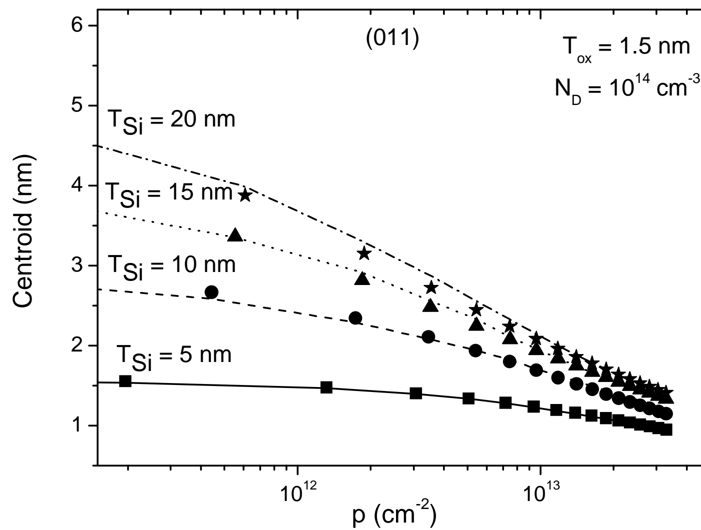


Figure 36. Inversion charge centroid versus inversion charge for an undoped DGMOSFET grown on a (011) substrate, for different silicon layer thicknesses. Simulation results are plotted in lines and modeled data (calculated by using equation 9) in symbols. T_{ox} = 1.5 nm (squares – T_{Si} = 5 nm, circles – T_{Si} =10 nm, triangles – T_{Si} =15 nm and stars – T_{Si}=20 nm).

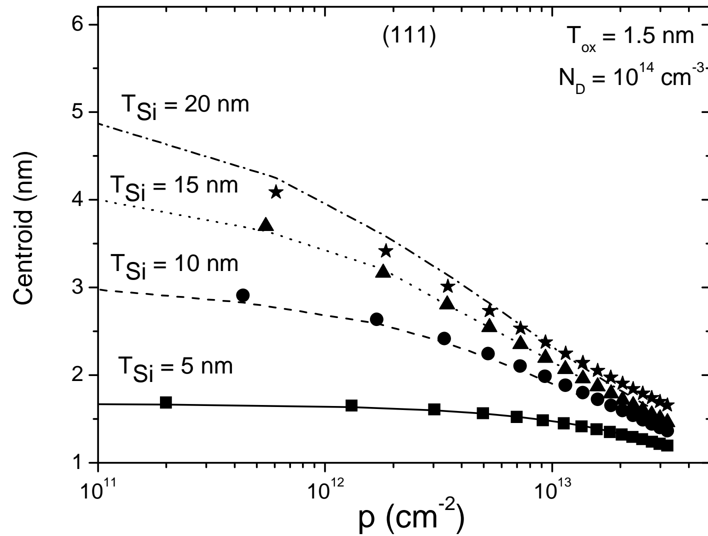


Figure 37. Inversion charge centroid versus inversion charge for an undoped DGMOSFET grown on a (111) substrate, for different silicon layer thicknesses. Simulation results are plotted in lines and modeled data (calculated by using equation 9) in symbols. Tox =1.5 nm (squares – TSi = 5 nm, circles – TSi = 10 nm, triangles – T_{Si} = 15 nm and stars – T_{Si} =20 nm).

A good fit is observed in all cases. It can also be seen, as in the electron case, that the centroid for the thinnest silicon inversion layer (T_{Si} = 5 nm) is almost constant for the considered range of inversion charges. This is due to structural confinement effects that, as explained before, lead to operation in the volume inversion regime [Balaguer-2011b, Balaguer-2011c, Celler-2003, Colinge-2004].

3.5. Inversion charge including quantum effects for different crystallographic orientations and geometries

In this section we step forward from the set of results presented in the previous section. An inversion charge model that takes into account QMEs allowing the description of devices with different crystallographic orientations is developed. To do so, the centroid model developed in the previous section was incorporated. As a first step, we considered a classical inversion charge model [Moldovan-2007a, Sallese-2005]. This model, as well as the enhanced version we are presenting here to include QMEs, are both explicit. Therefore, the inversion charge is obtained in a direct calculation without having to use iterative algorithms to solve non-linear equations. This is an outstanding advantage in comparison to other approaches for the inclusion of the model in compact models for circuit simulation schemes.

We have used the expression below to calculate a first estimation of the inversion charge. This value will be used to obtain other quantities (equations 13 and 14, where Q' is employed) that will be needed latter in equation 12, which is the final value we will consider for the classical inversion charge:

$$Q^{'}(V) = 2C_{ox}\left(\left(-\frac{2C_{ox}\beta^2}{Q_o}\right)+\sqrt{\left(\frac{2C_{ox}\beta^2}{Q_o}\right)^2+4\beta^2\ln^2\left[1+\exp\left[\frac{V_{GS}-V_o-V}{2\beta}\right]\right]}\right) \quad (10)$$

where the parameters used within are given as follows [Moldovan-2007a, Sallese-2005, Balaguer-2011c]:

$$\beta = \frac{KT}{q}$$
$$Q_o = 4\left(\frac{KT}{q}\right)C_{si} \quad (11)$$
$$V_0 = \Delta\varphi - \beta\ln\frac{qn_iT_{Si}}{2Q_o}$$

Where $\Delta\varphi$ is the work-function difference between the gate electrode and the intrinsic silicon, $C_{Si}=\varepsilon_{Si}/T_{Si}$, and V is the electron quasiFermi potential. For the classical calculation, the inversion charge was obtained with the expression given below,

$$Q(V) = 2C_{ox}\left(\left(-\frac{2C_{ox}\beta^2}{Q_o}\right)+\sqrt{\left(\frac{2C_{ox}\beta^2}{Q_o}\right)^2+4\beta^2\ln^2\left[1+\exp\left[\frac{V_{GS}-V_T+\Delta V_T-V}{2\beta}\right]\right]}\right) \quad (12)$$

where V_T and ΔV_T stand for,

$$V_T = V_o + 2\beta\ln\left(1+\frac{Q^{'}}{2Q_o}\right) \quad (13)$$

$$\Delta V_T = \frac{\left(\frac{C_{ox}\beta^2}{Q_0}\right)Q^{'}}{\frac{Q^{'}}{2}+Q_0} \quad (14)$$

The classical expression given in equation (12) was enhanced to account for QMEs. We did so by using a modified oxide capacitance C^{*}_{ox} (instead of C_{ox}) that includes the inversion layer centroid model developed in the previous section (see the equation below) [Balaguer-2012].

$$C^{*}_{ox} = \frac{\varepsilon_{ox}}{T_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{si}} z_I + \frac{Q'}{\varepsilon_{si}} \frac{dz_I}{dQ'} \varepsilon_{ox}} \qquad (15)$$

The term that introduces the centroid derivate has been included to correctly reproduce the device capacitance above threshold following the work of L. Ge et al. [Ge-2006]. The centroid derivative was calculated making use of the model given in equation 9, where Q' has been calculated by using $Q' = qN_I$. In the following figure the role played by the centroid derivative factor (third term in the denominator of equation 15) can be distinguished. In figure 38 the capacitance obtained from the simulation data is depicted together with the enhanced capacitance C^{*}_{ox} calculated with and without the centroid derivative term. It can be clearly seen that this term is needed in strong inversion.

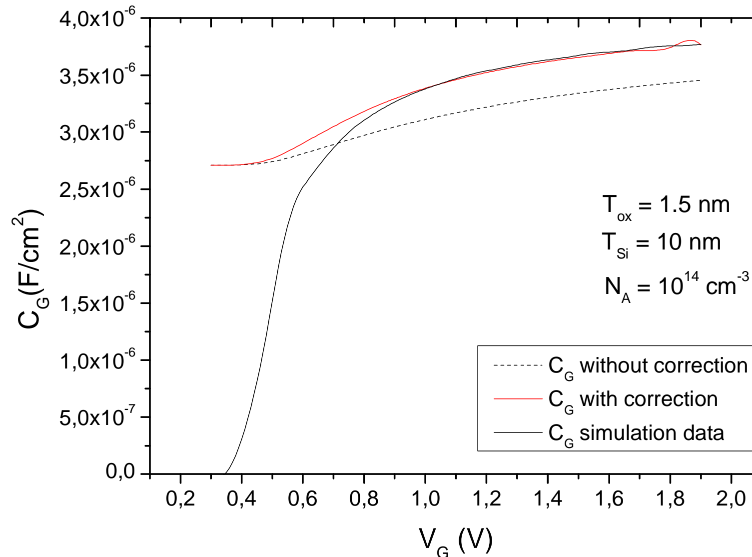


Figure 38. Gate capacitance versus V_G for a symmetrical n-type DGMOSFET with T_{Si} = 10 nm. Capacitance obtained from simulation data is plotted in black solid line, the capacitance obtained without taking into account the centroid derivative correction is shown in black dashed line and the capacitance obtained from the model including the centroid derivative term is shown in red.

The modified oxide capacitance C^{*}_{ox} was used in equation 14 and latter (in addition to the output of equation 14) in equation 12. In this way the inversion charge, including QMEs, was calculated. In figure 38, a comparison between the simulated and modeled (not including QMEs) inversion charge is shown. As can be seen, without the inclusion of QMEs simulation data can not be reproduced accurately.

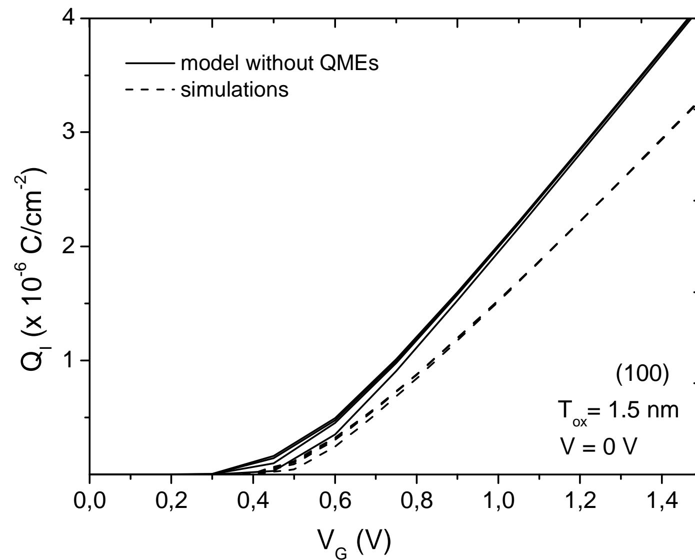


Figure 39. Inversion charge versus gate voltage for undoped silicon DGMOSFETs grown in (100) substrates with T_{ox} =1.5 nm and for different silicon thicknesses (T_{Si} = 5 nm, T_{Si} = 10 nm, T_{Si} = 15 nm and T_{Si} = 20 nm). Simulations are plotted in dashed lines and modeled data (without QMEs) in solid lines.

In figures 39 to 42, the inversion charge calculated making use of the model is plotted versus gate voltage and compared with simulation data for the (100) and (110) crystallographic substrate orientations (the inversion charge for (111) is approximately the same than in the (110) case).

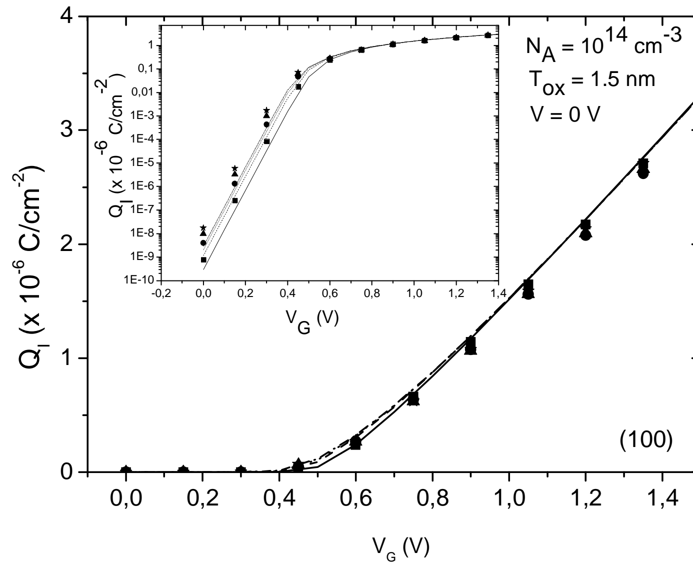


Figure 40. Inversion charge versus gate voltage for an undoped silicon DGMOSFET in linear and logarithmic (inset) scales with T_{ox} = 1.5 nm and (100) substrate orientation for different silicon thicknesses. Simulation results are plotted in lines and modeled data in symbols (squares – T_{Si} = 5 nm, circles – T_{Si} = 10 nm, triangles – T_{Si} = 15 nm and stars – T_{Si} = 20 nm).

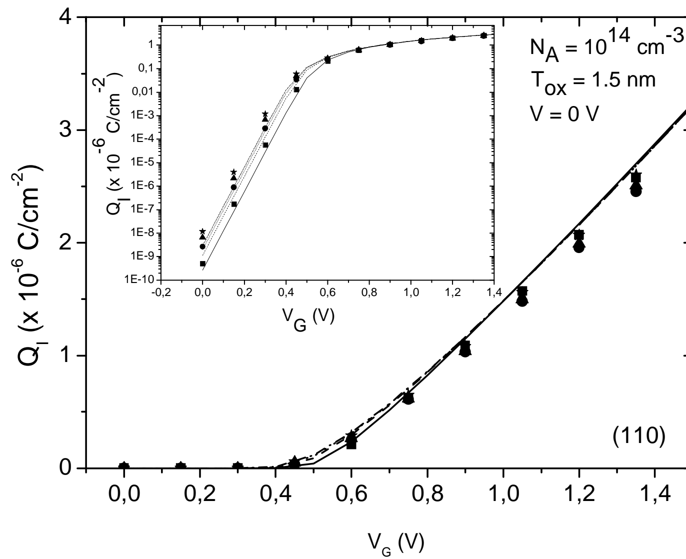


Figure 41. Inversion charge versus gate voltage for an undoped silicon DGMOSFET in linear and logarithmic (inset) scales with T_{ox} = 1.5 nm and (110) substrate orientation for different silicon thicknesses. Simulation results are plotted in lines and modeled data in symbols (squares – T_{Si} = 5 nm, circles – T_{Si} = 10 nm, triangles – T_{Si} = 15 nm and stars – T_{Si} = 20 nm).

We have also checked the validity of the model by using different oxide thicknesses. In particular, the following (see the figures below) results are obtained for T_{ox} = 3 nm.

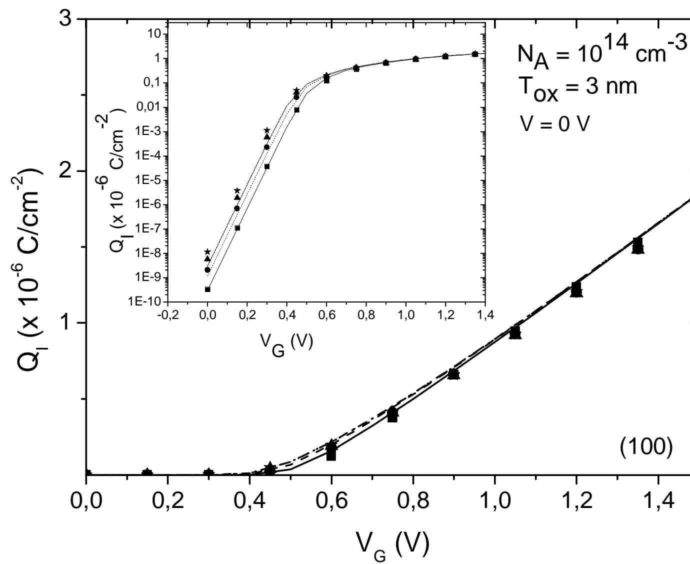


Figure 42. Inversion charge versus gate voltage for an undoped silicon DGMOSFET in linear and logarithmic (inset) scales with T_{ox} = 3 nm and (100) substrate orientation for different silicon thicknesses. Simulation results are plotted in lines and modeled data in symbols (squares – T_{Si} = 5 nm, circles – T_{Si} =10 nm, triangles – T_{Si} =15 nm and stars – T_{Si} =20 nm).

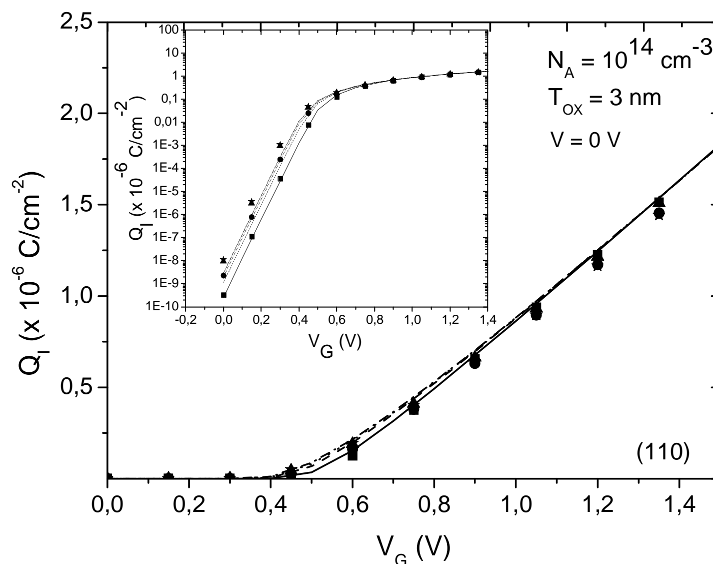


Figure 43. Inversion charge versus gate voltage for an undoped silicon DGMOSFET in linear and logarithmic (inset) scales with T_{ox} = 3 nm and (110) substrate orientation for different silicon thicknesses. Simulation results are plotted in lines and modeled data in symbols (squares – T_{Si} = 5 nm, circles – T_{Si} = 10 nm, triangles – T_{Si} = 15 nm and stars – T_{Si} = 20 nm).

As can be seen in figures 40-43, the model works reasonably well for all the devices considered (this means n-type structures with different substrate orientations, a wide range of

oxide and silicon layer thicknesses and for all the operation regimes worth being considered). The different effects involved are coherently taken into account; in this context a reasonable error in few cases is unavoidable since the accuracy of the physics that would be needed to perfectly fit all the cases under study would make extremely difficult the development of an analytical and explicit model that could be regarded appropriate from the compact modeling viewpoint. As can be seen in the previous figures, a weak dependence on T_{Si} in strong inversion is observed. This is due to the reduction of the influence of geometrical effects since almost all the charge is confined at the silicon-oxide interfaces due to the high transverse electric field (electric confinement effects). In this case, the silicon layer thickness has not much influence on the charge, this effect can be seen also in reference [He-2004] and has been deeply described before [Balaguer-2011b].

To reproduce the hole inversion charge, a model analogue to the one presented previously for electrons is used. The model is also explicit, as in the n-type device case; therefore, there is also no need of iterative algorithms. Following a modeling procedure similar to the one presented previously for the calculation of the electron inversion charge, we have obtained analogue analytical expressions for the hole case [Balaguer-2011c].

A first estimation of the holes inversion charge is calculated as follows:

$$Q^{'} = 2C_{ox}\left(\left(-\frac{2C_{ox}\beta^2}{Q_o}\right) + \sqrt{\left(\frac{2C_{ox}\beta^2}{Q_o}\right)^2 + 4\beta^2 \log^2\left[1+\exp\left[\frac{-(V_{GS}-V_o-V)}{2\beta}\right]\right]}\right) \qquad (16)$$

where the parameters used within are given as follows:

$$\beta = \frac{KT}{q}$$
$$Q_o = 4\left(\frac{KT}{q}\right)C_{si} \qquad (17)$$
$$V_0 = \Delta\varphi + \beta \ln \frac{q n_i T_{Si}}{2Q_o}$$

The classical inversion charge for holes was calculated with the following expression, obtained following the same procedure as in the electrons case:

$$Q = 2C_{ox}\left(\left(-\frac{2C_{ox}\beta^2}{Q_o}\right)+\sqrt{\left(\frac{2C_{ox}\beta^2}{Q_o}\right)^2+4\beta^2\log^2\left[1+\exp\left[\frac{-(V_{GS}-V_T+\Delta V_T-V)}{2\beta}\right]\right]}\right) \quad (18)$$

where V_T and ΔV_T stand for:

$$V_T = V_o - 2\beta\ln\left(1+\frac{Q^{'}}{2Q_o}\right) \quad (19)$$

$$\Delta V_T = \frac{\left(\frac{C_{ox}\beta^2}{Q_0}\right)Q^{'}}{\frac{Q^{'}}{2}+Q_0} \quad (20)$$

The classical expression given in equation (18) was modified to account for QMEs. We did so in an analogue way as it was done before; this is, by using a modified oxide capacitance C^{*}_{ox} where the inversion layer centroid model developed in the previous section was included (see the equation below).

$$C^{*}_{ox} = \frac{\varepsilon_{ox}}{T_{ox}+\frac{\varepsilon_{ox}}{\varepsilon_{si}}z_I+\frac{Q^{'}}{\varepsilon_{si}}\frac{dz_I}{dQ^{'}}} \quad (21)$$

As shown for n-type devices, the third term in the denominator (centroid derivate) has also been used to correctly reproduce the device capacitance above threshold. The centroid derivative was calculated making use of the model given in equation 7.

In figures 43 to 45, the inversion charge is plotted versus gate voltage for the (100) and (011) and (111) crystallographic substrate orientations (modeled and simulation data are shown).

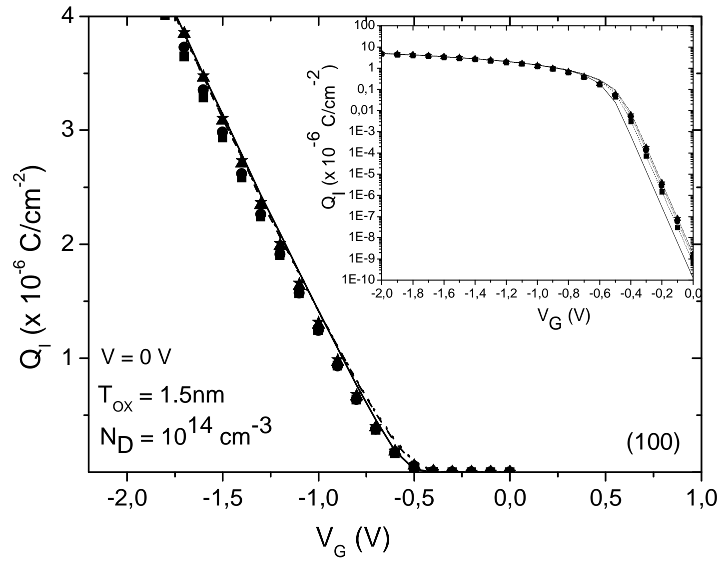


Figure 44. Inversion charge versus gate voltage for an undoped silicon DGMOSFET in linear and logarithmic (inset) scales with T_{ox} = 1.5 nm and (100) substrate orientation for different silicon layer thicknesses. Simulation results are plotted in lines and modeled data in symbols (squares – T_{Si} = 5 nm, circles – T_{Si} = 10 nm, triangles – T_{Si} = 15 nm and stars – T_{Si} = 20 nm).

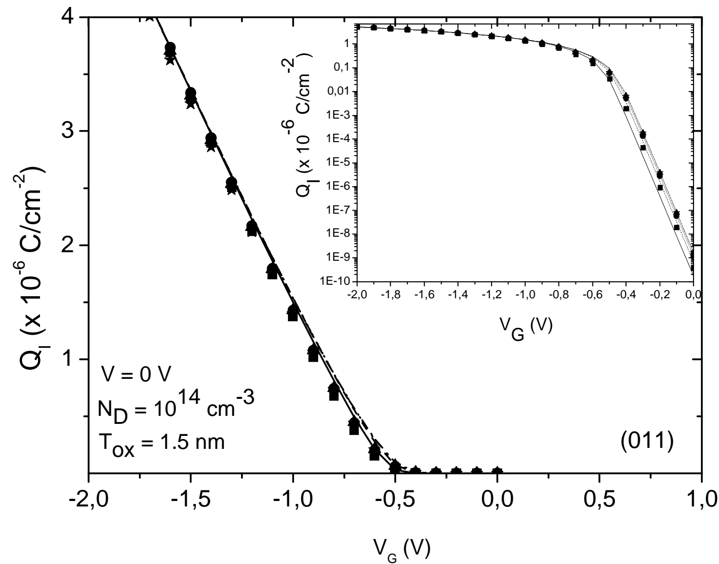


Figure 45. Inversion charge versus gate voltage for an undoped silicon DGMOSFET in linear and logarithmic (inset) scales with T_{ox} = 1.5 nm and (011) silicon substrate orientation for different silicon layer thicknesses. Simulation results are plotted in lines and modeled data in symbols (squares – T_{Si} = 5 nm, circles – T_{Si} = 10 nm, triangles – T_{Si} = 15 nm and stars – T_{Si} =20 nm).

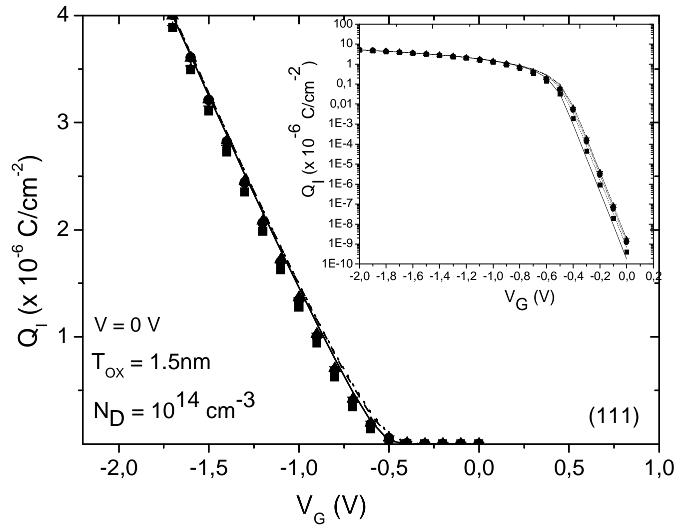


Figure 46. Inversion charge versus gate voltage for an undoped silicon DGMOSFET in linear and logarithmic (inset) scales with T_{ox} = 1.5 nm and (111) substrate orientation for different silicon layer thicknesses. Simulation results are plotted in lines and modeled data in symbols (squares – T_{Si} = 5 nm, circles – T_{Si} =10 nm, triangles – T_{Si} = 15 nm and stars – T_{Si} = 20 nm).

As can be seen in the previous figures, a reasonably good fit is obtained for the three silicon orientations considered and for different silicon layer thicknesses. For these p-type devices, QMEs, due to the anisotropy of the valence band, show a different behavior than in n-type devices; however, the model works well in both cases, proving its correctness. The model reproduces simulation data in the subthreshold and strong inversion operation regions.

	$n(T_{Si})$	a (nm)	b	c (nm^{-1})	$z_{I0}(T_{Si})$ (nm)
Electrons (100)	-0.0112 T_{Si} + 1.0200	0.0600	0.3284	-0.002	53.83 $T_{Si}^{-0.70}$
Electrons (110)	-0.0154 T_{Si} + 1.1150	0.0600	0.3286	-0.002	212.49 $T_{Si}^{-1.01}$
Electrons (111)	The same as (110)	The same as (110)	The same as (110)	The same as (110)	The same as (110)
Holes (100)	-0.0236 T_{Si} + 0.9600	0.355	0.2759	0.0005	323.38 $T_{Si}^{-1.38}$
Holes (110)	-0.0174 T_{Si} + 0.77750	0.275	0.2545	0.0016	14.46 $T_{Si}^{-0.467}$
Holes (111)	-0.0272 T_{Si} + 0.9650	0.3300	0.2762	0.0002	57.74 $T_{Si}^{-0.887}$

Table 2. Parameters used in equation 9 for the inversion charge centroid modeling. T_{Si} is given in nanometers for both n- and p-type devices.

To finish this section we highlight the role that high-κ materials play in the new nanometric MOSFET generation (as already pointed out in the first chapter). In relation to these materials, the main idea from the modeling viewpoint is that the capacitance does not change if the equivalent oxide thickness is maintained. It has to be highlighted that the energetic gap between the high-κ material and the silicon changes and this fact affects the penetration of the electron wave functions in the insulator and, consequently, the inversion charge centroid. As a result the inversion charge is different. As reported in the first chapter, a great reduction of the oxide tunneling current is achieved in these materials and consequently of the standby power in the circuits associated. In chapter 5, a detailed study is presented in relation to SGTs with high-κ dielectrics as gate insulators.

3.6. Mobility characterization in single- and double-gate MOSFETs

Mobility is one of the key parameters to characterize and model the transistor current. Taking into consideration the needs we highlighted previously in the circuit simulation context, its obvious that simple and physically-based mobility models are required, but this is not an easy task. In SOI single-gate devices and DGMOSFETs there are several effects (silicon thickness, gate voltage, roughness of the top and buried oxide layers, charge at the oxide interfaces and within the oxides…) influencing at the same time on the charge transport characteristics and leading to a very complex behavior of the total low-field mobility. For these devices, there are very few models simple enough (in most of them the oxide interfaces were supposed to be identical) that can be used in circuit simulators without including an algebraic burden that can turn a model useless for circuit simulation. For this reason it is very important to perform a systematic study, which can only be done by means of simulation, to analyze how Coulomb and surface-roughness scattering affect the mobility. The conclusions of this study will allow the simplification of future mobility models in order to include the Coulomb and surface-roughness effects of each oxide interface separately. In this respect, previously established mobility models could be enhanced, and new ones developed, to account for different oxide characteristics. Apart from the circuit simulation approach, an obvious interest from the process engineering field is deduced since a reasonable estimation of the final low-field mobility could be extracted for different fabrication processes.

This task has been carried out and is presented in this section. For the sake of clarity we will face the study in a progressive manner, therefore, firstly we will present the results obtained for single-gate devices and latter on we will deal with double-gate devices (DGMOSFETs) where the analysis is more complicated.

As explained before, the reduction of silicon layers in SOI devices increase the geometrical confinement and the distribution of the inversion charge in comparison with bulk transistors [Balaguer-2011b, Balaguer-2012]. Consequently, the main transport features (the conductivity effective mass and the phonon scattering rates, among others) are different [Gámiz-1998a]. In addition, the proximity of oxide interfaces to the channel inversion charge makes both surface-roughness and Coulomb scattering due to oxide interface charges much more important than in bulk devices [Gámiz-2002, Jiménez-Molinos-2005, Gámiz-2001]. Surface-roughness scattering has been studied in depth in [Gámiz-2001] and [Gámiz-1999b]. On the other side, Coulomb scattering mechanisms have been detailed in [Jiménez-Molinos-2010a, Gámiz-2002, Gámiz-2003a].

Understanding Coulomb scattering in UTB SOI transistors is essential since the microelectronic industry tends to thin the silicon layer in the scaling process. To improve the performance of the transistor (and to develop accurate models), it is useful to discover the influence of the interface charges (and surface-roughness) both at the buried and the gate oxide interfaces on the Coulomb (surface-roughness) mobility component. To do this, we have made use of the Monte Carlo simulator (developed within the nanoelectronic research group of the University of Granada) with advanced Coulomb and surface-roughness scattering models [Gámiz-2003b] presented in section 2.3.1.2.

In order to analyze the influence of Coulomb scattering on the mobility in UTB-SOI MOSFETs, we carried out a large number of simulations for different structures and densities of interfacial charged centers at the silicon-oxide interfaces.

a) SGMOSFET study

Figure 47 shows a schematic representation of the devices studied in this section, whose common features are the following: they consist of single-gate SOI NMOSFETs with a 1.5 nm layer of silicon dioxide as gate insulator under a metal gate. The thickness of the buried silicon dioxide is 80 nm. Finally, the silicon channel is intentionally kept undoped and its thickness is given several values (T_{Si}).

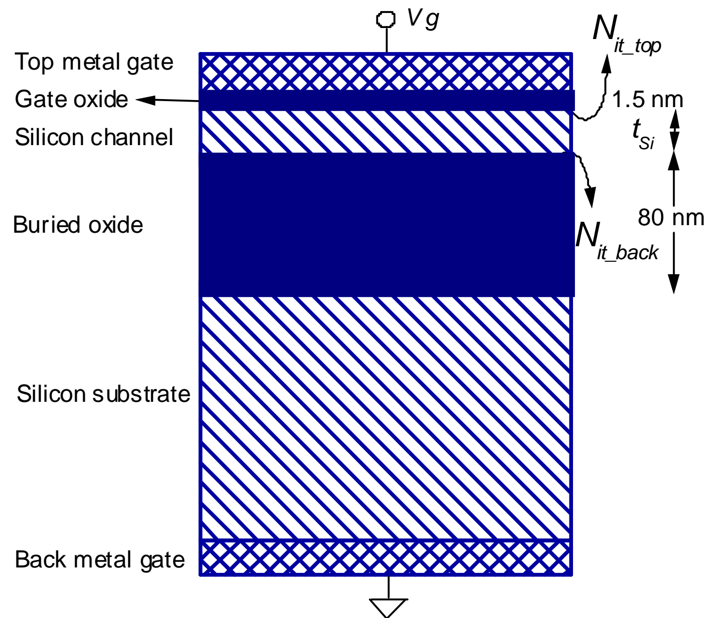


Figure 47. Schematic of the silicon-on-insulator structure considered.

Figure 48 shows the mobility curves obtained for the narrowest silicon layer (T_{Si} = 3 nm) versus the inversion electron concentration. Several densities of interfacial charged centers were considered at both interfaces. For each curve, the value of these interfacial charge densities is given by a pair of numbers: the first is the bi-dimensional density of charged centers at the gate oxide interface (N_{it_top}, expressed in 10^{10} cm^{-2}) whereas the second is the value of the charged center density at the buried oxide interface (N_{it_back}). In order to analyze the influence of the two interfaces separately, curves corresponding to devices with charges at only one interface are shown. We will later analyze the case of interface traps at both interfaces. As can be seen, curves corresponding to devices with the same density of interface-trapped charges approximately match: this means that the interface where they are placed has no significant influence (that is, curve (a,0) matches curve (0,a)). This result is consistent with the inversion charge distribution shown in figure 49 for an inversion charge concentration of N_I = 2 x 10^{12} cm^{-2}. The electron distribution in this case is almost symmetrical with regard to each interface and its center is practically in the middle of the silicon layer, at the same distance from both interfaces [Jiménez-Molinos-2010a]. Consequently, charges at the gate oxide interface have approximately the same influence as those placed at the buried oxide interface. Later we will show that the influence of charges at the buried oxide interface is reduced as the silicon layer thickness is increased since most of the carriers are confined near the gate oxide.

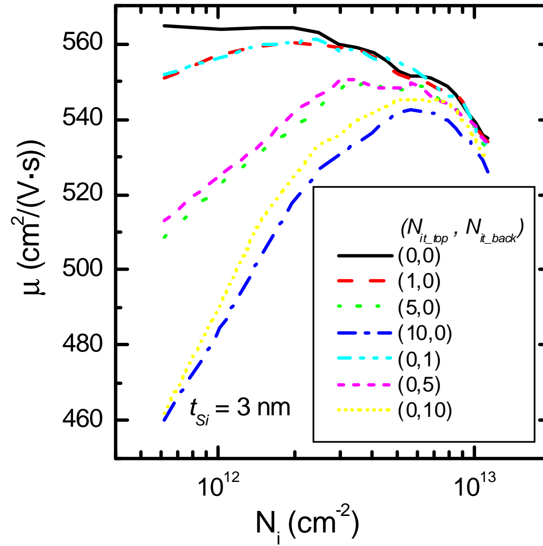


Figure 48. Simulated electron mobility curves in UTB-SOI MOSFETs with 3 nm of silicon layer thickness (T_{Si}) versus inversion electron bi-dimensional density. Interface-roughness scattering has not been taken into account. The quantity of interfacial charges has been given as a pair of numbers, where the first is the bi-dimensional density of charged centers at the gate insulator-silicon interface (expressed in 10^{10} cm^{-2}) while the second is the same but at the buried oxide interface.

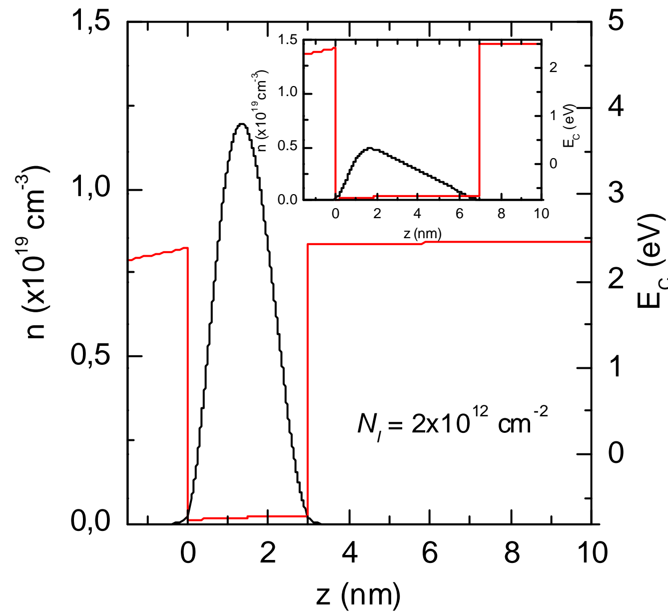


Figure 49. Inversion electron density and conduction band edge as functions of the position along the z-axis (perpendicular to the interfaces). The silicon layer thickness is 3 nm. In the inset, the same quantities are shown for a silicon layer thickness of 7 nm. The inversion bi-dimensional density is 2 x 10^{12} cm^{-2} in both cases. Note that the data range on the left axis is the same for both graphs.

In order to gain a more in-depth knowledge of the role of the charges at each interface, we are going to use Matthiessen's rule (MR). First, we consider it necessary to comment on some issues regarding its application. Matthiessen´s rule has been shown to be inaccurate in certain

cases [Stern-1980, Fischetti-2002, Driussi-2009, Esseni-2011]. The correct application of this rule requires the observance of two conditions, which are unsatisfied in some of the studies presented in the literature. Firstly, the different scattering mechanisms should have the same energy dependence, and secondly, only one sub-band should be populated [Stern-1980, Fischetti-2002, Driussi-2009]. In strained-silicon devices, the valley splitting contributes to enhancing the population of the fundamental band [Fischetti-2002, Driussi-2009, Weber-2008, Esseni-2011], allowing the second condition to be satisfied in most cases. In this way, the error due to the application of MR is minimized [Weber-2008]. The population enhancement of the fundamental sub-band is also obtained in ultra-thin body SOI MOSFETs due to a strong geometrical confinement. However, even in this case, characterized by the prevalence of the fundamental sub-band, the application of MR could produce an underestimate of the Coulomb mobility, as pointed out in reference [Driussi-2009]. Furthermore, the error depends on the mobility curve taken as reference (that is, the phonon-limited mobility) [Driussi-2009, Esseni-2011].

Taking these considerations into account, we assume that the extracted Coulomb mobility data shown in this section might be underestimated. However, the error should be smaller than in bulk devices because of the greater sub-band separation (especially for the thinnest transistors included in our study). Furthermore, for devices with the same silicon layer thickness, the reference mobility curve is the same for all the extracted Coulomb mobility curves, consequently, the error should be approximately the same and, therefore, we can confidently use the Coulomb mobility obtained to compare the influence of Coulomb scattering centers at the different oxide-semiconductor interfaces.

In this respect, although the extracted Coulomb mobility might differ from the exact Coulomb mobility, the use of MR allows us to model the influence of charges placed at the two interfaces. As will be shown below, we can easily obtain the total Coulomb mobility by adding the Coulomb mobility due to the contribution of each interface separately. Taking into account that only the total mobility (including all the main scattering mechanisms) of the devices matters, for both device and circuit modeling, the errors that might be introduced by MR would be compensated for by using the rule again to add up the contributions of the different scattering mechanisms in order to obtain the total device mobility. This is an important issue to highlight since the phonon plus surface-roughness mobility components follow a well-known universal behavior that simplifies the modeling of this essential transport parameter [Takagi-1994]. The advantage of using this approach is that in addition to the ease (mentioned above) of adding up the Coulomb mobility curves due to charges placed at the

different interfaces, it would allow the simplicity inherent in the universal behavior of the phonon and surface roughness mobility components to be maintained. In connection with latter explanation, it is important to highlight that for the determination of the surface-roughness mobility component by means of MR an error lower than 15% is expected for a wide range of inversion charges [Esseni-2011].

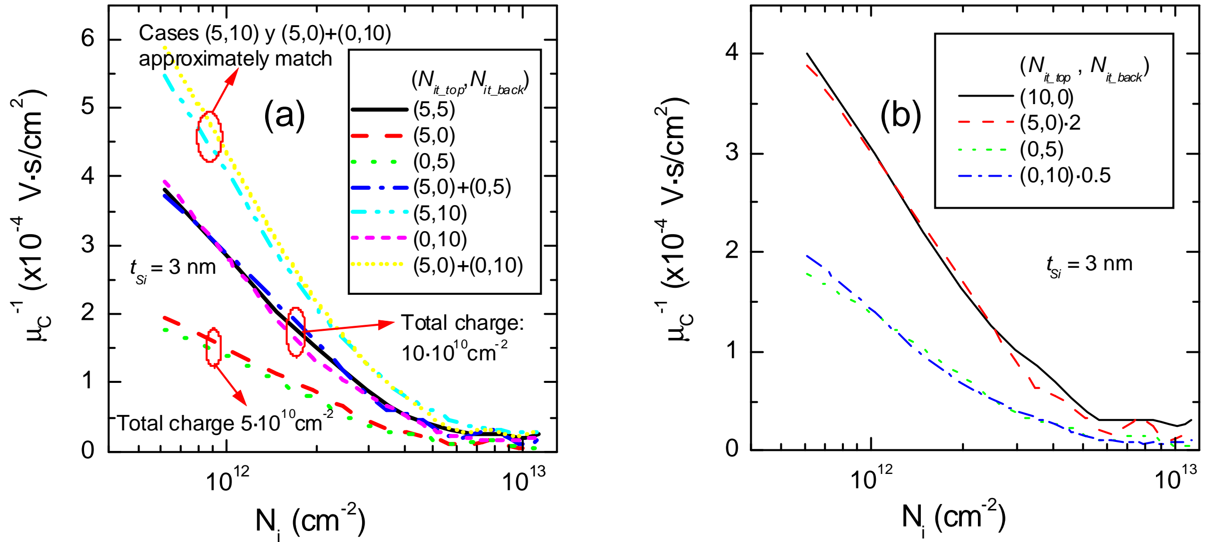


Figure 50. Inverse of Coulomb-limited mobility extracted by Matthiessen's rule. As in figure 47, the bi-dimensional charged center density at the interfaces is expressed as a pair of numbers with a scale of 10^{10} cm^{-2}. (a) The dark blue (__ _ __) curve has been calculated by adding the curves of cases (5,0) and (0,5). In the same way, the yellow curve (....) is obtained by adding the curves of cases (5,0) and (0,10). (b) The red curve (__ __) has been obtained by multiplying curve (5,0) (not shown) by two. Finally, the dark blue (___ __) curve has been calculated by dividing curve (0,10) by two.

Figure 50 shows the inverse of the Coulomb-limited mobility (μ_C) extracted by MR (equation 22):

$$\frac{1}{\mu_C} = \frac{1}{\mu_T} - \frac{1}{\mu_{ph}} \tag{22}$$

where μ_{ph} is the mobility obtained without including Coulomb scattering (phonon-limited mobility) and μ_T is the total mobility that includes both phonon and Coulomb scattering mechanisms. The following results have been obtained from figure 50:

As expected from figure 48, figure 50a shows that the Coulomb-limited mobility curve for the case with an interfacial density of 5 x 10^{10} cm^{-2} at the gate oxide interface ((5,0)) matches the curve with the same charge density at the buried oxide interface ((0,5)).
Furthermore, in figure 50a, curves corresponding to devices with charges at both interfaces are also shown. As can be seen, curves with similar total bi-dimensional oxide charged center densities of 10 x 10^{10} cm^{-2} also match (that is, cases (5,5) and (0,10)).
Moreover, figure 50a shows that the inverse of the Coulomb-limited mobility curve of a device with interfacial densities of 5 x 10^{10} cm^{-2} at both interfaces (case (5,5)) can be approximately reproduced by adding the curve obtained for the case with 5 x 10^{10} cm^{-2} of interfacial charge density at the gate oxide (curve (5,0)) and the curve corresponding to a device with 5 x 10^{10} cm^{-2} of interfacial charge density at the buried oxide (curve (0,5)). The result of the addition of these curves is labeled (5,0)+(0,5). Similarly, curve (5,0)+(0,10) is the addition of curves (5,0) and (0,10) and, as can be seen, closely matches curve (5,10). Therefore, the inverse of Coulomb-limited mobility due to charges sited at both interfaces (μ_C) can be calculated by adding the inverse of mobility curves corresponding to the separate contribution of each interface. That is:

$$\frac{1}{\mu_C} \approx \frac{1}{\mu_{C_top}} + \frac{1}{\mu_{C_back}} \qquad (23)$$

where μ_{C_top} is the Coulomb-limited mobility for a device with the buried oxide interface free of charges and μ_{C_back} is the Coulomb-limited mobility calculated without including charges at the top gate oxide interface. This result is important because (in the line of reasoning described at the beginning of this section) it makes the development of a Coulomb mobility model easier, taking into account the decoupling of the influence of interface charges at the gate and buried oxides.
Indeed, as far as modeling is concerned, figure 50b shows another important result. The inverse of Coulomb-limited mobility for the case (10,0) approximately matches the curve of the case (5,0) multiplied by two. That is, if the charge density at the top interface is doubled, the inverse of Coulomb mobility is also multiplied by the same factor. The same result is obtained for charges at the buried interface: the curve corresponding to case (0,5) can be obtained by dividing the data corresponding to curve (0,10) by two. Therefore, we can conclude that Coulomb-limited mobility (μ_{C_Nit1}) due to a given quantity of charges at one

interface (N_{it1}) can be approximately calculated from the Coulomb-limited mobility (μ_{C_Nit2}) due to another quantity of charges (N_{it2}) placed at the same interface by means of the following expression:

$$\frac{1}{\mu_{C_Nit1}} \approx \frac{1}{\mu_{C_Nit2}} \cdot \frac{N_{it1}}{N_{it2}} \tag{24}$$

We have also considered the case of thicker silicon layers in order to see if the important results obtained for ultrathin silicon layers are maintained as the silicon thickness increases.

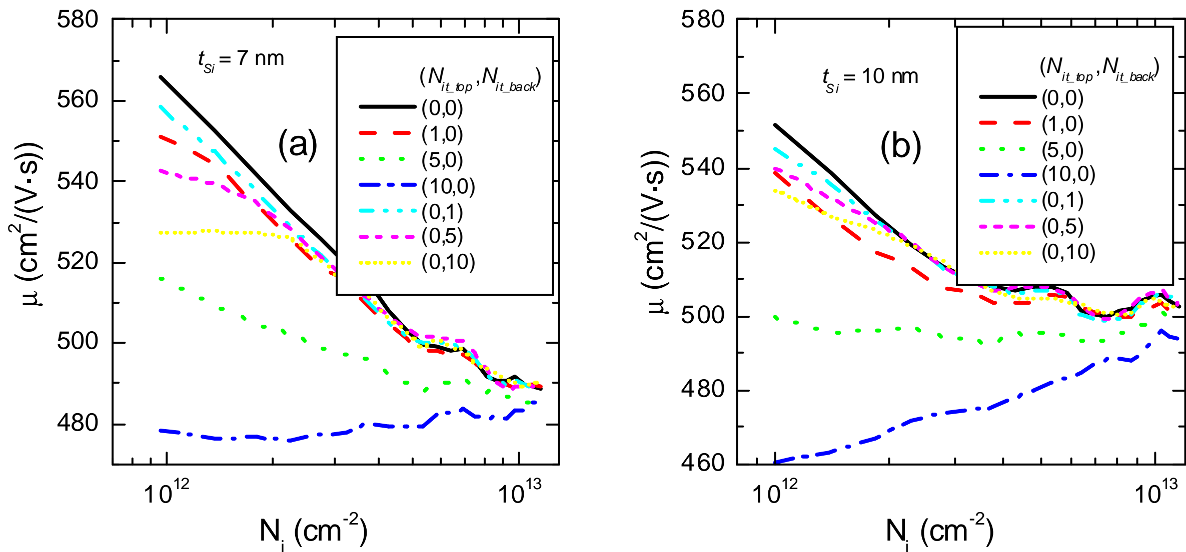


Figure 51. Mobility curves for a silicon layer thickness of (a) T_{Si} = 7nm and (b) T_{Si} = 10nm. As in figure 46, interface-roughness scattering has not been taken into account.

Figure 51 shows total mobility curves for a device with silicon layers of (a) T_{Si} = 7nm and (b) T_{Si} = 10 nm. As can be seen, in these cases the position of the Coulomb scattering centers (at the gate or at the buried oxide interfaces) is not irrelevant because the inversion electron centroid is closer to the gate oxide interface than to the buried oxide interface (see the inset of figure 49). As a consequence, mobility curves (a,0) and (0,a) do not match as in a structure with T_{Si} = 3 nm, and the difference becomes greater as the silicon layer thickness increases. Furthermore, we might expect that the influence of charges placed at the buried oxide interface vanishes when the silicon layer is thick enough. In this respect, it is important to highlight the fact that the mobility reduction due to a charged center density of 10 x 10^{10} cm^{-2}

at the buried oxide interface is significant for T_{Si} = 7 nm (figure 51a) but much less so for T_{Si}=10 nm (figure 51b).

The inverse of Coulomb mobility for these structures (T_{Si} = 7 nm and T_{Si} = 10 nm) is shown in figure 52 for several interfacial charge densities.

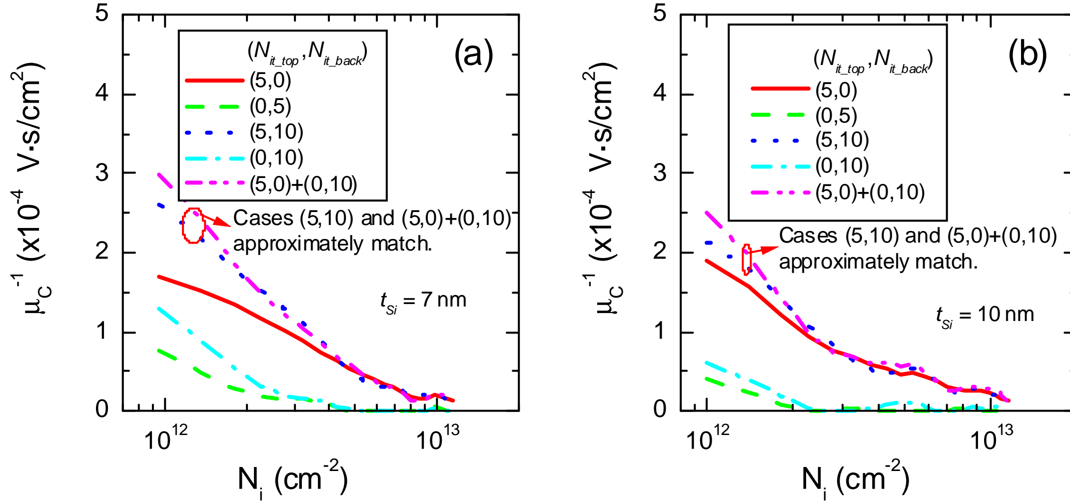


Figure 52. Inverse of Coulomb-limited mobility extracted by Matthiessen's rule for (a) T_{Si} = 7 nm and (b) T_{Si} = 10 nm. The same notation has been used as in Figure 48.

The following results were obtained in these cases:

Curves (5,0) and (0,5) do not match. As mentioned above, as the silicon thickness increases, the role played by the charges placed at the buried interface decreases: the inversion charge remains near the top interface, thus increasing the distance between the electrons and the charges at the buried interface. The Coulomb-limited mobility in the (0,5) case is higher than in the (5,0) case. In general, this result would be valid independently of the value of the interface charge.

However, if we consider the inverse of the Coulomb-limited mobility curves for the (5,0), (0,10) and (5,10) cases, it is interesting to highlight that the latter could be obtained as the sum of the two former, or in other words, because charges are placed at both interfaces, Coulomb-limited mobility can be calculated as the superposition of the separate effects of each one, i.e., equation 23 also holds for thicker samples.

Finally, we have verified that equation 24 also holds for thicker silicon films, both for the charges at the buried interface and for those at the top interface.

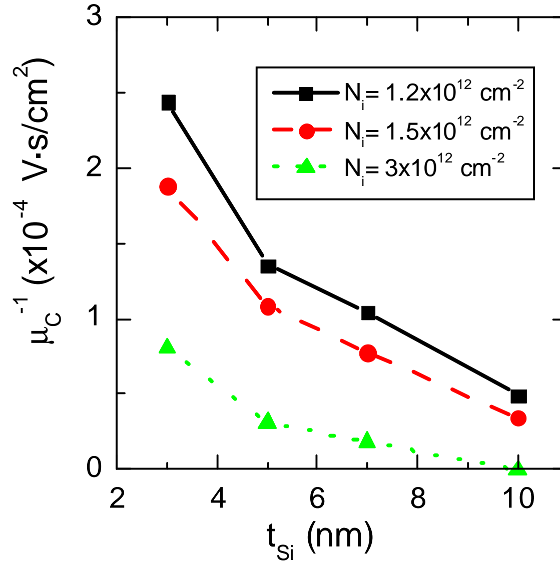


Figure 53. Coulomb mobility inverse versus T_{Si} for a superficial density of charged centers of $10x10^{10}$ cm^{-2} at the buried oxide interface, for three values of the inversion electron bi-dimensional density.

The importance of these results lies in the fact that the last two properties facilitate the development of a Coulomb mobility model that isolates the influence of the two interfaces. In order to investigate this issue more deeply, we have studied the dependence of Coulomb-limited mobility on the silicon layer thickness:

Figure 53 shows the evolution of the Coulomb-limited mobility due to an interfacial density of charged centers of $10x10^{10}$ cm^{-2} at the buried oxide interface as a function of the silicon layer thickness. As expected, the Coulomb mobility shows a strong dependence on T_{Si}, and it can also be seen that the inverse of the Coulomb-limited mobility monotonically decreases as the silicon thickness increases.

However, the influence of T_{Si} is weaker if we consider the Coulomb-limited mobility due to charges placed at the top oxide interface. In figure 54, the Coulomb mobility inverse versus T_{Si} is shown for a density of charged centers of (a) 10×10^{10} cm^{-2} and (b) 5×10^{10} cm^{-2} at the gate oxide interface. The curves are much flatter than those in figure 53 and a monotonic trend of Coulomb mobility versus T_{Si} is not observed.

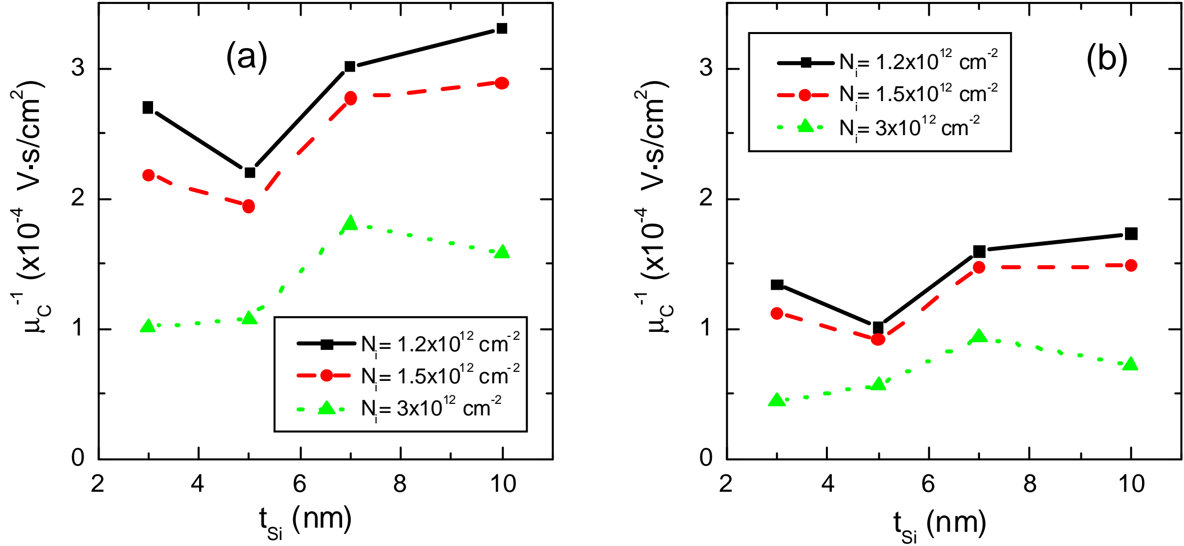


Figure 54. Coulomb mobility inverse versus T_{Si} for a superficial density of charged centers of (a) $10x10^{10}$ cm^{-2} and (b) $5x10^{10}$ cm^{-2} at the gate oxide interface, for three values of the inversion electron bi-dimensional density.

The last effect is due to the superposition of various phenomena with different dependencies on the silicon layer thickness:

i. The non-perturbed inversion charge distribution is modified by the presence of the external charges that cause the Coulomb scattering. The effect of this inversion charge redistribution implies the partial screening of the perturbation charges (see equation 2 in section 2.3.1.2 and later discussion). The screening of Coulomb charged centers by inversion electrons is more effective as the silicon layer thickness shrinks [Gámiz-2002]: the thinner the silicon layer, the greater the confinement of the electrons and the greater the screening (figure 55 shows different electron distributions for several values of the silicon layer thickness).

ii. There is another screening effect exerted on the perturbation charges. This is due to the polarization of the material as a response to these charges. As is known, the strength of this polarization is given by the permittivity of the material: the higher the permittivity, the stronger the polarization inside the material in the presence of charges, and, therefore, the lower the perturbation potential produced by the charges. The reduction of the silicon layer thickness can be seen as the substitution of a slide of silicon by a material (silicon dioxide) with a lower permittivity, which produces a less effective screening of the Coulomb centers [Jiménez-Molinos-2008] by the polarization of the materials which compose the device structure.

iii. As shown in figure 55, the confinement of the electrons becomes stronger as the silicon layer is made thinner. This reduces the distance of the inversion charge centroid from the

charged centers that cause Coulomb scattering (placed at the top oxide interface). For total inversion electron density of 10^{12} cm^{-2}, figure 55a shows that the peak of the inversion electron distribution approaches the top oxide interface as the silicon layer is thinned (especially when T_{Si} is reduced from 5 nm to 3 nm). On the other hand, for an electron density of 3 x 10^{12} cm^{-2} (figure 55b), although a more confined electron distribution is obviously obtained for the thinner silicon layers, the peaks of the distributions remain in almost the same positions for the four different silicon thicknesses considered.

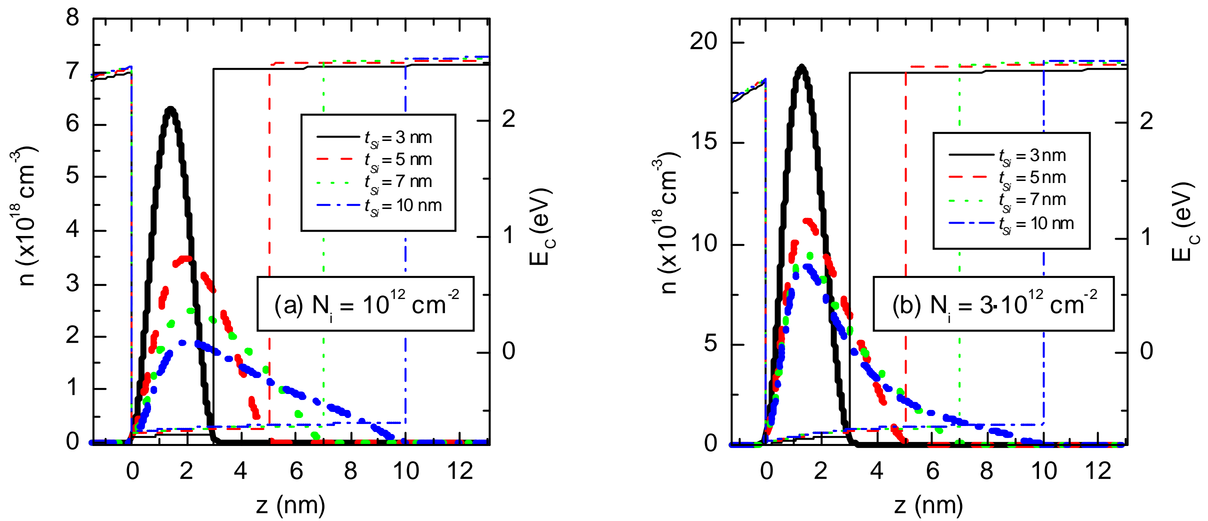


Figure 55. Inversion electron density and conduction band bottom edge as function of the position along the z-axis (perpendicular to the oxide interfaces) for several silicon layer thicknesses. These quantities are shown for two different values of the total inversion charge: (a) $N_I = 10^{12}$ cm^{-2} and (b) $N_I = 3 \times 10^{12}$ cm^{-2}.

As can be seen, as far as Coulomb scattering produced by the top interface charges is concerned, we have a complex scenario in which there are multiple effects with different dependencies on the silicon layer thickness and on the inversion electron density. In order to analyze the influence on the curves shown in figure 54, the following facts should be taken into account. Effect i. reduces the Coulomb scattering when the silicon slab is thinned (the Coulomb mobility increases), while effects ii. and iii. enhance Coulomb scattering. It is important to highlight that the influence of the effect i. (the screening by the mobile inversion electrons) is less noticeable at high inversion electron densities because of the more important role played by the electric field confinement. Therefore, for the sake of clarity, we are going to analyze separately the two curves corresponding to the lower inversion densities (1.2 x 10^{12} cm^{-2} and 1.5 x 10^{12} cm^{-2}) and the curve for the highest value considered (N_I = 3 x 10^{12} cm^{-2}) in figure 54.

For the curves linked to the two lowest inversion densities, a decrease of the Coulomb scattering probabilities (an increase of Coulomb mobility) can be observed when the silicon layer thickness is reduced from 10 nm to 5 nm. This fact is connected to effect i (a more effective screening by the inversion electrons); in this case the width of the silicon layer is still great enough to make effects ii. and iii. less influential than effect i. However, when T_{Si} is reduced from 5 nm to 3 nm, the scattering probability increases (the mobility decreases) because of the greater influence of effects ii and iii. In fact, for a total inversion electron density of 10^{12} cm^{-2} figure 55a shows that the peak of the inversion electron distribution approaches the top oxide interface as the silicon layer is thinned (especially when T_{Si} is reduced from 5 nm to 3 nm). This is why Coulomb mobility is reduced (see figure 54) for the two lowest inversion electron densities when T_{Si} is reduced from 5 nm to 3 nm.

In relation to the behavior of the curve for the highest inversion density, the peaks of the inversion charge distributions (figure 55b) remain in almost the same positions for the four different silicon thicknesses considered (in this case, the confinement due to the electric field is more than the structural confinement linked to the silicon layer thickness [Balaguer-2011b]). This explains why Coulomb mobility remains almost constant when T_{Si} is reduced from 5 nm to 3 nm for the case corresponding to an inversion electron density of $N_I = 3 \times 10^{12}$ cm^{-2} [Jiménez-Molinos-2010a].

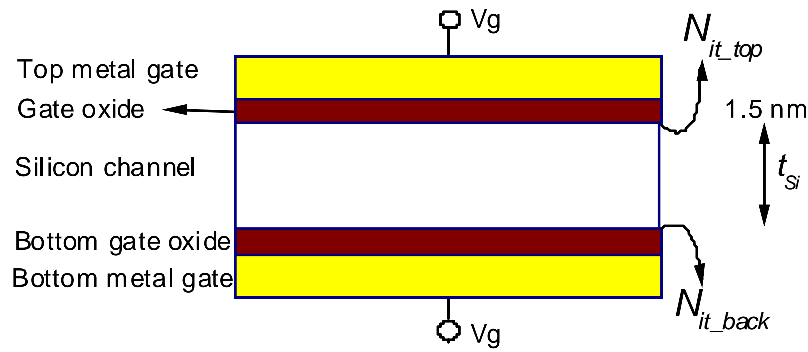
To sumarize this part of the section devoted to the mobility analysis of SGMOSFETs, we would like to state that for the thinnest structure (T_{Si} = 3 nm), the influence of charges sited at the buried oxide interface on the mobility is almost the same as that of charges at the gate oxide interface. The mobility is limited by the total interfacial charge, no matter where it is placed. However, as the silicon layer is made thicker, the buried interface is found further from the inversion charge and the influence on the low-field mobility of the charges at this interface is consequently reduced. Moreover, we have shown that the inverse of the total Coulomb-limited mobility (due to charges at both interfaces) can be approximately calculated as the addition of the inverse of the Coulomb-limited mobility due to charges at the gate oxide interface and the inverse of the Coulomb-limited mobility due to charges at the buried oxide interface. This fact is significant because it allows us to study independently the effect on mobility of the charges sited at each interface. Furthermore, for charges placed at the same interface, we have shown that the Coulomb mobility due to a given density of interfacial charges can be calculated using the Coulomb mobility data due to another interfacial charge density, considering only the ratio between the two interfacial charge densities. We have also shown that the Coulomb-limited mobility due to charges at the buried interface is an

increasing monotonic function of the silicon layer thickness and that the influence of the charges at the buried interface is greatly reduced for silicon thicknesses greater than 10 nm. However, the Coulomb-limited mobility due to the charges trapped at the top Si/SiO_2 interface has a weaker dependence on the silicon thickness and is not monotonic. This is because Coulomb scattering rates are influenced by several phenomena: confinement of the inversion electrons, screening by the inversion charge and screening by the polarization of the materials that surround the Coulomb centers and is represented by their permittivities. These effects show different dependencies on the silicon layer thickness and this fact causes the non-monotonic trend obtained. All these mechanisms also affect Coulomb-limited mobility due to the interface charges at the buried interface but in this case, the most important factor to take into account is the distance between the interfacial charges and the inversion electrons. The use of Matthiessen's rule is justified since it eases the addition of Coulomb mobility curves due to charges placed at the different interfaces and allows the simplicity inherent in the universal behavior of the phonon and surface-roughness mobility components to be maintained.

b) DGMOSFET study

In the second part of this section we will deal with a mobility study similar to the one presented above but devoted to DGMOSFETs. In this particular case, due to the focus of this chapter on DGMOSFETs, in addition to the characterization of Coulomb mobility we will also include the analysis on the surface-roughness mobility component.

To analyze the influence of the different scattering mechanisms on the low-field mobility in DGMOSFETs, we have carried out a large number of simulations for structures with different oxide interface characteristics in terms of surface-roughness and density of interfacial charged centers. Simulation data have been obtained by means of the simulator presented in section 2.3.1.2 of this work. Figure 56 shows a schematic representation of the device under study. It consists on a symmetrical structure similar to figure 12 with two mid-gap metal gates and a 1.5 nm layer of silicon dioxide as gate insulator. The silicon channel is intentionally kept undoped and several silicon thickness (T_{Si}) values are considered.



$$(a,b) \rightarrow \begin{cases} N_{it_top} = a \times 10^{10} \text{ cm}^{-2} \\ N_{it_back} = b \times 10^{10} \text{ cm}^{-2} \end{cases}$$

Figure 56. Schematics of the symmetrical DGMOSFETs considered in this study, and nomenclature for describing the interface charge at the oxide interfaces.

The nomenclature that will be used to describe the interface charge at the oxide interfaces, when dealing with Coulomb scattering, is also given in Figure 56. Figure 57 shows the mobility curves (including all the main scattering mechanisms: phonon, Coulomb and surface-roughness mechanisms) for two DGMOSFETs with different silicon layer thicknesses. Several combinations of densities of interfacial charged centers have been considered at both interfaces. The mobility is, in general, lower in the thinner devices, as expected, since phonon scattering mechanisms are higher (the confinement of the inversion charge is greater [Gámiz-1998b]), and surface-roughness and Coulomb scattering mechanisms are also higher due to the proximity of the inversion charge and the oxide interfaces. In the following part of the section, we are going to analyze the influence of these scattering mechanisms on the total mobility in order to establish a basis for the development of new mobility models and the characterization of the silicon-insulator interfaces quality as we have done previously for single gated devices.

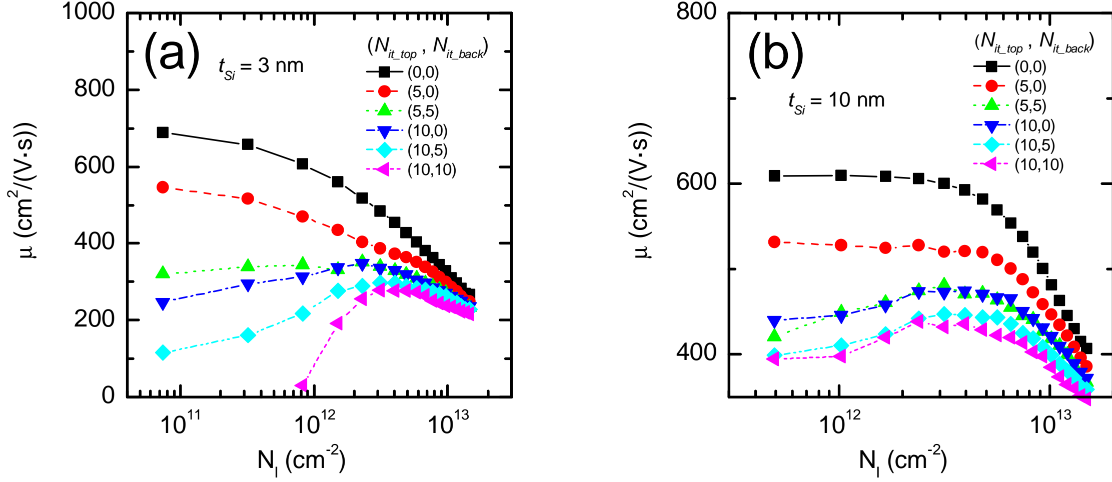


Figure 57. Simulated electron mobility curves versus inversion electron bi-dimensional density in DGMOSFETs with (a) T_{Si} = 3nm and (b) T_{Si} =10nm at room temperature. Coulomb, phonon and surface-roughness scattering mechanisms have been taken into account. The parameters used for the surface-roughness scattering were L = 1.5 nm and Δ = 0.4 nm [Gámiz-2001]. The amount of interfacial charges has been described as a pair of numbers (see Figure 56).

a.- Coulomb limited mobility

As pointed out before, figure 57 shows the mobility obtained for several configurations varying the interface charge distribution at the oxide interfaces while the other scattering mechanisms were kept unchanged. The following fact can be highlighted: the mobility curves for (5, 5) and (10, 0) are very similar. This fact suggests that it is not the distribution of charge but the amount of charge the main variable to take into account in these particular structures (this is observable in the two silicon layer thicknesses considered here, 3 and 10 nm). This phenomenon was already observed in our previous study focused on single gate MOSFET as was presented in figure 52. In order to clarify the latter idea and try to get a better understanding of the role played by the interfacial charges on the mobility, we have isolated the contribution of Coulomb scattering by obtaining the Coulomb-limited mobility (μ_C) making use of Matthiessen's rule as follows,

$$\frac{1}{\mu_C} = \frac{1}{\mu_T} - \frac{1}{\mu_{ph+sr}} \tag{25}$$

where μ_{ph+sr} is the mobility obtained without including Coulomb scattering (phonon and surface-roughness scattering is included) and μ_T is the total mobility that includes all the scattering mechanisms.

Most of the comments highlighted at the beginning of this section in relation to the appropriateness of the application of Matthiessen´s rule also hold for DGMOSFETs [Stern-1980, Fischetti-2002, Driussi-2009, Esseni-2011]. In fact, DGMOSFETs are supposed to have thinner silicon layers than SG devices, and in this respect the condition connected with the population enhancement of the fundamental sub-band is achieved to a greater extent. Therefore the errors in the determination Coulomb mobility component should be lower. All the other considerations, including the surface-roughness mobility component extraction can be also applied in this sub-section.

The following results have been obtained.

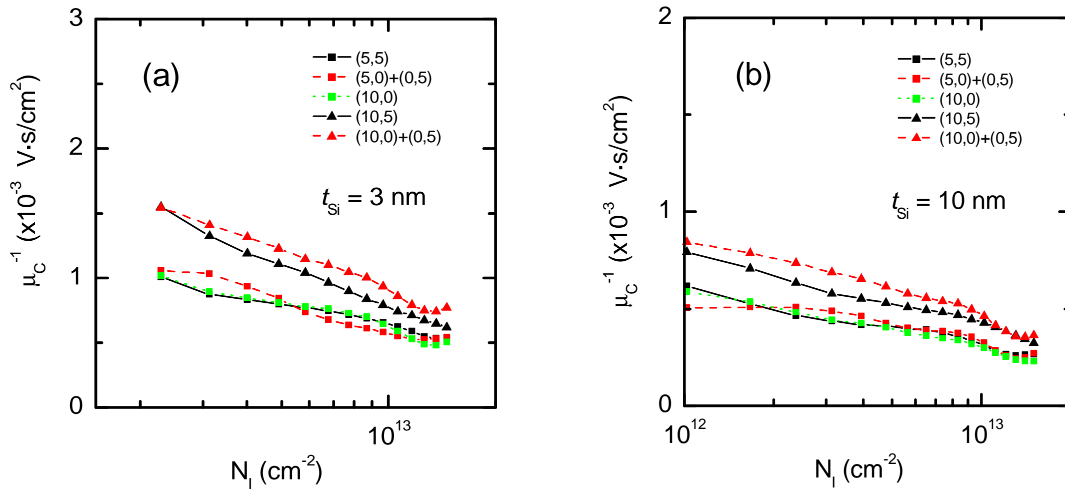


Figure 58. Inverse of Coulomb-limited mobility extracted by Matthiessen's rule for DGMOSFETs with (a) T_{Si} = 3nm and (b) T_{Si}=10nm at room temperature. The amount of interfacial charges has been described as a pair of numbers (see Figure 56).

The following facts can be obtained from Figure 58 (keeping in mind that the devices under study are symmetrical). On the one hand, and independently of the silicon layer thickness, the Coulomb-limited mobility curve for the case with an interfacial density of 5x10^{10} cm^{-2} at each gate oxide interface (5,5) matches approximately the curve with the same charge density but just at one of the oxide interfaces (10,0). On the other hand, the inverse of the Coulomb-limited mobility curve of a device with interfacial densities of 5x10^{10} cm^{-2} at both interfaces (curve labeled with (5,5)) can be approximately reproduced by adding the curve obtained for the case with 5x10^{10} cm^{-2} of interfacial charge density at the top gate oxide (curve (5,0)) and the curve corresponding to a device with 5x10^{10} cm^{-2} of interfacial charge density at the buried oxide (curve (0,5)). The result of the addition of these curves is labeled (5,0)+(0,5),

and its performed as indicated in equation 23. Similarly, curve (5,0)+(0,10) is the addition of curves (5,0) and (0,10) and, as can be seen, closely matches curve (5,10). Therefore, the inverse of Coulomb-limited mobility due to charges sited at both interfaces (μ_C) can be calculated by adding the inverse of mobility curves corresponding to the separate contribution of each interface. (as in the previous case, that means that μ_{C_top} is the Coulomb-limited mobility for a device with the buried oxide interface free of charges and μ_{C_back} is the Coulomb-limited mobility calculated without including charges at the top oxide interface). This result is important because it makes the development of a Coulomb mobility model easier, taking into account the decoupling of the influence of interface charges at the top and buried oxides. We would like to remark that this result, already pointed out for single gate devices presented at the beginning of this section, also holds true for double gate devices.

b.- Surface-roughness limited mobility

We have also dealt with the characterization of surface-roughness scattering in DGMOSFETs. In this respect, we have used a nomenclature similar to the one described above for the charge at the oxide interfaces. From now on, (a, b) will represent (Δ_{sr_top}, Δ_{sr_back}), where Δ values represent the abrupt variations of the oxide-semiconductor surface (in nm); for both interfaces L = 1.5 nm, according to the model described in [Gámiz-2001].
We isolated the contribution of surface-roughness scattering by obtaining the surface-roughness limited mobility (μ_{sr}) making use of Matthiessen's rule as follows,

$$\frac{1}{\mu_{sr}} = \frac{1}{\mu_T} - \frac{1}{\mu_{ph+C}} \tag{26}$$

where μ_{ph+C} is the mobility obtained including only phonon and Coulomb scattering and μ_T is the total mobility that includes all the scattering mechanisms.
The surface-roughness limited mobility has been obtained for two DGMOSFETs with different silicon layer thicknesses with different Δ parameters in the silicon-oxide.

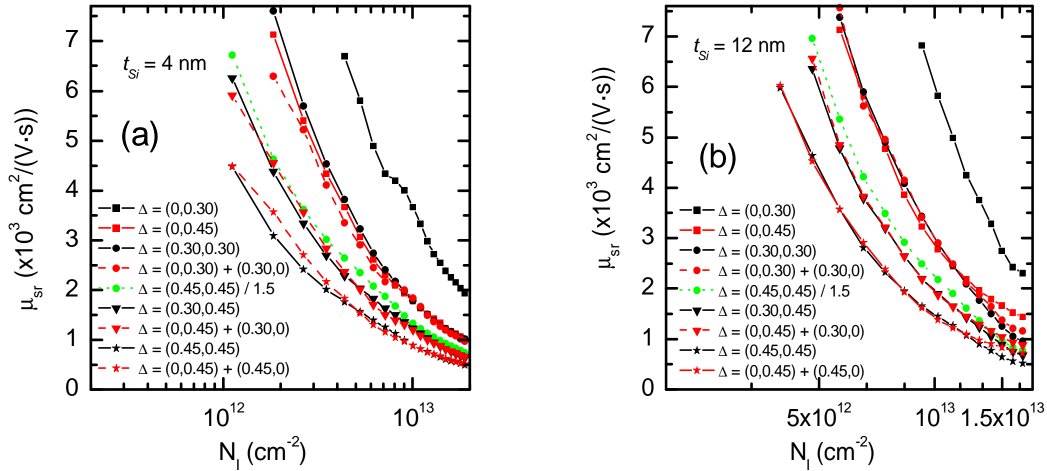


Figure 59. Surface-roughness limited mobility inverse extracted by Matthiessen's rule versus inversion electron bi-dimensional density for DGMOSFETs with (a) T_{Si} = 3nm and (b) T_{Si} =10nm at room temperature. The value of the parameters for the surface-roughness scattering model were L = 1.5nm, and Δ is given as a pair of numbers (in nanometers) where the first (second) corresponds the top (back) oxide interface.

A similar behavior, in comparison to the Coulomb-limited mobility, is observed here. As can be seen, (0.30, 0.30) can be reproduced by means of (0.30, 0)+(0, 0.30). The same happens for (0.30, 0.45) and (0, 0.45)+(0.30, 0). This means that the inverse of surface-roughness limited mobility due to roughness at both oxide interfaces (μ_{sr}) can be calculated by adding the inverse of mobility curves corresponding to the separate contribution of each interface. That is:

$$\frac{1}{\mu_{sr}} \approx \frac{1}{\mu_{sr_top}} + \frac{1}{\mu_{sr_back}} \tag{27}$$

where μ_{sr_top} is the surface-roughness limited mobility for a device with an ideal buried oxide interface and μ_{sr_back} is the surface-roughness limited mobility calculated without roughness at the top oxide interface.

Finally, we should clarify some aspects about the curve labeled as (0.45, 0.45)/1.5. The surface-roughness limited mobility corresponding to this curve has been obtained from the (0.45, 0.45) curve, multiplying point to point the mobility by 1.5. If there were an inverse linear dependence between mobility and Δ parameter, curve (0.45, 0.45)/1.5 would fit the (0.30, 0.30) curve. However, curve (0.45, 0.45) /1.5 can be found below curve (0.30, 0.30), therefore, this linear dependency does not exist. Surface-roughness scattering increases with Δ

in a much faster way than if it depended linearly on Δ. This can also be seen in the fact that curve (0, 0.45) is very close to curve (0.30, 0.30).

In the following figure the surface-roughness limited mobility for DGMOSFETs with different T_{Si} ($\mu_{sr}(T_{Si})$) divided by the curve corresponding to T_{Si} = 20 nm (μ_{sr} (T_{Si} = 20nm)) is plotted versus inversion charge.

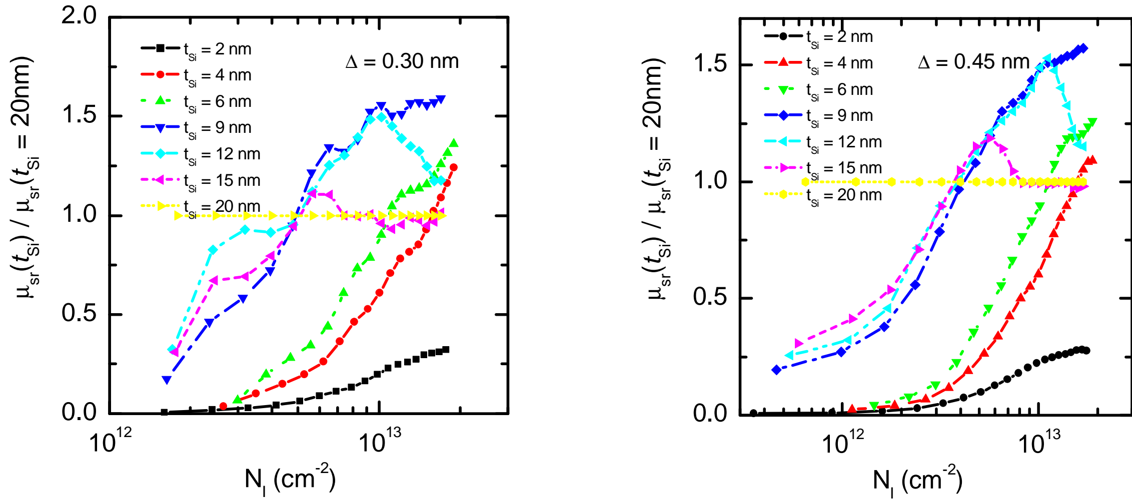


Figure 60. Surface-roughness limited mobility divided by the surface-roughness mobility corresponding to T_{Si} = 20nm versus inversion electron bi-dimensional density for DGMOSFETs for several silicon layer thicknesses at room temperature. The surface-roughness parameters were L=15nm, (a) Δ=0.3nm and (b) Δ=0.45nm.

As can be seen in the figure above, at low inversion charge the curves do not merge and they are always below one (the surface-roughness mobility for 20 nm is taken as reference). However, at high inversion charge the curves corresponding to the thickest silicon layers tend to converge. In fact, taking into account the graphs in figure 60, we can distinguish two different behaviors. For thin silicon slabs, the curves increase monotonously with the inversion charge. For thick devices, the curves at low inversion charge show the same monotonous behaviour, but tend to unity for high inversion charge. This twofold behavior can be explained easily: for low inversion charge the carriers are distributed throughout the channel (volume inversion) for all the devices, and the structural confinement predominates over electric confinement, see the figure below and the first section of this chapter [Balaguer-2011b]. As a consequence, the thinner the silicon slab, the closer the inversion charge is to the silicon-dielectric interfaces. Therefore, for low inversion charge, a similar behavior is shown no matter the silicon thickness, although the surface-roughness mobility is lower for the

thinner samples. For high inversion charge, the electric confinement predominates over the structural confinement for the thicker silicon films (see figure 61b) and two inversion channels appear [Balaguer-2011b]. As a consequence, the thickness of the silicon layer does not affect the surface-roughness mobility and the curves tend to merge. However, for the thinnest silicon slabs, the volume inversion operation regime remains even at high inversion charges (see figure 61a) and the structural confinement still predominates over electric confinement. A boundary between these two different confinement conditions (in terms of the surface-roughness mobility component) could be established for a silicon layer thickness around 9 nm, since the corresponding mobility curve show an intermediate trend.

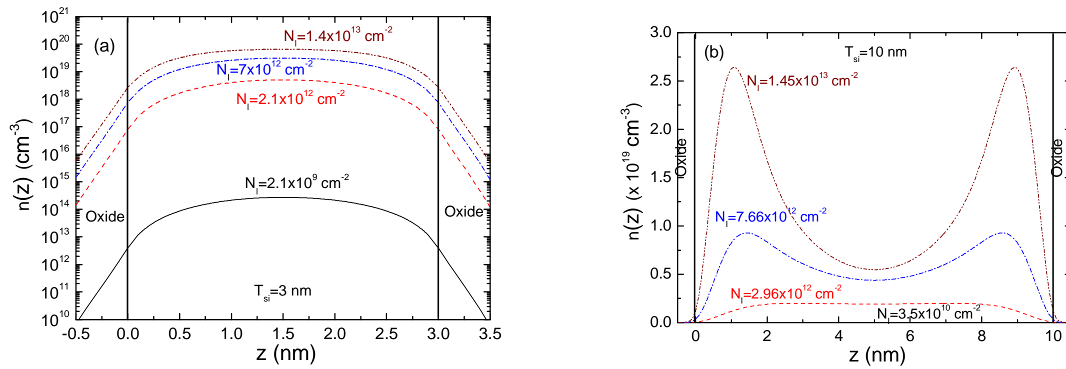


Figure 61. Electron density as a function of the position along the z-axis (perpendicular to the silicon-oxide interface) for an undopped DGMOSFETs grown on a (100) substrate for different inversion charges. (a) T_{Si} = 3 nm, (b) T_{Si} =10 nm.

To conclude this section dedicated to mobility characterization in DGMOSFETs, we would like to highlight that regarding Coulomb-limited mobility, we can take into account separately the charge at each oxide interface. That is because the Coulomb-limited mobility due to the charge (at both interfaces) can be approximately calculated by the addition of the contribution of each interface according with the expression of Matthiessen's rule as it was also observed for the single gate case. However, it has been also shown that, in these UTB double-gate structures, it is more relevant the amount of total interfacial charge than how it is distributed between the two interfaces.

For the DGMOSFET devices we have also studied the influence of surface-roughness. As far as this effect is concerned, it has been demonstrated that both interfaces can also be separately modeled. Again, the total surface-roughness-limited mobility of a system with two interfaces can be obtained as the superposition, via Matthiessen's rule, of the mobility determined by each oxide interface. In summary, in terms of interfacial charges and surface-roughness, both

interfaces could be characterized separately and their effect on the mobility could be added afterwards. This is important especially in SOI fabrication processes leading to different quality oxide interfaces. In order to make easy the future development of compact models, the surface-roughness limited mobility curves for several silicon layer thicknesses divided by the mobility curve corresponding to the structure with 20 nm (taken as reference) have been plotted versus the inversion electron bidimensional density. As expected, at low inversion charges, the thinner the silicon film, the lower the surface-roughness-limited mobility. At higher inversion charges, however, the curves corresponding to the thickest silicon films tend to merge because field confinement predominates over the structural confinement, making less influent the value silicon thickness. For the thinnest structures, volume inversion does not disappear even at high inversion charges, and this fact determines the distance between the inversion electrons and the oxide interfaces and, therefore, Coulomb and surface-roughness scattering.

3.7. DGMOSFET current model

The in-depth analysis we have performed for quantum effects, threshold voltage and surface potential on DGMOSFETs led us to a complete inversion charge model for n-type and p-type devices where different crystallographic orientations and geometrical configurations are considered. The model works well for all the interesting operation regimes that are usually found in current integrated circuits. In addition, in the previous section, we established a deep understanding of the low-field mobility by means of an exhaustive analysis of the most important mobility components from the modeling viewpoint. All these results were focused on an obvious objective: the development of a current model where they all could be integrated.

Consequently, the finalization of this chapter will consist on the development of a new current model for DGMOSFETs. We based our model in a previous one [Moldovan-2007a] where quantum (making use of the results of the previous sections), short channel, velocity saturation and velocity overshoot effects were included. In addition, the results connected to the mobility can be used to improve the mobility model selected [Trivedi-2004] accounting for the particular features (interface charge density and roughness) of the oxide interfaces.

The model development has been based on simulation results obtained with a state-of-the-art ensemble Multisubband Monte Carlo simulator developed at the Nanoelectronics Research Group of the University of Granada [Sampedro-2010, Sampedro-2011]. Two DGMOSFET structures were considered with different lengths and with HfO_2 as gate dielectric. These structures were used as template devices within the scope of NANOSIL European project[2].

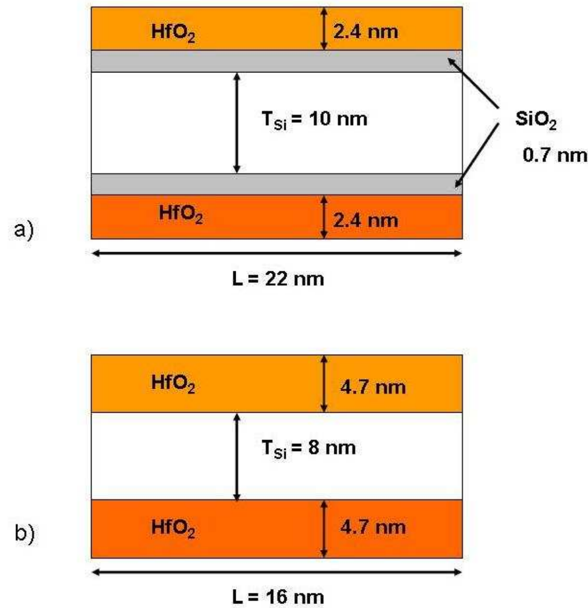


Figure 62. DGMOSFET devices simulated.

The simulated and modeled devices are shown in figure 62. The device in a) is a DGMOSFET with a gate length of 22 nm and a gate stack consisting of 2.4 nm of HfO_2 on top of 0.7 nm of SiO_2 (EOT = 1.1 nm). The channel is lowly doped (10^{15} cm^{-3}) and the silicon film thickness equals 10 nm. The device in b) is also a DGMOSFET with a gate length of 16 nm, a gate stack of 4.7 HfO_2 (EOT = 0.8 nm), also slightly doped (10^{15} cm^{-3}) and with silicon thickness of 8 nm.

We chose as a starting point the current model developed in [Moldovan-2007a].

$$I_{DS} = \frac{W\mu_{eff}}{L}\left[2\frac{kT}{q}(Q_S - Q_D) + \frac{Q_S^2 - Q_D^2}{4C_{ox}} + 8\left(\frac{kT}{q}\right)^2 C_{si}\log\left[\frac{Q_D + 2Q_0}{Q_S + 2Q_0}\right]\right] \quad (28)$$

where $Q_S = Q_S\ (V=0)$ and $Q_D = Q_D\ (V=V_{DS})$ are calculated by means of equation 12, and Q_0 is given in equation 11. The transistor presented in figure 62 a) consists of stack formed by a

[2] "Silicon-based nanostructures and nanodevices for long term nanoelectronics applications", FP7-NOE-216171, of the seventh Framework European programme.

layer of SiO_2 and another layer of HfO_2. C_{ox} is, therefore, calculated using the following expression:

$$C_{ox} = \frac{\varepsilon_{SiO_2}}{EOT} \qquad \text{where} \qquad EOT = T_{SiO_2} + T_{HfO_2}\frac{\varepsilon_{SiO_2}}{\varepsilon_{HfO_2}} \tag{29}$$

where T_{SiO2} and T_{HfO2} stand for the thicknesses of the silicon dioxide and Hafnium dioxide layers respectively.

The gate dielectric of the second transistor simulated (figure 62b) consists of a single layer of HfO_2, therefore, in this case C_{ox} has been calculated taken into account solely the HfO_2 permittivity and layer thickness. We calculated, as explained before, the inversion charge included in the current expression by means of the equation 12 already presented in section 3.5. In this case the C_{ox} has also been modified to take into account QMEs and C_{ox}^{*} has been used instead. The modified oxide capacitance was calculated using equation 15 and the inversion charge centroid was obtained by means of Table 2 for an n-type device with a substrate orientation (100) and equation 9.

The DGMOSFET current model presented in equation 28 does not take into account short channel effects, therefore, we have modified it to include mobility degradation due to velocity saturation produced by high lateral electric fields, channel length modulation and drain-induced barrier lowering (DIBL). As pointed out before, velocity overshoot effects as well as QMEs are also included.

We introduced the DIBL model presented in [Lime-2008] by using the following expression as starting point[3]:

$$\varphi = \phi_c - V_{GS} + \Delta\varphi - \left(1 + \frac{C_{ox}}{2C_{Si}}\left(1 - \frac{1}{n}\right)\right)\left(\frac{Q_S + Q_D}{2}\right)\frac{1}{2C_{ox}} \tag{30}$$

Where $\Delta\varphi$ represents the metal and semiconductor work functions difference, Q_S and Q_D are the charge at the source and drain ends respectively, n is a parameter whose value indicates the potential profile and ϕ_c represents the central potential, and it is calculated as given below,

$$\phi_c = \phi_s + \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\phi_s - V_{GS} + \Delta\varphi}{nT_{ox}}\left(\frac{T_{Si}}{2}\right) \tag{31}$$

[3] φ is a modified electric potencial as defined in [Lime-2008].

The minimum modified electric potential for φ (denoted as φ_{min}) is calculated as follows:

$$\varphi_{\min} = 2\sqrt{\varphi_s \varphi_d}\exp\left(\frac{-L}{2\lambda}\right) \tag{32}$$

Where φ_s and φ_d are values of φ evaluated at the source and drain respectively. λ is a characteristic length that depends on the device structure and stands for,

$$\lambda = \frac{T_{Si}}{2}\sqrt{\frac{1}{2} + \frac{2C_{Si}}{C_{ox}} - \frac{1}{n(n+1)}} \tag{33}$$

We have used n = 2 in the previous equation, which corresponds to the potential profile that is usually taken in weak inversion. As explained in [Lime-2008], φ_{min}, which is equal to zero for long-channel devices, can be considered as the barrier potential drop due to the DIBL effect. To take into account the DIBL effect, this value is introduced into the calculation of the inversion charge Q including quantum effects (equation 12 with the modified C_{ox}^{*}) by replacing V_{GS} with $V_{GS} + \phi_{min}$. However, as already indicated in [Lime-2008] the previous analysis fails in strong inversion, so, to achieve the correct behavior for the DIBL reduction above threshold, this value is multiplied by the fitting parameter F_{DIBL}, shown in the following equation and whose value changes progressively from one to zero when going from weak to strong inversion.

$$F_{DIBL} = \exp\left(-\left(\frac{\frac{Q_S + Q_D}{2}}{2\sigma_{DIBL} C_{ox}\frac{KT}{q}}\right)^{n_{DIBL}}\right) \tag{34}$$

The transition begins when $Q_{ch} = (Q_S + Q_D)/2$ is superior to $2C_{ox}$ (KT/q), which corresponds approximately to the threshold voltage, and can be adjusted with the parameters n_{DIBL} and σ_{DIBL}. n_{DIBL} defines the abruptness, whereas σ_{DIBL} defines the threshold of the transition.

To consider the DIBL effect in the model we have replaced V_{GS} by $V_{GS} + F_{DIBL}\varphi_{min}$ in the final expression of the inversion charge (equation 12 with the modified C_{ox}^{*}. Note that C_{ox}^{*} has to be used also in equations 30, 33 and 34).

To calculate the effective mobility used in the DGMOSETs current expression, we have introduced the model developed by Trivedi et al. [Trivedi-2004] which includes both the phonon and surface-roughness mobility components. Following the developments described

in the previous section, Coulomb mobility could be incorporated by means of Matthiessen's rule. The different oxides interface features (interface charges and roughness) could be taking into account as explained above and finally included in the total mobility equation given below.

$$\mu_{eff} = \frac{U0}{1 + \frac{U0}{\mu_{ph}(bulk)}\left(\frac{\mu_{ph}(bulk)}{\mu_{ph}(T_{Si(eff)})} - 1\right) + \theta\frac{U0}{\mu_{sr}}} \tag{35}$$

Where the effective U0 and θ are the fitting parameters and μ_{eff} stands for the total low-field mobility (μ_{sr} stands for the surface-roughness mobility component), see [Trivedi-2004] for further details.

We have taken into account the saturation velocity and velocity overshoot effects by means of the following expression [Roldán-1997a, Roldán-1998].

$$\mu = \frac{\mu_{eff}}{\left(1 + \delta_0 \frac{\mu_{eff} V_{DS}}{v_{sat} L}\right)} + \frac{\lambda_a}{L} \tag{36}$$

In the previous equation v_{sat} is the electron saturation velocity (we have assumed 10^7 cm/s) and λ_a is the velocity overshoot parameter [Roldán-1997a]. The λ_a value used was 40 x 10^{-5} cm^3/Vs. δ_0 is a parameter employed to improve accuracy if the usual electron velocity model versus the longitudinal electric field [Arora-2007, Roldán-2010] (we assumed $\delta_0 = 1$).

Finally, we introduced in the current model the effect of the channel length modulation through the following expression [Lázaro-2008, Enz-2006, Arora-2007].

$$\Delta L = L_C \operatorname{arcsin} h\left(\frac{V_{DS} - V_{Dsat}}{E_{sat} \lambda_C a}\right) \tag{37}$$

ΔL is the length of the pinch-off region near the drain, and "a" was a fitting parameter whose value is found between 0 and 1, in our case a = 0.34 for L = 16 nm and a = 0.68 for L = 22 nm, as can be seen in table 3. λ_C represents the natural length of the DGMOSFETs calculated using the following expression [Colinge-2004]:

$$\lambda_C = \sqrt{\frac{\varepsilon_{Si} T_{ox} T_{Si}}{2\varepsilon_{ox}}} \tag{38}$$

The saturation voltage V_{DSsat} was obtained as explained in [Roldán-2010], using the current continuity along the channel, i.e., equating the current given in equation 28 with the current in the saturated channel given as:

$$I_{DS} = WQ(V = V_{DSsat})v_{sat} \quad (39)$$

To account for velocity overshoot effects in the previous expression, an extra term is necessary. We have followed the model deduction presented in [Roldán-2010]. Thus, a term proportional to the longitudinal electric field gradient ($E_{long} = -dV(x)/dx$, with x being the coordinate that varies along the source–drain direction, $0 \le x \le L$, and $0 \le V(x) \le V_{DS}$) is added to the saturation velocity. The inclusion of velocity overshoot effects leads to the following equation:

$$I_{DS} = WQ(V = V_{DSsat})\left(v_{sat} + \lambda_a b\frac{V_{DS}}{L^2}\right) \quad (40)$$

where b is a fitting constant. The calculation of V_{DSsat} determines the transition between the linear and saturation regions. When channel length modulation has to be included, the channel length L has to be substituted by $(L - \Delta L)$. In order to avoid having to deal with two different drain current expressions (for the linear and saturation regions) and to make a smooth transition between these regions, a smoothing function was used [Arora-2007, Roldán-2010].

$$V_{DSx} = \left(1 - \frac{\ln\left[1 + e^{A\left(1 - \frac{V_{DS}}{V_{DSsat}}\right)}\right]}{\ln\left[1 + e^{A}\right]}\right) V_{DSsat} \quad (41)$$

Where A is a fitting parameter whose value is 1 for the transistor with L = 16 nm and the value is 4 for the transistor with L = 22 nm.

Taking all these considerations into account, the DGMOSFET current model can be finally written as follows:

$$I_{DS} = \frac{W}{L - \Delta L}\left[\frac{\mu_{eff}}{\left(1 + \delta_0 \frac{\mu_{eff} V_{DSx}}{v_{sat}(L - \Delta L)}\right)} + \frac{\lambda_a}{L - \Delta L}\right]\left[2\frac{kT}{q}(Q_S - Q_D) + \frac{Q_S^2 - Q_D^2}{4C_{ox}} + 8\left(\frac{kT}{q}\right)^2 C_{Si}\log\left[\frac{Q_D + 2Q_o}{Q_S + 2Q_o}\right]\right] \quad (42)$$

Making use of the previous equation we have modeled the data simulated for the two DGMOSFET devices presented in figure 62. The obtained results are depicted in the following figures. The fitting parameters used to fit the simulation data are included in Table 3, at the end of the section.

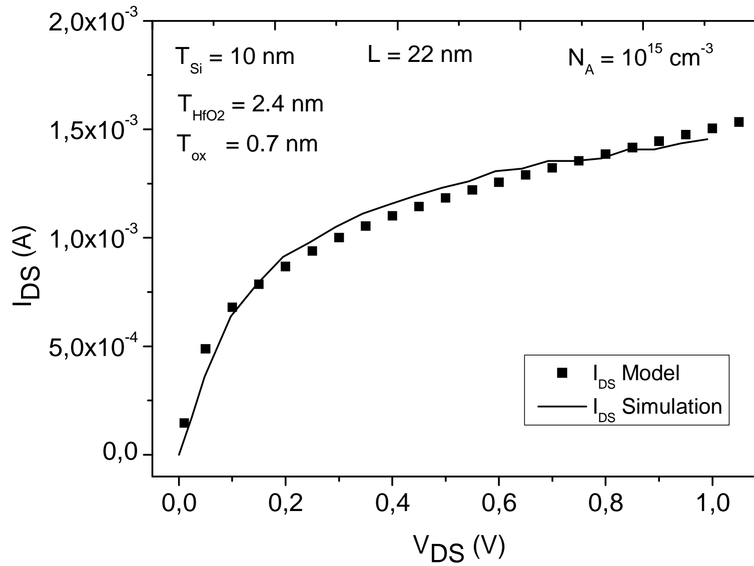


Figure 63. Output curves for V_{GS} = 1V for DGMOSFETs with L = 22 nm. The model is obtained by means of equation 42 where velocity overshoot, quantum effects, short channel effects and saturation velocity are considered. Simulation results are plotted in solid lines and the modeled in symbols.

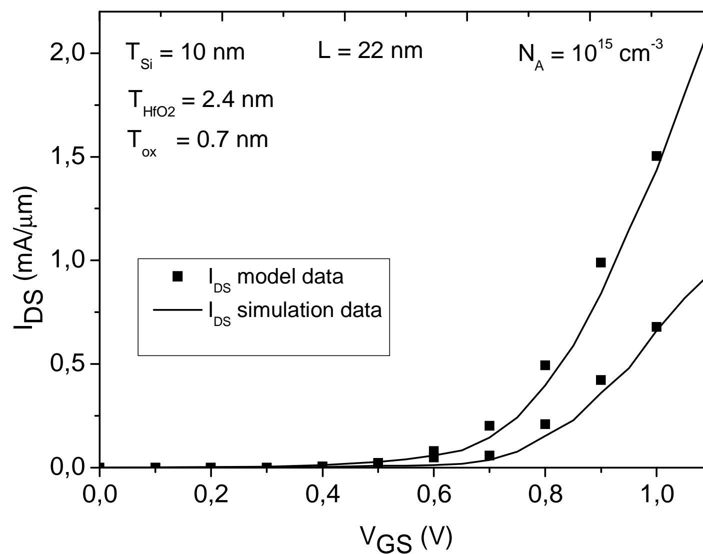


Figure 64. Drain current versus V_{GS} for V_{DS} =1V for DGMOSFETs with L = 22 nm. The model is obtained by means of equation 42 where velocity overshoot, quantum effects, short channel effects and saturation velocity are considered. Simulation results are plotted in solid lines and the modeled in symbols.

The following results have been obtained for device b) in figure 62, with a channel length of 16 nm.

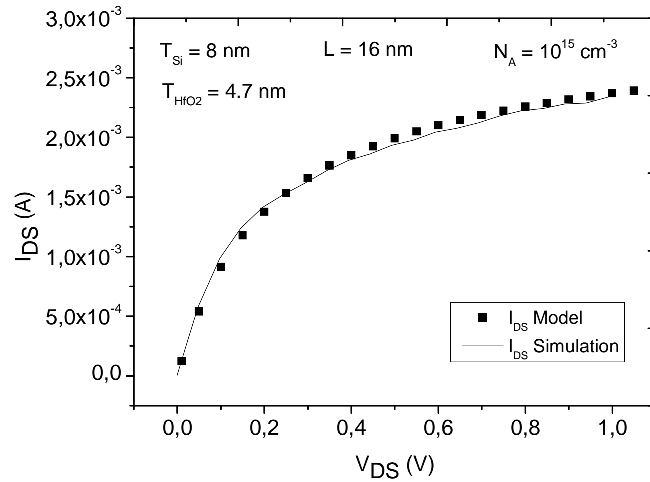


Figure 65. Output curves for V_{GS} = 1V for DGMOSFETs with L = 16 nm. The model is obtained by means of equation 42 where velocity overshoot, quantum effects, short channel effects and saturation velocity are considered. Simulation results are plotted in solid lines and the modeled in symbols.

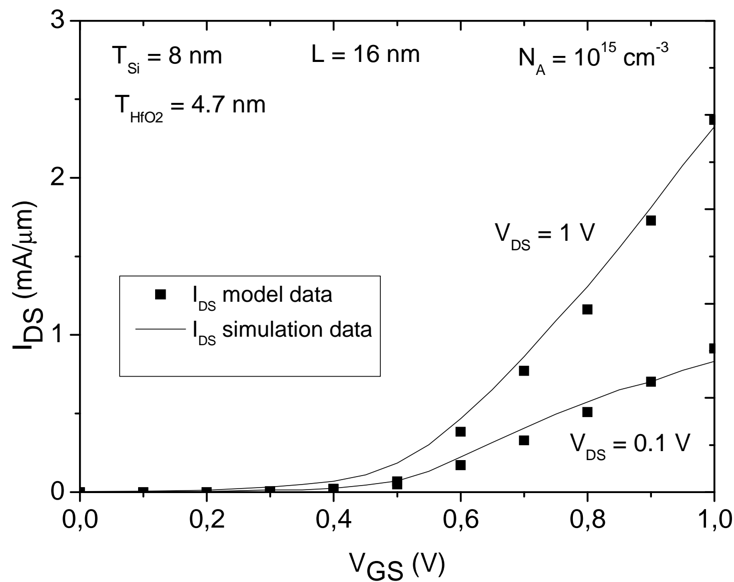


Figure 66. Drain current versus V_{GS} for V_{DS}=1V for DGMOSFETs with L = 16 nm. The model is obtained by means of equation 42 where velocity overshoot, quantum effects, short channel effects and saturation velocity are considered. Simulation results are plotted in solid lines and the modeled in symbols.

As can be seen, a reasonable good fit is obtained in all cases. It is important to highlight that the fit is obtained for two DGMOSFETs with different gate dielectric stacks, channel lengths and silicon layer thicknesses, and for the usual voltage ranges of operation.

	DGMOSFET (L = 22 nm)	**DGMOSFET (L = 16 nm)**
σ_{DIBL} (equation 35)	1	10
n_{DIBL} (equation 35)	1	1
U0 ($cm^2/(V.s)$ (equation 36)	60	300
a (equation 38)	0.68	0.34
b (equation 41)	0.1	0.1

Table 3. Model parameters used to reproduce the two simulated DGMOSFETs of figure 62.

4. Schottky Barrier DGMOSFET advanced modeling

4.1. Introduction

This section of the thesis is devoted to a group of devices that are raising great expectatives in the microelectronics community: Schottky barrier MOSFETs. They represent an interesting alternative to MOSFETs with conventional doped contacts for source and drain [Choi-2010, Kim-2010, Östling-2010, Jang-2010, Knoll-2011]. In these new devices the traditionally highly doped source and drain regions are replaced by metallic contacts. In particular, in line with the results presented in the previous chapter, we will focus on the modeling of Schottky Barrier Double-Gate MOSFETs (SB DGMOSFETs).

In previous chapters we have stated that one of the problems connected with multi-gate devices, also with SOI single-gate FD devices, is related to the high series resistance of the drain and source contacts. Scaling makes the role of source and drain resistances more important since the channel resistance gets reduced as the channel length does so. It is known that a reduction of the silicon layer, T_{Si}, helps to improve SCEs when the channel length is shrunk [Faynot-2011, Skotnicki-2011]. Therefore, for the next technology nodes (below 22nm) the silicon layer thickness of multi-gate devices will have to be reduced in order to control short channel effects, this reduction will also diminish the area between the source/drain contacts and the silicon core, and consequently increase source and drain series resistance[4]. Therefore, the limitation imposed by these parasitic resistances will increase.

One of the solutions proposed to address this important problem is the introduction of metallic materials instead of conventional highly doped semiconductor regions for the source and drain contacts [Lepsleter-1968] (as the reader can see, this is no new concept; however, in the current technological context it is regaining momentum). Rectifying metal-semiconductor junctions, known as Schottky barriers[5], present electric characteristics that resemble doped PN junctions, consequently the drain and source regions in MOSFETs can be replaced by metallic contacts maintaining the basics of the transistor operation. If done, the contact resistance is significantly reduced, even for very shallow junctions; however, this is not the

[4] Scaling in short-channel conventional MOSFETs requires shallower source and drain junctions. This leads to greater source and drain resistances, and consequently their role on the drain current begins to become appreciable.

5 The Schottky barrier can be formed either by deposition of a metal on a semiconductor surface or by silicidation of a portion of semiconductor to form a metal. The latter option is chosen in conventional SB MOSFETs for its simplicity to form with a silicon-compatible process.

only benefit that Schottky barrier (SB) MOSFETs show with respect to their conventional MOSFET counterparts [Xu-2006, Vega-2006, Knoll-2011, Larson-2006].

Another well-known problem related to conventional MOSFETs with semiconductor doped source and drain regions is the parasitic bipolar latch up between adjacent devices. This phenomenon is completely eliminated in transistors with metal source/drain contacts due to the presence of different transport mechanisms like the thermionic emission and tunneling between contacts and channel (the source is not a good emitter in this case) and the consequent reduction of the common-emitter current gain β of the SB junction [Vega-2006, Larson-2004, Sugino-1982]; three to six order of magnitude lower β values with respect to what is found in a conventional source junctions have been reported [Larson-2006]. It is also important to highlight that the SB MOSFETs are fabricated following simpler processing steps due to the fact that they don't need the conventional source and drain regions, which means the elimination of halo implants, dopant activation anneals (the high temperatures used in annealing are incompatible with proposed high-κ gate dielectrics, metal gates and strained substrates required for further scaling, which can be affected by such high temperature treatment) and associated masking and cleaning steps [Larson-2004, Östling-2010]. The fabrication of SB MOSFETs is completely compatible with current CMOS fabrication technologies. In addition to the aforementioned benefits, it also worth highlighting the possibility of reducing channel lengths by taking advantage of the abruptness of the metallic junctions which represent an advantage regarding device scaling [Tucker-1994, Snyder-1995, Larson-2006].

It has been shown that for a body thickness small enough the electrostatic control by the gate causes a significant reduction in the Schottky barrier, thus increasing drive current and improving the subthreshold swing [Knoch-2007]. For these SOI devices, as explained in previous chapters, there is no need for high doping in the channel and therefore Coulomb scattering can be decreased and, consequently, the mobility enhanced [Gámiz-2004]. There are also some drawbacks that show up in this kind of devices, in bulk SB MOSFETs. For example, when dimensions are reduced a large leakage current through the body in the OFF state is found that leads to a low I_{on}/I_{off} ratio. However, ultrathin Schottky barrier SOI MOSFETs have been studied [Knoch-2007] and a good device operation at nanoscale dimensions has been found, obtaining better I_{on}/I_{off} ratio than in bulk SB MOSFETs [Knoch-2007, Guo-2002].

Despite all the advantages detailed previously, the on-current in SB MOSFETs is always limited by the existence of the Schottky barrier at the drain and source contacts, and therefore,

SB MOSFETs performance is not comparable to conventional MOSFETs with doped source and drain regions. For this reason, one of the main challenges for future development of these devices is the finding of an appropriate material for the source and drain contacts with low Schottky barrier height. Silicides[6] seem to be an excellent choice [Jang-2010, Choi-2010, Plumeer-2000, Lu-2002, Padilla-2012] but due to the wide variety of characteristics of these materials, there is still a lot of investigation to be carried out in this field.
Regarding the electrical behavior of the SB MOSFETs, one of the main features to highlight is that they show ambipolar behavior, meaning that two I-V characteristics are obtained with a single device depending on the applied voltages, as can be seen in figure 67.

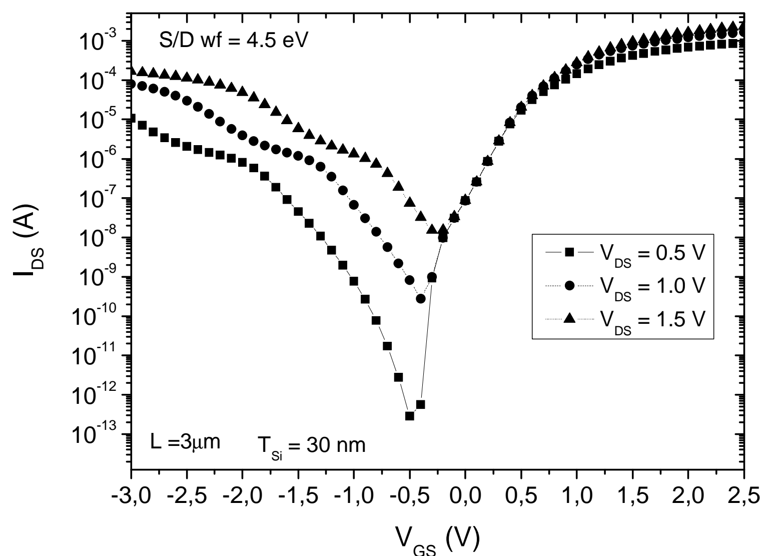


Figure 67. Ambipolar behavior in SB MOSFETs. Simulation data have been obtained from ATLAS for a SB DGMOSFET with the following technological parameters: T_{Si} = 30 nm, L = 3µm, $N_A = 10^{14}$ cm^{-3} and S/D metal contacts whose work function was 4.5 eV.

4.1.1. Schottky barrier basic principles

In this section we will explain the basic principles of operation of Schottky barrier based devices. As a starting point we will use the following figure, where the band structure for the formation of a Schottky barrier is presented. In Figure 68 a) the metal and semiconductor materials are represented as electrically isolated. When the materials are connected (in the rectifying case), electrons from the semiconductor will flow into the metal until the two Fermi

[6] Common silicides that are being used are PtSi, NiSi, $Ni_{1-x}Pt_xSi$, epitaxial $NiSi_2$, and rare earth silicides such as ErSi, $ErSi_2$, or $DySi_{2-x}$.

levels are aligned. When this happens, positively ionized donor atoms form a depletion region in the semiconductor and negative charges are accumulated at the surface of the metal. In this case an electric field is created in the junction region, and as consequence the energy bands in the silicon side are bent upwards. This is depicted in Figure 68b. In addition, in Figure 68c, an ohmic contact is shown. The band diagram of Figure 68b appears when WF > ϕ_s for n-type Si and the ohmic contact (Figure 68c) shows up when WF < ϕ_s.

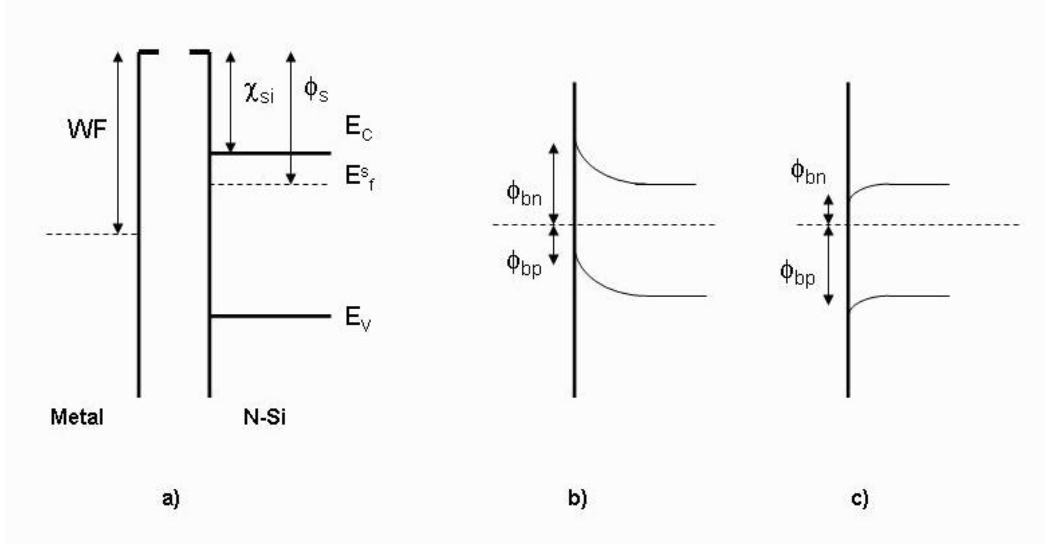


Figure 68. Band structures of a metal-semiconductor junction: a) electrical isolation, b) rectifying contact and c) ohmic contact.

An important parameter in SB MOSFETs is the energy barrier for electrons (Φ_{bn}), between the metal Fermi level in source/drain contacts and the conduction band in the silicon channel, which prevents electrons from entering and traversing the channel. This barrier, depicted in Figure 68, is calculated as follows:

$$\phi_{bn} = WF - \chi_{Si} \tag{43}$$

where WF is the metal workfunction. An analogue way, barrier (Φ_{bp}) is identified for holes, formed between the Fermi level in the metal contact and the valence band in the channel as shown in Figure 68.

$$\phi_{bp} = \chi_{Si} + \frac{E_g}{q} - WF \tag{44}$$

The height of the Schottky barrier (and also the shape) can be modified due to two mechanisms known as image force and dipole induced barrier lowering [Pearman-2007, Sze-2007].

The first mechanism can be explained as follows: in a rectifying metal-semiconductor junction, an electron with charge -q located a distance x from the metal-semiconductor interface establishes an electric field whose field lines terminate normally on the metal surface. These field lines act as if a positive charge +q were located at distance -x from the metal surface, i.e., the mirror image of the electron charge, and the force acting on the electron is the same if the metal surface were replaced by an image charge +q at -x [Yan-1988]. The induced barrier lowering, which is proportional to the square root of the applied electric field [Sze-2007], can be calculated using Coulomb's force of attraction. The second mechanism presented that causes barrier height reduction is due to the presence of a dipole layer at the metal-semiconductor interfaces. Interfacial states between the metal and semiconductor in an intermediate oxide layer were used as an explanation for barrier lowering. Another point of view is the following: the wave functions of electrons in the metal penetrate into the semiconductor (Heine tails) forming metal-induced gap states (MIGS), which form a static dipole layer at the interface. This layer was said to cause a barrier height variation approximately linearly with electric field [Sze-2007], although other approaches have been reported [Vega-2008]. The reduction of the barrier height due to these effects has as a consequence an increase in current because the main transport mechanisms involved in these devices (as they will be explained below) show an important dependency on the barrier height.

The transport mechanisms in SB MOSFETs differ from those that can be found in a conventional MOSFET. While in conventional MOSFETs carrier transport is due to drift-diffusion, different processes can be found in SB MOSFETs in addition to drift-diffusion that can still be applicable in the channel region. These processes are thermionic emission of carriers over the barrier, thermionic field emission of high energy carriers through the upper part of the barrier and field emission of carriers through the barrier at the Fermi level, the latter two are tunneling mechanisms. Depending on the bias condition, one or more of these components will dominate the carrier transport.

In the following figure, the transport mechanisms in SB MOSFETs can be described considering the band structure when different voltages are applied [Balaguer-2011a].

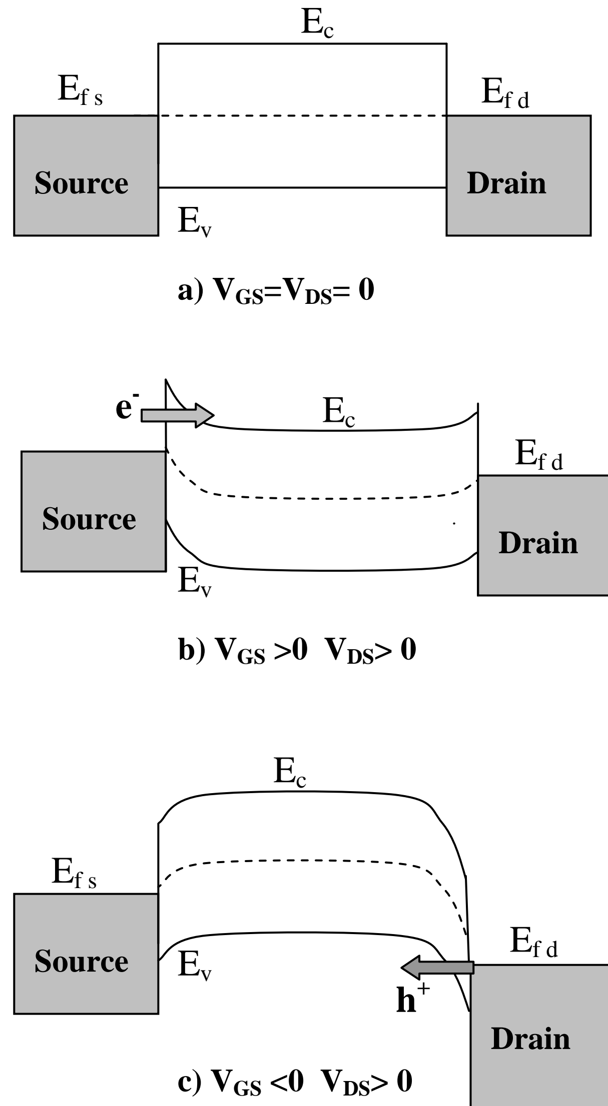


Figure 69. Energy band diagrams for a SB MOSFET loosely illustrating three different operation regimes:a) no drain bias, b) V_{GS} >0 and V_{DS} >0, c) V_{GS} <0 and V_{DS} >0.

As for a conventional MOSFET, the gate bias modifies the channel surface potential via capacitive coupling. The OFF state is presented in figure 69 a). In this case there are neither gate nor drain-source voltages applied. In figure 69 c), the valence band is pushed up as the gate voltages drops off so that the SB width at the drain contact shrinks and becomes increasingly transparent for holes. Some energetic holes are then allowed to tunnel the low Schottky barrier for holes Φ_{bp}. These carriers will then drift to the source end of the channel and exit towards the source metal. In the state depicted in figure 69 b), the conduction band is pushed down as the gate voltage rises, reducing the SB width at the source contact and increasing electron tunneling probability.

In the SB MOSFET drain current calculation, drift-diffusion mechanisms can be applied in the channel region, but also a tunneling current which injects carriers into and out of the channel can be identified (also the thermionic emission component). As it will be shown below, these current components need to be taken into account to accurately model the devices under study. Actually, in the deep subthreshold operation regime the total current seems to be a combination of the diffusion and thermionic emission current components.

Furthermore, leakage can be induced via gate-to-drain coupling at large drain biases and a relatively low or zero gate bias [Vega-2006], if the magnitude of the surface potential in the channel-end region near the drain is large enough to induce band-to-band tunneling (BTBT). It is also important to highlight that for negative gate voltages holes accumulate at drain/channel interface. In this case the barrier width for holes decreases and hole tunneling from the drain side occurs, hence, this mechanism contributes in OFF-state to the current enhancement. As already seen, the two types of carriers (holes and electrons) have an important role in SB MOSFET current calculation which leads to the ambipolarity, one of the most important characteristics of these devices.

4.1.2. SB DGMOSFET

In the introduction of this chapter we have described the advantages of SB MOSFETs compared to traditional MOSFETs with doped source and drain regions. Despite important advantages are found, the high Schottky barrier at the source and drain contacts makes these devices have worse performance than conventional MOSFETs [Knoch-2002, Knoch-2007]. Some important parameters, as the threshold voltage, can be strongly affected by the barrier height [Zhang-2008].

The problems related to the barrier height can be attacked by lowering the effective Schottky barrier using silicides [Larrieu-2005, Yang-2002, Larson-2006] and interfacial layers between the metal and semiconductor [Larson-2006, Kinoshita-2004, Zhang-2005] together with the use of ultra-thin gate oxide and ultra-thin body SOI. Therefore, it is important to study the features of SOI technology combined with SB MOSFETs. The advantages of SOI have already been presented in the first chapter of this work and the same arguments can be applied to the fabrication SB MOSFETs on SOI substrates. The main advantages related to SOI substrates, such as better electrostatic control and enhanced device performance when scaling, have also been found on SB MOSFETs fabricated on SOI [Larrieu-2004].

In using SOI SB devices, a special consideration has to be dedicated to the Si thickness. It has to be carefully chosen in order to find the optimum trade-off between the modification of barrier height caused by band splitting (due to quantum structural confinement) and the improvement in electrostatics obtained decreasing T_{Si}. In order to obtain high performance Schottky barrier MOSFETs, thin film SOI has been used in combination with silicidation, these techniques commented previously. The silicidation, in the MOSFET fabrication context, is a well-known process where a metal film is deposited on a prefabricated gate structure with oxide or nitride spacers (the sidewall thickness is key to minimize S/D-to-gate underlap). During annealing the metal reacts exclusively with Si or poly-Si regions and forms a silicide at source, drain and gate. The unreacted metal after silicidation can be selectively etched away. The spacer is very important for the electrical insulation between the gate and the source/drain in the fabrication. Silicides are commonly used as ohmic contacts, Schottky contacts and interconnects. The advantages of silicides include a low parasitic resistance and a high thermal stability. $TiSi_2$, PtSi and $CoSi_2$ have been investigated as materials for silicides in the development of Si technology [Maex-1998, Larson-2006].

The use of dopant segregation during silicidation enables the formation of thin, highly doped layers at the source/drain-channel interfaces. During the silicidation step, the dopants redistribute between the silicide and the silicon which affects the electrical properties of the resulting Schottky contact [Wittmer-1984]. Experimental results have shown that the SB devices with dopant segregation show behavior closer to conventional MOSFETs due to the decrease of the effective SB barrier height caused by the highly doped area [Knoch-2005]. The new technology of dopant segregation can be applied to high mobility channel materials like strained-Si and high-κ dielectrics to achieve a further development of device performance.

The interesting characteristics of SB MOSFETs have led to the development of models that describe their behavior for circuit simulation applications. Several models have been developed recently for SB DGMOSFETs to calculate the potential and charge within the devices [Schwarz-2011]. In the same way, models for new architectures like GAA have also been developed for SB MOSFETs [Zhu-2010].

4.2. Schottky Barrier Double-Gate MOSFET current model

In this section, an analytical and explicit compact model for undoped symmetrical silicon Double Gate MOSFETs (DGMOSFETs) with Schottky Barrier (SB) source and drain is

presented [Balaguer-2011a]. The model is based on a previously published DGMOSFET model [Moldovan-2007a] which has been extended to include the characteristic transport mechanisms of SB MOSFETs.

The final model has been validated with numerical data obtained with the 2D ATLAS device simulator presented in section 2.2, where a SB DGMOSFET structure including metallic contacts at the source and drain regions have been defined and characterized to obtain the transfer and output characteristics for several bias configurations. The simulated structure was presented in figure 11 where it can be seen that no drain and source regions are specified, they are represented by two metallic contacts instead. In ATLAS, an electrode contact with semiconductor material is assumed by default to be ohmic. Therefore, in order to assure that the source and drain contacts behave as Schottky contacts instead of as ohmic contact, a suitable work function has been defined for both of them.

As already indicated in section 2.2, the ATLAS models [ATLAS-2010] used to simulate the SB DGMOSFETs are the UST (Universal Schottky Tunneling) and the BTB (Band-To-Band Tunneling). The contribution of both types of carriers, electrons and holes, is considered in all the simulations. Lightly doped NMOS devices with two channel lengths (2 μm and 3 μm) have been simulated and modeled. We have also used different metal work functions to validate our model; in this respect, in sweeping this parameter we have indirectly included the effects connected with image force and dipole barrier lowering [Pearman-2007]. The model characterizes both the electron and hole currents in the device for the usual operation regimes. In this respect, we have identified and modeled the main current components that contribute to the calculation of the total current. The inclusion of the quantum, velocity saturation and short channel effects needed for the correct description of thin silicon layers and short channel devices will be considered in future works as an extension of the model presented here. The use of long channel devices is the best option to identify and analyze the different current mechanisms involved in the charge transport since short channel effects can be neglected. None of the parameters included in the model depend on the channel length.

The main characteristics of the SB DGMOSFET model are the fact that it is explicit and analytical [Balaguer-2011a], which makes it very useful from the compact modeling viewpoint. This model differs from others published so far for SB MOSFETs [Xiong-2005, Knoch-2007] which are numerical models where iterative algorithms have to be used in order to obtain the main device magnitudes, such us the current, the characteristic capacitances, etc.

4.2.1. Ambipolar current general model

The modeling of SB DGMOSFETs current was performed by separately modeling the contribution of electrons and holes. For the electron current calculation we have used as a starting point the analytical and explicit expression given in the previous chapter for an undoped DGMOSFET (29) [Moldovan-2007a]:

$$I_{drift_diffusion_n} = \frac{W\mu_n}{L}\left[\left(\frac{Q_{S_n}^2 - Q_{D_n}^2}{4C_{ox}} + 2\beta\left(Q_{S_n} - Q_{D_n}\right) + \beta^2 8C_{si}\ln\left(\frac{8\beta C_{si} + Q_{D_n}}{8\beta C_{si} + Q_{S_n}}\right)\right)\right] \tag{45}$$

Following a modeling procedure similar to the one presented in reference [Moldovan-2007a] for the calculation of the electron current, we have obtained an analogue analytical expression for the hole current.

$$I_{drift_diffusion_p} = \frac{W\mu_{holes}}{L}\left[\left(\frac{Q_{D_p}^2 - Q_{S_p}^2}{4C_{ox}} + 2\beta\left(Q_{S_p} - Q_{D_p}\right) - \beta^2 8C_{si}\ln\left(\frac{8\beta C_{Si} + Q_{D_p}}{8\beta C_{Si} + Q_{S_p}}\right)\right)\right] \tag{46}$$

where β has the same value as for equation 28.

Several investigations have demonstrated that SB MOSFETs threshold voltage depends on the height of the barrier formed between the Si and the S/D metallic contact [Zhang-2008]. In order to model this behavior, we have used as a starting point the threshold voltage model presented in reference [Moldovan-2007a] and modified it by introducing a parameter to account for the barrier height dependence. In this way, the expressions to model the threshold voltages for electrons and holes are the following,

$$V_{T_n} = V_{on} + \frac{K_n\phi_{bn}}{q} + 2\beta\ln\left(1 + \frac{Q_n^{'}}{2Q_0}\right) \tag{47}$$

$$V_{T_p} = V_{op} + \frac{K_p\phi_{bp}}{q} + 2\beta\ln\left(1 + \frac{Q_p^{'}}{2Q_0}\right) \tag{48}$$

where ϕ_{bn} and ϕ_{bp} are the Schottky barrier for electrons and holes calculated in equations 43 and 44. The values found for the fitting parameters were $K_n = 0.6$ and $K_p = -1$.

In equation 47 the charge $Q_n^{'}$ for electrons is calculated as follows [Moldovan-2007a]:

$$Q_n^{'} = 2C_{ox}\left(\left(-\frac{2C_{ox}\beta^2}{Q_0}\right)+\sqrt{\left(\frac{2C_{ox}\beta^2}{Q_0}\right)^2 + 4\beta^2\log^2\left[1+\exp\left[\frac{V_{GS}-V_{on}-V}{2\beta}\right]\right]}\right) \quad (49)$$

where β has the same value as presented previously and Q_0 and V_{0n} are calculated as follows:

$$Q_0 = 4\left(\frac{KT}{q}\right)C_{Si}$$
$$V_{0n} = \Delta\varphi - \beta\ln\frac{qn_iT_{Si}}{2Q_0} \quad (50)$$

In a similar way, Q_p' for holes can be obtained from the following expression:

$$Q_p^{'} = 2C_{ox}\left(\left(-\frac{2C_{ox}\beta^2}{Q_o}\right)+\sqrt{\left(\frac{2C_{ox}\beta^2}{Q_o}\right)^2 + 4\beta^2\log^2\left[1+\exp\left[\frac{-(V_{GS}-V_{op}-V)}{2\beta}\right]\right]}\right) \quad (51)$$

where β and Q_0 are calculated as given before for electrons and V_{0p} is calculated as follows:

$$V_{0p} = \Delta\varphi + \beta\log\left(\frac{qn_iT_{Si}}{2Q_0}\right) \quad (52)$$

The charges Q_{S_p} and Q_{D_p} for the drain current calculation are analytically computed using the following expression: Q_p at the source (V=0, corresponding to Q_{S_p}) and at the drain (V=V_{DS}, corresponding to Q_{D_p}):

$$Q_p = 2C_{ox}\left(\left(-\frac{2C_{ox}\beta^2}{Q_0}\right)+\sqrt{\left(\frac{2C_{ox}\beta^2}{Q_0}\right)^2 + 4\beta^2\log^2\left[1+\exp\left[\frac{-(V_{GS}-V_{T_p}+\Delta V_{T_p}-V)}{2\beta}\right]\right]}\right) \quad (53)$$

Where V_{T_p} is given in (48) and ΔV_{T_p} is calculated by means of the following equation:

$$\Delta V_{T_p} = \frac{\left(\frac{C_{ox}\beta^2}{Q_0}\right)Q_p^{'}}{\frac{Q_p^{'}}{2}+Q_0} \quad (54)$$

The electron charge calculation follows a similar procedure as described in [Moldovan-2007a].

Once the drift-diffusion components of the current for electrons and holes have been obtained, we can add them to obtain an ambipolar current model accounting only for drift-diffusion mechanisms which will fit simulation data well above the threshold voltage.

4.2.2. Current model for electrons. Tunneling current component

We have adapted the drift-diffusion current model to the SB transistor; to do so, a parameter has been added to the electrons and holes mobility models (μ_n, μ_p) to take into account the effect of the Schottky barrier formed for both type of carriers. In this respect, the electrons and holes mobilities can then be calculated as follows,

$$\begin{aligned} \mu_n^{SB}(\phi_{bn}) &= \mu_n(C_n + D_n\phi_{bn}) \\ \mu_p^{SB}(\phi_{bp}) &= \mu_p C_p \exp(-d_p\phi_{bp}) \end{aligned} \qquad (55)$$

where C_n, D_n, C_p, d_p are fitting parameters whose values are the following, C_n = 1.62, D_n = -2.08 (1/eV), C_p = 194.11 and d_p = 24.54 (1/eV). An optimized complementary silicide structure requires a silicide for NMOS having a low barrier to electrons (Φ_{bn}), and for PMOS a low barrier to holes (Φ_{bp}).

In order to model the subthreshold and near threshold behavior, we had to introduce further transport mechanisms. Following the previous modeling scheme, we focus on electrons and holes mechanisms separately. To model the electrons behavior in subthreshold region, we introduced a current component that accounts for the tunneling at the contact Schottky barriers [Pearman-2007]:

$$I_{tunneling_n} = area\, A T^2 \exp\left(\frac{-\phi_{bn}}{E_{00}}\right)\left(\exp\left(\frac{V_{GS}}{nkT}\right) - 1\right) \qquad (56)$$

A is the Richardson constant ($1.20173 \cdot 10^2$ $Acm^{-2}K^{-2}$) [Padovani-1966, Crowel-1969a] and E_{00} (eV) is a constant of the material and it is associated with the WKB expression for the transmission of the barrier for carriers of energy E=0). This parameter [Jang-2002, Crowel-1969b] is calculated as:

$$E_{00} = \alpha(\phi_{bn}) q \frac{\hbar}{2} \sqrt{\frac{N_A}{m^* \varepsilon_{Si}}} \tag{57}$$

where m* is the effective electron mass and α is a parameter that depends on the SB barrier height for electrons,

$$\alpha(\phi_{bn}) = F + U\phi_{bn} \tag{58}$$

F and U are fitting parameters that have the following values: F = 21.8 and U = 36.6 (1/eV).
We have combined this tunneling component with the drift-diffusion component in the following way to obtain the total electron current:

$$I_{DS_n} = \frac{I_{drift_diffusion_n} I_{tunneling_n}}{I_{drift_diffusion_n} + I_{tunneling_n}} \tag{59}$$

The thermionic emission current component has the same dependence on V_{GS} (exponential one) that the diffusion current component. In the deep subthreshold operation regime, the total current is a combination of these two components. In this respect, the thermionic emission component has been included in the diffusion one by means of the threshold voltage and mobility dependencies on the Schottky barrier height.
Equation 59 is built as an interpolation function to account for the different weight of the drift-diffusion, thermionic emission and tunneling current components (this equation has been used by several authors before, see for example Ref. Tsormpatzoglou-2009). Using this expression the total current behavior can be obtained because each current component behaves as the dominant mechanism in a specific operation region according to the bias. These current mechanisms have been calculated separately considering in the calculation that the other components do not exist. In this respect, in strong inversion the total current tends to the drift component (equation 45) as the tunneling current calculated from equation 56 is, in this case, much higher. For very low gate voltages the main current components to take into account are the thermionic emission and diffusion ones, for medium gate voltages (also within the subthreshold operation regime), and the tunneling component is the one that contributes mainly to the total electron current.
In figure 70 the electron current obtained using the previous model is shown together with the simulation data from ATLAS. As can be seen, the modeled data fit the simulation accurately and reproduce the different subthreshold slopes obtained in the simulation data.

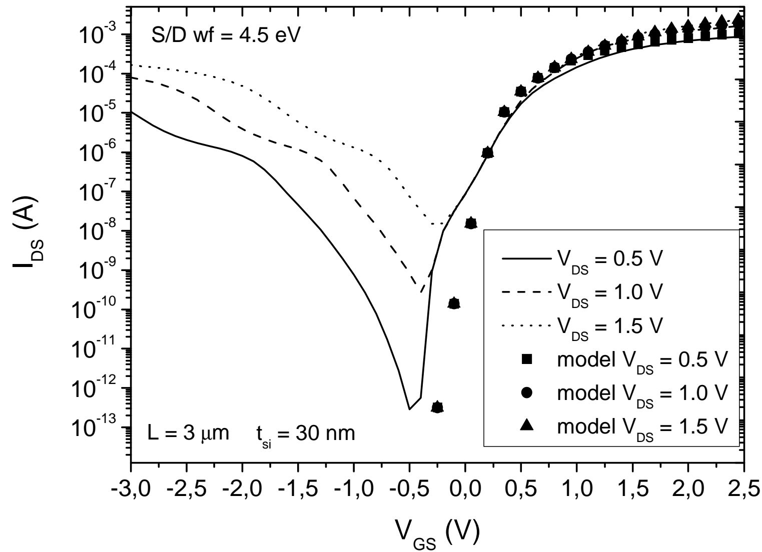


Figure 70. Drain current (accounting only for the electron contribution) including drift-diffusion and tunneling in SB DGMOSFETs with S/D metal contacts whose work function is equal to 4.5 eV and L = 3 µm. The simulation results obtained from ATLAS are plotted in solid lines and the modeled data in symbols.

In figure 71 the different components that contribute to the total current are depicted. In the case of the electron there are two components as explained in this section that are the drift-diffusion component and the tunnel current component.

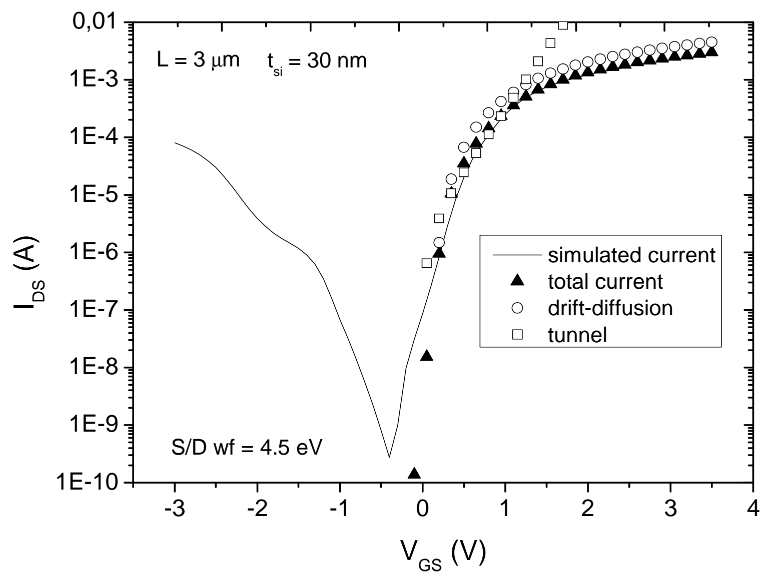


Figure 71. Drift-diffusion and tunnel current contribution to the total current for V_{DS} = 1.0 V. The simulated current obtained by ATLAS is plotted in solid line, the total current obtained from the model is plotted in solid triangles, the drift-diffusion component of the total current is plotted in hollow circles and the tunnel current component of the total current is plotted in hollow squares.

4.2.3. Drain current model for holes. GIDL current component

The next step in our modeling process was aimed at the calculation of the hole current. In this respect, as already stated at the introduction, an important mechanism to take into account is the band to band tunneling [Racko-2008]. The ATLAS [ATLAS-2010] model for the BTBT includes barrier lowering due to image charges, therefore, the model used to obtain the simulation data is consistent with the BTBT model proposed in [Adell-2007] that will be used here, and that has been adapted to account for the hole current component as follows:

$$I_{BTBT_p} = AqE_S^{\sigma} \exp\left[\frac{-B}{E_S}\right] \quad (60)$$

where A is a constant ($4x10^{14}$ $V^{-1}s^{-1}cm$) and B (V/cm) is a tunneling probability parameter where we have introduced a dependence on the barrier height for holes Φ_{bp},

$$B(\phi_{bp}) = S\frac{\phi_{bp}}{q} + T \quad (61)$$

where S = $-40x10^6$ cm^{-1} and T = 100 MV/cm.
In [Adell-2007] the parameter σ (equation 60) has a value of 2.5, but in our model we have used σ = 1 [Semenov-2002].

Finally the electric field at the silicon surface, E_S in equation 60, is calculated as follows [Adell-2007], where we have introduced a fitting parameter R = 2 (V).

$$E_S = \frac{-\left(V_{GS} - V_{DS}\right) - \frac{E_g}{q} + R}{3T_{ox}} \quad (62)$$

The BTBT current component is quantitatively important in the operation region when there is no inversion charge at the drain side. The total SB DGMOSFET hole current was obtained by adding this BTBT current to the drift-diffusion current as follows:

$$I_{DS_p} = I_{drift_diffusion_p} + \gamma(\phi_{bp}) I_{BTBT_p} \tag{63}$$

where

$$\gamma(\phi_{bp}) = V \exp(x\phi_{bp}) \tag{64}$$

with V = 0.34 and x = -10.88 $(eV)^{-1}$.

The model develops explicit expressions to account for the main current components of SB double gate MOSFETs. We have chosen this compact modeling approach focusing our efforts in obtaining a set of equations that can be easily implemented in a circuit simulator. Another way to tackle the problem could have been based on a modification of the boundary conditions at the sides of the channel. This approach might be regarded less empirical, although it would surely be affected by a higher numerical burden in terms of iterative algorithms that could pose important difficulties from the circuit simulation viewpoint.
In figure 72, the hole current obtained using the previous model is shown in symbols. As can be seen, simulation data are reproduced taking into account only the BTBT effect, despite of a tunneling mechanism, similar to the one included in the calculation of the electrons current, is also available for holes. In this case there is no need to include this mechanism, as it is masked by the BTBT component.

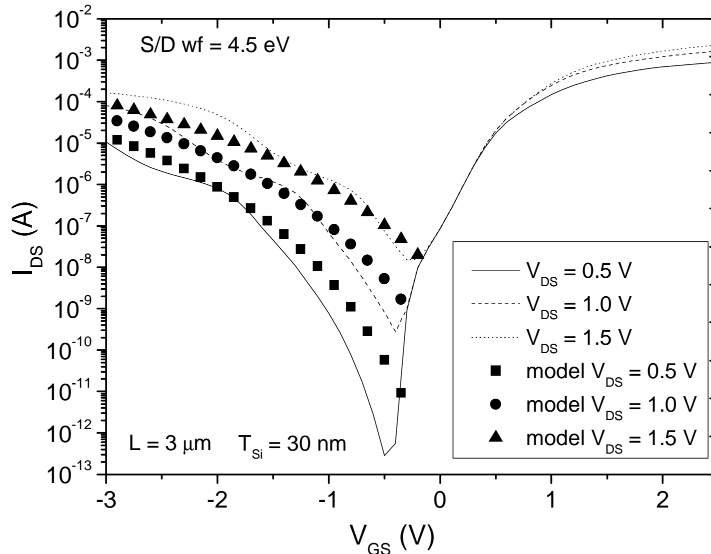


Figure 72. Drain current (accounting only for the hole contribution) including drift-diffusion and BTBT for a SB DGMOSFET with S/D metal contacts whose work function is equal to 4.5 eV and L = 3μm. The simulation results obtained from ATLAS are plotted in solid lines and the modeled data symbols.

In figure 73 the different components that contribute to the total hole current are depicted. In this case, the two components explained previously are the drift-diffusion and the GIDL current component.

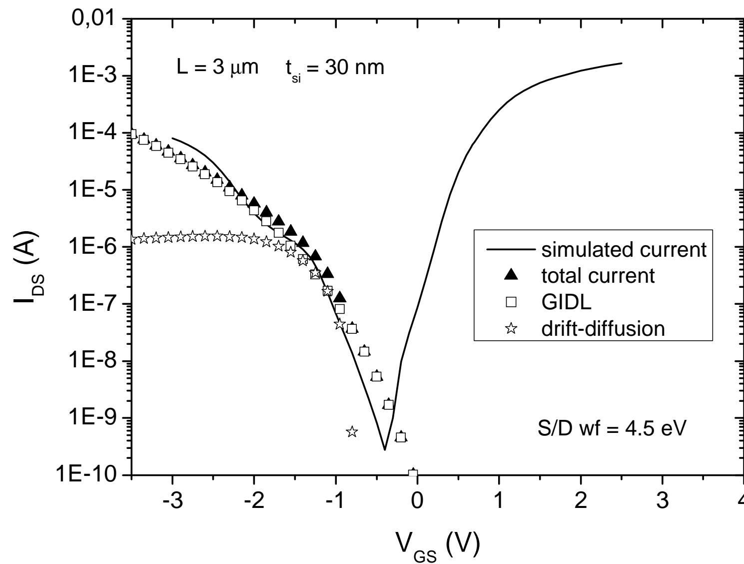


Figure 73. Drift-diffusion and GIDL current contributions to the total current for V_{DS} = 1.0V. The simulated current obtained by ATLAS is plotted in solid lines, the total current obtained from the model is plotted in solid triangles, the drift-diffusion component is plotted in stars and the GIDL current component is plotted in hollow squares.

4.2.4. Complete current model

The total current model for the SB DGMOSFET is therefore calculated by adding the electron and hole contributions:

$$I_{DS} = I_{DS_n} + I_{DS_p} \tag{65}$$

Using this model, the output characteristics for different gate voltages have been plotted, see figure 74. As can be observed, the model fits reasonably well the simulated drain current [Balaguer-2011a].

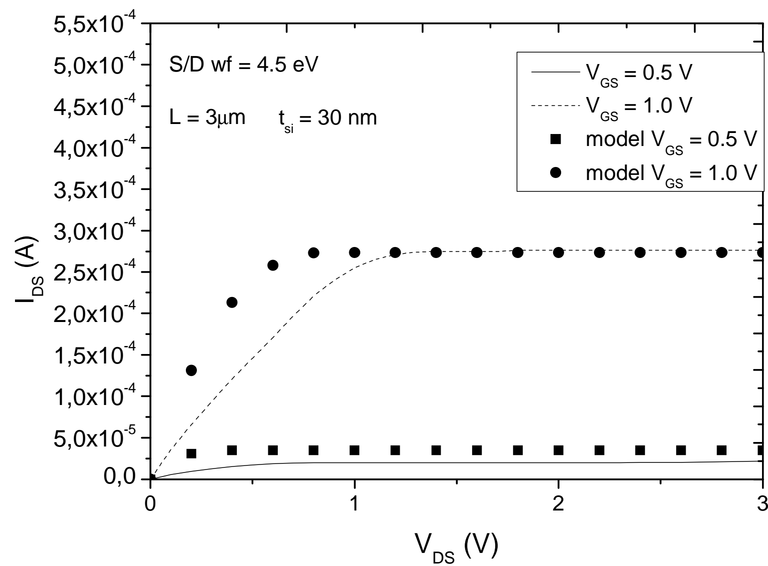


Figure 74. Drain current versus VDS for VGS=0.5V and 1V in SB DGMOSFETs with S/D metal contacts whose work function is equal to 4.5 eV and L = 3μm. The simulation results obtained from ATLAS are plotted in solid lines and the modeled data in symbols.

We have also used the model presented below to reproduce the simulation data obtained for SB DGMOSFETs with different values for the work function of the metal contact material used in the source and the drain and different channel lengths. Although some fitting discrepancies can be observed in figure 74; in general, the model agrees reasonably well with the 2D simulation data. Taking into consideration that this is the first version of an analytical and explicit model (from a compact modeling viewpoint) for SB DGMOSFETs, and the discrepancies are not severe, the overall accuracy is good enough.

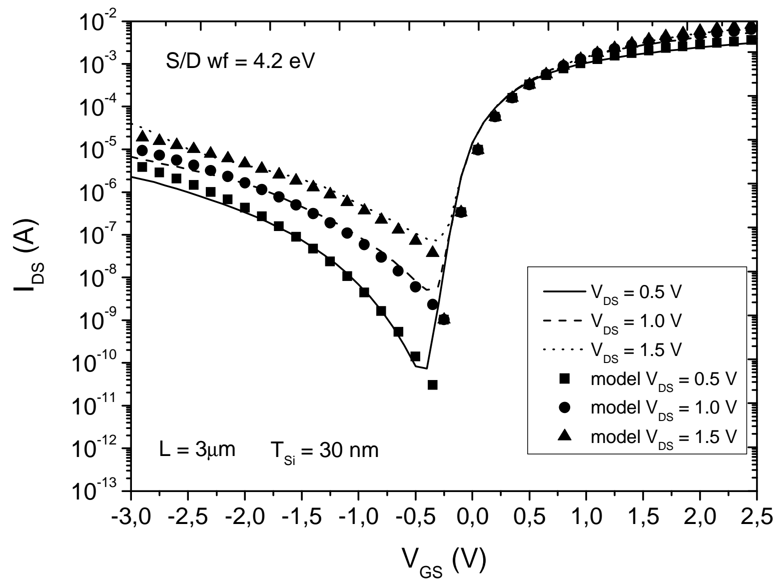


Figure 75. Transfer characteristics for different drain voltages for a SB DGMOSFETs with S/D metal contacts whose work function is equal to 4.2 eV and L = 2µm. The simulation results obtained from ATLAS are plotted in solid lines and the modeled data in symbols.

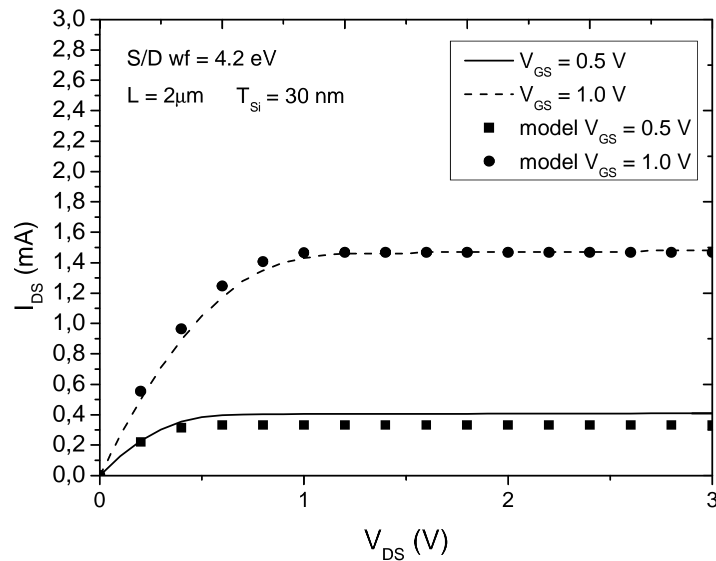


Figure 76. SB DGMOSFET drain current versus V_{DS} for V_{GS} = 0.5V and 1V. The S/D metal contacts work function is equal to 4.2 eV and L = 2µm. The simulation results obtained from ATLAS are plotted in solid lines and the modeled data in symbols.

In the previous figures it can also be seen that simulation data are accurately reproduced by the model. The different transport mechanisms that take place in the SB device for the different voltages in the gate and the source and drain and for the two types of carriers are

correctly taken into account in the model giving as a result a good fitting. It must also be remarked that changes in barrier height are accurately described by introducing in the mobility calculation the barrier height as a parameter.

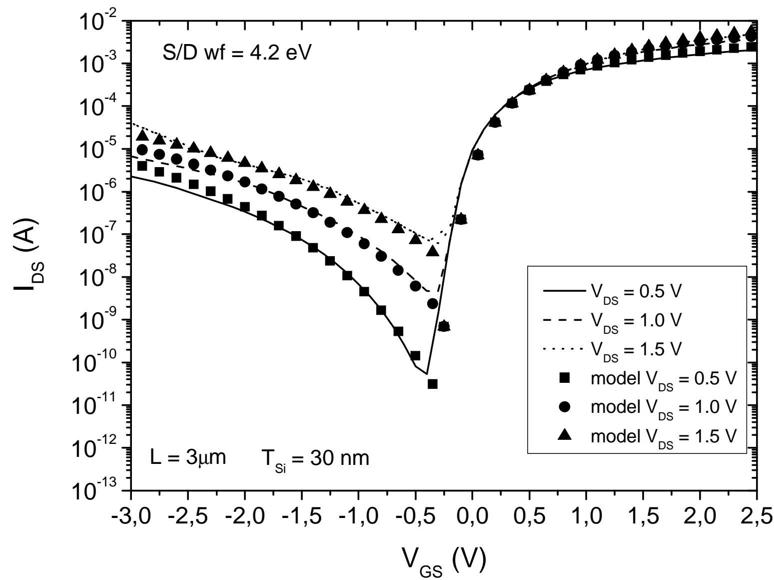


Figure 77. Transfer characteristics for different drain voltages for a SB DGMOSFET with S/D metal contacts whose work function is equal to 4.2 eV and L = 3µm. The simulation results obtained from ATLAS are plotted in solid lines and the modeled data in symbols.

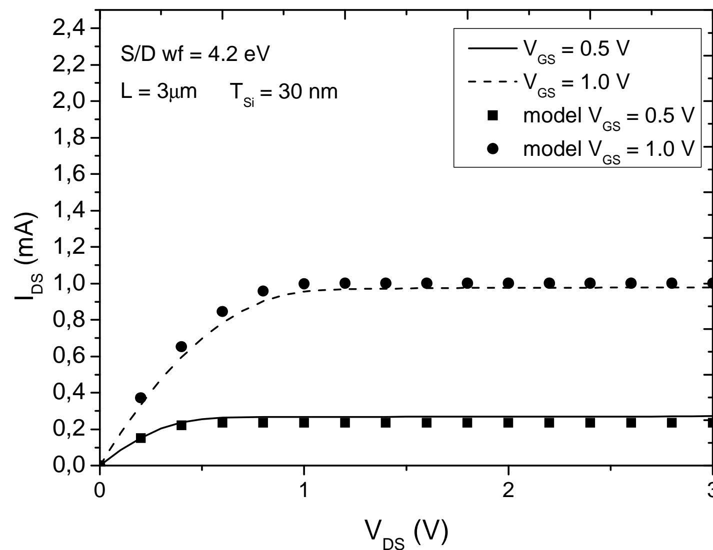


Figure 78. SB DGMOSFET drain current versus V_{DS} for V_{GS} = 0.5V and 1V. The S/D metal contacts work function is equal to 4.2 eV and L = 3µm. The simulation results obtained from ATLAS are plotted in solid lines and the modeled data in symbols.

A good fitting can also be seen in the figures above for SB DGMOSFETs with different channel lengths. Different metal workfunctions were used in the plots shown below.

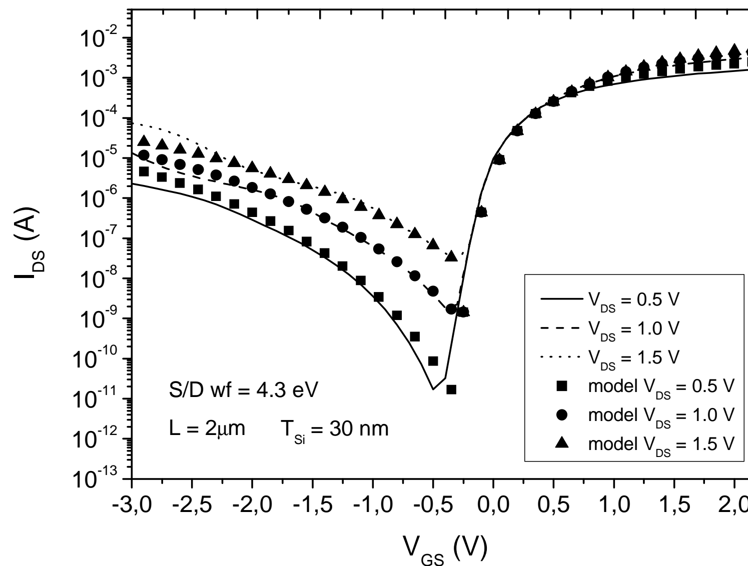


Figure 79. Transfer characteristics for different drain voltages for a SB DGMOSFET with S/D metal contacts whose work function is equal to 4.3 eV and L = 2µm. The simulation results obtained from ATLAS are plotted in solid lines and the modeled data in symbols.

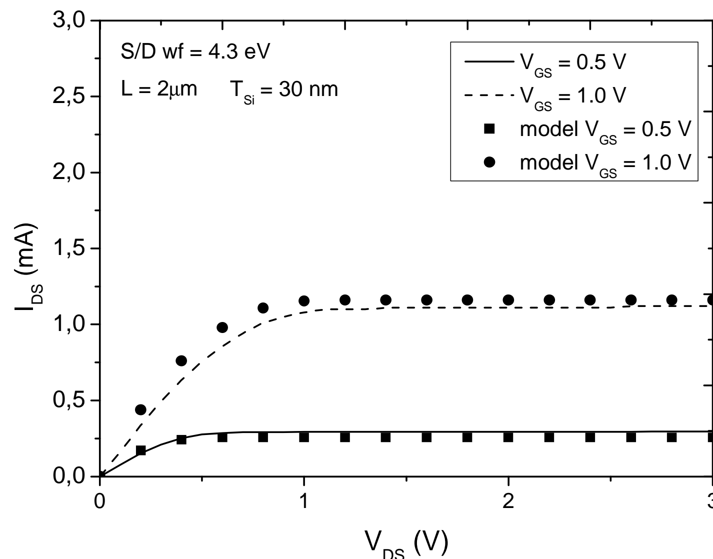


Figure 80. SB DGMOSFET drain current versus V_{DS} for V_{GS} = 0.5V and 1V. The S/D metal contact work function is equal to 4.3 eV and L = 3µm. The simulation results obtained from ATLAS are plotted in solid lines and the modeled data in symbols.

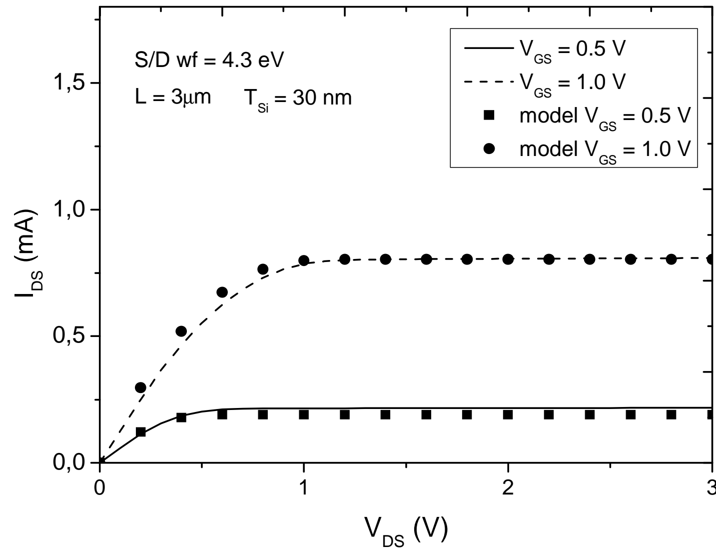


Figure 81. SB DGMOSFET drain current versus V_{DS} for V_{GS} =0.5V and 1V. The S/D metal contact work function is equal to 4.3 eV and L = 2μm. The simulation results obtained from ATLAS are plotted in solid lines and the modeled data in symbols.

To wrap up we will summarize the main results presented in the previous pages. We have developed a model for SB DGMOSFETS which includes the contribution of electrons and holes (for holes the model is based on a drift-diffusion current expression developed previously for n-type undoped DGMOSFETS). It also incorporates the main transport mechanisms presented in SB DGMOSFETs that differ from those presented in conventional DGMOSFETs, such as tunneling through the metal-semiconductor junction and band to band tunneling (BTBT) at the channel end, close to the drain. The ambipolar behavior is inherently taken into account. The model has been successfully applied to reproduce the simulation data obtained from ATLAS for different values of the source and drain metal contact work function. A good agreement was achieved for both the transfer and output characteristics, and for several bias configurations, different channel lengths and metal workfunctions, as can be seen from the previous figures.

5. Surrounding gate transistors advanced modeling

5.1. Introduction

This chapter is devoted to an important group of multi-gate MOSFETs. In these devices the gate completely surrounds the silicon core where conduction takes place (they are known as Gate-All-Around (GAA) MOSFETs or Surrounding-Gate Transistors (SGTs)). These transistors are thought to be the architecture choice when dealing with channel lengths below 10 nm (see the figure below [Faynot-2011], and also figure 8). As it will be shown in the next section, the geometrical confinement of the inversion charge is maximum for this device geometry (much higher than in DGMOSFETs) and also the complexity of the physics needed in the modeling process.

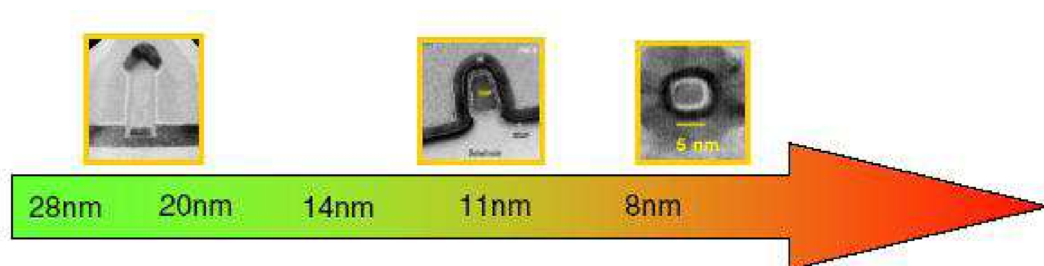


Figure 82. Device architecture evolution for the scaling landscape of the coming years [Faynot-2011].

Before summarizing the description of the following sections, we point out the most important features of SGTs. As explained in chapter 1, the use of several gates has demonstrated good electrostatic control of the channel charge and, hence, the possibility of scaling beyond the potential of traditional bulk MOSFETs. Structures such as SGTs are the most promising in this respect: drain-induced barrier-height lowering, threshold voltage roll-off, subthreshold voltage and OFF state leakage are greatly reduced.

These kind of transistors have not only been studied theoretically but they have been fabricated and their functionality has been accurately tested [Chen-2008, Chen-2010, Sato-2010]. The next step in their development is the implementation of compact models that could correctly describe the behaviour of these multi-gate transistors. Although some models have already been published [Iñiguez-2005, Jiménez-2004, Roldán-2008b], the modelling for these devices is still at an early stage. Therefore, this is a very interesting field that must be further developed.

The reduction in the dimensions of multi-gate structures, and their geometrical particularities, leads to a high degree of inversion charge confinement [Balaguer-2011b, Roldán-2008b, Nazarov-2011]. For SGTs, this effect is more critical or relevant since the electron gas is quantized in 2D and there is only one degree of freedom for the carriers transport, usually in the direction perpendicular to the area of confinement

This fact makes the characterization and modeling of quantum effects mandatory to accurately describe their electrical and transport properties [Moreno-2010, Moreno-2011, Nazarov-2011, Jiang-2012]. However, accounting for a pure physical description of QMEs on the inversion charge and drain current would make circuit simulation time-consuming due to the complexity of the analytical expressions needed; and therefore, inappropriate for IC design houses. For this reason, and in line with the results presented before for DGMOSFETs, analytic modeling has been carried out by means of a semiempirical approach [Roldán-2008b, Roldán-2010]. So, in order to coherently follow an approach similar to that presented in chapter 3 we will first focus on the study of quantum effects in SGTs. Then, we will deal with the inversion charge centroid characterization and modeling [Roldán-2008b], which will be the basis to calculate the inversion charge.

Cylindrical SGTs will be the devices mainly studied in this chapter. For the first time, QMEs have been included in an explicit inversion charge model for these transistors; this was done maintaining the main advantages of a previous model on which we based ours [Iñiguez-2005, Jiménez-2004]. The new model accounts for the threshold voltage shift to characterize the charge distribution [Roldán-2008b]. This approach helps to describe and comprehend the quantitative influence of the main physical effects on the inversion charge. The model was validated with data obtained from the simulator presented in section 2.4 (solving self-consistently the 2-D Poisson and Schrödinger equations, without limitations on the number of subbands). This fact makes our model a good complement as well as an improvement to others obtained using the analytical solution of the Schrödinger equation [Gnani-2004].

Before the model is fully developed, in section 5.2, QMEs are studied in depth in a parallel way to what we showed for DGMOSFETs. This study was also focused on the calculation of the Q factor (see equation 5), already introduced for DGMOSFETs. The Q factor characteristics for different SGTs geometries (T_{ox} and T_{Si} variations were included) and for the usual operation regime were analyzed. Some preliminary results related to the Q factor for SGT devices were already presented in [Roldán-2008a], however an enhanced study is presented here.

Section 5.4 is focused on the study SGTs with high-κ materials as gate dielectric to replace the traditional SiO_2. A model based on the previous one has been developed to incorporate the inclusion of these materials as gate insulators (QMEs included). We did so by enhancing the inversion charge centroid model developed for silicon devices. A comparison with simulation data proved the accuracy of the model. Finally some results related to the low-field mobility are presented in section 5.6. The aim of this section will be to present results similar to those for the DGMOSFETs to complete the modeling landscape of these devices.

5.2. Quantum mechanical effects

Here we will characterize the influence of quantum mechanical effects on the inversion charge of SGTs with both cylindrical and rectangular cross-sections by means of the Q factor defined in equation 5. Following the approach employed in section 3.2, different geometries and gate voltages were used. Firstly we characterized the cylindrical ones; secondly, and for the sake of clarity, we also introduced rectangular SGTs. In this manner the influence of the oxide-semiconductor interface perimeter and the cross-section, in particular the corners of the rectangular shapes, were analyzed.

The structure simulated in the cylindrical case is shown in figure 14. The basic technological characteristics correspond to a midgap metal gate and an undoped silicon substrate (the devices were supposed to operate at room temperature in all the cases considered in this section). The crystallographic orientation considered is (001)/<001>.

For the cylindrical device, different oxides thicknesses were used. On the one hand, a set of simulations were performed with a constant oxide thickness (T_{ox} = 1nm) changing the cylinder radius; the results are plotted in figure 83a. On the other hand, a constant insulator capacitance was used as a reference; this case is shown in figure 83b. Since the oxide capacitance of a cylindrical SGT is given by the equation below [Roldán-2008b], it is clear that for each silicon core radius R a different T_{ox} was needed to keep C_{ox} constant.

$$C_{ox} = \frac{\varepsilon_{ox}}{R \ln\left(1 + \frac{T_{ox}}{R}\right)} \tag{66}$$

The simulation data for the SGTs considered are given below.

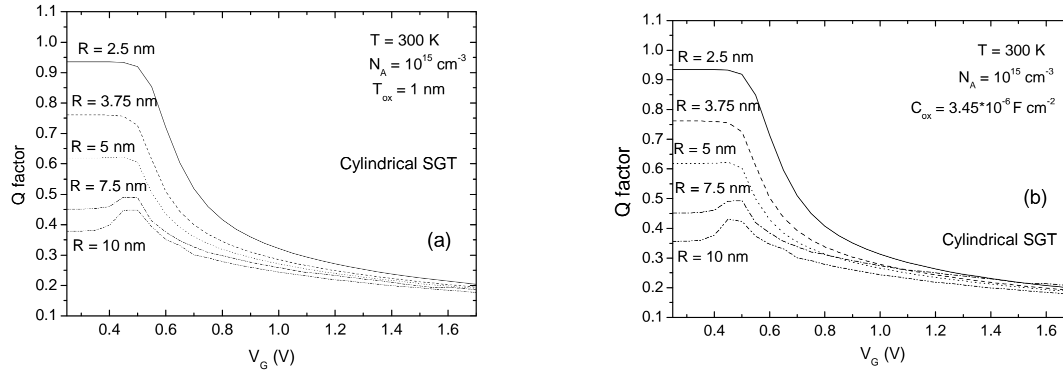


Figure 83. Cylindrical SGT Q factor versus gate voltage (a) $T_{ox} = 1$ nm (b) $C_{ox} = 3.45x10^{-6}$ F/cm^2. R =2.5nm (solid lines), R = 3.75nm (dashed lines), R = 5nm (dotted lines), R =7.5nm (dashed-dotted lines), R =10nm (double dotted-dashed lines).

In the figure above, it can be seen that the geometrical confinement is much higher than in DGMOSFETs. For R = 2.5nm, a size that could be compared to T_{si} = 5nm in DGMOSFETs, a Q factor above 0.9 is achieved with respect to a value of 0.7 for DGMOSFETs (see figure 15). This result is reasonable since the inversion charge in SGTs is quantized in two dimensions; hence a much higher Q factor is expected. At high inversion charges the Q factor (in this operation regime we showed that only ECEs were important in DGMOSFETs with values of 0.11 and 0.16 for T_{ox} =1 nm (T_{ox} = 2 nm) for the Q factor) is also higher. For SGTs a value around 0.2 is achieved in strong inversion. Most important at these high gate voltage values is the fact that the Q factor curves for different radii do not merge as in DGMOFETs (see figure 15). This fact suggests a higher influence of GCEs than in DGMOSFETs, even in strong inversion where only ECEs are supposed to be significant.

For the thicker SGTs a hump can be seen in the Q factor for gate voltages around the threshold voltage. This effect is not seen in DGMOSFETs. The explanation lays on the stronger role played by GCEs in SGTs because of the bidimensionality of quantum confinement. The behaviour of GCEs in the interval of gate voltages where GCEs diminish and ECEs rise (corresponding to the interval where the threshold voltage is to be found) is different to what we found in figure 15 for DGMOSFETs. This different behavior is linked to the way the inversion charge distribution behaves in the volume inversion regime in SGTs, and also to the way the charge moves closer to the semiconductor-insulator interface due to ECEs when the gate voltage is increased. If GCEs are very high (for R values below 7.5nm) this effect can not be seen.

There are no great differences between figures 83a and 83b. The approaches used for a constant oxide thickness, and a constant oxide capacitance do not show important differences. However, a slight difference can be found for the higher radii. Higher values of the Q factor can be found for the case with constant oxide thickness (figure 83a) at low gate voltages. For high gate voltages, slightly higher values for the Q factor can also be observed in these cases. However, in general, these differences are negligible.

In order to shed more light in the previous analysis, we have also considered rectangular SGTs. The inversion charge for several of these SGTs is shown below (the side length of the rectangular cross-section is given in the insets).

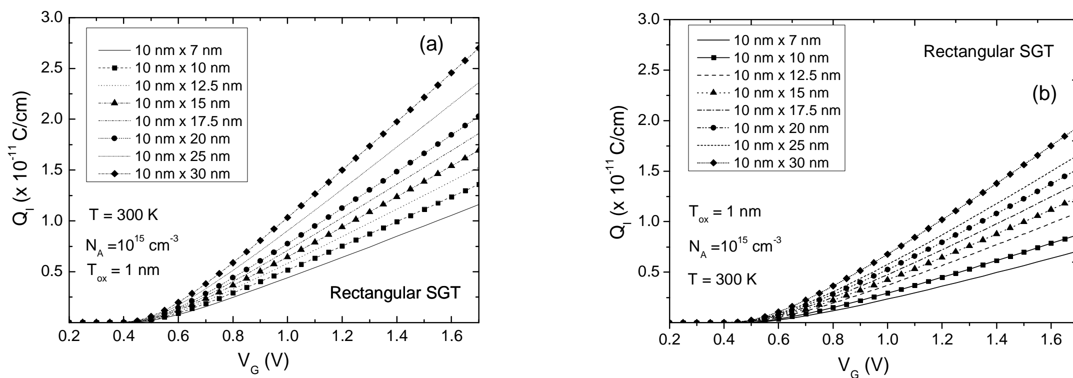


Figure 84. Inversion charge for rectangular SGTs versus gate voltage, T_{ox} = 1 nm. The size of the cross-section is shown in the inset. (a) Classical (b) quantum calculation.

The difference between the classical and quantum charge rise as the size of the rectangle decreases, as expected. In addition, these devices show approximately the same threshold voltages than their cylindrical counterparts. The Q factor is shown below.

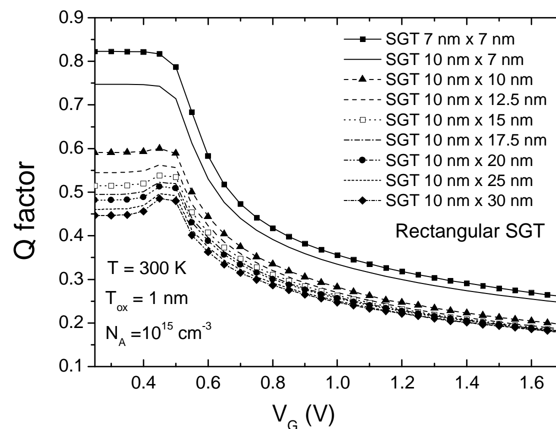


Figure 85. Rectangular SGT Q factor versus gate voltage.

The 10nm x10nm device (comparable to a SGT with R = 5nm) shows a slightly lower Q factor than its cylindrical counterpart (the rounded device presents a lower cross-section area). The hump referenced above in the gate voltage range corresponding to the threshold voltage can also be seen here for the devices with greater cross-section. It is interesting to highlight that at high inversion charges the Q factor for the transistors with the lower cross-section is much higher than the rest. This is not the case for cylindrical SGTs. An explanation for this behaviour can be connected to the fact that the achievement of the strong inversion regime does not make much difference in terms of charge distribution when the areas influenced by the corners of the device (in terms of charge distribution) represent an important portion of the total cross-section.

For the case of DGMOSFETs we studied the range of oxide and silicon thicknesses where quantum effects were needed to correctly model the inversion charge. For SGTs, see the cylindrical SGT with R = 10nm for which the Q factor is the lowest, the Q factor is over 0.2 for all the gate voltages considered, therefore quantum effects would have to be taken into consideration in a general manner in inversion charge models. A similar conclusion can be drawn for rectangular SGTs as can be observed in figure 85.

5.3. Inversion charge centroid for cylindrical SGTs

When the diameter of cylindrical devices shrinks, geometrical quantum confinement effects show up, as in the DGMOSFET case, making the self-consistent solution of the 2-D Poisson and Schrödinger equations essential (see figures 86 and 87).

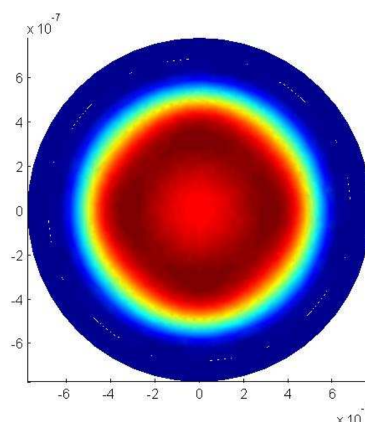


Figure 86. Electron density contour plot in a cross section of a SGT with R = 6.25 nm and T_{ox} = 1.5 nm at room temperature, V_G= 0.6 V

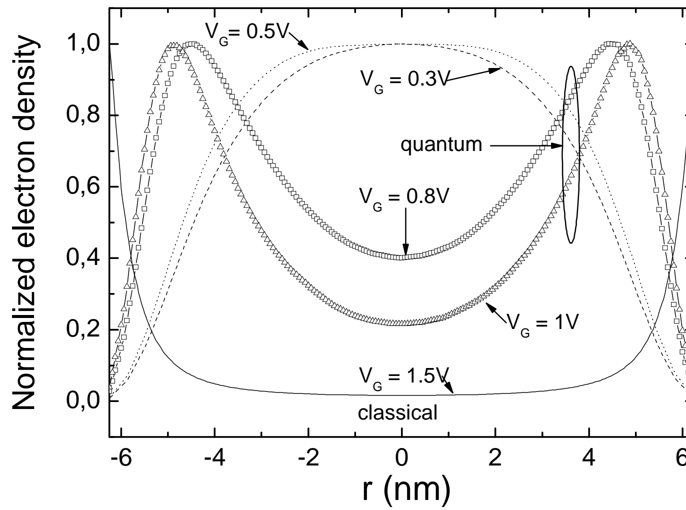


Figure 87. Normalized electron density along the diameter of the silicon section of a SGT with R = 6.25 nm and T_{ox} = 1.5 nm at room temperature for different gate voltages. The classical distribution is shown in solid line (V_G =1.5V), the quantum distributions are plotted (V_G =0.3V dashed line, 0.5V dotted line, 0.8V hollow squares, and 1V hollow triangles).

In the figure above, volume inversion effects are clearly seen when quantum effects are taken into account. Not only the spatial distribution of the charge but also its value depends on the consideration of quantum effects, as shown in figure 88 where the inversion charge versus gate voltage for an SGT with R = 6.25 nm at room temperature is plotted with (solid line) and without (dashed line) the inclusion of quantum effects.

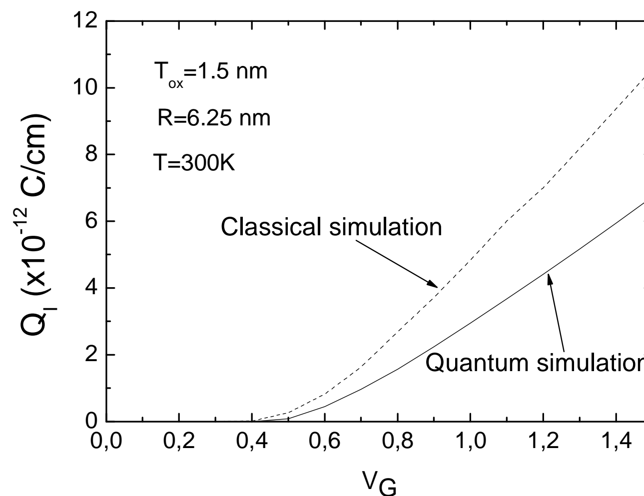


Figure 88. Channel charge (per unit length) of a SGT with R = 6.25 nm at room temperature. The classical (quantum) simulation results are plotted in dashed (solid) line.

It has been shown in the previous section the need to include quantum effects in the inversion charge models, and we have done so using a strategy already successfully applied for DGMOSFETs [Balaguer-2012], where the equations employed for the classical version of the model, particularly the expressions connected with the inversion charge calculation, have been extended to take into consideration quantum confinement effects.

This was carried out by introducing an enhanced oxide capacitance and a modified threshold voltage. The enhanced oxide capacitance was calculated by characterizing the quantum charge distribution in the semiconductor through the determination of the inversion layer centroid, as in the case of the DGMOSFET, which allowed us to account for the oxide interface separation of the inversion charge distribution. The centroid was used to obtain a modified oxide thickness which led us to a more accurate calculation in modeling devices with thin gate oxide layers.

The conventional definition of the inversion layer centroid [Roldán-2001, López-Villanueva-1997] has been adapted to the particularities of the geometry of SGTs [Roldán-2008b]. Firstly, we defined a Δ parameter as follows:

$$\Delta = \frac{\int_0^R \rho(r) r^2 dr}{\int_0^R \rho(r) r dr} = \frac{\int_0^R \rho(r) r^2 dr}{\frac{Q_I}{2\cdot\pi}} = 2\cdot\pi \frac{\int_0^R \rho(r) r^2 dr}{Q_I} \tag{67}$$

where the inversion charge per unit gate length Q_I is calculated in cylindrical coordinates, assuming that the inversion charge density is not dependent on the rotation angle,

$$Q_I = 2\cdot\pi \int_0^R \rho(r) r dr \tag{68}$$

Second, the inversion charge centroid z_I calculation is performed as follows:

$$z_I = R - \Delta \tag{69}$$

where R is the radius of the semiconductor cylinder. In order to model these centroid data, we have used the following empirical equation:

$$\frac{1}{z_I} = \frac{1}{a+2bR} + \frac{1}{z_{I0}} \left(\frac{N_I}{N_{I0}(R)} \right)^n \tag{70}$$

where a, b, z_{I0}, and n are constants independent on the bias, and N_I ($N_I = Q_I/2\pi Rq$) is the electron density per unit area. We calculated the inversion charge centroid making use of our simulator; the results are plotted using solid lines in figure 89, and the analytically obtained data using equation 70 are shown in symbols. The centroid shows the expected behavior; it can be seen that its value decreases as the inversion charge increases since the charge distribution shifts toward the Si/SiO_2 interface.

The model reproduces correctly the centroid values obtained for SGTs with different radii and for the gate voltage range employed in figure 89.

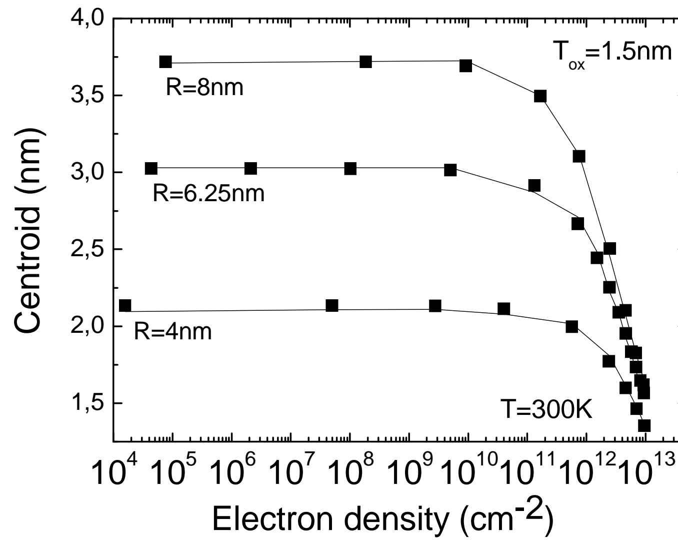


Figure 89. Inversion charge centroid for a SGT at room temperature with R= 4, 6.25, 8nm. The simulation results obtained including quantization are plotted in lines, the data obtained making use of the previously described model are plotted in solid squares.

The parameters used to fit the simulation data are the following: a = 0.55 nm, b = 0.198, z_{I0}=5.1 nm, n = 0.75, and

$$N_{I0}(R) = 8.26\times10^{12} cm^{-2} - 4.9\times10^{18} cm^{-3} \cdot R(cm) \tag{71}$$

The centroid model has been validated for the range of radii used in this work (diameter ≤ 16 nm). The threshold voltage of the SGTs simulated has also been corrected to account for the shift that takes place in this parameter when quantum effects are taken into account [Tsutsui-2005, Uchida-2001]. We calculated the energy values (calculated as $q\Delta V_{TQM}$) associated with the threshold voltage difference obtained for different SGTs (shown in figure 90 in hollow triangles), making use of the simulated classical and quantum inversion charge versus gate voltage curves (see figure 88). The threshold voltage was obtained by calculating the second derivative maximum of the inversion charge as a function of the applied gate voltage curves.

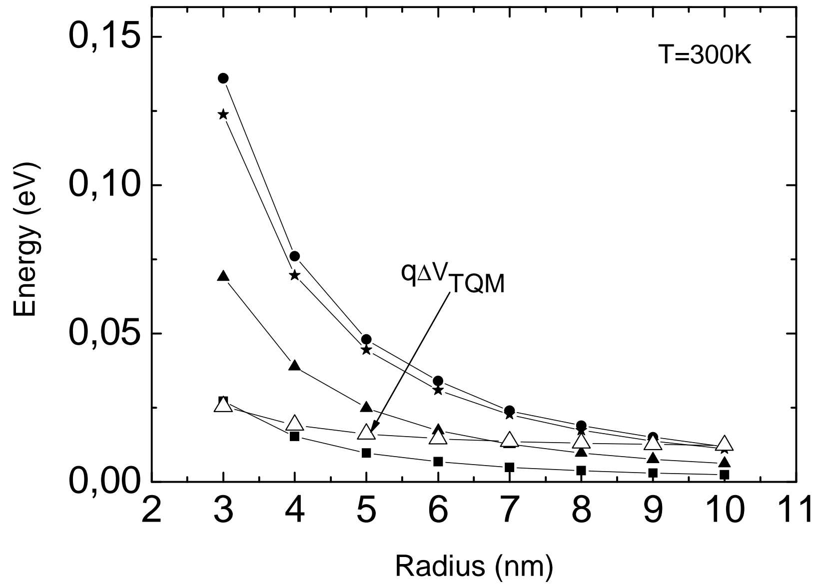


Figure 90. Energy values connected with the threshold voltage shift obtained by comparing the classical and quantum charge simulations versus SGT radius (hollow triangles). Energy levels (energy eigenvalues of Schrödinger equation in cylindrical coordinates for a SGT) versus radius are plotted in solid symbols. The lower energy levels obtained using the longitudinal effective mass in Schrödinger equation associated with the zero (first) [second]-order Bessel function of the first kind are plotted in solid squares (triangles) [stars], respectively. The lower energy level obtained using the transversal effective mass is in solid circles.

These data are modeled by using an empirical fitting term ΔV_{TQM} that is given in the following expression,

$$\Delta V_{TQM} = 0.011V + \frac{1.3 \cdot 10^{-15} V \cdot cm^2}{R^2} \qquad (72)$$

A good agreement is achieved. For the sake of comparison, the lower energy levels obtained from an analytical solution of the Schrödinger equation in a cylindrical structure such as an SGT (see [Gnani-2004]) are also shown. The mathematical expression for these energy levels is given by

$$E_{m,n,k}^{(0)} = \frac{\hbar^2 \mu_{m,n}^2}{2m_k^* R^2} \tag{73}$$

The zero superscript indicates the use of a null potential energy in the Schrödinger solution. The wave functions are obtained by means of Bessel functions of the first kind and order m ($J_m(x)$), so $\mu_{m,n}$ is the n-th zero of $J_m(x)$, and m_k^* is the effective mass normal to the oxide interface. It can be seen in equations 72 and 73 that there exists a R^{-2} dependence in both cases, as would be expected. The extracted energy values can be found between the second and third lowest energy levels for the higher radius structures and between the first and second energy levels for the shorter radius devices. In this respect, it is important to highlight that the lower energy level has been used, as a general rule, as a reference of the conduction band minimum shift (ΔE_C) produced by quantum effects. However, we show (see figure 90) here that the ΔE_C needed to obtain the extracted energy values connected with the threshold voltage variation is higher. These results make sense since electrons are found in several subbands with different energies, and therefore, ΔE_C should represent an average of the lower energy levels where electron charge can be found.

5.4. Inversion charge including quantum effects.

Making use of the new centroid model developed in the precedent section, we have improved a classical inversion charge model [Iñiguez-2005] to include quantum effects. With this in mind, we focused our study on the influence of separating the inversion charge distribution from the oxide interface, estimating a new and (from the modeling viewpoint) more realistic oxide thickness. The results obtained led us include a correction in the oxide capacitance. In particular, the classical oxide capacitance has been replaced by another, where the capacitance of the oxide layer is in series with the capacitance of a silicon layer; the thickness of which corresponds to the value of the inversion charge centroid. The new total capacitance can therefore be calculated as

$$\frac{1}{C_{Total}} = \frac{1}{C_{ox}} + \frac{1}{C_{Semiconductor}} \tag{74}$$

where C_{ox} is the well-known value of a cylindrical capacitor with external radius equal to ($R + T_{ox}$) and internal radius equal to R. The oxide capacitance is calculated by means of the expression 66 and the semiconductor capacitance is calculated using the following expression:

$$C_{Semiconductor} = \frac{\varepsilon_{Si}}{(R - z_I)\ln\left(1 + \dfrac{z_I}{R - z_I}\right)} \tag{75}$$

where ε_{Si} is the silicon permittivity.

The starting point for the calculation is an initial guess of the inversion charge that we call Q' [Iñiguez-2005].

$$Q' = C_{ox}\left(-\frac{2C_{ox}V_{th}^2}{Q_0} + \sqrt{\left(\frac{2C_{ox}V_{th}^2}{Q_0}\right)^2 + 4V_{th}^2\ln^2\left(1 + \exp\left(\frac{V_{GS} - V_0 - V}{2V_{th}}\right)\right)}\right) \tag{76}$$

where $V_{th} = kT/q$, V_{GS} is the gate–source voltage, and V is the channel potential (V = 0 at the source; all our calculations are performed at this point). The expressions for V_0 and Q_0 are given below:

$$Q_0 = \frac{4\varepsilon_{Si}}{R}\frac{kT}{q} \qquad V_0 = \phi_{MS} + \frac{kT}{q}\ln\left(\frac{8}{\delta R^2}\right) \qquad \delta = \frac{q^2 n_i}{kT\varepsilon_{Si}} \tag{77}$$

where n_i is the intrinsic carrier concentration, ϕ_{MS} is the metal-semiconductor work-function difference, and q is the electronic charge.

The inversion charge in equation 76 is used to calculate the threshold voltage V_T and ΔV_T, which are to be included in the final expression of the inversion charge. Note that the quantum threshold voltage shift modeled in the previous section is introduced in the V_T calculation described below

$$V_T = V_0 + 2V_{th} \ln\left(1 + \frac{Q'}{Q_0}\right) + \Delta V_{TQM} \qquad \Delta V_T = \frac{\left(\frac{2C_{Total}V_{th}^2}{Q_0}\right)Q'}{(Q_0 + Q')} \tag{78}$$

At this point, it is interesting to highlight the use of C_{Total} in equations 78 and 79. If C_{Total} is substituted for C_{ox}, the classical charge model is recovered. C_{Total} is calculated by introducing $Q'/q = N_I$ in equation 70 to calculate the inversion charge centroid. Then, the semiconductor capacitance (equation 75) is calculated to obtain finally C_{Total} (equation 74). The threshold voltage V_T and ΔV_T are calculated using Q' ((equation 76), which is an inherent part of the equation set developed in [Iñiguez-2005]) to obtain the final inversion charge which is calculated as follows.

$$Q = C_{Total}\left(-\frac{2C_{Total}V_{th}^2}{Q_0} + \sqrt{\left(\frac{2C_{Total}V_{th}^2}{Q_0}\right)^2 + 4V_{th}^2 \ln^2\left(1 + \exp\left(\frac{V_{GS} - V_T + \Delta V_T - V}{2V_{th}}\right)\right)}\right) \tag{79}$$

We have used the model described in the previous section to reproduce the simulation data obtained for SGTs of different sizes with the following technological parameters: $N_A = 10^{10}$ cm^{-3} and T_{ox} = 1.5 nm. The simulation results are shown in solid lines in figure 91, while symbols represent the inversion charge data obtained analytically by means of equation 79. For the sake of clarity, the data are plotted in Coulomb per centimetre since the curves in Coulomb per square centimetre crossed over for the considered SGTs. For this reason, we changed from one to another, applying the Gauss law, i.e., dividing by $2\pi R$. A good fit was achieved.

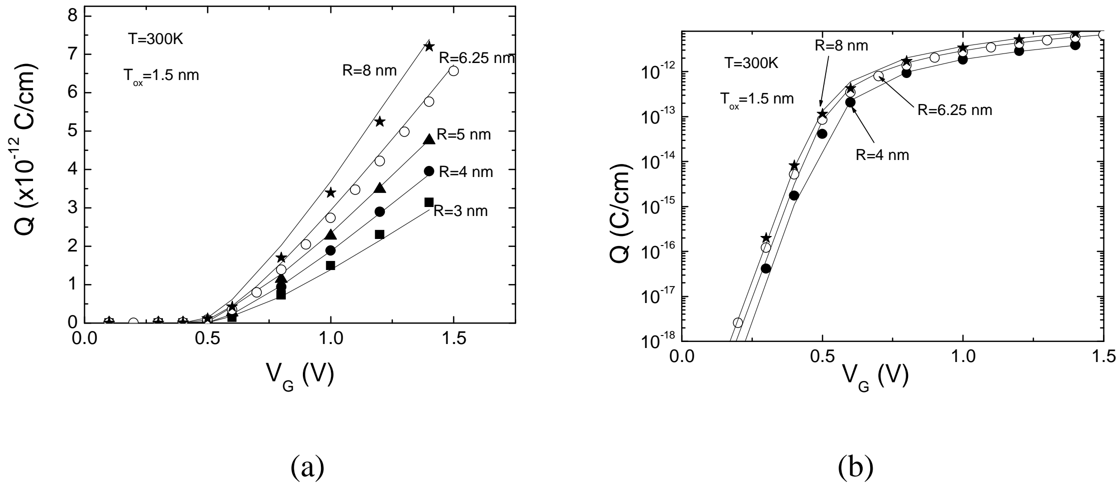


Figure 91. Channel charge (per unit length) at the source (V=0) of several SGTs at room temperature (R=3, 4, 5, 6.25, 8 nm). The simulation results, obtained taking quantum effects into account, are plotted in solid lines; the modeled data are shown in solid squares.

The simulation data obtained by the self-consistent solution of the 2-D Poisson and Schrödinger equations are reproduced correctly for a wide range of radius and gate voltage values. The main characteristics of the model and what makes it important from the compact modeling point of view is that it presents simple mathematical equations and an explicit calculation scheme that can easily be extended for the calculation of the drain current.

5.5. Inversion charge in cylindrical SGTs with high-κ dielectrics

As we already pointed out in the introduction of this chapter, in this section we have extended the model presented above [Roldán-2008b] by introducing high-κ dielectric materials as the insulator of SGTs instead of SiO_2. To do so, a model for the inversion charge centroid, based on the model developed in the previous section, has been introduced. Among several high-κ dielectric materials we have focused on HfO_2 as gate insulator. The results obtained with the model have been compared to simulation data provided by a self-consistent solution of the 2D Poisson and Schrödinger equations (section 2.4). It will be seen that the model reproduces correctly the inversion charge centroid data of several SGTs with different values of the silicon radii (4, 6.25 and 8 nm) and values of the HfO_2 effective mass in the range of m^*/m_0

[0.1-0.7]. Making use of the centroid developed for HfO_2 as gate insulator, the inversion charge including quantum effects has also been calculated [Balaguer-2009].
It has been remarked in the first chapter that high-κ materials will be used as gate insulators to allow the continuous scaling process [Colinge-2008, Huff-2005, Chiu-2006, Nazarov-2011]. They facilitate an increase of the insulator physical thickness and the reduction of parasitic tunneling currents. In the present case, since the potential barrier height of the HfO_2/Si interface (ΔE_C = 1.5 eV) is much lower than in the conventional SiO_2 (ΔE_C = 3.1 eV), the penetration of the wave functions in the insulator of HfO_2/Si structures is higher and, consequently, the influence of the insulator electron effective mass on the silicon inversion charge distribution rises. The electron effective mass in HfO_2 is not well defined as reported in [Chiu-2006]; in fact, values that range from $0.1m_0$ to $0.7m_0$ can be found in the literature. This dispersion of the insulator electron effective mass values, as well as the dispersion in the reported conduction band offset values, could be linked, as suggested in [Chiu-2006], to the thin film characteristics as well as the way it is grown (leading to amorphous or polycrystalline thin films). In this context, an inversion charge centroid model dependent on the insulator electron effective mass is very interesting.
The simulation data presented have been obtained using the simulator described in section 2.4 [Godoy-2007a]. The technological parameters were the following: an undoped substrate ($N_A=10^{12}$ cm^{-3}), a midgap metal gate and an oxide thickness of 1.5 nm. The penetration of the wave functions within the insulator is taken into account; this is known to be an important issue [Haque-2002]. Although both the oxide effective mass and the potential barrier height (ΔE_C = 1.5 for the silicon/HfO_2 interface) are essential parameters to obtain the correct inversion charge distribution in the device [Tienda-Luna-2008]; there is a lot of controversy about the effective mass in HfO_2 and this parameter is not well defined in the literature since different values have been tabulated [Chiu-2006]. In this work we have used a range of values of the HfO_2 effective mass from $0.1m_0$ to $0.7m_0$, which are considered to be the effective mass limiting values [Chiu-2006].

In order to model the centroid of the inversion charge we have used, as a starting point, the empirical equation presented previously in section 5.3 for conventional SGTs with SiO_2 as gate dielectric (equation 70). As already detailed before, z_I is the position of the inversion charge centroid calculated from the insulator-semiconductor interface making use of the equations 67 and 69 already described in section 5.3.

As the aim of this work is the generalization of this model when a high-κ material is used as a gate dielectric instead of SiO_2, in particular, we will focus on HfO_2 in the forthcoming part of the section. Firstly, the centroid of the inversion charge of SGTs with different silicon radii has been calculated by simulation following the procedure sketched in [Roldán-2008b]. In order to check the appropriateness of an empirical expression such as (70) we have simulated several SGTs with different oxide thicknesses and values of the relative permittivities k.

The results are shown in figure 92. As can be seen, the simulated centroid neither depends on the oxide thickness nor on the relative permittivity; it just shows a strong dependence on the inversion charge density (the same gate insulator effective mass has been used for all the curves shown in this figure). Therefore, the use of equation 70 as a starting point for the modeling of the inversion charge centroid is coherent; see that T_{ox} and k are not included as parameters in (70).

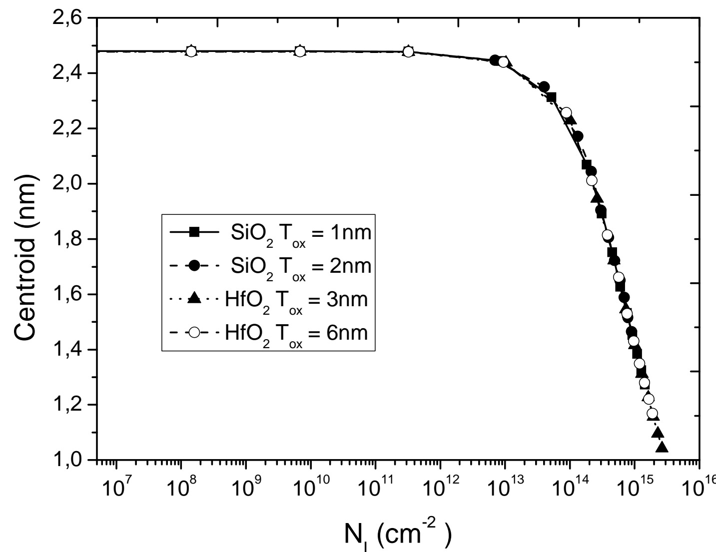


Figure 92. Simulated inversion charge centroid versus inversion charge for different values of the oxide thickness T_{ox} and relative permittivity k.

A new step forward in our scheme was the simulation of the centroid of SGTs with HfO_2 as gate insulator for different silicon radii (R = 4 nm, 6.25 nm, 8 nm) and different values of the insulator effective mass. With these data we modified the inversion charge centroid equation presented in [Roldán-2008b] (equation 70) to account for the insulator electron effective mass variation. The parameters used in this case were the following: n = 0.8, b = 0.1975 and z_{I0} = 5.5×10^{-7} cm.

The parameter "a" shows a clear dependence on the effective mass of the HfO_2 ($m^* = [0.1-0.7] \times m_0$), their value has been fitted with the following equation:

$$a(m^*) = 0.55 - 0.36(m^* / m_0 - 0.1) \qquad (80)$$

The parameter N_{I0} depends on the SGT radius as follows:

$$N_{I0}(R) = 8.26x10^{12} cm^{-2} - f(R)R \qquad (81)$$

where the function f(R) is calculated using the following expression:

$$f(R) = \left[3x10^{18} + 6.66x10^{24}(R - 4x10^{-7})\right] cm^{-3} \qquad (82)$$

In order to obtain a centroid model that correctly fits the simulation data for a wide range of inversion charges and especially in strong inversion, a new factor has been included depending on the effective mass of the gate insulator that multiplies N_{I0}, which is calculated making use of the following expression:

$$c(m^*) = -0.417x(m^* / m_0) + 1.13 \qquad (83)$$

Finally, the new centroid model is calculated as follows:

$$\frac{1}{z_I} = \frac{1}{a(m^*) + 2bR} + \frac{1}{z_{I0}} \left(\frac{N_I}{c(m^*) N_{I0}(R)} \right)^n \qquad (84)$$

Using this new expression developed for the inversion charge centroid we were able to reproduce simulation data for different silicon radii (R = 4 nm, 6.25 nm, 8 nm) [Balaguer-2009]. The results are plotted in the following figures.

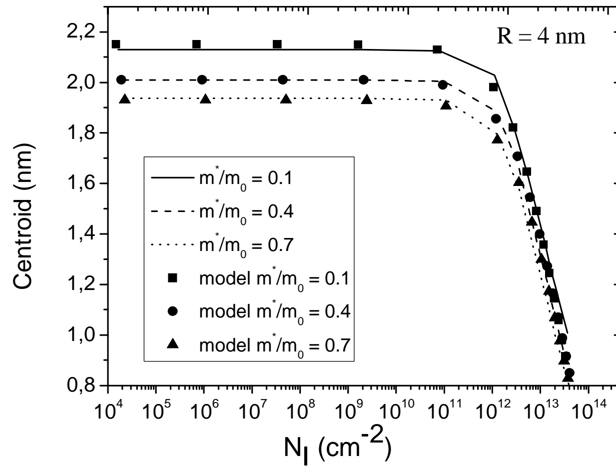


Figure 93. Inversion charge centroid for a SGT with R = 4 nm versus inversion charge density at room temperature. Simulation results are shown in lines and modeled data in symbols.

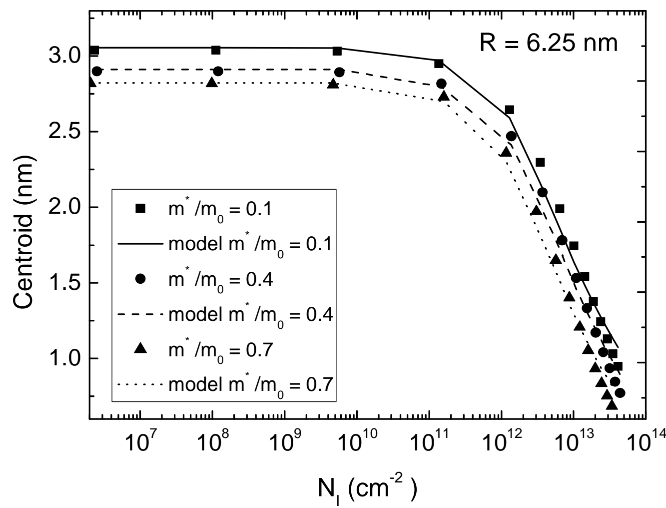


Figure 94. Inversion charge centroid for a SGT with R = 6.25 nm versus inversion charge density at room temperature. Simulation results are shown in lines and modeled data in symbols.

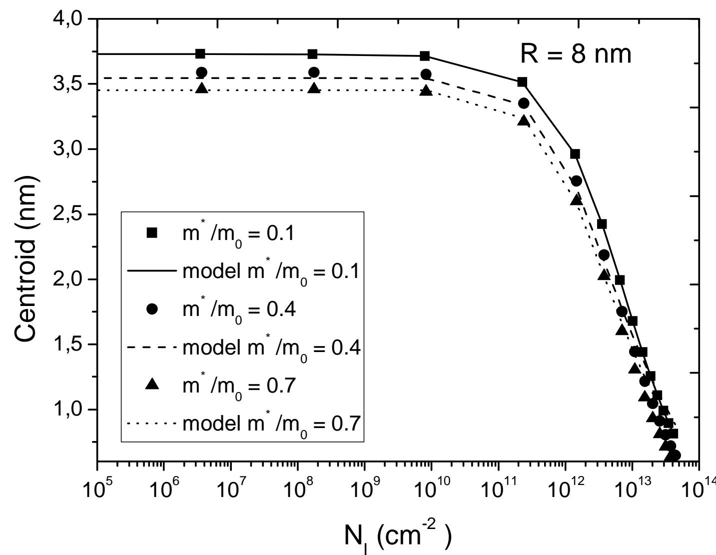


Figure 95. Inversion charge centroid for a SGT with R = 8 nm versus inversion charge density at room temperature. Simulation results are shown in lines and modeled data in symbols.

Figure 93 shows the inversion charge centroid in a SGT with a radius of 4 nm for different values of the HfO_2 effective masses versus inversion density. The simulation data are plotted in lines and the modeled data obtained using equation 91 are plotted in symbols. Similar data for SGTs with R = 6.25 nm are plotted in figure 94 and for R = 8 nm in figure 95. A good fit of the simulation data can be observed in all cases both at weak and strong inversion [Balaguer-2009].

We have also calculated the inversion charge using the model previously developed and described in equation 79 and the new centroid model that considers HfO_2 as gate dielectric. The model allowed us to reproduce simulation data for SGTs of different radii and different values of the insulator gate effective mass ($m^* = [0.1\text{- } 0.7] \times m_0$), assuming an undoped substrate. In figures 96, 97 and 98, the inversion charge in SGTs versus gate voltage is represented for radii of 4 nm, 6.25 nm and 8 nm respectively. Simulation data are plotted in lines and model data are plotted in symbols, as before.

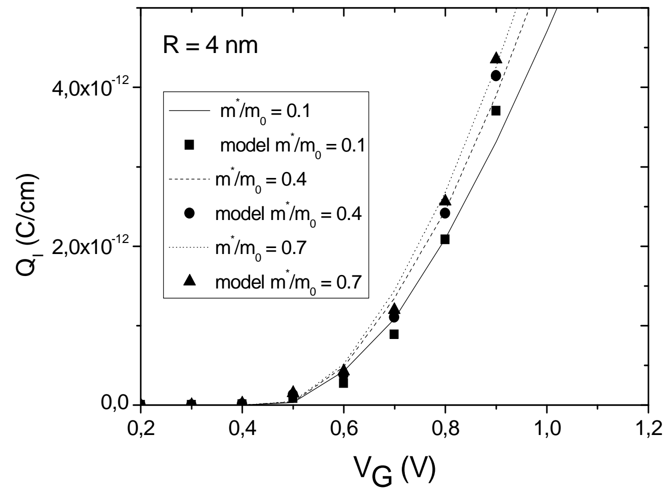


Figure 96. Channel charge (per unit length) at the source for a SGT with R = 4 nm versus gate voltage at room temperature. The simulation results are plotted in lines and the modeled data in symbols.

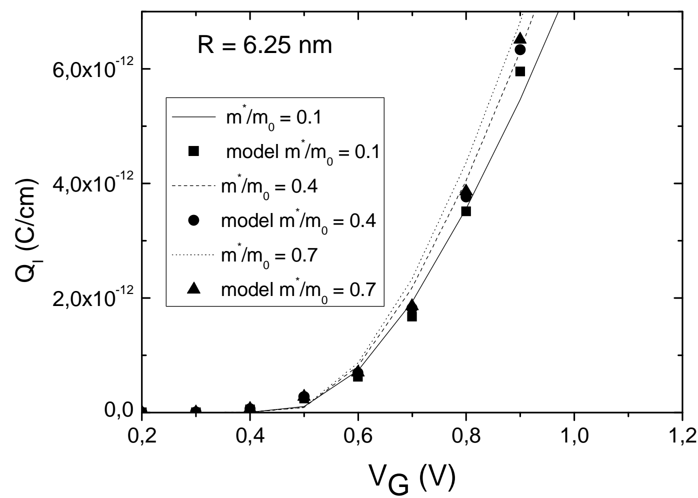


Figure 97. Channel charge (per unit length) at the source for a SGT with R = 6.25 nm versus gate voltage at room temperature. The simulation results are plotted in lines and the modeled data in symbols.

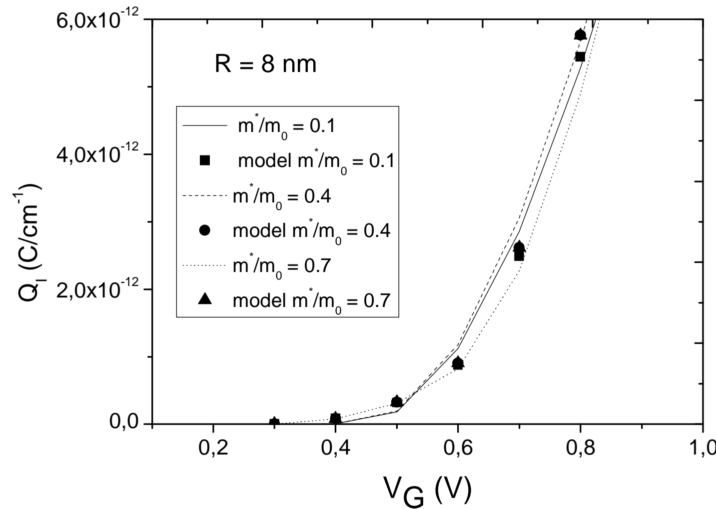


Figure 98. Channel charge (per unit length) at the source for a SGT with R = 8 nm versus gate voltage at room temperature. The simulation results are plotted in lines and the modeled data in symbols.

As can be seen, the inversion charge calculated using the model fits reasonably well the simulation data [Balaguer-2009]. It is important to highlight that for the thinnest SGTs (figure 96) the influence of HfO_2 effective mass on the inversion charge centroid is higher. This fact is due to a greater structural confinement of the inversion charge, even at low electron charge densities, that produces a higher penetration of the wave functions in the gate oxide. Through the results obtained in this section we have also demonstrated the validity of the inversion charge model of the previous section when changing some device characteristics like the material used as gate dielectric.

5.6. Mobility characterization SGT

This section is devoted to the low-field mobility characterization and modeling of cylindrical SGTs. In section 3.6 we already presented a study to characterize the different low-field mobility components for DGMOSFETs; in line with it, we present this study for cylindrical SGTs. Phonon and surface-roughness mobility components will be analyzed and modeled, as in chapter 3. The mobility model we present here is analytical and explicit therefore, following the general approach used along this manuscript, it can be used in circuit simulators integrated with already existing SGT compact models [Moldovan-2007b, Roldán-2008b, Jiménez-2004, Gnani-2004] where the description of the inversion charge and drain current is implemented.

The model developed has been compared to a set of mobility curves with different geometrical features and surface-roughness characteristics obtained by means of a state-of-the-art simulator that accounts for phonon and surface-roughness scattering [Ruiz-2011, see also section 2.4 in this document]. As a reminder, it is important to highlight that the simulator includes an adaptable grid in order to characterize correctly the geometry of the SGTs considered; for the inversion charge calculation a self-consistent 2D solver for Schrödinger and Poisson equations in the transversal cross-section of GAA square devices under the effective mass approximation is used [Tienda-Luna-2008]. This approximation is accurate enough for electrons in wires of the size simulated for this work [Bescond-2007, Wang-2005]. Both, electrons and holes are included in the Poisson equation although only electrons are treated from a quantum point of view. For the mobility calculation (phonon and surface-roughness scattering mechanisms are included), for a given subband i, we have used the Kubo-Greenwood formula [Kubo-1957]:

$$\mu_i = \frac{2e}{k_B T n_i m_{eff}} \int g_i(E)(E - E_i)\tau_i f(E)(1 - f(E))dE \tag{85}$$

where n_i is the population, m_{eff} is the effective conduction mass, g_i is the density of states, τ_i is the relaxation time of the subband i and f(E) is the Fermi distribution function. The effective mobility is obtained by a summation over the three doubly degenerated Si valleys and over all contributing subbands.

Both acoustic and optical phonons are considered in this study. The relaxation time for the acoustic phonon scattering is calculated as follows:

$$\frac{1}{\tau_{ij}^{AC}(E)} = \frac{d_j 4\pi D_{la}^2 k_B T}{g_\alpha \rho_{Si} \hbar c_{la}^2 W_{ij}} g_j(E) \tag{86}$$

where d_j and g_α are the degeneracy factors of the j-th subband and the α valley respectively. D_{la} is the deformation potential, ρ and c are the density and longitudinal sound velocity of silicon respectively. g_j (E) is the density of states of the j-th subband and W_{ij} is the overlap integral calculated as

$$\frac{1}{W_{ij}} = \int \psi_i^2(x, y)\psi_j^2(x, y)dxdy \tag{87}$$

On the other hand, the relaxation time for inter-valley optical phonon scattering is given by

$$\frac{1}{\tau_{ij}^{OP}(E)} = d_j \frac{2\pi D_k^2 \hbar}{\rho E_k W_{ij} g_\alpha} \left(N_k + \frac{1}{2} \pm \frac{1}{2} \right) g_j(E) \frac{1 - f(E \mp E_k)}{1 - f(E)} \tag{88}$$

where, D_k, E_k and N_k are the deformation potential, energy and occupancy number of optical phonons respectively. The plus and minus signs correspond to the phonon absorption and emission process.

To calculate the surface-roughness mobility the method developed in [Tienda-Luna-2011] was used, which is a generalization for arbitrarily oriented devices with 2D confinement of the method proposed in [Jin-2007a] for thin films, was used. Besides, it was assumed that the power spectrum of the interface random roughness follows an exponential model characterized by the parameters Δ and L_{sr} [Goodnick-1985] which are the rms value and correlation length of the surface roughness, respectively.

The devices under study are cylindrical SGTs with different radii going from 8 nm to 15 nm, a gate insulator 1 nm thick and a mid-gap metal gate (ϕ_m = 4.61 eV). Phonon and surface-roughness limited mobility components (isolated by using Matthiessen's rule) were modeled separately and finally merged again by Matthiessen's rule. Regarding the application of Matthiessen's rule, we must remark that the comments highlighted in section 3.6 hold also here [Stern-1980, Fischetti-2002, Esseni-2011, Driussi-2009].
Following a procedure similar to the one used in section 3.6, we have modelled, as a first step, the phonon mobility component according to [Roldán-2003, Jiménez-Molinos-2008] employing the phonon limited mobility model developed in [Gámiz-1995], where the temperature was fixed at T=300 K,

$$\frac{1}{\mu_{ph}(N_{inv})} = \frac{1}{\mu_{ph0}\beta(T_{Si})} \left[1 + \left(\frac{N_{inv}}{N_{inv0}} \right)^{\delta(T_{Si})} \right] \tag{89}$$

where N_{inv} is the electron density in the device channel, $N_{inv0} = 9 \times 10^{12}$ cm^{-2} and $\mu_{ph0} = 470$ cm^2/Vs are constants and $\beta(T_{Si})$ and $\delta(T_{Si})$ are fitting parameters that only depend on T_{Si} and can be calculated using the following expressions:

$$\beta(T_{Si}) = 0.9 + \frac{1}{8.5}\sqrt{T_{Si} - 5} \tag{90}$$

and

$$\delta(T_{Si}) = 0.35 + \frac{1.55}{(T_{Si} - 5)^{0.4}} \quad (91)$$

In both expressions T_{Si} is given in nm. In figure 99, simulation data (symbols) and the modeled data (lines) are depicted. It can be seen that a good fit is obtained for different SGTs with different radii. In this figure it can be observed that the phonon limited mobility decreases as T_{Si} is reduced due to the increase of the structural confinement of the inversion charge, and the resulting increase in the phonon scattering probability (see figure 4 in refernce [Godoy-2007b]).

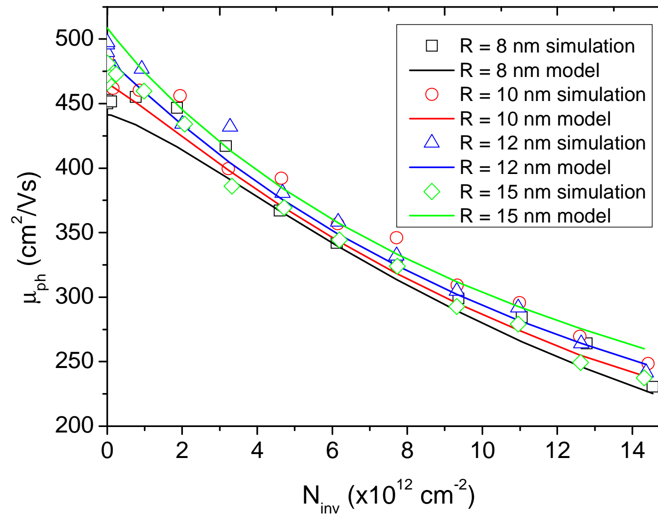


Figure 99. Phonon limited mobility for cylindrical SGTs with different radii. Solid lines (symbols) are used for the modeled (simulated) results.

The surface-roughness mobility component has been extracted from the total mobility curves by means of Matthiessen's rule ($1/\mu_{sr}=1/\mu_{total}-1/\mu_{ph}$). The analytical expression used for modeling this component is given below (in line with [Roldán-2003, Tienda-Luna-2012]),

$$\mu_{sr}(N_{inv}, T_{Si}) = \frac{A(T_{Si}, \Delta)}{N_{inv}^{1.51}} \quad (92)$$

A minimization procedure has been followed to obtain the empirical equation for the A function given below for the three different values of the surface-roughness parameter (Δ= 0.5 nm, Δ= 0.35 nm and Δ= 0.2 nm) considered, where T_{Si} is given in nm.

$$A(T_{Si}, \Delta) = \left[\left(3 + 6.10^{6}\left(|\Delta - 0.7|\right)^{2.7}\right) + 15.10^{4}\left(0.18 + \left(10|\Delta - 0.7|\right)^{6}\right)(T_{Si} - 5)\right]10^{22} \quad (93)$$

We have reproduced the simulated data for the total mobility simulated data well making use of the previous expressions, as it can be seen in figure 100. The errors are in a reasonably range for all the electron densities and for all device sizes and surface roughness considered. The final total mobility has been obtained by Matthiessen´s rule including the phonon (equation 89) and surface-roughness (equation 92) mobility components. The results are shown in figure 100 for different values of the radius and surface-roughness parameter Δ.

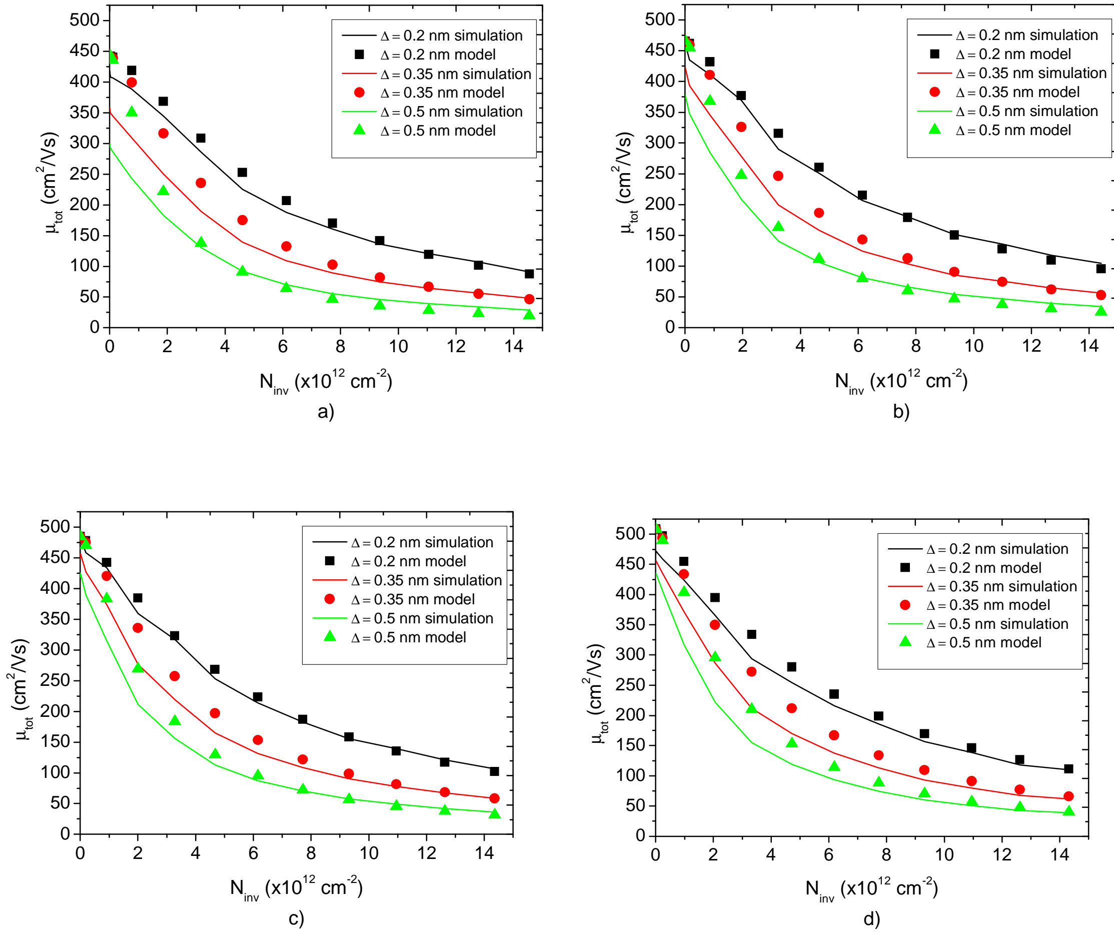


Figure 100. Total mobility (phonon and surface-roughness scattering mechanisms are considered) for (a) R=8nm, (b) R=10nm, (c) R=12nm and (d) R=15nm cylindrical SGTs. Solid lines are used for the simulation results while symbols represents the analytical model. Different parameters for the surface roughness have been used.

As can be seen, the simulation data is correctly reproduced by the model for all the devices and operation regimes considered.

6. Conclusions

The main goal of this thesis was the development of advanced models for different multi-gate devices; on the one hand conventional multi-gate devices like DGMOSFETs and SGTs and on the other hand novel structures like Schottky Barrier (SB) MOSFETs, in particular for this latter case, we chose SB DGMOSFETs. The models developed are based mainly on explicit analytical expressions that can be easily implemented in circuit simulators. In this respect, the new contributions presented here can be incorporated easily in a wider compact model.

Due to the limitations in the availability of experimental data, the models presented in the different sections have been validated by means of numerical data obtained from state-of-the-art simulators developed in our research group (The nanoelectronics research group at the University of Granada) in most cases, and also by means of commercial simulators, such us ATLAS (Silvaco) for the SB DGMOSFETs.

An important feature to highlight about the multi-gate MOSFET models introduced is the exhaustive inclusion of quantum effects on the inversion charge calculation. The geometries of the devices considered throughout the manuscript made it necessary since, in addition to electric confinement effects, structural confinement effects are very important. One of the most representative parts of this work has been dedicated to the study of these effects and the circumstances when they need to be included in the models. This fact was deeply explained at the beginning of chapter 3 for DGMOSFETs. In the characterization of low-field mobility quantum effects have also been deeply considered.

Among the main results and studies obtained the following can be counted:

-We analyzed the inversion charge geometrical and electrical confinement in DGMOSFETs. In the subthreshold region, electrical confinement can be neglected and only geometrical confinement must be taken into account if the silicon layers are thinner than 20 nm, otherwise it can also be neglected. Electrical confinement effects are only important above threshold, but they do not have to be considered if oxide layers are thicker than 2 nm. We obtained these results by representing the Q factor for a wide range technological data and bias voltages.

-A complete inversion charge model for DGMOSFETs accounting for quantum effects, for n-type and p-type devices and for different substrate crystallographic orientations has been developed. The inclusion of quantum effects is implemented by enhancing the oxide capacitance including the role of the inversion charge centroid and its derivative. The differences found for the usual substrate crystallographic orientations lead to different

inversion charge distributions. In all cases, the inversion charge models have been validated making use of simulation data and obtaining a good fit for all the cases considered.

-Another important topic was related to the mobility characterization in DGMOSFETs. Monte Carlo simulations were used to analyze how Coulomb and surface-roughness scattering affect the low-field mobility. Single-gate MOSFETs were also studied as a first step. For both type of devices we performed large number of simulations for different geometrical structures and densities of interfacial charged centers at the silicon-oxide interface and we came to the conclusion that for both devices the Coulomb-limited mobility due to charges (at both interfaces) can be calculated by adding the contribution of each interface using Matthiessen's rule. The DGMOSFET mobility characterization was complemented with the analysis of surface-roughness scattering. It was shown that the curves corresponding to the thickest silicon films tend to merge because electric field confinement predominates over structural confinement, making less influent the silicon thickness value. For the thinnest structures, volume inversion does not disappear even at high inversion charges, this fact determines the distance between the inversion electrons and the oxide-semiconductor interfaces and, therefore, Coulomb and surface-roughness scattering. Mobility models for this component can be simplified since the roughness of each interface can be calculated using Matthiessen's rule to add the components due to each interface separately.

-An advanced model of the drain current of DGMOSFET was also developed. A previously existing classical model was used to include quantum effects, velocity overshoot and saturation velocity, and short channel effects such us DIBL and channel length modulation. The current model was validated using simulation data obtained from a multisubband Monte Carlo simulator developed within our research group. Two different devices with nanometric dimensions were considered, one of them with HfO_2 as dielectric interface and the other one with SiO_2. In both cases the model reproduced simulation data accurately.

Another important chapter dealt with Schottky barrier devices. In order to maintain the coherence in relation to the multi-gate devices used along this manuscript, Schottky barrier DGMOSFETs have been modeled. The main characteristic from the structural point of view is that traditionally highly-doped drain and source regions are replaced by metal contacts. Consequently, new transport mechanisms appear in addition to drift-diffusion.

-A drain current model has been developed including the tunneling current component that injects carriers into and out the channel through Schottky barriers (source and drain contacts were metallic). For these devices, in particular for SB DGMOSFETs, it was shown that in the

deep subthreshold region the total current is a combination of the diffusion and thermionic emission current.

-In addition, BTBT (band-to-band tunneling) is also important in SB DGMOSFET devices for hole transport characterization. These mechanisms have also been considered.

-The main advantage of the current model presented is that it is explicit, very useful for the compact model community. In this sense, it differs from most of the models published so far for SB MOSFETs (numerical models with iterative algorithms that are not useful in circuit simulators).

- The current model was developed for long channel devices, therefore, no short channel effects were considered. This feature will be studied in the future. The contribution of electrons and holes has been included to calculate the total current which correctly reproduces the ambipolar behaviour of SB MOSFETs. The SB DGMOSFET structure was created and simulated for different values of channel length as well as for different metal workfunctions values for the drain and source contacts. By doing this, we have included the effects connected to image force and dipole barrier lowering. The output characteristics for different gate voltages, as well as the transfer characteristic, were compared with simulation data (obtained with ATLAS), obtaining in all cases a reasonably good fit.

Surrounding gate transistors, SGTs, have also been subject of this thesis. We have developed models in line with those presented for DGMOSFETs.

-An explicit inversion charge model that takes into account quantum mechanical effects making use of a new version of the inversion charge centroid has been developed. The threshold voltage was corrected to model the influence of quantization effects. The model was compared to simulation data for SGTs with different geometries (self-consistently solving the 2D Poisson and Schroedinger equations), obtaining in all cases a good agreement both in the subthreshold and above threshold regions.

-The inversion charge model was generalized to consider high-κ dielectrics as gate insulators instead of the traditionally used SiO_2. The selected material to base the study was HfO_2. The inversion charge model was modified to account for the specific characteristics of high-κ dielectrics. The accuracy of the new model was also checked with simulation data.

-A systematic study of quantum mechanical effects in SGT (both cylindrical and rectangular) was performed. In this case, the Q factor calculated from simulation data was also used to represent the relative influence of confinement effects for different device geometries and operation regimes. For these devices, as expected, the geometrical confinement is higher than

in DGMOSFETs. It was highlighted the need to account for quantum effects in inversion charge models for all the geometries and operation regimes considered.

-A section has also been dedicated to characterize the low-field mobility in SGTs. Models for the phonon and surface-roughness mobility components were introduced and simulated movility curves accounting for these scattering mechanisms were reproduced. Finally a total mobility model was obtained by using Matthiessen's rule that worked well for the mobility curves obtained for different devices were the geometrical, surface roughness and bias conditions were modified.

7. Conclusiones

El principal objetivo de esta tesis ha sido el desarrollo de modelos compactos avanzados para dispositivos multi-puerta. Por una parte hemos estudiado dispositivos multipuerta tradicionales como el transistor MOSFET de doble puerta y el transistor SGT y por otra parte el estudio se ha centrado en nuevas estructuras como el transistor MOSFET de barrera Schottky (SB MOSFET), en particular, para este último caso, nos hemos centrado en el SB MOSFET de doble puerta. Los modelos desarrollados en el presente trabajo están basados principalmente en expresiones analíticas explícitas que pueden ser implementadas fácilmente en simuladores de circuitos. Por esta razón, las nuevas contribuciones presentadas en esta tesis se pueden incorporar fácilmente en otros modelos compactos existentes para crear nuevos modelos más amplios.

Debido a las limitaciones en la disponibilidad de datos experimentales, los modelos presentados en las diferentes secciones se han validado en la mayoría de los casos con la ayuda de datos numéricos obtenidos a partir de simuladores que se han desarrollado recientemente en nuestro grupo de investigación (el grupo de investigación de nanoelectrónica de la Universidad de Granada). Con la misma finalidad, también se han usado simuladores comerciales como ATLAS (Silvaco) para los modelos correspondientes al transistor SB DGMOSFET.

Una caraterística importante a destacar de los modelos de transistores multipuerta presentados es la inclusión de efectos cuánticos en el cálculo de la carga en inversión debido a que las geometrías de los transistores estudiados a lo largo de esta tesis lo hacían necesario. Por esta razón, además de los efectos de confinamiento eléctrico, los efectos de confinamiento estructural han sido tenidos en cuenta. Una de las partes más representativas de este trabajo se ha dedicado al estudio de estos efectos cuánticos y a las circunstancias en las que es necesario incluirlos. Este hecho ha sido explicado con detalle al inicio del capítulo 3 para el caso de transistores MOSFET de doble puerta. Igualmente, en la caracterización de la movilidad de bajo campo, los efectos cuánticos también se han considerado.

Entre los principales resultados y estudios obtenidos, podemos citar los siguientes:

- Se ha analizado el confinamiento eléctrico y geométrico en la carga en inversión para transistores MOSFETs de doble puerta. En la región subumbral los efectos del confinamiento eléctrico se pueden despreciar y sólo habría que tener en cuenta los efectos del confinamiento geométrico si la capa de silicio es menor que 20 nm, por el contrario, si es mayor también se pueden despreciar estos efectos. A través del estudio realizado hemos llegado a la conclusión

de que los efectos del confinamiento eléctrico sólamente son importantes por encima de la tensión umbral, pero no es necesario considerarlos si las capas del óxido aislante son mayores de 2 nm. Estos resultados se han obtenido mediante la representación del factor Q para un amplio rango de datos tecnológicos y voltajes.

- Se ha desarrollado un modelo completo para la carga en inversión de transistores MOSFETs de doble puerta teniendo en cuenta efectos cuánticos, tanto para dispositivos de tipo p como de tipo n con sustratos de diferentes orientaciones cristalográficas. La inclusión de efectos cuánticos se ha implementado a través de una modificación en el cálculo de la capacidad del óxido incluyendo el centroide de la carga en inversión y su derivada. Las diferencias encontradas para las orientaciones cristalográficas usuales nos han conducido a diferentes distribuciones de cargas en inversión. En todos los casos, los modelos de carga en inversión se han validado a través de datos obtenidos por simulación y en todos los casos considerados se ha obtenido un buen ajuste.

- Otro punto importante de este trabajo está relacionado con la caracterización de la movilidad en MOSFETs de doble puerta. Se han usado simulaciones Monte Carlo para analizar cómo el scattering culombiano y por rugosidad superficial afectan a la movilidad de bajo campo. Como paso previo al estudio de transistores de doble puerta, se han estudiado en primer lugar transistores de puerta simple. Para los dos tipos de dispositivos se han realizado un gran número de simulaciones para diferentes estructuras geométricas y distintas densidades de cargas en la interfaz silicio-óxido. A partir de estos datos hemos llegado a la conclusión de que para los dos tipos de dispositivos la movilidad limitada por Coulomb debido a las cargas (en ambas interfaces) se puede calcular sumando las contribuciones de cada interfaz usando la regla de Matthiessen. La caracterización de la movilidad en un transistor MOSFET de doble puerta se ha complementado con el análisis del scattering por rugosidad surperficial. Se ha demostrado que las curvas correspondientes a transistores con capas de silicio más grueso tienden a converger debido al que el confinamiento por campo eléctrico predomina sobre el confinamiento estructural, lo que hace menos influyente el grosor de la capa de silicio. Para las estructuras con silicio más delgado, la inversión en volumen no desaparece incluso para cargas en inversión grandes. Este hecho determina la distancia entre los electrones en inversión y las interfaces óxido-semiconductor y, por lo tanto el scattering coulombiano y por rugosidad superficial. Los modelos de movilidad para este componente se pueden simplificar ya que la rugosidad en cada interfaz se puede calcular haciendo uso de la regla de Matthiessen para añadir los componentes debidos a cada interfaz de manera separada.

- También se ha desarrollado un modelo avanzado de corriente de drenador para un MOSFET de doble puerta. Para esto se ha partido de un modelo de corriente clásico previo al que se le han añadido efectos cuánticos, saturación de la velocidad y efectos de canal corto como el DIBL y la modulación de longitud de canal. El modelo de corriente desarrollado se ha validado con datos de simulación obtenidos a partir de un simulador multisubbanda de Monte Carlo que ha sido desarrollado en nuestro grupo de inestigación. Para validar el modelo se han utilizado dos dispositivos nanométricos con diferentes dimensiones, uno de ellos con HfO_2 como dieléctrico y el otro con SiO_2. En ambos casos el modelo reproduce correctamente los datos de simulación.

Otro capítulo importante de la tesis trata de los dispositivos con barrera Schottky. Para mantener la coherencia con respecto a los dispositivos multipuerta estudiados a lo largo de este trabajo, se han modelado transistores Schottky de doble puerta. La principal característica desde el punto de vista estructural es que las regiones de fuente y drenador tradicionalmente altamente dopadas se han reemplazado por contactos metálicos. Por esta razón hay que tener en cuenta mecanismos de transporte diferentes al de difusión y deriva.
- Se ha desarrollado un modelo de corriente incluyendo una componente de corriente túnel que inyecta portadores dentro y fuera del canal a través de barreras Schottky (los contactos de fuente y drenador son metálicos). Para estos dispositivos, en particular para el transistor SB MOSFET de doble puerta, se ha demostrado que en la región subumbral la corriente total es una combinación de la corriente de difusión y la corriente de emisión termoiónica.
- Además, una corriente de túnel banda a banda (BTBT) es importante en los transistores SB MOSFET para la caracterización del transporte de huecos. Este mecanismo también se ha considerado.
- La principal ventaja del modelo de corriente presentado es que es explícito, muy útil para la comunidad dedicada al desarrollo y uso de los modelos compactos. En este sentido, este modelo difiere de la mayor parte de los modelos publicados hasta ahora para SB MOSFETs (modelos numéricos con algoritmos iterativos que no pueden ser usados en simuladores de circuitos).
- El modelo de corriente presentado en esta tesis ha sido desarrollado para dispositivos de canal largo, por lo que no hemos considerado efectos de canal corto. Esta característica se estudiará posteriormente. Las contribuciones tanto de huecos como de electrones se han tenido en cuenta para el cálculo de la corriente total que reproduce adecuadamente el comportamiento ambipolar de los transistores SB MOSFET. La estructura de transistor SB

MOSFET de doble puerta se ha creado y simulado para diferentes valores de la longitud del canal y diferentes valores de la función trabajo del metal de los contactos de fuente y drenador. Haciendo esto hemos incluido los efectos relacionados con las fuerzas imagen y disminución de barrera por dipolos. Las características de salida para diferentes voltajes de puerta así como la característica de transferencia obtenidos se han comparado con datos de simulación (obtenidas con ATLAS), obteniendo en todos los casos un ajuste razonablemente bueno.

Los transistores SGT también han sido estudio de esta tesis. Se han desarrollado modelos compactos avanzados en la misma línea de los desarrollados para transistores MOSFET de doble puerta.

- Se ha desarrollado un modelo explícito de carga en inversión que tiene en cuenta efectos cuánticos haciendo uso para ello de una nueva versión del centroide de carga en inversión. La tensión umbral se ha corregido para modelar la influencia de los efectos cuánticos. El modelo se ha comparado con datos de simulación de diferentes transistores SGT de distintas geometrías (el simulador resuelve de manera autoconsistente las ecuaciones dePoisson y de Schrödinger), obteniendo en todos los casos un ajuste tanto en la región subumbral como en la región umbral.
- El modelo de carga en inversión se ha generalizado para considerar dieléctricos high-κ como aislante de puerta en lugar del SiO_2 usado tradicionalmente. El material elegido como base para el estudio ha sido HfO_2. El modelo de carga en inversión se ha modificado para tener en cuenta las características específicas de los dieléctricos high-κ. La bondad del nuevo modelo se ha validado con datos de simulación.
- Se ha realizado un estudio de caracterización de los efectos cuánticos en transistores SGT (redondos y rectangulares). En este caso el factor Q calculado a partir de los datos de simulación se ha usado para representar la influencia relativa de los efectos cuánticos por confinamiento debidos a las diferentes geometrías y se ha observado que es más alta que en el caso de los transistores MOSFETs de doble puerta. Se ha remarcado la necesidad de tener en cuenta los efectos cuánticos en los modelos de la carga en inversión para todas las geometrías y los regímenes de operación considerados.
- Se ha dedicado una sección para caracterizar la movilidad de bajo campo en transistores SGTs. Se han introducido modelos para las componentes de movilidad por fonones y rugosidad superficial y se han reproducido curvas simuladas teniendo en cuenta estos mecanismos de scattering. Finalmente, un modelo de movilidad total se ha obtenido usando la

regla de Matthiessen con la que se han obtenido buenos resultados para diferentes dispositivos para los que se ha modificado la geometría, las condiciones de rugosidad superficial y de tensiones aplicadas.

8. Scientific publications

8.1. SCI Journals

"Inversion charge modeling in n-type and p-type Double-Gate MOSFETs including quantum effects: the role of crystallographic orientation", M. Balaguer, J.B. Roldán, L. Donetti, F. Gámiz, Solid State Electronics, 67, pp. 30-37, 2012.

"In-depth study of quantum effects in SOI DGMOSFETs for different crystallographic orientations", M. Balaguer, J.B. Roldán, F.Gámiz, IEEE Transactions on Electron Devices, 58, pp. 4438-4441, 2011.

"An analytical compact model for Schottky-barrier double gate MOSFETs", M. Balaguer, B. Iñiguez, J. B. Roldán, Solid-State Electronics, Vol. 64, No. 1, pp. 78-84, October 2011.

"An in-depth simulation study of Coulomb mobility in ultra-thin body SOI MOSFETs", F. Jiménez-Molinos, J.B. Roldán, M. Balaguer, F. Gámiz, Semiconductor Science and Technology, 25, 055002, 2010.

"Modeling the centroid and the inversion charge in cylindrical surrounding gate MOSFETs including quantum effects", J.B. Roldán, A. Godoy, F. Gámiz, M. Balaguer, IEEE Transactions on electron devices, 55, pp. 411-416, 2008.
Award of the University of Granada to Excellence research work in Technical Science, 2011 edition.

"An in-depth Monte Carlo study of low-field mobility in ultra-thin body DGMOSFETs for modeling purposes", J.B. Roldán, F. Jiménez-Molinos, M. Balaguer and F. Gámiz, submitted for publication for Solid-State Electronics.

8.2. International conference contributions

"An inversion charge model for n-type and p-type DGMOSFETs accounting for different substrate Orientations", M. Balaguer, J.B. Roldán, L. Donetti, F. Gámiz, EUROSOI, 2011

(Seventh Workshop of the Thematic Network on Silicon on Insulator technology, devices and circuits), Granada (Spain), 17-19 January, 2011.

"An in-depth simulation study of Coulomb mobility in Double Gate MOSFETs", F. Jiménez-Molinos, J.B. Roldán, F. Gámiz, L. Donetti, A.M. Roldán, M. Balaguer, EUROSOI 2010 Sixth Workshop of the Thematic Network on Silicon-On-Insulator Technology, Devices and Circuits, Grenoble (France), 25-27 January, 2010.

"An analytical compact model for Schottky-Barrier Double Gate MOSFETs", M. Balaguer, B. Iñiguez, J.B. Roldán, EUROSOI 2010 Sixth Workshop of the Thematic Network on Silicon-On-Insulator Technology, Devices and Circuits, Grenoble (France), 25-27 January, 2010.

"A new inversion charge centroid model for surrounding gate transistors with Hfo2 as gate insulator", M. Balaguer, J.B. Roldán, I. Tienda, F. García Ruíz, A. Godoy, F. Gámiz, C. Sampedro, Spanish conference on electron devices, Santiago de Compostela, 2009.

"In-depth characterization of quantum effects in SOI MOSFETs for modeling purposes", J.B. Roldán, M. Balaguer, F. García-Ruíz, A. Godoy, F. Gámiz, EUROSOI 2008 Fourth Workshop of the Thematic Network on Silicon-On-Insulator Technology, Devices and Circuits, Cork, Ireland, 24-25 January, 2008.

9. References

[Adell-2007] P. Adell, H.J.Barnaby., R.D. Schrimp, B. Vermeire, “Band to band tunneling (BBT) induced leakage current enhancement in irradiated fully depleted SOI devices”, IEEE Transaction on Nuclear Science, Vol. 5, nº 6, pp. 2174-2180, 2007.

[Allibert-2001] F. Allibert, T. Ernst, J. Pretet, N. Hefyene, C. Perret, A. Zaslavsky, S. Cristoloveanu, “From SOI materials to innovative devices“, Solid State electronics, Vol. 45, nº 4, pp. 559-566, 2001.

[Ando-1992] T. Ando, A.B. Fowler and F. Stern “Electronic properties of two-dimensional systems” Rev. Mod. Phys. 54, pp. 437–672, 1982.

[Amara-2009] A. Amara, O. Rozeau, “Planar Double-Gate Transistor - From Technology to Circuit”, Springer, 2009.

[Arora-2007] N. Arora, “MOSFET Modeling for VLSI Simulation. Theory and Practice”, Singapore: World Scientific, 2007.

[Asenov-1998] A. Asenov, “Random dopant induced threshold voltage lowering and fluctuations in sub-0.1 μm MOSFET's: A 3-D “atomistic” simulation study”, IEEE Trans. Electron Devices, Vol. 45, nº 12, pp. 2505- 2513, 1998.

[ATLAS-2010] ATLAS user’s manual, Silvaco International, 2010.

[Auberton-1996] A.J. Auberton-Hervé, “SOI: Materials to systems”, IEEE IEDM Technical Digest, pp.3-10, 1996.

[Auth-1987] C.P. Auth, J.D. Plummer, “Scaling theory for cylindrical, fully-depleted, surrounding gate MOSFETs”, IEEE Electron Device Lett., Vol. 8. nº9, pp. 410-412, 1987.

[Autran-2005] J. L. Autran, K. Nehari, D. Munteanu, “Compact modeling of the threshold voltage in silicon nanowire MOSFETs including 2D-quantum confinement effects”, Molecular simulation, Vol. 31, pp. 839-843, 2005.

[Balaguer-2009] M. Balaguer, JB. Roldán, I.M. Tienda-Luna, F. G. Ruíz, A. Godoy, F. Gámiz, C. Sampedro, "A new inversion charge centroid model for surrounding gate transistors with HfO2 as gate insulator", 7ª Conferencia de dispositivos electrónicos CDE-2009, Santiago de Compostela (España), February 11-13, 2009.

[Balaguer-2010] M. Balaguer, B. Iñiguez, J.B. Roldán, “An analytical compact model for Schottky-Barrier Double Gate MOSFETs”, EUROSOI, 2010 (Sixth Workshop of the Thematic Network on Silicon on Insulator technology, devices and circuits), Grenoble (Francia), January 26-27, 2010.

[Balaguer-2011a] M. Balaguer, B. Iñiguez, J.B. Roldán, “An analytical compact model for Schottky-Barrier Double Gate MOSFETs”, Solid State Electronics, 64, pp.78-84, 2011.

[Balaguer-2011b] M. Balaguer, J.B. Roldán, F. Gámiz, “In-Depth Study of Quantum Effects in SOI DGMOSFETs for Different Crystallographic Orientations”, IEEE Trans. Electron Devices, Vol. 58, nº 12, pp. 4438-4441, 2011.

[Balaguer-2011c] M. Balaguer, J.B. Roldán, L. Donetti, F. Gámiz, “An inversion charge model for n-type and p-type DGMOSFETs accounting for different substrate Orientations”, EUROSOI, 2011 (Seventh Workshop of the Thematic Network on Silicon on Insulator technology, devices and circuits), Granada (Spain), January 17-19, 2011.

[Balaguer-2012] M. Balaguer, J.B. Roldán, L. Donetti, F. Gámiz, “Inversion charge modeling in n-type and p-type Double-Gate MOSFETs including quantum effects: the role of crystallographic orientation”, Solid State Electronics, 67, pp. 30-37, 2012.

[Balestra-1987] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini and T. Elewa, “Double-gate silicon-on-insulator transistor with volume inversion: A new device with greatly enhanced performance”, IEEE Electr Dev Lett 8 (9), pp. 410–412, 1987.

[Bernstein-2006] K. Bernstein et al., “High-performance CMOS variability in the 65-nm regime and beyond,” IBM J. Res. Develop., Vol. 50, nº 4/5, pp. 433–450, Jul.–Sep., 2006.

[Bescond-2007] M. Bescond, N. Cavassilas, and M. Lannoo, “Effective-mass approach for n-type semiconductor nanowire MOSFETs arbitrarily oriented,” Nanotechnology, Vol. 18, p. 255201–1–6, 2007.

[Bhattacharyya-2009] A.B. Bhattacharyya “Compact MOSFET models for VLSI design”, John Wiley and Sons, 2009.

[Bohr-2011] M. Bohr, “The Evolution of Scaling from the Homogeneous Era to the Heterogeneous Era”, IEDM, pp. 1-6, 2011.

[Borkar-1999] S. Borkar, “Design challenges of technology scaling,” IEEE Micro, Vol. 19, nº 4, pp. 23–29, Jul./Aug., 1999.

[Bremer-2010] J. Bremer, T. Peikert, W. Mathis, “Analytical inversion-mode varactor modeling based on the EKV model and its application to RF VCO design”, Mixed Design of Integrated Circuits and Systems (MIXDES). Proceedings of the 17th International Conference, 24-26 June 2010, pp. 64–69, 2010.

[Brown-2010] A. R. Brown, X. Wang, S. Markov, B. Cheng and A. Asenov, “Simulation of statistical variability in 18 and 13nm bulk MOSFETs”, Intel European Research and Innovation Conference, 12-14 October, Leixlip, Ireland. p. 99, 2010.

[BSIM] http://www-device.eecs.berkeley.edu/bsim3/.

[Bukhori-2010] M. F. Bukhori, S. Roy, A. Asenov, “Simulation of statistical aspects of charge trapping and related degradation in bulk MOSFETs in the presence of random discrete dopants”, IEEE Trans. Electron Devices, Vol. 57, nº 4, pp. 795- 803, 2010.

[Cantley-2007] K.D. Cantley, Y. Liu, H.S. Pal, T. Low, S.S. Ahmed, and M.S. Lundstrom, “Performance Analysis of III-V Materials in a Double-Gate nano-MOSFET”, IEDM 2007, pp. 113-116, 2007.

[Celler-2003] G. Celler, S. Cristoloveanu, "Frontiers of silicon-on-insulator", J. Appl. Phys. 93, pp.4955-4979, 2003.

[Chang-2000] L. Chang, C. Hu, "MOSFET scaling into the 10 nm regime", Superlattices Microstructures, 28, pp. 351–355, 2000.

[Chau-2004] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-K/Metal Gate Stack and Its MOSFET Characteristics," IEEE Electron Device Lett., Vol. 25, nº6, pp. 408-410, 2004.

[Chaves-2010] F. Chaves, D. Jiménez, J. Suñé, "Explicit quantum potential and charge model for double-gate MOSFETs", Solid State Electronics 54, pp. 530-535, 2010.

[Chen-2008] J. Chen, T. Saraya, K. Miyaji, K. Shimizu, and T. Hiramoto, "Experimental study of mobility in [110]- and [100]-directed multiple silicon nanowire GAA MOSFETs on (100) SOI," Proceedings of the 2008 Symposium on VLSI Technology, pp. 32 – 33, 2008.

[Chen-2010] J. Chen, T. Saraya, T. Hiramoto, "Mobility enhancement over universal mobility in (100) silicon nanowire gate-all-around MOSFETs with width and height of less than 10nm range" Symposium on VLSI Technology (VLSIT), 2010, pp. 175 – 176, 15-17 June 2010.

[Chiu-2006] F. Chiu, "Interface characterization and carrier transportation in metal/HfO2/silicon structure", J. of App. Phys., pp. 102-114, 2006.

[Choi-2010] Sung-Jin Choi, Jin-Woo Han, Sungho Kim, Dong-Il Moon, Moongyu Jang, Yang-Kyu Choi, "Dopant-Segregated Schottky Source/Drain FinFET With a NiSi FUSI Gate and Reduced Leakage Current", IEEE Transactions on electron devices, Vol. 57, Issue 11, pp. 2902 – 2906, 2010.

[Colinge-1990] J.P. Colinge, M.H. Gao, A. Romano, H. Maes, C. Claeys, "Silicon-on-insulator gate all-around MOS device", IEEE SOS/SOI Technology Conference, pp.137-138, October 2-4, 1990.

[Colinge-1997] J.P. Colinge, "Silicon on insulator technology: materials to VLSI", 2nd edition, Kluwer Academic Publishers, 1997.

[Colinge-2004] J. P. Colinge, "Multiple-gate SOI MOSFETs", Solid-State Electronics, 48, pp. 897–905, 2004.

[Colinge-2006] J.P. Colinge, Cynthia A. Colinge, "Physics of semiconductor devices", Springer, 2006.

[Colinge-2008] J. P. Colinge, "FinFETs and Other Multi-Gate Transistors", Springer Verlag, 2008.

[Craig-2008] A. Craig, G. Roy, A. Asenov, "Random-dopant-induced drain current variation in nano-MOSFETs: a three dimensional self-consistent Monte Carlo simulation study using "Ab Initio" ionized impurity scattering", IEEE Trans. Electron Devices, Vol. 55, nº 11, pp. 3251-3257, 2008.

[Cristoloveanu-2001] S. Cristolovenau, "Silicon on Insulator Technologies and devices: from present to future", Solid State Electronics, Vol. 43, pp.1403-1411, 2001.

[Crowel-1969a] C.R. Crowel, "Richardson constant and tunneling effective mass for thermoionic and thermionic- field emission in Schottky barrier diodes", Solid-State Electronics Pergamon Press. Vol. 12, pp. 55-59, 1969.

[Crowel-1969b] C.R. Crowell and V.L. Rideout, "Normalized Thermionic-Field (T-F) Emission in Metal-Semiconductor (Schottky) Barriers," Solid-State Electronics, Vol. 12, pp. 89-105, 1969.

[Darbandy-2011] G. Darbandy, F. Lime, A. Cerdeira, M. Estrada, I. Garduño, B. Iñiguez, "Study of potential high-κ dielectric for UTB SOI MOSFETs using analytical modeling of the

gate tunneling leakage", Semiconductor Science and Technology 26, pp 115002-115010, 2011.

[Donetti-2006a] L. Donetti, F. Gámiz, J.B. Roldan, A. Godoy, "Acoustic phonon confinement in silicon nanolayers. Effect on electron mobility", Journal of Applied Physics, 100 (1): Art. nº 013701, 2006.

[Donetti-2006b] L. Donetti, F. Gámiz, N. Rodríguez, F. Jiménez and C. Sampedro, "Influence of acoustic phonon confinement on electron mobility in ultrathin silicon on insulator layers" Appl. Phys. Lett. 88, 122108, 2006.

[Donetti-2007a] L. Donetti, F. Gámiz, S. Cristoloveanu, "A theoretical interpretation of magnetoresistance mobility in silicon inversion layers", Journal of applied physics 102: Art. nº 013708, 2007.

[Donetti-2007b] L. Donetti, F. Gámiz, S. Cristoloveanu, "Monte Carlo simulation of Hall and magnetoresistance mobility in SOI devices", Solid-state electronics 51 (9): pp. 1216-1220, September 2007.

[Donetti-2008] L. Donetti, F. Gámiz, A. Godoy, N. Rodríguez, "Fully self-consistent k · p solver and Monte Carlo simulator for hole inversion layers", In: Proceedings of the 38th ESSDERC, pp. 254–261, 2008.

[Donetti-2009] L. Donetti, F. Gámiz, N. Rodríguez, "Simulation of hole mobility in two dimensional systems", Semiconductor Science and Technology 24, pp. 035016-035023, 2009.

[Donetti-2010] L. Donetti, F. Gámiz, N. Rodríguez, F. Jiménez-Molinos, J.B. Roldán, "Hole transport in DGSOI devices: Orientation and silicon thickness effects" Solid State Electron., Vol. 54, pp. 191–195, 2010.

[Driussi-2009] F. Driussi and D. Esseni, "Simulation Study of Coulomb Mobility in Strained Silicon", IEEE Transactions on Electron Devices, Vol. 56, pp. 2052-2059, 2009.

[EKV] http://legwww.ekv.epfl.ch/ekv/.

[Eminente-2004] S. Eminente, M. Alessandrini, C. Fiegna, “Comparative analysis of the RF and noise performance of bulk and single ultra-thin SOI MOSFETs by numerical simulation”, Solid State Electronics, Vol. 48, nº 4, pp. 543-549, 2004.

[Enz-2006] C. Enz and E.A. Vittoz, “Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design”. New York: Wiley, 2006.

[Enz-2008] C. Enz, “A Short Story of the EKV MOS Transistor Model” Solid-State Circuits Newsletter, IEEE, Volume: 13 Issue: 3, pp. 24–30, 2008.

[Esseni-2011] D. Esseni and F. Driussi, "A Quantitative Error Analysis of the Mobility Extraction According to the Matthiessen Rule in Advanced MOS Transistors", IEEE Transactions on Electron Devices, Vol.58, pp.2415-2422, 2011.

[Faynot-2011] O. Faynot, “Benefits and Challenges of FDSOI Technology for 14nm Node”, Tutorial at the SOI Conference. IEEE International SOI Conference, 2011.

[Fischetti-1993] M.V. Fischetti and S. E. Laux, “Monte Carlo study of electron transport in inversion layers,” Phys. Rev. B, Condens. Matter, Vol. 48,nº 4, pp. 2244–2274, Jul. 1993.

[Fischetti-2002] M.V.Fischetti, F. Gámiz and W. Hansch, “On the enhanced electron mobility in strained-silicon inversion layers”, Vol. 92, pp. 7320-7324, 2002.

[Flandre-2001] D. Flandre, J.-P. Raskin, D. Vanhoenacker, “SOI CMOS transistors for RF and microwave applications”, International Journal of High Speed Electronics and Systems, Vol. 11, pp. 1159-1248, 2001.

[Flandre-2010] D. Flandre, V. Kilchytska and T. Rudenko, “gm/Id method for threshold voltage extraction applicable in advanced MOSFETs with nonlinear behaviour above threshold”, IEEE Electron Device Lett., Vol. 31, nº 9, pp. 930–932, 2010.

[Gámiz-1995] F. Gámiz and J. A. López-Villanueva, “A comparison of models for phonon scattering in Silicon inversion layers,” Journal Applied Physics, vol. 77, pp. 4128–4129, 1995.

[Gámiz-1994] F. Gámiz, J.A. López-Villanueva, J.A. Jiménez-Tejada, I. Melchor and A. Palma, “A comprehensive model for Coulomb scattering in inversion layers J. Appl. Phys. 75, pp. 924–34”, 1994.

[Gámiz-1996] F. Gámiz, J. Roldan, J.A. Lopez Villanueva, J.E. Carceller, "Electron Velocity Saturation in Quantized Silicon Carbide Inversion Layers". Applied Physics Letters, 69(15), pp. 2219 – 2221, 1996.

[Gámiz-1998a] F. Gámiz, J.A. López-Villanueva, J.B. Roldán, A. Godoy, J.E. Carceller and P. Cartujo “Monte Carlo simulation of electron transport properties in extremely thin SOI MOSFETs” IEEE Trans. Electron. Devices 45, pp. 1122–1128, 1998.

[Gámiz-1998b] F. Gámiz, J.B. Roldán, J.A. López-Villanueva, "Phonon-limited electron mobility in ultrathin silicon-on-insulator inversion layers", Journal of Applied Physics, Vol. 83, pp. 4802-4806, 1998.

[Gámiz-1999a] F. Gámiz, J.B. Roldán, P. Cartujo-Cassinello, J.E. Carceller, J.A. López-Villanueva and S. Rodríguez, "Electron Mobilty Behavior in Extremely Thin Single-Gate Silicon-On-Insulator Inversion Layers", Journal of Applied Physics, Vol. 86, pp. 6269-6275, 1999.

[Gámiz-1999b] F. Gámiz, J.B. Roldan, J.A. López-Villanueva, P. Cartujo-Cassinello and J.E. Carceller, “Surface roughness at the Si-SiO2 interfaces in fully depleted Silicon-on-insulator inversion layers”, Journal of Applied Physics, 86, pp. 6854-6862, 1999.

[Gámiz-2001] F. Gámiz, J.B. Roldán, P. Cartujo-Cassinello, J.A. López-Villanueva and P. Cartujo, “Role of surface-roughness scatterring in double gate silicon-on-insulator inversion layers”, Journal of Applied Physics, 89, pp. 1764-1770, 2001.

[Gámiz-2002] F. Gámiz, F. Jiménez-Molinos, J.B. Roldán, P. Cartujo-Cassinello, "Coulomb scattering model for ultrathin silicon-on-insulator inversion layers", Applied Physics Letters, 69, pp. 2219-2221, 2002.

[Gámiz-2003a] F. Gámiz, J.B. Roldán, J.E. Carceller, P. Cartujo, "Monte Carlo simulation of remote-Coulombscattering- limited mobility in metal-oxide-semiconductor transistors", Applied Physics Letters, Vol. 82 (19), pp. 3251-3253, 2003.

[Gámiz-2003b] F. Gámiz and M.V. Fischetti, "Remote Coulomb scattering in metal-oxide-semiconductor field effect transistors: screening by electrons in the gate", Applied Physics Letters, Vol. 83, pp. 4848-4850, 2003.

[Gámiz-2003c] F. Gámiz, J.B Roldán, A. Godoy, P. Cartujo-Cassinello, J.E. Carceller, "Electron mobility in double gate silicon on insulator transistors: Symmetric-gate versus asymmetric-gate configuration" Journal of Applied Physics, 94, pp. 5732-5741, 2003.

[Gámiz-2004] F. Gámiz, J.B. Roldán, A. Godoy, J.E. Carceller P. Cartujo, "Double gate silicon on insulator transistors. A Monte Carlo study", Solid State Electronics, Vol. 48, pp. 937-945, 2004.

[Galup-2007] C. Galup-Montoro, M.C. Schneider, "MOSFET modeling for circuit analysis and design", World Scientific, 2007.

[Ge-2001] L. Ge, J. Fossum, "Physical compact modeling and analysis of velocity overshoot in extremely scaled CMOS devices and circuits", IEEE Transactions on Electron Devices, 48, pp. 2074–2080, 2001.

[Ge-2006] L. Ge, F. Gámiz, G. O. Workman, S. Veeraraghavan, "On the capacitance limits of nanoscale DG and FD SOI MOSFET", IEEE Transaction on electron devices, Vol. 53, nº 4, pp. 753-758, 2006.

[Gildenblat-2010] G. Gildenblat, "Compact Modeling: Principles, Techniques and Applications", Springer 2010.

[Gnani-2004]. E. Gnani, S. Reggiani, M. Rudan, G. Baccarani, “A new approach to the self-consistent solution of the Schrödinger-Poisson equations in nanowire MOSFETs”, ESSDERC 2004, pp.177-180, 2004.

[Godoy-2006] A. Godoy, A. Ruiz-Gallardo, C. Sampedro, and F. Gámiz, “Self-consistent solution of the 2D Schrödinger-Poisson equations in Multiple-Gate SOI MOSFETs”, Proceedings of the first workshop of the thematic network, 2006.

[Godoy-2007a] A. Godoy, A. Ruiz Gallardo, C. Sampedro and F. Gámiz, “Quantum mechanical effects in multiple gates MOSFETs”, Journal Computational Electronics, Vol. 6, nº 1-3, pp. 145-148, Jan. 2007.

[Godoy-2007b] A. Godoy, F. Ruiz, C. Sampedro, F. Gámiz, and U. Ravaioli, “Calculation of the phonon-limited mobility in silicon Gate All-Around MOSFETs,” Solid-State Electronics, vol. 51, no. 9, pp. 1211–1215, 2007.

[Goodnick-1985] S. M. Goodnick, D. K. Ferry, C. W. Wilmsen, Z. Liliental, D. Fathy, and O. L. Krivanek, “Surface roughness at the Si(100)-SiO2 interface,” Physical Review B, Vol. 32, nº 12, pp. 8171–8186, 1985.

[Goodosn-1994] K.E. Goodson, M.I. Flik, L.T. Su, and D.A. Antoniadis, "Prediction and measurement of the thermal conductivity of amorphous dielectric layers", J. Heat Transfer, Vol. 116, pp.317-324, 1994.

[Guo-2002] J. Guo and M. Lundstrom “A Computational Study of Thin-Body, Double-Gate, Schottky Barrier MOSFETs”, IEEE Transactions on Electron Devices, Vol. 49, nº 11, pp. 1897-1902, November, 2002.

[Haque-2002] A. Haque, M.Z. Kauser, “A comparison of wave-function penetration effects on gate capacitance in deep submicron n- and p-MOSFETs”, IEEE Transactions on Electron Devices, 49 (9), pp 1580-1587, 2002.

[He-2004] J. He, X. Xi, C. Lin, M. Chan, A. Niknejad, and C. Hu, “A Non-Charge-Sheet Analytic Theory for Undoped Symmetric Double-Gate MOSFETs from the

Exact Solution of Poisson's equation using SPP Approach", NSTI-Nanotech 2004, www.nsti.org, ISBN 0-9728422-8-4, Vol. 2, 2004.

[HiSIM] http://home.hiroshima-u.ac.jp/usdl/HiSIM.html

[Hoffmann-2009] T. Hoffmann, "High-k/Metal Gates: Industry Status and Future Direction," IEDM Short Course, 2009.

[Huff-2005] H. R. Huff and D. C. Gilmer, "High Dielectric Constant Materials" .Berlin, Germany: Springer-Verlag, 2005.

[IBM-2007] "IBM Advancement to Spawn New Generation of Chips", IBM Corp., press release. [Online]. Available: http://www-03.ibm.com/ press/us/en/pressrelease/20980.wss., Jan. 2007.

[Intel-2007] "Intel's Transistor Technology Breakthrough Represents Biggest Change to Computer Chips in 40 Years", 2007. Intel Corp., press release. [Online]. Available: http://www.intel.com/pressroom/archive/releases/ 20070128comp.htm, 2007.

[Iñiguez-2005] B. Iñiguez, D. Jiménez, J. Roig, H. A. Hamid, L. F. Marsal and J. Pallares, "Explicit Continuous Model for Long-Channel Undoped Surrounding Gate MOSFETs", IEEE Transactions on Electron Devices, Vol.52, nº8, pp. 1868-1873, August 2005.

[Iñiguez-2006] B. Iñiguez, T.A. Fjeldly, A. Lázaro, F. Danneville, M.J. Deen, "Compact-modeling solutions for nanoscale double-gate and gate all-around MOSFET", IEEE Transaction on Electron Devices, 53, pp. 2128-2142, 2006.

[ITRS-2011] Internacional Technology Roadmap for semiconductors 2011 edition.

[Jang-2002] M. Jang and J. Lee, "Analysis of Schottky barrier height in small contacts using a thermionic field emission model", ETRI Journal, Vol. 24, number 6, pp. 455-461, December 2002.

[Jang-2010] M. Jang, M. Jun, T. Zyung,”Effective mobility characteristics of platinum-silicided p-type Schottky barrier metal-oxide-semiconductor field-effect transistor”, Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Vol. 28 , Issue: 4 Digital Object Identifier, pp. 799 – 801, 2010

[Jiang-2012] X. Jiang, S. Li, L. Wang, “A comparative study for quantum transport calculations of nanosized field-effect transistors”, Solid State Electronics, vol 68, pp.56-62, 2012.

[Jin-2007a] S. Jin, M. V. Fischetti, and T. Tang, “Modeling of surface-roughness scattering in ultrathin-body SOI MOSFETs,” IEEE Transactions on Electron Devices, Vol. 54, pp. 2191–2203, September 2007.

[Jin-2007b] S. Jin, M. V. Fischetti, and T. Tang, “Modeling of electron mobility in gated silicon nanowires at room temperature: Surface roughness scattering, dielectric screening, and band nonparabolicity,” Journal of Applied Physics, Vol. 102, nº 5, pp. 083715–1–14, 2007.

[Jiménez-2004] D. Jiménez, B. Íñiguez, J. Sune, L.F. Marsal, J. Pallarés, J. Roig et al., “Continuos analytic current-voltage model for surrounding gate MOSFETs”, IEEE Electron Device Letters, 25, pp. 571-573, 2004.

[Jiménez-Molinos-2008] F. Jiménez-Molinos, F. Gámiz and L. Donetti, “Coulomb scattering in high-κ gate stack silicon-on-insulator metal-oxide-semiconductor field effect transistors” J. Appl. Phys. 104, pp. 063704.1–.8, 2008.

[Jiménez-Molinos-2010a] F. Jiménez-Molinos, J.B. Roldán, M. Balaguer, F. Gámiz, “An in-depth simulation study of Coulomb mobility in ultra-thin-body SOI MOSFETs”, Semiconductor Science and Technology, 25, p. 055002, 2010.

[Jiménez-Molinos-2010b] F. Jiménez-Molinos, J.B. Roldán, F.Gamiz, L.Donetti, A.M. Roldán, M. Balaguer, “An in-depth study of Coulomb mobility in Double Gate MOSFETs”, EUROSOI, 2010 (Sixth Workshop of the Thematic Network on Silicon on Insulator technology, devices and circuits), Grenoble (Francia), January 26-27, 2010.

[Kang-2008] H. Kang, J. Han, Y. Choi, “Analytical threshold voltage model for double-gate MOSFETs with localized charges”, IEEE Electron Device Letters, Vol. 29, nº 8, pp. 927-930, 2008.

[Kim-2010] Tae-Hyeon Kim, Byung-Kwon Jung, Chang-Ju Lee, Dong-Seok Kim, Sang-Yun Sung, Young-Woo Heo, Jung-Hee Lee, Sung-Ho Hahm, “GaN schottky barrier MOSFET using indium-tin-oxide as source, drain and gate material“,Electron Devices and Solid-State Circuits (EDSSC), IEEE International Conference of Digital Object, pp. 1-4, 2010.

[Kinoshita-2004] A. Kinoshita, Y. Tsuchiya, A. Yagishita, K. Uchida and J. Koga, “Solution for high-performance Schottky-source/drain MOSFETs: Schottky barrier height engineering with dopant segregation technique”, 2004 Symposium VLSI Technology, pp. 168-167.

[Knoch-2002] J. Knoch, J. Appenzeller, „Impact of the channel thickness on the performance of Schottky barrier metal–oxide–semiconductor field-effect transistors“, Appl. Phys. Lett. 81, 3082 (2002)

[Knoch-2005] J. Knoch, M. Zhang, Q. T. Zhao, St. Lenk, S. Mantl, and J. Appenzeller, “Effective Schottky barrier lowering in silicon-on-insulator Schottky-barrier metal-oxide-semiconductor field-effect transistors using dopant segregation”, Appl. Phys. Lett. 87, 263505 (2005)

[Knoch-2006] J. Knoch, M. Zhang, S. Mantl, J. Appenzeller, „On the performance of single-gated ultrathin-body SOI Schottky-barrier MOSFETs”, IEEE Trans. Electron. Dev. 53, p. 1669 (2006)

[Knoch-2007] J. Knoch, M. Zhang, J. Appenzeller, S. Mantl, “Physics of ultrathing-body silicon-on-insulator SBFET”, Appl. Phys. A 87, pp. 351–357, 2007.

[Knoll-2011] L. Knoll, Q.T. Zhao, R. Luptak, S. Trellenkamp, K.K. Bourdelle, S. Mantl, “20nm Gate length Schottky MOSFETs with ultra thin NiSi/epitaxial NiSi2

source/drain", 12th International Conference on Ultimate Integration on Silicon (ULIS), 14-16 March 2011, pp. 1-4, 2011.

[Kotlyar-2004] R. Kotlyar, C. Weber, L. Shifren, S. Cea1, M. D. Giles, and M. Stettler, "Assessment of room-temperature phonon-limited mobility in gated silicon nanowires," Applied Physics Letters, Vol. 84, nº 25, pp. 5270–5272, 2004.

[Kovac-2008] U. Kovac, D. Reid, C. Millar, G. Roy, S. Roy and A. Asenov, "Statistical simulation of random dopant induced threshold voltage fluctuations for 35 nm channel length MOSFET," Microelectronics Reliability, Vol. 48, nº 8-9, pp. 1572–1575, 2008.

[Kubo-1957] R. Kubo, "Statistical-mechanical theory of irreversible processes. General theory and simple applications to magnetic and conduction problems," Journal of Physics Society Japan, Vol. 12, pp. 570–586, 1957.

[Iwai-2002] H. Iwai, T. Ohguro, S.I. Ohmia, "NiSi salicide technology for scaled CMOS", Microelectronic Engineering, vol. 60, no. 1-2, Jan. 2002, p. 157-69.

[Larrieu-2004] G. Larrieu and E. Dubois, "Schottky-barrier S/D MOSFETs on ultrathin SOI body with a tungsten metallic midgap gate," IEEE Electron Device Lett., vol. 25, no. 12, pp. 801–803, Dec. 2004.

[Larrieu-2005] G. Larrieu, E. Dubois, "Integration of PtSi-based Schottky-barrier p-MOSFET with a mid gap tungsten gate", IEEE Transaction on Electron Devices, vol. 52, no.12, pp. 2720-2726, Dec 2005.

[Larson-2004] J. Larson and J. Snyder, "Schottky barrier CMOS – technology overview". Spinnaker Semiconductor, 2004.

[Larson-2006] J.M. Larson, J.P. Snyder, "Overview and satatus of metal S/D Schottky-barrier MOSFETs technology", IEEE Trans. Electron. Dev. 53, p. 1048 (2006)

[Lázaro-2008] A. Lazaro and B. Iniguez, “RF and noise model of gate-all-around MOSFETs,” Semicond. Sci. Technol., Vol. 23, nº 7, p. 075 022, May 2008.

[Lepsleter-1968] M.P. Lepselter, S.M. Sze, “SB-IGFET: An Insulated-Gate Field Effect Transistor Using Schottky Barrier Contacts for Source and Drain”, IEEE Proceedings Letters, pp. 1400-1402, 1968.

[Lime-2008] F. Lime, B. Iñiguez and O. Moldovan, “A quasi two-dimensional compact drain current model for undoped symmetric double gate MOSFETs including shortchannel effects” IEEE Transaction on Electron Devices 55, Issue 6, pp. 1441–1448, 2008.

[Lo-1997] S.H. Lo, D.A. Buchanan, Y. Taur, and W. Wang, "Quantum-Mechanical Modeling of Electron Tunneling Current from the Inversion Layer of Ultra-Thin-Oxide nMOSFET's," IEEE Electron Device Lett., Vol. 18, nº 5, pp. 209-211, 1997.

[López-Villanueva-1997] J.A. López-Villanueva, P. Cartujo-Cassinello, J. Banqueri, F. Gámiz, and S. Rodríguez, “Effects of the inversion layer centroid on MOSFET behavior,” IEEE Trans. Electron Devices, Vol. 44, nº 11, pp. 1915–1922, November 1997.

[López-Villanueva-2000] J.A. López-Villanueva, P. Cartujo-Cassinello, F. Gámiz, J. Banqueri, and A.J. Palma, “Effects of the inversion layer centroid on the performance of double gate MOSFETs”, Trans. on Electron Devices, Vol. 47, nº 1, pp. 141 - 146 January 2000.

[Low-2005] T. Low, M. F. Li, W. J. Fan, S.T. Ng, “Impact of surface roughness on silicon and germanium ultra-thin body MOSFETs”, 2004 International Electron Devices Meeting (IEEE Cat. No.04CH37602), Piscataway, NJ, USA, IEEE, 2005, p. 151-4.

[Lu-2002] J.P. Lu, D. Miles, J. Zhao, A. Gurba,, ”A novel nickel silicide process technology for CMOS devices with sub-40 nm physical gate length”. International Electron Devices Meeting. Technical Digest (Cat. nº02CH37358), p. 371-4 Piscataway, NJ, USA: IEEE, 2002.

[Lui-2004] Y. Liu, M. Masahara, K. Ishii, T. Sekigawa, H. Takashima, H. Yamauchi, E. Suzuki, “A highly threshold voltage-controlable 4T FinFET with an 8.5-nm-thick Si-Fin channel”, IEEE Electron Device Letters, Vol. 25, nº 7, pp. 510 – 512, July 2004.

[Lundstrom-2002] M.S. Lundstrom and Z. Ren, “Essential Physics of carrier transport in nanoscale MOSFETs, IEEE Trans. electron Dev. 49, pp. 133-141, Jan 2002.

[Maex-1998] K. Maex, “Simly irresistible silicides”, Physics World, Nov. 1998.

[Manoj-2007] C.R. Manoj, V. Ramgopal Rao, "Impact of High-k gate dielectrics on the device and circuit performance of Nanoscale FinFETs " IEEE Electron Device Letters, Vol. 28, nº 4, pp. 295-297, April 2007.

[Millar-2008] C. Millar, D. Reid, G. Roy, S. Roy and A. Asenov, "Accurate Statistical Description of Random Dopant Induced Threshold Voltage Variability," IEEE Electron Device Letters, Vol. 29, nº 8, pp. 946–948, August 2008.

[Ming-2005] S. Ming-Shan, C. Pang-Shiu, M.J. Tsai, and T.F. Lei, “A Novel Dynamic Threshold Voltage MOSFET (DTMOS) Using Heterostructure Channel of Si1-y Cy Interlayer”, IEEE electron device letters, Vol. 26, nº 10, pp. 740 – 742, October 2005.

[Mohd-2011] A. S. Mohd Zain, B. Cheng, X. Wang and A. Asenov, "Insights on Device Performance of SOI MOSFET with 60 nm and 15 nm BOX Thickness," EuroSOI 2011 Conference: Jan. 17-19, 2011.

[Moldovan-2007a] O. Moldovan, D. Jiménez, J. Roig, F. A. Chaves and B. Iñiguez, “Explicit Analytical Charge and Capacitance Models Of Undoped Double Gate MOSFETs”, IEEE Transaction on Electron Devices, Vol. 54, nº 7, pp. 1718 - 1724, July 2007.

[Moldovan-2007b] O. Moldovan, B. Iñiguez, D. Jiménez, and J. Roig, “Analytical charge and capacitance models of undoped cylindrical surrounding-gate MOSFETs,” IEEE Transactions Electron Devices, vol. 54, no. 1, pp. 162–165, 2007.

[Moore-1965] G. E. Moore, “Cramming more components onto integrated circuits”, Electronics, Vol. 38, nº 8, 1965.

[Moreno-2010] E. Moreno, J.B. Roldán, F.G. Ruiz, D. Barrera, A. Godoy, F. Gámiz, “An analytical model for square GAA MOSFETs including quantum effects”, Solid State Electronics, vol 54, pp.1463-1469, 2010.

[Moreno-2011] E. Moreno, J.B. Roldán, F.G. Ruiz, D. Barrera, M.J. Ibáñez, A. Godoy, F.Gámiz, “An inversion charge analytical model for square Gate-All-Around MOSFETs”, IEEE Transactions on Electron Devices, 8, pp. 2854-2861, 2011.

[Mudanai-2001] S. Mudanai, L. F. Register, A. F. Tasch, and S. K. Banerjee, “Understanding the effects of wave function penetration on the inversion layer capacitance of NMOSFETs”, IEEE Electron Device Lett., Vol. 22, nº 3, pp. 145–147, 2001.

[Natori-1994] K. Natori, “Ballistic metal-oxide-semiconductor field effect transistor”, Journal of Applied Physics, 76, pp. 4879-4890, 1994.

[Nazarov-2011] A. Nazarov, J.P. Colinge, F. Balestra, J.P. Raskin, F. Gámiz, V.S. Lysenko, “Semiconductor-on-insulator material for nanoelectronics applications”, Springer, 2011.

[Nikolic-2008] B. Nikolic, “Design in the Power-Limited Scaling Regime”, IEEE Trans. on Elec. Dev., 10 (1), pp. 71-83, 2008.

[Okura-1990] Y. Okura, “Quantum effects in Si n-MOS inversion layer at high substrate concentration,” Solid-State Electron., Vol. 33, p. 1581, 1990.

[Omura-1993] Y. Omura, S. Horiguchi, M. Tabe, K. Kishi, “Quantum-mechanical effects on the threshold voltage of ultrathin SOI nMOSFETs”, IEEE Electron Device Letters, Vol. 14, nº 12, p. 569, 1993.

[Ortiz-Conde-2005] A. Ortiz-Conde, F.J. García Sánchez, J. Muci, "Rigurous analytic solution for the drain current of undopped symetric dual-gate MOSFETs", Solid State Electronics, 49, pp. 640-647, 2005.

[Ortiz-Conde-2007] A. Ortiz-Conde, F.J. García-Sánchez, J. Muci, S. Malobabic, J.J. Liou, "A Review of Core Compact Models for Undoped Double-Gate SOI MOSFETs", IEEE Transaction on Electron Devices, Vol. 54, n 1, pp. 131 – 140, January 2007.

[Östling-2010] M. Östling, Luo Jun, V. Gudmundsson, P.E. Hellström, B. Gunnar Malm, "Nanoscaling of MOSFETs and the implementation of Schottky barrier S/D contacts", Microelectronics Proceedings (MIEL), 27th International Conference on Digital Object, pp. 9-13, 2010.

[Padilla-2012] J.L. Padilla, L. Knoll, F. Gámiz, Q.T. Zhao, A. Godoy, S. Mantl, "Simulation of fabricated 20-nm Schottky-barrier MOSFETs on SOI: impact of barrier lowering", IEEE Trans. Electron. Dev. 59, p. 1320 (2012)

[Padovani-1966] F.A. Padovani, R. Stratton, "Field and thermionic field emission in Schottky barriers", Solid-State Electronics, Pergamon Press. Vol. 9, pp. 695-707, 1966.

[Park-2001] J.T. Park, J.P. Colinge, C.H. Diaz, "Pi-gate SOI MOSFET", IEEE Electron Device Lett., Vol. 22, nº 8, pp. 405-406, 2001.

[Passlack-2008] M. Passlack, et al, "High Mobility III-V MOSFETs For RF and Digital Applications", IEDM 2007 pp 621-624, 2008.

[Pearman-2007] D. Pearman, "Electrical Characterisation and Modeling of Schottky barrier metal source/drain MOSFETs". M.S. thesis, University of Warwick, 2007.

[Plumeer-2000] J.D. Plummer, M.D. Deal, P.B. Grin, "Silicon VLSI Technology", Prentice Hall, 2000.

[Poiroux-2005] T. Poiroux, M. Vinet, O. Faynot O, J. Widiez, J. Lolovier, T. Ernst, B. Pre-vitali, S. Deleonibus, “Multiple gate devices: advantages and challenges”, Microelectronic engineering, Vol. 80, p. 378, 2005.

[Pop-2004] E. Pop and K.E. Goodson, “Thermal Analysis of Ultra-Thin Body Device Scaling”, Proc. IEEE ITherm Conf. (Las Vegas, NV) pp. 1–7, 2004

[PSP] http://pspmodel.asu.edu.

[Racko-2008] J. Racko, R. Granzner, F. Schwierz, J. Breza, D. Donoval, O. Kucera, P. Pintes, “Comparison of a standard and a Schottky dual gate MOSFET”, Journal of Electrical Engineering, Vol. 59, nº 2, pp. 81–85, 2008.

[Rahman-2005] A. Rahman, M. S. Lundstrom, and A. W. Ghosh, “Generalized effective mass approach for n-type metal-oxide-semiconductor field-effect transistors on arbitrarily oriented wafers,” J. Appl. Phys., Vol. 97, nº 5, p. 053702, 2005.

[Reggiani-2007] S. Reggiani, L. Silvestri, A. Cacciatori, E. Gnani, A. Gnudi, G. Baccarani, “Physically-based unified compact model for low-field carrier mobility in MOSFETs with different gate stacks and biaxial/uniaxial stress conditions”, IEDM 2007, pp. 557-560, 2007.

[Ren-2000] Z. Ren, R. Venugopal, S. Datta, M. Lundstrom, D. Jovanovic, J. Fossum, “The ballistic nanotransistor: a simulation study”, IEDM Tech Digest, pp. 715–718, 2000.

[Ren-2001] Z. Ren, R. Venugopal, S. Datta and M.S, Lundstrom, “Examination of design and manufaturing issues in a 10 nm Double Gate MOSFET using non-equilibrium Green’s functions simulation”, IEDM Tech. Digest, Washington, December pp. 3-5, 2001.

[Rhew-2002] J.H. Rhew, Z. Ren and M. Lundstrom, “Numerical study of a ballictic MOSFET”, Solid State electronics, 46, nº 11, pp. pp. 1899-1906, 2002.

[Rodríguez-2007] N. Rodríguez, F. Gámiz and J.B. Roldán, “Modeling of the inversion layer centroid and polysilicon depletion effects on ultrathin gate oxide MOSFET behaviour: The influence of the crystallographic orientation”, IEEE Trans, Electron Devices, Vol. 54, nº 4, pp. 723-731, April 2007.

[Roldán-1997a] J.B. Roldan, F. Gamiz, J.A. Lopez-Villanueva, and J.E. Carceller, “Modeling effects of electron-velocity overshoot in a MOSFET,” IEEE Trans. Electron Devices, Vol. 44, nº 5, pp. 841–846, May 1997.

[Roldán-1998] J.B. Roldan, F. Gamiz, J.A. Lopez-Villanueva, P. Cartujo, and J.E. Carceller, “A model for the drain current of deep submicrometer MOSFETs including electron-velocity overshoot,” IEEE Trans. Electrón Devices, Vol. 45, nº 10, pp. 2249–2251, October 1998.

[Roldán-2001] J.B. Roldán, F. Gámiz, J.A. López-Villanueva, P. Cartujo and A. Godoy, “Strained-Si on Si1-xGex MOSFET inversion layer centroid modeling”, IEEE Trans. Electron Devices, Vol. 48, p.2447, October 2001.

[Roldán-2003] J. B. Roldán, F. Gámiz, P. Cartujo-Casinello, P. Cartujo, J. Carceller, and A. Roldán, “Strained-Si on Si1-x Gex MOSFET mobility model,” IEEE Transactions on Electron Devices, vol. 50, no. 5, pp. 1408–1411, 2003.

[Roldán-2008a] J.B. Roldan, M. Balaguer, A. Godoy, F.G. Ruiz, F. Gamiz, “In-depth characterization of quantum effects in SOI MOSFETs for modeling purposes”, Fourth Workshop of the Thematic Network on Silicon-On-Insulator Technology, Devices and Circuits, EUROSOI 2008, pp. 99-100, Cork (Ireland), 2008.

[Roldán-2008b] J.B. Roldan, A. Godoy, F. Gamiz, M. Balaguer, “Modeling the Centroid and the Inversion Charge in Cylindrical Surrounding Gate MOSFETs, Including Quantum Effects”, IEEE Trans. Electrón Devices, Vol. 55, pp. 411-416. 2008.

[Roldán-2010] J.B. Roldán, F. Gámiz, F. Jimenez-Molinos, C. Sampedro, A.Godoy, L. Donetti, N. Rodriguez, “Analytic I-V model for surrounding-gate MOSFET including

quantum and velocity overshoot effects", IEEE Trans. Electrón Devices, Vol. 57, pp. 2925-2933. 2010.

[Ruiz-2011] F. G. Ruiz, I. M. Tienda-Luna, A. Godoy, C. Sampedro, F. G´amiz, and L. Donetti, "Simulation of the electrostatic and transport properties of 3D-stacked GAA silicon nanowire FETs," Solid State Electronics, vol. 59, no. 1, pp. 62–67, 2011.

[Sah-1991] C.T. Sah, "Fundamentals of Solid-State Electronics", World Scient. Publ. Company, Singapore, ISBN 981-02-0637-2, 1991.

[Sahoo-2010] A. Sahoo, P.K. Thakur, and S. Mahapatra, "A Computationally Efficient Generalized Poisson Solution for Independent Double-Gate Transistors", IEEE Transactions on Electron Devices, Vol. 57, n. 3, pp. 632 – 636, March 2010.

[Sallese-2005] J.M. Sallese, F. Krummenacher, F. Pregaldiny, C. Lallement, A. Roy, and C. Enz, "A design oriented charge-based current model for symmetric DGMOSFET and its correlation with the EKV formalism", Solid State Electron., Vol. 49, nº 3, pp. 485–489, March 2005.

[Sampedro-2006] C. Sampedro, "Estudio, caracterización y simulación de transistores con modulación de la velocidad en silicio", Tesis Doctoral, 2006.

[Sampedro-2010] C. Sampedro, F. Gamiz, A. Godoy, R. Valin, A. Garcia-Loureiro, F.G. Ruiz, "Multi-subband monte carlo study of device orientation effects in ultra-short channel DGSOI," Solid State Electron., Vol. 54, pp. 131-136, January 2010.

[Sampedro-2011] C. Sampedro, F. Gámiz, A. Godoy, R. Valín, A. García-Loureiro, N. Rodríguez, I.M. Tienda-Luna, F. Martinez-Carricondo, B. Biel, "Multi-Subband Ensemble Monte Carlo simulation of bulk MOSFETs for the 32 nm-node and beyond", Solid State Electron., Vol. 65-66, pp. 88-93, 2011.

[Saremi-2010] M. Saremi, B. Ebrahimi, A. Afzali-Kusha, "Ground plane SOI MOSFET based SRAM with consideration of process variation", Electron Devices and Solid-State Circuits (EDSSC), IEEE International Conference, 15-17 Dec. 2010, pp. 1-4, 2010.

[Sato-2010] S. Sato, K. Kakushima, P. Ahmet, K. Ohmori, K. Natori, K. Yamada, H. Iwai, “Effects of corner angle of trapezoidal and triangular channel cross-sections on electrical performance of silicon nanowire field-effect transistors with semi gate-around structure”, Solid-State Electronics, Vol 65–66, November–December 2011, Pages 2–8. Selected Papers from the ESSDERC 2010 Conference

[Semenov-2002] O. Semenov, A. Vassighi, M. Sachdev, “Impact of technology scaling on thermal behavior of leakage current in sub-quarter micron MOSFETs: perspective of low temperature current testing”, Microelecronics Journal 33, pp. 985-994, 2002.

[Shimizu-2007] K. Shimizu and T. Hiramoto, University of Tokyo, “Si/Si1−xGex/Si quantum wells with high-κ/metal gate stacks and additive uniaxial strain for 22 nm technology node”, IEDM 2007, pp. 727-730, 2007.

[Snyder-1995] J.P. Snyder, C.R. Helms, and Y. Nishi, “Experimental investigation of a PtSi source and drain field emission transistor”. Applied Physics Letters, 67(10), pp. 1420–1422, 1995.

[Skotnicki 2011] T. Skotnicki, “Competitive SOC with UTBB SOI”, Tutorial at the SOI Conference, IEEE International SOI Conference, 2011.

[SOITEC] http://www.soitec.com

[Soleimani-2009] S. Soleimani, A. Sammak, B. Forouzandeh, IAENG, “A Novel Ultra-Low-Energy Bulk Dynamic Threshold Inverter Scheme”, Proceedings of the International MultiConference of Engineers and Computer Scientists, Vol. I IMECS 2009, March 18 - 20, 2009.

[Stern-1967] F. Stern and W.E. Howard, “Properties of semiconductor surface inversion layers in the electric quantum limit,” Phys. Rev., Vol. 163, nº 3, pp. 816–835, Nov. 1967.

[Stern-1972] F. Stern, “Self-consistent results for n-type Si inversion layers,” Phys. Rev.B, Condens. Matter, Vol. 5, nº 12, pp. 4891–4899, Jun. 1972.

[Stern-1980] F. Stern, “Calculated temperature dependence of mobility in silicon inversion layers”, Phys. Rev. Lett., Vol. 44, pp. 1469-1472, 1980.

[Sugino-1982] M. Sugino, L.A. Akers, and M.E. Rebeschini, “CMOS latch-up elimination using schottky barrier pMOS”, IEDM, pp 462–466, 1982.

[Schwarz-2011] M. Schwarz, T. Holtij, A. Kloes, B. Iñíguez, “2D Analysis of source/drain carrier tunneling in lightly doped Schottky barrier DG-MOSFETs using a fully analytical model”, 12th International conference on Ultimate Integration on Silicon (ULIS), pp. 1 – 4, 2011.

[Sze-2007] S.M. Sze and K. Ng. Kwik, “Physics of Semiconductor Devices”, Third Edition, by John Wiley & Sons, 2007.

[Takagi-1994] S. Takagi, A. Toriumi, M. Iwase, H. Tango, “On the universality of inversion layer mobility in Si MOSFET's: Part I-effects of the substrate impurity concentration”, IEEE Trans. Electron Devices, Vol. 41, nº 12, pp. 2357-2362, 1994.

[Takagi-2008] S. Takagi, T. Iisawa, et al, “Carrier-Transport-Enhanced Channel CMOS for Improved Power Consumption and Performance”, IEEE Trans. on Elec. Dev., 10 (1), pp 21-39, 2008.

[Tanaka-2000] T. Tanaka, T. Usuki, T. Futatsugi, Y. Momiyama and T. Sugii, “Vth Fluctuation induced by statistical variation of pocket dopant profile”, IEEE International Electron Devices Meeting, pp. 271-274, 2000.

[Taur-1998] Y. Taur and T. H. Ning, “Fundamentals of Modern VLSI Devices”. Cambridge, U.K.: Cambridge Univ. Press, 1998.

[Taur-2001] Y. Taur, "Analytical solutions of charge and capacitance in symmetric and asymmetric double-gate MOSFETs", IEEE Transactions on electron devices, Vol. 48, nº 12, pp.2861-2869, 2001.

[Taur-2004] Y. Taur, X. Liang, W. Wang, H. Lu, "A continuous, analytic drain current model for the DGMOSFETs", IEEE Electron Device Letters, 25, 107-109, 2004.

[Tienda-Luna-2008] I.M. Tienda-Luna, F.J. García Ruiz, L. Donetti, A. Godoy, F. Gámiz, "Modeling the Equivalent Oxide Thickness of Surrounding Gate SOI devices with high-K insulators", Solid-State Electronics 52 (12), pp. 1854–1860, 2008.

[Tienda-Luna-2011] I. Tienda-Luna, F. Ruiz, A. Godoy, B. Biel, and F. G´amiz, "Surface roughness scattering model for arbitrarily oriented silicon nanowires," Journal of Applied Physics, vol. 110, p. 084514, 2011.

[Tienda-Luna-2012] I. Tienda-Luna, J.B. Roldán, F. G. Ruiz, C. M. Blanque, F. Gámiz, "An Analytical Mobility Model for Square Gate-All-Around MOSFETs", EUROSOI, 2012 (Eighth Workshop of the Thematic Network on Silicon on Insulator technology, devices and circuits), Montpellier (France), enero 24-25, 2012

[Toriumi-1988] A. Toriumi, M. Iwase, M. Yoshimi, "On the performance limit for Si MOSFET: experimental study", IEEE Transactions on Electron Devices, 35, pp. 999-1003, 1988.

[Trellakis-1997] A. Trellakis, A.T. Galick, A. Pacelli, U. Ravaioli, "Iteration scheme for the solution of the two-dimensional Schrödinger-Poisson equations in quantum structures", Journal of Applied Physics, 81(12), pp. 7880-7884, 1997.

[Trivedi-2004] V. Trivedi, J.G. Fossum, and F. Gámiz, "A compact QM mobility model for nanoscalte ultra-thin-body CMOS devices," in IEDM Tech. Dig., pp. 763–766, 2004.

[Trivedi-2005] V. Trivedi, J.G. Fossum, “Quantum-mechanical effects on the threshold voltage of undoped Double-Gate MOSFETs”, IEEE Electron Device Letters, Vol. 26, nº 8, pp.579-582, 2005.

[Tsividis-1999] Y.P. Tsividis, “Operation and Modeling of the Metal-oxide Semiconductor transistor”, Mcgraw hill, 1999.

[Tsutsui-2005] G. Tsutsui, M. Saitoh, T. Nagunº, T. Hiramoto, “Impact of SOI thickness fluctuation on threshold voltage variation in ultra-thin body SOI MOSFETs”, IEEE Transactions on nanotechnology, Vol. 4, nº 3, pp. 369-373, May 2005.

[Tsormpatzoglou-2009] A. Tsormpatzoglou, D.H. Tassis, C.A. Dimitriadis, G. Ghibaudo, G. Pananakakis, and R. Clerc, “A compact drain current model of short-channel cylindrical gate-all-around MOSFETs”, Semiconductor Science and Technology, 24, 075017, 2009.

[Tucker-1994] J.R. Tucker, C. Wang, and P.S. Carney, “Silicon field-effect transistor based on quantum tunneling”, Applied Physics Letters, 65(5), 1994.

[Uchida-2001] K. Uchida, J. Koga, R. Ohba, T. Numata, S.I. Takagi, “Experimental evidences of quantum-mechanical effects on low-field mobility, gate channel capacitance, and threshold voltage of ultrathin body SOI MOSFETs”, Technical Digest of IEDM, 29.4.1, 2001.

[Uchida-2005] K. Uchida, “Transport in ultra-thin SOI devices”, Sinano Workshop 2005, Grenoble, http://www.sinano.org/index/public/17/workshop2005.html

[Vaddi-2009] R. Vaddi, S. Dasgupta, R.P. Agarwal, “Device and circuit design challenges in the digital subthreshold region for ultralow-power applications”, VLSI Design, 2009.

[Vega-2006] R.A. Vega, “Schottky Field Effect Transistors and Schottky CMOS Circuitry”, M.S thesis in microelectronic Engineering, Rochester Institute of Technology, 2006.

[Vega-2008] R. A. Vega, “A comparative study of dopant-segregated Schottky and raised source/drain double-gate MOSFETs”, IEEE Transaction on Electron Devices, vol. 55, no.10, pp. 2665-2677, 2008.

[Wang-2005] J. Wang, A. Rahman, A. Ghosh, G. Klimeck, and M. Lundstrom, “On the validity of the parabolic effective-mass approximation for the IV calculation of Silicon nanowire transistors,” IEEE Transactions on Electron Devices, Vol. 52, nº 7, pp. 1589–1595, 2005.

[Watts-2005] J. Watts, C. McAndrew, C. Enz, C. Galup-Montoro, G. Gildenblat, C. Hu, R. Langevelde, M. Miura-Mattausch, R. Ríos, C. Sah” Advanced Compact Models for MOSFETs”, Proc. Workshop on Compact Modeling at Nanotech 2005, Anaheim, Vol. WCM, pp. 3-12, 2005.

[Weber-2008] O. Weber and S. Takagi, “Experimental Examination and Physical Understanding of the Coulomb Scattering Mobility in Strained-Si nMOSFETs”, IEEE Transactions on Electron Devices, Vol. 55, pp. 2386-2396, 2008.

[Wittmer-1984] M. Wittmer, K.N. Tu, “Low-temperature diffusion of dopant atoms in silicon during interfacial silicide formation”, Phys. Rev. B 29, 2010 (1984)

[Woltjer-2007] R. Woltjer, L. Tiemeijer, D. Klaassen, “An industrial view on compact modeling”, Solid-State Electronics 51, pp. 1572–1580. 2007.

[Xiong-2005] S. Xiong, T. King, J. Bokor, “A comparison study of symmetric ultrathin-body double-gate devices with metal source/drain and doped source/drain”, IEEE Transaction on Electron Devices, Vol. 52, nº 8, pp. 1859-1867, 2005.

[Xu-2006] B. Xu, Z. Xia, X. Liu and R. Han, “An analytical potential model of double gate mosfet with schottky source/drain”, Proceeding of ICSICT '06. 8th International Conference on Solid-State and Integrated Circuit Technology, pp. 1296-1298, 2006.

[Yan-1988] E. S. Yang. Microelectronic Devices. McGraw-Hill, 1988.

[Yang-2002] M. Y. Jang, J.Oh, S. Maeng, W. Cho, „Characteristics of erbium silicided n-type Schottky barrier tunnel transistors", Applied Physical letters, vol. 83, pp. 2611-2613, 2002.

[Yang-2003] M. Yang, M. Ieong, L. Shi, K. Chan, V. Chan, A. Chou, E. Gusev, K. Jenkins, D. Boyd, Y. Ninomiya, D. Pendleton, Y. Surpris, D. Heenan, J. Ott, K. Guarini, C. D'Emic, M. Cobb, P. Mooney, B. To, N. Rovedo, J. Benedit, R. Mo, and H. Ng, "High performance CMOS fabricated on hybrid substrate with different crystal orientations", in IEDM, pp. 453-456, 2003.

[Zhang-2005] M. Zhang, J. Knoch, Q.T. Zhao, S. Lenk, U. Breuer, S. Mantl, „Shottky barrier height modulation using dopant segregation in Shottky-barrier SOI MOSFETs", Proc. Eur. Solid State Device Res. Conf., Conf. Digest, 2005, pp. 457-460.

[Zhang-2008] M. Zhang, J. Knoch, S. Zhang, S. Feste, M. Schröter and S. Mantl, "Threshold voltage variation in SOI Schottky-barrier MOSFET", IEEE Transactions on Electron Devices, Vol. 55, n° 3, pp. 858-865, 2008.

[Zhu-2010] G. Zhu, X. Zhou, Y.-K. Chin, K. L. Pey, J. Zhang, G. H. See, S. Lin, Y. Yan, and Z. Chen, "Subcircuit Compact Model for Dopant-Segregated Schottky Gate-All-Around Si-Nanowire MOSFETs", IEEE Transanctions on Electron Devices, vol. 57, No.4 p.772, 2010