Universidad de Granada

Tesis Doctoral

Desarrollo de herramientas de simulación para micro y nano dispositivos.

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Desarrollo de herramientas de simulación para micro y nano dispositivos.

Tesis Doctoral presentada por:

Abraham Luque Rodríguez

para optar al grado de doctor en Ingeniería Electrónica

Granada, 12 de Junio de 2012

Fdo: Abraham Luque Rodríguez

Universidad de Granada

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CERTIFICAN

Que el trabajo de investigación que se recoge en la presente Memoria, titulada "DESARROLLO DE HERRAMIENTAS DE SIMULACIÓN PARA MICRO Y NANO DISPOSITIVOS." presentada por D. **Abraham Luque Rodríguez** para optar al grado de Doctor, ha sido realizado en su totalidad bajo su dirección en el Departamento de Electrónica y Tecnología de Computadores de la Universidad de Granada así como en el centro Interuniversity MicroElectronic Center (IMEC), Lovaina (Bélgica).

Y para que así conste y tenga los efectos oportunos, firman este certificado en Granada, a 12 de Junio de 2012.

Dr. J.A. Jiménez Tejada - Dr. S. Rodríguez Bolívar - Dr. E. Simoen

Simulation tools for micro and nano-device modeling

by

Abraham Luque Rodríguez

A Thesis

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y a mis dos más preciados tesoros, Marisol y Abraham.

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Thanks to all of you,
Abraham

Granada, May 2012

List of Acronyms

1-D	One Dimensional
1T-DRAM	single Transistor Dynamic Random Access Memories
2-D	Two Dimensional
3-D	Three Dimensional
BOX	Buried OXide
BTBT	Band-To-Band Tunneling
CMOS	Complementary Metal-Oxide-Semiconductor
DC	Direct Current
DOS	Density Of States
EMA	Effective Mass Approximation
FD	Fully depleted
FinFET	Fin-shaped Field Effect Transistor
G4FET	Four gate Field Effect Transistor
HK	High-κ
g-r	Generation-Recombination
I-V	Current-Voltage
JDOS	Joint Density Of States
JFET	Junction Field Effect Transistor
LED	Light-Emitting Diode
LFN	Low Frequency Noise
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PD	Partially depleted
PSD	Power Spectral Density
QD	Quantum Dot

QD-IBSC	Quantum-Dot Intermediate Band Solar Cell
QDIP	Quantum-Dot Infrared Photodetector
QW	Quantum Wire
RMS	Root-Mean-Square
S/D	Source/Drain
SIMOX	Silicon IMplanted with Oxygen
SOI	Silicon On Insulator
SRH	Shockley–Read–Hall
SS	Subthreshold Swing
STI	Shallow-Trench Isolation
TAT	Trap-Assisted Tunneling
TEM	Transmission Electron Microscopy
UFNM	Unified Flicker-Noise Model
UTBOX	Ultra-Thin Buried OXide
VAF	Variance-Accounting-For
WKB	Wentzel-Kramers-Brillouin

List of Symbols

Symbol	**Unit**	**Description**
A	m^2	Area
c_{light}	m/s	Speed of light in vacuum
c_n	cm^3/s	Electron thermal-capture rate
c_p	cm^3/s	Hole thermal-capture rate
E_C	eV	Conduction band minimum
E_F	eV	Fermi energy level
E_G	eV	Band gap
E_i	eV	Intrinsic energy level
E_n	eV	Eigenenergy
E_T	eV	Energy of a trap level
E_V	eV	Valence band maximun
$\hbar$	eV·s	Reduced Planck constant
H	-	Hamiltonian operator
i	-	imaginary constant
I	A	Current
J_A	A/cm^2	Area current density
J_P	A/cm	Peripheral current density
k	eV/K	Boltzmann constant
g_m	S	Transconductance
L_D	m	Debye's length
L_{sc}	nm	Side length of the supercell
L_{qd}	nm	Side length of the quantum dot
m*	kg	Effective mass
m_0	kg	Electron rest mass

m_{ma}	kg	Effective mass of the matrix material
m_{qd}	kg	Effective mass of the quantum dot material
m_R	-	Reduced mass
n	cm^{-3}	Electron concentration
n_i	cm^{-3}	Intrinsic carrier concentration
n_{ie}	cm^{-3}	Effective intrinsic carrier concentration
n_r	-	Mean refraction index
N_A	cm^{-3}	Acceptor concentration
N_D	cm^{-3}	Donor concentration
N_T	cm^{-3}	Trap density
p	cm^{-3}	Hole concentration
P	m	Perimeter
q	C	Electron charge
$\vec{q}$	-	Wave vector related to the supercell periodicity
S_I	A^2/Hz	Power spectal density of the current
S_{xx}	Pa	Stress component
T	K	Temperature
T_{op}	-	Kinetic energy operator
U_{GR}	$cm^{-3}s^{-1}$	Generation-Recombination rate
v_{th}	cm/s	thermal velocity
V_{DS}	V	Drain to source voltage
V_G	V	Gate voltage
V_{JG}	V	Lateral junction-gate voltage
V_{op}	-	Potential energy operator
α	cm^{-1}	Absorption coefficient
ΔE_G	eV	Band gap variation due to stress
ϵ_0	F/cm	Dielectric constant of vacuum
γ	cm^{-1}	Tunneling coefficient
$\Gamma_{n,p}$	-	Field-enhancement factor for electrons and holes
μ_n	m^2/Vs	Electron mobility
μ_p	m^2/Vs	Hole mobility
Ψ_n	-	Wave function
σ_n	cm^2	Electron capture cross-section
σ_p	cm^2	Hole capture cross-section
σ_{sc}	V·s	Screened scattering coefficient

τ	s	Relaxation time
τ_g	s	Generation lifetime
τ_n	s	Electron lifetime
τ_p	s	Hole lifetime

“An investment in knowledge always pays the best interest”

Benjamin Franklin

Resumen

Muchos de los avances tecnológicos de los que podemos disfrutar hoy en día no se hubieran llegado a alcanzar sin la ayuda de los computadores. Un claro ejemplo se puede encontrar en la industria de los semiconductores, aunque es extensible a muchos otros campos. Un entendimiento detallado de los procesos físicos que se producen dentro de los dispositivos electrónicos no es suficiente para poder predecir o describir el funcionamiento de dichos dispositivos. En muchos casos, la complejidad y entramado de dichos mecanismos hace imposible obtener una solución analítica. Aquí entra en juego el cálculo numérico, el cual encuentra en los ordenadores su mejor baza.

Los simuladores están siendo ampliamente empleados en la industria de los semiconductores no sólo por ser capaces de dar una descripción aceptable del funcionamiento de los dispositivos y reproducir los datos experimentales, sino también por poder emplearse para prever el funcionamiento de estructuras o dispositivos que aún no han sido fabricados.

Esta tesis se centra en el desarrollo y aplicación de herramientas de simulación para micro y nano dispositivos. Dentro de estas herramientas existen tanto herramientas comerciales, actualmente disponibles para llevar a cabo distintos tipos de simulaciones, como otras que han sido expresamente desarrolladas por nuestro grupo. Uno de los principales corolarios obtenidos tras esta tesis es que una combinación de ambos tipos de herramientas es lo que imprimiría más versatilidad y potencia al estudio. Así pues, estas herramientas son empleadas en el estudio de tres temas muy candentes en el campo de la electrónica: i) estudio de las corrientes de pérdidas en heterouniones estresadas de SiGe/Si, ii) caracterización de trampas en transistores multipuerta por medio

de medidas y simulación de ruido, y iii) estudio de la estructura de minibandas y coeficiente de absorción en nanoestructuras ordenadas y periódicas.

En un primer bloque, se estudian las corrientes de pérdidas que tienen lugar en las heterouniones de SiGe/Si estresadas. Si en un transistor convencional de Si se sustituye el material de fuente y drenador por otro que tenga una constante de red ligeramente diferente, por ejemplo SiGe, aparecen unas tensiones mecánicas dentro del material que cambiarían las propiedades físicas de dicho material. Más concretamente, dichas tensiones producen una deformación de los elipsoides, lo que implica una reducción en la masa efectiva de los portadores que hace que aumente la corriente de conducción. No obstante, aunque la corriente de conducción del transistor se ve significativamente mejorada, la presencia de heterouniones hace que las corrientes de pérdidas en el estado de no conducción sean tan significativas que se vea comprometido su funcionamiento. En este sentido, el estudio e identificación de los mecanismos que producen dichas corrientes de pérdidas es muy importante para poder así buscar soluciones y mejorar el funcionamiento de estos transistores.

En esta parte se ha utilizado herramientas comerciales de simulación para llevar a cabo dicho estudio. La simulación de dichas corrientes ha sido llevada a cabo mediante el simulador comercial de dispositivos electrónicos *Medici*. El ajuste entre medidas experimentales y los resultados obtenidos mediante simulación han permitido identificar al mecanismo de generación-recombinación *Shockley–Read–Hall* como el principal causante de dichas corrientes de pérdidas. Este mecanismo depende fuertemente del número de trampas o defectos presentes en el dispositivo a través del parámetro *tiempo de vida media*. De este modo se propone un modelo que relaciona el contenido de germanio del compuesto SiGe y los máximos niveles de tensión mecánica presentes en la estructura con el tiempo de vida media de los portadores. Este resultado pone de manifiesto que los simuladores comerciales poseen carencias que impedirían obtener unos resultados que concuerden con los datos experimentales. Una posible solución sería incorporar manualmente al simulador comercial los nuevos modelos desarrollados. En este sentido, se necesitaría caracterizar previamente las trampas presentes en estos dispositivos para así poder incluirlas dentro de la simulación de la respuesta estática.

En otro segundo bloque se presentan técnicas de caracterización de trampas presentes en transistores con diferentes topologías, utilizando para ello medidas experimentales de la característica estática y de ruido. La detección y caracterización de trampas es una tarea importante y frecuente en el campo de los dispositivos electrónicos pues éstas determinan en muchas ocasiones un adecuado funcionamiento del dispositivo: bajo ruido y bajas perdidas, entre otras características. Cada vez más trabajos destacan que las medidas de ruido complementadas con simulaciones pueden ser utilizadas como una poderosa herramienta para la caracterización de trampas. Las medidas de ruido de baja frecuencia muestran principalmente dos espectros: uno de tipo Lorentziano y otro del tipo *flicker* o $1/f$. La reproducción numérica del primer espectro nos permite caracterizar trampas presentes en el volumen del semiconductor, mientras que el segundo nos ayuda a la caracterización de trampas dentro de los óxidos.

Esta tesis toma como partida el transistor de efecto campo de cuatro puertas (G4FET) donde se desarrollan los modelos necesarios para reproducir las medidas experimentales de ruido. Éste es un transistor multipuerta de reciente creación por lo que hay que adaptar los modelos de ruido para su simulación y estudio. Para llevar a cabo dicha tarea, se emplea un simulador desarrollado por nuestro grupo que resuelve autoconsistentemente las ecuaciones de difusión-deriva y Poisson en dos dimensiones. Empleando dicho simulador y los modelos desarrollados para el ruido se consigue caracterizar las trampas presentes en el volumen y dentro de los óxidos, así como proponer configuraciones donde se optimiza el funcionamiento del G4FET mediante minimización de las figuras de ruido y maximización de la transconductancia.

No obstante, en el proceso de ajuste entre simulaciones y medidas experimentales se encuentran pequeñas divergencias que ponen de manifiesto la necesidad de introducir aproximaciones de segundo orden en los modelos de ruido. Un ejemplo de ello se encuentra en las pendientes del ruido $1/f$ o *flicker*. Experimentalmente se ha observado que dicha pendiente puede variar según $1/f^{\alpha}$, donde $0.8 < \alpha < 1.2$. Esta desviación del comportamiento ideal (α =1) puede ser atribuida a una distribución de trampas dentro de los óxidos no uniformes con respecto a la profundidad. Así pues, incorporando las no uniformidades, este nuevo modelo se aplica a la caracterización de trampas dentro de los óxidos. Se demuestra que su aplicación es también extensible a puertas apiladas de diferentes materiales donde se emplean materiales de alta constante dieléctrica.

Las exigencias de la industria hacen que constantemente se exploren nuevas topologías de transistores de efecto campo, surgiendo de esa manera nuevas aplicaciones y mejoras. Dentro de este grupo podemos enmarcar diferentes transistores multipuerta, como es el caso del mencionado G4FET o los finFETs o el *triple-gate transistor*, ...,etc. Las técnicas de caracterización empleadas en el G4FET se han traladado a otros transistores multipuerta empleados hoy en día en la industria electrónica, como es el caso de los transistores de óxido enterrado de lámina ultradelgada (UTBOX). La motivación del tratamiento de dichos transistores es debida a la utilización de estos transistores para las memorias dinámicas de acceso aleatorio de un solo transistor (1T-DRAM). Esta nueva aplicación promete reducir considerablemente la densidad de integración de las memorias RAM al estar formada su celda unidad solamente por un transistor, eliminando así la voluminosa capacidad de la DRAM convencional.

Uno de los resultados más destacado de esta parte es que la frecuencia de corte del espectro Lorentziano depende del voltaje de puerta. Esto entraría en conflicto con lo ampliamente aceptado para los transistores convencionales. En esta tesis se dan las claves de por qué se observa esta tendencia y cómo se puede aprovechar esta característica en transistores completamente agotados para conseguir realizar espectroscopías a temperatura ambiente caracterizando así más precisamente las trampas presentes en dichos transistores.

Finalmente, en un último bloque, se presenta un estudio de la estructura de minibandas y del coeficiente de absorción en nanoestructuras ordenadas y periódicas. La inclusión de pequeños volúmenes manométricos de un material semiconductor ordenadamente repetidos dentro del seno de otro material semiconductor produce como resultado un nuevo pseudomaterial que tiene propiedades intermedias a las de los dos materiales originales. Además, estas propiedades pueden ser modificadas a conveniencia cambiando la distribución y/o forma del material nanométrico. De esta manera, una de las motivaciones del uso de estos pseudomateriales sería el poder ajustar una determinada propiedad de un material a un valor deseado. Esto lo hace muy interesante en aplicaciones optoelectrónicas, donde se podrían crear fotodetectores o emisores que trabajasen a una determinada longitud de onda deseada.

No obstante, para sacar el máximo rendimiento a estos pseudomateriales es necesaria una mínima cantidad de orden. Hoy en día, pocas técnicas permiten

crear estos pseudomateriales bien ordenados, y las que lo consiguen, no llegan a trabajar con tamaños suficientemente pequeños para observar los efectos cuánticos. Es por eso, que esta tesis pretende anticipar en este tema los resultados y servir como guía para centrar los esfuerzos en determinadas direcciones. Proporcionando unas directrices para obtener los resultados deseados y evitar caminos que no lleguen a un buen provecho.

Estas nanoestructuras se clasifican según el número de dimensiones en el que se realice el confinamiento. Así pues se denomina pozo cuántico cuando el confinamiento es en una dimensión, hilo cuántico para dos dimensiones y punto cuántico para tres dimensiones. En este bloque nos centramos en los dos últimos casos.

El procedimiento y expresiones necesarias para calcular las minibandas y el coeficiente de absorción son presentados en esta parte. Aunque, en un principio se podría calcular la estructura de minibandas que aparece en la banda de conducción y valencia. Nosotros nos centramos solamente en los procesos de absorción intrabanda para la banda de conducción ya que para los procesos de absorción interbanda habría que tener en cuenta interacciones fonón-fotón.

Uno de los resultados más relevantes en este tema es la independencia de la energía umbral para el coeficiente de absorción con el volumen. Los resultados han señalado que puntos cuánticos con igual aspecto (por ejemplo: cúbicos, alargados o aplanados) empiezan a absorber luz a una determinada energía, independientemente del volumen de dichos puntos cuánticos. Esto implicaría que, a la hora de fabricar fotodetectores, la forma del punto cuántico sea más importante que obtener un volumen constante.

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Introduction

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1.1 Computing simulations

Everybody agrees that computers can help people in their daily lives to make complex tasks easier. In this regard, science has changed the way to tackle some problems. One of these fields is semiconductor electronics. The behavior of electrons, holes, and atoms in a semiconductor material can be relatively well described using a certain number of physical equations. The problem is when these equations are not easy to solve analytically and then, one has to turn to numerical methods. At this point, computing simulation provides a huge number of benefits.

One can find two main groups of simulators in semiconductor electronics: process simulators and devices simulators. The former provides the dopant distributions considering as input parameters the configuration (the dose, tilt, energy, ...etc) used in the manufacturing process steps. Generally, these distributions are used as input parameters for the latter simulator. Device simulators can model the electrical, thermal and optical characteristics of semiconductor devices, providing a valuable picture of the device performance. These simulators can work with 1-D, 2-D, or even 3-D devices.

The main benefit of using a simulator is the cost saving in the optimization process. Simulations can reduce the number of prototype devices required before obtaining a final version with an optimal performance. Another important benefit is when one tries to identify the origin of some effects. For instance, the mechanism that produces the leakage currents in a device can be ascribed to different generation-recombination (g-r) processes: Shockley–Read–Hall (SRH), Trap-assisted tunneling (TAT), Band-to-Band tunneling (BTBT),...etc. Depending on which one is the responsible, the origin of these leakages can be attributed to the presence of a high number of traps, high electric fields, high temperatures,...etc, and thus the way to reduce such leakages is different.

However, all these benefits can be overshadowed by one drawback. The models used in the simulator have to describe the system accurately under some established conditions, but these conditions vary. Sometimes the models employed in simulators are limited and can only be applied to certain materials or devices. The huge possible combinations of materials and devices found

in the semiconductor industry make that the development of new models becomes a frequent task. In that sense, simulators have to be calibrated with experimental data frequently, making the experimental and simulation fields to work closely.

Simulators can be used not only for simulating "real" structures or devices, but can be also employed to foresee the behavior or performance of a structure or device which cannot still be created with the current technology. In that sense, the results of a simulation can provide some guidelines to concentrate all the efforts on some direction. However, one cannot be totally sure that the model is working perfectly until a comparison with experimental data is done. That is the case of quantum dots (QDs). For instance, some theoretical works have pointed to QDs as possible candidates for developing intermediate-band solar cells (IBSC) which could obtain a better use of the solar spectrum. Actually, the current technology is not able to achieve such desirable behavior due to the fact that QDs are too big or the amount of disorder is too high. Therefore, simulations can help to identify the best course to follow.

1.2 Main topics

A commercial simulator offers us the reliability of years of experience and a big number of users, who have been checking the models and testing the results. These simulators implement accurate and fast numerical methods to solve the physical equations, optimizing the computational time and the computer resources. These simulators incorporate a large number of models, which combined properly allow us to obtain the electrical, the thermal, or the optical behavior of a device. Despite the large number of models they contain, innovative devices that present new properties or new effects require new or different models. In order to incorporate a new model, a non-commercial simulator is much more versatile due to the control of all its parameters. The development of new tools for simulating micro- and nano-devices has been a common task in our group for many years. The development of our own code means that we are able to gain a further insight into new technological problems that commercial simulators cannot do. Two main simulation lines have been followed in this work

consisting of the computation of Poisson and drift-diffusion equations in 2-D, and the computation of the Schrödinger equation for regimented nanostructures.

This work is divided into three main sections. A first section is dedicated to the use of commercial simulators (Sec. 2). There, we solve technological problems found in experimental measurements, in particular the simulation of the leakage currents in strained SiGe/Si heterojunctions. Sections 3 and 4 are devoted to the development of non-commercial simulators. Section 3 is devoted to noise modeling in different transistors. Section 4 focuses on the simulation of the miniband structure and absorption coefficients for nanostructures.

1.3 Simulators applied to different physical mechanisms in micro- and nano-devices

In this section, we outline the main motivation of working with three topics of interest in micro- and nano-devices and their respective way to treat them by simulations. In some cases, we propose models to be incorporated in commercial simulators. In other cases, a complete simulator is developed in order to tackle a specific issue. We summarize the main advantages and drawbacks of each simulation problem. This section also describes the main lines of these three different topics.

1.3.1 Leakage currents in strained SiGe/Si heterojunctions

A novel interesting topic where process and device simulators (such as TSUPREM4 and MEDICI, respectively) are useful is in contact engineering. SiGe Source/Drain (S/D) contacts are used in Si metal-oxide-semiconductor field-effect transistors (MOSFET) in order to stress the channel and boost the mobility of the conducting carriers. However, an undesirable effect is present in these devices which cannot be ignored. The presence of a heterojunction makes that the leakage currents in the OFF-state of the transistor increase to such levels that the performance of the transistor is degraded.

A process simulator has proved to be an essential part in the simulation

task. This provides more accurate results since more realistic doping profiles are used in the simulations. A better starting point is obtained if we take into account the real doping distribution because some manufacturing processes could change the expected final configuration. This is the case of halo implantations or annealing processes. The metallurgical junctions that may be expected to be located at a certain position can be displaced due to dopant diffusion. However, not always these simulators can be used. In some cases the process steps are unknown, in other cases, models for these particular situations are not implemented. In this case, doping profiles have to be estimated and some approximations have to be considered.

Once the computed or estimated doping profiles are known, a device simulator such as MEDICI is ready to work. A commercial simulator offers a wide range of possible models and type of simulations (e.g. Fermi-Dirac or Boltzmann-Maxwell model, carrier mobility models, complete or partial ionization, g-r mechanism model,...). These simulators also implement fast algorithms to simulate the structures. However, they are limited when a problem or new effect arises. This is the case of the study of the leakage current through strained $Si_{1-x}Ge_x$/Si heterojunctions. The main problem to solve in this structure is how the Ge content impacts on the leakage currents. We will cope with this problem in Sec. 2. There, the lifetime has been identified as the variable that affects the leakage current the most. We have proposed a model that relates changes in the generation lifetimes τ_g as a function of Ge content and recess depth by means of the stress levels. This kind of model is not included in commercial simulators. The creation of bulk defects in the Si substrate close to the heterointerface due to the stress levels is proposed as the main factor that explains the increase in the leakage current. Thus, the characterization of such defects is needed as a complement of our model.

1.3.2 Trap characterization in multigate transistors

The next topic is related to trap characterization in multigate transistors. In this case, a complete simulator is developed and noise models are proposed and checked in different FET structures. A Poisson and drift-diffusion 2-D simulator has been tested on four-gate field-effect transistors (G4FET). In this simulator, DC and low frequency noise (LFN) characteristics of the G4FET are computed.

Essential parameters used in this simulator are those of traps present in the semiconductor. In parallel to the development of the simulator, characterization techniques have also been proposed. In particular, we characterize traps present in the bulk semiconductor or at the Si-SiO_2 interface. Noise measurements combined with simulations are demonstrating to be a convincing powerful characterization tool in MOSFETs, since such a characterization task can be done at room temperatures. The simulator provides accurate distributions of the electrical variables for a transversal cross-section of the G4FET, and hence the experimental noise spectra are well reproduced by simulations. The noise model, initially developed for G4FETs, is applied with excellent results in other FET structures, such as double gate transistors built in Ultra-Thin Buried OXide (UTBOX) Silicon-on-Insulator (SOI) wafers. In this particular case, our noise model is combined with commercial simulators as they offer a better DC approach in these structures. The result of this combination between our model and a commercial simulator has led to a characterization procedure based on the analysis of noise measurements. This characterization task can be migrated to novel more-complex transistors which are capturing the attention for innovative applications such as single transistor dynamic random access memories (1T-DRAM).

In Sec. 3, we present the simulator that computes Poisson and drift-diffusion 2-D equations in order to obtain current-voltage (I-V) curves in a G4-FET. Two models are developed in order to evaluate the drain-current noise power spectral density (PSD) in the G4FET, which are ascribed to g–r noise due to the presence of traps in the depletion regions of the device and 1/f noise due to traps located at the SiO_2/Si interfaces.

There are voltage ranges where one of these sources clearly dominates and other ranges where a combination of the two sources is present and makes it difficult to interpret experimental results. Using these models, we have reproduced the experiments and confirmed the different origins of the noise. It has been tested on different operating modes of the transistor and gives an explanation of the experimental measurements carried out by other authors. The traps present in the device have been characterized by means of the reproduction of experimental I-V and LFN curves.

Subsequently, we present an improved version of the noise model (Sec. 3.5). It is useful in order to reproduce second order effects and in order to be applied to other devices. In this regard, we have developed a $1/f^{\alpha}$ flicker noise model with variable frequency slope $\alpha = 1$, which has closed analytical form and is based on gradients in the gate oxide trap density. The model is initially developed for G4FETs but is also applicable to isolated-gate FETs with high-κ (HK) double-dielectric gate stacks.

The simulation of the G4FET including this advanced model for the $1/f^{\alpha}$ noise is followed by an optimization study of this structure. We have considered variations of the metallurgical boundaries of the junction gates in our facet simulator, which allowed identifying that the junction gate has to penetrate under the MOS gate in order to improve the performance of the G4FET, lowering the subthreshold swing (SS) and the LFN. The improvement is due to reduction in the depletion volume, lowering the number of g-r centers, which are not favorable for the G4FET, because the g-r centers increase the leakage, subthreshold slope, and LFN with Lorentzian shape of the spectrum in the G4FET.

A model for g-r noise produced by bulk traps in fully-depleted (FD) Silicon-On-Insulator (SOI) MOSFETs is also developed in this section. The most remarkable result is that the characteristic time associated to a trap depends on the applied gate voltage, unlike g-r noise produced by traps in the depletion region of bulk and partially depleted SOI MOSFETs. This behavior of the characteristic time leads to specific variations of the corner-frequency and plateau value of the g-r spectra as a function of the gate voltage. This specific variation with gate voltage allows for a better characterization of traps in FD SOI MOSFETs and may in principle be extended to 3-D fin-type transistors. The structures resulting from two different ways to fabricate the S/D regions have been analyzed in this work. At the same time, characterization problems associated to the presence of more than one trap or traps with different energy levels have been solved satisfactorily.

1.3.3 Miniband structure and absorption coefficient in regimented nanostructures

The last topic of this work is analyzed under a different perspective. In many cases, models and simulators are tested with experimental data. In other cases, their results are known before experimental data can be taken, as technology cannot provide this information. Therefore, simulation results act as the forefront of the technology. The technology is progressing so quickly in reducing sizes that quantum effects in novel devices are not negligible anymore. This is the case of the nanostructures studied in Sec. 4.

A 3-D simulator that computes the Schrödinger equation in order to obtain the band diagrams of regimented nanostructures is the third research line presented in this work. These nanostructures are semiconductor materials of nanometric sizes embedded in a matrix of other semiconductor materials. Consequently, different effective masses have been considered in the simulations for each material. The possible effects of strain have also been considered by means of the respective band offsets between materials in the conduction and valence bands. Although this simulator is able to compute the miniband structures arising from the conduction and valence bands, the work presented in Sec. 4 focuses on those produced only in the conduction band owing to only the intraband absorption coefficient is computed. In the interband absorption coefficient, the interactions with phonons are needed to compute indirect transitions. This fact requires the development of new models, and it is a topic for future consideration. The motivation of developing such a simulator is due to the interest aroused by these nanostructures (quantum dots, quantum wires, nanoribbons,...etc) in many fields of science, but mainly in optoelectronics. With these new nanostructures, the door to tunable materials is open. This means that one could be able to select some physical properties controlling sizes and shapes of these nanostructures, creating in that way a new kind of "pseudomaterial". However, although some devices based on these concepts have been manufactured, to obtain the maximum profit from these nanostructures a high degree of order is essential. In this regard, the current technology cannot obtain well-ordered structures and with small enough sizes in order to observe the quantum effects. However, the study presented in this work aims to obtaining some guidelines to create such nanostructures that behave in the way

that one expects. Therefore, we explore the effects of dimensions and shapes on the miniband structures and absorption coefficient for different nanostructures.

In this work, we investigate the solution of the Schrödinger equation for periodic nanostructures and study photon absorption by electrons in a periodic nanostructure based on quantum wire (QW) and quantum dots (QD) nanostructure arrays. We present results that shed light on the physics of these systems. Regarding computational implementation, we show data about the convergence of the calculations as a function of the number of plane waves used in the expansion and have explored the conditions for obtaining suitable values. We have also evaluated the miniband structure of electrons in the system for several nanostructure sizes, shapes, volumes and inter-dot distances, observing the presence of miniband gaps due to quantization, which could be useful in optoelectronic applications.

Our results are compared with those obtained from a 3-D Kronig-Penney model with different effective masses in the dot and the barriers, proving that this analytical approach may be useful only for cases where barriers are noticeably smaller than QD, but inadequate for investigating the general case, where our description would be more accurate.

We also carry out calculations on the absorption coefficient by electrons in doped and undoped semiconductors to check the effect of the Fermi level position and for light polarizations in different orientations. The results suggest the existence of well-defined energies determined by the miniband structure of the system where photons are absorbed for certain light polarizations. These threshold energies are in the far infrared region and could be useful for the future development of photodetectors in that region of the electromagnetic spectrum.

Our theoretical investigation suggests these systems may be useful in optoelectronic applications because of their absorption coefficient and also the possibility of removing the carriers after photon absorption through the second miniband of the structure. Carrier transport along the minibands is possible, in contrast with photon absorption by single impurities or single dots. Thus, these systems could be useful for manufacturing quantum dot infrared photodetectors (QDIP). Further, we believe that this type of structure could play an important role in designing intermediate band solar cells (IBSC). It would be important to achieve the periodic arrangement of the dots in order to obtain the miniband

structure and to investigate the implications of using different materials in the dot and matrix, in order to find the absorption thresholds of interest for these applications

Further, it has been shown that the absorption coefficient has a threshold independent of the QD volume in the range 128 nm^3 – 432 nm^3. In consequence, we suggest that the conditions to achieve a certain threshold might merely be based on achieving the regimentation and the right shape of the QD in certain regions of the sample (like a polycrystalline material). Changes in QD size along the sample could not influence the threshold, as shown in the results. In conclusion, the same threshold would be found for perfect 3-D lattices and for "polycrystalline" 3-D lattices with changes in QD volumes between points of the same sample.

2

Leakage currents in strained SiGe/Si heterojunctions (models adapted to commercial simulators)

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2.1 Introduction

A study of the impact of the Ge content and the recess depth on the leakage current of strained $Si_{1-x}Ge_x$/Si p^+n heterojunctions is presented in this chapter. A rise in the current, when the Ge content increases and/or the recess depth decreases, is experimentally observed. An analysis of the physical variables involved in the leakage current at low electric fields is carried out. The Shockley–Read–Hall (SRH) lifetime is identified as the variable that affects the leakage current the most [1]. Changes in the lifetimes are correlated to changes in the Ge content and the recess depth ($Si_{1-x}Ge_x$ thickness) by means of modification of the stress levels. An expression that directly relates the values of the lifetimes with the Ge content is proposed.

The presence of heterojunctions in current semiconductor devices is quite common since the implementation of different materials is required to improve their performance in line with the International Technology Roadmap for Semiconductors. That is the case for strained-silicon (ϵ-Si) p-channel MOSFETs (pMOSFETs) [2], where an enhancement factor of the hole mobility over bulk Si of ~ 2 is observed [3] and even greater factors are expected in optimized heterostructures [4]. This improvement is induced by the compressive uniaxial strain in the silicon, resulting from the growth of embedded $Si_{1-x}Ge_x$ (e-SiGe) in the S/D contacts [see Fig. 2.1a] [5]. In spite of the achievements on drive current/performance improvement, there are some undesired effects, such as an increased leakage current through the substrate in the off-state [6].

The S/D doping plays an important role in the device performance [7]. Two types of doping techniques have been considered in the formation of the S/D junctions in complementary metal-oxide-semiconductor (CMOS) technology. One is the *in-situ* boron doping during the growth of the e-SiGe S/D and the other is a boron implantation after the creation of an undoped e-SiGe contact layer. The first one has shown to produce higher drive currents, owing to higher levels of stress in the Si channel and lower parasitic resistance [8]. It is also a promising technique for the further miniaturization of the devices since the stress level increases as the MOSFET channel length decreases. However, the presence of a heterojunction produces high levels of undesired leakage current [9]. That is why boron implantations are preferred in the present CMOS nodes, due to the fact that this technique allows the electrical p^+-n junction

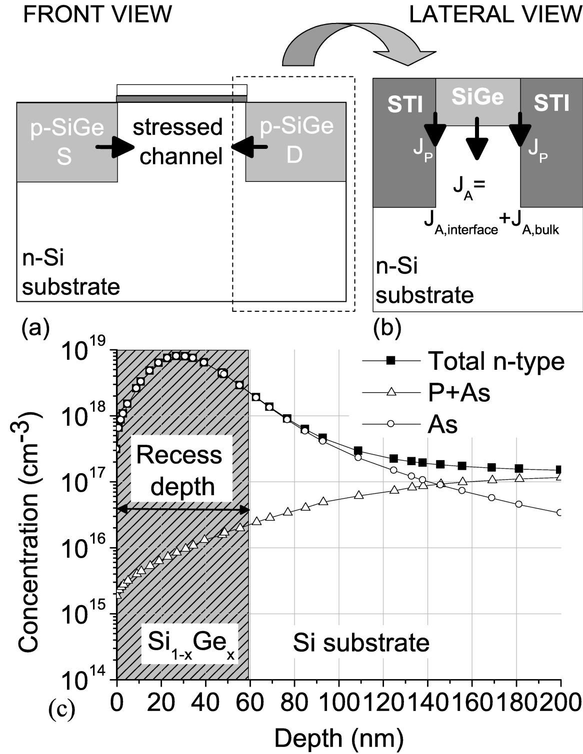

Figure 2.1: (a) Structure of a pMOSFET with a stressed channel. (b) Detail of an isolated heterojunction and the two components of the current in reverse bias operation: areal current density (J_A) and peripheral current density (J_P). (c) Doping profile in the n-well Si-substrate prior to the etching and after two kinds of implantations: deep phosphorous and arsenic implantations and shallow halo arsenic implantation. The gray region is the part of the substrate that is subsequently etched out and refilled with a SiGe alloy layer

to be moved away from the SiGe/Si heterointerface. Good understanding and control of the processes involved in the leakage current through a heterojunction are required in order to be able to take advantage of the intrinsic benefit of the *in situ* B-doped e-SiGe S/D.

Previous studies of the leakage current in *in situ* B-doped e-SiGe S/D have been carried out by Bargallo et al. [6]. For the studied devices, extra halo implantations are incorporated in the n-type substrate. These are essential in

the CMOS transistor in order to keep the short-channel effects under control. In this case, an increase of one decade in the leakage current is noticed when the Ge content is increased by 8% [10]. Initially, this rise in the current might be ascribed to strain-induced changes in the conduction and valence bands and, therefore, in the intrinsic carrier concentration, due to the fact that this variable exponentially increases with the band gap.

In this chapter, we analyze the possible origin of such an increment in the leakage current. To carry out this task, we have employed commercial simulators to simulate the structures and their electrical properties. It is shown that stress-induced changes in the intrinsic carrier concentration are not large enough to produce the observed increase in the leakage current. A detailed study shows that a modification of SRH lifetimes associated to traps and defects near the heterojunction can explain such a behavior. The effects on the lifetime either by changes in the deep-level parameters or by the creation of irreversible stress-induced defects have been considered in the past [11–13]. An enhancement of the stress appears to be the origin of these changes in the lifetime.

At the same time, the stress level can be technologically controlled by the Ge content and the recess depth of the e-SiGe layer. In this chapter, a study of the areal current density in strained $Si_{1-x}Ge_x$/Si heterojunctions has been carried out. Experimental data have been analyzed with simulation tools in order to identify the main parameters responsible for the higher leakage currents.

2.2 Experimental and simulation tools

The analysis of the leakage current flowing through the heterojunction under reverse bias is the main objective of this section. In order to avoid other mechanisms involved in the transistor leakage (e.g., gate-induced drain leakage), which are not the scope of this section, isolated heterojunctions are studied. These isolated heterojunctions also avoid the problems associated to the degradation of the side-wall interface of the SiGe/Si heterojunctions in the S/D regions, in comparison with the bottom-wall interface. A recess shape influences defect generation in the SiGe and the strain in the channel region of

the MOSFET [14]. In current CMOS technology, sigma-Σ shaped recess is a way to *in situ* control these problems.

The heterostructures are *in situ* B-doped ($\sim 10^{20}$ cm^{-3}) $Si_{1-x}Ge_x$ layers, epitaxially grown in the active regions of recessed (100) Czochralski (Cz) silicon wafers. The active regions are defined by Shallow-Trench Isolation (STI) as shown in Fig. 2.1b. The Ge concentration of the $Si_{1-x}Ge_x$ is varied between 20 and 40%, and the recess depth varies between 50 and 90 nm. Figure 2.1c shows the simulated doping profile in the n-well substrate prior to the Si etching, resulting from two kinds of implantations: deep phosphorous and arsenic implantations and a shallow arsenic implantation, the latter is the aforementioned halo implantation. A homojunction of Si-Si and a heterojunction both without halo implantation have also been included in this study as a reference.

The study of these structures is carried out mainly by simulation tools. The TSUPREM4 2-D [15] process-simulator provides the doping profiles and stress components in the structure whereby the experimental process conditions are used as input parameters. These results are then exported to MEDICI device simulator [16]. The stress components are used as input parameters for the calculation of the stress-induced band gap narrowing. MEDICI computes the conduction band edge shifts using the deformation potential theory [17], and the valence band edge shifts using the 6×6 $veck \cdot \vec{p}$ perturbation theory [18] in the silicon substrate. The SiGe region is treated with a model that relates the shifts in the band with the Ge content, taking the mismatch strain with respect to the silicon substrate into account [19]. Once the doping profiles and stress-reduced band gap are calculated, the evaluation of the leakage current in the heterojunction is feasible. Different physical mechanisms have been taken into account to evaluate the leakage current in the heterojunctions, i.e., conventional SRH recombination via traps [20], [21], trap-assisted tunneling (TAT) [22], and band-to-band tunneling (BTBT) [23]. However, the samples have been analyzed in the low electric field regime in order to avoid the dominance of the last contribution, to minimize the effect of the second one, and thus, to isolate the effect of basic parameters such as the SRH lifetimes.

To simulate the typical SRH and TAT components, a deep trap model is

required. A bulk trap located at midgap with equal values for electron and hole SRH lifetimes ($\tau_n = \tau_p = \tau$) is used as possible origin of these leakage currents. This kind of trap can be related to oxygen precipitation in Cz-grown Si wafers [24]. The position of the trap is also chosen taking into account the conclusions of a temperature study of the samples [6]. The activation energies (~ 0.56 eV) obtained experimentally at room temperature for reverse voltages ≤ 1.2 V are related to the SRH mechanism [9]. It is well known that the most effective recombination center is located at midgap, $E_T = E_C - 0.56$ eV ($E_{TRAP} = 0$, where E_{TRAP} is the distance between the deep trap energy level and the intrinsic Fermi energy ($E_{TRAP} = E_T - E_{Fi}$)), provided the hole and electron lifetimes are the same [25]. However, when τ_n and τ_p are different, the most effective recombination center would be displaced from midgap [24, 26, 27]. In any case, similar conclusions can be reached for other centers with different lifetimes $\tau_n \neq \tau_p$. Additionally, the model used for the TAT mechanism requires one extra physical parameter, the effective mass of the carriers m^*. A generally accepted value of relative mass in Si $m_R = 0.25$ ($m^* = m_R m_0$) is used [22], where m_0 is the electron rest mass.

2.3 Results

2.3.1 Current-Voltage measurements

To carry out this study, measurements of the leakage current are taken for different values of Ge content and recess depth, the two technological parameters under test. The SiGe surfaces are very difficult to passivate [28]. This fact is especially apparent for the SiGe-STI interfaces, where surface defects present in the peripheral regions of the S/D lead to the so-called peripheral leakage current density J_P (Fig. 2.1b). The remaining of the leakage current comes from the areal leakage current density J_A. The origin of the J_A can be associated to traps or defects created in the bulk of the depletion region of the Si-SiGe heterojunction, or it can be produced by surface traps at its heterointerface, $J_A = J_{A,bulk} + J_{A,interface}$. This work focuses on the J_A, and both experimental data and simulation results will be analyzed. The J_A is extracted from the total current, based on the extraction procedure outlined elsewhere [9], [29], [30]. It consists of measuring the leakage current I in junctions with different area A to

perimeter P ratios:

$$\frac{I}{A} = \frac{P}{A} \cdot J_P + J_A. \tag{2.1}$$

The leakage current is related to the generation-recombination (g-r) rate U_{GR} under stationary regime. An inspection of its expression enables to determine the variable that affects the leakage current the most [22]:

$$U_{GR} = \frac{n(x)p(x) - n_{ie}^2}{\frac{A_1\tau_p}{(1+\Gamma_p)} + \frac{A_2\tau_n}{(1+\Gamma_n)}}, \tag{2.2}$$
$$A_1 = n + n_{ie}e^{\left(\frac{E_{TRAP}}{kT}\right)},$$
$$A_2 = p + n_{ie}e^{\left(\frac{-E_{TRAP}}{kT}\right)},$$

where n and p are the electron and hole concentrations, respectively, $\tau_{n,p}$ are the SRH lifetimes for electrons and holes, $\Gamma_{n,p}$ is the field-enhancement factor for electrons and holes due to the TAT mechanism (see page 2.6 in [16]), and n_{ie} is the effective intrinsic carrier concentration. Since the stress-induced band gap narrowing is included in the simulation, an exponential relationship between the n_{ie} and band gap variation is expected [10], [31]:

$$n_{ie} = n_i e^{\frac{-\Delta E_G}{2kT}} \tag{2.3}$$

with k the Boltzmann's constant, n_i the intrinsic carrier concentration and T the temperature.

In reverse bias, the maximum contribution of U_{GR} to the leakage current is achieved inside the depletion region, where n, $p \ll n_{ie}$. Assuming a g-r center positioned at midgap, this maximum contribution can be approximated by:

$$U_{GR_{max}} = -\frac{n_{ie}}{\tau_g}(1+\Gamma) \tag{2.4}$$

where $\tau_g = \tau_n + \tau_p = 2\tau$ is the generation lifetime as $U_{GR} < 0$, and $\Gamma = \Gamma_n = \Gamma_p$ since n, $p \ll n_{ie}$. This simplified expression for the U_{GR} rate allows identifying the variable that is the origin of an increase of one decade in the leakage current when the Ge content is increased by 8%, as shown in experimental results.

A 1-decade rise in the leakage current when the Ge content is increased by 8% could be ascribed to an increase of one decade in the intrinsic concentration

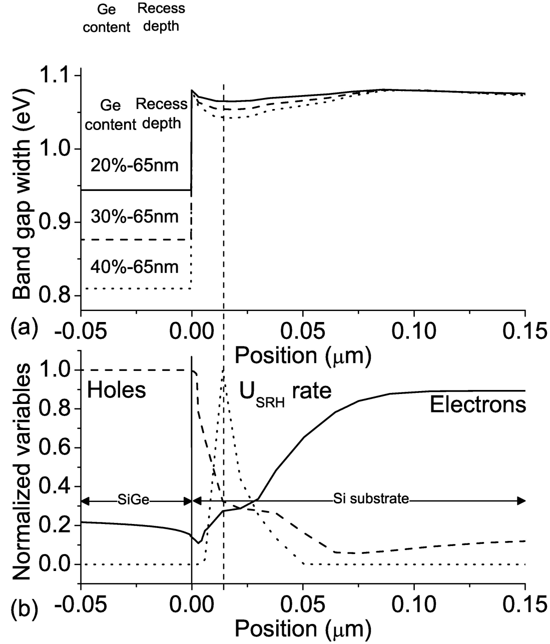

Figure 2.2: a) Band gap width along the structure for three different samples, b) electron and hole concentrations and U_{GR} rate along the sample with 30% Ge content and 65nm recess depth at V_R=1.0 V.

(2.3) ($n_{ie}/n_i = 10$). Thus, a variation in the band gap of $\Delta E_G = 0.116$ eV would be necessary for this increase to take place. In Fig. 2.2a, the simulated band gap is plotted for three different cases: 20%, 30%, and 40% of Ge content. Noticeable changes in the band gap width within SiGe are shown, while minor variations seem to be produced inside the Si. The absolute value of the simulated U_{GR} and the electron and hole distributions for the 30%-65nm sample biased at V_R=1.0 V are plotted in Fig. 2.2b. The greatest change in the band gap width is observed in the SiGe region. However, the high level of holes in this p^+ region produces a negligible U_{GR} rate (2.2). It is important to remark that the maximum of the U_{GR} rate is achieved within the Si-substrate layer where the changes in the band gap are much smaller than the 0.116 eV required to produce the rise of one decade in the leakage current.

Another parameter which could be responsible for the rise in the leakage

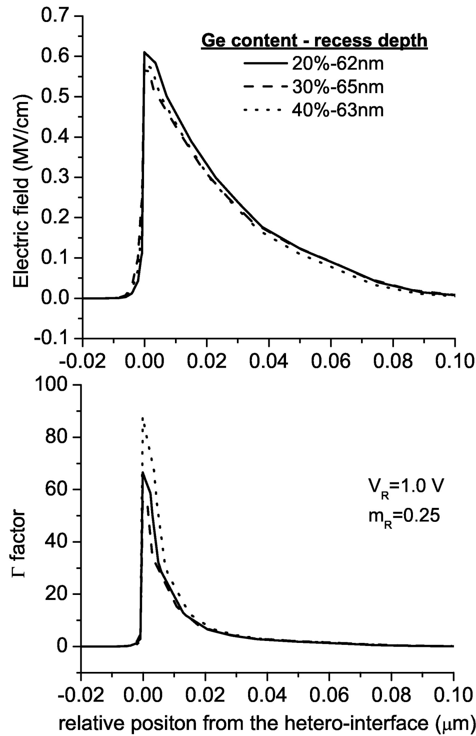

Figure 2.3: a) Distribution of the electric field and b) the TAT enhancement factor, Γ, along structures with different Ge content and recess depth.

current is the Γ factor. This factor varies as a function of the electric field. After analyzing two samples with the same recess depth and different Ge contents, one observes that they have nearly the same doping profile and hence, the same intrinsic electric field. In the cases under test, the recess depth is slightly different for the three samples considered in the experiments (%Ge content - recess depth: 20%-62nm, 30%-65nm, and 40%-63nm). However, the distribution of the electric field in these cases differs only slightly (Fig. 2.3a). The small differences in the electric field among the three cases are not enough to produce variations of one decade in the Γ factor (Fig. 2.3b). The maximum difference is found between the samples (20%-62nm) and (30%-65nm) to be $\Gamma_{20\%-62nm}/\Gamma_{30\%-65nm}$=1.57.

As a result of this analysis on the intrinsic concentration and the Γ factor,

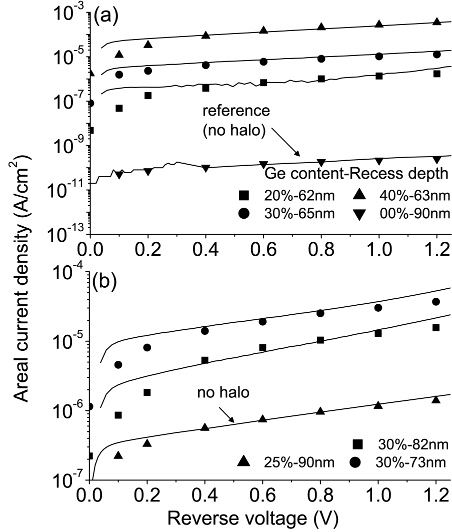

Figure 2.4: Comparison between experimental (solid lines) and simulated (symbols) current-voltages curves for the areal current density (J_A) in samples with (a) different Ge content and (b) recess depth.

equation (2.4) points to the τ_g as responsible for the increment in the leakage current. In that sense, current-voltages (I-V) curves are calculated numerically for different values of the τ_g and compared to the experimental data. The objective is to find a correlation between the Ge content and the recess depth with the lifetimes, through the best fitting of the experimental with the numerical I-V curves.

Figure 2.4 shows the comparison of the experimental J_A versus reverse bias (solid lines), with our simulation results (symbols). The simulated data shows a good agreement with the experimental curves in the range of voltages typically used in CMOS technology. An increase of the current at a rate of about 1 decade when the Ge content is increased by 10% is shown in Fig. 2.4a, even when the recess depth is kept practically constant. The leakage current measured in a homojunction is also represented as a reference (down triangles). We can observe a difference of four decades compared to the 20% case. This difference is attributed to the combination of a decrease of Ge content and a lower electric field in the sample due to the absence of the halo implantations. The effect

of the electric field can be also observed by varying the recess depth. This parameter plays an important role in the leakage current, since it largely controls the doping level at the heterojunctions by means of etching out part of the halo implantation. This fact is seen in Fig. 2.4b. The values of the lifetimes which produce the best fitting of the experimental data with the simulations are summarized in the fifth column of Table 2.1.

Table 2.1: Generation lifetimes determined from the experimental data by simulation for samples with different Ge content and recess depth. The maximum values for the simulated stress level, S_{xx}, in the silicon region are also given.

#	Structure	% Ge content-Recess depth	halo	τ_g (s) (Numerical)	Max S_{xx} (GPa)
1	SiGe/Si	20%-62nm	Y	3.5×10^{-8}	0.406
2	SiGe/Si	30%-50nm	Y	2.0×10^{-9}	0.586
3	SiGe/Si	30%-65nm	Y	4.3×10^{-9}	0.712
4	SiGe/Si	30%-73nm	Y	1.2×10^{-9}	0.746
5	SiGe/Si	30%-82nm	Y	2.5×10^{-9}	0.748
6	SiGe/Si	40%-63nm	Y	2.5×10^{-10}	0.947
7	SiGe/Si	25%-90nm	N	1.9×10^{-8}	0.617
8	Si/Si	0%-90nm	N	1.2×10^{-4}	0.000

2.3.2 Generation lifetime *vs.* technological parameters

Figure 2.5a shows the values of τ_g represented as a function of the Ge content in the SiGe alloy. An exponential relationship between τ_g and the Ge content is observed:

$$\tau_g(\%Ge) = 10^{-(0.15x+4)}, \tag{2.5}$$

where x represents the %Ge. The higher the Ge content introduced in the alloy, the lower the value of τ_g obtained in this analysis. In Fig. 2.5, a sample without halo implantation (25%-90nm, sample # 7 in table 2.1) has also been included in order to check the effect of the halo implantation on the creation of g-r traps. The halo implantation introduces defects which may not be completely removed by the subsequent spike annealing. However, the fact that this sample follows the same trend means that the changes in τ_g cannot be attributed to the halo implantation damage.

On the other hand, neither the 25%-90nm diode nor the 0%-90nm homo-

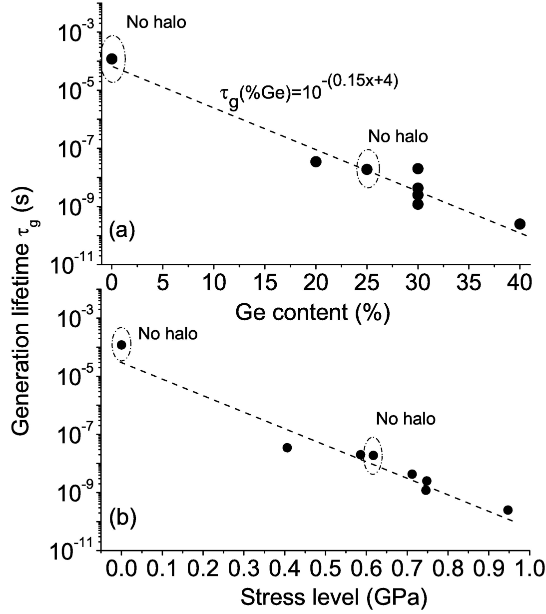

Figure 2.5: Generation lifetime as a function of (a) Ge content and (b) maximum stress level inside the Si-substrate.

junction (Si-Si) diode have a halo implantation (samples # 7 and # 8 in table 2.1 respectively), and the only difference between both diodes is the 25% of Ge content included in the growth of the p^+ layer for the sample # 7. However, an important impact of the position of the heterojunctions on the τ_g value is observed giving rise to a decline in τ_g of ~4 decades.

The group of samples with 30% of Ge content shows a high dispersion in the value of τ_g. The difference between these samples is the recess depth. Several authors, employing different experimental techniques, such as the photoconductive decay method [11, 12], or the analysis of I-V curves from forward-bias, breakdown and reverse-bias regimes [13], proposed a possible link between the stress level and the value of the lifetime. In that sense, Figure 2.5b depicts the dependence of τ_g with the maximum stress level inside the Si-substrate. The maximum stress levels occur in the x direction (S_{xx}) due to the presence of

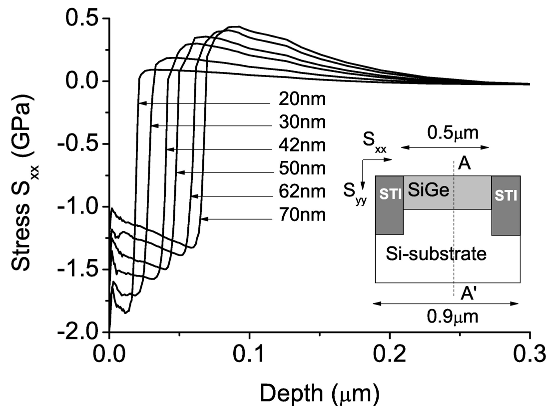

Figure 2.6: Stress component and simulated hetero-structure of several $Si_{0.8}Ge_{0.2}/Si$ samples with different recess depths (line AA' inset). The S_{xx} component is parallel to the hetero-interface.

the SiGe layer and the lateral STI regions (inset in Fig. 2.6). The values of the maximum stress level are summarized in the sixth column of Table 2.1. The group of samples with a 30% Ge content seems to line up, following the dashed line in Fig. 2.5b. A similar dependence of the lifetimes on the stress, Fig. 2.5b, has been obtained by Matukura *et al.* [11,12]. In this case a mechanical uniaxial compressive stress was applied perpendicular to Ge homojunctions.

Although the Ge content is the main responsible for the stress levels within the heterostructure, the thickness of the SiGe layer has an influence on the stress too. Figure 2.6 shows the simulated stress levels through a heterojunction when the Ge content is kept fixed to 20% and the recess depth is varied, consequently varying the thickness of the SiGe layer.

2.3.3 Capacitance measurements

In the previous section a link between the increment of the experimental leakage current and the lifetime, and a correlation between the lifetime and the stress level within the heterostructure have been demonstrated. In a general way, the value of the lifetime is inversely proportional to the capture cross-section σ, the thermal velocity v_{th}, and the density of traps N_T. Under compressive stress

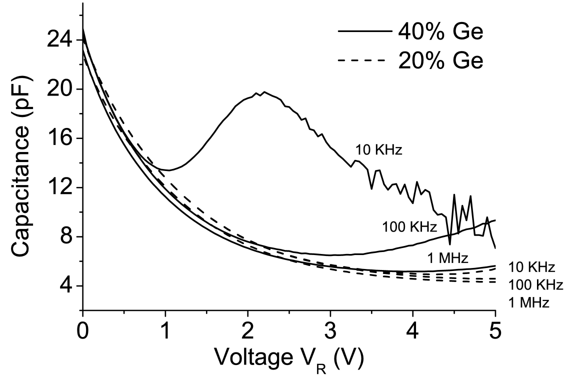

Figure 2.7: Capacitance measurements at different frequencies for two samples with the same recess depth (42nm) and different Ge content (20% and 40%).

up to 1 GPa a variation lower than 20% is theoretically expected for v_{th} [32]. Therefore, v_{th} is assumed to be constant in the present study. Although there are proposed models where σ depends on the stress level by means of the effective masses [33], other reports suggest an influence of the stress on the density of traps [11], [12]. Somehow, the amount of Ge in the alloy causes the lifetimes to decrease due to an increase in the defect density. This fact is also confirmed by means of capacitance-voltage measurements.

Figure 2.7 shows capacitance measurements as a function of the reverse voltage at three frequencies for two samples with the same recess depth (42nm) and different Ge contents (20% and 40%). At high frequencies there is no difference between the two cases. On the contrary, at 10 KHz the capacitance curve for the 40% Ge content case shows a peak that can be attributed to the presence of slow traps or defects in the depletion region [34]. In the case of relaxed $Si_{1-x}Ge_x$ layers, the creation of misfit and threading defects at the heterointerface is obvious. No evidence of relaxation is detected by Nomarski optical microscopy except for the specific case of 40%, confirming the capacitance results [10]. In any case, the S/D areas of transistors with a 30% Ge content have been analyzed by cross-sectional TEM, and very small defects are visible at the SiGe/Si interfaces (Fig. 2.8). However, this does not mean that the underlying Si depletion region is defect free, as observed in Fig. 2.5, where the τ_g for the 30% case lies

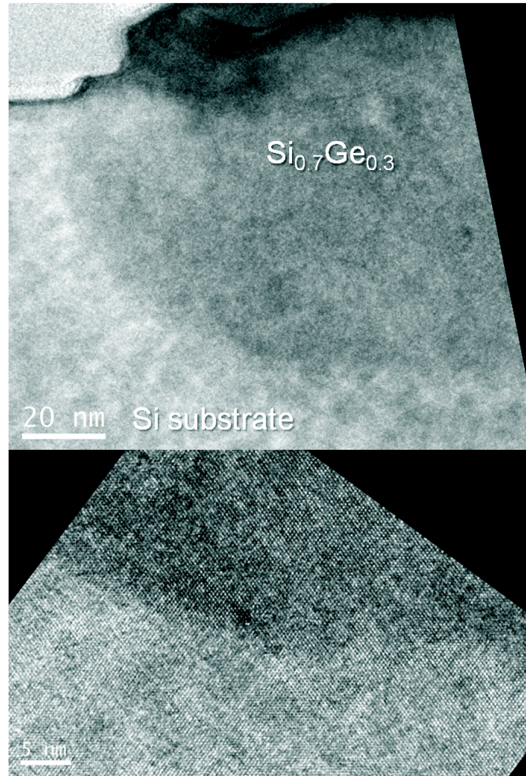

Figure 2.8: TEM cross-section of a $Si_{0.7}Ge_{0.3}$ S/D region for a 60-nm etch depth. Only small defects are present at the SiGe/Si interfaces.

between the corresponding values for the 20% and 40% cases.

2.4 Location of the stress induced defects

The information obtained by analyzing the current and capacitance curves leads to a correlation between the Ge content and stress level with the τ_g. Actually, the τ_g, and hence the SRH lifetime used in (2.2), corresponds to the effective lifetime. In the case of electrons, the values are given by [35]:

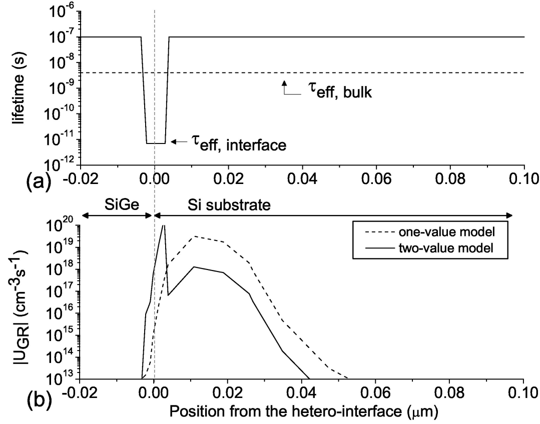

Figure 2.9: (a) Distribution of the generation lifetime along the structure. The one-value situation corresponds to defects distributed uniformly. The two-value case corresponds to a situation where interface defects are favored. (b) Representation of the generation recombination rate (U_{GR}) for a heterojunction with 30% Ge content and a recess depth of 65nm for the two cases depicted in a).

$$\frac{1}{\tau_{n,eff}} = \frac{2S_n}{d} + \frac{1}{\tau_{n,bulk}} \tag{2.6}$$
$$S_n = \sigma_n v_{th} N_{it}$$
$$\tau_{n,bulk} = \frac{1}{\sigma_n v_{th} N_T}$$

where S_n is the surface generation velocity, $\tau_{n,bulk}$ is the bulk lifetime for electrons, σ_n is the capture cross-section for electrons, v_{th} is the thermal velocity for electrons, and d is the thickness of the interface region. Similar expressions are obtained for holes. The variable $\tau_{n,bulk}$ depends on the number of traps per cubic centimeter present in the bulk N_T, whereas S_n depends on the traps per square centimeter localized at the heterointerface N_{it}.

Equation (2.6) points out that the origin of the decrease of the effective lifetime with an increment of the %Ge content can be located either in the silicon bulk or at the heterointerface, going back to the two components of the areal current density $J_A = J_{A,bulk} + J_{A,interface}$. In order to discern between

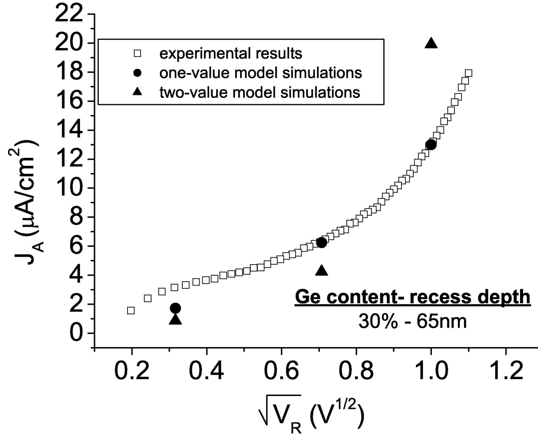

Figure 2.10: The areal current density as a function of the square root of the reverse-voltage applied to the heterojunction for the two situations modeled in Fig. 2.9a.

both regions, a situation different to that considered in Sec. 2.3.1 is analyzed. Section 2.3.1 assumes a constant value of the effective lifetime, $\tau_{eff,bulk}$, along the heterojunction (dashed line in Fig. 2.9a). Here, we compare the previous results with a new situation: a lifetime dependent on the position. In that sense, the lifetime has two values, one in the bulk region (much higher than $\tau_{eff,bulk}$) and a different one, $\tau_{eff,interface}$, in a thin layer of thickness d around the heterointerface (solid line in Fig. 2.9a). The objective is to find reasonable values for d and $\tau_{eff,interface}$ that are able to reproduce the experimental data, as done with the uniformly distributed $\tau_{eff,bulk}$. The dashed line in Fig. 2.9b shows the distribution of the U_{GR} rate obtained for a sample with 30% Ge content and 65 nm of recess depth for the uniform case, with $\tau_{eff,bulk}$ given in Table 2.1. It shows the region where the U_{GR} rate contributes to the leakage current the most. This region does not approach the interface in the whole range of reverse voltages. The solid line in Fig. 2.9b represents the distribution of the U_{GR} rate obtained with the two-value model. The values of d and $\tau_{eff,interface}$ employed in this analysis make the calculated current to overlap with the experimental data (Fig. 2.10).

The leakage current as a function of the depletion width, extracted from

capacitance measurements, is not shown. The reason is that the high doping concentration employed in the heterojunction produces transition regions similar to the depletion width. In any case, the values of the depletion width obtained from capacitance measurements are compared to the values obtained from simulations. A relative error of 29% is obtained. That means that analytical methods based on the experimental determination of the depletion width can accumulate the same error in order to determine the lifetimes [29].

In Fig. 2.10, experimental data of the areal leakage current density versus the square root of the reverse voltage are represented (square symbols). In addition, simulation results using the one-value and two-value models for the lifetime are also depicted. Despite the reasonable agreement obtained with the two-value model, large values for d (far from an interface localization), or very small values for $\tau_{eff,interface}$ (lower than the dielectric relaxation time) are necessary to fit the calculated current to the experimental data. The exact values are not reproduced here for being physically unreasonable. This result points to bulk defects as the most likely candidate responsible for the increased leakage current in the studied structures. We highlight the importance of this simulation study as TEM inspections were not capable to evidence the presence of these defects. Moreover, recent works agree with our conclusions [35], [36]. Defects are created at a certain position within the substrate in $Si_{0.75}Ge_{0.25}/Si$ heterojunctions, reducing the effective lifetime at this region [35]. The origin of these defects, in such structures, appears to be the combination of residual implantation defects after a spike anneal and the thermal stress due to laser annealing. The silicon interstitials created during an implantation step survive the millisecond annealing and could create dislocation loops. The mechanical and/or thermal stress might enhance the creation of those lattice defects. Clean lattice defects that only involve silicon atoms and no contamination introduce in the band gap relatively shallow energy levels of 0.1 eV which are not involved in the leakage processes. However, under a stress field the extended defects tend to attract metallic impurities that introduce deeper levels into the band gap, which modify significantly the effective lifetimes [36].

3

Simulation of multigate transistors: Applications on the Four-Gate Field-Effect Transistors

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3.1 Introduction

The problem associated to short channel effects in MOSFETs is becoming much more important as gate lengths are reduced. As the gate length decreases, the depletion regions of the source-to-body and drain-to-body are getting closer which can produce high levels of leakage current in the off-state. This results in a reduction in the threshold voltage and therefore a loss in the control of the gate over the MOSFET characteristic. The technology has avoided this problem considering higher body doping in order to obtain lower extensions for these depletion regions. However, the increase in the body doping leads to other drawbacks such as lower mobilities, higher capacitances, and higher statistical fluctuations, all of which pose serious challenges to scaling down the devices. An alternate way to increase the gate control over the channel would be to have an extra gate [37]. In that way, the additional gates that border these kinds of transistor reinforce the electrostatic control of the channel and help to strengthen the immunity of the channel from penetration effects of the drain electric field, and avoid the loss due to the constraints imposed by thinning of the Si film [38]. In this approach, the main variable for controlling the channel is not the body doping, but the separation between the gates. In fact the body doping is deliberately kept at a very low value, at near-intrinsic levels [37].The four-gate field effect transistor (G4FET), Fig. 3.1, is one among different multiple gate transistor architectures. Its main advantage is that conducting electrons can be located in the center region of the semiconductor channel far from scattering effects or noise sources located at the Si-SiO_2 interfaces. The control of the conducting channel is done with an appropriate bias of its four independent gates.

In this chapter, we describe a simulator developed by our group that copes with the problems associated to these extra gates analyzing mainly I-V curves from subthreshold to conduction and the noise behavior of the device. The description of the simulator and the structure details are presented in Sec. 3.2.

As the technology is going further in low power consumption, the noise response of a device is getting more important. When the power spectral density (PSD) is measured in these devices two main spectra are obtained: one related to the $1/f$ flicker noise and another Lorenztian spectrum related to

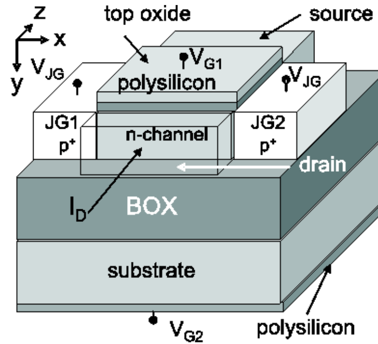

Figure 3.1: Structure of an n-channel G4FET.

the generation-recombination (g-r) noise. Experimental works show that the G4FET achieves low noise figures under certain polarization [39–41] basically due to a suppression of the $1/f$ noise. Therefore, a noise study to explain and reproduce $1/f$ and g-r noise focused on the G4FET is presented in Sec. 3.3 in order to reproduce the experimental PSD measurements both in fucntion of the drain-current or gate-voltage. Consequently, Sec. 3.4 presents a characterization procedure for the G4FET based on the results of the aforementioned noise models.

The noise measurements in these devices complemented with simulations become an interesting powerful characterization tool. Reproducing the I-V and noise response allows us to obtain a clear picture of the traps present in the G4FET. However, some details required further analysis which will be treated in a separated Sec. 3.5 where we present an advanced modeling in order to cope with these problems.

One of these detail is the different behavior of the $1/f$ noise observed in different modes of operation: strict $1/f$ noise has been observed in the accumulation MOS mode while $1/f^{\alpha}$ noise (with $\alpha < 1$) has been observed in the JFET mode. In Sec. 3.5.1.3, the unified flicker-noise model (UFNM) is modified to take into account the effect of non-uniform trap density in the oxides and its subsequent alteration by band bending [42]. Previous authors [43–47] have shown that if the trap distribution, along the region the electrons tunnel into, is non-uniform the frequency dependence of the noise spectrum is of the form

$1/f^{\alpha}$, with α varying with the gate voltage.

Moreover, we will treat other issues such as a characterization method to extract the dopant profile in the channel of a G4FET from experimental I-V curves and low frequency noise (LFN) measurements, Sec. 3.5.1.1. Systematic experimental data and simulations have been carried out in the past that show the bias conditions for optimized performance in these modes [48]. Experiments have also been carried out to test how the DC characteristics of these transistors are highly sensitive to the dopant in the channel. However, the value of the dopant concentration is not the only parameter that affects the behavior of the transistor. How these doping impurities are distributed in the sample, i.e. the dopant profile, is also an important parameter that controls the DC and noise behavior of the device. We also carry out a study of the trap characterization paying attention to the off-state of the transistor where leakage currents can help to identify these traps, Sec. 3.5.1.2. Finally, in Sec. 3.5.1.4, we optimize the dopant profile in the channel of a G4FET in order to achieve the best performance in terms of transconductance-gain and subthreshold-swing parameters and LFN.

The model for the flicker noise with variable spectrum slope developed for G4FETs can be used not only in these structures. In Sec. 3.5.2 we justify the use of this model also in high-κ (HK) gate oxide stacks. The range of frequencies and the low trap density in the native oxide in comparison with the high-κ dielectric make that this model can be applied to these structures.

The last point in the advanced modeling section, Sec. 3.5.3, presents a model for computing the g-r noise due to traps within the semiconductor film of fully depleted (FD) SOI MOSFETs that can be employed using the results of a commercial simulator. In this part, a dependence of the corner-frequency of the Lorentzian spectra on the gate voltage is addressed, which is different to the constant behavior expected for bulk transistors. The shift in the corner-frequency makes the characterization process easier. It helps to identify the energy position, capture cross-sections, and densities of the traps. This characterization task is carried out considering noise measurements of two different candidate structures for single transistor dynamic random access memories (1T-DRAM). However, it may in principle be extended to 3-D fin-type transistors too.

3.2 Structure details and simulator

The G4FET is a flexible-functionality transistor created using SOI technology. This is a combination of an accumulation-mode SOI MOSFET and a JFET in a single transistor with high integration density. As its name indicates, the G4FET is formed by four gates that control the current through the channel. The classical MOS transistor comprises two PN junctions called the source junction and the drain junction. These junctions are separated by a region with opposite doping type. The effective channel length in the MOS transistor is the distance that separates these two junctions. In the G4FET (Fig. 3.1), these junctions play the role of the lateral gates (V_{JG}). The other two gates are the top-gate (V_{G1} in Fig. 3.1), which is the same than in a normal MOSFET, and the bottom-gate (V_{G2} in Fig. 3.1) which is formed by the channel, buried-oxide (BOX) and the back contact. In Fig. 3.1, source and drain contacts are situated at the front and back of the structure, with the same doping type as the channel. This makes the G4FET a majority carrier device, i.e. electron carrier device based on an electron channel in n-type material. Therefore, the current is flowing in the direction showed by the arrow I_D in Fig. 3.1. The effective channel length in the classical MOSFET transistor is referred in the G4FET as the effective channel width. That means that topics associated to the shrinkage of the effective channel length in the MOSFET should be considered when analyzing the effective channel width in the G4FET. The transistors used in this study are n-channel G4FETs, fabricated in a conventional 0.35 μm partially depleted (PD) SOI process. The channel of each transistor is 0.35 μm wide, 3.4 μm long, and 0.15 μm thick [39]. The top-gate oxide and the BOX thickness is 8 and 350 nm, respectively (dimensions are showed in Fig. 3.2). The channel doping is in the range of 10^{17} cm^{-3}. In order to increase the drive current several transistor are connected in parallel, 20 in Ref. [39]. Throughout this study, all the measurements have been obtained for the sample operating at low drain-source voltage $V_{DS} \simeq 50$ mV. With linear operation and a gradual channel approximation, the 3-D structure shown in Fig. 3.1 can be reduced to a 2-D one (Fig. 3.2) for simulation purposes. Once the structure is reduced, we solve self-consistently the 2-D Poisson and drift-diffusion equations. A mobility-field-dependent model is used [49]. At this point, the potential, electron and hole concentration are known for the whole structure. To obtain the noise characteristics, we have developed models to be included in the simulator in order to obtain the flicker

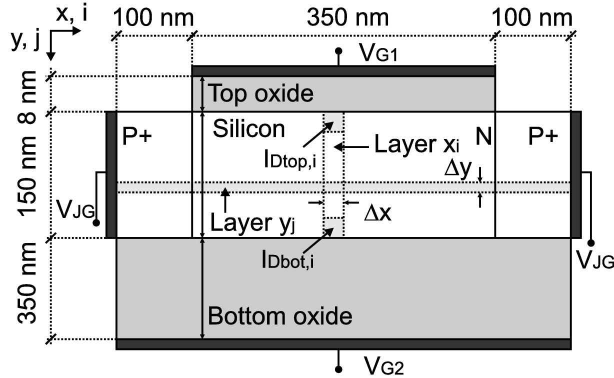

Figure 3.2: Cross-section of the simulated structure of the n-channel G4FET. It represents, not to scale, a surface perpendicular to the flow of the drain-current in the device.

noise and g-r noise. These models are explained in Sec. 3.3.

3.3 Noise study in the G4FET

The analysis of low-frequency fluctuations is essential to understand the performance of the device and thus to design an optimum transistor. In this case, the comparison of experimental data with numerical results requires more than the simple distribution of carrier density throughout the n-region obtained from a 2-D simulator. Adequate models that describe the noise behavior of the device are necessary. A model resulting from the combination of channel cross-section fluctuations with Hung's unified noise model is proposed [50]. This model takes into account g-r mechanisms in the depletion regions of the transistor and fluctuations of trapped charge inside the oxide, respectively [51]. The PSD of the drain-current, S_{I_D}, including both g-r and surface noise sources, ($S_{I_{Dgr}}$ and $S_{I_{Dsn}}$ respectively) is evaluated in different operating modes of the transistor, $S_{I_D} = S_{I_{Dgr}} + S_{I_{Dsn}}$. The numerical results reproduce the change from volume to surface noise shown in experimental data [39].

In the accumulation MOS mode, the channel is under the top oxide and electrons interact with traps in this oxide. In the JFET mode, the channel

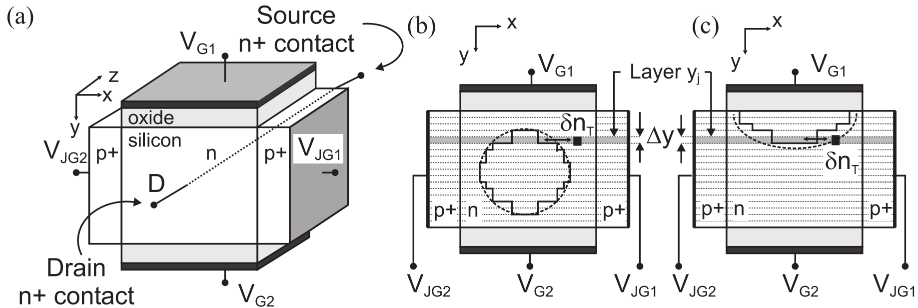

Figure 3.3: a) Structure of the G4FET. Cross-sections perpendicular to the current flow of the device. (b) Operating in the JFET mode. (c) Operating in the accumulation-MOS mode. The rectangular boxes inside the dashed curves in (b) and (c) show the limits of the depletion region. Electron concentration is assumed constant inside those boxes and null outside them. Dashed straight lines divide the device into horizontal layers.

is centered in the n-region and the top and bottom electrons of the channel are the ones responsible for the interaction with the traps in the oxides. A displacement of the channel towards the top or the bottom oxide determines which oxide plays the dominant role in the trapping and de-trapping processes. This displacement can be controlled by the values of the voltages applied to the top and bottom gates and by the distribution of the doping profile along the lateral p^+n junctions. A constricted channel located in the bottom half of the structure (as it will be determined from the analysis of the I-V curves in Sec. 3.5.1.1) may push electrons close to the bottom Si-SiO_2 interface. In a perfectly centered channel both oxides would contribute equally as noise sources. All these different situations show that none of the oxides can be discarded as a noise source. That means that differences between the two oxides should be incorporated in the noise model.

3.3.1 Generation-recombination noise model. Fluctuations of the channel cross-section.

In this subsection a model that calculates fluctuations of the channel cross-section is presented. It is related to the g-r noise produced by the fluctuation of the occupancy of deep traps in the depletion regions of the device. This model is based on the g-r noise produced in JFETs and it has satisfactorily been

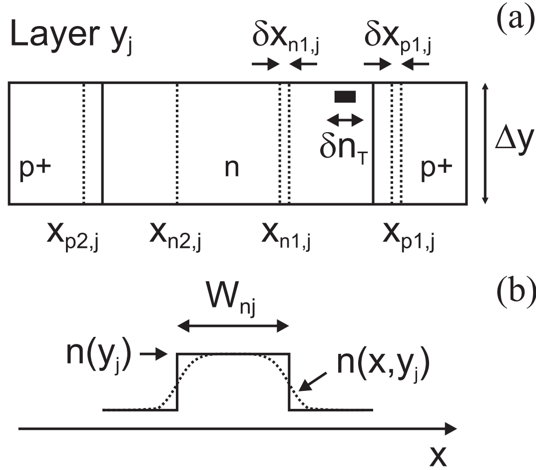

Figure 3.4: a) Single horizontal $j-$layer that the device has been divided into. (b) Distribution of electrons in layer j used for the evaluation of the drain-current: the concentration obtained by solving Poisson's equation ($n(x, y_j)$) and its approximation ($n(y_j)$ rectangular box model) are represented.

applied to these transistors [52, 53]. In first place, we focus on the conducting region of the device in any of the operating modes under study: a channel surrounded by depletion regions, and controlled mainly by the lateral junction-gate voltages V_{JG} (JFET mode, Fig. 3.3b) and a channel located near the top surface (accumulation-MOS mode, Fig. 3.3c).

In these figures, the structure is divided into N_y horizontal layers parallel to the insulators. Each layer has a width of Δy and is located at position y_j ($j = 1 \ldots N_y$). We have defined the variables x and y as parallel and normal, respectively, to the Si-SiO_2 interfaces. In any of these layers, a p^+-n-p^+ structure results (Fig. 3.4a). A conducting channel in the center of the n-region is delimited by the borders of the depletion regions of the right and left p^+-n junctions, named $x_{n1,j}$ and $x_{n2,j}$, respectively. The edges of the depletion region at the p-side of the right and left p^+-n junctions are named $x_{p1,j}$ and $x_{p2,j}$, respectively.

In the layer y_j, a fluctuation in the density of occupied traps $\delta n_T(x, y_j)$ is considered in the interval Δx around a point x within the depletion region of one of the junctions ($x_{p2,j} < x < x_{n2,j}$ or $x_{n1,j} < x < x_{p1,j}$). To maintain neutrality, a change of both edges of the depletion region must compensate this fluctuation.

A change of the edge of the n-depletion region $\delta x_{ni,j}(y_j)$ of junction i ($i = 1, 2$) produces a fluctuation of the channel thickness, and thus a fluctuation of the conductance of the n-channel, $G(y_j)$. Therefore, the current fluctuation in the layer y_j, originated by a fluctuation of trapped charge in the depletion region of junction i, is given by

$$\delta I(y_j) = V_{DS}\delta G(y_j) = -V_{DS} q n(y_j)\mu_n \delta x_{ni,j} \Delta y/L \tag{3.1}$$

where $\delta x_{ni,j}$ is minus the channel thickness fluctuation, V_{DS} is the drain-source voltage, q is the electron charge, μ_n is the electron mobility, L is the channel length and $n(y_j)$ is the electron density in the y_j-layer. In general, $n(x, y_j)$ and $\mu_n(x, y_j)$ are functions of the variables (x, y) and of the voltages applied to the four gates. Nevertheless, our model assumes constant values for these two variables inside the limits of the conduction region in the layer y_j ($x_{n2,j} < x < x_{n1,j}$), and $n(x, y_j)$= 0 outside these limits [see Fig. 3.4b]. To make this square box model physically acceptable, we define $n(y_j)$≡ $n(x, y_j)_{max}$ (Fig. 3.4b), and hence the dimension of the box $W_{nj} \equiv x_{n1,j} - x_{n2,j}$ is defined as:

$$W_{n,j} = \int_{n-region} \frac{n(x, y_j)}{n(y_j)} dx \tag{3.2}$$

and the effective mobility as:

$$\mu_n(y_j) = \int_{n-region} \frac{\mu_n(x, y_j) n(x, y_j)}{W_{n,j} n(y_j)} dx \tag{3.3}$$

In order to find these parameters, we solve, self-consistently, the 2-D Poisson and drift-diffusion equations for the device and the value of the $n(x, y_j)$ and $\mu_n(x, y_j)$ are taken in such a way that the current flowing through these boxes is the same as the one evaluated in the actual device. Figure 3.5 shows the excellent agreement between the current calculated in a G4FET operating in the accumulation-MOS mode using the exact distribution of $n(x, y_j)$ (solid line), and the one calculated under our box model (square markers) (The numerical results have been chosen in order to reproduce the experimental data obtained by Akarvardar *et al.* [39] (cross markers)).

In order to calculate the PSD, the noise contribution due to all the traps in the depletion region should be added, and this procedure must be repeated for

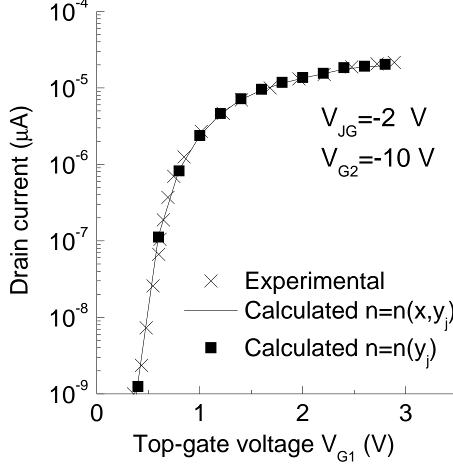

Figure 3.5: Drain current calculated in the G4FET in the accumulation-MOS mode as a function of the top-gate voltage (solid line). In symbols drain-current calculated using our model of rectangular boxes. The dashed line represents experimental data taken from [39].

both p^+-n junctions ($i = 1, 2$) in every layer in which the n-channel has been divided. Finally, the contribution of every layer has to be summed. We propose an expression for the PSD of the drain-current for the G4FET based on the expression obtained by Godoy *et al.* [53] developed for a 1-D JFET operating in linear regime:

$$\begin{aligned} S_I(\omega) = &\sum_{j=1}^{N_y} \sum_{i=1}^{2} \frac{4q^2 n^2(y_j) \mu_n^2 \Delta y V_{DS}^2}{\left(x_{ni,j} - x_{pi,j}\right)^2 N_D^2 L^3} \\ &\times \int_{x_{pi,j}}^{x_{ni,j}} N_T f_T \left(1 - f_T\right) \left(x - x_{pi,j}\right)^2 \frac{\tau}{1 + \left(\omega\tau\right)^2} dx \end{aligned} \tag{3.4}$$

where $N_D = N_D(x_{ni,j}, y_j)$ is the doping density evaluated at $(x_{ni,j}, y_j)$, $N_T = N_T(x, y_j)$ is the deep traps density, $f_T = f_T(x, y_j)$ its occupation function, and $\tau = \tau(x, y_j)$ the time constant given by

$$\tau(x, y_j) = \frac{1}{c_p \left(p(x, y_j) + p_1\right) + c_n \left(n(x, y_j) + n_1\right)} \tag{3.5}$$

where $n(x, y_j)$ and $p(x, y_j)$ are the electron and hole concentrations, respectively, c_n and c_p are the electron and hole thermal-capture coefficient rates, respectively, and n_1 and p_1 are the electron and hole densities when the Fermi level coincides with the deep one. The electron and hole thermal-capture coefficient rates are related with the respective capture-cross section by means of:

$$c_n = v_{th,n}\sigma_n$$
$$c_p = v_{th,p}\sigma_p \tag{3.6}$$

where v_{th} is the thermal velocity for the specific carrier. For the evaluation of the variables in expression (3.4), we solve self-consistently the 2-D Poisson and drift-diffusion equations in the device. They allow us to relate the value of these electrical variables with the applied voltages at the four gates. In the calculation of the PSD, number and mobility fluctuations in the channel should also be included, since g-r processes take place in both the depletion region and the conduction channel. These effects are demonstrated to affect mainly in semiconductors with defects with energy E_T above the Fermi level, (i.e. no crossover between E_T and E_F is found in the depletion region [54]). A lowering in temperature might also activate these mechanisms with a shift of the Fermi level to lower energies [54]. Since we are considering defects with energy level under the Fermi level (different common traps present in Czochralski-grown silicon (Cz-Si) are analyzed [55], [24]), and we are working at room temperature, these effects are neglected in our calculations.

3.3.2 $1/f$ noise. Surface fluctuations.

When channel electrons are captured or released from interface traps, the number of free carriers in the inversion layer changes. Moreover, as the oxide trap changes its electrical state, individual scatterers are turned ON and OFF and, therefore, channel mobility is also affected [56]. Thus, the current fluctuations are calculated as the combined effect of carrier number and mobility fluctuations. Hung and coworkers proposed a unified model that combines both types of fluctuations in a MOSFET in deep inversion [50]. We have applied this expression in the G4FET in any operating mode and any voltage range, above or under the threshold voltage. However, the electron distribution in the G4FET

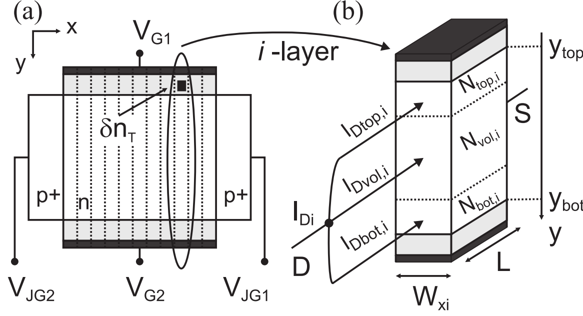

Figure 3.6: a) Division of the G4FET in vertical layers to cope with non-uniformities along $x-$axis. b)Detail of one of these layers in which the current is divided in the surface components, $I_{Dtop,i}$ and $I_{Dbot,i}$, and the volume component, $I_{Dvol,i}$.

is rather different than the corresponding one in a MOSFET, and therefore, some previous considerations about its operating modes are necessary in order to introduce the surface effects in our model.

To carry out this study, our model divides the structure in N_x vertical layers of thickness Δx (see layer x_i in Fig. 3.2 and in Fig. 3.6). This division enables us to consider the effect of non-uniformities along the x-axis. At the same time, our model distinguishes between electrons close to the top and bottom interfaces and electrons in the volume far from the interfaces. Thus, the drain current of layer x_i can be expressed as $I_{Di} = I_{Dtop,i} + I_{Dbulk,i} + I_{Dbot,i}$. The top- and bottom-surface components in the layer x_i ($I_{Dtop,i}$ and $I_{Dbot,i}$, respectively), can be affected by fluctuations in the occupancy of traps located in their respective closest oxides. Then, the flicker component $S_{I_{Dsn}}$ of the drain-current PSD in the G4FET can be evaluated as the sum of all the discrete contributions, $S_{I_{Dj,i}}$:

$$S_{I_{Dsn}} = \sum_{i=1}^{N_x} \sum_{j=top}^{bot} S_{I_{Dj,i}}. \tag{3.7}$$

Therefore, it is equivalent to consider a generic MOSFET of length L, width $W \equiv \Delta x$, and a drain current, $I_D \equiv I_{Di}$, flowing through its channel (Fig. 3.6a). The total drain current I_D can be expressed as:

$$I_D = \sum_{i=1}^{N_x} I_{Di} = \sum_{i=1}^{N_x} W_{xi} \mu_n q N_i E_z \tag{3.8}$$

where E_z is the channel field applied between source and drain contacts, W_{xi} is the width of the i-layer, and N_i is the carrier density per unit area calculated in the i-layer

$$N_i = \int_{y_{bot}}^{y_{top}} n_i(y)dy \tag{3.9}$$

where y_{top} and y_{bot} are the positions of the top and bottom interfaces, respectively (see Fig. 3.6b).

Depending on the bias of the four gates of the G4FET, surface and/or volume conduction modes are available. In the JFET mode, only a tail of electrons approaches the top and bottom interfaces at high V_{JG}. In the accumulation-MOS mode, conduction is mainly close to the interfaces. However, the electron concentration does not decay rapidly when moving inside the semiconductor volume, as it happens in conventional bulk-MOSFETs in inversion regime. Instead, the maximum electron density reached at the insulator interface is reduced in the y-direction to values, which in some cases, are close to the dopant concentration. It is clear that the volume conduction carriers exist in both modes, and in any case they cannot be included in the evaluation of surface noise. The contribution of all the mobile carriers in the sample would overestimate the noise in our device. To avoid this possible overcontribution, we divide the drain current of all the parallel channels in two components. one close to the surfaces ($I_{Dsurf,i}$), and another far from it ($I_{Dvol,i}$). In case both the top and bottom gates contribute to the current, the surface component can be divided in top and bottom contributions, $I_{Dtop,i}$ and $I_{Dbot,i}$ respectively. The drain current finally reads

$$I_{D_i} = I_{Dtop,i} + I_{Dbot,i} + I_{Dvol,i} = W_{xi}\mu_n q\left(N_{top,i} + N_{bot,i} + N_{vol,i}\right)E_z \tag{3.10}$$

where $N_{top,i}$, $N_{bot,i}$, and $N_{vol,i}$ are defined as

$$\begin{aligned} N_{top,i} &= \int_{y_{top}}^{y_{bot}} n_i(y)e^{\frac{-(y-y_{top})}{L_D}}dy, \\ N_{bot,i} &= \int_{y_{top}}^{y_{bot}} n_i(y)e^{\frac{-(y_{bot}-y)}{L_D}}dy, \\ N_{vol,i} &= N_i - N_{top,i} - N_{bot,i} \end{aligned} \tag{3.11}$$

we have chosen, as the boundary between the surface layers and the volume

layer, a distance from the interface equivalent to the Debye's length (L_D). It defines the effective thickness of the parallel plate capacitor, which capacitance per unit area equals that of the semiconductor contribution in a MOS capacitor in flat band ($C_D(FB) = \varepsilon_s/L_D$) [57], where ε_s is the permittivity of the semiconductor. Assuming that the volume charge does not contribute to the surface drain current noise, one can write the PSD of the total drain current as:

$$S_{I_D} = \sum_{i=1}^{N_x} S_{I_{D,i}} = \sum_{i=1}^{N_x} S_{I_{Dsurf,i}} = \sum_{i=1}^{N_x} \left(S_{I_{Dtop,i}} + S_{I_{Dbot,i}}\right) \tag{3.12}$$

For the surface components $I_{Dtop,i}$ and $I_{Dbot,i}$, fluctuations in the local drain current produced by fluctuations in the occupancy of the traps located in an infinitesimal volume $\Delta V = \Delta x \Delta z = W \Delta z$ in the oxide traps induces correlated fluctuations in the carrier number and mobility [50]:

$$\frac{\delta I_d}{I_d} = -(\frac{1}{\Delta N}\frac{\partial \Delta N}{\partial \Delta N_{ox}} \pm \frac{1}{\mu_{eff}}\frac{\partial \mu_{eff}}{\partial \Delta N_{ox}})\delta \Delta N_t. \tag{3.13}$$

with $\Delta N = N\Delta V$ and $\Delta N_{ox} = N_{ox}\Delta V$, where N is the number of channel carriers per unit area and N_{ox} is the number of occupied traps per unit area. In (3.13) the fluctuation in channel carriers related with the fluctuation in occupied traps ($\delta\Delta N/\delta\Delta N_{ox}$) is the so-called coupling coefficient R. In strong inversion, this term is practically equal to unity ($R = (\delta\Delta N/\delta\Delta N_{ox}) = (\delta N/\delta N_{ox})$ [50, 58]. However, in other regimes, this factor needs to be evaluated, as it can reach values as low as 10^{-10} in the depletion region [59]. Reimbold deduced an expression for this ratio from strong to weak inversion, relating all the charges involved in a MOS structure [58]:

$$R = \frac{-\beta Q_n}{C_D + C_{ox} + C_{it} - \beta Q_n}, \tag{3.14}$$

where $\beta = (kT/q)^{-1}$, Q_n is the channel charge, C_{ox} is the oxide capacitance, C_D the depletion capacitance and C_{it} the interface trap capacitance, all per unit area. The sign preceding the second term in (3.13) is determined by whether the active traps are repulsive (+ sign) or attractive (− sign). For the case of acceptor traps in an n-channel MOSFET, as is the case here, the mobility fluctuations term would be additive. By introducing the screened scattering coefficient σ_{sc} in the effective mobility to account for the Coulomb scattering of free carriers

at trapped charges near the Si-SiO_2 interface, (3.13) now becomes:

$$\frac{\delta I_d}{I_d} = -(\frac{R}{\Delta N} \pm \sigma_{sc}\mu_{eff})\frac{\delta N_{ox}}{\Delta V}. \tag{3.15}$$

The total drain current noise PSD can be calculated from the local drain current noise power (or PSD of the local current fluctuations):

$$\begin{aligned} S_{\Delta I_D}(z,f) &= \left[\frac{I_D}{\Delta N}(R \pm \sigma_{sc}\mu_{eff}N)\right]^2 S_{\Delta N_{ox}}(z,f) \\ &= \left[\frac{I_D}{\Delta z W}\left(\frac{R}{N} \pm \sigma_{sc}\mu_{eff}]\right)\right]^2 S_{\Delta N_{ox}}(z,f) \end{aligned} \tag{3.16}$$

where $S_{\Delta N_{ox}}$ is the PSD for mean-square fluctuations of the trapped charge carriers over the $W\Delta z$ area, and is expressed as

$$\begin{aligned} S_{\Delta N_{ox}}(z,f) = \int_{E_V}^{E_C}\int_0^W\int_0^{Tox} & 4N_{ox}(E,x,y,z)\Delta z f_T\,(1-f_T) \\ & \times\frac{\tau(E,x,y,z)}{1+\omega^2\tau^2(E,x,y,z)}dydxdE, \end{aligned} \tag{3.17}$$

where $N_{ox}(E,x,y,z)$ is the distribution of the traps over the space and energy, f_T is the trap occupancy function, $\tau(E,x,y,z)$ is the trapping time constant, E_{fn} the quasi-Fermi level, $\omega = 2\pi f$ the angular frequency, W is the device gate width, y is the electron tunneling distance from $y = 0$ (interface) to T_{ox} (the oxide thickness), and E_C and E_V are the bottom of the conduction band and top of the valence band for silicon.

Hung [50] proposed a simple solution for (3.17) taking into account two assumptions: i) the traps within the oxide have an uniform spatial distribution ($N_{ox}(E,x,y,z) \simeq N_{ox}(E)$), and ii) the probability of an electron penetrating into the oxide decreases exponentially with the distance from the interface. This means that the trapping time constant can be expressed as

$$\tau = \tau_0 \exp(\gamma y) \tag{3.18}$$

where τ_0 is the trapping time constant at the interface ($\tau_0 \approx 10^{-10}s$ for silicon case) and γ is the tunneling coefficient that can be expressed as $(4\pi/h)\sqrt{2m^*\phi}$, according to the Wentzel-Kramers-Brillouin (WKB) approxima-

tion ($\gamma \approx 10^8 cm^{-1}$). Here, m^* is the electron effective mass in the dielectric, h is the Planck's constant, and ϕ is the barrier height (band offset between Si and the dielectric). The factor $f_T(1-f_T)$ in (3.17) has the shape of a delta function around the quasi-Fermi level. Thus, only the traps around E_{fn} would contribute to the noise. In other words, $N_{ox}(E)$ can be approximated by $N_{ox}(E_{fn})$ and taken out of the integral. Finally, evaluating the integral in energy, depletion region, and depth in the oxide, expression (3.17) can be reduced to:

$$S_{\Delta N_{ox}}(z,f) = N_{ox}\left(E_{fn}\right)\frac{kTW\Delta z}{\gamma f} \tag{3.19}$$

Considering (3.16) and (3.19), one can obtain an expression for computing the PSD of drain current noise for a single vertical layer (see Fig. 3.6b):

$$S_{I_{D,i}}(f) = \frac{kT}{\gamma f}\frac{I_D^2}{W\Delta z}\left[\frac{R}{N(z)} + \sigma_{sc}\mu_n\right]^2 N_{ox}(E_{fn}) \tag{3.20}$$

Finally, to obtain the total PSD drain current noise of the whole G4FET, the contribution of each vertical layer and the two interfaces (top and bottom interface) have to be added. Therefore, the expression for computing the S_{I_D} can be expressed as:

$$S_{I_{D,i}}(f) = \sum_{i=1}^{N_x}\sum_{j=top}^{bot}\frac{kT}{\gamma f}\frac{I_{Dj,i}^2}{W_{xi}\Delta z_i}\left[\frac{R_{j,i}}{N_{j,i}(z)} + \sigma_{sc}\mu_n\right]^2 N_{ox}(E_{fn,j,i}) \tag{3.21}$$

where $N_{j,i}$ is the number of channel carriers per unit area computed using expressions in (3.11), and $R \leq 1$ is the coupling coefficient between channel carriers and oxide traps. In strong inversion or accumulation MOS regime of G4FET, $R \approx 1$ [50,58], but can reduce to $R \approx 10^{-10}$ in the depletion regime [59] by JFET operation of G4FET. Overall, R is a ratio of carrier "capacitance" (carrier charge over thermal voltage kT/q) to the total capacitance at oxide interface [58]. We determine the ratio R/N numerically.

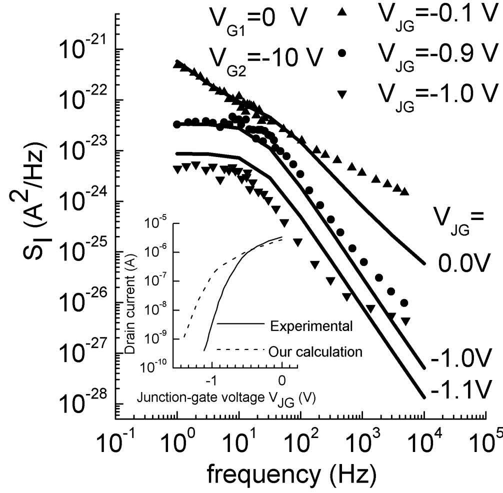

Figure 3.7: Numerical calculation of the power spectral density (PSD) of the drain-current noise for different junction-gate voltages V_{JG} (solid lines), and comparison with experimental results taken from [39] (symbols). Inset: drain-current in the JFET mode as a function of the junction-gate voltage. Comparison between the current obtained from our numerical calculations of $n(x, y_j)$ (dashed line) and experimental data taken from [39] (solid line).

3.4 Characterization of the G4FET by means of I-V and noise measurements

The models developed in Sec. 3.3 are tested in both accumulation-MOS mode and JFET mode considering both g-r (3.4) and surface (3.21) contributions to the noise. In order to compare our results with experimental measurements, the technological parameters of the devices under study are taken from an actual G4FET [39]. The parameters of the traps from which the noise originates, deep impurities in the volume of the semiconductor, oxide traps, and the doping profile in the n-region ($N_D \approx 10^{17} cm^{-1}$) are considered as fitting parameters to reproduce experimental measurements, since no data are provided in this respect.

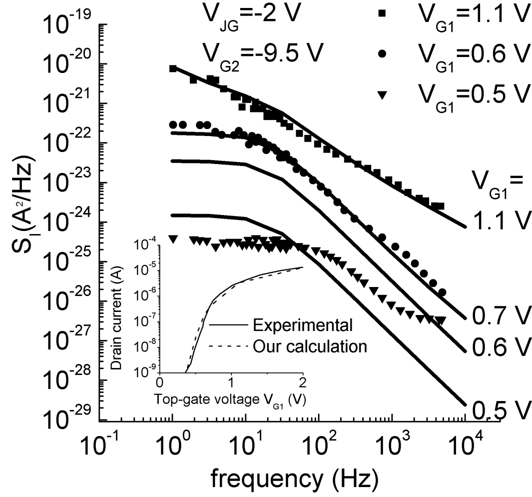

Figure 3.8: Numerical calculation of the power spectral density (PSD) of the drain-current noise for different top gate voltages V_{G1} (solid lines), and comparison with experimental results taken from [39] (symbols). Inset: drain-current in the accumulation-MOS mode as a function of the top gate voltage. Comparison between the current obtained from our numerical calculations of $n(x, y_j)$ (dashed line) and experimental data taken from [39] (solid line).

3.4.1 Comparison with experimental data

Figures 3.7 and 3.8 show the results of the simulated PSD of the drain-current when the transistor is operating in the JFET and accumulation-MOS mode, respectively (solid lines). To fit the experimental PSD (symbols), a deep trap located at $E_T = E_C - 0.45eV$ is considered in the calculations. A similar deep level trap, probably related to oxygen precipitates [60], was proposed by Ang [55] when analyzing g-r noise in silicon implanted by oxygen (SIMOX) n-MOSFETs. The capture cross-sections for electrons σ_n and holes σ_p are chosen in order to reproduce the experimental corner-frequency f_0 of the Lorentzian spectra. Table 3.1 summarizes the trap parameters used in the simulation to fit the g-r and $1/f$ noise. The maximum contribution of g-r noise is located at the point where the Fermi level crosses the energy level of the trap and this occurs inside the depletion region.

In order to include screening effects, a scattering coefficient α depending

Table 3.1: Summary of the parameters used in the simulation to reproduce the g-r noise and $1/f$ noise

Generation-Recombination noise		
E_T	$E_c - 0.45$	eV
σ_n	3.68×10^{-18}	cm^2
σ_p	3.52×10^{-14}	cm^2
N_T	5×10^{13}	cm^{-3}
$1/f$ noise		
$N_{ox,0}^{top}$	4×10^{14}	cm^{-3}·eV^{-1}
$N_{ox,0}^{bot}$	2×10^{14}	cm^{-3}·eV^{-1}

on the surface electron density $N_{j,i}(z)$ ($\sigma_{sc} = \sigma_{sc,0} - \sigma_{sc,1}\dot{l}n\left(N_{j,i}(z)\right)$ [61]) was assumed in (3.21). These effects have no remarkable influence on the results as the gate voltage range where the $1/f$ noise is dominant is very small. An overall good agreement is observed in both figures, explaining the noise PSD behavior in the G4FET as a function of different gate voltages. In Fig. 3.7, our noise model reproduces the transition from pure g-r noise spectra (lowest curves) toward a $1/f$ noise spectrum (highest curve). The different curves in Fig. 3.7 are labeled with the junction–gate voltage values V_{JG}, and these values differ slightly from the experimental to our calculated curves. This slight difference can be justified in the inset of Fig. 3.7 where we compare the drain-current as a function of the gate voltage obtained with our simulator with experimental data [39]: for low drain-currents, the calculated gate voltages are lower than the experimental ones, and for high drain–currents, the calculated gate voltages are higher than the experimental ones. In the accumulation mode (see Fig. 3.8), the transition from the g-r noise spectra to the $1/f$ spectra obtained with our model also reproduces the experimental spectra. In this case, similar values of the noise PSD as well as of the drain-current values (inset in Fig. 3.8) are found between simulated and experimental curves in the whole range of applied voltages. Two facts seem to escape from the agreement between the noise experiments and our calculated noise PSD. One is found in the highest curve of Fig. 3.7 ($V_{JG} = 0V$); while the low-frequency region of this curve shows an excellent agreement, the high-frequency tail tends to be different. We are assuming a $1/f$ model, whereas the slope of the experimental curve at high frequencies varies as $1/f^{0.8}$.

A probable explanation to this divergence could be ascribed to the non-uniform distribution of traps along the oxide depth. The second fact is found at the high-frequency tail of the lowest curve in both Figs. 3.7 and 3.8, where the slope of the calculated curve does not reproduce the experimental one. This change of slopes at high frequencies is similar to that found in ([24], Fig. 3), where the g-r noise produced by one and two traps in the depletion region of a p-n junction was compared. The presence of a second trap in the semiconductor with a different time constant can be the origin of this change in the slope. As we will see later, it is proposed a more complex model to deal with these problems in the section of advanced modeling (Sec. 3.5).

3.4.2 Comparison between bulk and surface noise contribution

In order to compare the relative contributions of the bulk g-r noise (3.4) and the surface noise (3.21), we have firstly calculated the PSD for different gate voltages in both modes, assuming that only the volume g-r noise is present in the device (squares in Figs. 3.9 and 3.10). Then, these results are compared to those ones assuming that both the bulk and surface noise sources are simultaneously present (solid lines in Figs. 3.9 and 3.10). The aforementioned parameters of the device and traps are again used in this calculation.

In the JFET mode, the total noise (solid lines in Fig. 3.9) increases with the junction-gate voltage for $V_{JG} < -0.4V$ in the whole frequency range. From -0.4 to 0 V a different trend is seen depending on the frequency range. This behavior can be explained by analyzing the g-r component (squares). Below the turn-ON voltage ($V_{JG} = -0.4V$), the channel is being built and the concentration of electrons in the channel grows, thus increasing the value of the S_I in (3.4). Once in the on-state, when the electron concentration reaches its maximum value inside the channel ($n = N_D$), this trend is inverted since the value of S_I decreases ($V_{JG} > -0.4V$ in Fig. 3.9). That means that τ in (3.4) should also decrease; it should not be constant, as predicts the complete depletion approximation in the space charge layer ($n \approx p \approx 0$), it follows from (3.5) that

$$\tau = \frac{1}{c_n n_1 + c_p p_1} \tag{3.22}$$

This assumption would lead to the conclusion that τ, and hence, f_0 in the

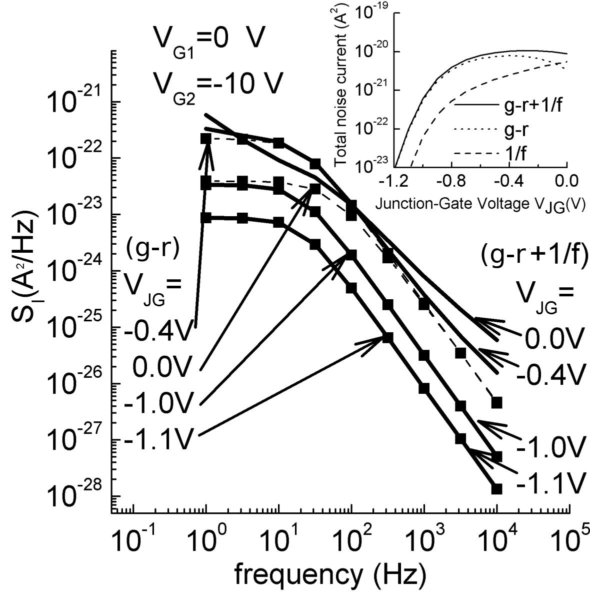

Figure 3.9: Numerical calculation of the PSD of the drain-current noise for different junction-gate voltages V_{JG} (JFET mode). Comparison between the contributions coming from the bulk g-r noise (squares) and the global noise (solid lines). Inset: total noise current as a function of the junction-gate voltage in the JFET mode. The dashed line represents the $1/f$ component, the dotted line corresponds to the g-r noise, and the solid line is the sum of both terms ($V_{G2} = -10V$ and $V_{G1} = 0V$).

Lorentzian g-r spectra, are independent of the gate voltage. Such a conclusion was previously formulated in MOSFETs [62]. However, this is not our case since the g-r contribution at $V_{JG} = 0V$ shows a higher corner-frequency than in the rest of the curves. Similar results are obtained in Sec. 3.5.3 for a fully depleted (FD) SOI MOSFET. In order to compare the g-r and $1/f$ contributions, we have also evaluated the total noise current in a given frequency band $\overline{i^2{}_T}$, defined as [63]:

$$\overline{i_T^2} = \int_{f_{min}}^{f_{max}} S_I(f)df \tag{3.23}$$

This magnitude has been depicted as a function of V_{JG}(inset in Fig. 3.9). We see how, at low voltages, the main contribution stems from the g-r noise (dotted line); however, when V_{JG} increases there is a maximum in the g-r noise, followed by a decrease. On the other hand, the $1/f$ component always increases

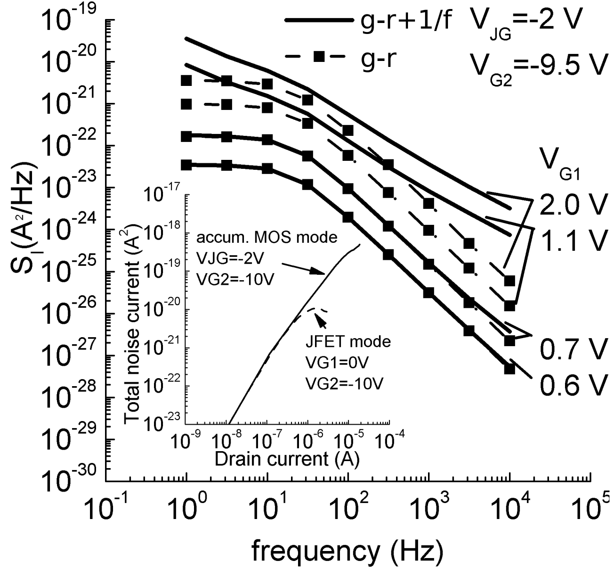

Figure 3.10: Numerical calculation of the PSD of the drain-current noise for different junction-gate voltages V_{JG} (JFET mode). Comparison between the contributions coming from the bulk g-r noise (squares) and the global noise (solid lines). Inset: total noise current as a function of the junction-gate voltage in the JFET mode. The dashed line represents the $1/f$ component, the dotted line corresponds to the g-r noise, and the solid line is the sum of both terms ($V_{G2} = -10V$ and $V_{G1} = 0V$).

(dashed line). There is a crossover point around $-0.1V$ where the $1/f$ term becomes dominant. The curve of the total noise (solid line) increases at low values of V_{JG} and tends to saturate at higher values. This curve reproduces the behavior of samples measured in similar conditions [39]. A study similar to this one, presented for the JFET mode, is carried out for the accumulation-MOS mode, where the parameters of the traps in the volume of the semiconductor and in the oxide are the same as in the previous case. In Fig. 3.10, we see how the g-r noise component (squares) and the total noise (solid lines) always increase when the top gate voltage increases. The main difference with the JFET mode is that, in this case, the total noise current does not saturate but monotonically increases. The inset in Fig. 3.10 shows this fact, where the total noise current evaluated in both modes is represented. The values of the gate voltages V_{JG} and V_{G1} are adjusted in the JFET and accumulation-MOS modes,

respectively, to obtain the same drain-current. At high currents, the total noise current in the accumulation-MOS mode is higher than in the JFET mode. This is justified by the higher number of carriers near the interface, which interact with oxide traps in the accumulation-MOS mode. A similar behavior can be found in experimental data (see [39], Fig. 5).

3.4.3 Effect of volume-trap parameters

Another goal of this study is to understand the different behavior of the noise in accumulation-MOS and JFET modes. The total noise current in the accumulation-MOS mode increases with current, whereas it reaches a saturated value in the JFET mode. It is clear from Figs. 3.9 and 3.10, that the reason of this different trend lies in the g-r noise component. To explain this different behavior, different kinds of trap have been considered, and their effects on the g-r noise are analyzed in this subsection. A representation of different electrical magnitudes such as carrier concentrations, time constant and occupation factor of the center origin of the noise is useful to give insight to experimental and numerical results. Three cases with the same center, located at $E_C - 0.45eV$ and concentration $N_T = 10^{-15}cm^{-3}$, are studied, according to the values of σ_n and σ_p:

- A recombination center with $\sigma_n = 3.68 \times 10^{-18}cm^2$ and $\sigma_p = 3.52 \times 10^{-14}cm^2$ ($c_n \times n_1 + c_p \times p_1 \approx 2c_n \times n_1$); this corresponds to the case studied in the previous subsection.
- An electron trap with $\sigma_n = 7.38 \times 10^{-18}cm^2$ and $\sigma_p = 5.31 \times 10^{-22}cm^2$ ($c_n \times n_1 \gg c_p \times p_1$).
- A hole trap $\sigma_n = 7.38 \times 10^{-23}cm^2$ and $\sigma_p = 7.06 \times 10^{-14}cm^2$ ($c_p \times p_1 \gg c_n \times n_1$).

These three cases are chosen to obtain the same value for the maximum time constant in the device, and thus, the same corner-frequency in the S_I ($1/\tau = 2\pi f_0$).

In Fig. 3.11, the total noise current is represented as a function of the drain-current for each of the aforementioned three cases. In the accumulation-MOS mode (solid lines), the three curves increase with the drain-current. In the JFET mode (dashed lines), the total noise current increases with the drain-current for both the electron- and the hole-trap cases. They follow a similar trend to

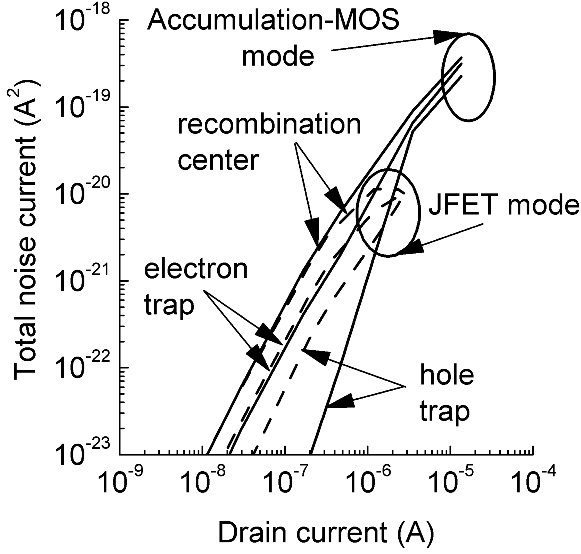

Figure 3.11: Total noise current as a function of the drain-current in the accumulation-MOS mode, dotted lines ($V_{JG} = -2V$, $V_{G2} = -9.5V$) and in the JFET mode, solid lines ($V_{G2} = -9.5V$ and $V_{G1} = 0V$) for three cases: (a) recombination center, (b) electron trap, and (c) hole trap.

that in the accumulation-MOS mode. Only the recombination center, in the JFET mode, shows a different behavior from the rest: the total noise current tends to saturate at high currents. This is justified, as mentioned earlier, by the decreasing component of the g-r noise in this mode (inset of Fig. 3.9).

In order to find a physical explanation for this trend, we represent the concentration of electrons and holes along a horizontal j-layer located at 80 nm from the top Si-SiO_2 interface [shaded region corresponding to the horizontal layer in Fig. 3.2] when the transistor operates in the JFET mode with V_{JG} in the range $-1.4V \leq V_{JG} \leq 0V$ [see Fig. 3.12(a)]. The higher the voltage, the deeper the minority carriers penetrate into the depletion region. The concentration of electrons and holes are independent of the capture cross-section values of the center origin of the volume g-r noise. However, this is not the case for the time constant τ, which is highly dependent on the values of σ_n and σ_p [see (3.5)]. In Fig. 3.12(b), the time constant τ is calculated for the case of a recombination

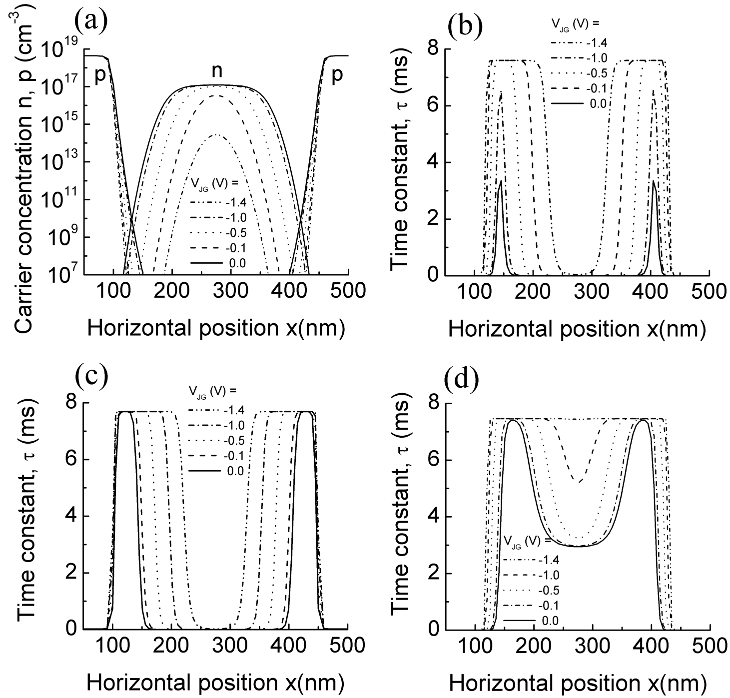

Figure 3.12: (a) Representation of the concentration of electrons and holes as a function of the lateral position (at a horizontal line of the channel located at 80 nm from the top interface) for different junction-gate voltages. The distribution of electrons and holes clearly shows the position of the metallurgical junction located at 100 and 450 nm along the p^+-n-p^+ structure. Representation of the time constant along the same line in the channel for three cases: (b) recombination center, (c) electron trap, and (d) hole trap.

center along the same j-layer as Fig. 3.12(a). At low voltages V_{JG}, we see a maximum of τ that covers almost all the depletion region, which corresponds to the complete depletion approximation where (3.22) is fulfilled. For high values of V_{JG}, a tail of holes penetrating from the p-region, even under reverse-biased voltages, and a simultaneous injection of electrons coming from the n-region refute the assumption of complete depletion. Hence, the approximation (3.22) is no longer valid and the evaluation of τ must take into account both majority and minority carriers [see (3.5)]. The maximum of the time constant decreases

accordingly for these higher voltages producing, as a consequence, an increase in the corner frequency and a reduction in the plateau value of S_I. This fact justifies the change of the corner-frequency and the plateau value for the g-r noise spectra shown in Fig. 3.9 when $V_{JG} > -0.4V$.

The same phenomenon might be expected to occur for the electron or hole traps, as the carrier distribution shown in Fig. 3.12(a) is also valid in both cases. However, we can find a region along this layer where the following conditions are fulfilled simultaneously: $c_n \times n_1 \gg c_p \times p$ and $c_n \times n_1 \gg c_n \times n$. This does not mean that complete depletion approximation is valid, but that we have found a region where the usual approximation $\tau \approx (c_n \times n_1)^{-1}$ is fulfilled [plateau regions in Fig. 3.12(c)]. The case of a hole trap is similar to that of the electron trap and $\tau \approx (c_p \times p_1)^{-1}$ [plateau regions in Fig. 3.12(d)]. These results highlight the importance of treating recombination centers appropriately. Recent results can be found in other contexts demonstrating that the typical assumptions associated with electron and hole traps are not valid with recombination centers [24, 26], and how the corner-frequency is also shifted as a function of the gate voltage [64]. A recombination center and a simultaneous injection of electrons and holes into the depletion region of the gate junctions explain the trend of the total noise current as a function of the drain-current. These results show first an increasing region, and then, a saturated one when the device operates in the JFET mode, while in the accumulation-MOS mode, such a trend does not appear since there is an increase at high currents. The reason for that increase in the accumulation mode lies in the low values for the junction-gate voltage used in this mode ($V_{JG} = -2V$). Thus, the tails of minority carriers penetrating the depletion regions are also low.

Experimental measurements evaluate the total noise current, making very difficult to distinguish the physical origin of all its different components. Therefore, the usefulness of our model is not in doubt since it incorporates different noise sources, evaluates the total noise current, and weights its different components. However, more complex model and simulation are needed to fully interpret all the physical aspects of these devices.

3.5 Advanced modeling

In the previous sections, we have acquired a view of the performance of the G4FET. However, some discrepancies between experimental and simulated results pointed out to the necessity of improving the models or to consider second order approaches. Sec. 3.5.1 focuses on these specific details to shed light on the processes and mechanisms present in this device. The subsequent subsections present the extension of these models to others devices.

Prior to the noise analysis, the importance of an accurate enough interpretation of experimental I-V curves in the device is of main concern. This implies the establishment of a realistic distribution for the electrons and holes in this device. This is not a trivial task, since it implies to control a significant number of variables. Moreover, this becomes more complicated if the set of I-V curves cover a wide range of bias voltages. However, a configuration that reproduces admissibly several curves is rather preferred than one which reproduces perfectly only one curve. In that sense, Sec. 3.5.1.1 aims for an overall fitting of experimental I-V curves which implies to consider non-uniform doping profiles. In this process, we see that traps involved in the noise response can also modify the I-V response of the device, Sec. 3.5.1.2.

The flicker noise model presented in Sec. 3.3.2 allows us to reproduce partially the experimental measurements. The discrepancy found between experimental and simulated results are due to simplification and approximation considered in the model. In Sec. 3.5.1.3, the modifications to the $1/f$ noise required to reproduce the changes in the slope of the spectrum due to non-uniformities of the oxide-traps with the depth are shown.

Finally, to close the study of the G4FET, Sec. 3.5.1.4 presents an optimization study where the main goal is to improve the G4FET performance in terms of transconductance-gain, subthreshold-swing parameters and LFN.

The noise models and characterization techniques for a G4FET presented in the previous sections can also be used in other structures. The characterization technique for traps within the oxides presented in Sec. 3.5.1.3 for the G4FET is applied to transistors with high-κ dielectrics. In Sec. 3.5.2 considerations needed to adapt this technique to high-κ gate oxide stacks are described.

The last point in the advanced modeling sections, Sec. 3.5.3, is devoted

to the simulation of g-r noise in FD SOI MOSFETs. The model to compute this noise is presented and a comparison between simulations and experimental measurements is carried out in order to characterize the traps present in these devices. The characterization of traps in these structures is essential in order to shed light on problems associated to retention time and noise in 1T-DRAM memories that employ this structure.

3.5.1 G4FET: second order approaches

3.5.1.1 Model for the effective channel width

As we have seen above, the conducting channel of the G4FET is sandwiched between two MOS gates, 3.1. At the same time, the channel has two lateral p^+n junctions, resembling a JFET structure. The metallurgical junctions are usually depicted as vertical lines under the top gate mask [41, 51]. However, an uniform penetration of the p^+ region into the n-channel along the y-axis is difficult to achieve with actual sequences of implantations and diffusions of impurities during the fabrication of the transistor's conducting channel. Thus, the metallurgical junction can penetrate under the top gate mask and present non-uniformities from the top to the bottom Si-SiO_2 interfaces. Treating with a real dopant distribution can be a complex task, as many technological parameters are involved. We propose to model a real profile with simpler ones, as shown in Fig. 3.13a. The dotted lines in Fig. 3.13a show the real profile of the metallurgical junctions of the lateral gates for an actual G4FET. This profile can be approximated by a polygonal profile as depicted in the same figure. A trapezium, displaced a distance t from the SiO_2 mask, with height a, and minor base $h2$ (this base separated from the top gate a distance $h1$), can model the actual curved shape of the metallurgical junction, as seen in Fig. 3.13a.

Figure 3.13b shows the typical uniform profile used in the simulations which corresponds with a trapezium with $a = t = h1 = 0$ and $h2 = h_{channel}$. Particular cases of this trapezium can be a rectangle Fig. 3.13c ($h1 = 0$, $h2 = 0$, the profiles are uniform but penetrating under the SiO_2 a distance a); or a triangle Fig. 3.13d ($h2 = 0$, $a = cte$, and varying $h1$). The objective of using a set of parameters to model the metallurgical junction along the y-axis of the structure is twofold. In the first place, we propose a method to extract the dopant distribution from DC or LFN measurements. In the second place we can establish a procedure to

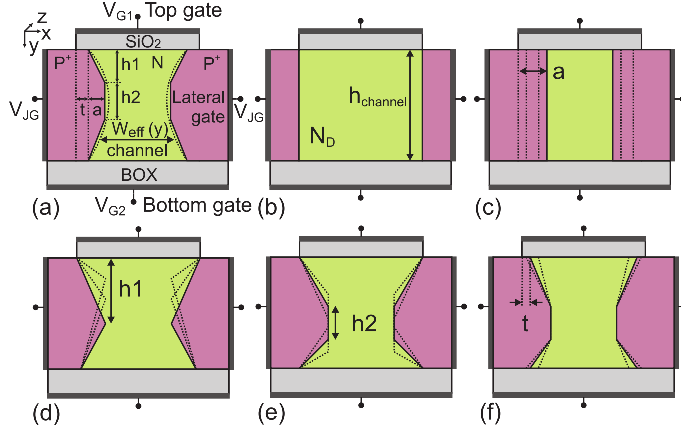

Figure 3.13: G4FETs employed in this work showing a non-uniform effective channel width along the y-axis: (a) Representation of all the parameter to model non-uniform effective channel, (b) G4FET with uniform effective channel width aligned with the oxide mask, (c) uniformly-displaced or rectangle-shaped metallurgical junction, (d) triangle-shaped metallurgical junction, (e) trapezium-shaped metallurgical junction, (f) displaced trapezium-shaped metallurgical junction.

determine the position of the channel that achieves the best performance of the transistor in terms of DC and noise characteristics, thus gaining control of the transistor by the fabrication process (Sec. 3.5.1.4).

The procedure to extract doping profiles of the conducting channel from experimental I-V curves and LFN is given in this subsection. It consists of generating a sequence of different dopant profiles defined by the geometrical parameters t, a, $h1$, and $h2$ (see Fig. 3.13a), and the dopant concentration in the channel N_D and in the lateral gates N_A. The dopant profile generated this way is introduced in a 2-D simulator. The simulation results are subsequently compared to the experimental data, either I-V curves or LFN S_I. The sequence of variation of the parameters defining the metallurgical junction are the following.

- The initial profile in the characterization procedure is the simplest one, a profile with a uniform metallurgical junction that coincides with the border of the top oxide, Fig. 3.13b ($t = a = h1 = 0$ and $h2 = h_{channel}$, where $h_{channel}$ is the channel height). The value of the concentration in the channel N_D is varied in first place, maintaining the values of the rest of the parameters. I-V and/or S_I curves are calculated and compared to

the experimental ones until a best fitting is obtained for a value of the parameter $N_D = N_{D0}$.

- The second step considers uniform metallurgical junctions but displaced under the SiO_2 edges, varying the parameter a, while maintaining the values $N_D = N_{D0}$, $h1 = 0$ and $h2 = h_{channel}$, Fig. 3.13c. Different profiles are generated by varying the sum $d \equiv t + a$. Numerical results are again obtained for these dopant profiles and compared with the experiments until a new best fitting is obtained, giving $d = t + a = d_0$.
- Once the maximum penetration under the top oxide is determined, the next step provides a way to locate this maximum penetration along the y-axis. To do this, the following parameters are maintained constant ($N_D = N_{D0}$, $a = d = d_0$, $(t = 0)$, and $h2 = 0$) and $h1$ is varied from 0 to $h_{channel}$. This configuration corresponds to triangles with the same height $a = d_0$, Fig. 3.13d. The best fitting of the numerical results with the experimental data provides a value for the parameter $h1 = h1_0$.
- In the following step, $h2$ is varied while considering $N_D = N_{D0}$, $a = d = d_0$, $(t = 0)$, and $h1 = h1_0 - h2/2)$, Fig. 3.13e. The best fitting in this step provides a value for $h2 = h2_0$.
- In the next step, t is varied while considering $N_D = N_{D0}$, $h2 = h2_0$, $h1 = h1_0 - h2_0/2$, and $a = d_0 - t$, Fig. 3.13f.
- Finally, when all the geometrical parameters are obtained, N_D is modified.
- The sequence is repeated until a good agreement between measured and simulated results is obtained.

The decisions are manually guided, since uncertainty in experimental data and instabilities in the simulation results have been encountered. In order to determine the best fittings of the experimental data with our simulations we calculate the "variance-accounting-for" (VAF) correlation coefficient [65]. This correlation coefficient is calculated from Cauchy-Schwarz's inequality via the expression

$$C = \frac{\sum_{i=1}^{n} (m_i s_i)^2}{\sum_{i=1}^{n} {m_i}^2 \sum_{i=1}^{n} {s_i}^2} \tag{3.24}$$

where m_i is the measured data (drain-current or drain current noise spectral

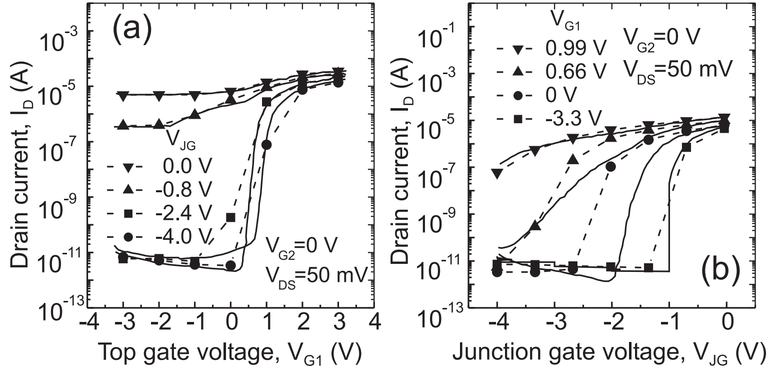

Figure 3.14: Current voltage curves showing the best fitting of experimental data (solid lines) measured in (a) the accumulation MOS mode and (b) the JFET mode with our calculations (dashed lines).

density), s_i is the simulated data, and n is the number of data. The root-mean-square (RMS) relative difference between the same data m_i and s_i is

$$RMS = \sqrt{\frac{1}{n}\sum_{i=1}^{n}\left(\frac{s_i m_i + \delta}{(m_i)^2 + \delta} - 1\right)^2} \tag{3.25}$$

where $\delta \approx 10^{-15}$ is a small positive number and the RMS formula is slightly modified to avoid division by zero. Ideally, if $m_i = s_i$ for every data point pair m_i, s_i, i=1,2,...,n, then C=1 and RMS=0. The coherence C cannot exceed unity, and both C and RMS are positive. Fitting the simulation to experiment, the geometry parameters for the junction metallurgical boundary and other parameters of G4FET are varied until maximum C and minimum RMS are obtained.

The doping profiles are modeled by uniform concentrations in the p^+-regions and n-regions. However, the metallurgical junctions of the lateral p^+-n junctions are assumed variable along the y-axis. A position-dependent metallurgical-junction of the lateral p^+-n junctions models the effect of non-uniform doping profiles in the drain, source and channel regions. In fact, a channel that is constricted in the middle, Fig. 3.13a, is necessary in order to obtain a good agreement with the experimental I-V curves, Fig. 3.14, in the conducting and subthreshold regimes.

When the G4FET is working in the JFET mode, the carrier concentration in the conducting channel approaches the doping concentration ($\sim 10^{17}cm^{-3}$). For these concentrations a value of $\mu_{bulk} \sim 700cm^2/Vs$ is employed in the simulator to reproduce the experimental currents. This value agrees with the reported values for electron mobility for Si with doping level of $N_D \sim 10^{17}cm^{-3}$ [66]. However, if this value for the electron mobility is used in the simulator when the G4FET is operating in accumulation mode, the high electron concentration produces an overestimation of the drive current through the device in the conduction regime. To solve this problem, we have implemented in the simulator a mobility model dependent of the transversal electric field $\mu_n(j,i) = R_\perp(j,i)\mu_{bulk}$, where the factor $R_\perp$ is given by [67]:

$$R_\perp(j,i) = \frac{1}{1 + \left(\frac{|E(j,i)|}{E_{univ}}\right)^\alpha} \tag{3.26}$$

The value of E_{univ} and α for electrons and holes are given in the following table:

Table 3.2: Values for the simulation of electron and hole mobilities

	α	$E_{univ}(V/cm)$
electrons	1.02	5.71×10^5
holes	0.95	2.57×10^5

With this model (3.26) the conduction regions of both experimental and simulated cases are in good agreement, either in JFET mode as in accumulation-MOS mode (Fig. 3.14).

In order to achieve the best fit in the subthreshold regions different doping profiles associated to the lateral p-n junctions have been considered. The doping profile has no effect on the leakage regime. In this regime, impurities in the bulk have been considered. This regime is treated in the following section.

3.5.1.2 I-V curves in the leakage regime

The leakage regime in Fig. 3.14 corresponds with a transistor in off-state. That means that the level in the drain-current is expected to be zero, but this is not

the case. A constant current around 10^{-11} A is observed in this regime and it is independent of the gates voltages. Although the channel should be fully depleted, a small amount of majority carriers is present in the semiconductor due to the equilibrium conditions imposed by the presence of recombination centers.

To reproduce the experimental data and to gain an insight into the mechanisms that produce these leakage currents, a recombination center is incorporated in the simulations, with the same energy level and concentration than the previous one considered in the noise study ($E_T = E_C - 0.45$ eV and $N_T = 5 \times 10^{14}$ cm^{-3}, respectively) but different capture cross-sections . Three different pairs of capture cross-sections are considered for the deep traps present in the device:

- i) A recombination center with $\sigma_n = 3.68 \times 10^{-15}$ cm^2 and $\sigma_p = 3.52 \times 10^{-11}$ cm^2.
- ii) A recombination center with $\sigma_n = 3.68 \times 10^{-18}$ cm^2 and $\sigma_p = 3.52 \times 10^{-14}$ cm^2.
- iii) No presence of traps.

Figure 3.15a shows different leakage levels in the I-V curve for a G4FET working in JFET mode. The minimum current in the subthreshold region is obtained for case *iii*. Otherwise the current level increases as the recombination center is becoming more efficient, worsening the ON/OFF-current ratio. The electron concentrations along a cutline at 80 nm distant from the top Si-SiO_2 interface and parallel to the top oxide have been depicted in Fig.3.15b, c, and d. When $V_{JG} = -4$ V the channel is strongly depleted and the maximum electron concentration depends significantly on the injected carriers from the lateral gates into the deep traps, Fig. 3.15b. However, once the conducting channel begins to form, Fig. 3.15d, these maximum electron concentrations and the drain-currents are the same for the three cases and the contribution of the injected carriers from the lateral gates to the drain-current could be neglected.

Choosing the first recombination center from the three previous cases, it allowed us to reproduce the leakage currents observed in the same devices in the subthreshold region [68], Fig. 3.14. Nevertheless, the introduction of a recombination center slightly reduces the calculated g-r noise (see Figs. 2a and 7a in [68]). From the noise perspective, this is a beneficial result, otherwise, detrimental in terms of leakage current. Basically, the recombination center makes

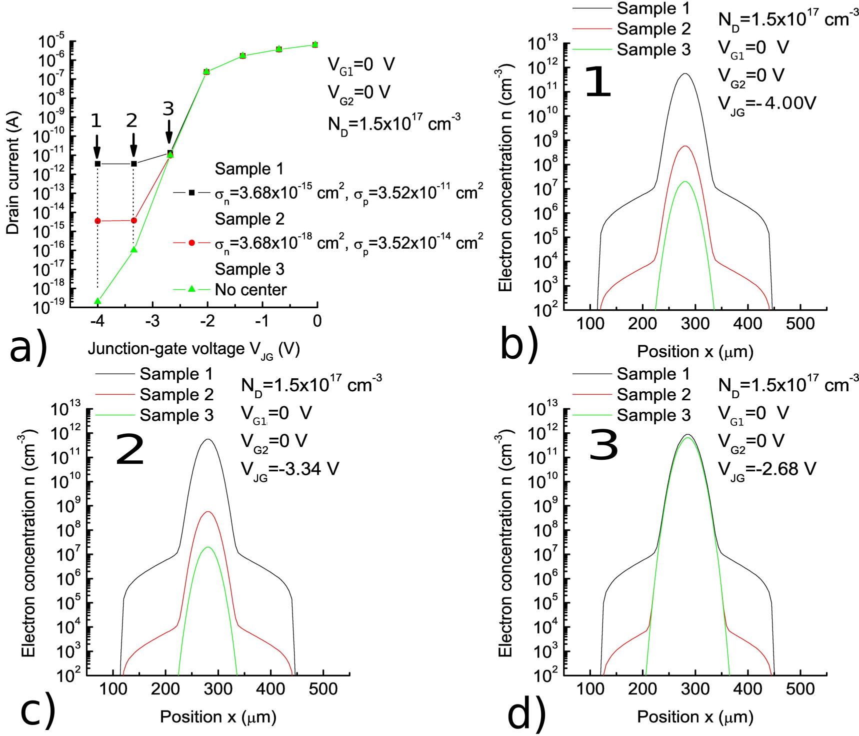

Figure 3.15: a) Current-voltage response of a G4FET working in JFET mode for three different deep-level traps present in the device. The labels 1, 2, and 3 indicate three different polarization points in the leakage regime. For these three points, the electron distributions along a cutline at 80 nm distant from the top Si-SiO_2 interface are depicted in b), c), and d), respectively.

the carrier concentration (in this case electrons) in the depletion regions to increase. Thus, the time constant $\tau = [c_p(p + p_1) + c_n(n + n_1)]^{-1}$ decreases from its maximum, $\tau_{max} = (c_p p_1 + c_n n_1)^{-1}$.

3.5.1.3 Low-frequency noise with variable spectrum slope

In Sec. 3.3, we have presented a model for the g-r noise in the channel semiconductor bulk and for $1/f$ noise due to oxide traps. The numerical simulations consider the corresponding noise components, reproducing the cross-over between bulk and surface noise in the experimental data from [39]. The exper-

imentally observed variations of the frequency exponent α of the flicker $1/f^{\alpha}$ noise in these regimes are now addressed. The levels and the exponent $\alpha < 0.7$ of the $1/f^{\alpha}$ noise are low in the experimental data [39] for the JFET regime at low bias of the MOS gates V_{G1} and V_{G2}, because the channel carriers (electrons in this case) are in the semiconductor bulk. The G4FET operates in the accumulation MOS mode by higher biasing the MOS gates [68], the position of the conduction channel approaches the oxides, the current flows at the surface and the noise and α increase, because the channel carriers and oxide traps interact. Therefore, we pursue a hypothesis for $1/f^{\alpha}$ noise in G4FET due to trapping in gate oxides. While the trap distributions in lateral axes (x and z in Fig. 3.1) of the gate oxides could be uniform, the non-uniform oxide trap density N_{ox} in energy and in the oxide depth (collinear with y-axis in Fig. 3.1) causes variation of the exponent α of the $1/f^{\alpha}$ noise in MOS transistors [43–47], due to the exponential distributions of N_{ox} as a function of the distance from the oxide interface and the difference from the silicon mid-gap energy (the latter causes U-shape energy distribution of N_{ox}). Thus, N_{ox} in a MOS-gate oxide is

$$\begin{aligned} N_{ox}(E, V_{ox}, y) &= N_{ox,0} \exp\left[|(E - E_i)\xi_1 + \frac{qV_{ox}\xi y}{T_{ox}}| + \eta y \right] \\ &\approx N_{ox}(E) \exp\left[\left(\frac{qV_{ox}}{T_{ox}}\xi + \eta \right) y \right] \end{aligned} \tag{3.27}$$

where N_0 is the trap density of the oxide at the semiconductor interface and at the silicon mid-gap energy E_i, $V_{ox} = V_G - V_{chan} \approx V_G - V_T$ is the potential difference between gate and channel, which is approximately equal to the gate overdrive voltage above the threshold voltage V_T for the linear operation of the G4FET, T_{ox} is the oxide thickness and ξ_1, ξ (ideally, $\xi_1 \approx \xi$) and η are gradient-like parameters for the exponential dependence of N_{ox} on energy E, potential bending $V_{ox}y/T_{ox}$ in the oxide and depth y in the oxide, respectively. The absolute value in (3.27) reflects the aforementioned U-shape, but at not very negative gate bias, $E - E_i + qV_{ox} > 0$, one can define $N_{ox}(E) = N_{ox,0}exp[(E_F - E_i)\xi_1]$ (which corresponds with the N_{ox} employed in Sec. 3.3.2). Defining $g(V_G) = (qV_{ox}\xi/T_{ox} + \eta)$ as a constant depth-gradient at particular bias V_G in the linear regime, equation (3.27) can be written as:

$$N_{ox}(E, V_{ox}, y) = N_{ox}(E) \exp(gy) \tag{3.28}$$

We will add letter "b" in the notations for the bottom gate V_{G2} and define $N_{ox,F} = N_{ox}(E = E_F)$ at the quasi-Fermi level. Considering that the surface channel current I_D is known, replacing N_{ox} by the previous equation (3.28) in expression (3.17), and using the result together with (3.16), the expression for the drain-current PSD noise can be now written as:

$$
\begin{aligned}
S_{I_D} &= \frac{4kTI_D{}^2}{WL^2}\int_0^L\left(\frac{R}{N}\pm\sigma_{sc}\mu_{eff}\right)^2 M(f)dz \\
&\approx \frac{4kTI_D{}^2}{WL}\left(\frac{R}{N}\pm\sigma_{sc}\mu_{eff}\right)^2 M(f), for V_D \ll (V_G - V_T) \qquad (3.29)
\end{aligned}
$$

For the experimental data in the linear regime of G4FET operation, the variations of the different quantities along the channel length (z-axis) are small, and the noise model simplifies to the second line in (3.29), where the noise spectral shape is due to the superposition integral M of the random trapping and release of carriers in the oxide, given by

$$
\begin{aligned}
M(f) &= \int_0^{T_{ox}} N_{ox}(E_F, V_{ox}, y)\frac{\tau(y)}{1+\omega^2\tau^2(y)}dy \\
&\approx N_{oxF}\int_0^{T_{ox}} e^{gy}\frac{\tau_0 e^{y/\lambda}}{1+\omega^2\left[\tau_0 e^{y/\lambda}\right]^2}dy \qquad (3.30)
\end{aligned}
$$

where the exponential dependence of the trapping time τ is given by (3.18), being $\gamma = 1/\lambda$. We assume that $\tau_0 \sim 0.1$ ns at the semiconductor-oxide interface and tunneling attenuation distance $\lambda \sim 0.1$ nm for SiO_2 on Si. A value of $\tau_0 \sim 10^{-10}$s is approximate and λ varies within a factor of two for different semiconductors and oxides and holes and electrons. Expression (3.18) gives a relationship between y and τ which is used to apply a change of variables in the second line of (3.30). Thus, one can rewrite (3.30) as

$$
M(f) \approx \frac{\lambda N_{oxF}}{\tau_{min}^{g\lambda}}\int_{\tau_{min}}^{\tau_{min}e^{T_{ox}/\lambda}}\frac{\tau^{g\lambda}}{1+\omega^2\tau^2}dy = \frac{\lambda N_{oxF}}{\tau_{min}^{g\lambda}}M_1(f) \qquad (3.31)
$$

Hereafter, the integral $M_1(f)$ is defined as

$$
M_1(f) = \int_{\tau_{min}}^{\tau_{min}e^{T_{ox}/\lambda}}\frac{\tau^{g\lambda}}{1+\omega^2\tau^2}dy \qquad (3.32)
$$

The lower limit of the integral in (3.31) can be obtained considering $y = 0$ in (3.18). Therefore, $\tau_{min} \sim \tau_0 < ns \ll \mu s < 1/(2\pi 100kHz)$. The upper limit has a dependence with the oxide thickness. In this specific case, an oxide with a thickness of $T_{ox} = 3$nm is used to form the devices. In that way the upper limit is approximately $1/(2\pi 1Hz) < s \ll \tau_{max} = \tau_{min} \times e^{T_{ox}/\lambda} \sim 0.1ns \times e^{30} \sim 10^3 s$. If one takes into account that for LFN the typical frequency range is (1Hz-100KHz), then the limits in the last integral can be extended from zero to infinite, obtaining an approximate formula, as

$$M(f) \approx \frac{\lambda N_{oxF}}{\tau_{min}^{g\lambda}} \int_0^{\infty} \frac{\tau^{g\lambda}}{1+\omega^2\tau^2} dy = \frac{\lambda N_{oxF}}{\tau_{min}^{g\lambda}} M_2(f) \tag{3.33}$$

Therefore, with the new limits the integral can be analytically solved.

$$M_2(f) = \frac{\pi/2}{(2\pi f)^{(1+g\lambda)} cos(g\lambda\pi/2)} \propto \frac{1}{f^{(1+g\lambda)}} = \frac{1}{f^{\alpha}} \tag{3.34}$$

This expression shows that the flicker noise in G4FET can deviate from $1/f$ noise, $\alpha \neq 1$, if the gradient $g(V_G) = (qV_{ox}\xi/Tox + \eta) \neq 0$, that is, the oxide trap density N_{ox} has either spatial gradient $\eta \neq 0$ or energy gradient $\xi \neq 0$, and there is a gate bias dependence of the flicker noise slope, $\alpha = \alpha(V_G)$, if $\xi \neq 0$. In fact, $\alpha \neq 1$ applies for any isolated-gate transistor, such as the regular MOSFET, once a gradient in the distribution of the gate oxide traps is present. Overall, our analyses suggest that the approximation by (3.34) is within 1-2dB error (more detail will be shown in the next section 3.5.2), while published experiments normally have 3dB uncertainty for LFN, and (3.34) offers straightforward modeling and characterization over the more complicated for handling (3.30). Thus, backward substitution of the expressions from (3.34) into (3.31) and the result in (3.29) yields the $1/f^{\alpha}$ model of isolated-gate (MOS) transistor, as

$$S_{I_D} = \frac{kT{I_D}^2 \lambda N_{oxF}}{f^{1+g\lambda} WL} \left(\frac{R}{N} \pm \sigma_{sc}\mu_{eff}\right)^2 \left[\frac{f_{max}^{g\lambda}}{cos(g\lambda\pi/2})\right] \tag{3.35}$$

We have so far discussed the $1/f$ noise in the drain current. In analogy with the amplifier noise model, the $1/f$ noise in the drain current can be referred to an equivalent input gate voltage source. The equivalent input gate voltage noise is calculated from the drain current noise as $S_{V_G} = S_{I_D}/{g_m}^2$. If the

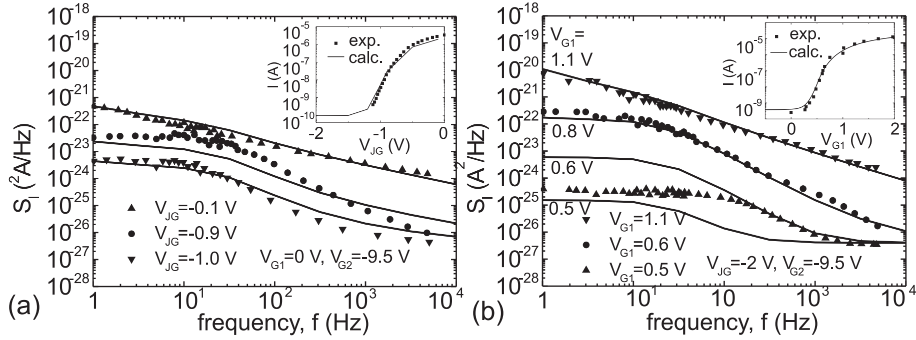

Figure 3.16: Numerical calculation of the drain-current noise spectral density for different gate voltages (solid lines) and comparison with experimental results taken from [39] (symbols). (a) JFET mode; numerical junction-gate voltages V_{JG} (from top to bottom): -0.1, -0.9, and -1.0 V. Inset: drain-current as a function of the junction-gate voltage (our numerical calculations in symbols and experimental data [39] in solid line. (b) Accumulation MOS mode; numerical top-gate voltages V_{G1} (from top to bottom): 1.1, 0.8, 0.6, 0.5 V. Inset: drain-current as a function of the top-gate voltage (our numerical calculations in symbols and experimental data [39] in solid line).

device is biased in the linear region $V_{DS} \leq V_{GS} - V_T$, we can assume that the inversion charge, qN, the mobility and the electric field are all constant along the channel. Thus, using simple MOSFET theory $I_D = (W/L)\mu_{eff} qNV_{DS}$, $qN = C_{ox}(V_{GS} - V_T)$, $g_m = I_D/(V_{GS} - V_T) = I_d C_{ox}/(qN)$ and (3.35):

$$S_{V_G} = \frac{q^2 \lambda N_{oxF}}{f^{1+g\lambda} WLC_{ox}^2} \left(R \pm \frac{\sigma_{sc}\mu_{eff} I_D C_{ox}}{qg_m} \right)^2 \left[\frac{f_{max}^{g\lambda}}{cos(g\lambda\pi/2})\right] \tag{3.36}$$

Finally, taking into account the model developed in this section and the one in Sec. 3.3.2, whereby a good fitting between experimental and simulated I-V curves was obtained, a much better overall fitting is obtained which is shown in Fig. 3.16. The deviation from the $1/f$ trend in the flicker noise is also reproduced considering this new model in both accumulation-MOS and JFET modes.

In order to reproduce the change in the slope in the $1/f$ noise, the following oxide parameters are introduced in (3.27): $\xi_1 = 3.1$ eV^{-1}, $\xi = 19.5$ eV^{-1}, $\eta = -2.4 \times 10^7$ cm^{-1}. Similar values for these parameters can be found in previous studies from noise measurements on MOS devices, [44, 69]. Different values for the trap density at midgap $N_{ox,0}$ are employed for the top and bottom oxides, $N_{ox,0}^{top} = 3.0 \times 10^{15}$ cm^{-3}eV^{-1} and $N_{ox,0}^{bot} = 1.5 \times 10^{18}$ cm^{-3}eV^{-1} respectively.

This agrees with the fact that in SOI technology, the buried oxide is expected to have worse quality than the front one, even in smart cut wafers where the back oxide is thermally grown, not by annealing of an oxygen-implanted layer [70]. The thicknesses of the top and bottom oxides were 8 and 350 nm, respectively. For the Lorentzian spectra we have used the following parameters: the capture cross-sections were chosen to reproduce the experimental corner-frequency, f_0, of the spectra, obtaining the best fit for a trap with $\sigma_n = 3.7 \times 10^{-18}$ cm^2 and $\sigma_p = 5.2 \times 10^{-14}$ cm^2. The level of the plateau region at low frequencies provides the trap density, $N_T = 5 \times 10^{14}$ cm^{-3}. The leakage regions are reproduced considering a recombination center located at midgap $E_T = E_C - 0.45$ eV and with capture cross-section $\sigma_n = 3.7 \times 10^{-15}$ cm^2 and $\sigma_p = 5.2 \times 10^{-11}$ cm^2, with a concentration of $N_T = 5 \times 10^{14}$ cm^{-3} as well.

3.5.1.4 DC and noise optimization of the G4FET

In this subsection is shown an optimization study of the DC and noise performance of the device. During the characterization procedure, we have seen that the device drain-current and its associated noise are very sensitive to small variations of the doping profile in the channel. Now, we show a study in which the profile has been varied in order to minimize the noise, and the subthreshold swing (SS) and to maximize the transconductance (g_m) of the device in different operation modes. Previous studies show that the G4FET transistor exhibits adjustable and improved subthreshold slope characteristics compared to MOSFET devices in a conventional partially depleted technology with no additional process adjustments. Excellent SS (below 100 mV/decade) can be achieved in G4FETs with either front-gate or junction gate control [71]. This is fulfilled with the help of the other passive gates that deplete the channel, and make the active gate to have a smaller charge to control. When this condition is not fulfilled, the SS degrades and the active gate is no longer able to deplete the film. This can be seen in Fig. 3.17, where the calculated g_m and SS seen from the lateral junction gates is represented as a function of the top and bottom gate voltage ($V_{G1} = V_{G2}$). A uniform effective width in the channel is employed in these calculations with a value of the doping concentration in the n-region $N_D = 1.6 \times 10^{17}$ cm^{-3}. The SS seen from the junction gates has a minimum when the top and bottom gates are in depletion ($V_{G1} < -2$ V). Even in this favorable range, another situation can lead to partial depletion, enlarging the

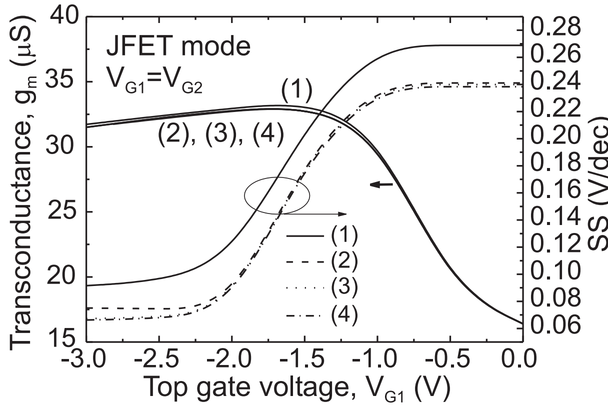

Figure 3.17: Calculated transconductance and subthreshold swing seen from the lateral junction gates (JFET mode) as the top gate voltage V_{G1} is swept, $V_{G2} = V_{G1}$. A recombination center with different values of the electron and hole capture cross-sections is considered in the calculations: (1) $\sigma_n = 3.7 \times 10^{-13}$ cm^2, $\sigma_p = 3.5 \times 10^{-9}$ cm^2; (2) $\sigma_n = 3.7 \times 10^{-15}$ cm^2, $\sigma_p = 3.5 \times 10^{-11}$ cm^2; (3) $\sigma_n = 3.7 \times 10^{-18}$ cm^2, $\sigma_p = 3.5 \times 10^{-14}$ cm^2; (4) no center.

population of electrons in the depletion region of the n-channel. This is associated to the existence of recombination centers in the semiconductor. We have calculated the g_m and the SS for a G4FET with a center with different electron and hole capture cross-sections. We can see from this figure that the more effective the recombination center is the greater the degradation of the SS. This effect is observed in the whole gate voltage range. A slight degradation in the g_m is also detected when the capture cross sections are varied. The center with the higher values of the electron and hole capture cross sections corresponds to the center characterized by the comparison of the experimental leakage current and our calculations in Fig. 3.17. A similar behavior is observed in the g_m and SS seen from the top gate while varying the lateral gate voltage.

The objective of this section is to determine a distribution of the effective channel width in the semiconductor that optimizes the behavior of the transistor in terms of the g_m, SS and LFN. The idea is to compensate the detrimental effect of the recombination centers by means of a proper doping distribution in the semiconductor. In order to do this, we consider the worst-case scenario, a transistor with a recombination center, with the same parameters as determined from experimental data. The metallurgical junctions shown in Fig. 3.13 are

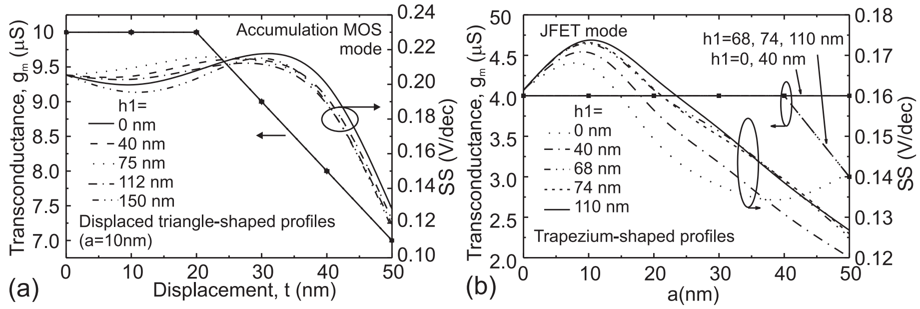

Figure 3.18: Calculated transconductance and subthreshold swing seen from (a) the top gate junction (V_{G2} = 0 V, V_{JG} = −1.5 V) and (b) the lateral junction gates (V_{G1} = 0 V, V_{G2} = −10 V) for different shapes of the lateral metallurgical junctions controlled by the parameters *a*, *t*, *h1*, *h2*. (a) Displaced triangle-shaped profiles ; (b) trapezium shaped profiles.

considered in the study (rectangle-, triangle-, displaced triangle-, trapezium-, and displaced trapezium-shaped metallurgical junctions). They are controlled by the parameters t, a, $h1$ and $h2$, previously defined. The electrical variables to optimize are calculated for different combinations of these four parameters. The sum $a + d$ ranges from 0 to 60 nm, and $h1$ and $h2$ from 0 nm to the thickness of the channel, 150 nm. The optimization procedure is made in both accumulation-MOS and JFET modes. Figure 3.18a shows the g_m and SS seen from the top gate of a G4FET with triangle-shaped metallurgical junctions in its lateral gates calculated as a function of the displacement t under the oxide mask, for different values of the parameter $h1$ with a triangle height $a = 10$ nm. The other gates voltages are $V_{G2} = 0$ V and $V_{JG} = -1.5$ V. For this bias condition, we see a simultaneous minimum for the SS and a maximum in the g_m for a displacement t around 10 nm and $h1 = 150$ nm. The value of SS at this point is 192 mV/dec. A significant reduction is obtained from the case with uniform effective channel width ($SS = 220$ mV/dec). A similar behavior is seen for any other pair of values for V_{G2} and V_{JG}, and the different metallurgical junctions profiles analyzed.

The optimum parameters for each set of profiles considered in this study can be seen in Fig. 3.18a. The transconductance shows no variation, $g_m = 10 \times 10^{-6}$ S, for all the profiles considered in the accumulation MOS mode in this figure. However, its representation next to the SS is important because we can see regions where SS decreases at the expense of reducing the g_m (see the range of

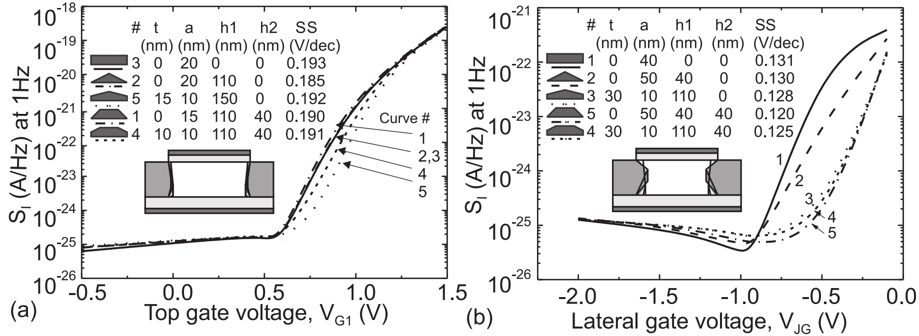

Figure 3.19: Drain-current noise spectral density evaluated at 1 Hz for different gate voltages in the (a) accumulation MOS mode and (b) JFET mode. It is evaluated for the profiles that optimize the transconductance and subthreshold swing, *SS*. The value of SS of each profile is given in the figure. The value of the transconductance is $g_m = 4 \times 10^{-6}$ (S) for all the profiles considered in the JFET mode and $g_m = 10 \times 10^{-6}$ (S) for all the profiles considered in the accumulation MOS mode.

high values of the displacement t in Fig. 3.18a). From this representation, we can see that all the shapes considered tend to converge to a profile where the effective channel width is maximum at the top and reduces slightly towards the bottom of the channel. The S_I evaluated for the profiles that optimize the g_m and SS is represented in Fig. 3.19a. It is evaluated at 1 Hz for different gate voltages in the accumulation MOS mode. In this mode, the profile that optimizes the SS does not coincide with the one that optimizes the noise. The reason is the similarity between these optimum shapes. Actually, the best situation in each set of profiles is represented and tend to converge, as seen in the figure.

Similar conclusions are obtained if the g_m and SS seen from the lateral gates of the G4FET are analyzed. Figure 3.18b shows g_m and SS of a G4FET with trapezium-shaped metallurgical junctions in its lateral gates. These variables are calculated as a function of the penetration under the oxide mask, for different values of the parameter $h1$ ($t = 0$ nm and $h2 = 40$ nm). The rest of the gate voltages are $V_{G1} = 0$ V and $V_{G2} = -10$ V. In this case, we see a simultaneous minimum for the SS swing and a maximum in the g_m for $a = 50$ nm and $h1 = 40$ nm. It has to be noticed that for $a > 50$ nm, g_m starts decreasing while SS keeps decreasing (not shown in the figure).The value of SS at this point is 120 mV/dec. Again, a significant reduction is obtained from the case with uniform effective channel width (SS= 160 mV/dec). A similar behavior is seen for any other pair

of values for V_{G1} and V_{G2}. This study is repeated for all the shapes of the doping profiles considered above.

The optimum parameters for each set of profiles can be seen in Fig. 3.19b. The transconductance, $g_m = 4 \times 10^{-6}$ S, for all the cases considered in the JFET mode in this figure. From these represented profiles, we can see that they tend to an optimal solution where the channel is constricted at around 50 nm from the top oxide and the effective channel width increases towards the top and bottom oxides. The S_I and the optimum profiles are indicated in Fig. 3.19b. It is evaluated at 1 Hz for different gate voltages in the JFET. In this mode, the profile that optimizes the SS coincides with the one that optimizes the noise and the variation between the spectra is more pronounced than in the previous mode. That makes the device working in the JFET mode more sensitive to doping profile variations than in the accumulation MOS mode. This can be seen by analyzing the voltage range where the doping profile really affects the noise ($-1 < V_{JG} < 0$ V in the JFET mode and $0.6 < V_{G1} < 1.3$ V). At low values of the gate voltage all the spectra converge, the channel is fully depleted and the profile has no influence on the noise. At high voltages, the $1/f$ noise overshadows the g-r noise and the physical mechanisms that control the noise move to the Si-SiO_2 interfaces. The region in between is clearly controlled by the doping profile, being more important its contribution in the JFET mode.

3.5.2 $1/f$ in stack gate oxides

Physical models for double stack high-κ dielectric MOSFETs have previously been developed [72–74]. They consider tunneling through a double step barrier and incorporate the noise originated in both the interfacial layer (IL) and the high-κ (HK) dielectrics. The formal difference between their model and the one described in this section lies in the spatial integral (3.30). There, their integral is split in two terms corresponding to both layers: IL and HK. Different non-uniform distributions of trap densities [72, 73] and different distributions of trapping-time constant are considered in both layers [72–74]. A new potential barrier model for the double-layer gate structure is proposed in order to accurately describe the trapping-time constant along the whole structure. The resulting trapping time constant is compared with the one obtained with the conventional square potential, showing that the model is especially accurate for tunneling distances above 2 nm (equivalent to frequency measurements below

1Hz) (Fig. 2 in [74]). On the other side, they demonstrate that in most practical cases the contribution of the IL to the total noise is negligible. The two main reasons are that either the measurement frequency is below 100 Hz or the trap concentration in the IL is far below the one in the HK. Under these considerations, we compare their exact expression (Eq. 13 in [72]),

$$\begin{aligned} S_{I_d}(f) &= \frac{4kTI_d^2}{WL^2}\int_0^L\left(\frac{1}{N(x)}+\sigma_{sc}\mu_{eff}\right) \\ &\times \left[\frac{N_{t0IL}\exp[\xi_{IL}(E_{fn}-E_i)]}{\gamma_{IL}\tau_{0IL}^{(\beta_{IL}V_{IL}+\eta_{IL})/\gamma_{IL}}(2\pi f)^{1+(\beta_{IL}V_{IL}+\eta_{IL})/\gamma_{IL}}}\right. \\ &\times \int_{2\pi f\tau_{0,IL}}^{2\pi f\tau_{0,IL}\exp(\gamma_{IL}T_{IL})}\frac{u_{IL}^{(\beta_{IL}V_{IL}+\eta_{IL})/\gamma_{IL}}}{1+u_{IL}^2}du_{IL} \\ &+ \frac{N_{t0HK}\exp[\xi_{HK}(E_{fn}-E_i)]}{\gamma_{HK}\tau_{0HK}^{(\beta_{HK}V_{HK}+\eta_{HK})/\gamma_{HK}}(2\pi f)^{1+(\beta_{HK}V_{HK}+\eta_{HK})/\gamma_{HK}}} \\ &\times \left.\int_{2\pi f\tau_{0,HK}}^{2\pi f\tau_{0,HK}\exp(\gamma_{HK}T_{HK})}\frac{u_{HK}^{(\beta_{HK}V_{HK}+\eta_{HK})/\gamma_{HK}}}{1+u_{HK}^2}du_{HK}\right]dx \end{aligned} \tag{3.37}$$

that requires the evaluation of an integral between two exact limits, with our analytical expression in (3.29), (3.32), and (3.34). Assuming $\tau_{min} \equiv \tau_{0HK}$ in these expressions, we compare integrals M_1 and M_2, appearing in (3.32) and (3.34), respectively. To do so, we consider a double-stack device with the following typical parameters [72, 73]:, $T_{HK} = 2.7$ nm, $T_{IL} = 1.0$ nm, $\gamma_{IL} = 10^8$ cm^{-1}, $\gamma_{HK} = 0.96 \times 10^8$ cm^{-1} ($m_{HK}{}^* = 0.8m_0$, $\phi_{HK} = 1.13$ eV) and traps decaying exponentially with the distance ($g = \eta_{HK} = -5.7 \times 10^5$ and $g = \eta_{IL} = -8.4 \times 10^6$ cm^{-1}). The integral M_1 and the analytical approximation M_2 are represented as a function of the frequency in Fig. 3.20. The comparison shows that M_2 (solid line) is a good approximation of M_1 (dashed line) for frequencies $f << 1/(2\pi\tau_{0HK}) = 72$ kHz. On the other side, one can see that the slope of the integral M_1 decreases just for frequencies above this limit. A quick analysis of experimental data showing a decrease in the slope of noise spectra could be attributed to a change in the distribution of traps in the dielectric. However, we see that this is only a mathematical artefact. In order to determine from experiments the value of g, and thus the distribution of traps in the dielectric, it is then advisable to analyze the low frequency region, just where M_1 equals M_2. This result can be extended to the most practical situations

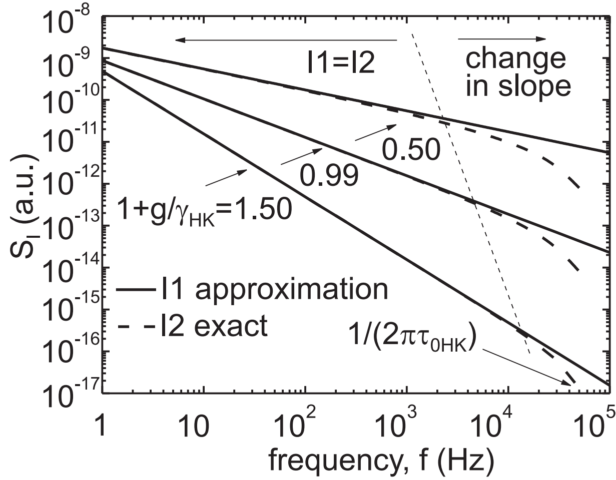

Figure 3.20: Theoretical calculation of the current power spectral density in a double-stack with traps decaying exponentially with the distance, $g = \eta_{HK} = -5.7 \times 10^5$ and $g = \eta_{IL} = -8.4 \times 10^6$ cm^{-1}. The solid lines correspond to the exact calculation (integral M_1) and the dashed lines to the approximation given by M_2

found in these devices. Thus, the expression M_2 offers practical advantages over M_1.

The noise model developed in the previous section has also been tested with experimental measurements taken in triple gate fin field effect transistors (FinFETs) processed on strained Si-on-insulator (sSOI) substrates, with HfO_2 or HfSiON stacks [47]. Noise of the type $1/f^\alpha$ ($\alpha < 1$ for low frequencies and $\alpha \approx 1$ at higher frequencies) was measured for these devices [47]. By using a simple tunneling model, authors interpreted this behavior in terms of a profile in the oxide trap density, N_{ox}, which decays with further distance from the Si-SiO_2 interface. The origin of this decay with further distance and its difference with trap profiles in planar transistors, revealed by different techniques, was also discussed by these authors. Our aim here is to confirm this trend by employing a model that implicitly considers a non-uniform trap profile: $N_{ox}(y) = N_{ox,0} \exp(\eta y)$. The decay or increase rate with distance is controlled by the additional parameter, η, see (3.27). The dependence with the gate voltage in (3.27), controlled by the parameter ξ, can be omitted if the experimental LFN shows no dependence with this variable, as is the case analyzed here. The experimental data showed that the noise is approximately constant with the gate overdrive and for the

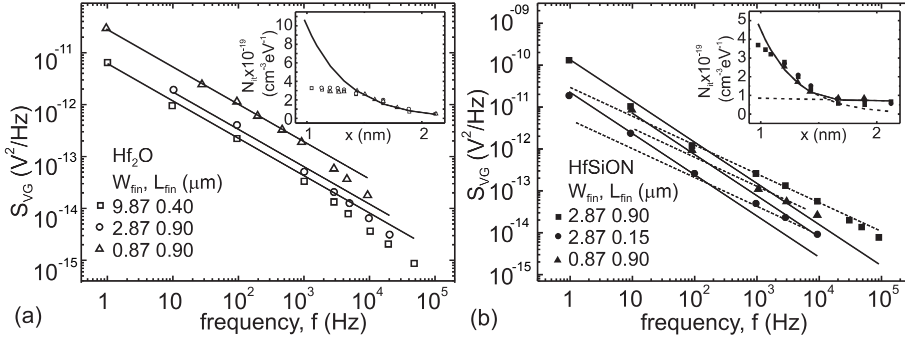

Figure 3.21: Comparison between our calculations (solid lines) and experimental data (symbols) [47] of the equivalent gate voltage noise for sSOI nfinFETs with (a) HfO_2/SiO_2 and (b) $HfSiON/SiO_2$ gate dielectric as a function of the frequency. The inset shows the oxide trap density profile introduced in (3.27) in order to reproduce the experiments (solid line) and the comparison with the results obtained with the unified noise model (symbols).

different range of geometries. In this sense, the parameter σ_{sc} can be considered well below its saturation value, and the term depending on I_d/g_m in (3.35) can also be neglected in the calculations.

Figure 3.21 shows the equivalent gate voltage noise for sSOI n-FinFETs with HfO_2/SiO_2 and $HfSiON/SiO_2$ gate dielectric as a function of the frequency for different values of the fin width, W_{fin}, and its length L_{fin}. For both gate stacks, the high-κ dielectrics are deposited on top of 1 nm interfacial SiO_2. Fig. 3.21a shows a good agreement at low frequencies between the experimental data (symbols) [47] and our calculations (solid lines) when considering an exponential oxide trap density profile modelled by $N_{ox0} = 10^{20}$ cm^{-3} eV^{-1} and $g = \eta = -2.8 \times 10^7$ cm^{-1}. At higher frequencies the slope of the experimental curve decreases as predicted in the analysis of Fig. 3.20. The experimental data in this region are reproduced by the exact integral M_1. Figure 3.21b shows a different trend in the slope of the PSD. At low frequencies the experimental data can also be reproduced with our calculations when considering an exponential oxide trap density profile modelled by $N_{ox0} = 8.5 \times 10^{18}$ cm^{-3} eV^{-1} and $g = \eta = -1.64 \times 10^6$ cm^{-1}. However, for frequencies above 100 Hz, the slope of the experimental curve increases, unlike the trend show in Fig. 3.21a or in the theoretical analysis in Fig. 3.20. That means that the trap density increases more rapidly towards the SiO_2/HfSiON interface. The region between 10^2 and 10^4 Hz is reproduced

with our calculations with a trap distribution modeled by $N_{ox0} = 4.5 \times 10^{19}$ cm^{-3} eV^{-1} and $g = \eta = -3.11 \times 10^7$ cm^{-1}. At higher frequencies the slope in the experimental data decreases as theoretically expected (Fig. 3.20). The trap density profile for both sets of data (inset in Fig. 3.21) is represented in the region associated to the measured frequency range, that lies in the high-κ dielectric region. The trap density in the HfO_2 dielectric can be reproduced by a single decreasing exponential. The trap density in the HfSiON dielectric can be modeled by two exponential distributions. Our results are compared with the ones obtained following the unified noise model [47], showing discrepancies, especially at positions close to the high-κ/SiO_2 interface. Our approximation to the multi stack unified model defined in [72, 73] shows with these examples a quicker and precise way to characterize traps in the dielectrics of double stack high-κ dielectric MOSFETs.

3.5.3 Generation-recombination model applied to FD SOI MOSFETs

In this section we present a g-r noise model similar to the one developed in Sec. 3.3.1 for a G4FET, but applied in this case to FD SOI double-gate transistors. We start from a model proposed by Yau and Sah [75] for the g-r noise in a MOSFET which is adapted for simulation purposes to this structure. The mean-square value for the drain current fluctuation in a MOSFET is related to the charge fluctuation δQ_n within the channel by means of [75]:

$$\overline{\delta I_D^2} = \int_{x=0}^{L} \int_{y=0}^{y_{max}} \left(\frac{\mu_n Z}{L}\right)^2 \overline{\delta Q_n^2} \Delta x \left(\frac{\Delta V}{\Delta x}\right)^2 dx \tag{3.38}$$

where L and Z are the length and width of the channel, respectively, μ_n is the electron mobility, y_{max} the maximum depth of the depletion region, V is the voltage drop in x, and the x-axis and y-axis are parallel and perpendicular to the oxide, respectively (Fig. 3.22). The electric field along the x direction is $F(x)= V/x$.

In turn, the charge induced in the channel δQ_n can be related to a trapped charge fluctuation δq_t in the volume $\Delta x \Delta y$ located at (x, y) [75]:

$$\delta Q_n = \left(\frac{C_N}{C_N + C_O + C_W}\right) \left(1 - \frac{y}{y_{max}}\right) \delta q_t \tag{3.39}$$

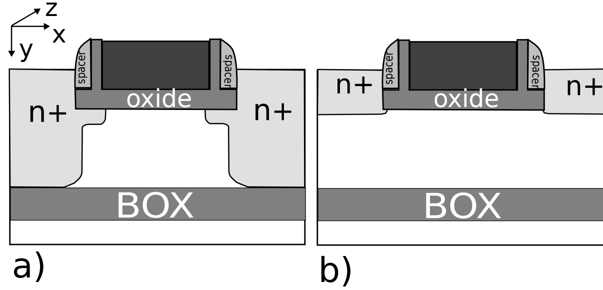

Figure 3.22: Sketch of a FD SOI transistor considering two different manufacturing processes for the source and drain regions: a) standard junction FD SOI nMOSFET which includes extension implantations, and b) extension-less FD SOI nMOSFET without extension implantations.

where C_N, C_O, and C_W are the corresponding capacitances for the channel, oxide and depletion region. The coupling factor $R{=}C_N/(C_N + C_O + C_W)$ is included in order to avoid the noise power divergence [75]. Introducing (3.39) in (3.38), and considering that the mean-square value of the charge fluctuation for a single time-constant g-r process is given by:

$$\overline{\delta q_t^2} = q^2 N_T f_t \left(1 - f_t\right) \frac{4\tau\Delta f_t}{1+\omega^2\tau^2} \frac{(\Delta y)^2}{\Delta x \Delta y Z} \tag{3.40}$$

one can obtain an expression for the $S_I(f)$:

$$\begin{aligned} S_{I_d}(f) &= \frac{\overline{\delta I_d^2}}{\Delta f} = \frac{4q^2 Z}{L^2} \int_{x=0}^{L} \left(\mu_n R F(x)\right)^2 \\ &\times \int_{y=0}^{y_{max}} N_T \left(1 - \frac{y}{y_{max}}\right)^2 \frac{f_t\left(1-f_t\right)\tau}{1+(2\pi f \tau)^2} dx dy \end{aligned} \tag{3.41}$$

where q is the electron charge, N_T is the trap density, f_t is the trap occupancy function, τ is the time-constant of the fluctuation, and f is the frequency. This expression is similar to the one developed for a G4FET, (3.4), but two main differences are found. In the G4FET the noise is computed considering a transversal cross-section of the current flow. Here, this is computed along the same direcction of the current. The second point is due to the FD character of the transistor. The calculated depletion region of FD double-gate devices, W, can be many times larger than the thickness of the Si film T_{Si}. In these cases,

the upper limit of the integral along y in (3.38) and (3.41) should be replaced by $y_{max}= T_{Si}$. Analytical models deduced from Yau and Sah such as those found in [76], [77] are based on the gradual-channel approximation. In these models, the integral along the variable x is transformed into an integral along the channel voltage $V(x)$ limited by the S/D voltages. Equation (3.41) maintains the dependence with the x variable in order to consider possible lateral non-uniformities in the structure. These non-uniformities may arise close to the S/D regions. This is especially important when different processes to manufacture the S/D regions are employed, such as the ones depicted in Fig. 3.22. The evaluation of (3.41) is done by a prior numerical determination of the electrical variables that appear in it. A fine mesh is defined in the FD double-gate device and the electrical variables are evaluated by a numerical solution of the Poisson and drift-diffusion equations using a commercial simulator. The evaluation of the effective electron mobility $\mu_{n,eff}$ and the coupling coefficient R require the estimation of the number of carriers involved in vertical layers of width Δx in which the structure is divided. The Debye's length L_D is used in order to estimate this number [51]. The $\mu_{n,eff}$ is weighted with the electron concentration. Once the $\mu_{n,eff}$, R, and the lateral electric-field F for each vertical slice are evaluated, the whole integral along the x-axis and y-axis can be computed. The local time-constant τ depends on the local free electron and hole concentrations, as can be seen in (3.5).

3.5.3.1 Evolution of the PSD with the gate voltage

A way to distinguish whether Lorentzian noise spectra are produced by interface traps or by a given trap level within the depletion region, is by analyzing the dependence with the front-gate voltage (V_{GS}) of the corner-frequency f_0 and the plateau value $S_I(0)$ of the drain-current or gate-voltage PSD. For a given trap within the depletion region of bulk and partially depleted (PD) SOI MOSFETs the time-constant, is independent of V_{GS}. Hence, the value of f_0 is also gate voltage independent and the plateau value shows significant differences from the case of interface related Lorentzians [76]. The reason is that free electrons and free holes in the middle part of the depletion layer are practically absent, and the complete depletion approximation ($n = p = 0$) can be used. This implies that (3.5) reduces to a constant value $\tau = (c_n n_1 + c_p p_1)^{-1}$. Unlike bulk and PD SOI MOSFETs, FD SOI transistors have such a thin semiconductor layer

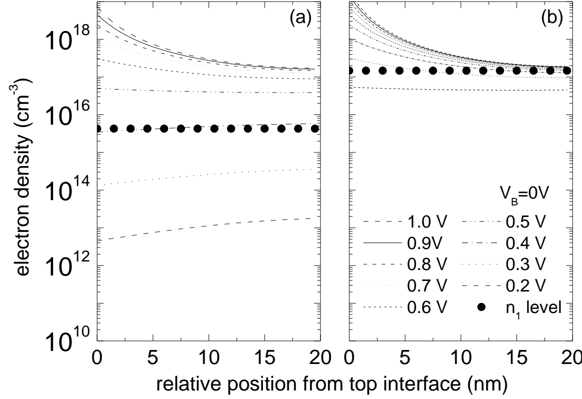

Figure 3.23: Electron density in a FD SOI MOSFET as a function of the depth for different gate voltages obtained for a vertical line at the middle of the channel, with a trap located (a) 0.32 eV and (b) 0.41 eV above midgap. The dotted line represents the electron density n_1 when the Fermi level coincides with the trap level.

that no neutral region is found. Moreover, the inversion layer can occupy the whole semiconductor film. In this regard, no depleted region is found in the device despite being called a fully-depleted device. Fig. 3.23 shows numerical calculations of the inverted charge carrier population (electrons) along a vertical line at the middle of a 20 nm thick channel of a FD SOI transistor. The doping of the semiconductor used in the simulation would produce a depletion layer depth in a bulk transistor five times higher than the thickness of the silicon layer ($W_{max} \approx 5 \times T_{Si}$). Fig. 3.23a shows a dotted line that points out the value of n_1 for a trap located at $E_{T1} - E_i$=0.32 eV above midgap E_i. Fig. 3.23b shows a dotted line corresponding to a more shallow level located at $E_{T1} - E_i$=0.41 eV.

The first observation in both curves is that electrons distribute almost uniformly along the Si-layer from front to back interfaces. Except deep in the subthreshold region, the concentration of electrons cannot be considered negligible in comparison with the value of n_1. The corresponding hole densities obtained in the simulations are always equal or lower than 10^{10} cm^{-3}. Therefore, the time-constant (3.5) can be reduced to τ=$(c_n(n + n_1))^{-1}$, and hence f_0 is expected to depend on the electron concentration: $f_0 \approx c_n(n + n_1)/(2\pi)$. At low

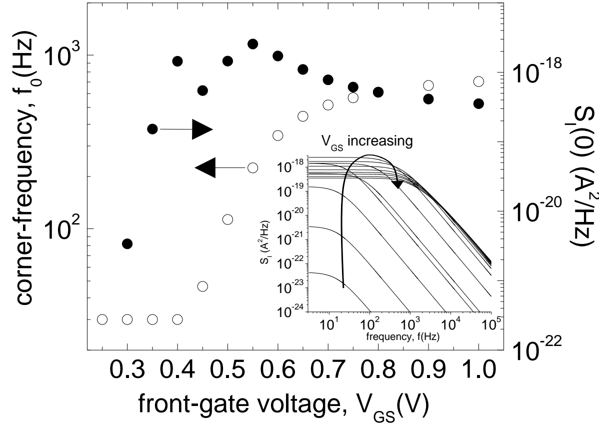

Figure 3.24: Simulated corner-frequencies f_0 and plateau value $S_I(0)$ of the Lorentzian component as a function of the front-gate voltage. The trap responsible for these spectra corresponds to trap # 1 of the extension-less sample in Table 3.3. The back-gate voltage is 0 V. Inset: detail of the variation of the corresponding Lorentzian spectra with gate voltage.

gate-voltages ($V_{GS} \leq 0.4$ V), $n \ll n_1$ (Fig. 3.23a) and τ and f_0 are constant (open circles in Fig. 3.24). In this region, the plateau value $S_I(0)$ increases both by an increase of the term ($\mu_{n,eff}RF$) in (3.41) and by the variation of the occupancy factor $f_t(1-f_t)$ (solid circles in Fig. 3.24). This last term reaches its maximum value, 0.25, when E_F coincides with E_T. In bulk transistors, where complete depletion is achieved, this cross point occurs at a given point inside the depleted region. Its exact position depends on the energy position of the trap inside the band gap [76]. In the transistor of Fig. 3.23a, this occurs when the electron concentration equals n_1, at a given gate voltage (V_{GS}= 0.4 V). In a FD SOI transistor, the Fermi levels at the front- and back- interface are established by their respective gate voltages. Thus, the value of the top gate voltage V_{GS}, at which $n = n_1$, can vary depending on the value of the back gate voltage, V_B. In Fig. 3.23a, the Fermi level coincides with the trap level practically along the whole channel ($n = n_1$) for V_{GS}= 0.4 V. The occupancy factor is maximum under this condition. A null back gate voltage is considered in this calculation.

Higher values of V_{GS} imply that n is always greater than n_1 in the whole channel (Fig. 3.23a). That means that decreases as a function of n and hence, f_0 increases (open circles in Fig. 3.24). The plateau value of the PSD $S_I(0)$

follows another trend with the gate voltage. At low gate voltages, while the time-constant does not vary, it increases with V_{GS} due to the increase of $f_t(1-f_t)$ towards 0.25 and an increase in the $(\mu_{n,eff}RF)$ factor. Above this point, if V_{GS} keeps increasing, the Fermi level moves away from the trap level and a competition is established between the increasing $(\mu_{n,eff}RF)$ factor and the decreasing and $f_t(1-f_t)$ factors. At higher values of V_{GS}, and $f_t(1-f_t)$ decrease quicker than $(\mu_{n,eff}RF)$ increases. Hence, $S_I(0)$ decreases, as seen with solid circles in Fig. 3.24.

The features of the g-r noise produced by traps in FD SOI MOSFETs give specific clues on how to characterize these traps. Inset of Fig. 3.24 shows the evolution of the g-r noise produced by the $E_{T1}-E_i$=0.32 eV trap. The maximum of the plateau value $S_I(0)$ or the point where f_0 starts increasing with the gate voltage are an indicator of the energy position of the trap. The position of the Fermi level evaluated at the gate voltage where these features are observed determines the energy position of the trap. Once the energy position of the trap is determined, the f_0 provides the value of the electron and hole capture cross-section, σ_n and σ_p, respectively ($c_n = v_{th,n}\sigma_n$, $c_p = v_{th,p}\sigma_p$). Finally, the magnitude of the PSD is an indicator of the concentration of traps. In consequence, the trap parameters can be accurately determined by studying the gate voltage dependence over a sufficiently wide range at a fixed temperature.

Particular cases, that do not follow exactly the trend shown above, can also be expected. More shallow traps or small ranges of V_{GS} (producing a small variation of the Fermi level inside the band gap) may not produce this complete variation of τ and $S_I(0)$ with the gate voltage. Fig. 3.23b shows an example for a shallow trap and a narrow band gap scanning. For this case, we would obtain almost constant f_0 and $S_I(0)$ in the whole gate voltage range. This is equivalent to analyze the sample in Fig. 3.24 only in the range V_{GS} [0.7, 1] V. This leads to an indetermination of the parameters of the trap (E_T and N_T). Therefore, the use of the widest range of possible gate voltages is recommended in the measurement process in order to define the traps properly. A way to tackle this problem would be to modify the value of V_B. The study presented in Fig. 3.23 has been made for V_B=0 V. The variation of this voltage would open the door to a characterization of traps within the Si film, for example, a full spectroscopic characterization might be done at a fixed temperature, e.g., room temperature by varying the back-gate voltage. This is a topic for future consideration.

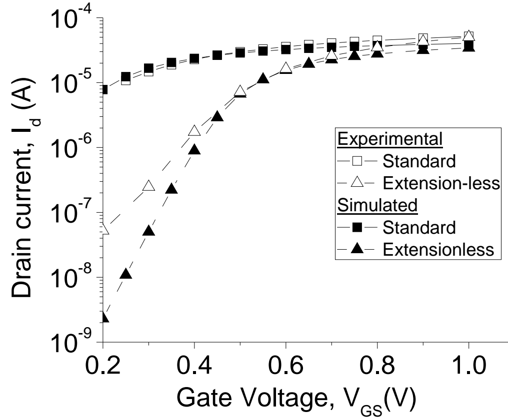

Figure 3.25: Comparison between experimental (open symbols) and simulated (solid symbols) current-voltage curves for a standard junction sample (squares) and an extension-less sample (triangles).

3.5.3.2 Experimental details: Static and noise characteristic

The characterization technique developed in the previous section is tested on nMOSFET transistors fabricated on 300 mm Ultra-Thin Buried Oxide (UTBOX) SOI wafers. All the samples have a 5 nm front SiO_2, a 20 nm thick Si film, a 10 nm buried oxide (BOX), and a channel width of 1 μm. Standard extension samples (Fig. 3.22a) are distinguished from those without extension implantations called extension-less samples (Fig. 3.22b). The objective is to characterize different structures that are now subject of study for 1T-DRAM applications. The former have an effective channel length of 105 nm, for the latter the channel is much larger due to the inclusion of spacers and the absence of extension implantations. A sketch of both structures can be found in Fig. 3.22. The channel is expected to show an almost-undoped behavior with a doping level $N_A \approx 10^{15}$ cm^{-3}.

The drain-current I_D is measured as a function of V_{GS}. The back-gate voltage is kept constant at 0 V and a low drain-to-source voltage ($V_{DS} = 50$ mV) is applied in order to work in the linear regime. Fig. 3.25 shows a comparison between experimental and simulated I-V curves. The standard nMOSFETs shows a lower threshold voltage ($V_T = 0.05$ V) than the extension-less sample ($V_T =$

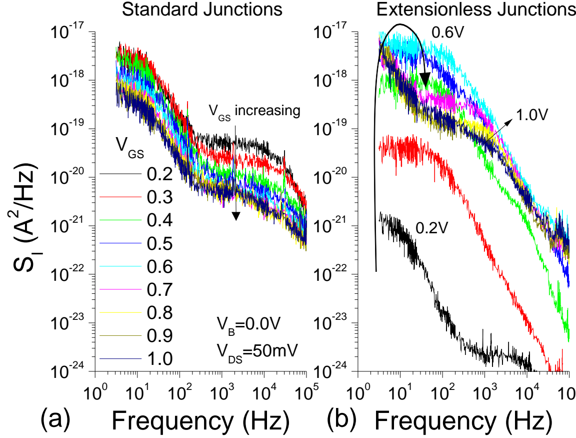

Figure 3.26: Noise spectra for two different samples: a standard junction sample and another one without extension implantation (extension-less sample).

0.37 V). From the static characteristic of the nMOSFETs it can be concluded that in the range 0.2 - 1.0 V the standard junction sample is working in inversion regime, while the extension-less sample varies from depletion to inversion regime. That means that the Fermi level covers a wider portion of the band gap in the extension-less device than in the standard one. This can be also observed in the PSD S_I measured for the same two samples, Fig. 3.26. The range swept by the values of the noise spectra is clearly higher in the extension-less transistor, rather than in the standard device.

The noise has been measured on wafer in linear operation, with zero back-gate bias and the front-gate bias stepped from weak to strong inversion. The LF noise spectra for a standard junction device are dominated by g-r noise (Fig. 3.26a), and it is almost invariant in the whole range of applied gate-voltages. S_I varies within a decade, in agreement with the range of I_D (Fig. 3.25, square symbols). Two clear Lorentzian spectra are found with corner-frequencies f_0 at 4 Hz and 7.5 KHz. These corner-frequencies are independent of V_{GS}.

In the case of the extension-less sample, the noise exhibits a larger variation (Fig. 3.26b). The noise magnitude changes four orders of magnitude, which is also in agreement with the I-V measurements.

Fig. 3.27 shows four examples of the comparison between the experimental and simulated PSD of the drain current noise S_I at two V_{GS} in two different

samples: the standard junction sample and the extension-less sample. A more extensive study considering a wider V_{GS} range is summarized in Figs. 3.28 and 3.29 where experimental and simulated corner-frequencies f_0 and noise levels $S_I(0)$ are compared. A good agreement is obtained. However, it is worth mentioning how the parameters of the traps, used in the simulation and summarized in Table 3.3, origin of the noise spectra, are determined.

Initially, the experimental spectra are decomposed into a flicker noise component and two g-r noise components. These noise components are depicted with the global S_I in Fig. 3.27. Figs. 3.27a and 3.27b confirm that the noise for a standard junction sample is always dominated by two g-r components in the whole range of voltages and frequencies. Fig. 3.28b represents the experimental corner-frequencies associated to these two g-r components (solid squares) as a function of V_{GS}. Unlike the standard junction sample, the extension-less sample presents a $1/f$ component which is of the same order of magnitude as the two g-r components, thus, playing a similar influence on the total noise (Fig. 3.27c and 3.27d).

Fig. 3.26b shows that, at low values of V_{GS}, the noise of an extension-less sample seems to be dominated by two g-r components. In the case of V_{GS}=0.2 V, a Lorentzian clearly appears at low frequencies and a second one at higher frequencies with a lower plateau level. At V_{GS}=0.3 V, only one of these Lorentzian spectra is observed. Two g-r components can be observed again at V_{GS}=0.4 V. The plateau level of the LF g-r component increases as V_{GS} is increased until

Table 3.3: Traps considered in the simulations

Parameter	Standard	Extension-less	Units
N_{T1}	5×10^{13}	1×10^{16}	cm^{-3}
$E_{T1} - E_i$	0.41	0.32	eV
σ_{n1}	5.8×10^{-24}	1.0×10^{-21}	cm^2
σ_{p1}	–	4.4×10^{-14}	cm^2
N_{T2}	1×10^{14}	1×10^{17}	cm^{-3}
$E_{T2} - E_i$	0.43	0.16	eV
σ_{n2}	5.8×10^{-21}	2.5×10^{-19}	cm^2
σ_{p2}	–	1.4×10^{-16}	cm^2

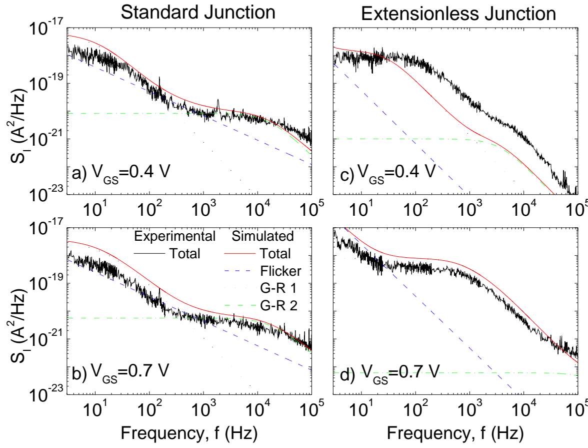

Figure 3.27: Comparison between experimental and simulated PSD of the drain current noise for a standard junction sample (a and b) and for an extension-less sample (c and d) at two different V_{GS} voltages. The simulated total noise component has been depicted with its three different components: flicker noise component and the two generation-recombination components.

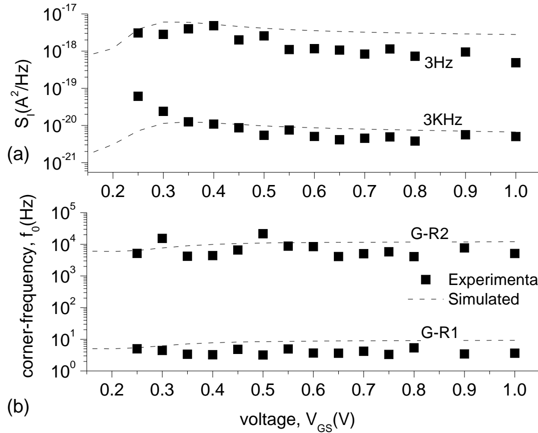

Figure 3.28: Comparison between simulations and experimental noise data: a) Plateau value $S_I(0)$ of the two g-r components, obtained at two frequencies for a standard junction sample, and b) position of the corner-frequency for the two Lorentzian curves produced by two different traps that appear in Fig. 3.26a.

V_{GS}=0.6 V (Fig. 3.26b). For $V_{GS} \geq 0.7$ V, only one g-r component is observed with decreasing magnitude, and a $1/f$ component appears at low-frequencies (1-100 Hz). The corner-frequencies extracted from these experimental spectra are represented in Fig. 3.29b as a function of V_{GS} (solid squares). An interesting point observed in Fig. 3.29b is that the corner-frequencies of both g-r components (G-$R1$ and G-$R2$) increase with the V_{GS}, with the exception of the high f_0 at V_{GS}=0.2 V which requires special attention.

Once the different components are extracted from the spectra, an analysis of the individual g-r or $1/f$ components is done in order to extract information on the traps origin of the noise. The parameters extracted this way are introduced in the simulation, and the numerical results checked with the experimental data. The $1/f^{\alpha}$ component that arises in Fig. 3.26b is reproduced with a UFNM, with modifications and improvements that extend to trap distributions with gradients, that was presented in Sec. 3.5.1.3. There, (3.27) provides an expression for this non-uniform oxide-trap distribution. We have considered a trap-density at midgap of $N_{ox,0}$=5.7$\times$10^5 cm^{-3}eV^{-1}, and the following factors: ξ_1=16.5 eV^{-1}, ξ=-19.12 eV^{-1}, and η=9.47$\times$10^7 cm^{-1} that account for energy, voltage, and depth dependences of the trap within the oxide, respectively. The analysis of the g-r noise is done by assuming two traps which parameters are summarized in Table 3.3. For each one, Lorentzian g-r spectra are evaluated at different gate voltages according to (3.41). In order to compare our results with the experimental data, we analyze the corner-frequencies and the plateau values $S_I(0)$ of the experimental and calculated spectra.

Figs. 3.28 and 3.29 show these correlations for a standard and an extension-less sample, respectively. The plateau values $S_I(0)$ for the standard sample are measured or evaluated at 3 Hz and 3 KHz. Fig. 3.28a shows a good agreement between these experimental and calculated values of $S_I(0)$. The small decrease of $S_I(0)$ with V_{GS} corresponds to the tail of $S_I(0)$ in Fig. 3.24 at high V_{GS}. According to Sec. 3.5.3.1, a deeper trap with higher concentration could also interpret the results. Therefore, an indetermination in the exact values of N_T and $E_T - E_i$ exists. Fig. 3.28b shows in symbols the values of two corner-frequencies extracted from the experimental data as a function of V_{GS}. These two corner-frequencies are also reproduced by our simulations.

The simulated and experimental S_I magnitudes for an extension-less sample are analyzed at 3 and 100 Hz (Fig. 3.29a). The 3 Hz frequency is chosen in order

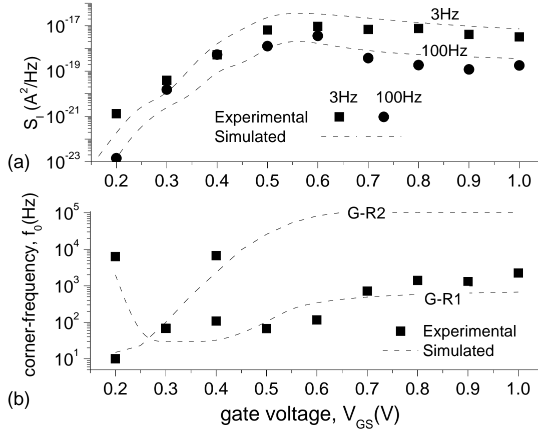

Figure 3.29: Comparison between simulations and experimental noise data: a) Plateau value $S_I(0)$ of the two g-r components, obtained at two frequencies for an extension-less junction sample, and b) position of the corner-frequency for the two Lorentzian spectrum that appear in Fig. 3.26b.

to analyze the $1/f$ component plus one of the g-r components (G-$R2$). The 100 Hz frequency allows for the analysis of the other g-r component. In both cases, at low V_{GS}, the noise magnitude increases when V_{GS} increases. At $V_{GS} = 0.6$ V, the g-r component reaches its maximum value (see Figs. 3.26b or 3.29a) and then starts decreasing. Fig. 3.29a gives a more precise view of this phenomenon. It shows that at 3 Hz the $1/f$ component makes the noise to remain almost constant for $V_{GS} > 0.6$ V, while at 100 Hz there is a clear decrease of the noise magnitude. The reason is that, at 100 Hz, the noise is controlled only by the g-r component (this behavior can be seen in Figs. 3.24 and 3.27d).

An important behavior found in the measurements for an extension-less sample is that the f_0 increases as a function of the V_{GS} (lines in Fig. 3.29b). Several authors have suggested that this should be related to traps located within the oxide [76]. However, as mentioned in the previous section, traps in the semiconductor are responsible for such a behavior. Moreover, the same trend is reproduced by the simulations considering traps located within the Si film (closed symbols in Fig. 3.29b). It should be remarked that the low f_0, observed for $V_{GS} \leq 0.3$ V is originated by a trap located at $E_{T2} - E_i$=0.16 eV, which parameters are detailed in Table 3.3. The noise produced by this trap quickly

disappears as V_{GS} increases because it is overshadowed by the noise that the other trap (E_{T1}) produces.

The high value of f_0 observed at V_{GS}=0.2 V can be interpreted by a trap that behaves as a hole trap in this voltage regime. The shallower trap, $E_{T1} - E_i$ = 0.32 eV reproduces the G-$R1$ noise component for V_{GS} >0.3 V, where it behaves as an electron trap. This dual behavior of a hole and electron trap can be achieved with proper values for σ_n and σ_p [78], [79]. This dual behavior has previously been observed in other devices [24]. As a hole trap, the term $c_p \times p$ is dominant in the denominator of the time-constant (3.5). In that condition, this trap is responsible for the higher corner-frequency $f_0 \approx 4 \times 10^3$ Hz (Fig. 3.29b at V_{GS}=0.2 V) which is in agreement with the one found in the experimental noise. For higher V_{GS}, the E_{T1} trap becomes an electron trap and produces a constant f_0 ($\sim$ 30Hz) until the gate-voltage reaches 0.4 V. From there on, f_0 is increasing as a function of V_{GS}. The increment in the f_0 is about one decade for the studied range of voltages. It is remarkable how the abnormal trend at 0.2 V allows for the determination of σ_p of the E_{T1} trap, apart from the determination of the σ_n from the analysis of the rest of the gate voltage range. For the E_{T2} trap, the σ_p is undetermined, although it does not affect the determination of σ_n.

4

Miniband structure and optical absorption (simulation tools for nanostructures)

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4.1 Introduction

In this chapter we calculate the conduction miniband energy dispersion relation in quantum periodic nanostructures embedded into a matrix of other semiconductor material. Our main aim is to evaluate the behavior of these nanostructures when used as optoelectronic components such as photodetectors. Hence, that we put special emphasis on the study of the optical absorption response of these systems. We take into consideration the effects of nonparabolicity and anisotropy and the different electron states arising from each valley when solving the Schrödinger equation. When necessary, strain is also included in this analysis in order to obtain the conduction band offset between the materials by solving the Pikus-Bir 8×8 $\vec{k} \cdot \vec{p}$ Hamiltonian. From these results, we investigate the intra-miniband photon absorption coefficient for those transitions between minibands arising from the conduction band. We analyze the influence of light polarization, level of doping, and volumes and shapes of the systems, in order to ascertain the best conditions for operation.

To deal with a certain material means to work with a set of properties which are established beforehand. More often, these properties are well defined (i.e. band gap, effective mass, absorption coefficient,...etc) and cannot be modified which reduces its range of application. In addition, working with semiconductor materials reduces the number of candidates since there is a fixed number of them, thus the options are even fewer. The use of nanometric semiconductor structures embedded into other semiconductor materials has been proposed to obtain new pseudomaterials with new properties in order to overcome this problem. The reduced dimensions of such structures involve exciton confinement in the spatial dimensions. Consequently, such materials have electronic properties intermediate between those of bulk semiconductors and those of discrete nanostructures. This opens the door to the science of tunable materials. However, one of the most important conclusions of all these works is that a certain amount of order is required to obtain the desirable behavior.

The physics of ordered nanostructures has become a topic of interest in current research on semiconductor devices, due mainly to its potential applications in optoelectronic devices [80–82]. For instance, they have been proposed to be a plausible candidate for photodetectors, especially for Quantum-Dot Infrared Photodetector (QDIP) [83], for the Quantum-Dot Intermediate Band Solar Cell

(QD-IBSC) [81, 84–86], for the quantum computer [87], transistors, LEDs, and a large etcetera.

The classification of these nanostructures is based on the dimensions of the confinement and the symmetry of the system. Hence, nanometric wires repeated along one dimension and with 1-D confinement are called quantum wells, and quantum wires (QW) if the repetition is along two dimensions and the confinement is in 2-D. Tiny nanostructures repeated along three dimensions and with 3-D confinement are called quantum dots (QD), and its shapes can be very varied (cubes, cuboids, pyramids, truncate pyramids,...etc). Although, there exist other nanostructures such as nanoribbons, nanorods, nanopillars,...etc, in this work we focus only on those with an ordered spatial distribution.

Regarding 1-D ordered nanostructures, much research has been done on superlattices, revealing their unique features in optoelectronic applications [88,89] and carrier transport [90,91]. Nevertheless, 2-D and 3-D ordered nanostructures are still a challenging area in the experimental field. In addition, manufacturing uniform nanostructures is a challenging area in the experimental field [92, 93], and most of the investigations on these structures are carried out on assembled QD created mainly by the Stranski-Krastanov technique [94], in which a certain amount of disorder is inevitable. For this reason, the theoretical effects of the order are not generally observed. Although some noteworthy techniques for obtaining highly ordered nanostructures in two and three dimensions have been developed by means of patterns [95], the periodicity of these systems is about 50–100 nm. Consequently, coupling between confined states of neighboring structures is negligible in most cases. Recently, researchers have proposed experimental techniques to obtain a novel kind of ordered nanostructure [96]. These procedures make it possible to obtain ordered QW arrays and from them to obtain ordered quantum dotlike effects arising from some spatial regions of the structure.

However, theoretical research is needed to predict the behavior of such systems, and consequently, to anticipate its potential applications. In this work, we focus on two ordered nanostructures: the quantum wires (QW) and the quantum dots (QD). Both of them are regimented structures in 2-D and 3-D respectively. In such ordered systems a miniband structure appears as long as an interaction between neighboring nanostructures exists. In this chapter, a model for comput-

ing the miniband structure taking into account different values of the effective mass for the quantum nanostructure and the matrix materials is presented in Sec. 4.2.1. In Sec. 4.2.2 another model for computing the absorption coefficient considering the results of the miniband structure for these systems is presented. Finally, these two models are applied to the two different regimented nanostructures, QDs and QWs, in order to study the dependence of the miniband structure and absorption coefficient with different geometrical parameters such as sizes and shapes, Sec. 4.4.

4.2 Theory

This section describes the method to obtain the miniband structure of regimented nanostructures. Although this method can be also applied to the valence band, in this work we focused on that miniband structure arising from electronic states belonging to the conduction band. Different effective masses for the quatum nanostructure material and the matrix material are taking into account in the calculations. The model which uses the results of the miniband structure for computing the intra-miniband absorption coefficient is also described in this section.

4.2.1 Minibands and different effective masses.

In order to be able to describe the behavior of electrons and holes within a bulk material we have to solve the Schrödinger equation independent of the time:

$$H\Psi_n = E_n\Psi_n \tag{4.1}$$

being Ψ_n the wave function, E_n the energy of each state (also know as eigenenergy), and H the Hamiltonian which is described by two operators: the kinetic energy operator (T_{op}) and the potential energy operator (V_{op}). Under the effective mass approach (EMA) [97–99] the Hamiltonian can be written as:

$$H\Psi_n = T_{op}\Psi_n + V_{op}\Psi_n = -\frac{\hbar^2}{2m}\left[\nabla\frac{1}{m(\vec{r})}\nabla\right]\Psi_n + V_{op}\Psi_n = E_n\Psi_n \tag{4.2}$$

The systems under study throughout this work are always ordered nanostructures in 2-D or 3-D. Periodic arrays of nanostructures give rise to a periodic

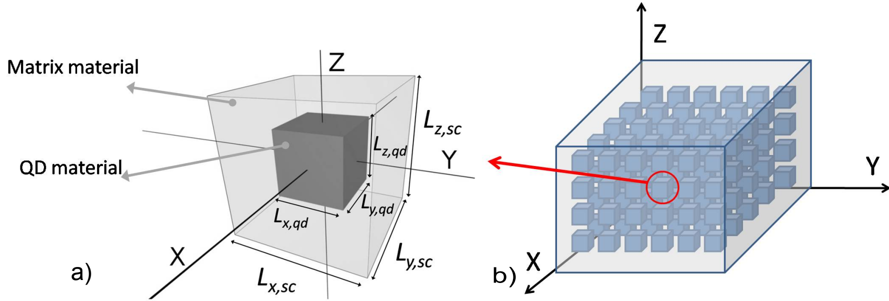


Figure 4.1: a) *Supercell* of the periodic nanostructure. b) The repetition of the *supercell* in the x, y and z directions provides the new pseudomaterial which corresponds with the studied system.

electrostatic potential profile which simplifies the solutions of (4.2).

The nanostructures are aligned along the X, Y, and/or Z axes. An example of these structures is shown in Fig. 4.1 where a cubic nanostructure is repeated along the three spatial coordinates (Fig. 4.1a shows a detail of one of the *supercells*).

This system is similar to those previously studied and described in the literature [80], [81] using analytical solutions of the Schrödinger equation. However, these previous approaches are based on a separable potential $V(\vec{r})$ that could be expressed as a sum of three potentials $V(\vec{r}) = V_x(x) + V_y(y) + V_z(z)$. This potential is not accurate, since it gives rise to regions of the space where the barrier is twice or three times higher than the real value. Nevertheless, the authors considered it to be a good approach since coupling between the nearest neighboring dots is exactly calculated, and those regions with higher barriers are between dots placed further apart. We will deal with this specific issue further on in our investigation and discuss the main effects of such a simplified approach, Sec. 4.3.2.

Our approach starts from the Schrödinger equation in the periodic system, where the Bloch-Floquet theorem provides the structure of the solutions:

$$\Psi_{\vec{q},n} = \eta_{\vec{q},n}(\vec{r})e^{i\vec{q}\vec{r}} \tag{4.3}$$

In (4.3) the wave function is written as the product of a plane wave and a function with the periodicity of the *supercell*, $\vec{q}$ being the wave vector related

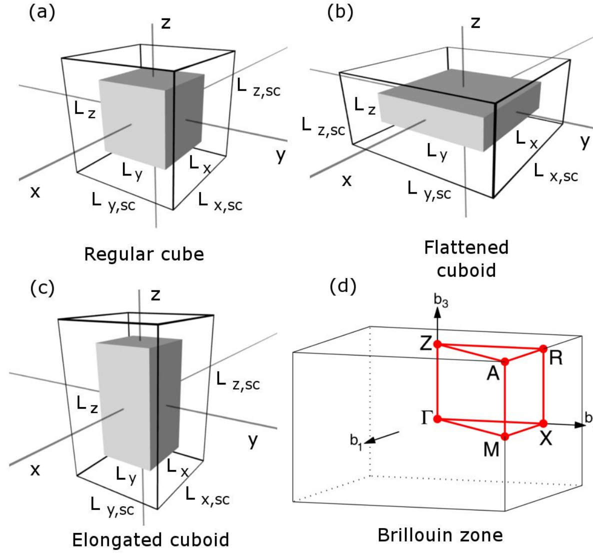


Figure 4.2: Different shapes of the *supercell* for QD having different shapes: a) regular cubes, b) flattened cuboids, and c) elongated cuboids. The equivalent Q-space is depicted in d).

to the *supercell* periodicity, and $\eta_{\vec{q},n}(\vec{r})$ being a $\vec{q}$-dependent function with the same period of potential (n is the miniband quantum number). Therefore $\eta_{\vec{q},n}$ can be expanded into a plane waves base:

$$\eta_{\vec{q},n} = \sum_{n=-N}^{N} \sum_{m=-M}^{M} \sum_{l=-L}^{L} \frac{c_{n,m,l}}{\sqrt{2\pi}} e^{i(k_{x,n}x + k_{y,m}y + k_{z,l}z)} \tag{4.4}$$

where

$$k_{x,n} = \frac{2\pi n}{L_{x,sc}}; k_{y,m} = \frac{2\pi m}{L_{y,sc}}; k_{z,l} = \frac{2\pi l}{L_{z,sc}}; \tag{4.5}$$

$L_{x,sc}$, $L_{y,sc}$, and $L_{z,sc}$ are the lengths of the *supercell* in each of the directions (Fig. 4.1a). The resulting wave function has $(2N+1)(2M+1)(2L+1)$ terms, since $n = 0, \pm 1, \pm 2, ..., \pm N$. The counterparts of $\vec{q}$ and $\eta_{\vec{q},n}$ in regular crystal theory would be $\vec{k}$ and $u_{\vec{k},n}(\vec{r})$ respectively. In a similar way, this treatment leads to the existence of a Q space analogous to the K space of regular crystals, where states in a miniband can be labeled using a $\vec{q}$ vector, Fig. 4.2d. Combining

(4.4) and (4.3) into (4.2), left-multiplying by the complex-conjugator of (4.4) and integrating in the whole space we obtained a matrix to be diagonalized in order to obtain the eigenenergies and envelope functions for the selected point of the Q-space.

The existence of different materials within the *supercell* makes this system more complex than regular crystals, which have few atoms in their unit cell. As mentioned before and in order to obtain a physical insight into these systems, we modeled the structures within the *supercell* by means of an improved modification of the effective mass approach (EMA) where anisotropy and non-parabolicity of the conduction band are included to obtain a more accurate description of the system [97–99]. Therefore, the Schrödinger equation can be expressed as (4.2).

To differentiate the effective mass of the quantum material (m_{qd}) from the matrix material (m_{ma}) we use the expression:

$$\begin{aligned} \frac{1}{m(\vec{r})} &= \frac{1}{m_{ma}} + \frac{m_{ma} - m_{qd}}{m_{ma} m_{qd}} \\ &\times \chi(-\frac{L_{x,qd}}{2}, x, \frac{L_{x,qd}}{2})\chi(-\frac{L_{y,qd}}{2}, y, \frac{L_{y,qd}}{2})\chi(-\frac{L_{z,qd}}{2}, z, \frac{L_{z,qd}}{2}) \end{aligned} \tag{4.6}$$

where the function $\chi(a, b, c)$ is a window function with a value in the b-axis of one for $a \leq b \leq c$ and zero for the rest of positions. In that way, we can compute the kinetic energy of the system using this expression:

$$\begin{aligned} \left\langle \vec{q_\alpha}, \vec{k_a} | T_{op} | \vec{q_\beta}, \vec{k_b} \right\rangle &= \frac{\hbar^2}{2m_{ma}} \delta(\vec{q_\beta} - \vec{q_\alpha}) \times [(\vec{q_\beta} + \vec{k_b})^2 \times \delta(\vec{k_b} - \vec{k_a}) + \\ &+ \frac{8}{L_{x,sc} L_{y,sc} L_{z,sc}} \frac{m_{ma} - m_{qd}}{m_{qd}} (\vec{q_\beta} + \vec{k_b})(\vec{q_\beta} + \vec{k_a}) \\ &\times g_x(\vec{k_b} - \vec{k_a}) g_y(\vec{k_b} - \vec{k_a}) g_z(\vec{k_b} - \vec{k_a})] \end{aligned} \tag{4.7}$$

where $\vec{k_a} = k_{x,n}\hat{\imath} + k_{y,m}\hat{\jmath} + k_{z,l}\hat{k}$ and $\vec{k_b} = k_{x,r}\hat{\imath} + k_{y,s}\hat{\jmath} + k_{z,t}\hat{k}$. The function $g_c(k_a - k_b)$ is given by:

$$g_c(k_a - k_b) = \begin{cases} \frac{sin((k_{c,a} - k_{c,b})\frac{L_{qd,c}}{2})}{k_{c,a} - k_{c,b}} & \text{if } k_{c,a} \neq k_{c,b} \\ \frac{L_{qd,c}}{2} & \text{if } k_{c,a} = k_{c,b} \end{cases} \tag{4.8}$$

4.2.2 Absorption.

To study photon interaction in such periodic nanostructure arrays, we used the time-dependent perturbation theory, this being the Hamiltonian of the perturbed system [100].

$$H'(\vec{r},t) \cong -\frac{|q|}{m_0}\vec{A}\cdot\vec{p} \tag{4.9}$$

where $|q|$ and m_0 are the absolute values of the electric charge and the electron rest mass, respectively, $\vec{p}=-i\hbar\nabla$ the linear momentum operator and $\vec{A}$ is the potential vector of the radiation which can be expressed as:

$$\vec{A}=\widehat{\xi}\left\{\frac{A_0}{2}e^{i(\vec{k_{op}}\cdot\vec{r}-\omega t)}+\frac{A_0}{2}e^{-i(\vec{k_{op}}\cdot\vec{r}-\omega t)}\right\} \tag{4.10}$$

where $\vec{k_{op}}$ is the wave vector of the radiation within the material in which the radiation is propagating, $\widehat{\xi}$ is the polarization of the potential vector of the photon. Taking into account that in the Fermi's Golden Rule the time-dependent term gives the energy conservation, equation (4.9) can be rewritten as:

$$H'(\vec{r}) \cong -\frac{|q|A_0}{2m_0}e^{i(\vec{k_{op}}\cdot\vec{r})}\widehat{\xi}\cdot\vec{p} \tag{4.11}$$

On the other side, the theoretical expression of the absorption coefficient in regimented nanostructures is given by:

$$\alpha(\hbar\omega_{op})=\sum_{n_i}\sum_{n_f>n_i}\frac{w_{n_i\to n_f}(\hbar\omega_{op})}{V} \tag{4.12}$$

where $w_{n_i\to n_f}(\hbar\omega_{op})$ is the absorption probability for transitions going from the n_i to the n_f minibands, $\hbar\omega_{op}$ is the photon energy and V is the volume of the periodic nanostructure. Taking into account (4.11), $w_{n_i\to n_f}(\hbar\omega_{op})$ can be obtained considering the following expression [101, 102]:

$$w_{n_i\to n_f}(\hbar\omega_{op})=\frac{\hbar^2\pi|q|^2}{n_r c_{light}\epsilon_0 m_0^2\omega_{op}}\int_{Q-space}f(E_{n_i})\left(1-f(E_{n_f})\right) \tag{4.13}$$
$$\times|\widehat{\xi}\cdot\int_{supercell}\eta^*_{\vec{q},n_f}(\vec{r})\nabla\eta_{\vec{q},n_i}d\vec{r}|^2\delta(E_{n_f}-E_{n_i}-\hbar\omega_{op})\rho_Q d\vec{q}$$

n_r is the mean refraction index in the system, c_{light} is the speed of light in

vacuum, ϵ_0 is the vacuum dielectric constant, ω_{op} is the photon frequency, $f(E)$ is the Fermi-Dirac function, and ρ_Q is the density of states in the Q-space.

For a given array with a miniband structure, (4.13) provides a result depending on light polarization ($\vec{\xi}$) and the position of the Fermi level ($f(E)$). In order to increase the absorption, it is desirable to place the Fermi level between the two lowest minibands. In this manner, the lowest miniband would be almost full of carriers and the second one would be almost empty, having a high number of available states to receive the carrier after the absorption. Nevertheless, our calculations indicate that this implies very high levels of doping, leading to undesired effects because of impurities. A Fermi level located just at the bottom of the bulk conduction band might be related to a medium or high level of doping, close to the doping results reported elsewhere [84]. Therefore, a study of position of the Fermi level is needed in order to relate the doping level with the optical absorption levels. We will return to this topic within the results section.

4.3 Validations

4.3.1 Number of plane waves and minibands

In order to obtain suitable results, we carried out an investigation about the convergence of the calculations *vs.* the number of terms used in the expansion. Considering a low number of terms in the expansions would provide spurious results, while a high number of terms would need important computational resources. Therefore, a compromise should be established.

For instance, the following study is carried out for a cubic QD where the three spatial component are equivalent. Taking into account that the total number of plane waves is $(2N+1)(2M+1)(2L+1)$ and assuming that N=M=L, Fig. 4.3 shows the eigenenergies obtained for the lowest 15 eigenenergies versus the N parameter. The nanostructure that we have chosen for carrying out this study is a silicon 2-D periodic nanostructure of QW embedded into a SiO_2 matrix. A sketch of such a nanostructure is depicted in Fig. 4.5a. We considered the possibility of different behaviors in the convergence of the solutions, depending on the point in the Q-space. Therefore, the calculations were carried out at three different points of the Q-space: M, Γ, and X (see Fig. 4.2d).

The convergence of the simulations could be also affected by the size of the nanostructure. In this regard, we have chosen a small nanostructure of 3 nm

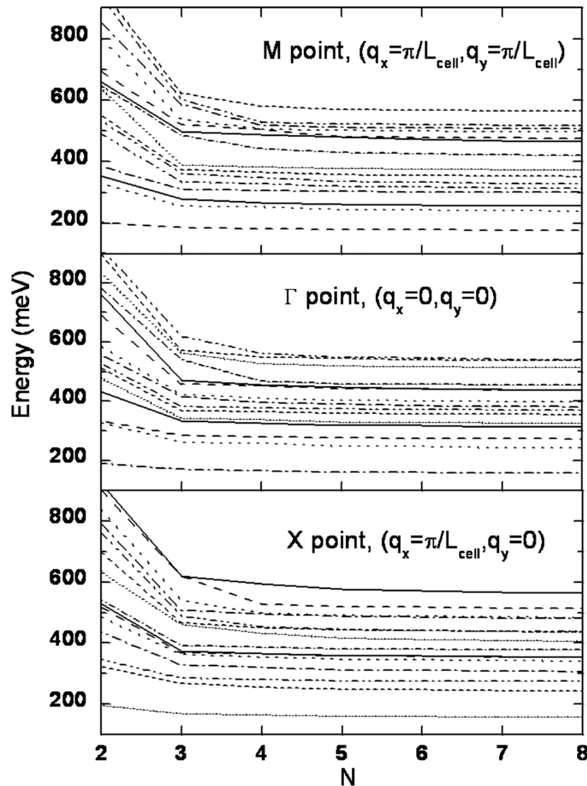


Figure 4.3: Lowest 15 eigenenergies of the system studied with sizes $L_{supercell}$=6 nm and L_{wire}=3 nm evaluated at several points of the Q-space for a Si quantum wire nanostructure repeated along 2 dimensions and embedded in a SiO_2 matrix.

width in order to cope with this problem. From these results we agreed that $N = 6$ would be a suitable choice for describing a wide set of low-energy minibands of both nanostructures: QDs and QWs. This value is more than enough for QDs since similar results were obtained for InAs QDs embedded in GaAs with different shapes and sizes [103]. There, the conclusions were that $N = 3$ was enough to describe accurately the system employing suitable computation times.

Regarding the issue of the number of minibands involved in the calculation, we studied the term $f(E_{n_i})\left(1 - f(E_{n_f})\right)$ in (4.13), indicating the probability of having a carrier in the initial state through $f(E_{n_i})$ and the probability of having an empty final state for the carrier before the absorption through $\left(1 - f(E_{n_f})\right)$.

Thus, we established the criterion that the probability of occupation of the states of the highest miniband would be about 10^{-6} times the probability of that of the lowest miniband at room temperature. This provided a suitable set of ten minibands in the system studied, ranging between about 400 and 500 meV for the absorbed photon energy. Therefore, $1 \leq n_i,\, n_f \leq 10$ in (4.12).

The evaluation of the integral in (4.13) was carried out by means of a discretization of 23×23 points in the Q-space. Taking into account the small energy amplitude of the bands, this discretization was good enough to provide accurate results. This value does not affect the accuracy of the results, but the miniband representation by mean of a fine mesh in the Q-space.

4.3.2 Comparison with analytical models

We start by comparing the results provided by the analytical expressions given by Lazarenkova and Balandin [80] with those obtained in our study for cubic QD of InAs embedded in a GaAs matrix. A sketch of this structure can be found in Fig. 4.1. Before going further in the comparison and as mentioned before, it should be noticed that the formalism followed in these works, although providing a good starting point for understanding periodic nanostructures, is not strictly correct from a mathematical point of view. These authors assumed that for a separable potential $V(\vec{r}) = V_x(x) + V_y(y) + V_z(z)$, the total energy of the electron could be expressed as $E_T(\vec{q}) = E_x(q_x) + E_y(q_y) + E_z(q_z)$ and in this way they obtained the dispersion relations from the 1-D Kronig-Penney model. However, the kinetic energy operator is not separable, since $\nabla \frac{1}{m(\vec{r})} \nabla$ cannot be expressed as a sum of three operators, each related to x, y, and z, because of the spatial dependence of $m(\vec{r})$ [102]. Thus, the treatment is not totally accurate, although the effect of this inaccuracy on the published results has not been analyzed, to the authors' knowledge. Other authors have also commented on this approach [86]. Using $axis$ to stand for x, y, or z, the energies $E_{axis}(q_{axis})$ are calculated from [80]:

$$\begin{aligned} cos(q_{axis} L_{axis,sc}) &= cos(k^W_{axis} L_{axis,dot}) cos(k^B_{axis} L_{axis,bar}) \\ &- \frac{1}{2}\left(\frac{k^B_{axis} m_{qd}}{k^W_{axis} m_{ma}} + \frac{k^W_{axis} m_{ma}}{k^B_{axis} m_{qd}}\right) \\ &\times sin(k^W_{axis} L_{axis,dot}) sin(k^B_{axis} L_{axis,bar}) \end{aligned} \tag{4.14}$$

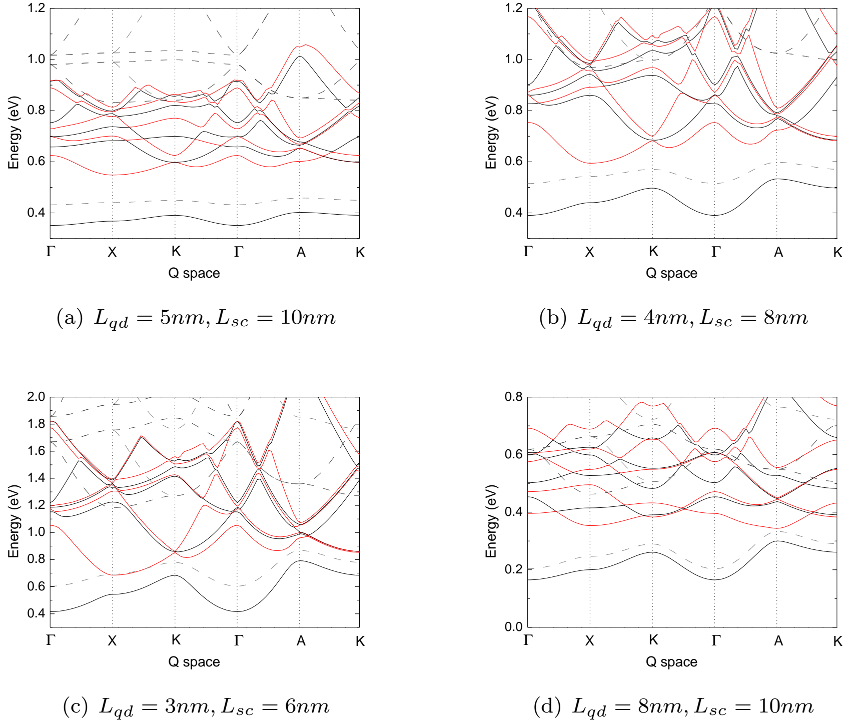
where

$$k^B_{axis} = \frac{\sqrt{2m_{ma}(E_{axis} - V_0)}}{\hbar}, k^W_{axis} = \frac{\sqrt{2m \pm E_{axis}}}{\hbar} \tag{4.15}$$

$L_{axis,dot}$ and $L_{axis,bar}$ are the side length of the dot and the barrier in the direction *axis*. V_0 is the conduction band offset of the system studied. The above expressions are valid only for $E_{axis} > V_0$, but we have extended them for $0 < E_{axis} < V_0$ utilizing complex values of k^B_{axis} and therefore converting sine and cosine functions into hyperbolic ones. In this manner, the states having energies below the matrix conduction band were modeled.

In Fig. 4.4 we compared the miniband structure provided by Lazarenkova and Balandin's model (dashed lines) with those obtained by means of the plane wave method (solid lines) for QDs having a 5 nm side length in a *supercell* with 10 nm side length, $L_{qd}/L_{sc} = 5/10$ (Fig. 4.4a), $L_{qd}/L_{sc} = 4/8$ (Fig. 4.4b), $L_{qd}/L_{sc} = 3/6$ (Fig. 4.4c), and $L_{qd}/L_{sc} = 8/10$ (Fig. 4.4d). Zero energy is defined as the bottom of the InAs conduction band, and hence V_0 =0.5007 eV which corresponds to the conduction band offset between InAs and GaAs including strain effects.

Significant differences are observed between the results given by each model. It is observed that the minibands of Lazarenkova and Balandin's model have higher energies and smaller amplitudes because of the higher confinement (there are regions of the space with $2V_0$ and $3V_0$ potential, $V = V_x + V_y + V_z$, due to simultaneous contributions of two or three potentials; $V_x = V_0$ if $|x| \leq L_{x,qd}$, $V_y = V_0$ if $|y| \leq L_{y,qd}$, $V_z = V_0$ if $|z| \leq L_{z,qd}$). These regions modify the miniband structure significantly, as is well known. However, we focused our attention on Fig. 4.4d (L_{qd}/L_{sc}=8/10), where both methods seem to provide closer results for the lowest energy band. The reason for this could be the smaller ratio of the regions with $2V_0$ and $3V_0$ potentials in relation with the whole *supercell*. In the remaining cases, 50% of the *supercell* is correctly modeled, while 37.5% of the *supercell* has $2V_0$ and 12.5% has $3V_0$. On the other hand, the latter case has 89.6% of the *supercell* correctly modeled, while 9.6% has $2V_0$ and just 0.8% has $3V_0$, thus providing closer values. This is an important point in validating the studies of Lazarenkova and Balandin, since they used QDs of 6.5 nm separated by barriers 1.5 nm thick (6.5 nm QD side length in a *supercell* of 8 nm side length, L_{qd}/L_{sc}=6.5/8), thus correctly modeling a significant percentage of the total *supercell* using this simple approach. To summarize this



(a) $L_{qd} = 5nm, L_{sc} = 10nm$

(b) $L_{qd} = 4nm, L_{sc} = 8nm$

(c) $L_{qd} = 3nm, L_{sc} = 6nm$

(d) $L_{qd} = 8nm, L_{sc} = 10nm$

Figure 4.4: Miniband structure for the four different systems. L_{qd} and L_{sc} are the size length of the quantum dot and the *supercell*, respectively. Solid lines are obtained by means of the plane wave method (black and red are used to distinguish adjoining minibands). Dashed lines are the solution of the 3-D Kronig-Penney model as reported by previous authors

comparison, our approach gives results different from those provided by the above authors, [80,81], although they asserted that their calculations were suitable for investigating periodic cubic QD systems. It has been proved useful only for those cases where barriers are noticeably smaller than QDs, such as those investigated by these authors, but not in the general case where our approach would be closer to the real system.

4.4 Results/structures

In this section, we present the results of miniband structures and absorption coefficients for two different regimented nanostructures: quantum wires (QW) and quantum dots (QD). The results are related to shapes, sizes, Fermi levels, and materials of the nanostructures.

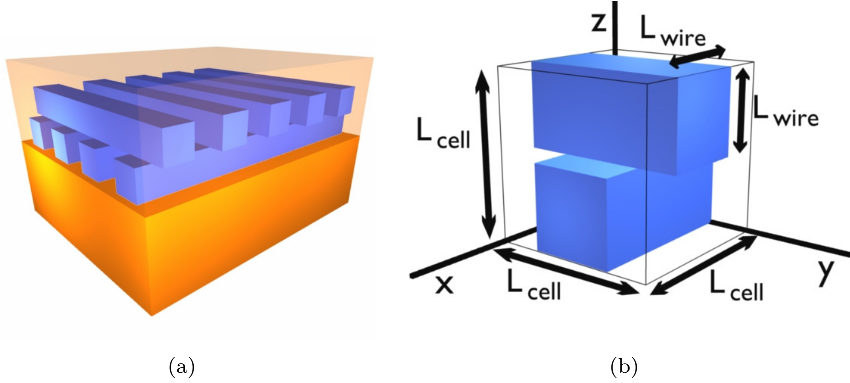
4.4.1 2-D structures. Quantum wires.

Recently, researchers have proposed experimental techniques to obtain a novel kind of ordered nanostructure [96]. These procedures make it possible to obtain ordered quantum wire (QW) arrays and from them to obtain ordered quantum dot-like effects arising from some spatial regions of the structure. An example of such ordered QD nanostructures is depicted in Fig. 4.5a. These QW arrays might behave like an ordered QD system, since there are states where electrons are confined mainly in the crossings of the wires. In these systems, coupling between neighboring structures is very important and gives rise to significant effects in the confinement. Thus, interesting physical behavior can be observed. The highest density reported in such nanostructures has a periodicity of 16 nm, making it likely that coupling between confined states would be observed. If higher densities were obtained, clearer evidence of the coupling might be shown. Theoretical studies would help us gain an insight into the influence of different variables.

It is important to note that recent papers have dealt with the same topic but applied to different periodic systems [86].

4.4.1.1 Description of the system.

The system under study basically consists of a parallel quantum wire array placed over another parallel QW array turned 90°. This structure could be repeated along several layers or simply placed on an insulator layer and covered by a capping layer of a wider energy band gap material to confine carriers in the wires. It was obtained experimentally [96] and studies on confinement and carrier transport have been carried out [104]. However, they focused on the results at only the Γ point and did not provide any result on optical absorption. One of the key features of this structure is the possibility of strong carrier spatial confinement at the crossings of the wires in the lowest energy miniband and a



(a) (b)

Figure 4.5: (a) Periodic 2-D system studied in this section. It is plotted in blue a section of the silicon quantum wire arrays. In orange (both solid and with transparency) is represented the silicon dioxide capping layer. (b) Detail of one of the cells of the periodic nanostructure. Its repetition in the x and y direction provides the studied system. In the z direction there is no repetition. Capping layers above and below the cell are modeled as hard barriers.

significant carrier delocalization along the wires in higher energy minibands [104] that could lead to interesting optoelectronic applications.

We have studied the case of electron confinement in the Si QW array covered by SiO_2, as shown in Fig. 4.5a. Figure 4.5b shows the *supercell* considered in the simulations. Our purpose was to obtain the miniband structure and study the intraband optical transitions caused by photon absorption. We would like to discuss on our approach and in the simplifications we carried out to develop this work. In our simplified model it is assumed that the electrostatic potential is flat inside the wires and in the capping SiO_2. Thus, our premise is that the band bending due to the spatial distribution of the charge would be a second order correction. This will be justified within the optical absorption section. Regarding the valence band, it was assumed that its complexity would not provide miniband gaps useful for absorption [86]. Furthermore, as silicon is an indirect band gap semiconductor, intraband optical transitions might be the dominant absorption process, especially in n-type doped semiconductors.

We used a conduction band offset between Si and SiO_2 of 3.25 eV. We also include the effects of anisotropy and nonparabolicity [97, 98] in the conduction band structure to obtain a better physical description of the system. The six

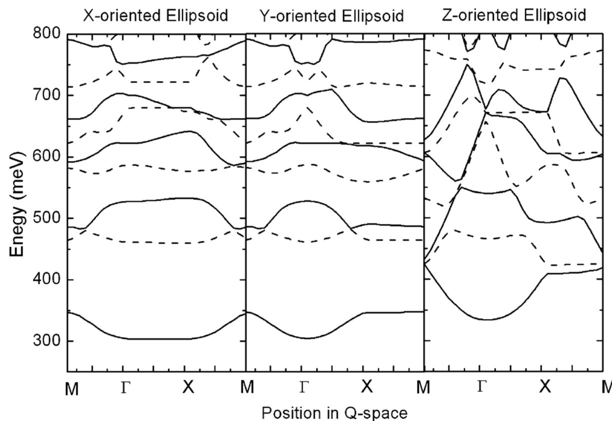


Figure 4.6: Miniband structure of carriers in each ellipsoid along the path depicted in Fig. 4.2 in the Q-space for a system with sizes L_{sc}=4 nm and L_{qd}=2 nm. Solid and dashed lines are used to distinguish alternate minibands.

equivalent valleys at the Si conduction band edge make that the effective masses in each spatial direction are different. In that way, the anisotropy is included in the simulator considering three effective masses for each material both QD or matrix material: $m_{eff,x}$, $m_{eff,y}$, and $m_{eff,z}$.

4.4.1.2 Miniband structure.

We have calculated the miniband structure of the system using the method described in Sec. 4.2.1 and considering L_{sc}=4 nm and L_{wire}=2 nm.

In Fig. 4.6, we plotted the miniband structure obtained for carriers in x-, y-, and z-oriented ellipsoids along the path in the Q-space depicted in Fig. 4.2d. Worthy to note is the existence of an indirect energy gap in the x- and y-oriented ellipsoids between the lowest and the second bands of 100 meV. The existence of a second band gap in the x- and y-oriented ellipsoids is also noticeable between the third and fourth minibands, with an energy 30 meV. Nevertheless, for the purpose of studying light absorption, the value of the first gap has more relevance, since the carrier population of the first miniband will be much higher than that of the third. For this reason, we focus on its value later.

Figure 4.6 also shows the non-existence of miniband gaps in the z-oriented ellipsoids. The different confinement in that direction with respect to the x and

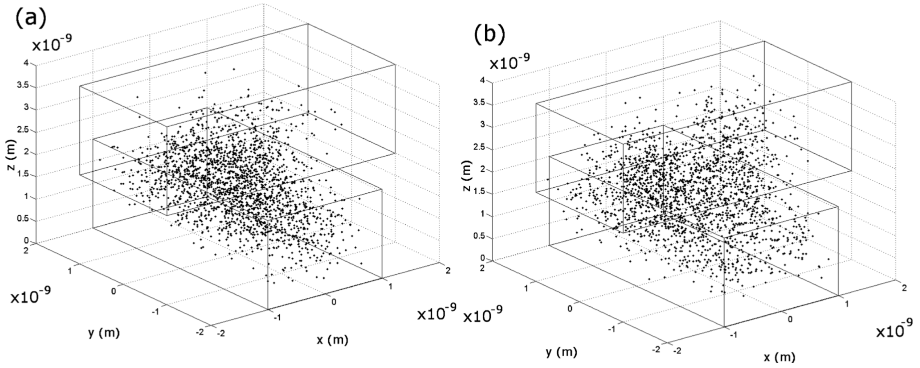


Figure 4.7: Density probability for carriers in the Γ point of the Q-space in the lowest energy miniband (a) and in the second miniband (b). The densities of dots are proportional to the density probabilities.

y directions in the system studied could be the cause of this dissimilar behavior.

The charge distribution is another interesting issue to consider for understanding the physics of this system. In this regard, it is useful to have a picture of the probability density to know the spatial regions populated by carriers. Figure 4.7 shows the probability density for states in the lowest and second minibands in the Γ point of the Q-space. It is noticeable that in both cases carriers tend to be around the crossing. The depicted state of the lowest miniband has a great probability of being in the center of the crossing and just a small part of the charge distribution spreads along the wires. The state of the second miniband seems to have lobes in the charge distribution, and the spreading along the wires seems to be more important.

As it is noticeable in Fig. 4.7a, electrons in the lowest miniband have a more approximate spherical charge distribution around the crossing. Here, taking into consideration that this would be the most occupied miniband, we can do a rough estimation on the aforementioned band bending by assuming a uniformly charged sphere having a radius of 1 nm and evaluating the variation of the electrostatic potential from the center to the border. This calculation would suggest the order of magnitude of the band bending in the crossings. Our calculations in Si suggest a band bending about 50 meV in the crossing ($\Delta V \approx 0.065/r$ eV, r being the sphere radius in nm containing the most of the charge), far of being comparable with the conduction band offset between Si

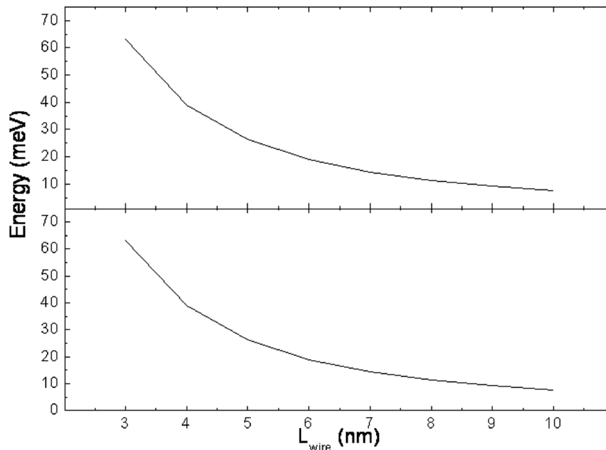


Figure 4.8: Miniband gap between the first and second minibands as a function of L_{wire} ($L_{sc} = 2 \times L_{wire}$) for carriers in x (up panel) and y (down panel) ellipsoids.

and SiO_2. Taking into consideration the value of the energy of the bottom of the lowest energy miniband, we consider the band bending could be considered as a second order correction to our results.

Turning back to the gaps in the minibands of carriers in x- and y-oriented ellipsoids, we thought it would be interesting to discover their amplitude in structures of other sizes. We set $L_{wire} = L_{sc}/2$ with the aim of obtaining a unique parameter for the study. In Fig. 4.8 the energy miniband gaps are represented as a function of L_{wire} for carriers in x and y ellipsoids. The similarities between the gaps found for carriers in the x- and y-oriented ellipsoids could be caused by the fact that the confinement in this structure is equivalent in the x and y directions (the difference being merely a rotation of 90° and a mirror symmetry with respect to the plane $z = L_{sc}/2$). The trend observed in Fig. 4.8 is reasonable, since increasing the wire and cell sizes greatly weakens the confinement. Thus, the miniband gaps tend to disappear.

4.4.1.3 Optical absorption.

Finally, we evaluated the absorption coefficient for two different light polarizations and two different levels of doping of the silicon wires and plotted it in Figs. 4.9 and 4.10. With regard to the former, we carried out calculations changing the light polarization in order to analyze the dependence of the absorption coef-

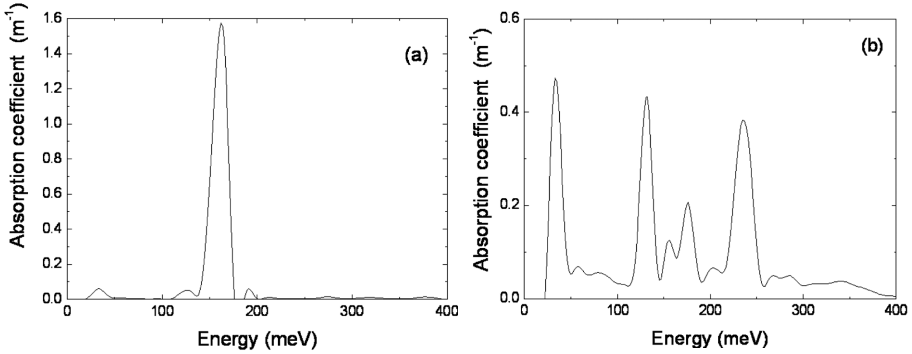


Figure 4.9: Optical absorption coefficients *vs* photon energy for (a) undoped silicon and light polarization in the x direction and (b) undoped silicon and light polarization in the z direction. Sizes are L_{sc}=4 nm and L_{wire}=2 nm.

ficient on the particular spatial arrangement of the materials in these structures. The existence of a strong absorption peak for polarization in the x direction, related to the gap between the first and second minibands is noticeable, while for polarization in the z direction, a set of peaks is observable, this being caused by the non-existence of a dominant gap. It is interesting that light polarization in the x direction seems to be unaffected by the non-existence of gaps in the z ellipsoids, even though carriers in minibands arising from z-oriented ellipsoids could a priori take part in the absorption too. It can be related with the strong selection rules that can be found in these systems. A deeper study on these selection rules are presented in Sec. 4.4.2.2.

Concerning the peak observed in light polarized in the x direction, this is found at an energy greater than the gap value and is caused by the way the absorption is carried out in the Q-space, i.e., vertical transitions. In Fig. 4.6 the energy difference between the first and second minibands for vertical transitions is 150 meV, corresponding with Fig. 4.9 Similarly, we would expect to find peaks in the absorption coefficient for energies greater than the band gap in nanostructures of other sizes, corresponding to the values in Fig. 4.8.

Regarding the doping level, (4.13) reports a crucial relation between the absorption coefficient and the level of occupancy of the minibands. Absorption can be greatly increased by means of donor impurities, doping in such a way that the Fermi energy would be placed between the first and second minibands, thus populating the lowest miniband. Nevertheless, for such a doping level other

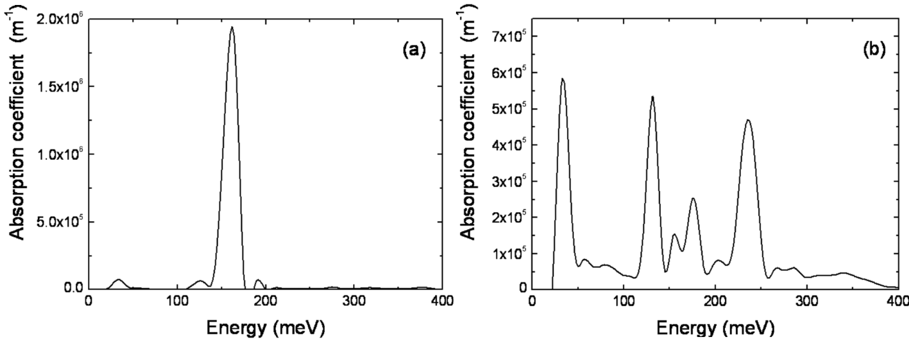


Figure 4.10: Optical absorption coefficients *vs* photon energy for (a) doped silicon and light polarization in the x direction and (b) doped silicon and light polarization in the z direction. Sizes are L_{sc}=4 nm and L_{wire}=2 nm.

effects due to impurities could arise in the absorption process. Thus, we placed the Fermi level 200 meV below the bulk conduction band, corresponding to a moderate doping level.

Figure 4.10 shows the results obtained. These results seem to be exactly proportional to those plotted in Fig. 4.9 for both light polarizations but are greater by several orders of magnitude. Understanding this proportionality is not straightforward, since in (4.13) the $f(E)$ functions are integrated in the calculation. Nevertheless, this could be explained by taking into account the fact that this moderate doping does not introduce degeneration in the semiconductor, thus $f(E) \approx e^{\frac{E_F - E}{k_B T}}$ and $(1 - f(E)) \approx 1$. Taking the factor $e^{E_F/k_B T}$ outside of the integral would explain the proportionality between Figs. 4.9 and 4.10. Roughly speaking, the proportionality constant is $e^{\Delta E_F/k_B T}$, which could be related to the difference in the Fermi levels in the two figures, ΔE_F. With the values used, we obtain a proportional constant of $e^{\Delta E_F/k_B T} \approx 1.2 \times 10^6$, in accordance with the data reported in Figs. 4.9 and 4.10.

4.4.2 3-D structures. Quantum dots.

In this section we study regimented InAs QDs repeated along the three spatial dimensions and embedded in a GaAs matrix. We focus on nanostructures with cuboid shapes, hence we modify the aspect ratio of these cuboids, volume, and the separation between QDs. The miniband structure is computed in order to be able to evaluate the absorption coefficient for different QD and light

polarizations. We used m_{InAs}=0.023m_0 (obtained from the Pikus-Bir 8×8 $\vec{k}\cdot\vec{p}$ Hamiltonian) and m_{GaAs}=0.063m_0. We have divided the results into two groups in order to clarify the study. In a first study, we have taken into account four QD arrays in the study of the miniband structure and optical absorption: array L_{qd}/L_{sc}=5/10, L_{qd}/L_{sc}=4/8, L_{qd}/L_{sc}=3/6, and L_{qd}/L_{sc}=8/10. Three of them have a fixed ratio between QD and *supercell* of L_{qd}/L_{sc}=0.5 and the total volume is changed. The L_{qd}/L_{sc}=5/10 and L_{qd}/L_{sc}=8/10 are used to check the impact of the dot size on the miniband structure and absorption coefficient when the *supercell* length is fixed. In a second study, we focus on the effects of the shape and volume of the QDs [105]. There, we have grouped the samples into three different sets. A set corresponds with a group of QDs with a particular volume (128 nm^3, 250 nm^3, and 432 nm^3). Within each set, the shape of the QD is modified, changing the aspect ratio between the base and the height. The three samples considered in each set have the shapes of: i) elongated cuboid (L_x=L_y=L_z/2), ii) regular cube (L_x=L_y=L_z), and iii) flattened cuboid (L_x=L_y=4L_z). A sketch of these structures can be found in Fig. 4.2. Neighboring dots are separated by a 3 nm GaAs barrier for every case.

4.4.2.1 Miniband structure.

The miniband structures for the samples: L_{qd}/L_{sc}=5/10, L_{qd}/L_{sc}=4/8, L_{qd}/L_{sc}=3/6, and L_{qd}/L_{sc}=8/10, are depicted in Fig. 4.4. An indirect miniband gap is observed in most of the cases. The maximum of the lowest miniband is placed at the A point, while the minimum of the second miniband is at the X point. However, Fig. 4.4d shows a direct miniband gap at the A point that might be caused by the different ratio between QD and matrix volumes. However, the importance of indirect or direct miniband gaps in these structures is not as great as in bulk semiconductors. The width of the lowest minibands is of the order of 100 meV, and for practical purposes the carriers could be considered to populate the whole miniband, not just the miniband extrema. Furthermore, optical transitions are vertical in the Q-space and the photon energies for direct and indirect absorption have roughly the same values due to the flatness of the minibands compared to bulk bands.

Several parameters can influence the miniband structure of the array of dots. An interesting issue is QD density. For example, with dots of the same

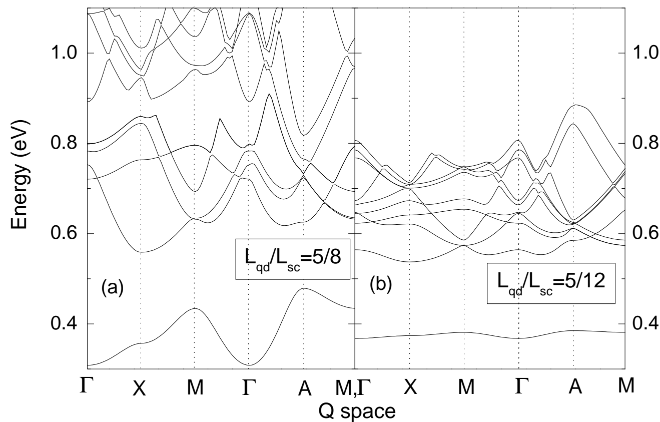


Figure 4.11: Comparison between miniband structures of cubic dots of 5 nm side length in *supercells* of (a) 8 nm (L_{qd}/L_{sc}=5/8) and (b) 12 nm (L_{qd}/L_{sc}=5/12) respectively. The ten lowest energy minibands are represented.

size it is possible to have different dot densities. This basically consists in changing the thickness of the barriers between dots. In Fig. 4.11 we compare the results of cubic dots of a 5 nm side length in *supercells* of (a) 8 nm (L_{qd}/L_{sc}=5/8) and (b) 12 nm (L_{qd}/L_{sc}=5/12). Several differences are noticeable. For example, a significant increase of the miniband amplitudes is observed in the first case because of the stronger dot coupling. This effect also causes a reduction in the electrical bandgap for high-density profiles. This quantity ranges from 79.6 meV in the first case to 152.3 meV in the second.

The results are in agreement with that one expects for carrier transport in such systems. Miniband width is a very interesting issue for investigating this fact. Stronger dot couplings provide lighter carriers because due to their greater miniband curvatures, they could be removed more easily than in structures with more isolation between the dots, where the minibands are flattener. This might be relevant in optoelectronic applications.

We also studied the influence of dot size, keeping the same *supercell*. Figure 4.12 shows the results for QDs having (a) an 8 nm side length (L_{qd}/L_{sc}=8/10) and (b) a 2 nm side length (L_{qd}/L_{sc}=2/10). The *supercell* had a 10 nm

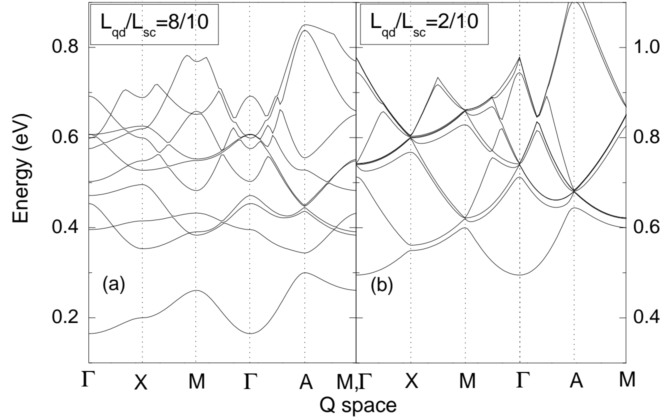


Figure 4.12: Comparison between miniband structures of cubic dots of (a) 8 nm side length (L_{qd}/L_{sc}=8/10) and (b) 2 nm side length (L_{qd}/L_{sc}=2/10). The *supercells* had 10nm side length in both cases. The ten lowest energy minibands are represented.

side length in both cases. It is worth noting the existence of a miniband gap in the first case, while in the second case the minibands overlap. This can be explained paying attention to the dimensions of the QD in relation with the *supercell* size. Large dots with small interdot distances still retain the character of a periodic nanostructure, the *supercell* is practically occupied by the QD. However, coupling between small dots with large interdot distances is negligible. The *supercell* behaves like the matrix material. Therefore, the miniband structure resembles a continuum of states and the lowest energy in such systems is close to the energy of the conduction band offset of strained InAs/GaAs. Quantum dots are not important in this structure, representing less than 1% of the total volume of the *supercell*. In summary, a compromise between QD size and interdots separation should be achieved in order to retain the quantum effects. Otherwise, if the L_{qd}/L_{sc} ratio is close to 0 or 1, the nanostructure tends to behave like the bulk material or QD material, respectively.

Finally, the influence of the QD shape is studied. The miniband structures for the elongated, regular and flattened cuboids are depicted in Fig. 4.13 together

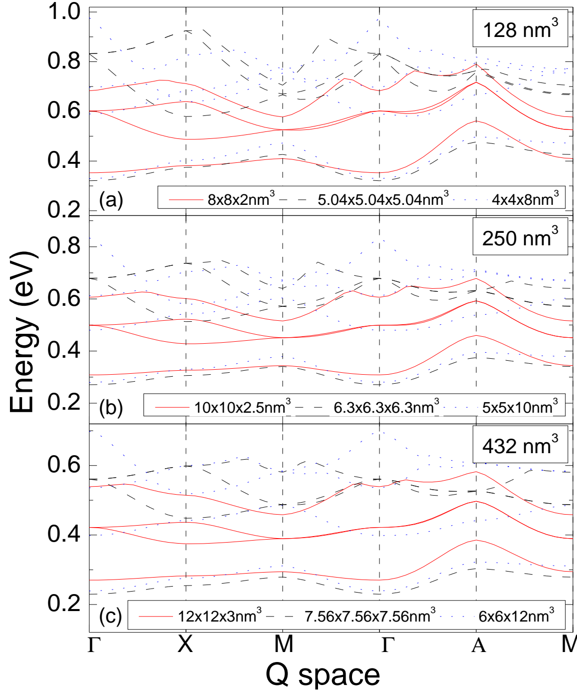


Figure 4.13: Miniband structures for the quantum dots with different shapes and sizes. Flattened cuboids (solid lines), regular cubes (dashed lines), and elongated cuboids (dotted lines). The legend for each line indicates the quantum dot width in each spatial direction ($L_{qd,x}$, $L_{qd,y}$, and $L_{qd,z}$ respectively) The samples are grouped in sets with the same volume: a) 128 nm^3, b) 250 nm^3, and c) 432nm^3. In every case, a separation of 3 nm between quantum dots has been considered in each spatial direction.

within each figure. All the samples within a set show a similar lowest miniband. The difference in this first miniband at the Γ point is in the range of 0.32-0.35 eV for the 128 nm^3, 0.27-0.30 eV for the 250 nm^3, and 0.24-0.27 eV for the 432 nm^3 case. It can be seen that the level of the lowest miniband goes up as the volume of the QD shrinks. This is due to a higher confinement, i.e. the electrons are more limited in space inside the QD as the size of the QD decreases. A similar trend is also observed within each set for the three different samples. Around the Γ point, the lowest energy for the first miniband is obtained when the QD has a cubic shape, regardless of the size of the set. The following higher energy

is for an elongated shape of the QD which has lower L_x and L_y dimensions than those of the regular cube, and the higher energy is for the flattened cuboid in which the L_z dimension achieves the lowest value for a certain set. At the Γ point in the Q-space, the solution to the Schrödinger equation depends only on the dimensions of the *supercell*. At this point the three spatial components (L_x, L_y, L_z) have the same influence and a reduction in one of them produces an increase in the confinement level.

A change in the shape of the QD has a strong influence on the shape of the band structure in the upper minibands for a particular set. The first thing to be noticed is the break in the degeneration when the QD is not perfectly cubic. This effect can be easily observed at the Γ point, where, in the case of the regular cube, three minibands converge in a single point. For the other two cases, i.e. elongated and flattened cuboids, the confinement is lower in at least one of the three spatial components. This can give rise to minibands being closer to each other and therefore the energy levels of the upper minibands are lower than those for the regular cube. Moreover, the trend in the miniband structure with regard to shape is practically the same for each set. A change in the volume implies a bigger or smaller spreading of energy but the shape of the minibands is the same.

Finally, these results on minibands suggest that intermediate band solar cells [84] could be developed in ordered QD systems, as indicated by other researchers [81]. Wide intermediate bands and large miniband gaps could be obtained by tuning the density and dot size. In our investigation, the case with QDs being 25% of the total volume of the *supercell* seems to be closer to this behavior. However, the materials studied do not provide the values needed for the energy gaps [106] and other alternatives would have to be explored for this kind of application.

4.4.2.2 Optical absorption.

This section aims to gain an insight into the absorption processes between minibands belonging to the conduction band in QDs. To tackle this issue, we start by analyzing, step by step, the parameters involved in the calculation of the absorption coefficient. We use the samples with different shapes to carry out this study. The first quantity that we analyze is the distance between the first and second minibands at each point of the Q-space. In light absorption this

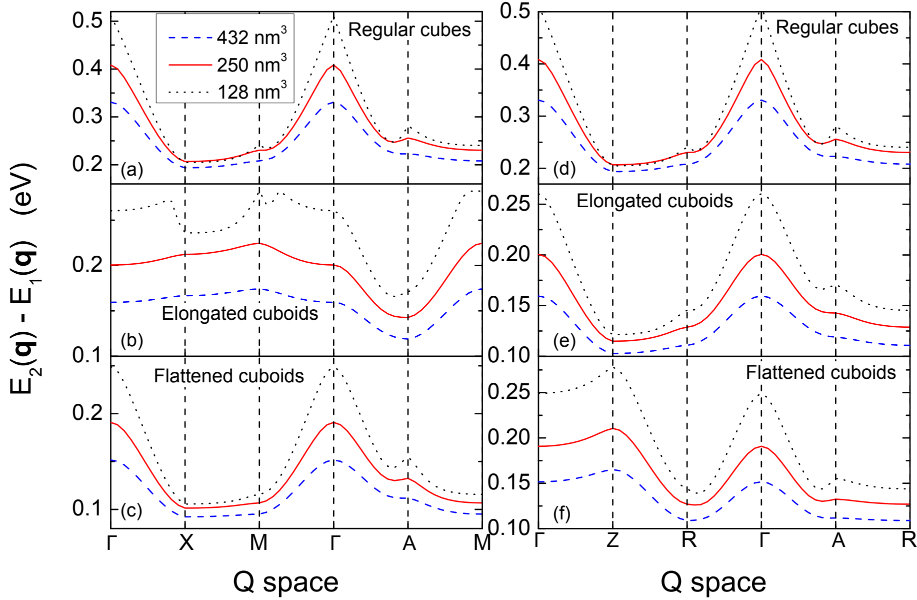


Figure 4.14: Difference between the energy of the second and the first miniband along the Q-space following the points Γ, X, M, A, Γ, Z, R, and A depicted in Fig. 4.2. The results have been grouped by shape: a) and d) regular cubes, b) and e) elongated cuboids, and c) and f) flattened cuboids.

is the photon energy involved in the process. Considering as a rough approximation that practically all the transitions are taking place between the first and the second miniband and neglecting the occupancies in the minibands, the distance between these two minibands could help to gain a first insight into the threshold absorption energies and where they are produced. These distances have been depicted in Fig. 4.14 for different shapes, sizes and paths in the Q-space. Looking at the left panel on Fig. 4.14, where a specific path (Γ, X, M, and A) was followed, we observed two different behaviors: Figs. 4.14a and 4.14c share common features. For instance, the minimum distance between the minibands is observed along the path X to M, which corresponds to a face of the Brillouin zone in both regular cubes and flattened cuboids. However, the elongated cuboids (Fig. 4.14b) behave in a completely different fashion, suggesting noticeable changes when the QD volume changes. Nevertheless, the Brillouin zone for elongated cuboids has a flattened shape. In consequence, different features can be observed across different paths. The right panel in Fig. 4.14 shows

this exactly. We examined the behavior on a different path (Γ, Z, R, and A), noticing in this case that elongated cuboids behaved in the same way as regular and flattened cuboids on the first path. Further, flattened cuboids on the new path behaved differently since the Brillouin zone has different features.

Regular cubes behave in the same manner in both paths because of the symmetry. Regardless of the QD volume, the curves have flat sections of about 200-230 meV, these also being around the lowest parts of the curves. Flattened cuboids also have flat sections at about 100-140 meV. Concerning elongated cuboids, the left panel in Fig. 4.14 shows flat regions with very different energies for each QD volume. However, the curves on the path depicted in the right panel on Fig. 4.14 show flat regions at about 110-140 meV for all the volumes studied. All these details are very relevant in optical absorption as will be shown later.

A "toy model" could be useful to understand and to roughly predict the miniband gap energy, E_G, in these systems. Considering that the states in an ordered QD array come from couplings between single states of isolated QDs, we could calculate the energy difference between the ground state and the first excited state in an isolated QD of side lengths L, αL and βL ($\alpha \leq 1$ and $\beta \leq 1$) modeled using hard barriers:

$$E_G = 3\frac{\hbar^2}{2m_{dot}}\left(\frac{\pi}{L}\right)^2 \tag{4.16}$$

m_{dot} being the effective mass inside the QD. When comparing E_G of a QD with the E_G of a regular cubic QD having the same volume, the ratio between gaps is:

$$\frac{E_G}{E_{G,cube}} = (\alpha\beta)^{2/3} \tag{4.17}$$

The foregoing would be a simplified first estimation of the miniband gap energy. The coupling between neighboring QDs could change this value, and the shift would be higher when the interaction between dots increases. Despite the simplifications, the model retains important features of the physical origins of this quantity. Equation (4.17) explains several features of the calculated results: i) the miniband gap energy for regular cubes tends to be the highest when compared with other shapes and ii) in this study, elongated cuboids have α=1/2 and β=1/2 and flattened cuboids have α=1 and β=1/4. Therefore, both cases

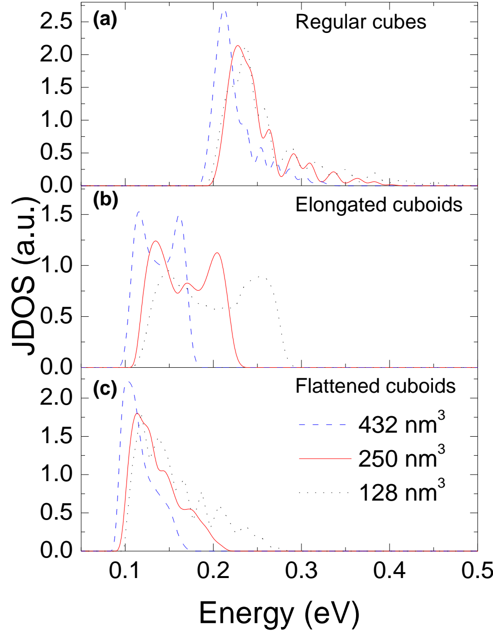


Figure 4.15: Representation of the joint-density of states (JDOS), considering the first two minibands. The results have been grouped by shape: a) regular cubes, b) elongated cuboids, and c) flattened cuboids.

provide the same result: $E_G/E_{G,cube}$ ≈0.4. This result approximately corresponds to the ratii $E_G/E_{G,cube}$ ≈0.4-0.6 between the lowest values in the curves depicted in Fig. 4.14. Finally, as we shall show, this could also explain the similarities between the threshold energy in the absorption coefficient for elongated and flattened cuboids.

In order to discover how many states are available for optical absorption, in the next step we calculated the joint density of states (JDOS). JDOS takes into account the number of available states transferring from the first to the second miniband for certain energies. This parameter is a rough simplification of the absorption coefficient, since it considers a fully occupied first miniband and an empty second one (there are further simplifications within the approach like the selection rules, but this would be the most relevant). Figure 4.15 depicts the JDOS for different sizes and shapes of QDs. A well defined shape-dependent

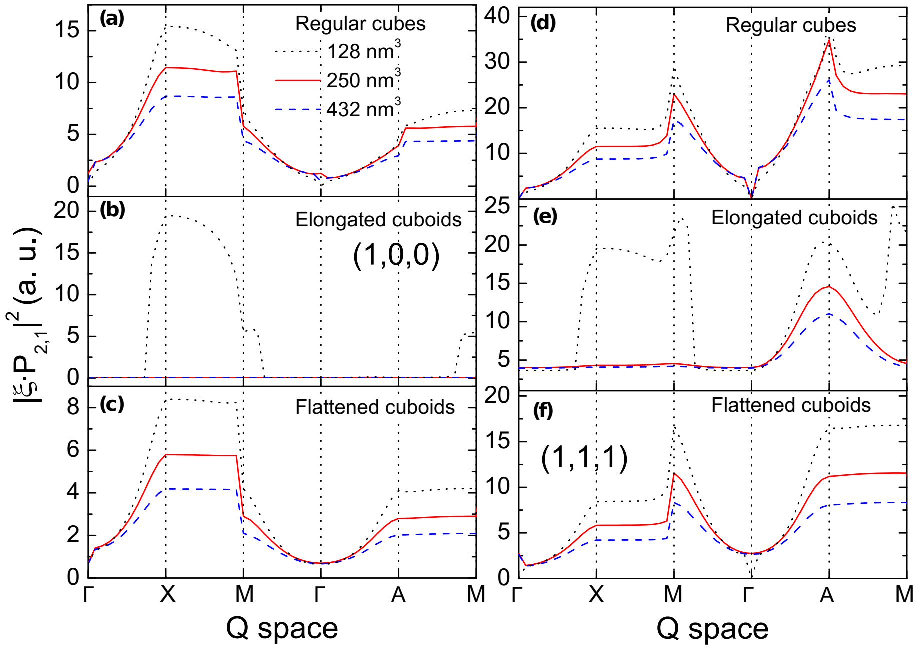


Figure 4.16: Representation of $|\hat{\xi} \cdot \vec{P}_{2,1}|^2$ for (1,0,0) light polarization (left panel) and (1,1,1) light polarization (right panel). The initial and final states in the transitions are those belonging to the first and second minibands, respectively.

threshold value is found in the JDOS representation. The threshold energy is located at approximately 80-125 meV for flattened and elongated cuboids, while regular cubes have a threshold energy of 200 meV. A change in the volume maintaining the shape of the QD gives rise to changes in the threshold energy smaller than 25 meV. It is worth noting that these values are in accordance with Fig. 4.14. As shown, those paths where the curves were flat in these figures are crucial in order to understand the threshold energy in the JDOS, suggesting that this transition energy is favored. In the particular case of elongated cuboids, there are several flat regions in the curves depicted in Fig. 4.14b and Fig. 4.14e, and the JDOS has its threshold at the lowest value (energies across Z to R and A to R, Fig. 4.14b), but there is also a peak in the JDOS curves in Fig. 4.15b in correspondence with the energies in the flat region from X to M in Fig. 4.14b.

JDOS is used in this work to understand the origins of the threshold

energy in these systems, but the absorption coefficient must take into account other effects, such as occupancy of the states and wavefunction features. Regarding the latter issue, we analyzed the effects of the term $|\ \hat{\xi} \cdot \vec{P}_{n_f,n_i}\ |^2 = |\hat{\xi} \cdot \int_{supercell} \eta^*_{\vec{q},n_f}(\vec{r}) \nabla \eta_{\vec{q},n_i}(\vec{r}) d\vec{r}|^2$ in the absorption coefficient (4.13). This is essentially related to two different quantities: light polarization, through $\vec{\xi}$, and the initial and final wavefunctions of the transition analyzed. We represented the $|\hat{\xi} \cdot \vec{P}_{2,1}|^2$ term in the same path as Fig. 4.14 across the Q-space, investigating two different light polarizations, (1,0,0) and (1,1,1), where the vectors are expressed in the reference system of Fig. 4.2. Figure 4.16 shows the results for (1,0,0) and (1,1,1) light polarizations, respectively. The influence of the wavefunctions is noticeable in the strength of the optical transitions from certain regions of the Q-space, suppressing or strengthening some transitions. Regarding regular cubes and flattened cuboids, a similar behavior is observed when the dot volume is changed: the smaller the cube, the higher the $|\hat{\xi} \cdot \vec{P}_{2,1}|^2$ term. However, there are subtle differences, since the integral in $|\hat{\xi} \cdot \vec{P}_{2,1}|^2$ depends on both the integration volume (the *supercell*) and the wavefunction derivatives. They have opposite effects in the calculation, and as a result they cancel each other out and the $|\hat{\xi} \cdot \vec{P}_{2,1}|^2$ curves remain in the same order of magnitude. We would like to emphasize the fact that optical transitions from the Γ point are almost suppressed, and transitions from points in the Q-space in the borders of the Brillouin zone are noticeably favored. With regard to elongated cuboids, we observe huge differences in the $|\hat{\xi} \cdot \vec{P}_{2,1}|^2$ parameter due to the polarization. When light is (1,0,0) polarized, $|\hat{\xi} \cdot \vec{P}_{2,1}|^2$ transitions are noticeably reduced in a large region of the Brillouin zone, according to the curves, especially for larger quantum dots, where the transition from miniband 1 to 2 is practically forbidden for that light polarization. When light is (1,1,1) polarized, the reduction is less relevant, but also important. This quenching of the absorption between these two first minibands is very relevant to the absorption coefficient, gaining more relevance transitions between first and third miniband, as we shall see.

Going a step further in complexity, we merge the JDOS and the selection rules in order to obtain a closer behavior to the absorption coefficient. Equation (4.13) indicates that the absorption coefficient is related to the integral of the $|\hat{\xi} \cdot \vec{P}_{n_f,n_i}|^2$ curves in the Q-space. Therefore, we defined a simplified version of

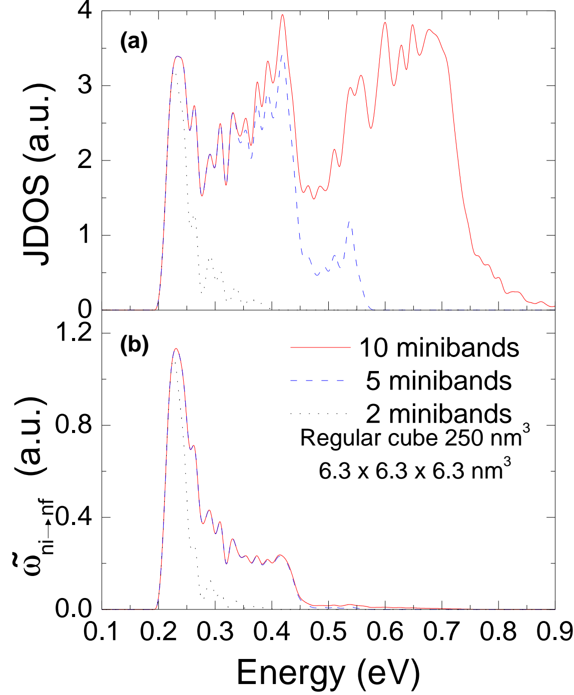


Figure 4.17: Comparison between the possible energy transitions for a regular cube of 250 nm^3 obtained by means of the a) JDOS and b) $\tilde{w}_{n_i \to n_f}(\hbar\omega_{op})$ when 2, 5, and 10 minibands are considered in the calculations. $\tilde{w}_{n_i \to n_f}(\hbar\omega_{op})$ is computed considering light polarization in the (1,0,0) direction.

the $w_{n_i \to n_f}(\hbar\omega_{op})$ curves as follows:

$$\tilde{w}_{n_i \to n_f}(\hbar\omega_{op}) = \int_{Q-space} |\hat{\xi} \cdot \vec{P}_{n_f,n_i}|^2 \delta(E_{n_f} - E_{n_i} - \hbar\omega_{op})\rho_Q d\vec{q} \qquad (4.18)$$

These functions consider the $|\hat{\xi} \cdot \vec{P}_{n_f,n_i}|^2$ term on all the paths in the Brillouin zone, thus giving a more precise picture of the transition process. We calculated the addition of $\tilde{w}_{n_i \to n_f}(\hbar\omega_{op})$ for several transitions, all starting from the lowest miniband, and compared them with the addition of JDOS for several transitions, all of these also starting from the lowest miniband.

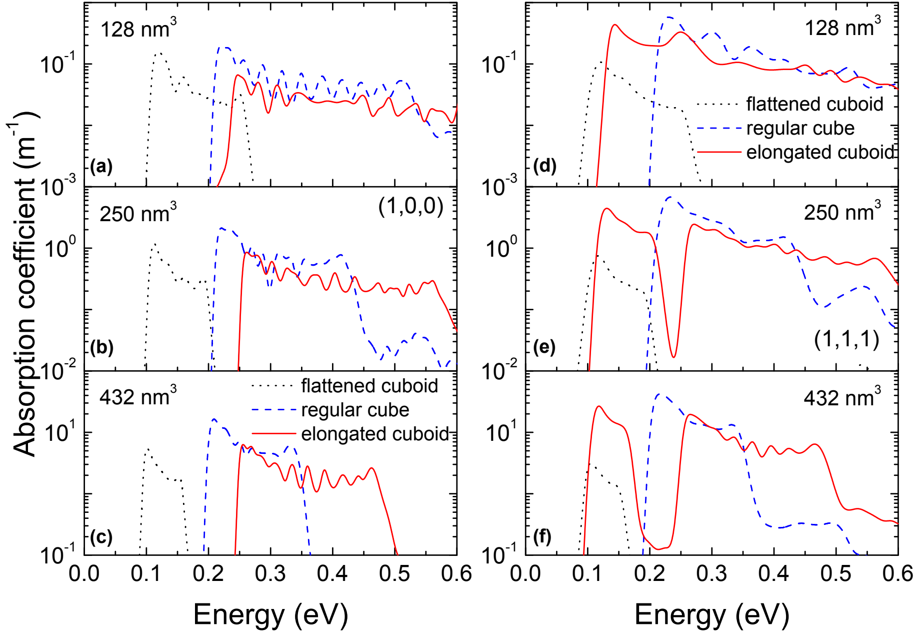


Figure 4.18: Absorption coefficient for nine different samples for light polarization in the (1,0,0) direction (left panel) and light polarization in the (1,1,1) direction (right panel). Fermi energy was placed at the midgap of the quantum dot material. The results are grouped by volume: a) and d) 128 nm3, b) and e) 250 nm3, and c) and f) 432 nm^3.

The curves are depicted in Fig. 4.17. The purpose of this evaluation is to compare these curves and to determine the influence of the $|\hat{\xi} \cdot \vec{P}_{n_f,n_i}|^2$ terms on the transitions between minibands, since these curves would be proportional if $|\hat{\xi} \cdot \vec{P}_{n_f,n_i}|^2$ were of the same order of magnitude for every transition. It is noticeable that JDOS and $\tilde{w}_{1\to 2}(\hbar\omega_{op})$ for 250 nm^3 regular cubes share similar features, being almost proportional. When we include more minibands in the calculation, big differences between JDOS and $\tilde{w}_{n_i \to n_f}(\hbar\omega_{op})$ appear. This clearly suggests an important suppression of transitions between the lowest and high-energy minibands because of the wavefunction features. Five minibands would apparently be enough to study the absorption coefficient in these systems, since transitions to higher minibands are quenched and the existence of a selection rule implicit in this calculation is perceived.

Finally the absorption coefficient is obtained. In every case, we have considered an intrinsic doping level for the materials which form the QDs. Thus, the Fermi level is positioned at the midgap of the QD material. Fig. 4.18 shows the absorption coefficient grouped by sets of QDs with equal volume for (1,0,0) and (1,1,1) light polarizations. Once again, it is shown that a clear threshold value is found for each shape of the QDs. This is practically independent of the volume and is determined by the shape. In the left panel of Fig. 4.18 the smallest threshold value is obtained for the case of flattened cuboids, in agreement with the results of Figs. 4.14c and 4.14f. Threshold values of about 200 meV are found for regular cubes, in good agreement with Figs. 4.14a and 4.14d. Elongated cuboids have threshold values of about 250 meV, in disagreement with Figs. 4.14b and 4.14e. A deeper investigation will clarify this fact. Analyzing the results in Fig. 4.18 now, for (1,1,1) light polarization, flattened and regular cubes maintain the same features and threshold values, the reasons giving rise to this behavior having already been clarified. Interestingly, 250 nm^3 and 432 nm^3 elongated cuboids have a "double threshold": the absorption curves seem to be constituted by the (1,0,0) absorption coefficient curve, but adding a new curve with a threshold at about 100 meV, which is in accordance with Fig. 4.14e. A deep analysis of the results reveals the influence of the different transitions: transitions between the lowest and second minibands with (1,0,0) light polarization are forbidden, therefore the threshold is due to transitions from the lowest and the third miniband. (1,1,1) light polarization leaves the opportunity for transitions between the lowest and second miniband, thus modifying dramatically the absorption threshold. The smallest elongated cuboidal QDs also behave in the same manner, but the (1,1,1) threshold curve overlaps the (1,0,0) curve. A second absorption hump in Fig. 4.14d around 250 meV confirms this. In order to investigate the details of the quenching found in elongated cuboids in (1,0,0) light polarization, Fig. 4.19 depicts $|\hat{\xi} \cdot \vec{P}_{3,1}|^2$ across a path in the Q-space with (1,0,0) light polarization together with the JDOS for the first and third miniband. Comparison of the values of $|\hat{\xi} \cdot \vec{P}_{3,1}|^2$ and $|\hat{\xi} \cdot \vec{P}_{2,1}|^2$ in Fig. 4.14b, and comparison of the elongated cuboid JDOS threshold in Fig. 4.19b and Fig. 4.18 finally evidences the importance of selection rules in intraband optical absorption in minibands for regimented QD nanostructures.

Moreover, it is worth noting that the values in the absorption coefficient

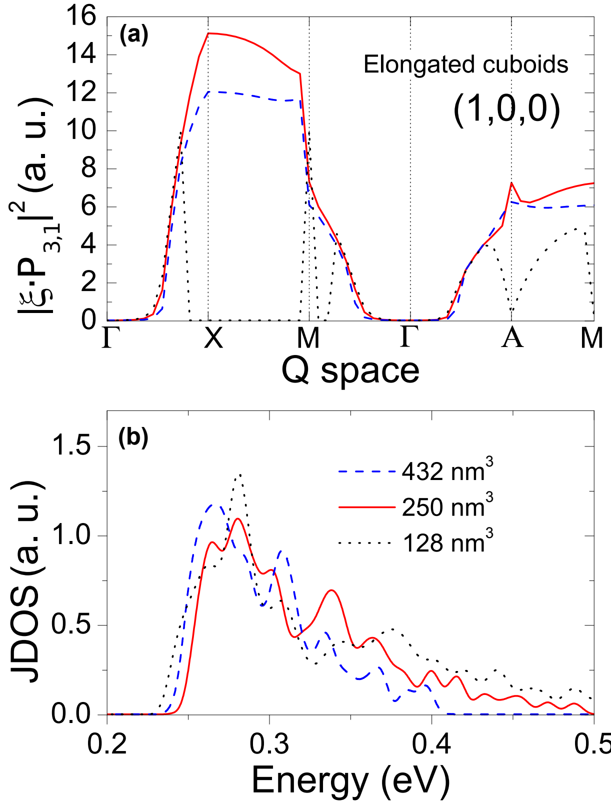


Figure 4.19: a) $|\hat{\xi} \cdot \vec{P}_{3,1}|^2$ across a path in the Q-space with (1,0,0) light polarization and b) joint-density of states (JDOS) representations. In both cases, those belonging to the first and third minibands have been considered as initial and final states.

depicted in Fig. 4.18 are obtained for intrinsic semiconductors. The right values could be obtained by multiplying by $e^{\frac{\Delta E_F}{k_B T}}$ $(\Delta E_F = E_{F,doped} - E_{F,undoped})$ when moderately doped semiconductors are considered.

The previous study has taken into account the effect of varying the shape and volume of the QD but keeping constant the size of the barrier. Now, we investigate the impact of changing the volumen of cubic QD and the size of the barrier on the absorption coefficient. The following analysis of absorption coefficients is performed on three different arrays that were investigated previously to obtain their miniband structures: array L_{qd}/L_{sc}=3/6, L_{qd}/L_{sc}=4/8,

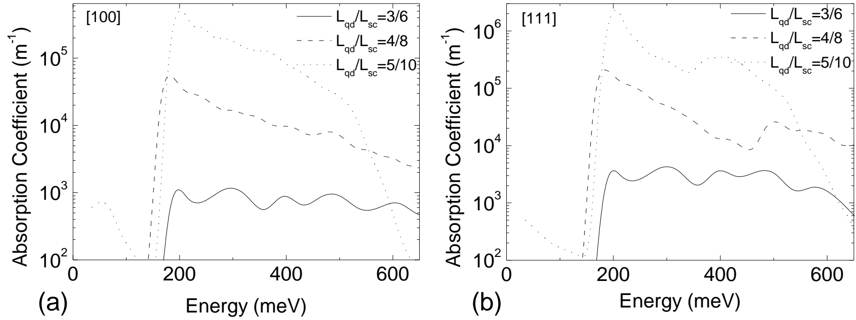


Figure 4.20: Absorption coefficient for three different arrays for light polarization in the (a) (1,0,0) and (b) (1,1,1) direction. Fermi energy was placed at the bottom of the conduction band in the quantum dot.

and L_{qd}/L_{sc}=5/10. Here, the ratio between QD and *supercell* lengths is fixed to L_{qd}/L_{sc}=0.5 and the total volume is changed. The absorption coefficients for these arrays are shown in Figs. 4.20a and 4.20b for light polarization in the (1,0,0) and (1,1,1) directions, respectively. The results correspond to optical transitions between the ten lowest energy minibands. We observed the existence of thresholds for photon absorption, determined by the miniband structure of the system. For the studied cases, these thresholds are approximately energies corresponding to far infrared ($\approx$ 200 meV). It is well noticeable that thresholds are almost independent of the light polarization. For the arrays studied, the results provide a greater absorption coefficient for larger dots and greater interdot separations. The reason for this behavior might be the lesser width of the lowest energy miniband when decreasing the dot coupling with neighbors, providing an almost constant energy level spread over about 20–30 meV and enhancing the absorption for certain photon energies. On the other hand, array L_{qd}/L_{sc}=3/6 has the highest energy miniband spread, about 100 meV (see Fig. 4.4c), and therefore there are many photon energies able to pump carriers from the first to the second miniband, thus decreasing absorption at the threshold.

For the sake of clarity, Fig. 4.21 shows the JDOS of the arrays using the two lowest energy minibands, i.e., the most populated ones. The x-axis represents the difference of energies between minibands corresponding to the energy of the absorbed photon. Here we can clearly notice that referred to above: there is a threshold about the same energy in the three arrays because they have most

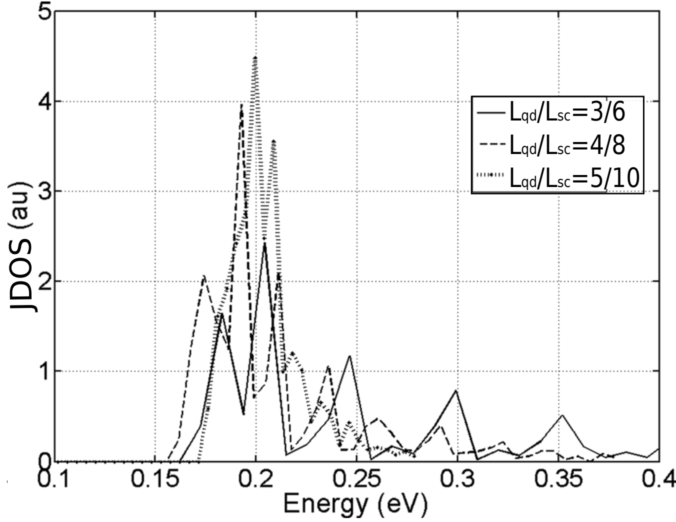


Figure 4.21: Joint density of states for the three different arrays. In the calculation we only used the two lowest energy minibands.

of the states about the same energy difference between these two minibands. Neglecting the oscillations in the curves, it is observed that the three curves are about the same order of magnitude (data are in arbitrary units, but the values are comparable). In this manner the threshold would be explained.

Regarding the progressive enhancement in the photon absorption with the *supercell* volume, it might be caused by the difference between the Fermi energy and those states having optical absorptions between the two lowest energy minibands involving photon energies in the observed threshold. In fact, having the same placement of the Fermi energy level (located at zero energy) for the three investigated arrays is in coherence with this behavior: optical absorptions between the two lowest energy minibands in array $L_{qd}/L_{sc} = 3/6$ (Fig. 4.4c) involving photons having energies about the thresholds would take place in regions of the Q-space close to the X and M points.Since states about the X point have energies below those about the M point, the first ones would be the most populated. There is an energy difference of about 0.55 eV between states close to the X point and the Fermi energy level. Regarding array $L_{qd}/L_{sc} = 5/10$ (Fig. 4.4a) optical absorptions from the X point would be also produced by photons having energies about the threshold. There is an energy difference of about 0.35

eV between these states and the Fermi level. As a consequence, the states of interest in array $L_{qd}/L_{sc} = 3/6$ are about 200 meV further from the Fermi energy level than in array $L_{qd}/L_{sc} = 5/10$. The reasons explained above can justify a difference of $\approx 10^3$ in the curves caused by the different distances between Fermi energies and the states of interest $\Delta E_F \approx 200$ meV, as noticed. Therefore, the observed trend of the absorption profiles is qualitatively explained.

Regarding polarization, photon absorption with light polarization in the (1,1,1) direction is more intense. For the transitions studied, there is a "hump" in this case in arrays $L_{qd}/L_{sc} = 3/6$ and $L_{qd}/L_{sc} = 4/8$, the opposite of the behavior is observed in Fig. 4.20a where a decreasing monotonous trend is shown. It is difficult to find a simple explanation for this hump, since it depends on the integral $\int_{supercell} \eta^*_{\vec{q},n_f}(\vec{r})\nabla\eta_{\vec{q},n_i}(\vec{r})d\vec{r}$ which gives rise to a three-dimensional vector energy dependent for a selected transition. The differences between the absorption coefficients for different light polarizations suggest a very anisotropic result of the integral.

5

Conclusions and future work

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In this thesis, different tools have been presented for simulating micro- and nano-devices. The application of these tools to different topic have been structured in three chapters.

5.1 Leakage currents in strained SiGe/Si heterojunctions

In chapter 2, a study of the impact of the Ge content and the recess depth on the leakage current through strained $Si_{1-x}Ge_x/Si$ heterojunctions has been presented. A commercial process simulator (Tsuprem4) and a commercial device simulator (Medici) have been employed to carry out this study. The lifetime has been identified as the variable that affects the leakage current the most. A model that relates changes in the lifetimes as a function of Ge content and recess depth by means of the stress levels is presented. The need of including such a model is addressed in this chapter in order to reproduce the experimental data. Unfortunately, this model is not included in the simulator. Therefore, the incorporation of such effects have to be manually added to the simulator *a posteriori*. A Ge content lower than 40% is advisable in the compromise of achieving simultaneously high drive currents and low leakage currents. The results suggest the creation of bulk defects in the Si substrate close to the heterointerface due to the stress levels as the main factor that explains the increase in the leakage current. In this regard, the identification and characterization of such traps would help to shed light on the understanding of the device performance.

5.2 Simulation of multigate transistors: Applications on the G4FET

In chapter 3, we have focused on this characterization process by means of reproducing low-frequency noise measurements. We have proposed noise models for being applied to the G4FET that takes into account both volume and surface effects. A 2-D numerical simulator that solves self-consistently Poisson and drift-diffusion equations developed by us has been chosen in order to incorporate

the models which compute the drain-current noise spectral density. Different components of the noise signal have been studied: generation-recombination noise due to the presence of traps in the depletion regions of the device and 1/f flicker noise due to traps located at the Si-SiO_2 interfaces. There are voltage ranges where one of these sources clearly dominates and other ranges where a combination of the two sources is present and makes it difficult to interpret experimental results. In this thesis, we have proposed models that reproduce the experiments and confirm the different origins of the noise. It has been tested in different operating modes of the transistor and gives an explanation of the experimental measurements carried out by other authors.

The reproduction of the noise and the current-voltage response of the G4FET has allowed us to identify and characterize the traps present in this device. The results suggest that more than one trap should be considered in the calculation in order to obtain a good agreement between experimental and simulated data. However, some discrepancies were found in the fitting process which aim to the need of considering second order effects.

One of these discrepancies can be found in the slope of the flicker noise. Experimental results showed that a $1/f^{\alpha}$ flicker noise model with variable frequency slope $\alpha \neq 1$ should be considered in order to reproduce the noise due to traps within the oxides. This model is based on gradients in the gate oxide trap density and was applied to different transistors. The model is applicable also to isolated-gate FETs with high-κ double-dielectric gate stacks. Results suggest that an exponential distribution as a function of the depth from the Si-SiO_2 interface corresponds with better correlations between experimental and simulated flicker noise spectra. On the contrary, not all the samples showed a dependence of the trap distribution with the gate voltage, which implies that the band bending parameter can be neglected for these samples.

The usefulness of the g-r model lies in the possibility of calculating the local noise contribution in any part of the device in order to locate those regions that contribute higher noise, and thus, estimate the applied voltages that will minimize the total noise in these devices. We have implemented also variations of metallurgical boundaries of the junction gates in our facet simulator for the channel cross-section, which allowed identifying that the junction gate has to penetrate under the MOS gate in order to improve the performance of the G4FET, lowering the subthreshold swing and the low-frequency noise. The im-

provement is due to a reduction of the depletion volume, lowering the number of g-r centers, which are not favorable for G4FET, because the g-r centers increase the leakage, subthreshold slope and low-frequency noise with Lorentzian shape of the spectrum in G4FET.

The influence of trap parameters on the total noise was studied. In this thesis, we found operating regions in the G4FET where the corner-frequency of the Lorentzian spectra, originated by volume deep centers, changed with gate voltage. This result contradicts the classical assumption that no variation of the corner-frequency occurs in Lorentzians related to a given trap level in the depletion layer of an MOS transistor. This is explained mainly by the fact that a bipolar structure (a p-n junction) is added to a unipolar device (a MOS transistor). However, similar conclusions have been also obtained for other transistors. A study of g-r noise produced by bulk traps in FD SOI MOSFETs has been made. The most remarkable result is that the characteristic time associated to a trap depends on the applied gate voltage, unlike g-r noise produced by traps in the depletion region of bulk and partially depleted SOI MOSFETs. This behavior of the characteristic time leads to specific variations of the corner-frequency and plateau value of the g-r spectra as a function of the gate voltage. This specific variation with gate voltage allows for the characterization of traps in FD SOI MOSFETs and may in principle be extended to 3D fin-type transistors. In particular, structures with two different approaches to fabricate the source and drain regions have been analyzed in this thesis. At the same time, characterization problems associated to the presence of more than one trap or traps with different energy levels have been solved satisfactorily. As an important point for future consideration is the possibility of carrying out a full spectroscopic characterization in FD SOI MOSFETs just varying the voltages of its two gates. This fact is due to the reduced dimension of the transistor in order to obtain the FD condition. However, working with nanometric dimensions might imply to deal with quantum effects.

5.3 Miniband structure and optical absorption

In chapter 4, we focus on another topic which implies to use other simulation tools to cope with quantum effects. There, we investigated the solution of the Schrödinger equation for periodic regimented nanostructures employing a sim-

ulator developed by us which considers different effective masses for quantum dot and barrier material. Our aim was to study the photon absorption by electrons belonging to the conduction band in such systems. We have presented our results on miniband structures for two different nanostructures: quantum dots and quantum wires. Several parameter of the nanostructures were changed in order to check their effects on the optical absorption: sizes, shapes, light polarization, doping level, and for several interdot distances. Observing the presence of miniband gaps due to quantization which could be useful in optoelectronic applications. In that way, we have presented results that shed light on the physics of these systems.

Regarding computational implementation, we have shown data on convergence of the calculations of confinement and have explored the conditions for obtaining suitable values. Our results were compared with those obtained from a 3-D Kronig-Penney model with different effective masses in the dot and the barriers, as reported by previous authors, proving that this analytical approach may be useful only for cases where barriers are noticeably smaller than quantum dots, but inadequate for investigating the general case, where our description would be more accurate.

Finally, we carried out calculations on the absorption coefficient by electrons in doped and undoped semiconductors and for light polarizations in two different orientations. The results suggest the existence of well-defined energies where photons are absorbed for certain light polarizations, determined by the miniband structure of the systems.

Regarding quantum wires, for the cases studied, with the indicated Fermi energy levels, these thresholds are about 200 meV and are almost independent of the light polarization. Greater absorption coefficients for larger dots and greater interdot separations were calculated. We attribute this behavior to the particular miniband structures obtained for each case and their relative distances to the Fermi energy level. Regarding polarization, photon absorption with light polarization in the [111] direction is more intense.

Our theoretical investigation suggests that these systems could be useful in optoelectronic applications because of their absorption coefficient and also the possibility of removing the carriers after photon absorption through the second miniband of the structure. Carrier transport along the minibands is possible, in contrast with photon absorption by single impurities or single dots.

Thus, these systems could be useful for manufacturing quantum dot infrared photodetectors (QDIPs). Further, we believe that this type of structure could play an important role in designing intermediate band solar cells. It would be important to achieve the periodic arrangement of the dots in order to obtain the miniband structure and to investigate the implications of using different materials in the dot and matrix, in order to find the absorption thresholds of interest for these applications.

Regarding quantum dots, we have calculated the absorption coefficient in arrays of InAs quantum dots embedded in GaAs and found thresholds at about 100 meV, 200 meV and 250 meV, depending mainly on the dot shape and light polarization, and depending slightly on the quantum dot volume. These thresholds are in the far infrared region and could be useful for the future development of detectors in that region of the electromagnetic spectrum. We propose to use our results to characterize the manufactured samples in order to determine the best quality for the arrangement and the best quality for the shapes obtained. Further, it has been shown that the absorption coefficient has a threshold independent of the quantum dot volume in the range 128 nm^3 – 432 nm^3. In consequence, we suggest that the conditions to achieve a certain threshold might merely be based on achieving the regimentation and the right shape of the quantum dots in certain regions of the sample (like a polycrystalline material). Changes in quantum dot size along the sample could not influence the threshold, as shown in the results. In conclusion, the same threshold would be found for perfect 3-D lattices and for “polycrystalline” 3-D lattices with changes in quantum dot volumes between points of the same sample. Studies on the influence of non-cuboid shapes in arrangements of quantum dots are still open, and this will be the topic of future research. Further, studies on two-dimensional arrays would also be of interest.

Resumen

En esta tesis se han presentado diferentes herramientas para la simulación de micro y nano dispositivos. La aplicación de dichas herramientas se ha dividido en tres capítulos donde se trata en cada uno de ellos un diferente tema de interés en el campo de la electrónica.

El primer tema de interés se presenta en el capítulo 2 donde se realiza un estudio de la influencia del contenido de Ge y de la profundidad de grabado sobre las corrientes de perdidas en heterouniones estresadas de $Si_{1-x}Ge_x/Si$. Para llevar a cabo dicho estudio se ha utilizado un simulador comercial de procesos (Tsuprem4) y un simulador comercial de dispositivos (Medici). Se ha identificado a el tiempo de vida medio de los portadores como la variable que más afecta a dichas corrientes de pérdidas. Por lo que se ha presentado un modelo que directamente relaciona los cambios en los tiempos de vida media con el contenido de Ge y la profundidad de grabado por medio de los niveles de la tensión mecánica. La necesidad de incluir dicho modelo para así poder reproducir los datos experimentales se justifica en el capítulo 2. Desafortunadamente este modelo aún no se incluye en ninguna versión comercial del simulador. Por lo tanto, la incorporación de tales efectos ha de ser añadida manualmente *a posteriori* en el simulador. Tras este estudio, habría que remarcar una conclusión importante y es que se aconseja utilizar un contenido de Ge no mayor al 40% si se quiere conseguir simultáneamente una corriente de conducción alta y unas corrientes de perdidas bajas. Los resultados señalan como una posible explicación al aumento de las corrientes de pérdidas a la creación de defectos en el volumen del sustrato de Si cerca de la heterointerfaz debido a los altos niveles de tensión mecánica presentes. Respecto a esto, la identificación y caracterización de tales defectos sería de gran ayuda

para aclarar y entender mejor el funcionamiento de estos dispositivos.

Con respecto al segundo tema ubicado en el capítulo 3 sobre el proceso de caracterización de trampas por medio de la simulación y reproducción de las medidas de ruido de baja frecuencia, varios modelos de ruido se han propuesto para ser aplicados a un G4FET los cuales tienen en cuenta los efectos superficiales y de volumen. En este capítulo se ha utilizado un simulador desarrollado por nosotros que resuelve autoconsistentemente las ecuaciones de Poisson y difusión-deriva en 2-D para así incorporar los modelos de ruido y obtener la densidad de potencia espectral de la corriente de drenador. Aquí, se ha estudiado diferentes componentes de la señal de ruido: ruido generación-recombinación (g-r) debido a la presencia de defectos dentro de la zona de agotamiento del transistor y el ruido $1/f$ o ruido *flicker* el cual es debido a trampas localizadas en la interfaz Si-SiO_2.

Existen rangos de voltaje donde una de las componentes claramente predomina sobre la otra y otros rangos donde existe una combinación de dos o más componentes, complicando así el estudio experimental del ruido. En esta tesis, hemos propuesto modelos de ruido que reproducen las medidas experimentales y que confirman los diferentes orígenes del ruido. Dichos modelos han sido comprobados bajo diferentes modos de operación del transistor y han dado una explicación a las medidas experimentales llevadas a cabo por otros autores.

La simulación de la respuesta de ruido y la característica corriente-voltaje (I-V) de un transistor G4FET nos ha permitido identificar y caracterizar los defectos presentes en este dispositivo. Los resultados indican que se debería de considerar más de una trampa en las simulaciones para poder así obtener un buen ajuste entre los datos experimentales y simulados. No obstante, se encontraron algunas discrepancias en los procesos de ajuste que indican la necesidad de considerar efectos de segundo orden. Una de estas discrepancias se puede encontrar en la pendiente del ruido *flicker*. Los espectros de ruido *flicker* de los datos experimentales mostraron pendientes del estilo $1/f^{\alpha}$ con un $\alpha \neq 1$. Esta pendiente se puede reproducir utilizando un modelo que considera una distribución de trampas dentro de los óxidos variable con la profundidad. Dicho modelo ha sido aplicado a diferentes transistores y es también aplicable a transistores de efecto campo (FETs) de puerta-aislada con doble pila de puerta con dieléctricos de alta-κ. En este punto, los resultados mostraron que una dis-

tribución exponencial en función de la profundidad desde la interfaz Si-SiO_2 se corresponde con una mejor correlación entre espectros simulados y experimentales de ruido *flicker*. No obtante, no todas las muestran mostraron una dependencia de la distribución de trampas con el voltaje de puerta, lo cual implica que se podría perfectamente despreciar el parámetro de la curvatura de banda para estas muestras.

La utilidad de los modelos g-r recae en la posibilidad de calcular la contribución local de ruido en cualquier parte del dispositivo pudiendo identificar las regiones con mayores contribuciones y poder así, estimar los voltajes aplicados que minimizarían el ruido total en estos dispositivos.

También se ha llevado acabo un estudio donde se ha modificado la posición de la unión metalúrgica de las puertas laterales, lo cual nos ha permitido identificar que la puerta lateral ha de penetrar por debajo de la puerta MOS para que el funcionamiento del G4FET mejore, reduciéndose así la pendiente de la región subumbral y el ruido de baja frecuencia. Estas mejoras se deben a una reducción del volumen de la zona de agotamiento, disminuyendo el número de centros g-r, los cuales no son buenos para el funcionamiento del G4FET, ya que los centros g-r incrementan las pérdidas, pendiente subumbral y el ruido Lorentziano de baja frecuencia.

También se ha estudiado la influencia de los parámetros de las trampas en el ruido total. En esta tesis, se ha encontrado regiones de operación del G4FET donde la frecuencia de corte de los espectros Lorentzianos, originados por centros profundos en el volumen, cambia en función del voltaje de puerta. Este resultado contradice la asunción clásica de que la frecuencia de corte no varía para espectros Lorentzianos relacionados con trampas dentro de la zona de agotamiento para transistores MOS. Esto se puede explicar principalmente por el hecho de que se ha unido una estructura bipolar (una unión p-n) a un dispositivo unipolar (un transistor MOS). No obstante, para otros transistores también se han obtenido conclusiones similares.

También se ha realizado un estudio del ruido g-r producido por trampas en el volumen de un transistor totalmente agotado fabricado en tecnología silicio-sobre-aislante (FD SOI MOSFETs). El resultado más significativo es que la típica constante de tiempo asociada a la trampa depende del voltaje de puerta aplicado, al contrario del ruido g-r producido por trampas en la zona de agotamiento de transistores SOI MOSFETs de volumen o parcialmente agota-

dos. El comportamiento de esta constante de tiempo conlleva unas variaciones determinadas de la frecuencia de corte y del valor de la zona plana del espectro g-r en función de la tensión de puerta. Estas determinadas variaciones con la tensión de puerta nos permite una mejor caracterización de las trampas en transistores totalmente agotados (FD SOI MOSFETs) y, en principio, podría ser también extensible a transistores tipo 3-D $fin - FETs$. En concreto, en esta tesis se han estudiado dos estructuras fabricadas con tecnología SOI de capa de óxido enterrado ultradelgado (UTBOX) con diferentes procesados para crear los contactos de drenador y fuente. Al mismo tiempo, se ha resuelto satisfactoriamente problemas de caracterización asociados a la presencia de más de una trampa o trampas con diferentes niveles energéticos. Como un punto muy importante para futuras consideraciones es la posibilidad de llevar a cabo una espectroscopía completa de caracterizacción en estos transistores FD SOI MOSFETs con sólo variar el voltaje de sus dos puertas. Este hecho es debido a las reducidas dimensiones del transistor necesarias para alcanzar la condición de agotamiento total. No obstante, trabajar con dimensiones nanométricas implicaría tratar con efectos cuánticos.

En el capítulo 4 hemos tratado con el tercer y último tema. Aquí, nosotros nos hemos centrado en otro tema que implica tratar con herramientas de simulación para hacer frente a efectos cuánticos. Así pues, se investiga las soluciones de la ecuación de Schrödinger para nanoestructuras periódicamente ordenadas empleando para ello un simulador desarrollado por nosotros el cual considera diferentes masas efectivas para los materiales que forman la matriz y el punto cuántico. Nuestro objetivo es estudiar en dichos sistemas la absorción de fotones por electrones pertenecientes a la banda de conducción. Se han presentado resultados de la estructura de minibandas para dos tipos de nanoestructuras: puntos cuánticos e hilos cuánticos. Se han cambiado varios parámetros de las nanoestructuras para comprobar sus posibles efectos en la absorción óptica: tamaños, formas, polarización de la luz, nivel de dopado y distancias de separación entre puntos. Se ha observado la presencia de saltos en las minibandas lo cual puede ser útil en aplicaciones optoelectrónicas. En ese sentido, se han presentado resultados que pueden ayudar a aclarar la física que albergan estos sistemas.

Respecto a la implementación computacional, se han mostrado datos sobre

la convergencia de los cálculos de confinamiento y se han explorado las condiciones para obtener valores adecuados sin comprometer el tiempo de cálculo y los recursos. Nuestros resultados han sido comparados con otros obtenidos analíticamente por otros autores que han utilizado un modelo de Kroning-Penney tridimensional con diferentes masas efectivas para el punto y la barrera, concluyendo que la aproximación analítica puede ser útil sólo para casos donde la barreras sean mucho más pequeñas que los puntos cuánticos, pero inadecuadas para investigar casos generales, donde nuestra descripción sería más exacta.

Finalmente, se han llevado a cabo cálculos del coeficiente de absorción por electrones en semiconductores dopados y sin dopar y para dos orientaciones de luz polarizada incidente. Los resultados indican la existencia de un energía umbral bien definida para la cual los fotones serían absorbidos para una determinada luz polarizada, determinada por la estructura de minibandas del sistema.

Respecto a los hilos cuánticos, para los casos estudiados, con los niveles de energía de Fermi indicados, estas energías umbrales estarían alrededor de los 200 meV y serían casi independientes de la polarización de la luz. Mayores coeficientes de absorción se obtienen para puntos más grandes y para mayores separaciones entre puntos. Este comportamiento se puede atribuir a la determinada estructura de minibandas obtenida para cada caso y las relativas distancias con respecto a el nivel de energía de Fermi. Respecto a la polarización, la absorción de fotones es más intensa para una luz polarizada en la dirección [111].

La investigación teórica llevada a cabo en este tema nos sugiere que estos sistemas podrían ser de utilidad en aplicaciones optoelectrónicas debido a sus coeficientes de absorción y también a la posibilidad de eliminar los portadores excitados tras la absorción de fotones a través de su segunda minibanda. El transporte de portadores a lo largo de las minibandas es posible en estos hilos cuánticos, al contrario de lo que sucede en la absorción de fotones por impurezas o puntos cuánticos individuales. Por lo tanto, estos sistemas podrían ser útiles en la fabricación de fotodetectores de infrarrojos de puntos cuánticos (QDIPs). Además, existen indicios de que estas estructuras también podrían jugar un papel muy importante en el diseño de células solares de banda intermedia. Esto podría ser interesante para poder conseguir la ordenación periódica de los puntos para así poder obtener la estructura de minibandas e investigar las implicaciones en la utilización de diferentes materiales para el punto y la

matriz, de tal forma que se pueda encontrar el umbral deseado de la absorción para dichas aplicaciones.

Respecto a los puntos cuánticos, se ha obtenido el coeficiente de absorción en matrices de puntos cuánticos de InAs incrustados en GaAs y se ha obtenido umbrales alrededor de los 100 meV, 200 meV y 250 meV, dependiendo principalmente de la forma del punto y de la polarización de la luz. Estos umbrales están en la región del infrarrojo lejano y podrían ser de utilidad para un futuro desarrollo de fotodetectores en esta región del espectro electromagnético. Nosotros proponemos utilizar nuestras resultados para caracterizar las muestras fabricadas determinando la calidad de la ordenación de los puntos y la calidad en las formas obtenidas.

Además, se ha observado que el coeficiente de absorción tiene un umbral prácticamente independiente del volumen del punto cuántico para un rango de volúmenes de 128 nm^3 – 432 nm^3. Por consiguiente, nosotros sugerimos que las condiciones para alcanzar un cierto valor de la energía umbral debería recaer simplemente en obtener la ordenación y la forma correcta del punto cuántico en ciertas regiones de la muestra (como un material policristalino). Cambios en el tamaño del punto cuántico a lo largo de la muestra no influirían en la energía umbral, como han mostrado nuestros resultados. En resumen, la misma energía umbral sería encontrada para redes tridimensionales perfectas y para redes tridimensionales "policristalinas" con sólo cambios de volúmenes en los puntos cuánticos entre puntos diferentes dentro de la misma muestra.

No obstante, aún está abierto el estudio sobre la influencia de formas no cubicas en los puntos cuánticos ordenados, y esto sería un punto a tener en cuenta para futuras investigaciones. Añadido a esto, seria también interesante el estudio de matrices periódicas bidimensionales.

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